X20 system

User's Manual

Version: **3.20 (February 2016)**
Model no.: **MAX20-ENG**

1 General information

1.1 Manual history

Version	Date	Comment
3.20	February 2016	Book updated • Unified formatting • Updates ° Chapter "General information", section "Connecting/Disconnecting IF modules" ° Chapter "System features", section "re-LEDs" ° Chapter "Mechanical and electrical configuration", section "Safe cutoff" ° Chapter "X20 system modules", section "Data point information" ° Chapter "Standards and certifications", section "Certifications" • Combined coated and non-coated modules into shared documents. • Modified chapter "Coated modules" • Revised chapter overviews "X20 system modules" and "Coated modules" Existing module groups updated • Analog input modules • Digital input modules • Digital signal processor modules • Other modules • Temperature modules New module group "reACTION Technology"
3.10	May 2015	Book updated Existing module groups updated • Counter modules • Motor modules • X20 electronics module communication • Digital signal processor modules Chapter "Coated modules" updated
3.00	October 2014	New edition • All chapters updated • Register descriptions added for every module The following groups of modules are still being revised; some modules have not been included in this manual or have been only partially updated: • Analog input modules • Digital signal processor modules • X20 electronics module communication • Motor modules • Other modules • Temperature modules • Counter modules The most up-to-date data sheets for the respective modules can be downloaded from the B&R website.
2.10	March 2009	Book updated New module groups added • Expandable bus controllers • Expandable bus controller system modules • X20 hub system • System modules for the X20 hub system • X20 redundancy system • System modules for the X20 redundancy system Existing module groups updated • Compact CPU system modules • Fieldbus CPU system modules • Bus controller system modules • X20 electronics module communication • Bus transmitter • Bus controller • Digital input modules • Digital output modules • Analog input modules • Temperature modules • Other modules • Counter modules

Version	Date	Comment
		Accessories added New: Appendix B "B&R ID codes"
2.00	July 2007	Book updated New module groups added • CPU modules • Compact CPUs • Compact CPU system modules • Fieldbus CPUs • Fieldbus CPU system modules • Communication in the X20 IF module • X20 electronics module communication • Digital mixed modules • Other modules Existing module groups updated • Bus modules • Terminal blocks • Bus controller • Power supply modules • Digital input modules • Digital output modules • Analog input modules • Counter modules Accessories added
1.20	June 2006	First edition

1.2 Safety notices

1.2.1 Introduction

Programmable logic controllers, operating and monitoring devices (e.g. industrial PCs, Power Panels, Mobile Panels etc.) as well as the uninterruptible power supplies have all been designed, developed, and produced by B&R for conventional use in industry. They were not designed, developed and manufactured for any use involving serious risks or hazards that could lead to death, injury, serious physical damage or loss of any kind without the implementation of exceptionally stringent safety precautions. In particular, such risks and hazards include the use of these devices to monitor nuclear reactions in nuclear power plants, their use in flight control or flight safety systems as well as in the control of mass transportation systems, medical life support systems or weapons systems.

When using programmable logic controllers or operating/monitoring devices as control systems together with a Soft PLC (e.g. B&R Automation Runtime or comparable product) or Slot PLC (e.g. B&R LS251 or comparable product), safety precautions relevant to industrial control systems (e.g. the provision of safety devices such as emergency stop circuits, etc.) must be observed in accordance with applicable national and international regulations. The same applies for all other devices connected to the system, e.g. drives.

All tasks such as the installation, commissioning and servicing of devices are only permitted to be carried out by qualified personnel. Qualified personnel are those familiar with the transport, mounting, installation, commissioning and operation of devices who also have the appropriate qualifications (e.g. IEC 60364). National accident prevention regulations must be observed.

The safety notices, connection descriptions (type plate and documentation) and limit values listed in the technical data are to be read carefully before installation and commissioning and must be observed.

1.2.2 Intended use

Electronic devices are never completely failsafe. If the programmable control system, operating/monitoring device or uninterruptible power supply fails, the user is responsible for ensuring that other connected devices, e.g. motors, are brought to a secure state.

Modules from B&R are designed as "open equipment" (EN 61131-2) and "open type equipment" (UL). They are therefore designated for installation in an enclosed control cabinet. All applicable national and international standards and guidelines, such as machinery directive 2006/42/EC, must be observed and complied with.

1.2.3 Protection against electrostatic discharge

Electrical components that can be damaged by electrostatic discharge (ESD) must be handled accordingly.

1.2.3.1 Packaging

- Electrical components with a housing
  … do not require special ESD packaging, but must be handled properly.
  (see section "Electrical components with a housing").
- Electrical components without a housing
  … are protected by ESD-suitable packaging.

1.2.3.2 Guidelines for proper ESD handling

Electrical components with a housing

- Do not touch the connector contacts on the device (bus data contacts).
- Do not touch the connector contacts on connected cables.
- Do not touch the contact tips on circuit boards.

Electrical components without a housing

The following applies in addition to the points listed under "Electrical components with a housing":

- Any persons handling electrical components or devices with installed electrical components must be grounded.
- Components are only permitted to be touched on their narrow sides or front plate.
- Components should always be stored in a suitable medium (ESD packaging, conductive foam, etc.).
  Information: Metallic surfaces are not suitable storage surfaces!
- Components should not be subjected to electrostatic discharge (e.g. through the use of charged plastics).
- Ensure a minimum distance of 10 cm from monitors and TV sets.
- Measuring instruments and equipment must be grounded.
- Probes on potential-free measuring instruments must be discharged on sufficiently grounded surfaces before taking measurements.

Individual components

- ESD protective measures for individual components are thoroughly integrated at B&R (conductive floors, footwear, arm bands, etc.).
- These increased ESD protective measures for individual components are not necessary for customers handling B&R products.

1.2.4 Transport and storage

During transport and storage, devices must be protected against undue stress (mechanical loads, temperature, moisture, corrosive atmospheres, etc.).

Devices contain components sensitive to electrostatic charges that can be damaged by inappropriate handling. It is therefore necessary to provide the required protective measures against electrostatic discharge when installing or removing these devices (see also section 1.2.3 "Protection against electrostatic discharge").

1.2.5 Installation

- Installation must be performed according to this documentation using suitable equipment and tools.
- Devices are only permitted to be installed by qualified personnel without voltage applied.
- General safety guidelines and national accident prevention regulations must be observed.
- Electrical installation must be carried out in accordance with applicable guidelines (e.g. line cross sections, fuses, protective ground connections).
- Take the necessary steps to protect against electrostatic discharges (see section 1.2.3 "Protection against electrostatic discharge").

1.2.5.1 Inserting and removing I/O modules while the controller is running

I/O modules may be connected and disconnected while the controller is running under the following conditions:

- Connectors are not allowed to carry voltages and must be removed.
- Replacing a module during operation must be supported by the software; otherwise, disconnecting a module will cause an emergency stop of the controller.

1.2.5.2 Connecting/Disconnecting IF modules while the controller is running

Unlike I/O modules, IF module CANNOT be connected or disconnected while the controller is running.

Warning!

IF modules that are connected or disconnected while the controller is running are not recognized by the CPU or bus controller and will cause the application to behave incorrectly.

1.2.6 Operation

1.2.6.1 Protection against touching electrical parts

To operate programmable logic controllers, operating and monitoring devices, and uninterruptible power supplies, certain components must carry dangerous voltage levels. Touching one of these parts can result in a life-threatening electric shock. This could lead to death, severe injury or damage to equipment.

Before turning on the programmable logic controller, operating/monitoring devices or uninterruptible power supply, the housing must be properly grounded (PE rail). Ground connections must be established even when testing or operating operating/monitoring devices or the uninterruptible power supply for a short time!

Before turning the device on, all parts that carry voltage must be securely covered. During operation, all covers must remain closed.

1.2.7 Environmentally friendly disposal

All B&R control components are designed to inflict as little harm on the environment as possible.

1.2.7.1 Separation of materials

It is necessary to separate different materials so the device can undergo an environmentally friendly recycling process.

Component	Disposal
X20 modules Cables	Electronic recycling
Cardboard/paper packaging	Paper/Cardboard recycling

Table 1: Environmentally friendly separation of materials

Disposal must comply with applicable legal regulations.

1.2.8 Organization of safety notices

Safety notices in this manual are organized as follows:

Safety notice	Description
Danger!	Disregarding these safety guidelines and notices can be life-threatening.
Warning!	Disregarding these safety guidelines and notices can result in severe injury or substantial damage to equipment.
Caution!	Disregarding these safety guidelines and notices can result in injury or damage to equipment.
Information:	This information is important for preventing errors.

Table 2: Description of the safety notices used in this documentation

1.3 Terminology

Term	Explanation
SG3	System Generation 3 (SG3) - CPUs with Motorola processors The following CPUs belong to this series: • IF161, IP161 • XP152 • CP100, CP104, CP152, CP153, CP200, CP210, CP260, CP430, CP470, CP474, CP476, CP770, CP774 • PP15, PP21, PP35, PP41
SG4	System Generation 4 (SG4) - CPUs with Intel processors The following CPUs belong to this series: • CP1583, CP1584, CP1585, CP1586, CP3583, CP3584, CP3585, CP3586 • CP1483, CP1483-1 • CP340, CP360, CP380, CP382, CP570 • PP45, PP65 • PP100/200, PP300/400 • MP100/200 • EC20, EC21 • AC140, AC141 • ARsim, ARwin, ARemb • APC620, APC700, APC810
SGC	System Generation Compact CPUs (SGC) - CPUs with Motorola processors (embedded µP) The following CPUs belong to this series: • CP0201, CP0291, CP0292 • XC0201, XC0202, XC0292

Table 3: Terminology

2 System features

2.1 Setting the standards in automation

There are many different I/O slice systems. With the X20 system, B&R continues to set standards according to its motto "Perfection in Automation". Born from experience gained from applications all over the world, numerous conversations with customers and with the aim for easier, more economical and secure usage, the X20 system is a universal solution for any automated task in machine and system manufacturing.

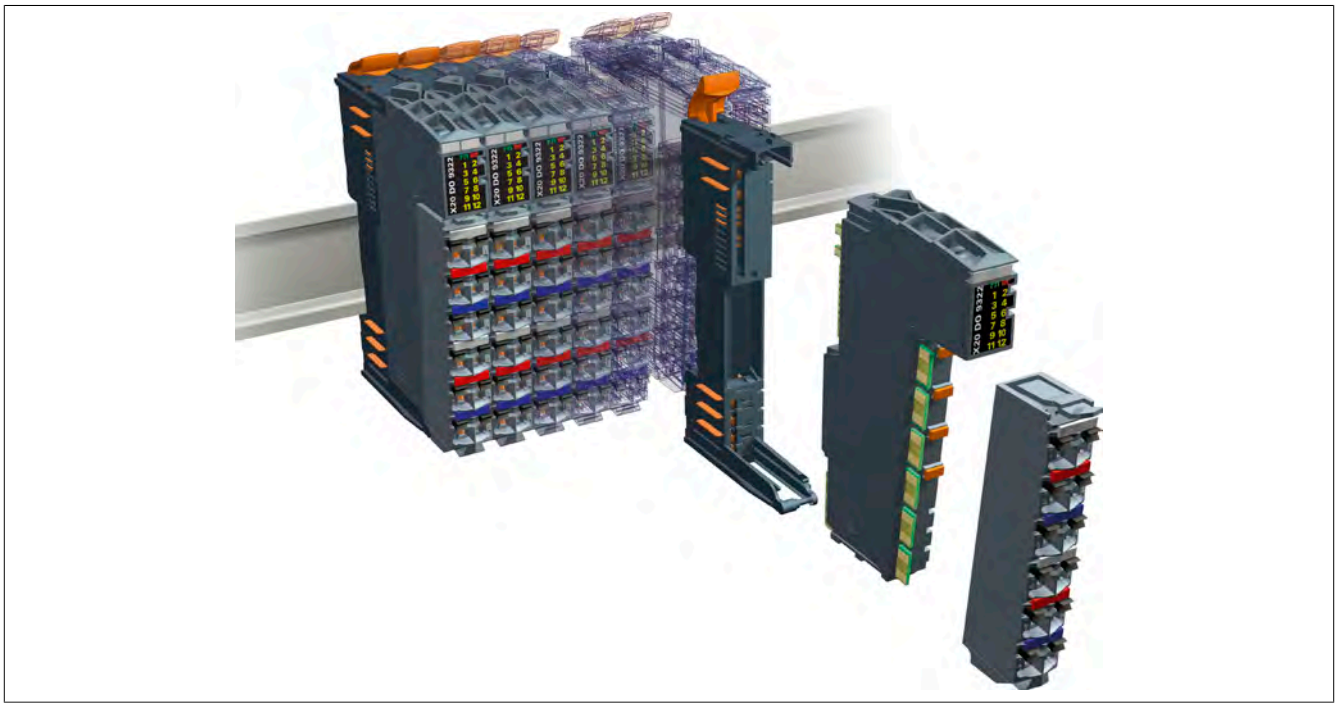


Figure 1: Each module consists of three basic elements: Terminal block – Electronics module – Bus module

2.1.1 More than just I/O

With its well thought-out details and a sophisticated ergonomic design, the X20 system is more than a remote I/O system – it's a complete control solution. The X20 system family makes it possible to combine the exact components needed to meet any application requirements.

- The X20 system is the ideal addition to a standard fieldbus and expands the possibilities of conventional control systems. Simply connect it, configure it and you're done.
- Teamed up with other B&R components, the X20 system achieves its full potential and allows the implementation of applications with unimagined performance and flexibility. This type of seamless integration is a major advantage.

2.1.2 3 x 1 = 1

Three basic elements make up one module: Terminal block – Electronic module – Bus module

This modularity results in a system that combines the advantages of both rack and I/O slice systems:

- Prewiring without the module
- Hot pluggable electronics
- Extra bus slots for added options

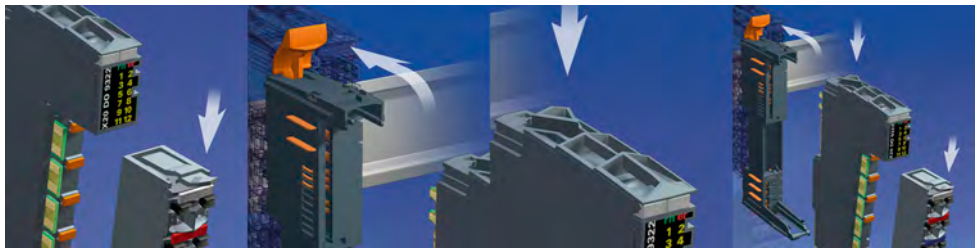


Figure 2: X20 modules are divided into three parts to guarantee the simplest usability

The X20 system delivers 50% more component density, perfected connection technology and optimal granularity.

- **Added value**
  12 channels with a width of 12.5 mm allow a component density never before achieved with optimal terminal ergonomics. As a result, the X20 system offers 50% more channels than conventional slice systems. And this without sacrificing terminal connections.
- **Uniformity**
  Consistent implementation of 1-, 2- or 3-wire connections – no additional jumper terminals needed.
- **Granularity**
  1-channel and 2-channel modules: Maximum flexibility so you only have to pay for what you really need.

2.2 Optimized design

X20 modules consist of three submodules to provide maximum ease of use throughout their entire life cycle. This division into bus module, electronics module and terminal block has several advantages.

- **Preconfigured for different machine types**
  The X20 system bus modules are the basic platform for many machine variations. The design of the machine determines which electronics modules are used. The software recognizes this design automatically and makes sure that the right functions are provided where they are needed. Handling a range of different machine variants couldn't be easier.
- **Industrial control cabinet construction**
  X20 system terminal blocks are separate from the electronics module and make it possible to pre-wire the entire control cabinet. This is especially ideal for series-produced machines.
- **Easy maintenance**
  X20 modules can be easily exchanged to simplify troubleshooting. The electronic modules can be exchanged without interrupting operation. The wiring remains exactly the same thanks to the separate terminal blocks. Being able to quickly replace automation components guarantees reduced down-time.

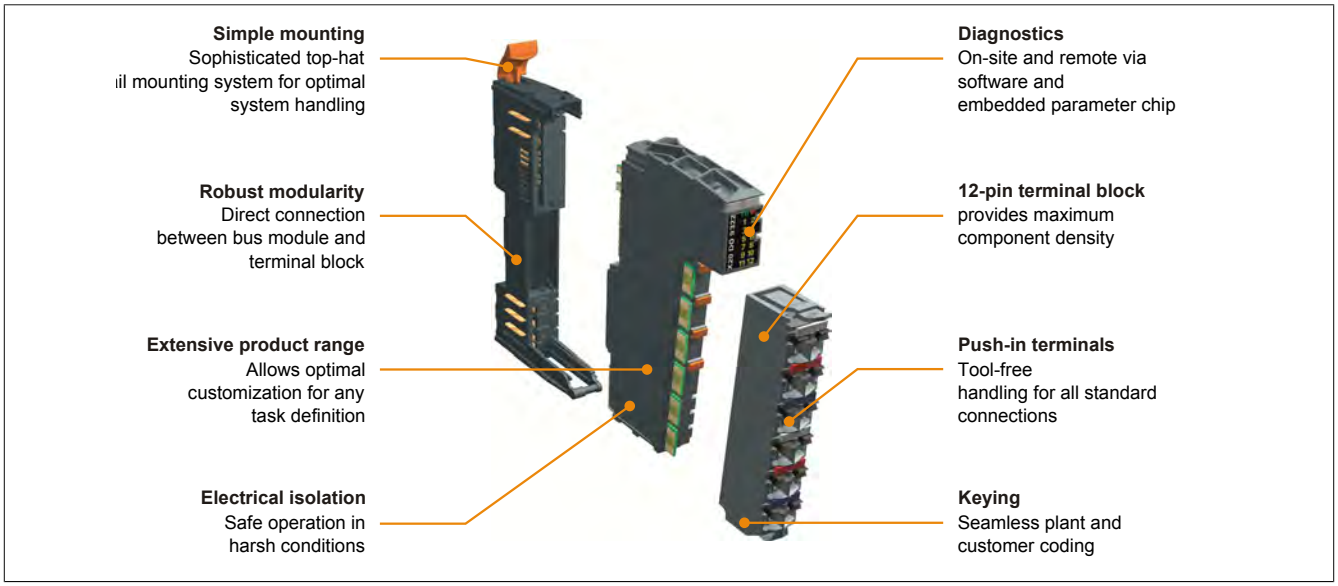


Figure 3: Features of the X20 system

2.3 Remote backplane

The main idea: Remote backplane for a rack system – in other words, the cable is the backplane. All modules are connected to the uniform backplane (X2X Link). Directly connected X20, X67 or XV modules can each be placed at a distance of up to 100 m outside the confines of the control cabinet. X2X Link guarantees the highest possible level of resistance to disturbances based on twisted copper cables.

This not only provides a universal remote backplane which handles the communication between bus modules and via the X2X Link cable, but makes it possible without converters or any loss in performance. A unique feature of the X20 is the possibility to later integrate machine options on bus modules that are not yet being used without having to change the software addressing.

Note:

A 100 m X2X Link cable is available from B&R for custom assembly (model number: X67CA0X99.1000).

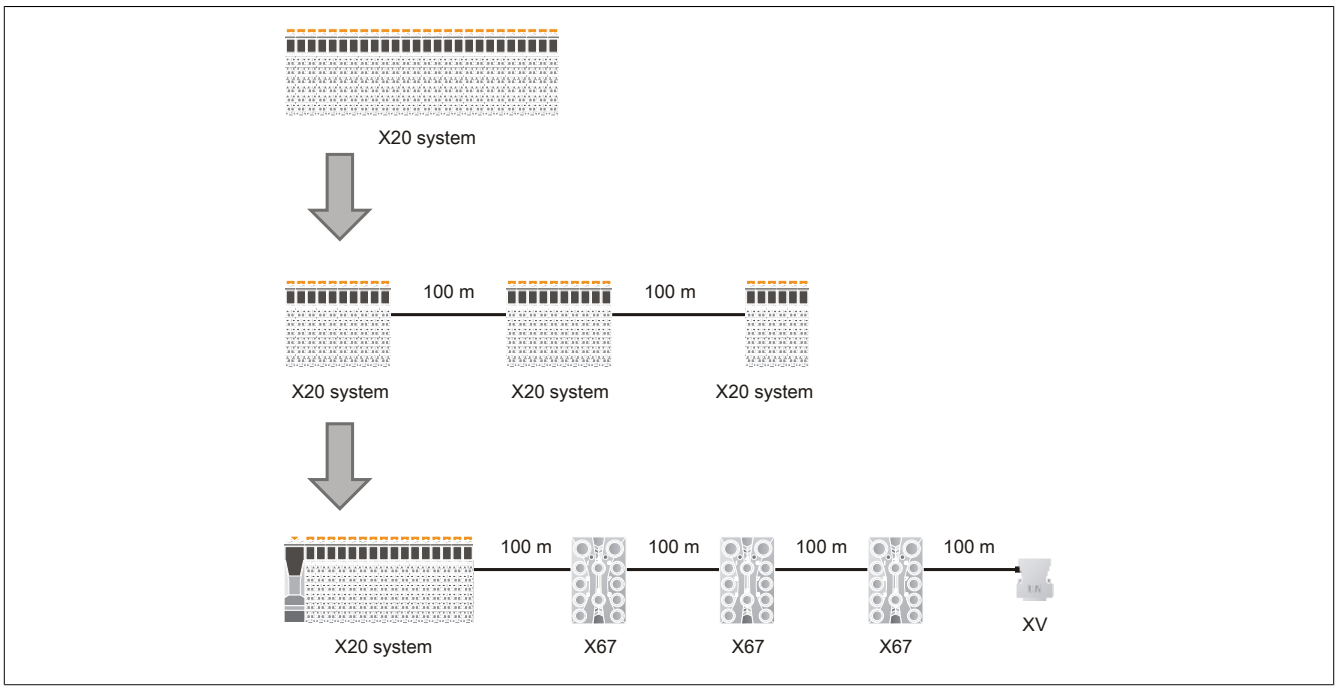


Figure 4: X2X Link - universal backplane based on twisted copper cables

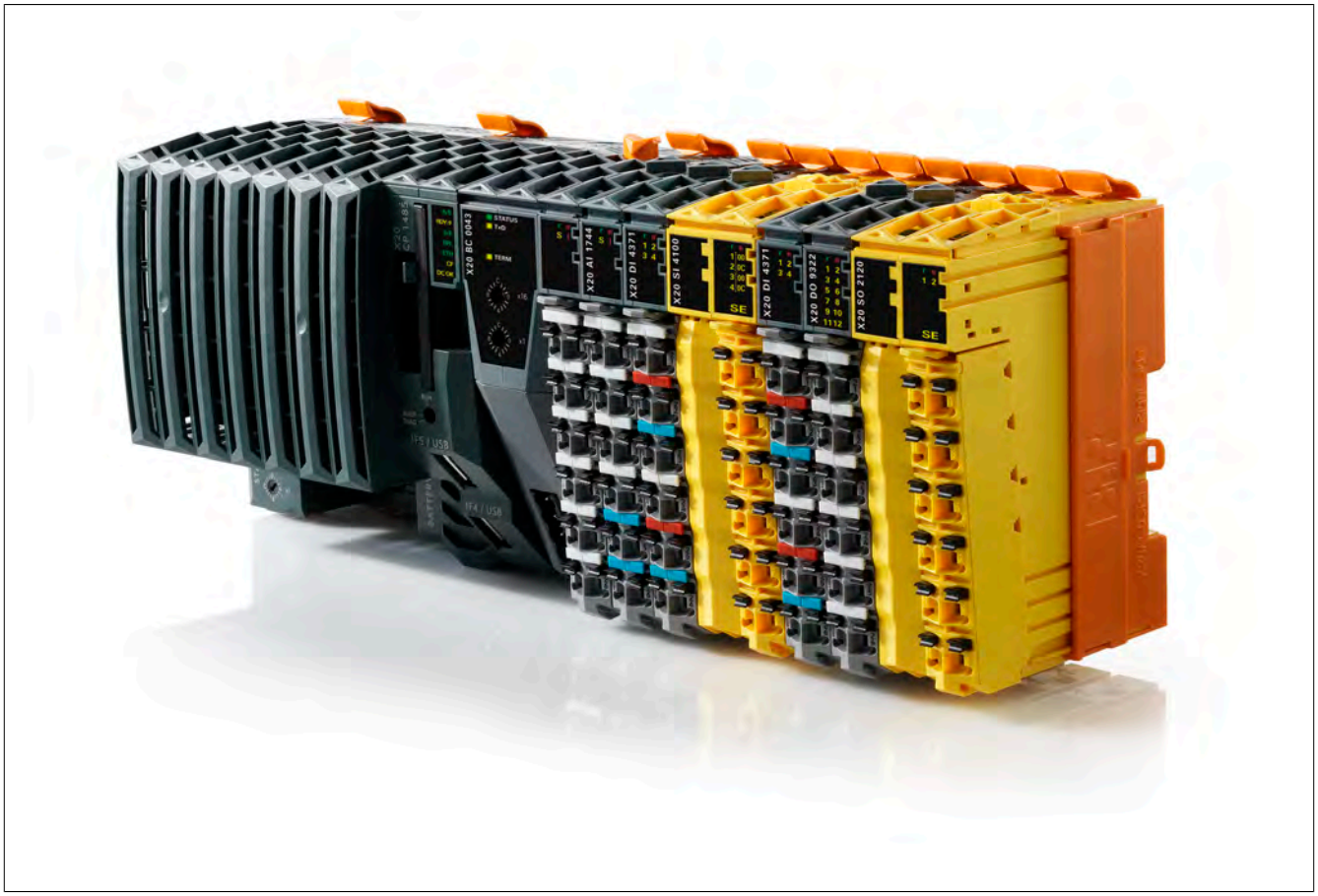
2.4 X20 CPUs

2.4.1 General information

The optimally scaled X20 system CPU line satisfies a wide range of needs. It can be implemented anywhere, from standard applications to the most demanding applications with the highest performance requirements. It can even master cycle times of 100 µs.

At B&R, RS232, Ethernet and USB are already standard equipment. Network capability and connecting USB devices are therefore possible at no additional cost. In addition, every CPU has a POWERLINK interface for real-time communication. The possibility to directly connect axes is already integrated. Although the standard features of the CPUs can handle the majority of applications, there are also up to three multipurpose slots for additional interface modules.

Because the X20 CPU was designed for top-hat rail installation in a control cabinet, up to 250 X20 I/O modules – 3000 channels – can be connected directly. This provides the highest performance as well as the advantages of the remote backplane.



2.4.2 Remote backplane

A power supply integrated in the CPU with I/O supply terminals provides power for the backplane and I/O sensors and actuators, eliminating the need for additional system components. With a direct I/O connection to an X20 CPU, you get all the advantages of the remote backplane, i.e. the ability to repeatedly place I/O line sections anywhere within 100 m using a cable or to add modules with IP67 protection.

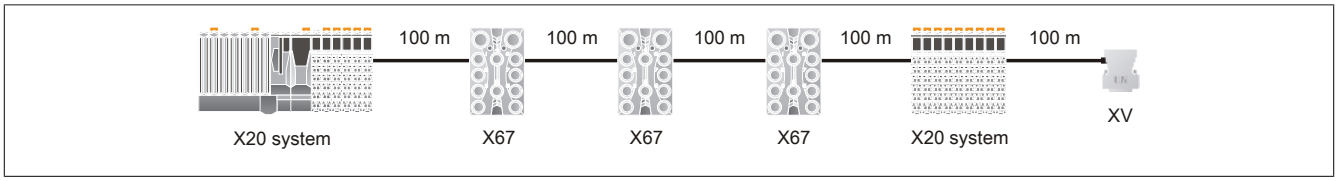


Figure 5: X20 CPUs - Direct I/O connection to X20 CPU and advantages of remote backplanes

2.4.3 B&R Automation Studio

B&R Automation Studio is the only programming tool needed for all platforms. It can be used to create application software in all relevant IEC 61131-3 languages as well as C. Integrated visualization, NC and soft CNC functions and web server technologies complete the range of powerful features.

2.4.4 PC-based technology

Based on the latest Intel ATOM™ processor technology, X20 CPUs can effectively utilize cycle times down to 100 µs.

An extensive amount of RAM provides the user with unlimited freedom when it comes to application development. This is complemented by battery-backed nonvolatile SRAM for task-specific data and remanent variables. In the case of a power failure, variables that have been declared as being remanent are automatically copied from the fast RAM to the secure SRAM. Data contents are therefore retained after the controller is restarted so that the process can simply be resumed. A slot for a CompactFlash card is also integrated into the system to hold program memory or application data such as recipes.

2.4.5 Suitable for industrial use

Providing the highest performance, with many standard interfaces and interface modules for expansions, yet the dimensions are unbelievably compact. The dimensions of the CPU match those of the X20 modules, which prevents unnecessary waste of space in the control cabinet.

Fanless operation - a demand the X20 CPUs can satisfy. None of the processors require a fan, which makes them virtually maintenance-free.

2.5 X20 Compact CPUs

2.5.1 General information

With a width of 37.5 mm the X20 Compact CPUs are extremely compact, yet surprisingly powerful. Less powerful than the PC-based CPUs, there are several models of Compact CPUs available in 2 performance classes.

Compact CPUs are ideal for situations where cycle times in the millisecond range are sufficient and a cost-benefit analysis plays a decisive role. A range of models with CAN bus and Ethernet can be perfectly adapted to all requirements, resulting in extremely sleek automation solutions.

The Compact CPU's design and dimensions correspond to the X20 system. The X20 I/O modules are connected directly to the CPU. These are attached seamlessly to the CPU, making the entire system an extreme space saver in the control cabinet. Despite the sleek profile, the CPU supply, the X2X Link supply, and the I/O module supply are integrated in the system. No additional power modules are necessary.

All CPUs have at least two things in common: multitasking capability and programming with B&R Automation Studio using all relevant IEC61131-3 languages and C.

2.5.2 Product range

The many different variants start with the most space-saving solution, the X20 compact CPU. This module is equipped with an RS232 online interface and an integrated X20 module connection. Selecting another bus module also provides an additional onboard CAN bus interface. The upper end of the product range is characterized by CPUs with a Fast Ethernet interface. The variant with Ethernet is also available with approx. 60% more processing power.

Figure 6: X20 compact CPUs

2.6 X20 Fieldbus CPUs

2.6.1 General information

Remote design of I/O systems is one of the standard topologies used in automation solutions for machines and equipment. In addition, fieldbuses with bus controllers are normally used. Larger topologies or standard fieldbuses like CANopen, PROFIBUS DP, or DeviceNet can cause relatively long response times.

An input must travel via the bus controller to the CPU before it is processed. The output data must then return on the same path. This is sufficient for most I/O functions. However, this response time is too long for some functions. The best solution is for the bus controller to process the data. This type of data preprocessing is usually associated with limited CPU functionality in the programmable bus controller.

Fieldbus CPUs with integrated fieldbus connections overcome these limitations. Fieldbus CPUs are variations of Compact CPUs. In addition to these features, there is also the option of connecting fieldbus modules to the left side. The full CPU functionality of the Compact CPUs plus a plug-in fieldbus module create many more possibilities than simply data preprocessing. There are enough reserves for relatively complex application processing. Intelligent substations are another area of use. That means a part of the machine part must continue to function, even when separated from the main controller.

Based on the Compact CPU platform with up to two plug-in interface modules for the respective fieldbus connection, this results in a very compact (62.5 mm and 87.5 mm), powerful and intelligent fieldbus controller.

Figure 7: Fieldbus CPU with connected interface module

2.6.2 Product range

As with the Compact CPUs, the new CPUs with fieldbus connection are available in two performance classes. Depending on the bus module being used, the CPU has an RS232 interface or an RS232 interface plus a CAN bus interface. The CPU with higher processing power is available with or without an onboard Ethernet interface. Various fieldbus modules are available.

2.6.3 Programming

All CPUs have several features in common, including integrated connection of X20 modules and system multitasking capability. With B&R Automation Studio, programming can be done in all IEC 61131-3 languages and in C.

2.7 For all fieldbuses, integration through standardization

The X20 system is ideally suited for expanding existing control systems using standard fieldbus technology.

For example, a bus controller allows the X20 system to be used as a powerful I/O expansion unit. Standardized EDS or GSD description files allow X20 system components to be integrated, configured, and programmed in the programming environment of a non-B&R system.

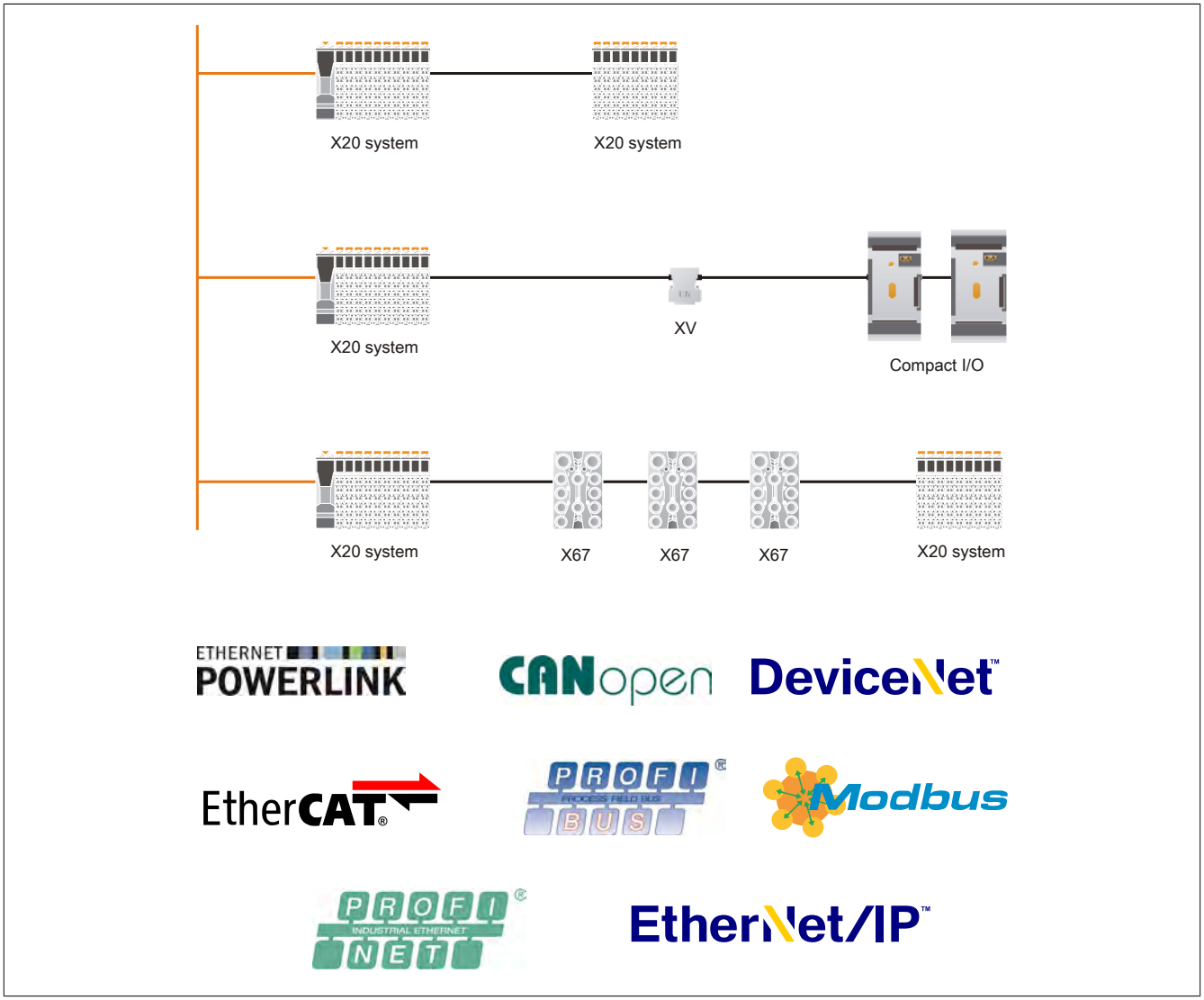


Figure 8: Expansion of existing control systems using standard fieldbuses and the X20 system

2.8 Complete system

2.8.1 IP67 - then X67

The X67 is the robust version of the X20 for use outside the control cabinet. The same basic technology, with an extremely robust housing and 4 to 32 channel modules, guarantees economical solutions in the roughest conditions.

2.8.2 Integrated valve terminal control

The development of the XV system allows for the first time direct and manufacturer-independent control of valve terminals. A complete digital output module in a size and form comparable with a normal DSUB connector. XV allows any valve terminal manufacturer to be selected because it is connected directly to the standardized multiple pin connector on the valve terminal.

Fully integrated in the remote backplane, it rounds off the X20 and X67 for complete automation solutions. One system, several variations - advantages that pay off. You select your automation components and distribute them as needed inside and outside the control cabinet.

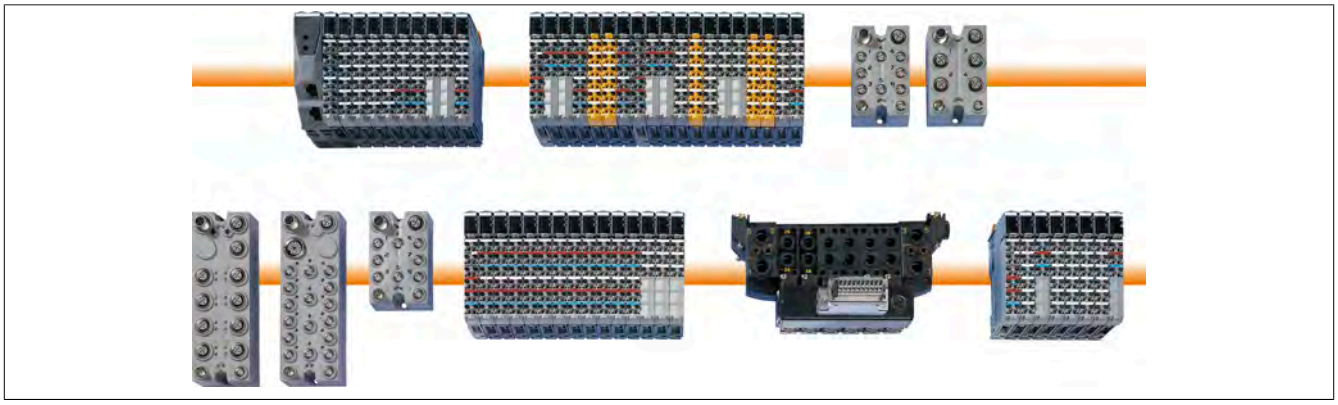


Figure 9: X20, X67, XV - variations of a single system

2.9 Easy wiring

Industrial control cabinet construction streamlines production cycles. Prefabricated cable trees enable faster and easier assembly directly on the machine or system. The X20 system supports efficient prewiring of the entire control cabinet using separate terminal blocks. The complete X20 system configuration is mounted in the control cabinet and connected to the prewired cable trees.

The supply of the X20 modules and the supply of the sensors and actuators do not add any requirements for energy distribution. The X20 system reduces manual wiring to a minimum.

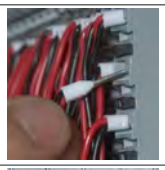
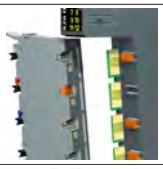
2.9.1 Install the wires, plug it in, and it's ready to go

Simple, tool-free wiring for fast installation. The X20 system terminal blocks use a fully integrated and proven push-in connector system. Each terminal can also handle double wire sleeves up to a diameter of 2x 0.75 mm². The user saves time wiring the system multiple times and distributing the signals.

The wire connections can be removed with a screwdriver. Each terminal also has an access point for a measurement probe. A great deal of thought was given to designing every aspect of the X20 system. Right down to the wire connectors.

Information:

To avoid damaging the terminals, the X20AC0SD1 B&R screwdriver should be used.

	**Detached** The terminals can be prewired apart from the actual I/O module. This provides many advantages for control cabinet construction. Separate manufacturing, just-in-time logistics and the installation of preassembled systems during start-up become reality.		**Tool-free** Simple, tool-free wiring for fast installation. The X20 system terminals use a fully integrated and proven push-in connector system. Available with 6-pin and extremely compact 12-pin terminals.
	**Coded in the system** Factory coding prevents dangerous mix-ups. Coding guarantees that only parts which are permitted to be combined can be combined. Intuitively and without additional work.		**Ergonomic** Component density does not have to negatively affect ergonomics. With terminal spacing of more than 5 mm, this was handled optimally on the X20 system. Experience gained in the field - used in the field.
	**Coded in the application** Incorrectly inserting terminals does not necessarily damage the electronics, but always causes faulty functioning of the system. Application coding prevents this problem.		**Unmistakable** Distinct forms intuitively define various functions, such as clearly assigned latching and unlatching functions for terminals. This prevents errors from the very beginning.
	**Labeling** Each terminal is clearly labeled, directly in the plastic. Additional label tags are available as system accessories including a printer with ECAD connection.		**Easy servicing** A system's strengths can be seen in its details: In addition to the terminal connector and unlocking mechanism, each terminal has an access point for a test probe. You can easily measure the terminal potential without disconnecting the wire.

2.10 Sophisticated mechanics

The name B&R stands for many years of experience in developing and manufacturing industrial electronics. But it's also the mechanics of the X20 system that have been thought through to the last detail. Its robust design, long guides and strengthened housing guarantee the stability it needs in industrial environments. These features allow the X20 system to be mounted on a top-hat rail with the same ease as a rack system. They also make it just as simple to remove it from the rail.

The sophisticated mechanics of the X20 are needed not just to provide this type of handling, but also to be able to quickly and easily remove I/O slices from the entire system.

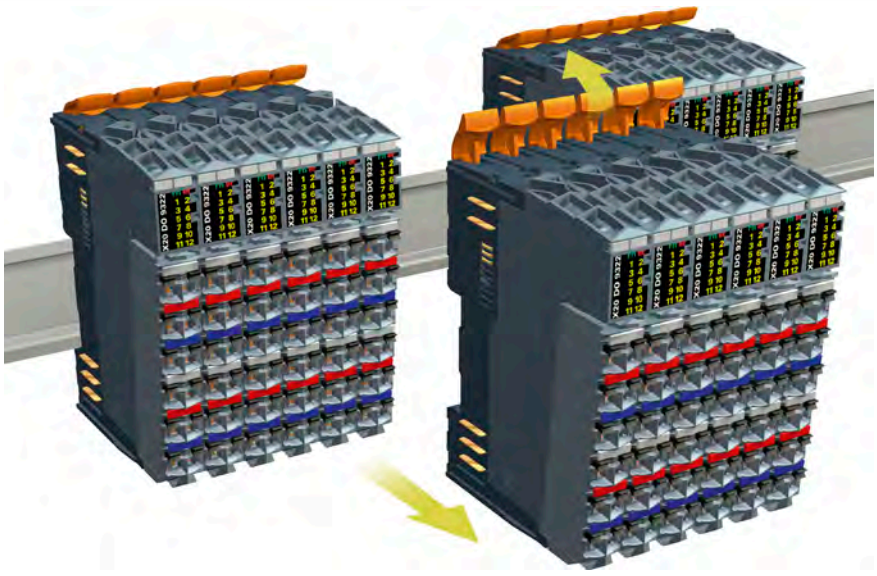
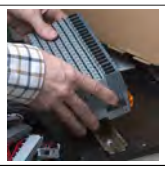


Figure 10: Easy mounting on and removal from the top-hat rail

	**Unlocking mechanism with two positions** Closed for secure fit on the top-hat rail.		**Defined open position makes the difference** Open to remove a module or the entire system.
	**Removing a single module from the system** Remove or reconnect vertically.		**Mount the entire system as a whole** Or just as easily removing the entire system.

2.11 Diagnostics

Outstanding diagnostic options are needed for errors to be found quickly. The X20 system offers several levels of diagnostics:

- Direct on the module using visual LED displays. Bus status, I/O status and channel states are displayed in direct relationship to the channels or the function. The different states are displayed in different ways, e.g. green for OK, red for error.
- Via software in the cyclic data image. With the X20 system, status data does not result in an additional communication load, which would result in considerable differences between theoretically possible bus speeds and real requirements during operation. All necessary status data is always transferred cyclically, with no exceptions.
- Expanded diagnostic data in acyclic data traffic without loss in performance. If a problem occurs, detailed diagnostic data can be requested from the application by the respective module using an asynchronous channel. This does not result in additional communication load and cycle times remain unchanged.

Figure 11: Visual diagnostics directly on the module using LED indicators

2.11.1 re LEDs

Most X20 I/O modules have LEDs for diagnostics at the top.

The operating state of the module firmware is indicated by the two topmost LEDs "r" (green) and "e" (red). The operating state can also be indicated with the help of special LED status indicators (e.g. on the X20ATC402 module).

Additional LEDs depend on the module and generally indicate the status of I/O channels. Green LEDs are usually used for inputs, while orange is used for outputs. These I/O LED status indicators are only operational in RUN mode on some modules.

Operating states and error states

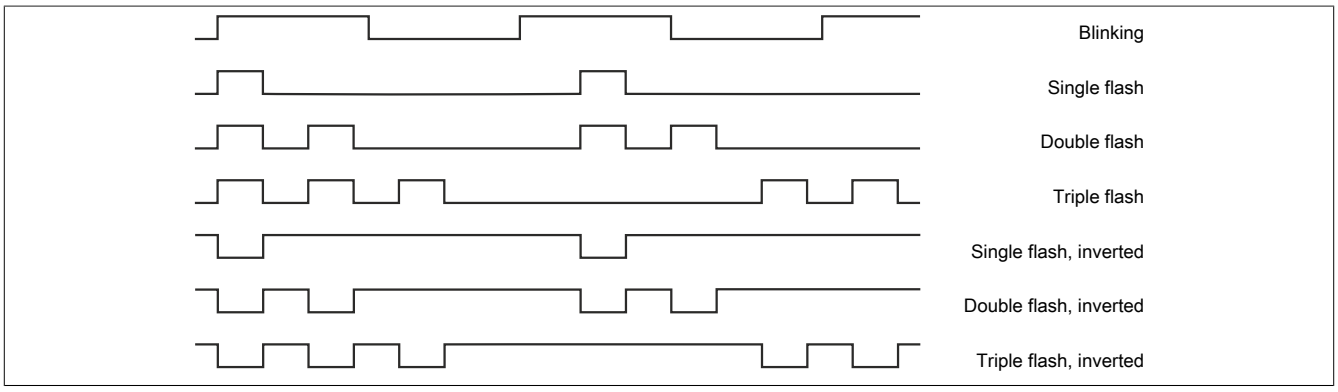
The following table provides a complete description of all operating states and error states for X20 I/O modules. The operating state and error state actually indicated by the I/O module depends on the type of module as well as how it is being used.

	LED	Description	Note
	"r" and "e" off	No power to module	Module does not have power.
	Module status LED "r"		
	Single flash ("e" = Off)	RESET mode	No connection to the X2X Link master, or the X2X Link master is not yet running. Some modules remain in single flash mode during a firmware update.
	Single flash ("e" = On)	Firmware is not valid	Invalid firmware: Occurs when a firmware update has been interrupted. The firmware is reloaded as soon as the X2X Link master is active again. It is only loaded if the module is also entered in the configuration, however.
	Double flash	BOOT mode (RESET mode with communication)	Firmware update. A firmware update usually only takes place once after the module has been replaced or if new firmware has been loaded to the master CPU during a project update. **Depending on the configuration, a firmware update can take several minutes.**
	Blinking	PREOPERATIONAL mode	Modules whose slot is configured for a different module (or none at all) remain in PREOPERATIONAL mode. Possible error: • Incorrect module connector or slot not configured • Incorrect slot number for bus modules with node number switches
	On	RUN mode	No error
	Error status LED "e", if "r" = On		
	Off		Everything OK
	On	Fatal error	It is not possible for the module to continue functioning correctly. Possible error: • Power supply outside warning range • Operating temperature outside permitted range **Monitoring for fatal errors is not integrated into all modules.**
	Single flash or blinking	I/O channel error	An error or warning is present on one or more I/O channels. Which channel error on the module is being indicated depends on the module and can be determined with the respective module description.
	Double flash	System errors	A system error occurred in the module. The cause of error depends on the module and can be determined with the respective module description.
	Triple flash	I/O error and system error	An I/O error and system error occurred at the same time.
	Single flash inverted[1)]	Fatal error and I/O error	A fatal error and I/O error occurred at the same time.
	Double flash inverted[1)]	Fatal error and system error	A fatal error and system error occurred at the same time.
	Triple flash inverted[1)]	Fatal error, I/O error and system error	A fatal error, I/O error and system error occurred at the same time.

1) Only on modules that monitor for fatal errors.

LED status indicators - Flashing sequences

The flashing sequences shown in this image specify only the principle ratio between the switch-on and switching-off times for the LED. The actual ratio of blink times to each other can vary depending on the module.



2.12 Embedded parameter chip

Information such as module type, serial number, functionality and version number is contained in the embedded parameter chip of the X20 module. This information is automatically evaluated by the programming environment (Automation Studio) and by the application program. This prevents errors during both commissioning and service. In addition, the system configuration is automated and flexible variations are made possible.

Serial numbers of modules that are defined worldwide are gaining increasing significance in validated systems as demanded, for example, by the FDA.

2.13 Space for options

The X20 system family makes it possible to combine the exact components necessary depending on the user's demands and individual application requirements. This allows machine options to be implemented easily and flexibly. Bus modules provide the base, and are more or less a rack replacement. Depending on the option, the necessary electronics modules are then inserted in the predefined slots.

Addresses are assigned implicitly via the slot. Software that has been developed once is valid for all versions and does not need to be changed. This is even possible for later machine expansion. The I/O modules are simply inserted in the defined bus modules, and assigned to the corresponding potential groups and E-stop groups.

To prevent unwanted expansion, each module can be identified and then enabled using the application software.

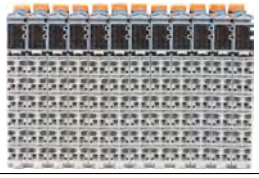
2.14 Flexibility for options

The implementation of different machine variations using free bus modules is only one of the many features that the X20 system offers. With the support of B&R Automation Studio, there is an optimized solution using I/O mapping. What does this mean?

Each I/O configuration is created optimally according to the actual requirements. However, the application software is designed to handle all potential options. Only the I/O channels that are actually available are configured in the application program. If an expansion is required, then the additional hardware needed can be easily connected and the I/O mapping changed. This is done without having to compile the application software.

It doesn't matter where the I/O mapping list is created:

- Manually in B&R Automation Studio
- With tools, e.g. with a database or a table calculation program
- Directly from an ERP system, just like the parts list for the machine
- Automatically in the application software, depending on the hardware used

	**Machine variation A** The possibilities of the X20 system can be best explained using examples. This is a machine constellation with two variations, A and B. All of the necessary electronics modules for machine variation A are shown in the picture to the left. The bus modules needed for variation B are also present, but without electronic modules.
	**Machine variation B** Variation B shows the necessary electronic modules but the modules necessary for variation A are missing. The distribution of the free bus modules for the variations is also clear: The variable I/O modules can be very easily connected to the required electrically isolated groups and don't need to be attached in the back. The extensive process of taking apart the configuration to expand existing electrically isolated groups is also eliminated. Simply insert the electronic module and attach the terminal block.
	**Machine variation A - optimized** The features included in Automation Studio can also be used to achieve completely optimized hardware configurations without losing the advantage of comprehensive application software for all variations. As described earlier, simply mapping physical I/O points to the application program makes it extremely easy to optimize the hardware variations without even requiring compilation.

2.15 Configurable X2X Link address

The remote X2X Link backplane, which connects the individual I/O modules with each other, is set up to be self-addressing. Because of this, it is not necessary to set the node numbers. The module address is assigned according to its position in the X2X Link line.

In certain cases, e.g. when configurations of modular machines change, it is necessary to define specific module groups at a fixed address, regardless of the preceding modules in the line.

For this purpose, there are modules in both the X20 system and the X67 system with node number switches that allow you to set the X2X Link address. All subsequent modules refer to this offset and use it automatically for addressing purposes.

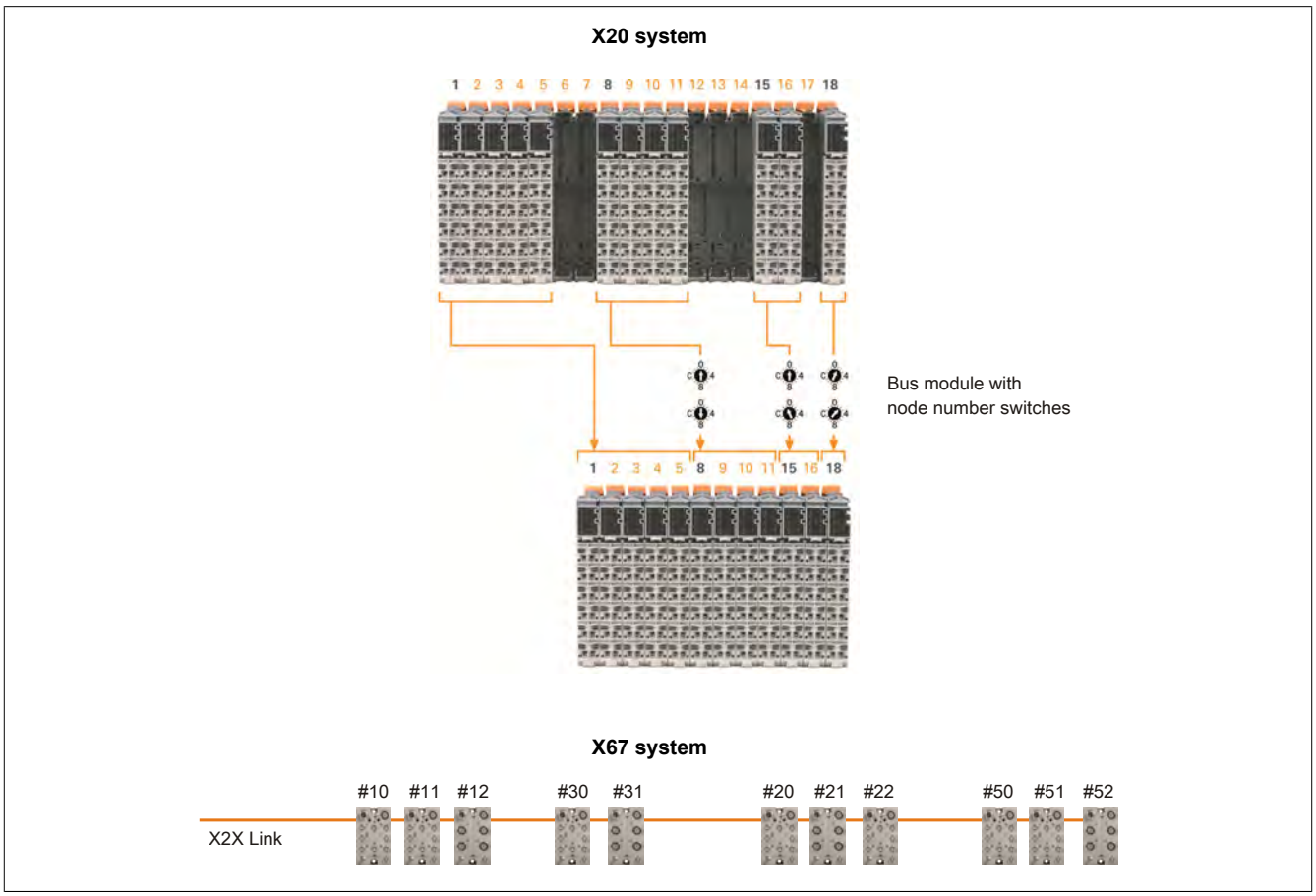
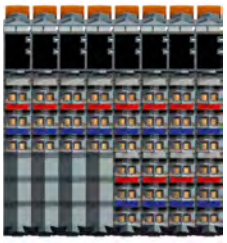


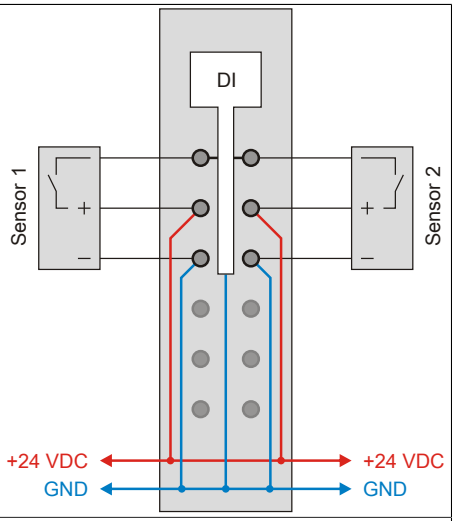
Figure 12: Setting the X2X Link address

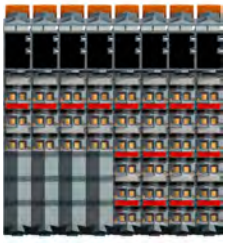
2.16 Universal 1, 2, 3-wire connections

Consistent connection types for all requirements – no additional jumper terminals are needed. All connection types can also be mixed and matched.

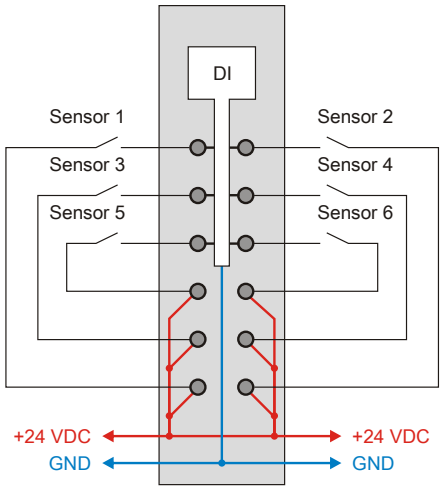


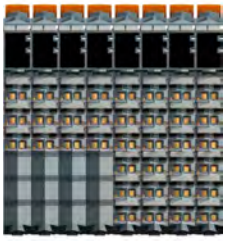
Universal 3-wire connections
Integrated supply and ground for sensors and actuators.



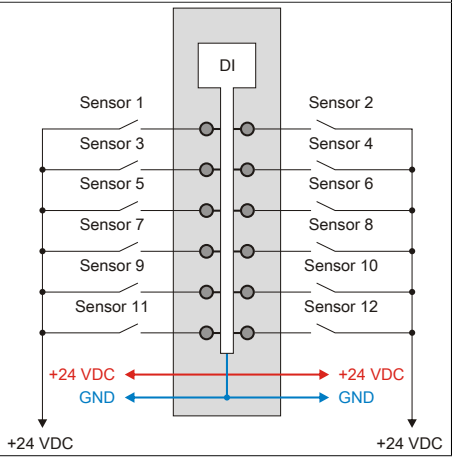


Universal 2-wire connections
No extra terminals needed.





Universal 1-wire connections
12 channels - unequaled component density



2.17 Coated X20 system

The X20 system includes modules with a protective coating for the electronics. These modules are suitable for use in adverse atmospheric conditions and are protected against condensation and corrosive gases.

Data sheets can be found under 5 "Coated modules".

2.18 Redundancy

The X20 system provides the following forms of redundancy:

- Controller
- Network
- Power supply modules for X20 standalone devices and expandable POWERLINK bus controllers
- X2X Link supply

The first three areas are covered in the "Redundancy for control systems" user's manual. The user's manual is available in the Downloads section of the B&R website www.br-automation.com.

For a description of the redundant X2X Link supply, see section 3.20 "X2X Link supply".

2.19 reACTION technology

The X20 Compact CPUs and a number of I/O modules are available featuring ultrafast reACTION technology. This allows the I/O channels integrated in the reACTION module to be controlled with response times down to 1 µs. This new approach allows extremely time-critical subprocesses to be managed using standard hardware – which lowers hardware costs by reducing the load on the controller and allowing it to be scaled down.

All of the commands that can be used for reACTION programs are provided as function blocks in special libraries (e.g. AsIORTI). Programming using the standard Function Block Diagram (FBD) editor in Automation Studio is compliant with IEC 61131-2.

Documentation for reACTION technology is included in the Automation Studio help system.

2.20 X20 system configuration

The X20 system is designed so that can be connected to standard fieldbuses (with a bus controller) or the remote X2X Link backplane (with a bus receiver). The connection to the next station is made with a bus transmitter. Supply modules and I/O modules are placed between the bus receiver or bus controller and the bus transmitter as needed.

The power supply system used in the X20 systems is described in the section 3.8 "The supply concept".

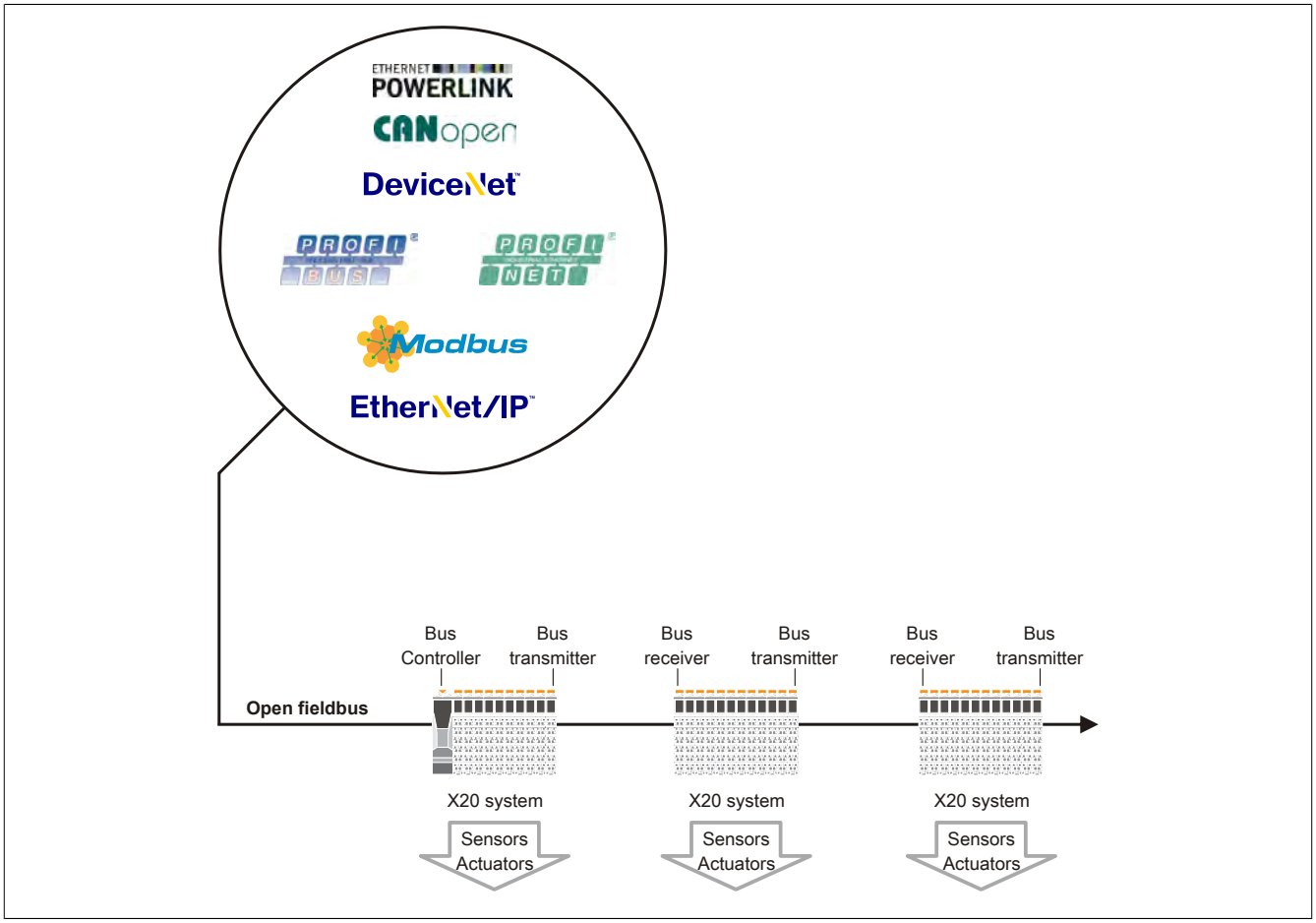


Figure 13: X20 system configuration

2.20.1 Fieldbus connection

Several bus controllers for standard fieldbus technologies like POWERLINK, DeviceNet, PROFIBUS, CANopen, ModbusTCP or EtherNet/IP are available to connect X20 modules to existing control systems. Fieldbus configurators transparently integrate the X20 system into the 3rd-party development environment.

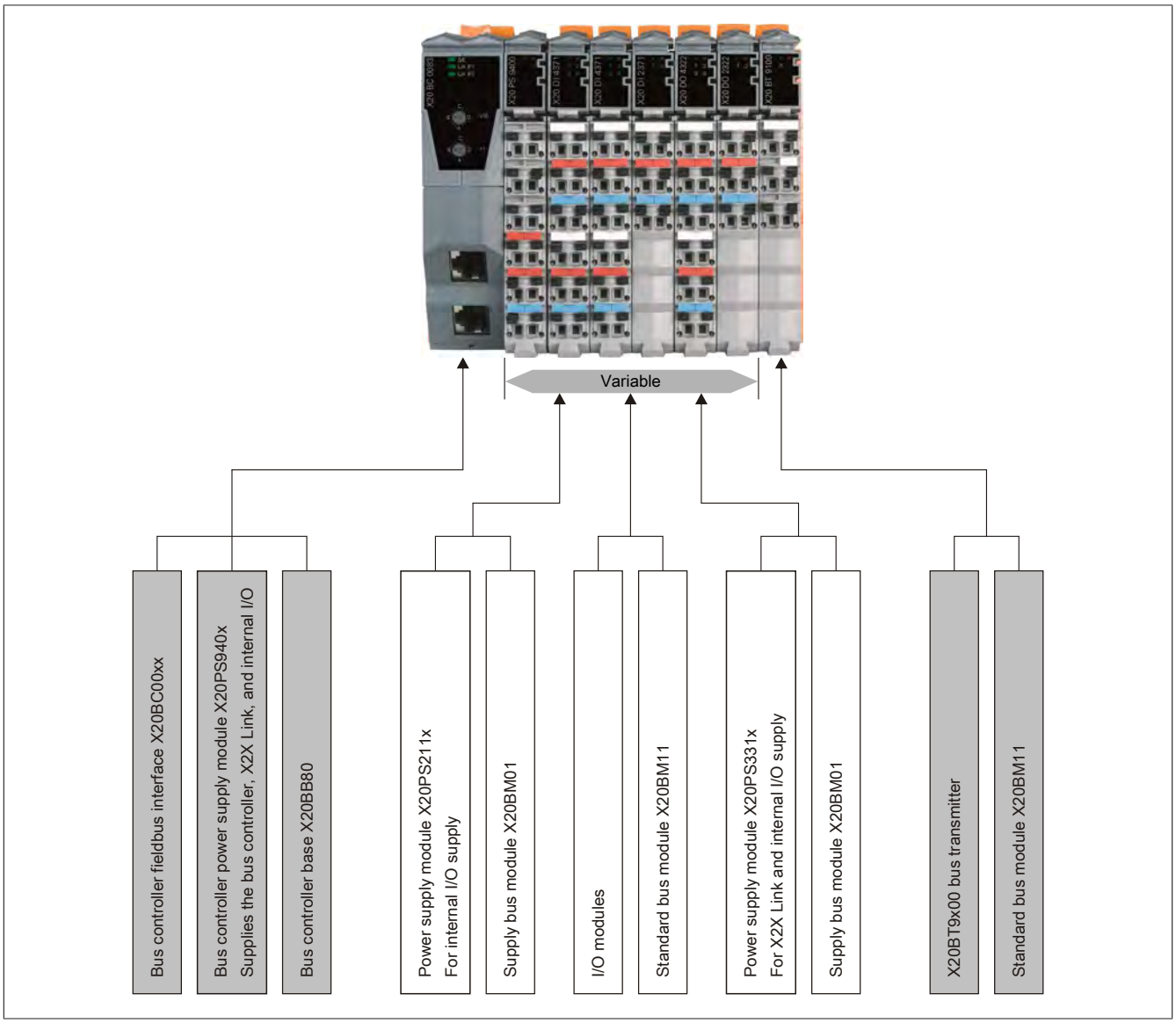


Figure 14: X20 system configurator for fieldbus connection

2.20.2 Connection to X2X Link backplane

The bus receiver X20BR9300 is used to connect the X20 system directly to the remote X2X Link backplane.

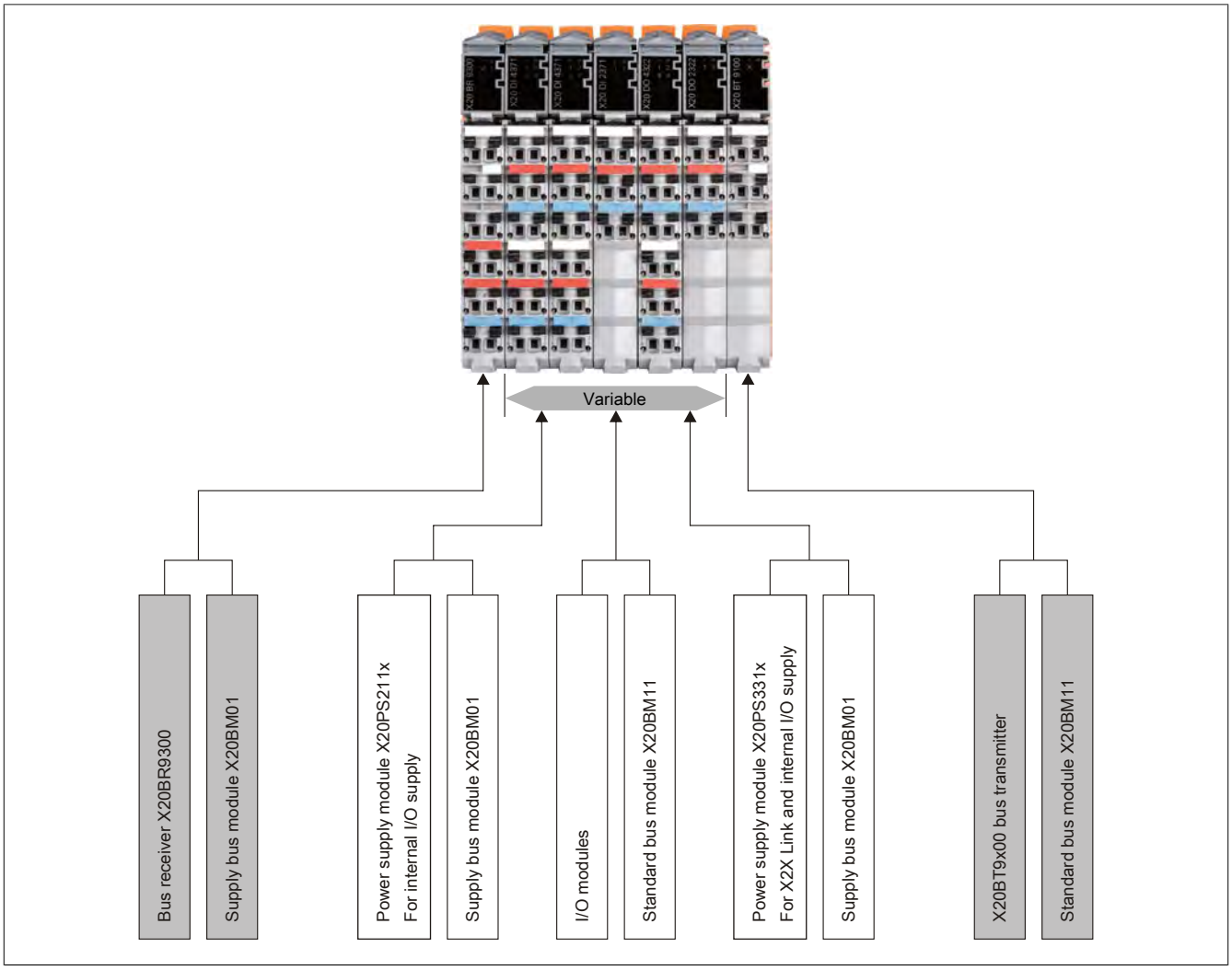


Figure 15: X20 system configurator for connection to X2X Link backplane

3 Mechanical and electrical configuration

3.1 Dimensions

3.1.1 X20 CPUs with one slot for interface modules

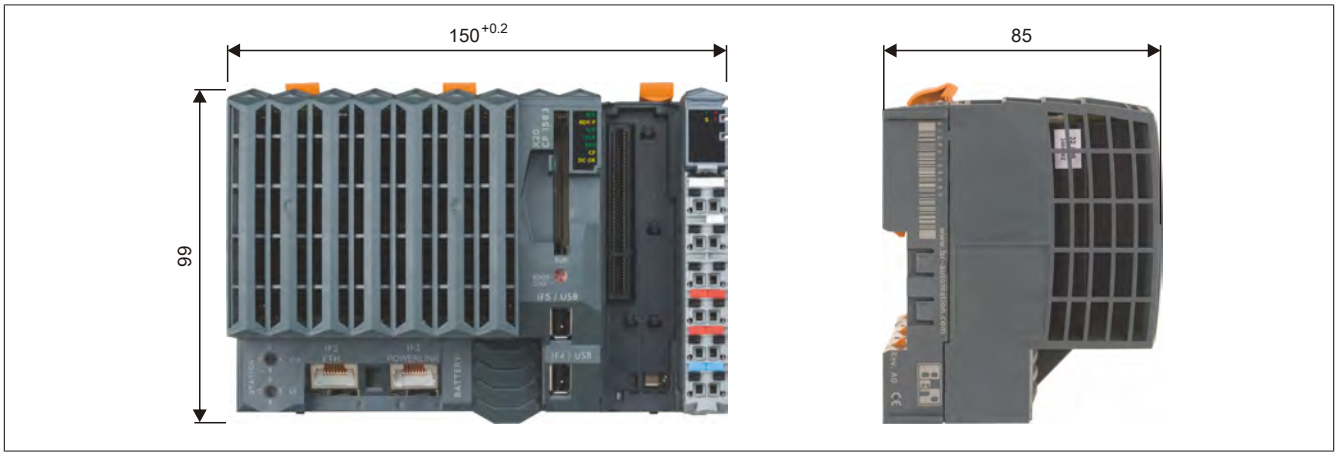


Figure 16: Dimensions of the X20 CPUs with one slot

3.1.2 X20 CPUs with three slots for interface modules

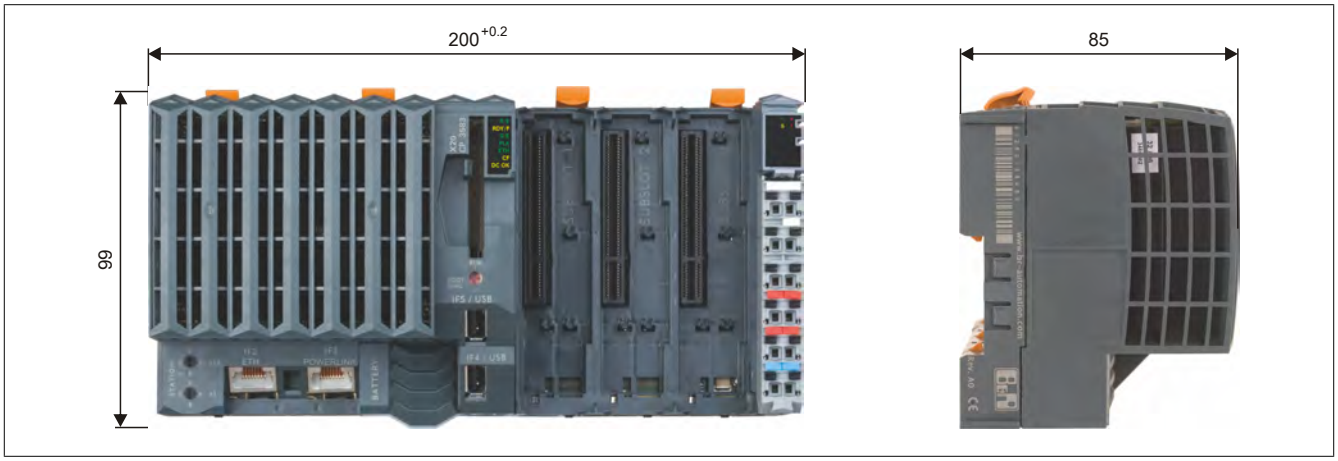


Figure 17: Dimensions of the X20 CPUs with three slots

3.1.3 Compact CPUs and bus controllers

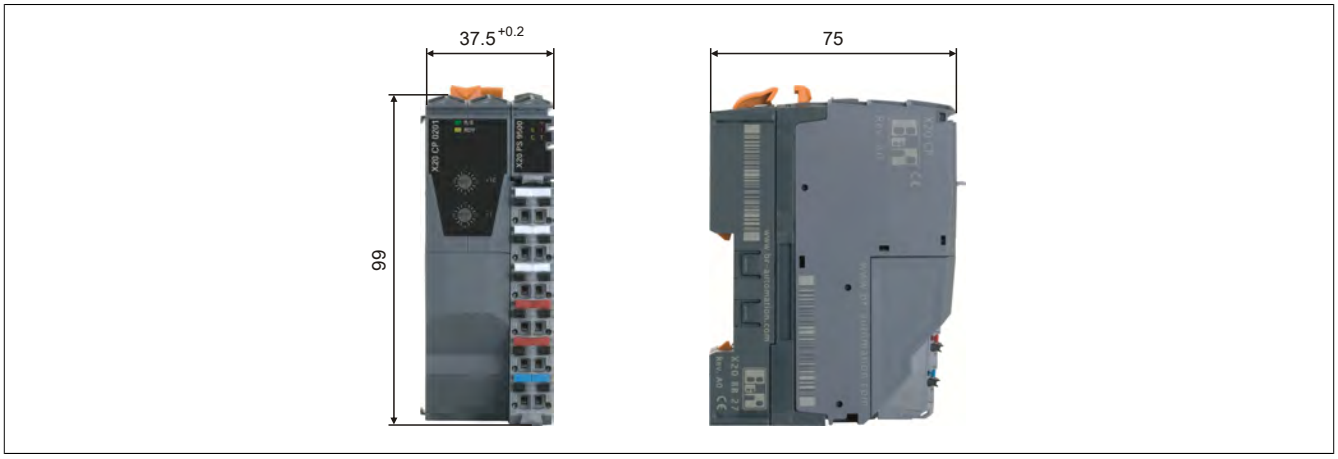


Figure 18: Dimensions of the compact CPUs and bus controllers

3.1.4 Fieldbus CPUs and expandable bus controller

3.1.4.1 With an additional slot

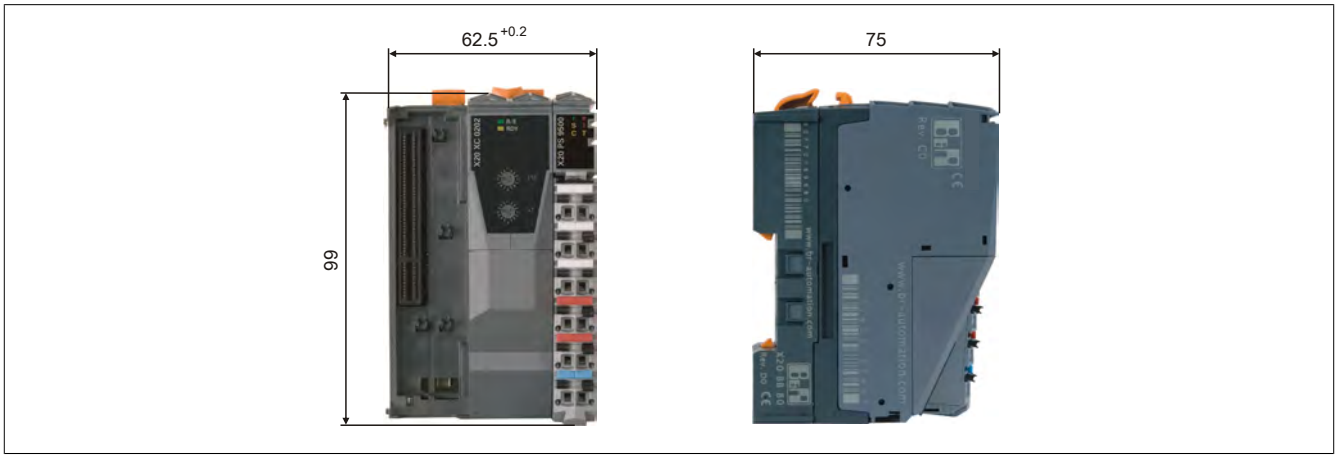


Figure 19: Dimensions of the fieldbus CPUs and expandable bus controller with one additional slot

3.1.4.2 With two additional slots

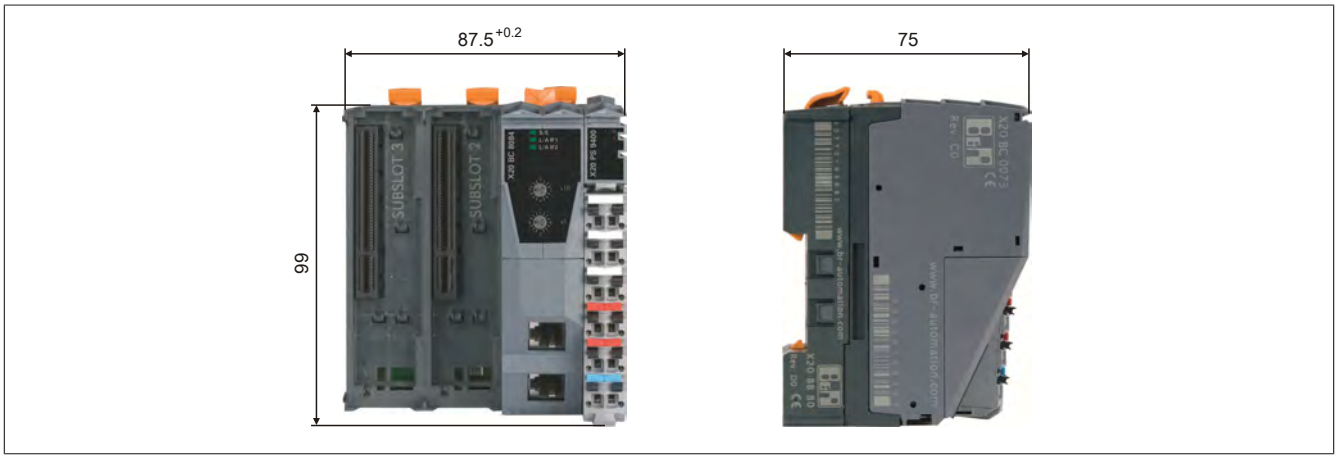


Figure 20: Dimensions of the fieldbus CPUs and expandable bus controller with two additional slots

3.1.5 I/O modules

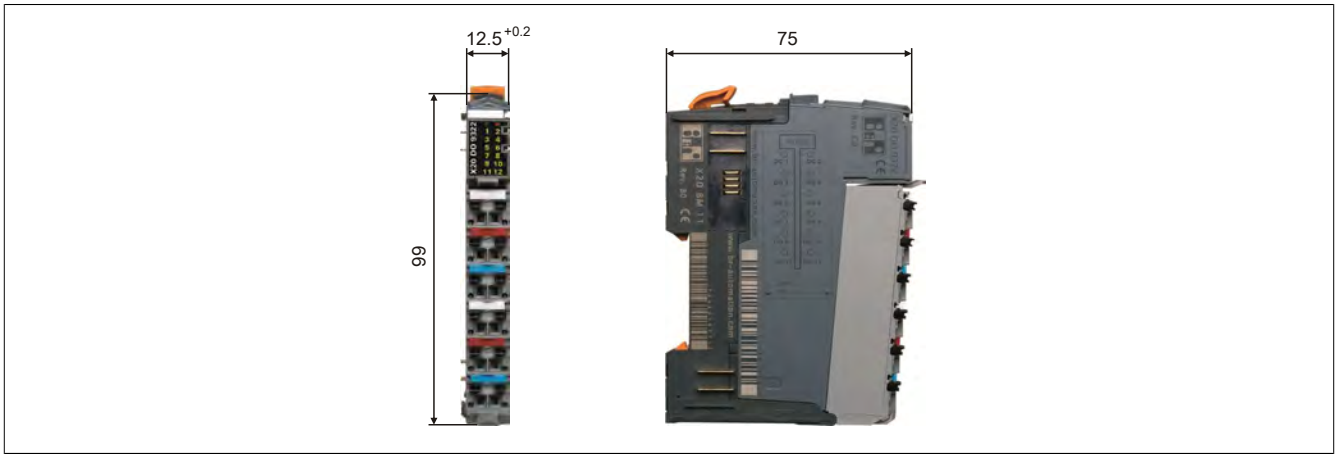


Figure 21: Dimensions of the I/O modules

3.1.6 CAD support

To ensure CAD support, the dimensions are included in the ECAD macros in 2D. STEP data is available to allow 3D viewing.

The STEP data can be found in the Downloads section of the B&R website at www.br-automation.com under the respective module.

3.2 Design support

3.2.1 Macros for ECAD systems

The electronics in a machine must be designed in a way that optimizes use of available space and materials. Graphic ECAD systems have proven themselves as the right tool for this job.

Every module in the X20 system is delivered with pre-designed electronic descriptions of the mechanical dimensions, electrical signals and module functions. These macros can be loaded directly to proven ECAD systems. The wiring plans are automatically applied by the configuration and programming system, Automation Studio. Design and changes are immediately reflected at all levels of development. This saves time for the more important tasks and prevents errors right from the start. The accelerated development, programming, maintenance and documentation involved with the X20 system mean lower costs, enhanced quality and increased sales by earlier entry into the market.

3.2.2 Printing support

System printers and standard identification labels are supported by the appropriate printer software. Printing can be done manually from table calculations or directly from ECAD software (all methods are supported). The software and printer systems correspond with the Weidmüller standard.

3.3 Installation

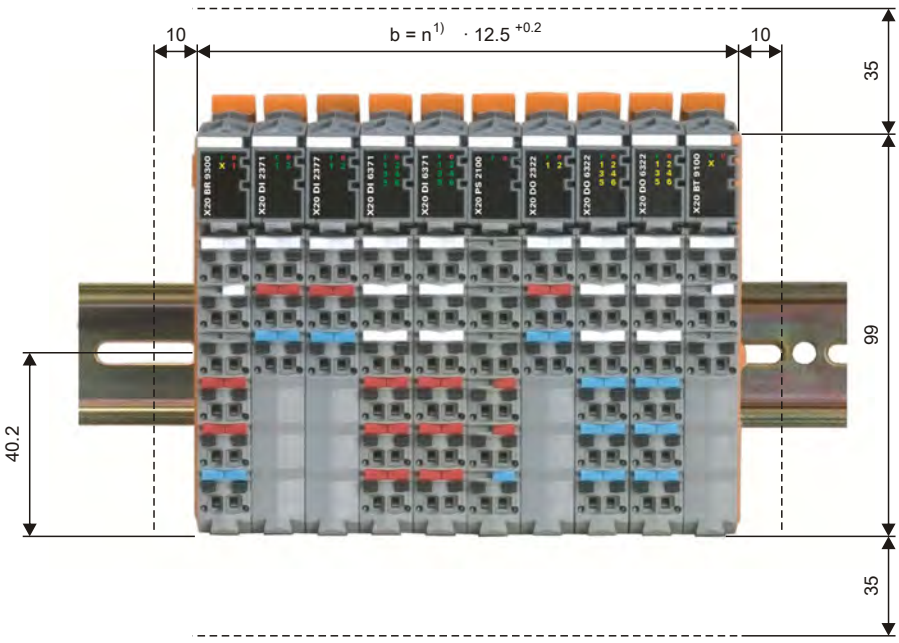
A top-hat rail conforming to the EN 60715 standard (TH35-7.5) is required to mount the PLC. The conductive top-hat rail is fastened to the back wall of the control cabinet.

The complete system including all individual modules is hung in the desired location on the top-hat rail with the unlocking mechanisms open and locked in place by closing the unlocking mechanisms. Finally, the modules are equipped with the prewired terminal blocks.

Information:

Only horizontal or vertical mounting orientation is permitted.

3.3.1 Horizontal installation

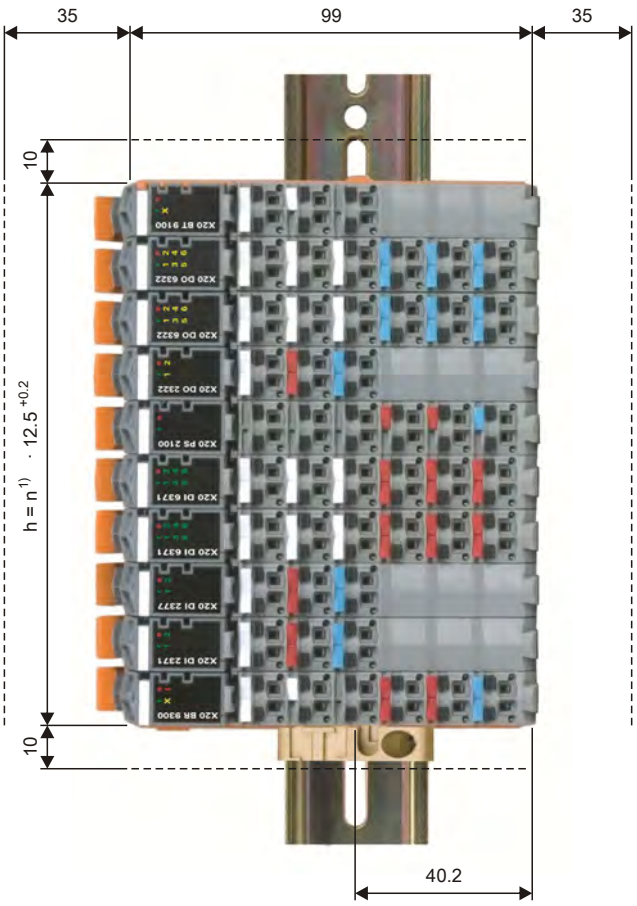


1) n ... Number of modules

Figure 22: X20 system - Horizontal installation

For optimal cooling and air circulation, there must be at least 35 mm free space above the modules. To the left and right of the X20 system, there must be at least 10 mm of free space. Underneath the modules, 35 mm space must be left free for I/O and power supply cabling.

3.3.2 Vertical installation



1) n ... Number of modules

Figure 23: X20 system - Vertical installation

For optimal cooling and air circulation, there must be at least 35 mm free space to the left of the modules. Above and below the X20 system, there must be at least 10 mm of free space. To the right of the modules, 35 mm space must be left free for I/O and power supply cabling.

The modules must be arranged so that the controller is on the lower end of the system. The temperature range is limited to -25 to 50°C when modules are mounted vertically.

Information:

The controller must be secured against slipping. An end bracket or ground terminal can be used for securing.

3.4 Wiring

In order to achieve a secure connection in the terminal blocks, wires must be stripped accordingly.

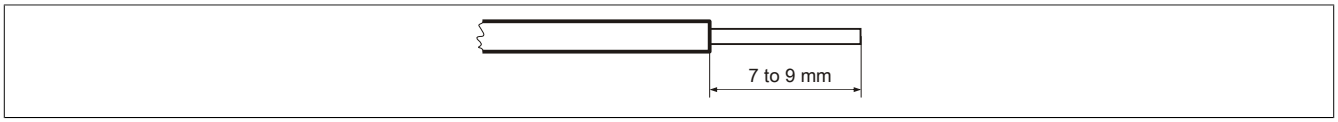


Figure 24: Wire stripping for a secure connection

Information:

The wire stripping length must not be more or less than 7 to 9 mm.

3.5 Stress relief using cable ties

Figure 25: Stress relief using cable ties

The X20 system terminal blocks have slots for the cable ties. If needed, a cable tie can be fed through these slots to reduce the stress on the cable.

Cable tie dimensions:	Width ≤ 4.0 mm Thickness ≤ 1.2 mm

Figure 26: Slots through which the cable ties are fed

3.6 Shielding

In principle, the shield must be grounded in all shielded cables:

- Analog signals (inputs and outputs)
- Interface modules
- Counter modules
- X2X Link cables
- Fieldbus connections (PROFIBUS DP, CAN bus, etc.)

In general, the following guidelines apply for shielding:

- The X20 top-hat rail must always be mounted to a conductive backplane.
- Shielded cables must be grounded on both sides.

3.6.1 Direct shielding connection

The shield is twisted and connected to the bus module's ground connection using a cable lug (2.8 x 0.5 mm). The cable is additionally secured to the terminal block using a cable tie (stress relief).

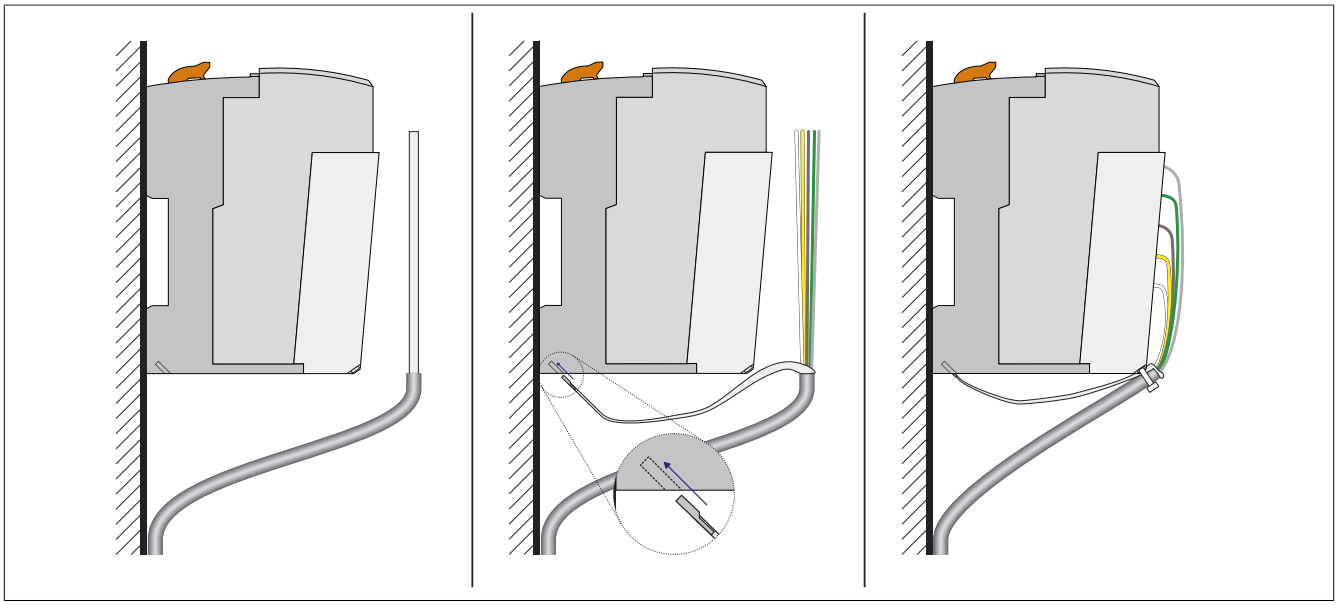


Figure 27: Direct shielding connection

Information:

The ground connection should be made as short and with as little resistance as possible.

3.6.2 X20 cable shield clamp

The X20 cable shield clamp (model number X20AC0SG1) is latched to the terminal block and connected to the bus module's ground connection using a cable lug. Cable ties are used to press the shield against the grounding plate.

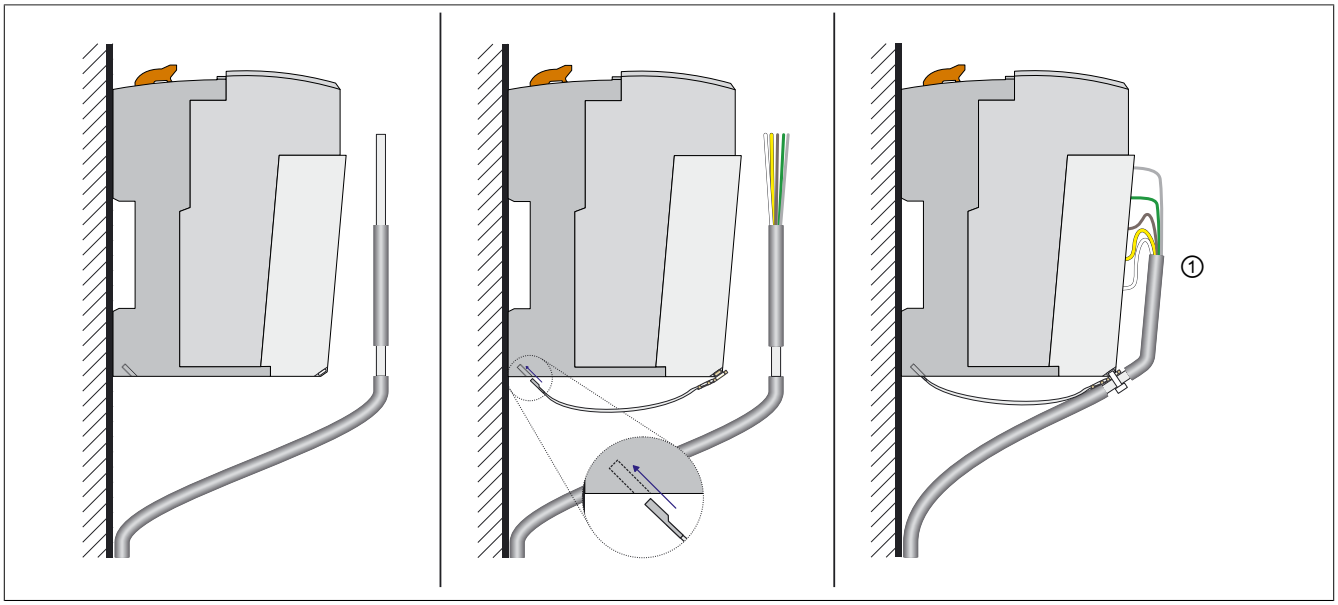


Figure 28: Shielding via X20 cable shield clamp

To reduce the EMC emissions most effectively, the cable shield must be as long as possible after the cable tie (see ① in the diagram above).

3.6.3 X20 shielding bracket

The X20 shielding bracket (model number X20AC0SF7.0010) is installed below the X20 system. The shield is pressed against the shielding bracket using ground terminals from another manufacturer (e.g. PHOENIX or WAGO) or a cable tie.

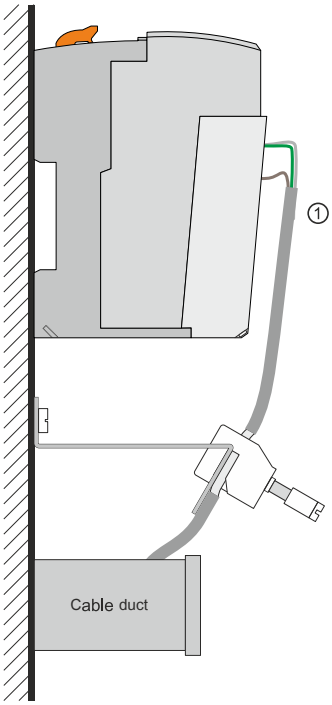
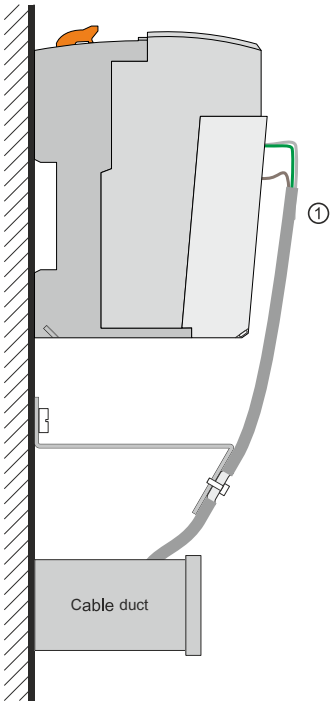
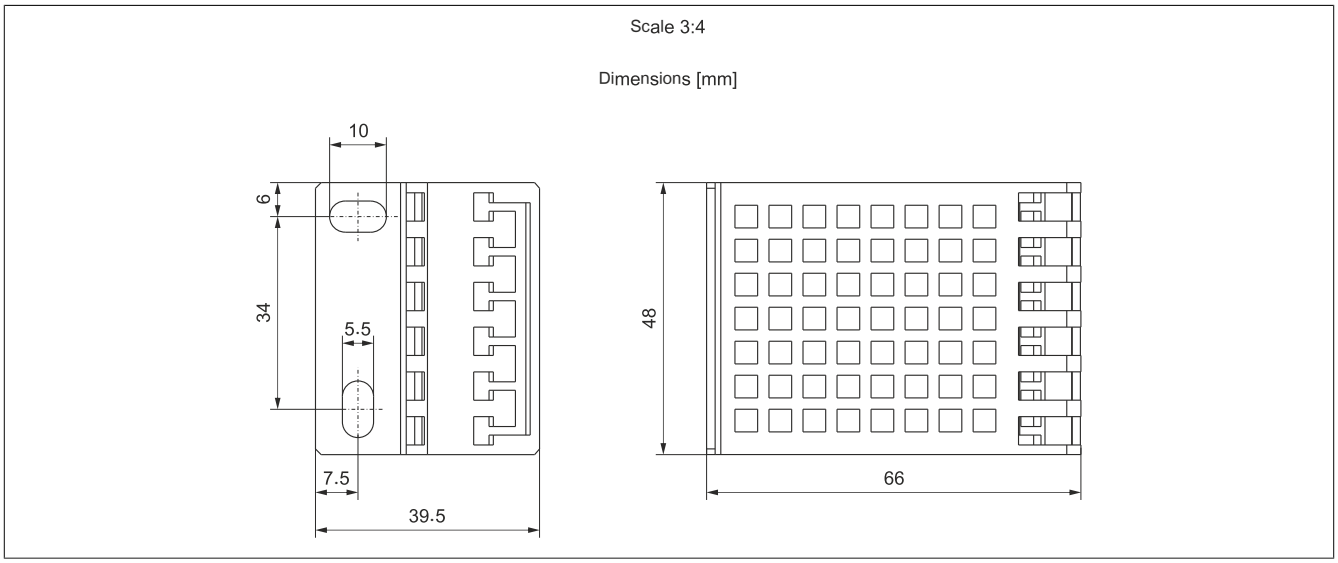
Attaching the shield with a ground terminal	Attaching the shield with a cable tie
	

Table 4: Cable shielding via X20 shielding bracket

To reduce the EMC emissions most effectively, the cable shield must reach as high as possible after the cable tie (see ① in the diagram above).

Dimensions



Content of delivery

- 10 X20 shielding brackets
- Installation template

3.6.4 Shielding via top-hat rail or bus bar

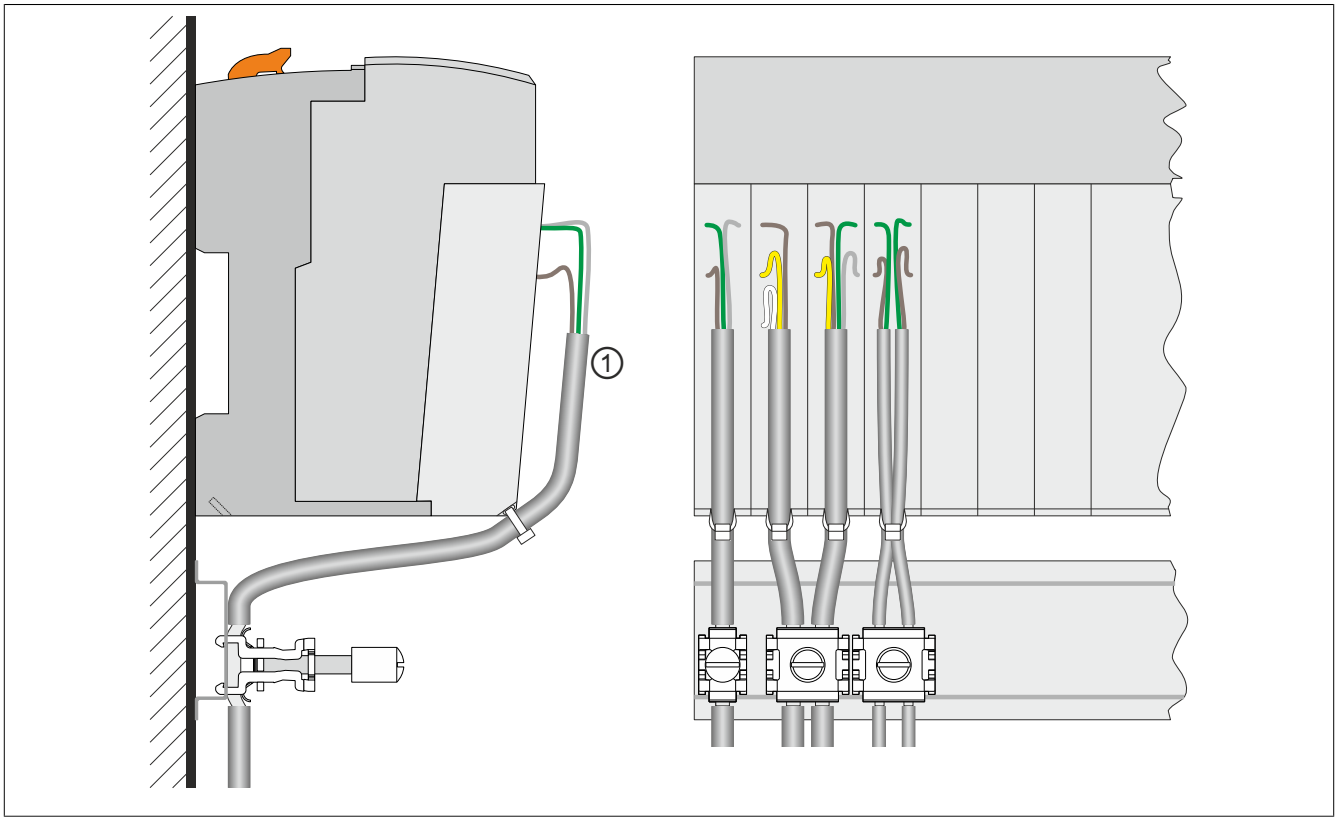


Figure 29: Shielding via top-hat rail or bus bar

Grounding terminals from other manufacturers (such as GOGATEC) can be used to achieve shielding right on the top-hat rail or on special bus bars directly below the controller.

- B&R recommends always using a grounding terminal via the top-hat rail to connect the X2X Link cable shield directly with the conductive and grounded backplane. This will generally exceed the specified EMC minimal requirements.
- The shielded cables from other modules can be grouped and clamped together. This may also be necessary due to space limitations. A different number of cables can be grounded together with a single terminal depending on the grounding terminals being used.

To reduce the EMC emissions most effectively, the cable shield must be as long as possible after the cable tie (see ① in the diagram above).

3.7 Wiring guidelines for X20 modules with an Ethernet cable

A number of X20 modules are based on Ethernet technology. POWERLINK cables offered by B&R can be used for the necessary wiring.

Model number	Connection type
X20CA0E61.xxxx	Connection cable - RJ45 to RJ45
X67CA0E41.xxxx	Attachment cable - RJ45 to M12

Table 5: POWERLINK cable with RJ45 connector

The following wiring guidelines must be observed:

- Use CAT5 SFTP cables.
- Observe minimum cable flex radius (see data sheet for the cable)
- Secure the cable underneath the bus controller. The cable must be secured vertically under the female RJ45 connector on the bus controller.

Information:

Using POWERLINK cables offered by B&R (X20CA0E61.xxxx and X67CA0E41.xxxx) satisfies the EN 61131-2 product standard.

For any further requirements, the customer must take additional measures.

Wiring diagram

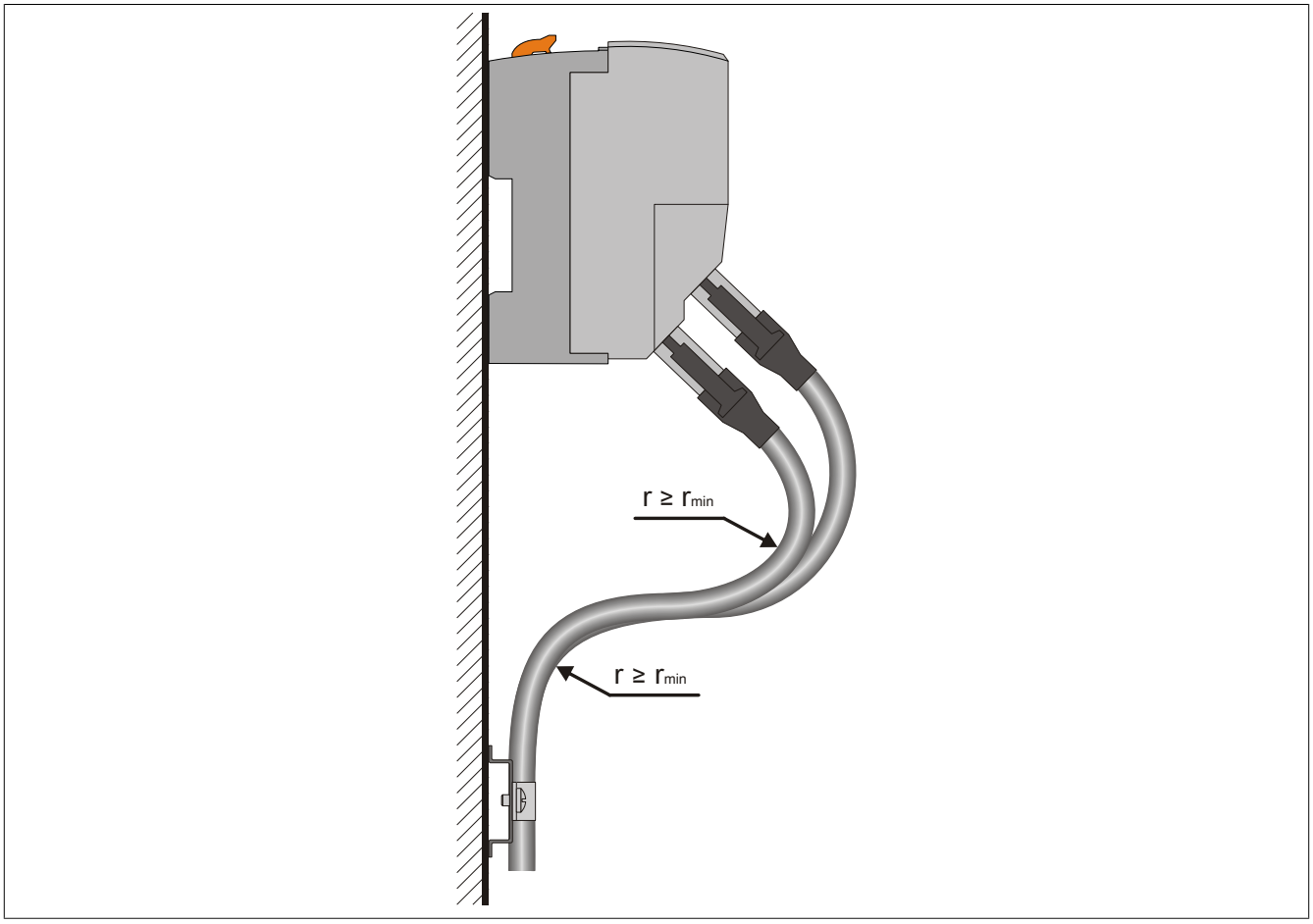


Figure 30: Wiring diagram for X20 modules with an Ethernet cable

3.8 The supply concept

Danger!

In order to guarantee a specific supply voltage, a SELV power supply that conforms to IEC 60204 must be used to supply the bus and I/O.

3.8.1 Bus module rack replacement

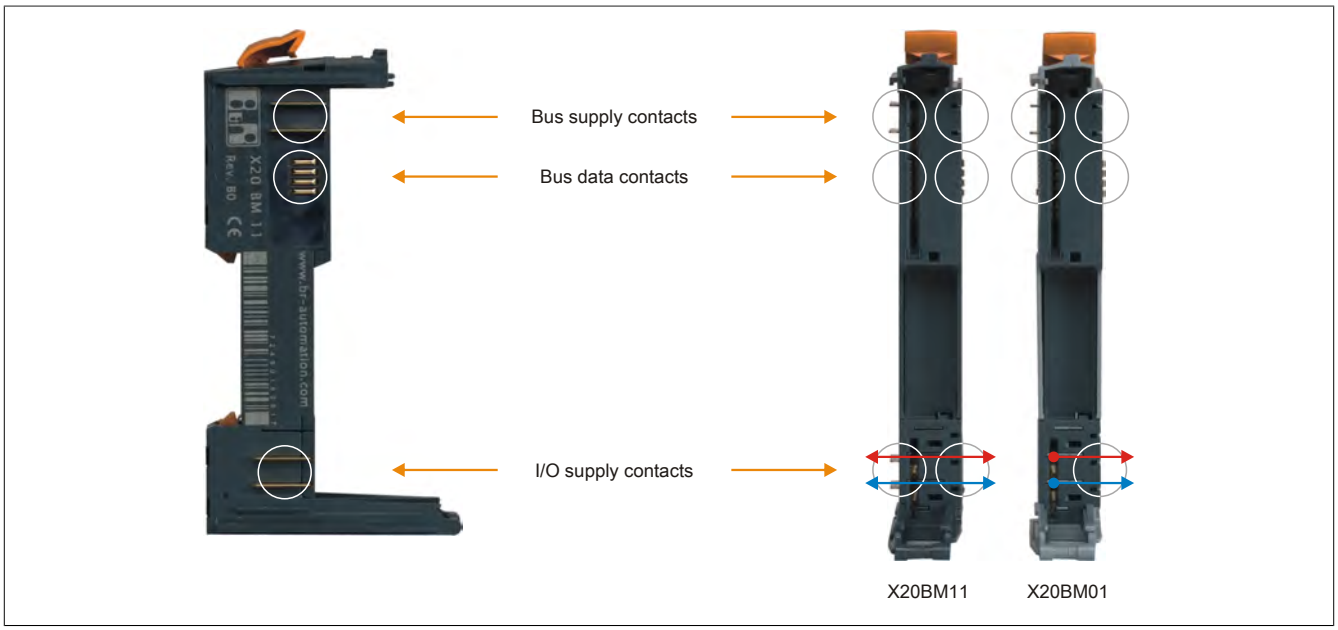


Figure 31: The bus module replaces the rack in the X20 system

The bus module is the backbone of the X20 system regarding the bus supply and bus data as well as the I/O supply for the electronics modules. Each bus module is an active bus station, even without an electronics module. There are two variations of the bus module:

- Interconnected I/O supply
- I/O supply isolated to the left (for power supply modules)

3.9 X20 system infrastructure

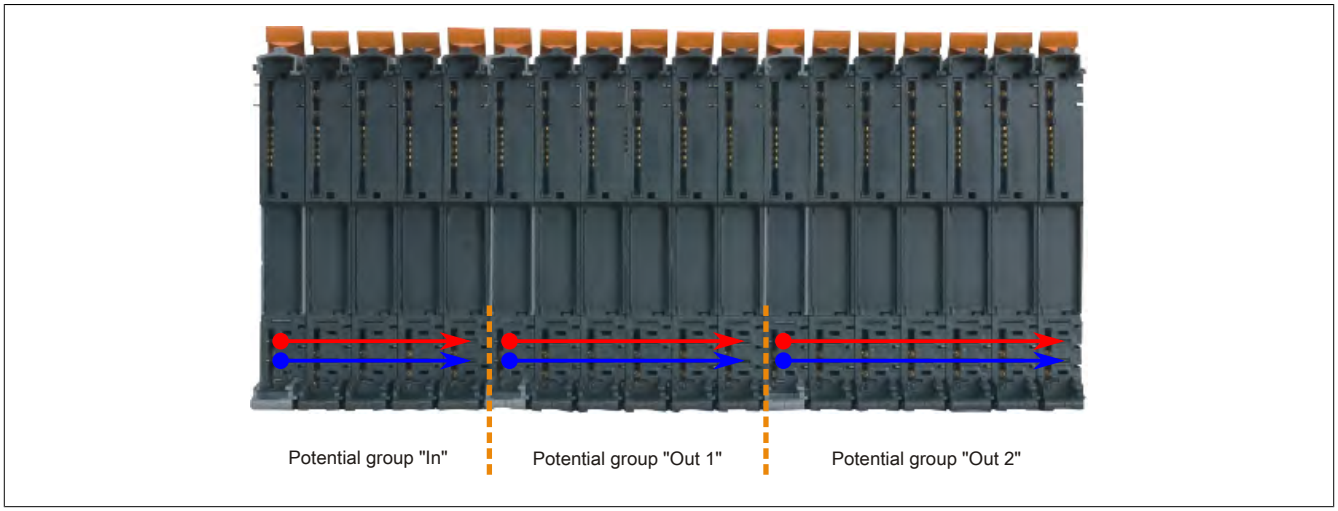


Figure 32: Simple implementation of different potential groups

Different potential groups can be implemented with the appropriate arrangement of supply bus modules, (e.g. for input groups or different E-stop circuits on the outputs). The I/O supply is fed by power supply modules.

3.10 Bus supply

Because the remote X2X Link backplane and I/O electronics are completely electrically isolated, the X2X Link supply needs to be fed in at certain intervals. This is initially handled by the bus receiver. A supply module for X2X Link must be added to refresh the supply after approximately 30 modules (for an example calculation, see 3.23 "Calculating the power requirements"). On the same module, a separate feed for the I/O supply can also be connected.

3.11 Potential groups

The I/O supply is connected via the bus modules, and the supply is fed in using corresponding power supply modules. This makes it possible to implement simple potential groups (e.g. for input groups or different output groups). For isolation, the corresponding bus module is also necessary, which provides isolation of the internal I/O supply.

3.12 Output modules with supply

Generally, a power supply module is also necessary for current output modules with many channels, such as the 8 channel output module with 2 amp outputs. This is not the case with the X20 system. With this module, the supply is provided directly on the module, thereby saving power supply modules and construction width.

3.13 Bus receiver with supply

The X20BR9300 bus receiver for the X20 system is equipped with a supply for X2X Link as well as for the internal I/O supply. This eliminates the need for an additional power supply module.

3.14 Supply module for internal I/O supply

The first I/O modules in an X20 system are supplied by the bus receiver. The internal I/O supply is refreshed via the X20PS2100 power supply module.

3.15 Power supply module for internal I/O supply and bus supply

The X2X Link is fed by the X20BR9300 bus receiver. After approx. 30 modules (see section 3.23 "Calculating the power requirements" for a calculation example), the supply must be "refreshed". The X20PS3300 power supply module is used for this. This module is equipped with a feed for X2X Link as well as for the internal I/O supply.

3.16 Bus transmitter with supply

The X20BT9100 bus transmitter has an integrated I/O supply feed. This saves a power supply module for the last potential group.

3.17 Internal I/O supply failure (ModuleOk)

The ModuleOk status for monitoring the X20 modules is made up of different module parameters. A loss of voltage in modules that are supplied via the internal I/O supply causes the ModuleOk data point to return the value 0 (false). This affects all modules that require 0.01 W on X2X Link.

3.18 X20 system power supply

The X20 system is powered by a B&R 24 VDC power supply. B&R power supplies ensure that control systems are reliably supplied even when operated at the minimum mains input voltage or when maximum power is output even if there are temporary power failures (≤10 ms).

3.19 X20 system protection

The protection for the X20 system depends on the supply concept.

3.19.1 Potential groups

Using the X20BM01 bus module and organizing the power supply bus modules accordingly allows various potential groups to be implemented (e.g. for input groups or various power circuits for the outputs).

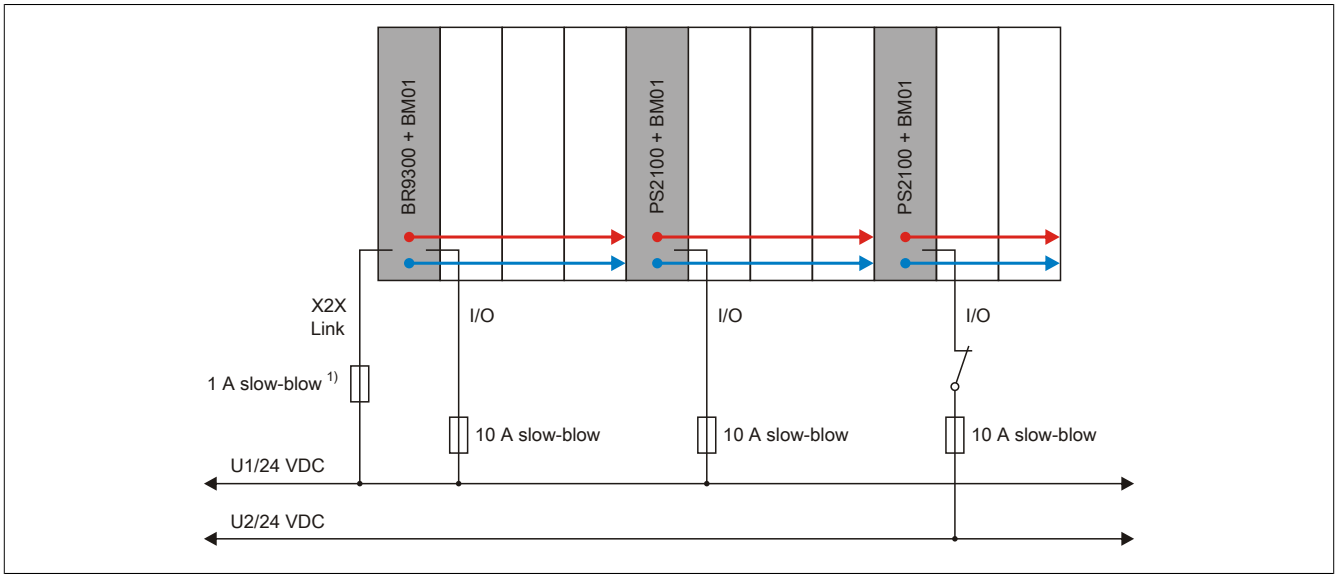


Figure 33: Protecting various potential groups

1) Recommended for line protection.

3.19.2 Supply via bus transmitter

The bus transmitter has an integrated internal I/O supply feed. This saves a power supply module for the last potential group.

Keep in mind: this potential group is separated from the rest of the potential groups by an I/O module with the bus module.

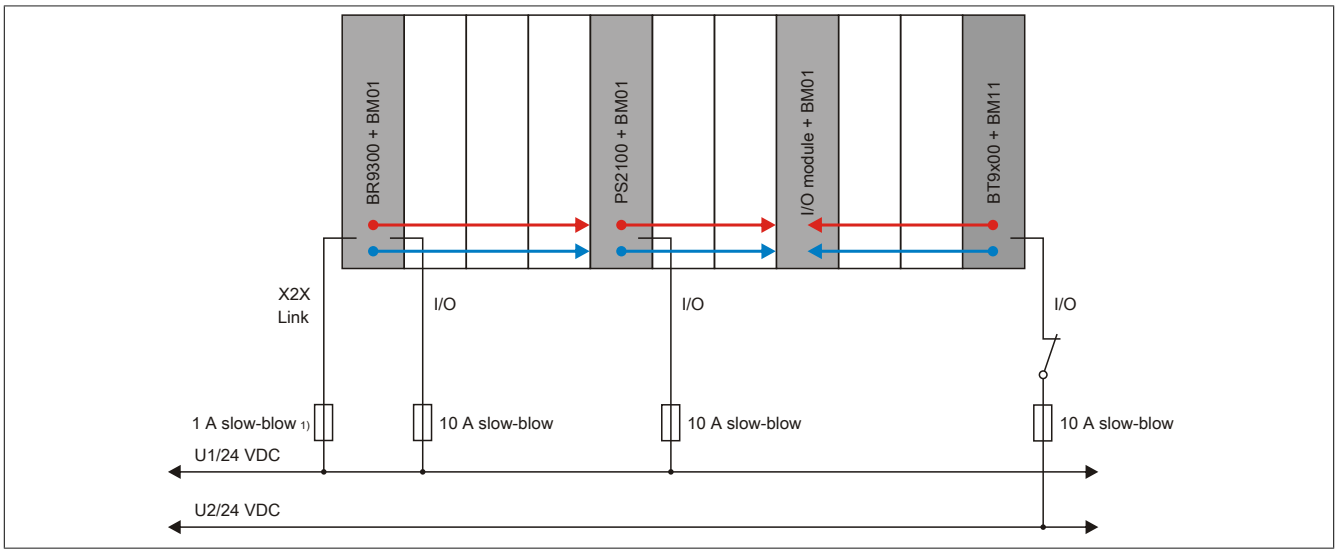


Figure 34: Protection when supplied via bus transmitter

1) Recommended for line protection.

3.20 X2X Link supply

3.20.1 Extended and redundant X2X Link supply

The X2X Link remote backplane is supplied separately from the I/O points. This ensures that the remote backplane doesn't fail if there is a power failure on the I/O side, for example with an emergency stop. After approx. 30 modules, it is necessary to "refresh" with a power supply module for X2X Link.

To achieve increased supply security, it is possible to set up a redundant X2X Link supply. To do so, the necessary X2X Link power must be determined and then covered by the corresponding quantity plus at least one additional X2X Link power supply module. This guarantees the functionality of the remote backplane even if the X2X Link supply fails.

Please note the following for the correct calculation:

- To determine the necessary X2X Link power, calculate using 75% of the power supply module's rated power during parallel operation.

Information:

This must be done for all power supply modules at the same time for a non-redundant X2X Link supply or when completely turning the X2X supply of an X20 module block on/off.

3.20.2 Example for extended X2X Link supply

It is possible to set up potential groups through the use of different supplies for the power supply modules.

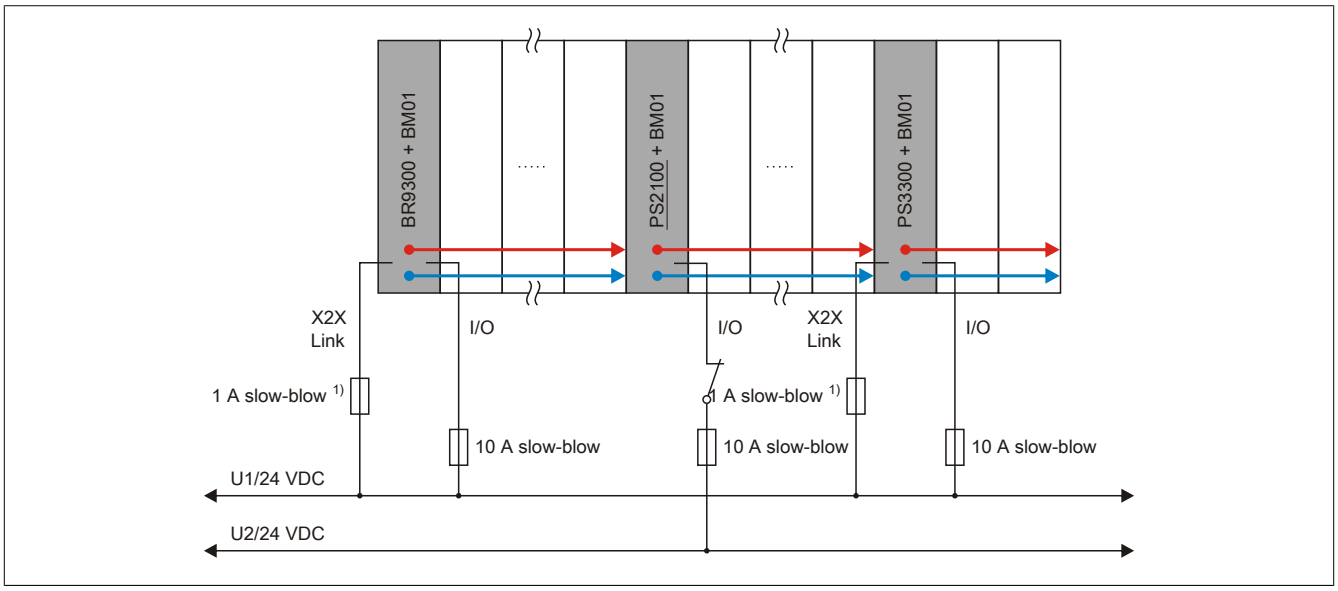


Figure 35: Example for extended X2X Link supply

1) Recommended for line protection.

The X20PS3300 power supply module supplies both the X2X Link and I/O; the X20PS2100 power supply module only supplies the I/O.

3.20.3 Example for redundant X2X Link supply

Multiple X20PS3300 power supply modules can be set up in parallel. It is possible to set up potential groups through the use of different supplies.

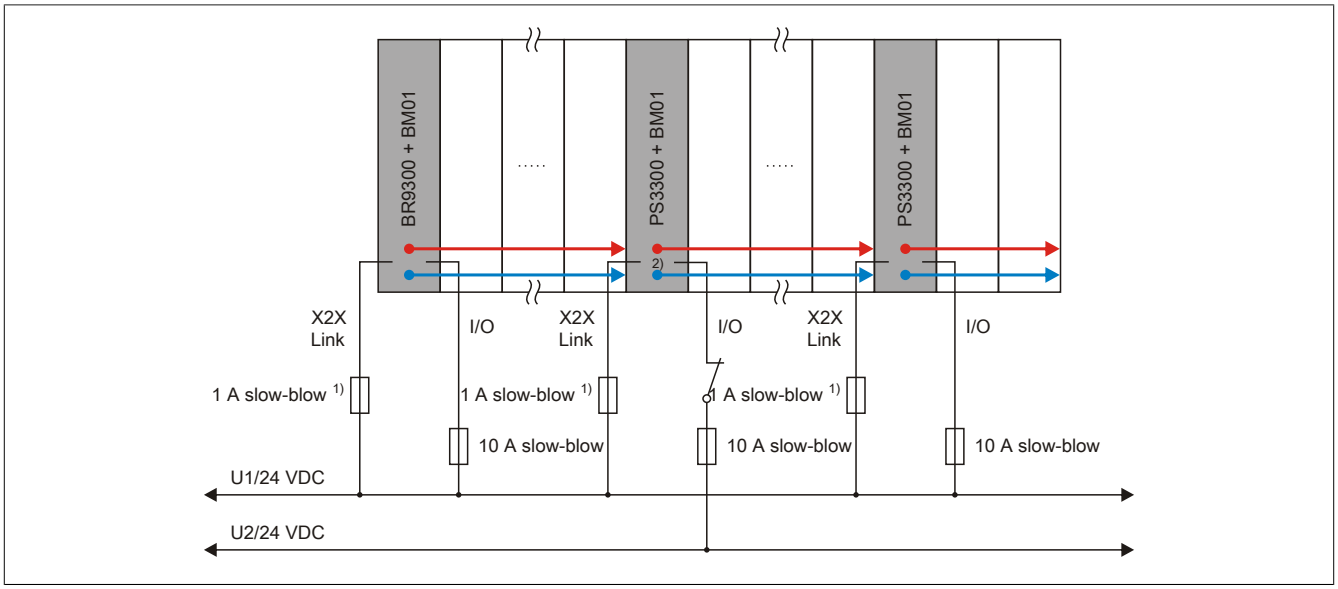


Figure 36: Example for redundant X2X Link supply

1) Recommended for line protection.
2) With separate supplies, the two reference potentials (GND_1 and GND_2) are combined via the terminal block on the PS3300.

The X20PS3300 power supply module supplies both X2X Link and the I/O.

3.21 Safe cutoff

3.21.1 General information

The operating principle "Safe cutoff of a potential group" allows the user to implement safety functions that satisfy the requirements of ISO 13849 within a B&R system when using an external safety relay.
The safety function is limited to cutting off or interrupting the power to the connected actuators.

Functionality

An external safety relay is connected to the I/O supply for the potential group. When the functional safe state is requested or a "Failsafe" state occurs, then this safety relay cuts off the I/O supply of the potential group. The power is then also cut off for all actuators connected to this potential group.

3.21.2 Scope of application / Standards referenced

The operating principle is confined to machine manufacturing applications, and therefore implicitly to the following standards:

- ISO 13849-1:2007 and ISO 13849-2:2013

Requirements of other standards are not taken into consideration.

3.21.3 Intended use

It is the user's responsibility to clarify guidelines for the use of safety-related B&R components with the respective authorities and to ensure these guidelines are met.

B&R will not assume warranty or liability for damages that occur due to:

- Improper use
- Non-observance of standards and guidelines
- Unauthorized modifications to devices, connections and settings
- Operation of unauthorized or unsuitable devices or device groups
- Failure to follow the safety notices covered in this manual
- Malfunctions caused by the external safety relay

3.21.4 Qualified personnel

Safety functionality is only permitted to be implemented by personnel with appropriate training in safety technology and knowledge of applicable regulatory and technical requirements.

Use of safety-related products is restricted to the following persons:

- Qualified personnel who are familiar with relevant safety concepts for automation technology as well as applicable standards and regulations
- Qualified personnel who plan, develop, install and commission safety equipment in machines and systems

Qualified personnel in the context of this manual's safety guidelines are those who, because of their training, experience and instruction combined with their knowledge of relevant standards, regulations, accident prevention guidelines and operating conditions, are qualified to carry out essential tasks and recognize and avoid potentially dangerous situations.

In this regard, sufficient language skills are also required in order to be able to properly understand this manual.

3.21.5 Application in the X20 system

The operating principle applies to a potential group in the X20 system. For information about how to create a potential group in the X20 system, see section 3.11 "Potential groups".

When implementing the operating principle, each X20 potential group must be supplied by a single power supply module. Only X20BM01, X20BM23 and X20BM26 modules that guarantee the interruption of the internal I/O supply to the left are permitted for use as bus modules for the power supply module. This ensures that each potential group in the X20 system will receive power from exactly one power supply module and prevents the possibility of multiple power sources.

3.21.5.1 Suitable modules

The operating principle is supported by the following X20 modules:

Module group	Module		Starting with revision
Bus modules	X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	D0
	X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	D0
	X20BM23	X20 power supply bus module, for X20 SafeIO power supply modules, internal I/O supply interrupted to the left	B0
	X20BM26	X20 power supply bus module, for X20 SafeIO power supply modules, with node number switch, internal I/O supply interrupted to the left	B0
Power supply modules	X20PS2100	X20 power supply module, for internal I/O supply	F0
	X20PS2110	X20 power supply module for internal I/O supply, integrated microfuse	C0
Safe power supply modules	X20SP1130	X20 safe power supply module, for internal I/O supply, 24 VDC, 10 A, with integrated safe cutoff function, be aware of the list of permitted modules in the potential group	B2
Digital outputs	X20DO2322	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, source, 3-wire connections	F0
	X20DO4322	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections	F0
	X20DO4332	X20 digital output module, 4 outputs, 24 VDC, 2 A, source, 3-wire connections	F0
	X20DO6321	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections	F0
	X20DO6322	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections	F0
	X20DO8232	X20 digital output module, 8 outputs, 12 VDC, 2 A, source, feed directly on module, 1-wire connections	E0
	X20DO8322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 1-wire connections	E0
	X20DO8332	X20 digital output module, 8 outputs, 24 VDC, 2 A, source, feed directly on module, 1-wire connections	G0
	X20DO9321	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections	E0
	X20DO9322	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections	H0
	X20DOF322	X20 digital output module, 16 outputs, 24 VDC, 0.5 A, source, 1-wire connections	C0
Digital signal processing and preparation	X20DS1119	X20 multifunctional digital signal processor, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module	F0
	X20DS1319	X20 multifunctional digital signal processor, 4 digital input channels, 4 digital channels configurable as inputs or outputs, 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with max. 2 reference pulses, SSI absolute encoder, NetTime module	D0
	X20DS4389	X20 digital signal module, 4 digital inputs, 24 VDC, 4 digital outputs, 24 VDC, 0.1 A, oversampling I/O functions, time-triggered I/O functions, NetTime module	B0
Analog outputs	X20AO2622	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	H0
	X20AO2632	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution	F0
	X20AO4622	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	H0
	X20AO4632	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution	I0
Counter functions	X20DC2395	X20 digital counter module, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function	F0
	X20DC4395	X20 digital counter module, 2 SSI absolute encoder, 24 V, 2 ABR incremental encoder, 24 V, 4 AB incremental encoders, 24 V, 8 event counters or 4 PWM, local time measurement function	G0
Additional functions	X20CM8323	X20 PWM module, 8 digital outputs for switching electromechanical loads, 0.6 A continuous current, 2 A peak current, current monitoring, switching time detection	F0
Motor controllers	X20MM2436	X20 PWM motor module, 24 to 39 VDC ±25%, 2 PWM motor bridges, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, configurable as incremental encoder	D0
	X20SM1426	X20 stepper motor module, 1 motor connection, 1 A continuous current, 1.2 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder	C0
	X20SM1436	X20 stepper motor module, module supply 24-39 VDC ±25%, 1 motor connection, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder	D0

Table 6: List of X20 modules

The operating principle of the X20 system has been tested by TÜV Süd, with the results documented under report number BE85906T.

3.21.6 General notices

3.21.6.1 Installation notes

Modules must be protected against impermissible dirt and contaminants. The maximum permissible level of dirt and contaminants is Pollution Level II as specified in the IEC 60664 standard. This can be achieved through installation in a control cabinet that provides IP54 protection.

When using the operating principle, uncoated X20 modules must not be operated in condensing relative humidity or with ambient temperatures below 0°C.

3.21.6.2 Timing

3.21.6.2.1 Worst case scenario

A maximum cutoff time of 500 ms must be assumed for the potential group for worst case scenarios. This time is needed to guarantee that energy stored within the module is discharged and the actuators are cut off in worst case scenarios. The cutoff times needed for the upstream external safety relay and actuator must also be added.

Worst case conditions for "Output = Off"

- Digital output: <5 V
- Analog output: <100 mV

3.21.6.2.2 Load-dependent cutoff time

The actual duration of cutoff can be calculated with the following formula.

$$t_{spec} = -\frac{C_{tot} * U_{in}}{I_{load}} * 2 * \ln\left(\frac{U_{off}}{U_{in}}\right)$$

t_{spec}	Actual cutoff time
C_{tot}	Total capacity of all modules in the potential group. (e.g. 10 modules 47 µF + 3 modules with 150 µF → Ctot = 920 µF)
U_{in}	Supply voltage
U_{off}	Voltage, if Output = Off
I_{load}	External load

Table 7: Parameter descriptions

Module	Module's internal capacity
X20MM2436 X20SM1426 X20SM1436	150 µF
Other modules [1)]	47 µF

1) Only modules from section 3.21.5.1 "Suitable modules".

If the result is t_{spec} = >500 ms, then the worst-case assumption from section 3.21.6.2.1 "Worst case scenario" applies.

Information:

- **The calculated load-dependent cutoff time must be verified by a test measurement!**
- **At the time a safety function is requested, there is no guarantee that the outputs used to calculate the load-dependent cutoff time are enabled. For example, if an output is disabled at the time of a request, then the respective internal capacities in the module will not be discharged in the calculated time (t_{spec}). The worst-case time of 500 ms should be taken into account in this situation. If the output is enabled from the functional application (shown in the sketch as the interval $t_{application}$) during the worst-case time (<500 ms), then the output subsequently remains enabled for the calculated time.**

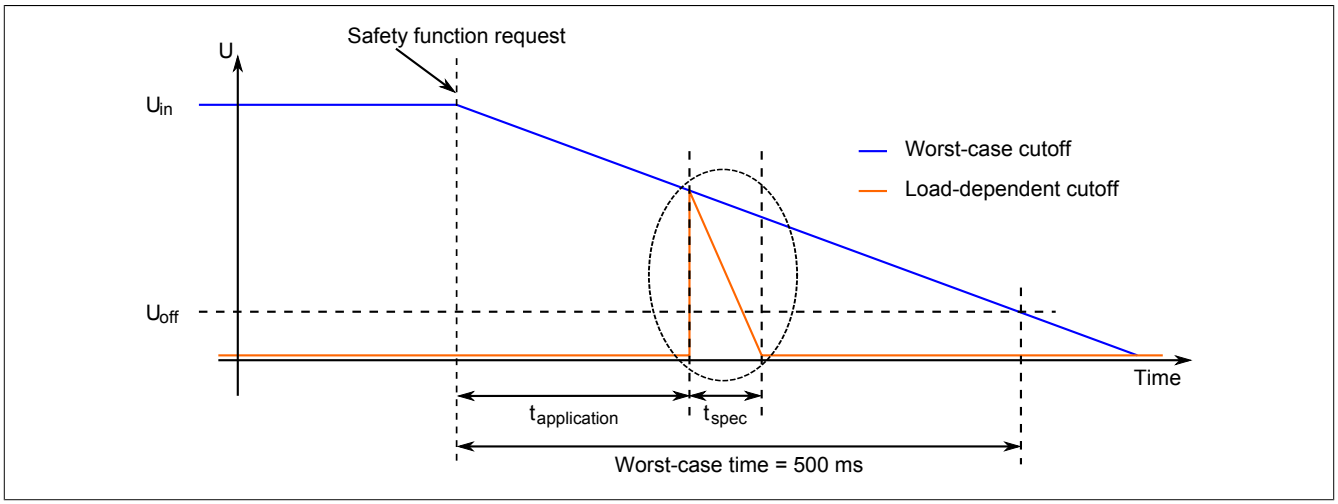


Figure 37: Output behavior following safety request

3.21.6.3 Potential group structure

The potential group can be made up only of modules in accordance with the table in section 3.21.5.1 "Suitable modules". Modules not listed in this table would compromise the "absence of feedback" of the external cutoff and therefore put the safety function at risk.

To ensure clarity and that the external cutoff is triggered when a fault occurs, installing multiple power supply sources in a potential group is not permitted.

SELV/PELV power supplies must be used for both the bus supply (X2X) and the module supply; otherwise, safety-related malfunctions can occur due to overvoltages.

For modules with isolated I/O potential for sensors and actuators, the upstream safety relay must shut off the supply for both the sensors and actuators; otherwise, energy regeneration cannot be excluded.

3.21.6.4 Circuit examples

1. One-channel without feedback

The following example shows a load being cutoff using the E-stop safety function. Only error-free actuators such as a motor or the "Enable" input of an ACOPOS / ACOPOSmulti drive may be used as the load in this case.
This type of circuit is not permitted for defective actuators such as relays since here the lack of feedback makes it impossible to detect contact sticking.

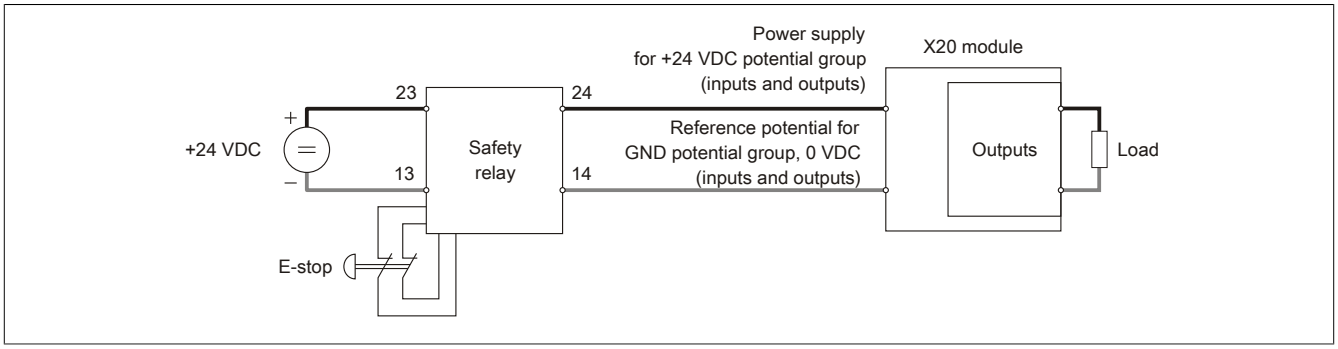


Figure 38: Circuit example 1: "One-channel without feedback"

Provided that the external components used (E-stop button, safety relay, load) satisfy the respective requirements, this example can achieve PL e (performance level as specified in ISO 13849).

2. Two-channel with feedback

The following example shows a load being cutoff using the E-stop safety function. Thanks to the feedback, errors in the actuator are detected, and with the full two-channel circuit, the cutoff is ensured even in the event of an error. Whether or not two fully isolated potential groups – as shown in the example – are necessary depends on the application and how the safety solution is designed.

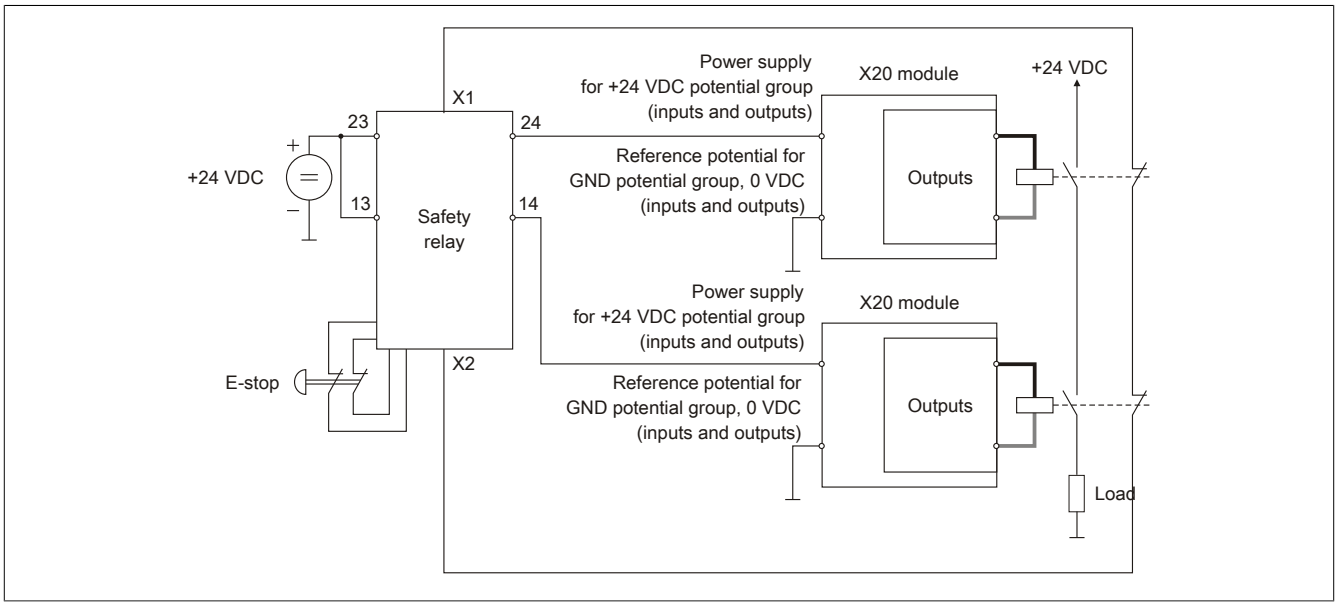


Figure 39: Circuit example 2: "Two-channel with feedback"

Provided that the external components used (E-stop button, safety relay, load) satisfy the respective requirements, this example can achieve PL e.

3. Example with X20SP1130 power supply module

The following example shows a load being cutoff using an X20SP1130 safe power supply module and an X20SI4100 safe input module together with the "E-stop" safety function.

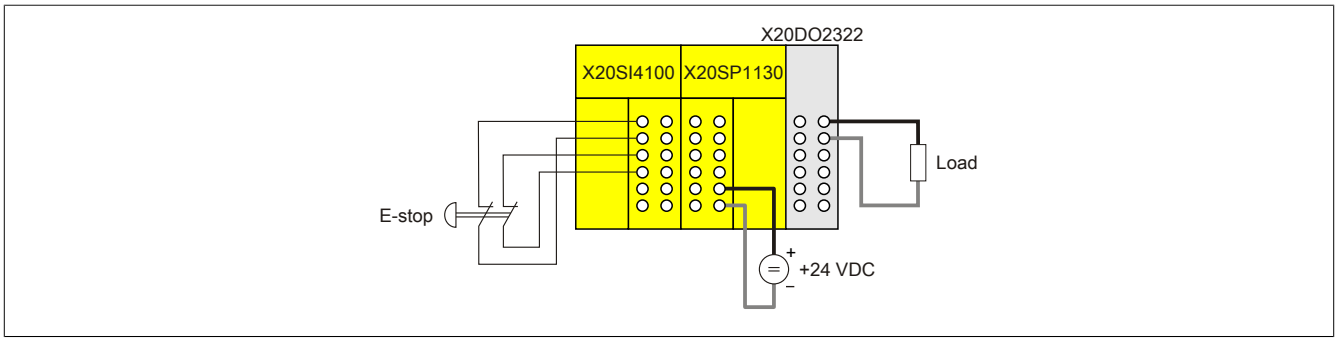


Figure 40: Circuit example 3: With X20SP1130 power supply module

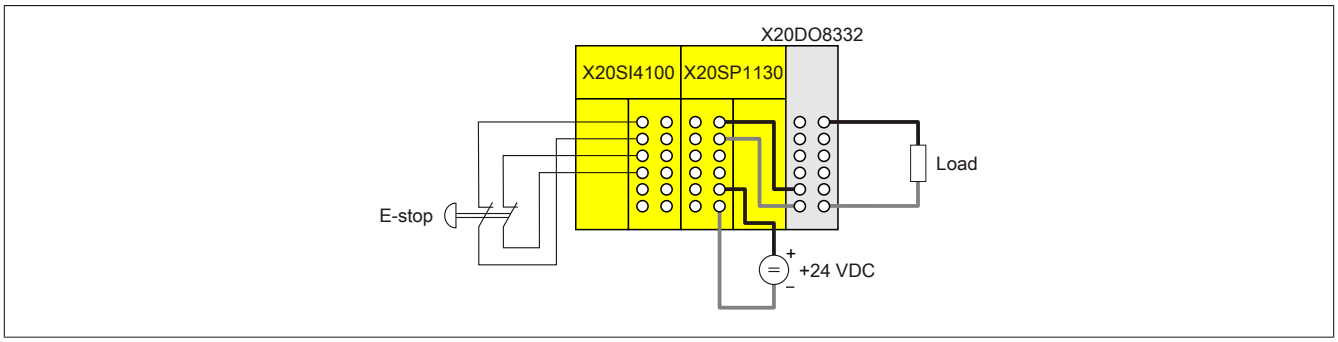


Figure 41: Circuit example 3: With X20SP1130 power supply module and X20DO8332

Provided that the external components used (E-stop button, load) satisfy the respective requirements, this example can achieve PL e.

3.21.6.5 Wiring notices

The operating principle "Safe cutoff of a potential group" only applies to the B&R modules used. All other parts of the safety chain, such as the application, upstream sensors or downstream actuators are NOT included in this principle.

For this reason, it is important to take the following points into consideration:

- Ensure proper wiring of the safety relay with the I/O supply. A short circuit between the output of the safety relay and an external 24 V voltage source can cause an unintended supply of 24 V to the internal supply voltage of the potential group. As a result, the safety function can no longer be guaranteed, which means that **ALL** of the channels in the potential group can no longer be cut off by the upstream safety switching device.
- Make sure that **ALL** of the potential group's input and output channels and the connected sensors and actuators are wired properly. A short circuit between an input or output of the potential group and an external 24 V voltage source can cause the unintended feedback of 24 V to the internal supply voltage of the potential group. As a result, the safety function can no longer be guaranteed, which means that **ALL** of the output channels in the potential group can no longer be cut off by the upstream safety relay.
- In accordance with EN ISO 13849-2:2013, Appendix D.2, Table D.4, a short circuit between any two conductors can be excluded, provided that:
    - they are permanently connected and protected against external damage (e.g. using a cable duct or armored conduit)
    - OR they are in separate plastic-sheathed cables
    - OR they are installed within an electrical enclosure (provided that both the conductors and the enclosure meet the appropriate requirements [see EN 60204-1 (IEC 60204-1)])
    - OR they are individually shielded with a ground connection

3.21.7 Safety guidelines

This section provides a summary of safety notices for the user.

Danger!

Please observe the following safety notices. Failure to observe one of the following notices can lead to loss of safety functionality and may result in serious injury.

- **The safety relay determines which category (according to ISO 13849) is achieved.**
- **When using the operating principle, it is the user's responsibility to adhere to the relevant standards and safety directives. The notices provided in sections 3.21.1 "General information" through 3.21.4 "Qualified personnel" regarding functionality, applicable standards, proper use and qualified personnel are also to be observed.**
- **The safety function is limited to cutting off or interrupting the power to connected devices. Safety functions that require actively powering on an actuator in a safe state cannot be implemented with this function.**
- **For all potentials supplying the modules, SELV/PELV power supplies must be used.**
- **The potential groups for which the operating principle is applied must only contain modules listed in the table in section 3.21.5.1 "Suitable modules".**
- **When using the operating principle with uncoated X20 modules, the modules must not be operated in condensing relative humidity or with ambient temperatures below 0°C.**
- **It is not permitted to mix modules from different systems (X20, X67) within a potential group.**
- **It is not permitted to install multiple power supply modules in a potential group (particularly with regard to power supply modules that also supply the bus supply).**
- **Ensure that the upstream safety relay is wired properly.**
- **Ensure that ALL sensors and actuators connected to the potential group are wired properly.**
- **Be aware of the maximum safety-related response time of 500 ms when shutting down the potential group. The cutoff times needed for the upstream external safety relay and actuator must also be added. Using the formulas defined in section 3.21.6.2.2 "Load-dependent cutoff time", it is possible to achieve cutoff times under 500 ms.**
- **The calculated load-dependent cutoff time must be verified by a test measurement!**
- **For modules with isolated I/O potential for sensors and actuators, the upstream safety relay must shut off the supply for both the sensors and actuators.**
- **The ground connections should be used as functional ground and not as protective ground and must not be connected to the 24 V supply voltage (GND is permitted). There must not be any protective components between the ground and the 24 V supply voltage.**

3.22 Combining X2X Link systems

3.22.1 General information

The X2X Link provides a complete remote backplane, which is used for communicating between bus modules and over the X2X Link cable. Systems based on X2X Link can be combined with one another as needed.

3.22.2 Connection overviews

The following connection overviews illustrate combinations of different systems that are based on X2X Link. The model numbers indicate which standard cables available from B&R can be used to connect with one another.

3.22.2.1 Combining X20, X67 and compact I/O system

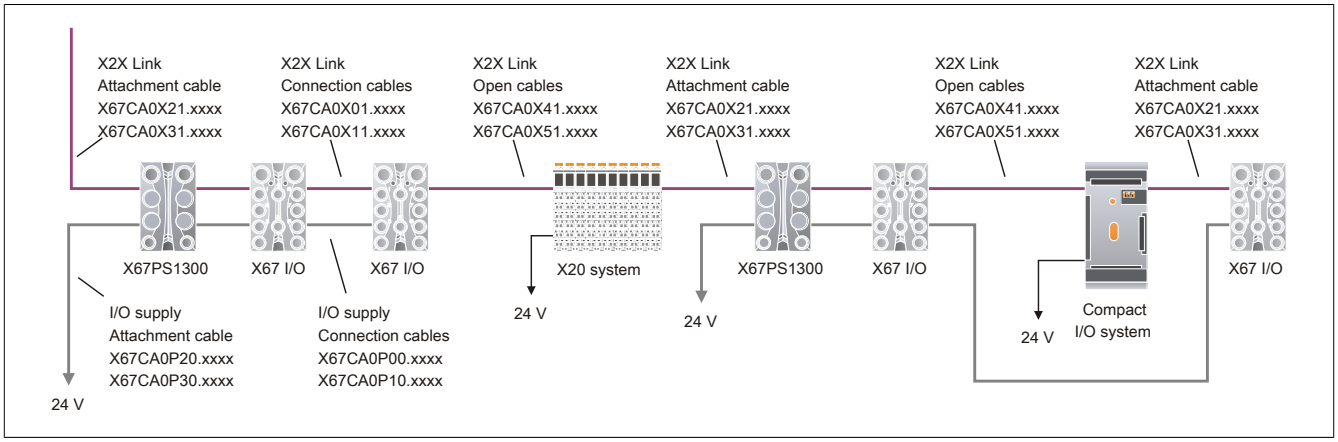


Figure 42: Connection overview - Combining X20, X67 and compact I/O system

3.22.2.2 Combining X20, X67 and valve terminal connections

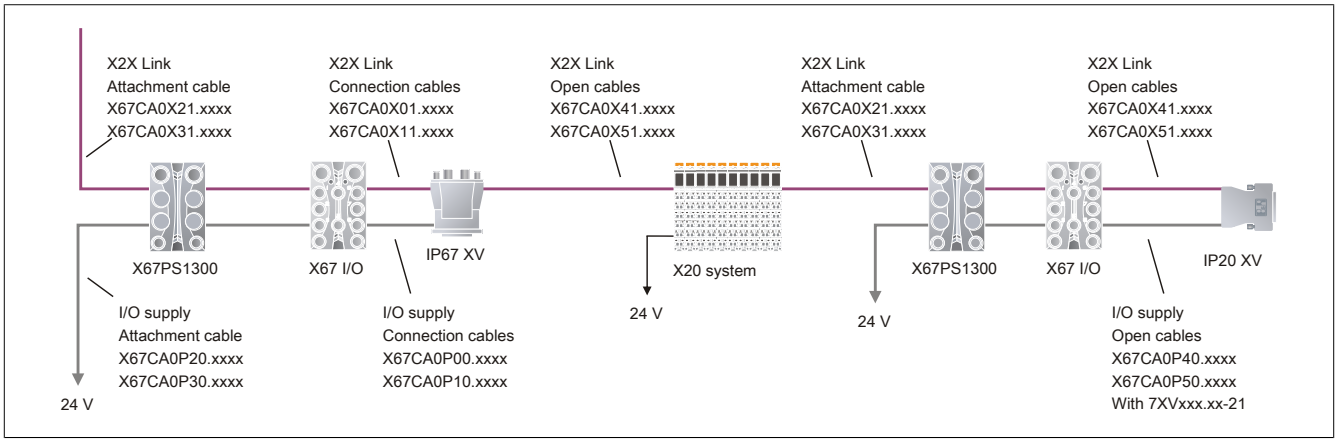


Figure 43: Connection overview - Combining X20, X67 and valve terminal connections

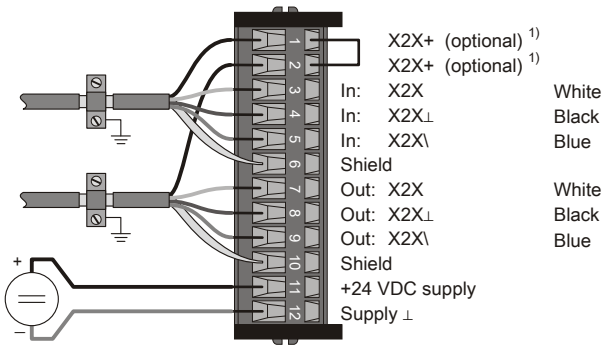
3.22.3 Connection examples

3.22.3.1 X20 system

Connection examples are listed in the module description:

- X20BR9300 bus receiver: 4.8.2.7 "Connection examples"
- X20BT9100 bus transmitter: 4.8.3.7 "Connection examples"

3.22.3.2 Compact I/O system



1) Used to forward the X2X Link supply when using IP67 modules.

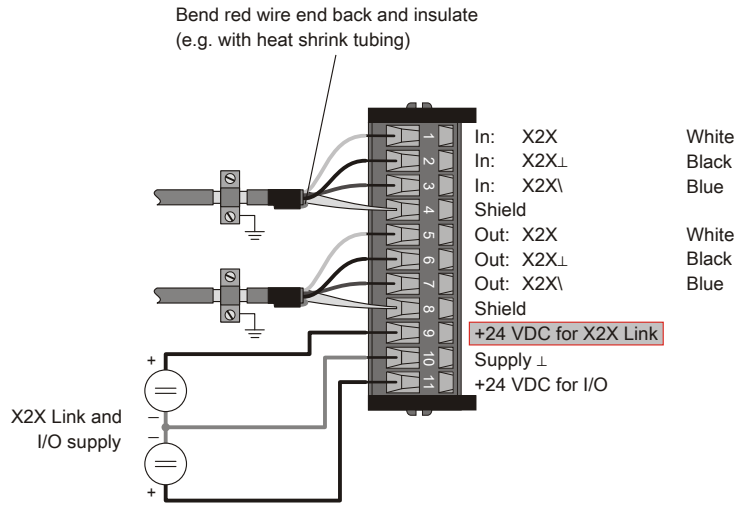
Signal	Cable type	Model number
X2X Link In	Open cables[1)]	X67CA0X41.xxxx
		X67CA0X51.xxxx
X2X Link Out	Attachment cable[1)]	X67CA0X21.xxxx
		X67CA0X31.xxxx
X2X Link in/out	Cable for custom assembly, 100 m	X67CA0X99.1000

Table 8: Compact I/O system - Connection example

1) Bridge for X2X+ in connection with X67 modules.

3.22.3.3 Valve connection

Connection example with 7XVxxx.xx-11/-12

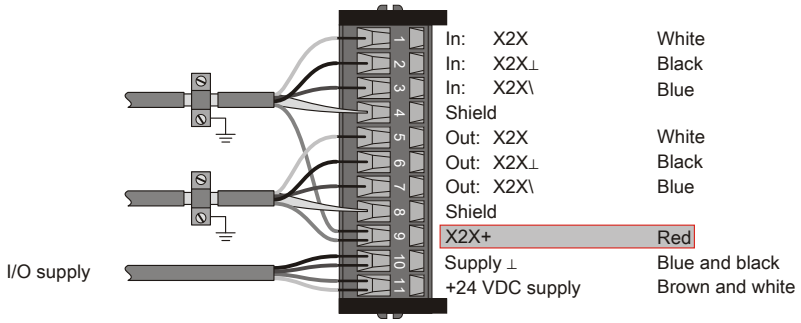


Signal	Cable type	Model number
X2X Link In	Open cables[1)]	X67CA0X41.xxxx
		X67CA0X51.xxxx
X2X Link Out	Attachment cable[1)]	X67CA0X21.xxxx
		X67CA0X31.xxxx
X2X Link in/out	Cable for custom assembly, 100 m	X67CA0X99.1000

Table 9: Connection example for valve connection (7XVxxx.xx-11/-12)

1) In connection with X67 modules.

Connection example with 7XVxxx.xx-21

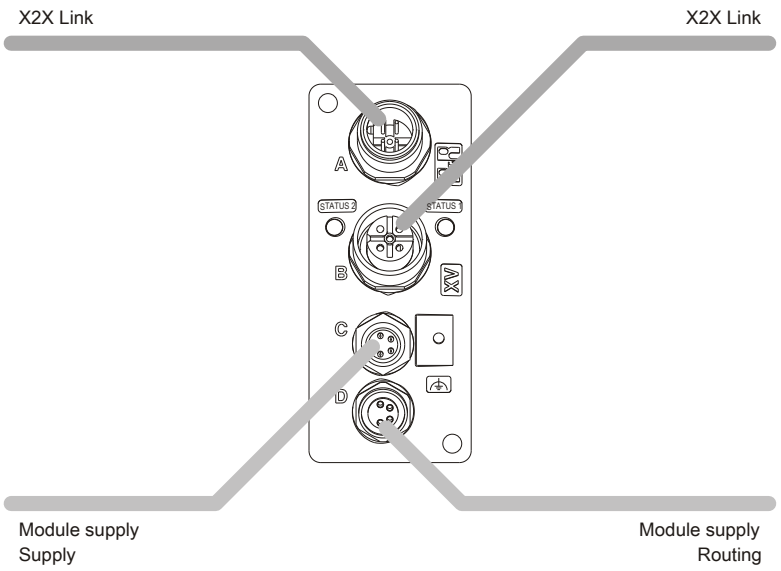


Signal	Cable type	Model number
X2X Link In	Open cables[1)]	X67CA0X41.xxxx
		X67CA0X51.xxxx
X2X Link Out	Attachment cable[1)]	X67CA0X21.xxxx
		X67CA0X31.xxxx
X2X Link in/out	Cable for custom assembly, 100 m	X67CA0X99.1000
I/O supply	Open cables[1)]	X67CA0P40.xxxx
		X67CA0P50.xxxx

Table 10: Connection example for valve connection (7XVxxx.xx-21)

1) In connection with X67 modules.

Connection example with 7XVxxx.xx-51/-62



Signal	Cable type	Model number
X2X Link	Connection cables[1)]	X67CA0X01.xxxx
		X67CA0X11.xxxx
I/O supply	Connection cables[1)]	X67CA0P00.xxxx
		X67CA0P10.xxxx

Table 11: Connection example for valve connection (7XVxxx.xx-51/-62)

1) In connection with X67 modules.

3.23 Calculating the power requirements

Overview of I/O supply

The power necessary for operation is provided by the power supply modules, the X20 CPU, the bus receivers and the bus transmitters.

Module	I/O internal power	Bus power
X20CP148x, X20CP158x, X20CP358x	+240 W	+7 W
X20BR9300	+240 W	+7 W
X20PS2100	+240 W	-0.2 W
X20PS2110	+144 W	-0.2 W
X20PS3300	+240 W	+7 W
X20PS3310	+144 W	+7 W
X20PS9xxx	+240 W	+7 W

Bus transmitter

When calculating the power requirements for bus transmitters, it is important to know whether they are only being used as such or are also being used as an I/O power supply module.

Model number	I/O internal power		Bus power
	When operated as a bus transmitter	When operated as a bus transmitter and I/O power supply module	
X20BT9100	-0.1 W	+240 W	-0.5 W
X20BT9400	-0.1 W	+240 W	-0.5 W

Table 12: Overview of bus transmitter power

Information about power consumption

The power consumption of individual modules can be found on the respective technical data sheet. Information about power consumption can be found in the technical data under "General information - Power consumption".

- The value in the "Internal I/O" row refers to the internal power requirements of the I/O module covered by the 24 VDC I/O supply.
- The value specified in the "Bus" row refers to the X2X Link power balance.

These rows can be used to quickly and easily create a power balance for a certain hardware configuration. The power consumption values of individual modules should then be subtracted from the power provided by the power supply module. The sum is not permitted to be less than zero.

Information:

For a calculation example, see 3.23.1 "Example 1" and 3.23.2 "Example 2".

Embedded parameter chip

On modules with 0.01 W power requirements, it is only possible to read the embedded parameter chip if the I/O supply is also active. Information about the embedded parameter chip can be found in the 2.12 "Embedded parameter chip" section.

3.23.1 Example 1

Calculating the power requirements for the bus and 24 VDC I/O supply with the following hardware configuration:

Module	Bus power [W]	I/O-internal power [W]	I/O-external power [W]	Sensor/Actuator supply [W][1]
X20DI4371	0.14	0.59	-	12.00
X20DI2371	0.12	0.29	-	12.00
X20DO4322	0.16	0.49	48.00[2]	12.00
X20DO4322	0.16	0.49	48.00[2]	12.00
X20BT9100	0.50	0.10	-	-
Subtotal		**1.96**	**96.00**	**48.00**
Total	**1.08**		**145.96 (=1.96 + 96.00 + 48.00)**	

1) Rated power at 24 VDC and 0.5 A.
2) Rated power at 24 VDC and 100% simultaneity.

The total power to be supplied by the 24 VDC I/O power supply is 145.96 W. One power supply module is already integrated in the X20BR9300 bus receiver. The power comparison indicates that the power provided by the power supply module is sufficient.

	Bus power [W]	Power 24 VDC I/O supply [W]
X20BR9300	+7.00	+240.00[1]
Power requirements of I/O modules	-1.08	-145.96
Power requirements of all bus modules	-0.78	-
Remaining power	**+5.14**	**+94.04**

1) Rated power at 24 VDC and 10 A.

3.23.2 Example 2

The I/O modules are divided into 3 potential groups in this example:

Potential group 1	Potential group 2	Potential group 3
Digital input modules	Digital output modules	Analog input modules and temperature modules

Calculating the power requirements for the bus and 24 VDC I/O supply per potential group with the following hardware configuration:

Potential group 1				
Module	**Bus power [W]**	**I/O-internal power [W]**	**I/O-external power [W]**	**Sensor/Actuator supply [W][1]**
X20DI6371	0.15	0.88	-	-
X20DI6371	0.15	0.88	-	-
X20DI2377	0.15	0.82	-	12.00
Subtotal		**2.58**	-	**12.00**
Total	**0.45**		**14.58 (= 2.58 + 12.00)**	

1) Rated power at 24 VDC and 0.5 A.

Potential group 2				
Module	**Bus power [W]**	**I/O-internal power [W]**	**I/O-external power [W][1)]**	**Sensor/Actuator supply [W][2)]**
X20DO2322	0.13	0.33	24.00	12.00
X20DO6322	0.18	0.71	72.00	-
X20DO8332	0.22	-	-[3)]	-
Subtotal		**1.04**	**96.00**	**12.00**
Total	**0.53**		**109.04 (=1.04 + 96.00 + 12.00)**	

1) Rated power at 24 VDC and 100% simultaneity.
2) Rated power at 24 VDC and 0.5 A.
3) The power supply is integrated in the module.

Potential group 3				
Module	**Bus power [W]**	**I/O-internal power [W]**	**I/O-external power [W]**	**Sensor/Actuator supply [W]**
X20AI4622	0.01	1.10	-	-
X20AI4622	0.01	1.10	-	-
X20AT4222	0.01	1.10	-	-
X20AT2402	0.01	0.72	-	-
X20BT9100	0.50	0.10	-	-
Subtotal		**4.12**	-	-
Total	**0.54**		**4.12**	

It is then necessary to perform a power comparison between the power needed by the I/O modules and the power supplied by the power supply modules.

Potential group 1 is supplied by the supply module integrated in the X20BR9300 bus receiver. The total power supplied by the bus, including all bus modules, is 3.34 W (= 1.52 W +1.82 W). The total amount of power that must be provided for the potential group 1 via the 24 VDC I/O supply is 14.58 W.

The power comparison indicates that the power provided by the power supply module integrated in the X20BR9300 is sufficient.

Potential group 1	Bus power [W]	Power 24 VDC I/O supply [W]
X20BR9300	+7.00	+240.00[1)]
Power requirements of I/O modules	-1.52[2)]	-14.58[3)]
Power requirements of all bus modules	-1.82	-
Remaining power	**+3.66**	**+225.42**

1) Rated power at 24 VDC and 10 A.
2) Bus power to be supplied for all I/O modules (i.e. sum of the bus power of all potential groups).
3) 24 VDC I/O supply to be provided for potential group 1.

In potential groups 2 and 3, the 24 VDC I/O supply is fed via the X20PS2100 power supply module. One power supply module is needed for each potential group.

The power comparison indicates that the power provided by the X20PS2100 is sufficient.

Potential group 2		Power 24 VDC I/O supply [W]
X20PS2100		+240.00[1)]
Power requirements of I/O modules		-109.04
Remaining power		**+130.96**

1) Rated power at 24 VDC and 10 A.

Potential group 3		Power 24 VDC I/O supply [W]
X20PS2100		+240.00[1)]
Power requirements of I/O modules		-4.12
Remaining power		**+235.88**

1) Rated power at 24 VDC and 10 A.

3.24 Power supply module power loss

3.24.1 General information

Power supply modules are used to provide power to an X20 system. The power supply modules are either a separate module or part of a CPU or a bus controller.

The power consumed by the power supply modules is passed on to the X20 system, taking into consideration its own power requirements and the effectiveness of the power supplies. The data sheets for the power supply modules list their own power requirements and power loss (as maximum power consumption). With the formulas in the following sections, the exact power consumption can also be calculated. This calculation is explained using an example.

The following image shows where the power supply module uses power for its own requirements. It also shows where the power supply module uses power to supply the system and where power loss occurs.

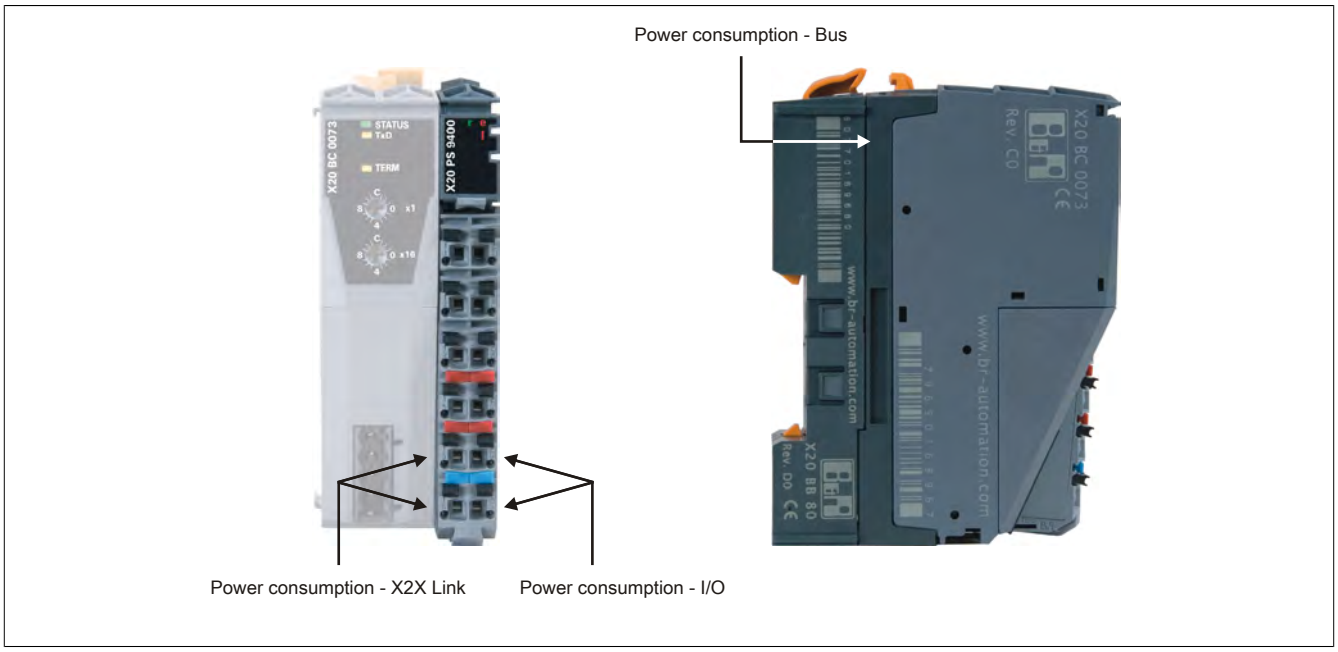


Figure 44: Power supply modules draw power at up to three supply points

3.24.2 Power supply modules without X2X Link supply

Module	Power consumption - Bus [W]	Power consumption - I/O-internal [W]	Power consumption - X67 X2X Link-internal [W]
X20PS2100	0.2	$0.1 + I_{IO}^2 \times 0.005$	-
X20PS2110	0.2	$0.1 + I_{IO}^2 \times 0.02$	-
X20BT9100	0.5	$0.1 + I_{IO}^2 \times 0.005$	-
X20BT9400	0.5	$0.1 + I_{IO}^2 \times 0.005$	$0.5 + 0.11 \times \Sigma X67$

Table 13: Power consumption of power supply modules without X2X Link supply

$I_{I/O}$ ... I/O summation current of all I/O modules supplied by this power supply module
$\Sigma X67$ ... Sum of X67 modules (max. = 8)

3.24.3 Power supply module with X2X Link supply

Module	Power consumption - Bus [W]	Power consumption - I/O-internal [W]	Power consumption - X2X Link-internal [W]
X20PS3300, X20PS9400, X20PS9500, X20CP1483, X20CP1483-1, X20CP158x, X20CP358x	0.2	$0.1 + I_{IO}^2 \times 0.005$	$0.8 + \frac{0.06 \cdot \sum P_{X2X}}{n}$
X20PS3310	0.2	$0.1 + I_{IO}^2 \times 0.02$	$0.8 + \frac{0.06 \cdot \sum P_{X2X}}{n}$
X20BR9300	0.4	$0.1 + I_{IO}^2 \times 0.005$	$0.8 + \frac{0.06 \cdot \sum P_{X2X}}{n}$
X20PS9402, X20PS9502	0.2	$0.1 + I_{IO}^2 \times 0.005$	$0.6 + 0.12 \times \Sigma P_{X2X}$

Table 14: Power consumption of power supply modules with X2X Link supply

ΣP_{X2X} ... Sum of the bus power consumption of all modules in the X20 system (compact CPU, fieldbus CPU, BC, BR, I/O, BM, BT)
n ... Number of all power supply modules in the X20 system with X2X Link supply, including X20BR9300
$I_{I/O}$ ... I/O summation current of all I/O modules supplied by this power supply module

3.24.4 Power supply module for X20 standalone devices

Module	Power consumption [W]
X20PS8002	$0.5 + 0.12 \times P_{Out}$

Table 15: Power consumption of power supply module for X20 standalone devices

P_{Out} ... Sum of power consumption values of all modules (HB) supplied by the power supply module

3.24.5 Potential distribution modules

Module	Power consumption - Bus [W]	Power consumption - I/O [W]
X20PD0011, X20PD0012	0.12	$0.15 + I_{IO}^2 \times 0.02$
X20PD0016, X20PD2113	0.12	$0.28 + I_{IO}^2 \times 0.02$

Table 16: Power consumption of potential distributor modules

$I_{I/O}$ ... PD0011, PD0012, PD0016, PD2113 with internal supply
$I_{I/O}$ corresponds to the sum of all load currents.

PD2113 with external supply (power supply module)
If the X20PD2113 module is being used as a power supply module, then $I_{I/O}$ corresponds to the summation current of all I/O modules supplied by the X20PD2113.

3.24.6 Example

Calculating the total internal power consumption of a BR9300 bus receiver with the following hardware configuration:

Module	Bus power [W]	I/O-internal power [W]
X20DI4371	0.14	0.59
X20DI2371	0.12	0.29
X20DO4322	0.16	0.49
X20DO4322	0.16	0.49
X20BT9100	0.50	0.10
Total	**1.08**	**1.96**

Two power values have to be calculated in order to determine the entire internal power consumption of the bus receiver.

- Internal X2X Link power consumption of the X20BR9300
- Internal I/O power consumption of the X20BR9300

3.24.6.1 Calculating the internal X2X Link power consumption of the X20BR9300

Bus power consumption of all modules in the X20 system

The sum of the bus power consumption from all of the modules in the X20 system is necessary in order to calculate the internal X2X Link power consumption of the X20BR9300.

The sum for the example configuration is calculated using the following formula: The bus module of the X20BR9300 does not have to be taken into account in the calculation. The power consumption of the bus module is already included with a factor of 0.8 (see formula below).

A power consumption of 0.13 W for each bus module must be included in the calculation for the 4 I/O modules and the bus transmitter.

$$\sum P_{X2X} = P_{X2XBus_{BR9300}} + \sum P_{X2XBus_{IOMod}} + \sum P_{X2XBus_{Busmod}} = 0.4 + 1.08 + 5 \cdot 0.13 = 2.13\,W$$

Internal X2X Link power consumption of the X20BR9300

The internal X2X Link power consumption of the X20BR9300 is calculated using the following formula. Since X2X Link is only supplied by the X20BR9300 bus receiver, the factor is n = 1:

$$P_{X2Xint._{BR9300}} = 0.8 + \frac{0.06 \cdot \sum P_{X2X}}{n} = 0.8 + \frac{0.06 \cdot 2.13}{1} = 0.8 + 0.13 = 0.93\,W$$

3.24.6.2 Calculating the internal I/O power consumption of the X20BR9300

The I/O summation current of all I/O modules supplied by the X20BR9300 is needed to calculate the internal I/O power consumption. The I/O summation current is composed of three parts:

- Internal power consumption of the I/O modules
- Sum of the output currents
- Sum of the actuator currents

Internal power consumption of the I/O modules

The current that results from the internal consumption of the I/O modules is calculated according to the following formula:

$$I_{IO_{int.}} = \frac{P_{IO_{int.}}}{V} = \frac{1.96}{24} = 0.082\,A$$

Sum of output and actuator currents

Two X20DO4322 modules are included in the example configuration. The following images show which outputs are wired and how high the output current and actuator current are per channel.

Connections and currents of the first X20DO4322:

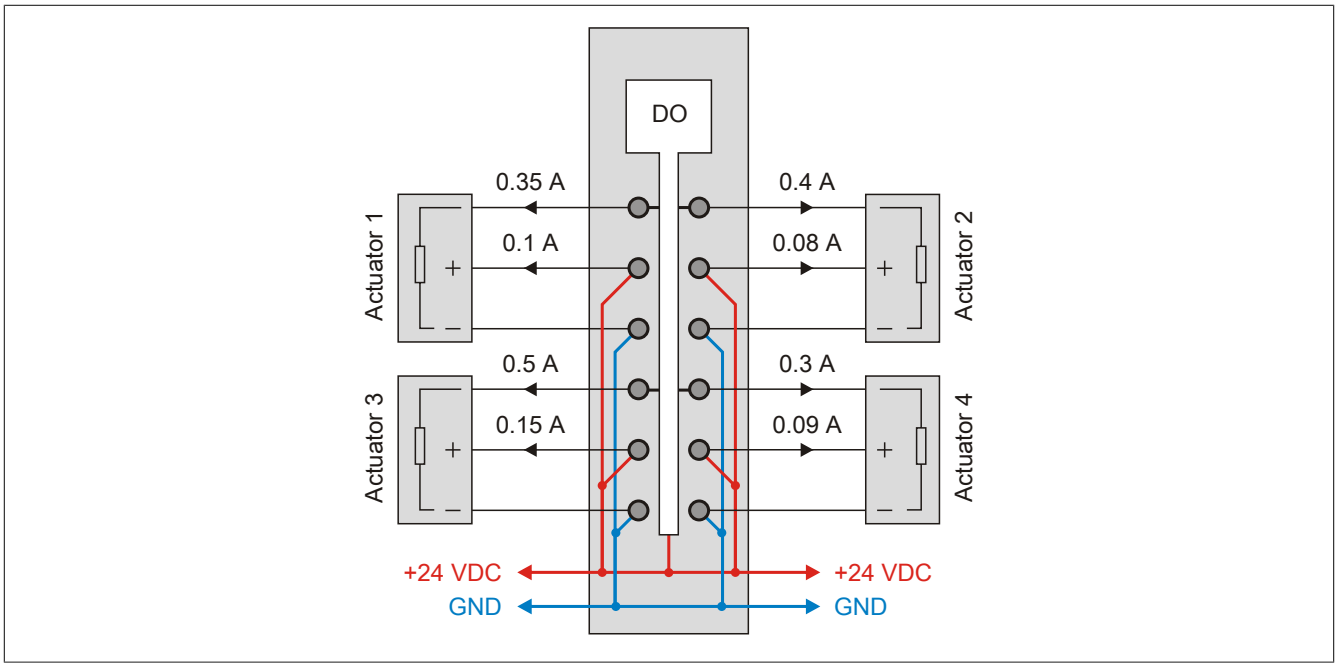


Figure 45: Connections and currents of the first X20DO4322

Connections and currents of the second X20DO4322:

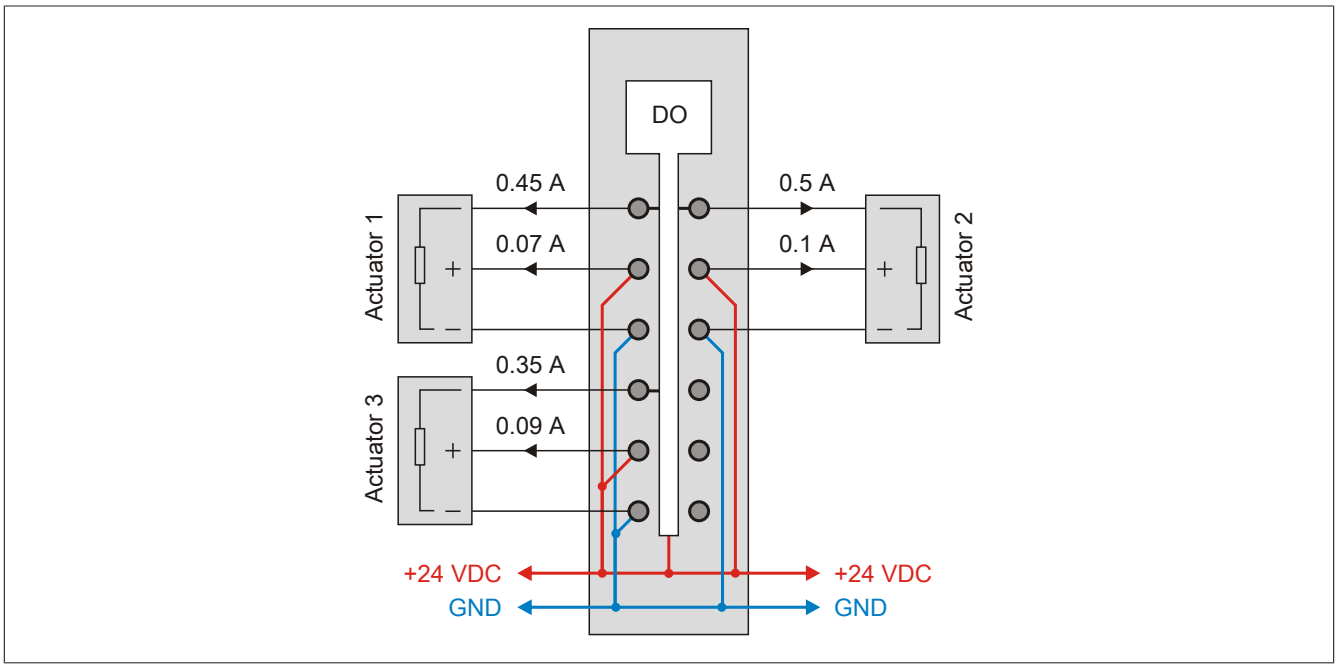


Figure 46: Connections and currents of the second X20DO4322

Calculating the sum of the output currents:

$$I_{DO} = I_{DO_1} + I_{DO_2} = 0.35 + 0.4 + 0.5 + 0.3 + 0.45 + 0.5 + 0.35 = 2.85\,A$$

Calculating the sum of the actuator currents:

$$I_{Actuator} = I_{Actuator_1} + I_{Actuator_2} = 0.1 + 0.08 + 0.15 + 0.09 + 0.07 + 0.1 + 0.09 = 0.68\,A$$

Calculating the I/O summation current

The I/O summation current is calculated from the sum of all three partial currents.

$$I_{IO} = I_{IO_{int.}} + I_{DO} + I_{Actuator} = 0.082 + 2.85 + 0.68 = 3.612\,A$$

Calculating the internal I/O power consumption of the X20BR9300

The internal I/O power consumption is calculated using the following formula:

$$P_{IOint._{BR9300}} = 0.1 + I_{IO}^2 \cdot 0.005 = 0.1 + 3.612^2 \cdot 0.005 = 0.17\,W$$

3.24.6.3 Total internal power consumption of the X20BR9300

The following 3 power values must be added together to calculate the total internal power of the X20BR9300:

- Power consumption - Bus
- Power consumption - I/O-internal
- Power consumption - X2X Link-internal

$$P_{BR9300int._{tot.}} = P_{X2XBus_{BR9300}} + P_{IOint._{BR9300}} + P_{X2Xint._{BR9300}} = 0.4 + 0.17 + 0.93 = 1.5\,W$$

Connections and currents of the second X20DO4322:

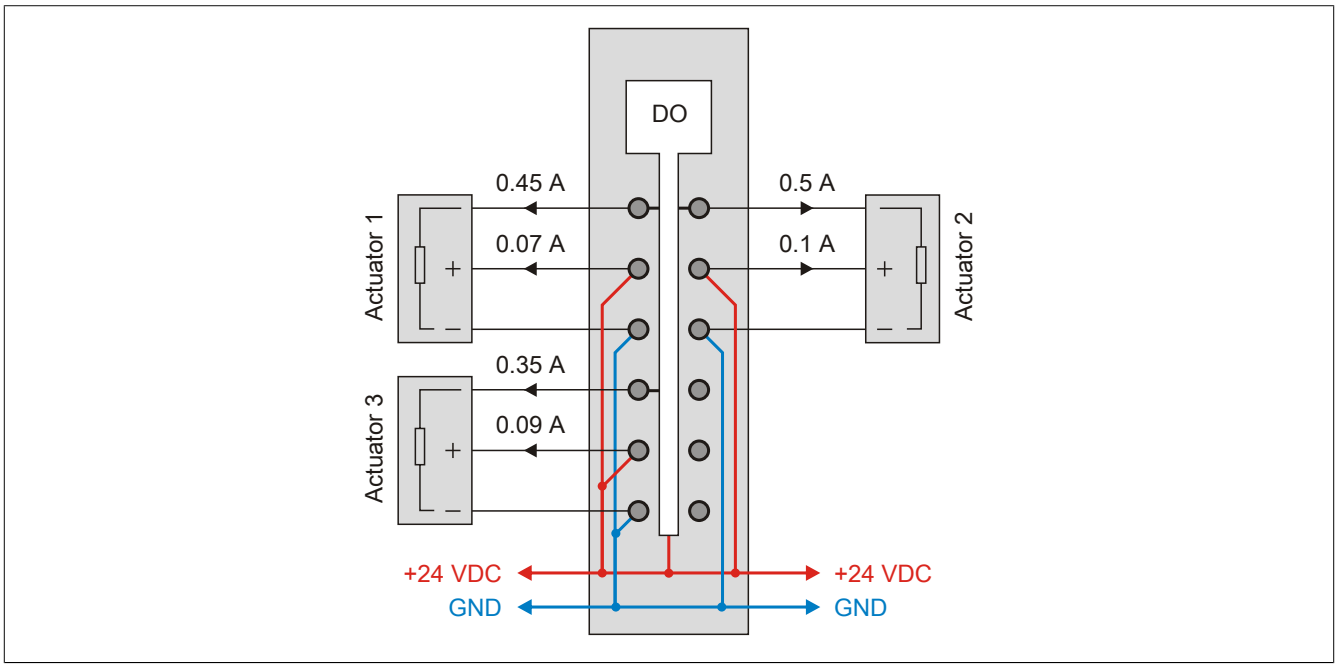


Figure 47: Connections and currents of the second X20DO4322

Calculating the sum of the output currents:

$$I_{DO} = I_{DO_1} + I_{DO_2} = 0.35 + 0.4 + 0.5 + 0.3 + 0.45 + 0.5 + 0.35 = 2.85\,A$$

Calculating the sum of the actuator currents:

$$I_{Actuator} = I_{Actuator_1} + I_{Actuator_2} = 0.1 + 0.08 + 0.15 + 0.09 + 0.07 + 0.1 + 0.09 = 0.68\,A$$

Calculating the I/O summation current

The I/O summation current is calculated from the sum of all three partial currents.

$$I_{IO} = I_{IO_{int.}} + I_{DO} + I_{Actuator} = 0.058 + 2.85 + 0.68 = 3.588\,A$$

Calculating the internal I/O power consumption of the X20BR9300

The internal I/O power consumption is calculated using the following formula:

$$P_{IO_{BR9300}} = 0.1 + I_{IO}^2 \cdot 0.005 = 0.1 + 3.588^2 \cdot 0.005 = 0.16\,W$$

4 X20 system modules

4.1 Module overview: Alphabetically

Order data	Short description
X20AI1744	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 kHz input filter
X20AI1744-3	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 Hz input filter
X20AI2222	X20 analog input module, 2 inputs, ±10 V, 13-bit converter resolution, configurable input filter
X20AI2237	X20 analog input module, 2 inputs, ±10 V, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply
X20AI2322	X20 analog input module, 2 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter
X20AI2437	X20 analog input module, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply
X20AI2438	X20 analog input module, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply, supports HART protocol
X20AI2622	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter
X20AI2632	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20AI2632-1	X20 analog input module, 2 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter
X20AI2636	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions
X20AI4222	X20 analog input module, 4 inputs, ±10 V, 13-bit converter resolution, configurable input filter
X20AI4322	X20 analog input module, 4 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter
X20AI4622	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter
X20AI4632	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20AI4632-1	X20 analog input module, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20AI4636	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions
X20AI8221	X20 analog input module, 8 inputs, ±10 V, 13-bit converter resolution
X20AI8321	X20 analog input module, 8 inputs, 0 to 20 mA, 12-bit converter resolution
X20AIA744	X20 analog input module, 2 full-bridge strain gauge inputs, 24-bit converter resolution, 2.5 kHz input filter
X20AIB744	X20 analog input module, 4 full-bridge strain gauge inputs, 24-bit converter resolution, 2.5 kHz input filter
X20AO2437	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated
X20AO2438	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated, supports HART protocol
X20AO2622	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution
X20AO2632	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution
X20AO2632-1	X20 analog output module, 2 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution
X20AO4622	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution
X20AO4632	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution
X20AO4632-1	X20 analog output module, 4 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution
X20AO4635	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, low temperature drift
X20AP3111	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 20 mA AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20AP3121	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20AP3131	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 5 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20AP3161	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 333 mV AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20AT2222	X20 temperature input module, 2 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections
X20AT2311	X20 temperature input module, 2 inputs for resistance measurement, PT100, resolution 0.001°C, 4-wire connections
X20AT2402	X20 temperature input module, 2 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C
X20AT4222	X20 temperature input module, 4 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections
X20AT6402	X20 temperature input module, 6 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C
X20ATA312	X20 temperature input module, 2 inputs for resistance measurement, PT100, resolution 0.01 °C, 4-wire connections
X20ATA492	X20 temperature input module, 2 thermocouple inputs, type J, K, N, S, B, R, E, C, T, single channel electrically isolated, 2x PT1000 integrated for terminal temperature compensation, with 1x X20TB1E terminal block, order terminal block separately
X20ATB312	X20 temperature input module, 4 inputs for resistance measurement, PT100, resolution 0.01 °C, 4-wire connections
X20ATC402	X20 temperature input module, 6 thermocouple inputs, type J, K, N, S, B, R, E, C, T, 2x PT1000 integrated for terminal temperature compensation, with 1x X20TB1E terminal block, order terminal block separately
X20BB22	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB27	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB32	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB37	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, Slot for X20 interface module, X20 connection, X20 locking plates X20AC0SL1/X20AC0SR1 (left and right) included
X20BB42	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB47	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included

Order data	Short description
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BC0043	X20 bus controller, 1 CANopen interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately
X20BC0043-10	X20 bus controller, 1 CANopen interface, FieldbusDESIGNER supported, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately
X20BC0053	X20 bus controller, 1 DeviceNet interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately
X20BC0063	X20 bus controller, 1 PROFIBUS DP interface, 9-pin DSUB connection, order bus base, power supply module and terminal block separately
X20BC0073	X20 bus controller, 1 CAN I/O interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately
X20BC0083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, 2x RJ45, order bus base, power supply module and terminal block separately.
X20BC0087	X20 bus controller, 1 Modbus TCP or Modbus UDP interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately.
X20BC0088	X20 bus controller, 1 EtherNet/IP interface, integrated switch, web interface, 2x RJ45, order bus base, power supply module and terminal block separately
X20BC00E3	X20 bus controller, 1 PROFINET RT interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately.
X20BC00G3	X20 bus controller, 1 EtherCAT interface, 2x RJ45, order bus base, power supply module and terminal block separately
X20BC0143-10	X20 bus controller, 1 CANopen interface, 9-pin DSUB, FieldbusDESIGNER supported, order 1x 7AC911.9 terminal block separately Order bus base, power supply module and terminal separately
X20BC1083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, supports X20 interface module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20BC8083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, supports X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20BC8084	X20 bus controller, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20BC80G3	X20 bus controller, 1 EtherNet/IP interface, supports expansion with X20 EtherCAT junction modules, 2x RJ45, order bus base, power supply module and terminal block separately.
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left
X20BM05	X20 power supply bus module, with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous
X20BM21	X20 power supply bus module, for double-width modules, 24 VDC keyed, internal I/O supply interrupted to the left
X20BM31	X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous
X20BM32	X20 bus module for double-width modules, 240 VAC keyed, internal I/O supply continuous
X20BR9300	X20 bus receiver, X2X Link, supply for X2X Link and internal I/O supply, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BT9100	X20 bus transmitter, X2X Link, supply for internal I/O supply
X20BT9400	X20 bus transmitter X2X Link, feed for internal I/O supply, X2X Link supply for X67 modules, reverse polarity protection, short circuit protection, overload protection, parallel connection possible, redundancy operation possible
X20CM0985	X20 digital and analog mixed module, multi-measurement transducer/ synchronization module, 5 digital outputs, 24 VDC, 0.5 A source, 1 relay, 1 A, changeover contact, 8 analog inputs, ±480 V / 120 V, 16-bit converter resolution, 3 analog inputs 5 A / 1 A AC, 16-bit converter resolution, order terminal blocks 0TB3102-7011, 0TB3104-7011, 0TB3102-7012, 0TB3104-7012 and 2x TB12 separately.
X20CM0985-1	X20 digital and analog mixed module, multi-measurement transducer/ synchronization module, 5 digital outputs, 24 VDC, 0.5 A, source, 1 relay 1 A, 8 analog inputs, ±480 V / 120 V, 16-bit converter resolution, 3 analog inputs 5 A / 1 A AC, 16-bit converter resolution, additional software functions, order terminal blocks 0TB3102-7011, 0TB3104-7011, 0TB3102-7012, 0TB3104-7012 and 2x X20TB12 separately
X20CM1201	X20 combination module, 1 AB incremental encoder, 24 V, 4 digital inputs 24 V, 4 channels 24 V configurable as inputs or outputs, flexible digital controller logic
X20CM1941	X20 resolver module, 14-bit resolver input, converter up to 12-bit ABR output
X20CM4810	X20 analog input module for vibration measurement and analysis for condition monitoring, 4 IEPE analog inputs, 51.5625 kHz sampling frequency, 24-bit converter resolution
X20CM6209	X20 diode array module, 1 A, 40 V reverse voltage, no module status data
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement
X20CM8323	X20 PWM module, 8 digital outputs for switching electromechanical loads, 0.6 A continuous current, 2 A peak current, current monitoring, switching time detection
X20CP1301	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 1 GB flash drive onboard, 1 insert slot for X20 interface modules, 1 USB interface, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including power supply module, 3x X20TB1F terminal blocks, slot cover and X20 locking plate X20AC0SR1 (right) included
X20CP1381	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included

Order data	Short description
X20CP1381-RT	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, reACTION technology, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included
X20CP1382	X20 CPU, with integrated I/O, x86-400, 256 MB DDR3 RAM, 32 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included
X20CP1382-RT	X20 CPU, with integrated I/O, x86-400, 256 MB DDR3 RAM, 32 kB FRAM, 2 GB flash drive on board, 2 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, reACTION technology, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included
X20CP0201	X20 compact CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, order bus base, power supply module and terminal block separately
X20CP0291	X20 compact CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, 1 Ethernet interface 100 Base-T, order bus base, power supply module and terminal block separately
X20CP0292	X20 compact CPU, µP 25, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, 3 Ethernet interface 750 Base-T, order bus base, power supply module and terminal block separately
X20CP1483	X20 CPU, x86 100 MHz Intel compatible, 32 MB DRAM, 128 kB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1483-1	X20 CPU, x86 100 MHz Intel compatible, 64 MB DRAM, 128 kB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1583	X20 CPU, ATOM 333 MHz compatible, 128 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1584	X20 CPU, ATOM 0.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1585	X20 CPU, ATOM 1.0 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1586	X20 CPU, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP3583	X20 CPU, ATOM 333 MHz compatible, 128 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP3584	X20 CPU, ATOM 0.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.
X20CP3585	X20 CPU, ATOM 1.0 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.
X20CP3586	X20 CPU, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.
X20CS1011	X20 interface module, 1 Moeller SmartWire interface
X20CS1012	X20 interface module, 1 M-Bus master interface, integrated slave supply
X20CS1013	X20 interface module, 1 DALI master interface
X20CS1020	X20 interface module, 1 RS232 interface, max. 115.2 kbit/s
X20CS1030	X20 interface module, 1 RS422/485 interface, max. 115.2 kbit/s
X20CS1070	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, object buffers in both send and receive directions
X20CS2770	X20 interface module, 2 CAN bus interfaces, max. 1 Mbit/s, object buffers in both send and receive directions
X20DC1073	X20 digital counter module, 1x SinCos, 1 Vss, 400 kHz input frequency, encoder monitoring, NetTime module
X20DC1176	X20 digital counter module, 1 ABR incremental encoder, 5 V 600 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC1178	X20 digital counter module, 1 SSI absolute encoders, 5 V, 1 Mbit/s, 32-bit, encoder monitoring, NetTime module
X20DC1196	X20 digital counter module, 1 ABR incremental encoders, 5 V, 600 kHz input frequency, 4x evaluation
X20DC1198	X20 digital counter module, 1 SSI absolute encoder, 5 V, 1 Mbit/s, 32-bit
X20DC11A6	X20 digital counter module, 1 ABR incremental encoder, 5 V 5 MHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC1376	X20 digital counter module, 1 ABR incremental encoder, 24 V 100 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC137A	X20 digital counter module, 1x ABR incremental encoder, 24 V (differential), 300 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC1396	X20 digital counter module, 1 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation
X20DC1398	X20 digital counter module, 1 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit
X20DC1976	X20 digital counter module, 1x ABR incremental encoder, 5 V (single ended), 250 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC2190	X20 digital counter module, ultrasonic transducer module, interfaces: EP start/stop, DPI/IP, 2 transducer rods, 4 path evaluation
X20DC2395	X20 digital counter module, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function

Order data	Short description
X20DC2396	X20 digital counter module, 2 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation
X20DC2398	X20 digital counter module, 2 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit
X20DC4395	X20 digital counter module, 2 SSI absolute encoder, 24 V, 2 ABR incremental encoder, 24 V, 4 AB incremental encoders, 24 V, 8 event counters or 4 PWM, local time measurement function
X20DI0471	X20 digital input module, 10 inputs, 48 VDC, sink, configurable input filter, 1-wire connections
X20DI2371	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 3-wire connections
X20DI2372	X20 digital input module, 2 inputs, 24 VDC, source, configurable input filter, 3-wire connections
X20DI2377	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 2 event counters 50 kHz, 3-wire connections
X20DI2653	X20 digital input module, 2 inputs, 100 to 240 VAC, 240 V keyed, 3-wire connections
X20DI4371	X20 digital input module, 4 inputs, 24 VDC, sink, configurable input filter, 3-wire connections
X20DI4372	X20 digital input module, 4 inputs, 24 VDC, source, configurable input filter, 3-wire connections
X20DI4375	X20 digital input module, 4 inputs, 24 VDC, sink, configurable input filter, open line and short circuit detection, 3-wire connections
X20DI4653	X20 digital input module, 4 inputs, 100 to 240 VAC, 240 V keyed, 2-wire connections
X20DI4760	X20 digital input module, 4 NAMUR inputs, 8.05 V
X20DI6371	X20 digital input module, 6 inputs, 24 VDC, sink, configurable input filter, 2-wire connections
X20DI6372	X20 digital input module, 6 inputs, 24 VDC, source, configurable input filter, 2-wire connections
X20DI6373	X20 digital input module, 6 inputs, 24 VDC, sink/source, all inputs floating, configurable input filter, 2-wire connections
X20DI6553	X20 digital input module, 6 inputs, 100 to 120 VAC, 240 V keyed, 1-wire connections
X20DI8371	X20 digital input module, 8 inputs, 24 VDC, sink, configurable input filter, 1-wire connections
X20DI9371	X20 digital input module, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections
X20DI9372	X20 digital input module, 12 inputs, 24 VDC, source, configurable input filter, 1-wire connections
X20DID371	X20 digital input module, 8 inputs, 24 VDC, sink, configurable input filter, 2-wire connections
X20DIF371	X20 digital input module, 16 inputs, 24 VDC, sink, configurable input filter, 1-wire connections
X20DM9324	X20 digital mixed module, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source 1-wire connections
X20DO2321	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, sink, 3-wire connections
X20DO2322	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, source, 3-wire connections
X20DO2623	X20 digital output module, 2 outputs, 100-240 VAC, 1 A, source, 240 V keyed, 3-wire connections
X20DO2633	X20 digital output module, 2 triac outputs, 12 to 240 VAC, 2 A, L switching, phase angle control, 240 V keyed
X20DO2649	X20 digital output module, 2 relays, changeover contacts, 240 VAC / 5 A, 24 VDC / 5 A
X20DO4321	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, sink, 3-wire connections
X20DO4322	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections
X20DO4331	X20 digital output module, 4 outputs, 24 VDC, 2 A, sink, 3-wire connections
X20DO4332	X20 digital output module, 4 outputs, 24 VDC, 2 A, source, 3-wire connections
X20DO4529	X20 digital output module, 4 relays, changeover contacts, 115 VAC / 0.5 A, 24 VDC / 1 A
X20DO4613	X20 digital output module, 4 triac coupler outputs, 12 to 240 VAC, 50 mA, zero-crossing detection, 240 V keyed,...
X20DO4623	X20 digital output module, 4 outputs, 100-240 VAC, 0.5 A, source, 240 V keyed, 2-wire connections
X20DO4633	X20 digital output module, 4 triac outputs, 12 to 240 VAC, 1 A, L switching, phase angle control, 240 V keyed
X20DO4649	X20 digital output module, 4 relays, N.O. contacts, 240 VAC / 5 A
X20DO6321	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections
X20DO6322	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections
X20DO6325	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, open line and overload detection, 2-wire connections
X20DO6529	X20 digital output module, 6 relays, normally open contacts, 115 VAC / 0.5 A, 30 VDC / 1 A
X20DO6639	X20 digital output module, 6 relays, normally open contacts, 240 VAC / 2 A, 30 VDC / 2 A
X20DO8232	X20 digital output module, 8 outputs, 12 VDC, 2 A, source, supply directly on module, 1-wire connections
X20DO8322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20DO8323	X20 digital output module, 8 outputs, 12 to 24 V, 0.5 A, sink/source, 1-wire connections, full bridge, half bridge, thermal overload protection
X20DO8331	X20 digital output module, 8 outputs, 24 VDC, 2 A, sink, supply directly on module, 1-wire connections
X20DO8332	X20 digital output module, 8 outputs, 24 VDC, 2 A, source, supply directly on module, 1-wire connections
X20DO9321	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections
X20DO9322	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20DOD322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 2-wire connections
X20DOF322	X20 digital output module, 16 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20DS1119	X20 multifunctional digital signal processor, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module
X20DS1319	X20 multifunctional digital signal processor, 4 digital input channels, 4 digital channels configurable as inputs or outputs, 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 2 reference pulses, SSI absolute encoder, NetTime module
X20DS1828	X20 digital signal module, 1 HIPERFACE interface, NetTime module
X20DS1928	X20 digital signal module, 1 EnDat 2.1/2.2 interface, NetTime module
X20DS4387	X20 digital signal module, 4x IO-Link master, 4 digital channels configurable as inputs or outputs, 3-wire connections
X20DS4389	X20 digital signal module, 4 digital inputs, 24 VDC, 4 digital outputs, 24 VDC, 0.1 A, oversampling I/O functions, time-triggered I/O functions, NetTime module
X20DS438A	X20 digital signal module, 4x I/O-Link master V1.1, can also be configured as 4x digital input or output channels, 3-wire connections
X20ET8819	X20 Ethernet analysis tool, can be expanded with active hub modules, 2x RJ45
X20HB1881	X20 hub expansion module, integrated 1-port hub, for fiber optic cable
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable
X20HB2885	X20 hub expansion module, integrated active 2-port hub, 2x RJ45
X20HB2886	X20 hub expansion module, integrated active 2-port hub, 2 fiber optic interfaces
X20HB28G0	X20 EtherCAT junction module, integrated 2-port EtherCAT junction, 2x RJ45
X20HB8815	X20 POWERLINK - TCP/IP gateway, can be expanded with active hub modules, 2x RJ45
X20HB8880	X20 base hub module, integrated 2-port hub, 2x RJ45
X20HB8884	X20 compact link selector, 2x RJ45, order bus base, power supply module and terminal block separately.

Order data	Short description
X20HB88G0	X20 EtherCAT junction (basic module), integrated 2-port EtherCAT junction, 2x RJ45
X20IF0000	X20 dummy interface module (non-functional)
X20IF1020	X20 interface module, 1 RS232 interface, max. 115.2 kbit/s, electrically isolated
X20IF1030	X20 interface module, 1 RS422/485 interface, max. 115.2 kbit/s, electrically isolated
X20IF1041-1	X20 interface module, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1043-1	X20 interface module, for DTM configuration, 1 CANopen slave interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1051-1	X20 interface module, for DTM configuration, 1 DeviceNet scanner (master) interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1053-1	X20 interface module, for DTM configuration, 1 DeviceNet adapter (slave) interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1061	X20 interface module, 1 PROFIBUS DP V0/V1 master interface, max. 12 Mbit/s, max. 3.5 kB input data and max. 3.5 kB output data, electrically isolated
X20IF1061-1	X20 interface module for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated
X20IF1063	X20 interface module, 1 PROFIBUS DP V0 slave interface, max. 12 Mbit/s, electrically isolated
X20IF1063-1	X20 interface module, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated
X20IF1065	X20 interface module, 1 PROFIBUS DP V1 slave interface, max. 12 Mbit/s, electrically isolated
X20IF1072	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately
X20IF1074	X20 interface module, for SGC, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately
X20IF1082	X20 interface module, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function
X20IF1082-2	X20 interface module, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function PRC function
X20IF1086-2	X20 interface module, 1 POWERLINK interface, managing or controlled node, PRC function, 1 fiber optic connection
X20IF1091	X20 interface module, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately
X20IF1091-1	X20 interface module, for expandable bus controller, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately
X20IF10A1-1	X20 interface module, for DTM configuration, 1 ASi master interface, electrically isolated, order 1x TB704 terminal block separately
X20IF10D1-1	X20 interface module, for DTM configuration, 1 EtherNet/IP scanner (master) interface, electrically isolated
X20IF10D3-1	X20 interface module, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated
X20IF10E1-1	X20 interface module for DTM configuration, 1 PROFINET RT controller (master) interface, electrically isolated
X20IF10E3-1	X20 interface module, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated
X20IF10G3-1	X20 interface module for DTM configuration, 1 EtherCAT slave interface, electrically isolated
X20IF10X0	X20 interface module, 1 redundancy link interface 1000BASE-SX, CPU-CPU data synchronization module for controller redundancy
X20IF2181-2	X20 interface module, 1x link selector for POWERLINK cable redundancy, POWERLINK functions: - Managing node - Controlled node for iCN operation - Redundant managing node for controller redundancy - Ring redundancy - 2x hub - Multi ASend - PRC function 2x RJ45
X20IF2772	X20 interface module, 2 CAN bus interfaces, max. 1 Mbit/s, electrically isolated, order 2x TB2105 terminal block separately
X20IF2792	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, 1 X2X Link master interface, electrically isolated, order 1x TB2105 and 1x TB704 terminal block separately
X20MM2436	X20 PWM motor module, 24 to 39 VDC ±25%, 2 PWM motor bridges, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, configurable as incremental encoder
X20MM3332	X20 digital motor module, 24 VDC, 3 digital outputs, full bridge (H bridge), 3 A continuous current, 5 A peak current
X20MM4331	X20 digital motor module, 24 VDC, 4 digital outputs, half bridge, 3 A continuous current, 5 A peak current
X20MM4456	X20 PWM motor module, 24 to 48 VDC ±25%, 4 PWM motor bridges, 6 A continuous current, 10 A peak current, 4x 4 digital inputs 24 VDC, sink, configurable as incremental encoder
X20PD0011	X20 potential distributor module, 12x GND, integrated microfuse
X20PD0012	X20 potential distributor module, 12x 24 VDC, integrated microfuse
X20PD0016	X20 potential distributor module, 5x GND, 5x 24 VDC, each with 1x floating feed, integrated microfuse
X20PD2113	X20 potential distributor module, 6x GND, 6x 24 VDC, with feed option, integrated microfuse
X20PS2100	X20 power supply module, for internal I/O supply
X20PS2110	X20 supply module, for internal I/O supply, integrated microfuse
X20PS3300	X20 power supply module, for X2X Link and internal I/O supply
X20PS3310	X20 power supply module, for X2X Link and internal I/O supply, integrated microfuse
X20PS4951	X20 power supply module, for potentiometers, 4x ±10 V for potentiometer supply
X20PS8002	X20 power supply module for standalone hub and compact link selector
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated
X20PS9500	X20 supply module for compact and fieldbus CPUs and internal I/O supply, X2X Link supply
X20PS9502	X20 supply module, for compact and fieldbus CPUs and internal I/O supply, X2X Link supply, supply not electrically isolated
X20RT8001	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, reACTION technology module
X20RT8201	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, 2 analog inputs ±10 V, 500 kHz sampling frequency, 13-bit converter resolution (including sign), configurable input filter, reACTION technology module
X20SM1426	X20 stepper motor module, 1 motor connection, 1 A continuous current, 1.2 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder
X20SM1436	X20 stepper motor module, module supply 24-39 VDC ±25%, 1 motor connection, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed
X20TB1E	X20 terminal block, 12-pin, 24 VDC keyed, 2x PT1000 integrated for terminal temperature compensation
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed
X20XC0201	X20 fieldbus CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus and interface module according to fieldbus CPU base, order power supply module, bus base and terminal block separately

Order data	Short description
X20XC0202	X20 fieldbus CPU, µP 25, 750 kB SRAM, 3 MB FlashPROM, support of RS232, CAN bus and interface module according to fieldbus CPU base, order power supply module, bus base and terminal block separately
X20XC0292	X20 fieldbus CPU, µP 25 750 kB SRAM, 3 MB FlashPROM, support of RS232, CAN bus and interface module, according to fieldbus CPU base, 1 Ethernet interface 100 Base-T, order bus base, power supply module and terminal block separately
X20ZF0000	Dummy X20 module (non-functional)
X20ZF000F	Dummy X20 module (non-functional)

4.2 Module overview: Grouped

4.2.1 CPUs

Standard CPU

Order data	Short description
X20CP1301	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 1 GB flash drive onboard, 1 insert slot for X20 interface modules, 1 USB interface, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including power supply module, 3x X20TB1F terminal blocks, slot cover and X20 locking plate X20AC0SR1 (right) included
X20CP1381	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included
X20CP1382	X20 CPU, with integrated I/O, x86-400, 256 MB DDR3 RAM, 32 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included
X20CP1483	X20 CPU, x86 100 MHz Intel compatible, 32 MB DRAM, 128 kB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1483-1	X20 CPU, x86 100 MHz Intel compatible, 64 MB DRAM, 128 kB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1583	X20 CPU, ATOM 333 MHz compatible, 128 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1584	X20 CPU, ATOM 0.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1585	X20 CPU, ATOM 1.0 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1586	X20 CPU, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP3583	X20 CPU, ATOM 333 MHz compatible, 128 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP3584	X20 CPU, ATOM 0.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.
X20CP3585	X20 CPU, ATOM 1.0 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.
X20CP3586	X20 CPU, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.

Compact CPU

Order data	Short description
X20CP0201	X20 compact CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, order bus base, power supply module and terminal block separately
X20CP0291	X20 compact CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, 1 Ethernet interface 100 Base-T, order bus base, power supply module and terminal block separately
X20CP0292	X20 compact CPU, µP 25, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, 3 Ethernet interface 750 Base-T, order bus base, power supply module and terminal block separately

Fieldbus CPU

Order data	Short description
X20XC0201	X20 fieldbus CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus and interface module according to fieldbus CPU base, order power supply module, bus base and terminal block separately
X20XC0202	X20 fieldbus CPU, µP 25, 750 kB SRAM, 3 MB FlashPROM, support of RS232, CAN bus and interface module according to fieldbus CPU base, order power supply module, bus base and terminal block separately
X20XC0292	X20 fieldbus CPU, µP 25 750 kB SRAM, 3 MB FlashPROM, support of RS232, CAN bus and interface module, according to fieldbus CPU base, 1 Ethernet interface 100 Base-T, order bus base, power supply module and terminal block separately

reACTION Technology CPU

Order data	Short description
X20CP1381-RT	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, reACTION technology, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included
X20CP1382-RT	X20 CPU, with integrated I/O, x86-400, 256 MB DDR3 RAM, 32 kB FRAM, 2 GB flash drive on board, 2 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, reACTION technology, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included

4.2.2 Module overview: Grouped

Analog inputs

Order data	Short description
X20AI1744	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 kHz input filter
X20AI1744-3	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 Hz input filter
X20AI2222	X20 analog input module, 2 inputs, ±10 V, 13-bit converter resolution, configurable input filter
X20AI2237	X20 analog input module, 2 inputs, ±10 V, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply
X20AI2322	X20 analog input module, 2 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter
X20AI2437	X20 analog input module, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply
X20AI2438	X20 analog input module, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply, supports HART protocol
X20AI2622	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter
X20AI2632	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20AI2632-1	X20 analog input module, 2 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter
X20AI2636	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions
X20AI4222	X20 analog input module, 4 inputs, ±10 V, 13-bit converter resolution, configurable input filter
X20AI4322	X20 analog input module, 4 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter
X20AI4622	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter
X20AI4632	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20AI4632-1	X20 analog input module, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20AI4636	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions
X20AI8221	X20 analog input module, 8 inputs, ±10 V, 13-bit converter resolution
X20AI8321	X20 analog input module, 8 inputs, 0 to 20 mA, 12-bit converter resolution
X20AIA744	X20 analog input module, 2 full-bridge strain gauge inputs, 24-bit converter resolution, 2.5 kHz input filter
X20AIB744	X20 analog input module, 4 full-bridge strain gauge inputs, 24-bit converter resolution, 2.5 kHz input filter
X20AP3111	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 20 mA AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20AP3121	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20AP3131	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 5 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20AP3161	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 333 mV AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement

Analog outputs

Order data	Short description
X20AO2437	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated
X20AO2438	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated, supports HART protocol
X20AO2622	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution
X20AO2632	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution
X20AO2632-1	X20 analog output module, 2 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution
X20AO4622	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution
X20AO4632	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution
X20AO4632-1	X20 analog output module, 4 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution
X20AO4635	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, low temperature drift
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement

Bus controllers

Order data	Short description
X20BC0043	X20 bus controller, 1 CANopen interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately
X20BC0043-10	X20 bus controller, 1 CANopen interface, FieldbusDESIGNER supported, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately
X20BC0053	X20 bus controller, 1 DeviceNet interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately
X20BC0063	X20 bus controller, 1 PROFIBUS DP interface, 9-pin DSUB connection, order bus base, power supply module and terminal block separately
X20BC0073	X20 bus controller, 1 CAN I/O interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately
X20BC0083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, 2x RJ45, order bus base, power supply module and terminal block separately.
X20BC0087	X20 bus controller, 1 Modbus TCP or Modbus UDP interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately.
X20BC0088	X20 bus controller, 1 EtherNet/IP interface, integrated switch, web interface, 2x RJ45, order bus base, power supply module and terminal block separately
X20BC00E3	X20 bus controller, 1 PROFINET RT interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately.
X20BC00G3	X20 bus controller, 1 EtherCAT interface, 2x RJ45, order bus base, power supply module and terminal block separately
X20BC0143-10	X20 bus controller, 1 CANopen interface, 9-pin DSUB, FieldbusDESIGNER supported, order 1x 7AC911.9 terminal block separately Order bus base, power supply module and terminal separately

Bus modules

Order data	Short description
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left
X20BM05	X20 power supply bus module, with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous
X20BM21	X20 power supply bus module, for double-width modules, 24 VDC keyed, internal I/O supply interrupted to the left
X20BM31	X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous
X20BM32	X20 bus module for double-width modules, 240 VAC keyed, internal I/O supply continuous

Bus receivers and transmitters

Order data	Short description
X20BR9300	X20 bus receiver, X2X Link, supply for X2X Link and internal I/O supply, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BT9100	X20 bus transmitter, X2X Link, supply for internal I/O supply
X20BT9400	X20 bus transmitter X2X Link, feed for internal I/O supply, X2X Link supply for X67 modules, reverse polarity protection, short circuit protection, overload protection, parallel connection possible, redundancy operation possible

Counter functions

Order data	Short description
X20CM1201	X20 combination module, 1 AB incremental encoder, 24 V, 4 digital inputs 24 V, 4 channels 24 V configurable as inputs or outputs, flexible digital controller logic
X20CM1941	X20 resolver module, 14-bit resolver input, converter up to 12-bit ABR output
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement
X20DC1073	X20 digital counter module, 1x SinCos, 1 Vss, 400 kHz input frequency, encoder monitoring, NetTime module
X20DC1176	X20 digital counter module, 1 ABR incremental encoder, 5 V 600 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC1178	X20 digital counter module, 1 SSI absolute encoders, 5 V, 1 Mbit/s, 32-bit, encoder monitoring, NetTime module
X20DC1196	X20 digital counter module, 1 ABR incremental encoders, 5 V, 600 kHz input frequency, 4x evaluation
X20DC1198	X20 digital counter module, 1 SSI absolute encoder, 5 V, 1 Mbit/s, 32-bit
X20DC11A6	X20 digital counter module, 1 ABR incremental encoder, 5 V 5 MHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC1376	X20 digital counter module, 1 ABR incremental encoder, 24 V 100 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC1396	X20 digital counter module, 1 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation
X20DC137A	X20 digital counter module, 1x ABR incremental encoder, 24 V (differential), 300 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC1398	X20 digital counter module, 1 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit
X20DC1976	X20 digital counter module, 1x ABR incremental encoder, 5 V (single ended), 250 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module
X20DC2190	X20 digital counter module, ultrasonic transducer module, interfaces: EP start/stop, DPI/IP, 2 transducer rods, 4 path evaluation
X20DC2395	X20 digital counter module, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function
X20DC2396	X20 digital counter module, 2 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation
X20DC2398	X20 digital counter module, 2 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit
X20DC4395	X20 digital counter module, 2 SSI absolute encoder, 24 V, 2 ABR incremental encoder, 24 V, 4 AB incremental encoders, 24 V, 8 event counters or 4 PWM, local time measurement function

Digital inputs

Order data	Short description
X20CM1201	X20 combination module, 1 AB incremental encoder, 24 V, 4 digital inputs 24 V, 4 channels 24 V configurable as inputs or outputs, flexible digital controller logic
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement
X20DI0471	X20 digital input module, 10 inputs, 48 VDC, sink, configurable input filter, 1-wire connections
X20DI2371	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 3-wire connections
X20DI2372	X20 digital input module, 2 inputs, 24 VDC, source, configurable input filter, 3-wire connections
X20DI2377	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 2 event counters 50 kHz, 3-wire connections
X20DI2653	X20 digital input module, 2 inputs, 100 to 240 VAC, 240 V keyed, 3-wire connections
X20DI4371	X20 digital input module, 4 inputs, 24 VDC, sink, configurable input filter, 3-wire connections
X20DI4372	X20 digital input module, 4 inputs, 24 VDC, source, configurable input filter, 3-wire connections
X20DI4375	X20 digital input module, 4 inputs, 24 VDC, sink, configurable input filter, open line and short circuit detection, 3-wire connections
X20DI4653	X20 digital input module, 4 inputs, 100 to 240 VAC, 240 V keyed, 2-wire connections
X20DI4760	X20 digital input module, 4 NAMUR inputs, 8.05 V
X20DI6371	X20 digital input module, 6 inputs, 24 VDC, sink, configurable input filter, 2-wire connections
X20DI6372	X20 digital input module, 6 inputs, 24 VDC, source, configurable input filter, 2-wire connections
X20DI6373	X20 digital input module, 6 inputs, 24 VDC, sink/source, all inputs floating, configurable input filter, 2-wire connections
X20DI6553	X20 digital input module, 6 inputs, 100 to 120 VAC, 240 V keyed, 1-wire connections
X20DI8371	X20 digital input module, 8 inputs, 24 VDC, sink, configurable input filter, 1-wire connections
X20DI9371	X20 digital input module, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections
X20DI9372	X20 digital input module, 12 inputs, 24 VDC, source, configurable input filter, 1-wire connections
X20DID371	X20 digital input module, 8 inputs, 24 VDC, sink, configurable input filter, 2-wire connections
X20DIF371	X20 digital input module, 16 inputs, 24 VDC, sink, configurable input filter, 1-wire connections
X20DM9324	X20 digital mixed module, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source 1-wire connections
X20DS1119	X20 multifunctional digital signal processor, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module
X20DS1319	X20 multifunctional digital signal processor, 4 digital input channels, 4 digital channels configurable as inputs or outputs, 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 2 reference pulses, SSI absolute encoder, NetTime module
X20RT8001	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, reACTION technology module
X20RT8201	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, 2 analog inputs ±10 V, 500 kHz sampling frequency, 13-bit converter resolution (including sign), configurable input filter, reACTION technology module

Digital inputs/outputs

Order data	Short description
X20CM1201	X20 combination module, 1 AB incremental encoder, 24 V, 4 digital inputs 24 V, 4 channels 24 V configurable as inputs or outputs, flexible digital controller logic
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement
X20DM9324	X20 digital mixed module, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source 1-wire connections
X20RT8001	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, reACTION technology module
X20RT8201	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, 2 analog inputs ±10 V, 500 kHz sampling frequency, 13-bit converter resolution (including sign), configurable input filter, reACTION technology module

Digital outputs

Order data	Short description
X20CM1201	X20 combination module, 1 AB incremental encoder, 24 V, 4 digital inputs 24 V, 4 channels 24 V configurable as inputs or outputs, flexible digital controller logic
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement
X20CM8323	X20 PWM module, 8 digital outputs for switching electromechanical loads, 0.6 A continuous current, 2 A peak current, current monitoring, switching time detection
X20DM9324	X20 digital mixed module, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source 1-wire connections
X20DO2321	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, sink, 3-wire connections
X20DO2322	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, source, 3-wire connections
X20DO2623	X20 digital output module, 2 outputs, 100-240 VAC, 1 A, source, 240 V keyed, 3-wire connections
X20DO2633	X20 digital output module, 2 triac outputs, 12 to 240 VAC, 2 A, L switching, phase angle control, 240 V keyed
X20DO2649	X20 digital output module, 2 relays, changeover contacts, 240 VAC / 5 A, 24 VDC / 5 A
X20DO4321	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, sink, 3-wire connections
X20DO4322	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections
X20DO4331	X20 digital output module, 4 outputs, 24 VDC, 2 A, sink, 3-wire connections
X20DO4332	X20 digital output module, 4 outputs, 24 VDC, 2 A, source, 3-wire connections
X20DO4529	X20 digital output module, 4 relays, changeover contacts, 115 VAC / 0.5 A, 24 VDC / 1 A
X20DO4613	X20 digital output module, 4 triac coupler outputs, 12 to 240 VAC, 50 mA, zero-crossing detection, 240 V keyed,...
X20DO4623	X20 digital output module, 4 outputs, 100-240 VAC, 0.5 A, source, 240 V keyed, 2-wire connections
X20DO4633	X20 digital output module, 4 triac outputs, 12 to 240 VAC, 1 A, L switching, phase angle control, 240 V keyed
X20DO4649	X20 digital output module, 4 relays, N.O. contacts, 240 VAC / 5 A
X20DO6321	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections
X20DO6322	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections
X20DO6325	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, open line and overload detection, 2-wire connections
X20DO6529	X20 digital output module, 6 relays, normally open contacts, 115 VAC / 0.5 A, 30 VDC / 1 A
X20DO6639	X20 digital output module, 6 relays, normally open contacts, 240 VAC / 2 A, 30 VDC / 2 A
X20DO8232	X20 digital output module, 8 outputs, 12 VDC, 2 A, source, supply directly on module, 1-wire connections
X20DO8322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20DO8323	X20 digital output module, 8 outputs, 12 to 24 V, 0.5 A, sink/source, 1-wire connections, full bridge, half bridge, thermal overload protection
X20DO8331	X20 digital output module, 8 outputs, 24 VDC, 2 A, sink, supply directly on module, 1-wire connections
X20DO8332	X20 digital output module, 8 outputs, 24 VDC, 2 A, source, supply directly on module, 1-wire connections
X20DO9321	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections
X20DO9322	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20DOD322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 2-wire connections
X20DOF322	X20 digital output module, 16 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20DS1119	X20 multifunctional digital signal processor, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module
X20DS1319	X20 multifunctional digital signal processor, 4 digital input channels, 4 digital channels configurable as inputs or outputs, 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 2 reference pulses, SSI absolute encoder, NetTime module
X20RT8001	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, reACTION technology module
X20RT8201	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, 2 analog inputs ±10 V, 500 kHz sampling frequency, 13-bit converter resolution (including sign), configurable input filter, reACTION technology module

Digital signal processing and preparation

Order data	Short description
X20CM1201	X20 combination module, 1 AB incremental encoder, 24 V, 4 digital inputs 24 V, 4 channels 24 V configurable as inputs or outputs, flexible digital controller logic
X20DC1073	X20 digital counter module, 1x SinCos, 1 Vss, 400 kHz input frequency, encoder monitoring, NetTime module
X20DS1119	X20 multifunctional digital signal processor, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module
X20DS1319	X20 multifunctional digital signal processor, 4 digital input channels, 4 digital channels configurable as inputs or outputs, 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 2 reference pulses, SSI absolute encoder, NetTime module
X20DS1828	X20 digital signal module, 1 HIPERFACE interface, NetTime module
X20DS1928	X20 digital signal module, 1 EnDat 2.1/2.2 interface, NetTime module
X20DS4389	X20 digital signal module, 4 digital inputs, 24 VDC, 4 digital outputs, 24 VDC, 0.1 A, oversampling I/O functions, time-triggered I/O functions, NetTime module

Dummy modules

Order data	Short description
X20IF0000	X20 dummy interface module (non-functional)
X20ZF0000	Dummy X20 module (non-functional)
X20ZF000F	Dummy X20 module (non-functional)

Electronics module communication

Order data	Short description
X20CS1011	X20 interface module, 1 Moeller SmartWire interface
X20CS1012	X20 interface module, 1 M-Bus master interface, integrated slave supply
X20CS1013	X20 interface module, 1 DALI master interface
X20CS1020	X20 interface module, 1 RS232 interface, max. 115.2 kbit/s
X20CS1030	X20 interface module, 1 RS422/485 interface, max. 115.2 kbit/s
X20CS1070	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, object buffers in both send and receive directions
X20CS2770	X20 interface module, 2 CAN bus interfaces, max. 1 Mbit/s, object buffers in both send and receive directions

Expandable bus controllers

Order data	Short description
X20BC1083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, supports X20 interface module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20BC8083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, supports X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20BC8084	X20 bus controller, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20BC80G3	X20 bus controller, 1 EtherNet/IP interface, supports expansion with X20 EtherCAT junction modules, 2x RJ45, order bus base, power supply module and terminal block separately.

Hub system

Order data	Short description
X20ET8819	X20 Ethernet analysis tool, can be expanded with active hub modules, 2x RJ45
X20HB8815	X20 POWERLINK - TCP/IP gateway, can be expanded with active hub modules, 2x RJ45
X20HB8880	X20 base hub module, integrated 2-port hub, 2x RJ45
X20HB88G0	X20 EtherCAT junction (basic module), integrated 2-port EtherCAT junction, 2x RJ45

Interface module communication

Order data	Short description
X20IF1020	X20 interface module, 1 RS232 interface, max. 115.2 kbit/s, electrically isolated
X20IF1030	X20 interface module, 1 RS422/485 interface, max. 115.2 kbit/s, electrically isolated
X20IF1041-1	X20 interface module, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1043-1	X20 interface module, for DTM configuration, 1 CANopen slave interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1051-1	X20 interface module, for DTM configuration, 1 DeviceNet scanner (master) interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1053-1	X20 interface module, for DTM configuration, 1 DeviceNet adapter (slave) interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1061	X20 interface module, 1 PROFIBUS DP V0/V1 master interface, max. 12 Mbit/s, max. 3.5 kB input data and max. 3.5 kB output data, electrically isolated
X20IF1061-1	X20 interface module for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated
X20IF1063	X20 interface module, 1 PROFIBUS DP V0 slave interface, max. 12 Mbit/s, electrically isolated
X20IF1063-1	X20 interface module, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated
X20IF1065	X20 interface module, 1 PROFIBUS DP V1 slave interface, max. 12 Mbit/s, electrically isolated
X20IF1072	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately
X20IF1082	X20 interface module, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function
X20IF1082-2	X20 interface module, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function PRC function
X20IF1086-2	X20 interface module, 1 POWERLINK interface, managing or controlled node, PRC function, 1 fiber optic connection
X20IF1091	X20 interface module, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately
X20IF10A1-1	X20 interface module, for DTM configuration, 1 ASi master interface, electrically isolated, order 1x TB704 terminal block separately
X20IF10D1-1	X20 interface module, for DTM configuration, 1 EtherNet/IP scanner (master) interface, electrically isolated
X20IF10D3-1	X20 interface module, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated
X20IF10E1-1	X20 interface module for DTM configuration, 1 PROFINET RT controller (master) interface, electrically isolated
X20IF10E3-1	X20 interface module, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated
X20IF10G3-1	X20 interface module for DTM configuration, 1 EtherCAT slave interface, electrically isolated
X20IF10X0	X20 interface module, 1 redundancy link interface 1000BASE-SX, CPU-CPU data synchronization module for controller redundancy
X20IF2181-2	X20 interface module, 1x link selector for POWERLINK cable redundancy, POWERLINK functions: - Managing node - Controlled node for iCN operation - Redundant managing node for controller redundancy - Ring redundancy - 2x hub - Multi ASend - PRC function 2x RJ45
X20IF2772	X20 interface module, 2 CAN bus interfaces, max. 1 Mbit/s, electrically isolated, order 2x TB2105 terminal block separately
X20IF2792	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, 1 X2X Link master interface, electrically isolated, order 1x TB2105 and 1x TB704 terminal block separately

Motor controllers

Order data	Short description
X20MM2436	X20 PWM motor module, 24 to 39 VDC ±25%, 2 PWM motor bridges, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, configurable as incremental encoder
X20MM3332	X20 digital motor module, 24 VDC, 3 digital outputs, full bridge (H bridge), 3 A continuous current, 5 A peak current
X20MM4331	X20 digital motor module, 24 VDC, 4 digital outputs, half bridge, 3 A continuous current, 5 A peak current
X20MM4456	X20 PWM motor module, 24 to 48 VDC ±25%, 4 PWM motor bridges, 6 A continuous current, 10 A peak current, 4x 4 digital inputs 24 VDC, sink, configurable as incremental encoder
X20SM1426	X20 stepper motor module, 1 motor connection, 1 A continuous current, 1.2 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder
X20SM1436	X20 stepper motor module, module supply 24-39 VDC ±25%, 1 motor connection, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder

Other functions

Order data	Short description
X20CM0985	X20 digital and analog mixed module, multi-measurement transducer/ synchronization module, 5 digital outputs, 24 VDC, 0.5 A source, 1 relay, 1 A, changeover contact, 8 analog inputs, ±480 V / 120 V, 16-bit converter resolution, 3 analog inputs 5 A / 1 A AC, 16-bit converter resolution, order terminal blocks 0TB3102-7011, 0TB3104-7011, 0TB3102-7012, 0TB3104-7012 and 2x TB12 separately.
X20CM0985-1	X20 digital and analog mixed module, multi-measurement transducer/ synchronization module, 5 digital outputs, 24 VDC, 0.5 A, source, 1 relay 1 A, 8 analog inputs, ±480 V / 120 V, 16-bit converter resolution, 3 analog inputs 5 A / 1 A AC, 16-bit converter resolution, additional software functions, order terminal blocks 0TB3102-7011, 0TB3104-7011, 0TB3102-7012, 0TB3104-7012 and 2x X20TB12 separately
X20CM4810	X20 analog input module for vibration measurement and analysis for condition monitoring, 4 IEPE analog inputs, 51.5625 kHz sampling frequency, 24-bit converter resolution
X20CM6209	X20 diode array module, 1 A, 40 V reverse voltage, no module status data
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement
X20CM8323	X20 PWM module, 8 digital outputs for switching electromechanical loads, 0.6 A continuous current, 2 A peak current, current monitoring, switching time detection
X20DS4387	X20 digital signal module, 4x IO-Link master, 4 digital channels configurable as inputs or outputs, 3-wire connections
X20DS438A	X20 digital signal module, 4x I/O-Link master V1.1, can also be configured as 4x digital input or output channels, 3-wire connections
X20PD0011	X20 potential distributor module, 12x GND, integrated microfuse
X20PD0012	X20 potential distributor module, 12x 24 VDC, integrated microfuse
X20PD0016	X20 potential distributor module, 5x GND, 5x 24 VDC, each with 1x floating feed, integrated microfuse
X20PD2113	X20 potential distributor module, 6x GND, 6x 24 VDC, with feed option, integrated microfuse
X20PS4951	X20 power supply module, for potentiometers, 4x ±10 V for potentiometer supply

Power supplies

Order data	Short description
X20PS2100	X20 power supply module, for internal I/O supply
X20PS2110	X20 supply module, for internal I/O supply, integrated microfuse
X20PS3300	X20 power supply module, for X2X Link and internal I/O supply
X20PS3310	X20 power supply module, for X2X Link and internal I/O supply, integrated microfuse

reACTION Technology

Order data	Short description
X20RT8001	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, reACTION technology module
X20RT8201	X20 reACTION module, 4 digital inputs, 24 VDC, <1 µs, 4 digital channels, 24 VDC, 0.1 A, <1 µs, can be configured as input or output, 2 analog inputs ±10 V, 500 kHz sampling frequency, 13-bit converter resolution (including sign), configurable input filter, reACTION technology module

Redundancy systems

Order data	Short description
X20HB8884	X20 compact link selector, 2x RJ45, order bus base, power supply module and terminal block separately.

System modules for bus controllers

Order data	Short description
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated

System modules for compact CPUs

Order data	Short description
X20BB22	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB27	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20PS9500	X20 supply module for compact and fieldbus CPUs and internal I/O supply, X2X Link supply
X20PS9502	X20 supply module, for compact and fieldbus CPUs and internal I/O supply, X2X Link supply, supply not electrically isolated

System modules for expandable bus controllers

Order data	Short description
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20IF1041-1	X20 interface module, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1043-1	X20 interface module, for DTM configuration, 1 CANopen slave interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1051-1	X20 interface module, for DTM configuration, 1 DeviceNet scanner (master) interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1053-1	X20 interface module, for DTM configuration, 1 DeviceNet adapter (slave) interface, electrically isolated, order 1x TB2105 terminal block separately
X20IF1091-1	X20 interface module, for expandable bus controller, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately
X20IF10A1-1	X20 interface module, for DTM configuration, 1 ASi master interface, electrically isolated, order 1x TB704 terminal block separately
X20IF10D1-1	X20 interface module, for DTM configuration, 1 EtherNet/IP scanner (master) interface, electrically isolated
X20IF10D3-1	X20 interface module, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated
X20IF10E1-1	X20 interface module for DTM configuration, 1 PROFINET RT controller (master) interface, electrically isolated
X20IF10E3-1	X20 interface module, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated
X20IF10G3-1	X20 interface module for DTM configuration, 1 EtherCAT slave interface, electrically isolated
X20HB1881	X20 hub expansion module, integrated 1-port hub, for fiber optic cable
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated

System modules for fieldbus CPUs

Order data	Short description
X20BB32	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB37	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, Slot for X20 interface module, X20 connection, X20 locking plates X20AC0SL1/X20AC0SR1 (left and right) included
X20BB42	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB47	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20IF1074	X20 interface module, for SGC, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately
X20PS9500	X20 supply module for compact and fieldbus CPUs and internal I/O supply, X2X Link supply
X20PS9502	X20 supply module, for compact and fieldbus CPUs and internal I/O supply, X2X Link supply, supply not electrically isolated

System modules for X20 hub system

Order data	Short description
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20HB1881	X20 hub expansion module, integrated 1-port hub, for fiber optic cable
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable
X20HB28G0	X20 EtherCAT junction module, integrated 2-port EtherCAT junction, 2x RJ45
X20PS8002	X20 power supply module for standalone hub and compact link selector
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated

System modules for X20 redundancy systems

Order data	Short description
X20HB2885	X20 hub expansion module, integrated active 2-port hub, 2x RJ45
X20HB2886	X20 hub expansion module, integrated active 2-port hub, 2 fiber optic interfaces

Temperature measurement

Order data	Short description
X20AT2222	X20 temperature input module, 2 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections
X20AT2311	X20 temperature input module, 2 inputs for resistance measurement, PT100, resolution 0.001°C, 4-wire connections
X20AT2402	X20 temperature input module, 2 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C
X20AT4222	X20 temperature input module, 4 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections
X20AT6402	X20 temperature input module, 6 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C
X20ATA312	X20 temperature input module, 2 inputs for resistance measurement, PT100, resolution 0.01 °C, 4-wire connections
X20ATA492	X20 temperature input module, 2 thermocouple inputs, type J, K, N, S, B, R, E, C, T, single channel electrically isolated, 2x PT1000 integrated for terminal temperature compensation, with 1x X20TB1E terminal block, order terminal block separately
X20ATB312	X20 temperature input module, 4 inputs for resistance measurement, PT100, resolution 0.01 °C, 4-wire connections
X20ATC402	X20 temperature input module, 6 thermocouple inputs, type J, K, N, S, B, R, E, C, T, 2x PT1000 integrated for terminal temperature compensation, with 1x X20TB1E terminal block, order terminal block separately

Terminal blocks

Order data	Short description
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed
X20TB1E	X20 terminal block, 12-pin, 24 VDC keyed, 2x PT1000 integrated for terminal temperature compensation
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed

4.3 Analog input modules

Analog input modules convert measured values (voltages, currents) into numerical values, which can be processed by the PLC.

In the PLC, analog data is always in 16-bit 2s complement regardless of the resolution. Therefore, the resolution of the module used does not have to be taken into consideration when creating an application program.

Every channel on an analog input module has a status LED.

4.3.1 Brief information

Product ID	Short description	on page
X20AI1744	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 kHz input filter	132
X20AI1744-3	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 Hz input filter	132
X20AI2222	X20 analog input module, 2 inputs, ±10 V, 13-bit converter resolution, configurable input filter	148
X20AI2237	X20 analog input module, 2 inputs, ±10 V, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply	157
X20AI2322	X20 analog input module, 2 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter	174
X20AI2437	X20 analog input module, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply	183
X20AI2438	X20 analog input module, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply, supports HART protocol	199
X20AI2622	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	252
X20AI2632	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	263
X20AI2632-1	X20 analog input module, 2 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter	288
X20AI2636	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions	313
X20AI4222	X20 analog input module, 4 inputs, ±10 V, 13-bit converter resolution, configurable input filter	344
X20AI4322	X20 analog input module, 4 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter	353
X20AI4622	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	362
X20AI4632	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	373
X20AI4632-1	X20 analog input module, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	399
X20AI4636	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions	425
X20AI8221	X20 analog input module, 8 inputs, ±10 V, 13-bit converter resolution	456
X20AI8321	X20 analog input module, 8 inputs, 0 to 20 mA, 12-bit converter resolution	465
X20AIA744	X20 analog input module, 2 full-bridge strain gauge inputs, 24-bit converter resolution, 2.5 kHz input filter	474
X20AIB744	X20 analog input module, 4 full-bridge strain gauge inputs, 24-bit converter resolution, 2.5 kHz input filter	492
X20AP3111	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 20 mA AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	510
X20AP3121	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	510
X20AP3131	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 5 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	510
X20AP3161	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 333 mV AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	510
X20cAI2438	X20 analog input module, coated, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply, supports the HART protocol	199
X20cAI4622	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	362
X20cAI4632	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	373
X20cAI4632-1	X20 analog input module, coated, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	399
X20cAP3121	X20 energy metering module, coated, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	510

4.3.2 X20AI1744, X20AI1744-3

4.3.2.1 General Information

The X20AI1744 and X20AI1744-3 modules work with both 4-line and 6-line strain gauge cells. If a 6-line strain gauge cell is connected, the line compensation no longer functions. This module concept requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, suchas component tolerances, effective bridge voltage, or zero offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

The AI1744 analog input module is available in two versions:

Model number	Description
X20AI1744	The module is equipped with a 5kHz input filter for fast signal sequences. It therefore also allows high frequency signals and disturbances to pass through.
X20AI1744-3	This version is equipped with a slow 5Hz input filter. It is therefore suitable for slow signal sequences and provides good suppression of high frequency disturbance signals.

- 1 full-bridge strain gauge input
- Data output rate can be set from 2.5 Hz to 7.5 kHz
- Special operating modes (synchronous mode and multiple sampling)

4.3.2.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI1744	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 kHz input filter	
X20AI1744-3	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 Hz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 17: X20AI1744, X20AI1744-3 - Order data

4.3.2.3 Technical data

Product ID	X20AI1744	X20AI1744-3
Short description		
I/O module	1 full-bridge strain gauge input	
General information		
B&R ID code	0x1CDE	0xA4EF
Status indicators	Channel status, operating status, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Open line	Yes, using status LED and software	
Input	Yes, using status LED and software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.25 W	
Additional power dissipation caused by the actuators (resistive) [W]	Max. 0.36 W [1)]	
Electrical isolation		
Bus - Analog input	Yes	
Bus - Bridge supply voltage	Yes	
Channel - I/O supply	No	
Certification		
CE	Yes	
cULus	Yes	
KC	Yes	
GOST-R	Yes	
Full-bridge strain gauge		
Strain gauge factor	±2 to ±256 mV/V, configurable using software	

Table 18: X20AI1744, X20AI1744-3 - Technical data

Product ID	X20AI1744	X20AI1744-3
Connection	4- or 6-wire connections [2]	
Input type	Differential, used to evaluate a full-bridge strain gauge	
Digital converter resolution	24-bit	
Conversion time	Depends on the configured data output rate	
Data output rate	2.5 - 7500 samples per second, configurable using software (f_{DATA})	
Input filter		
Cutoff frequency	5 kHz	5 Hz
Orderliness	3	
Slope	60 dB	
ADC filter characteristics	Sigma-Delta, see section "Filter characteristics of the Sigma-Delta ADC"	
Operating range / Measurement sensor	85 to 5000 Ω	
Influence of cable length	The shielded, twisted pair cable should be as short as possible and run separately to the sensor (isolated from load circuit) without intermediate terminals	
Input protection	RC protection	
Input current	690 nA	
Common-mode range	0 to 3 VDC Permissible input voltage range (with regard to the potential strain gauge GND) on the inputs "Input +" and "Input -"	
Isolation voltage between input and bus	500 V_{eff}	
Conversion procedure	Sigma-Delta	
Output of the digital value		
Broken bridge supply line	Value approaches 0	
Broken sensor line	Value approaches ±end value (Status bit "open circuit" in register *Module status* is set)	
Valid value range	0x007FFFFF to 0xFF800001	
Strain gauge supply		
Voltage	5.5 VDC / max. 65 mA [3]	
Short circuit protection, overload protection	Yes	
Voltage drop for short circuit protection	Max. 0.2 VDC at 65 mA	
Quantization		
LSB value (16-bit)		
2 mV/V	336 nV	
4 mV/V	671 nV	
8 mV/V	1.343 µV	
16 mV/V	2.686 µV	
32 mV/V	5.371 µV	
64 mV/V	10.74 µV	
128 mV/V	21.48 µV	
256 mV/V	42.97 µV	
LSB value (24-bit)		
2 mV/V	1.31 nV	
4 mV/V	2.62 nV	
8 mV/V	5.25 nV	
16 mV/V	10.49 nV	
32 mV/V	20.98 nV	
64 mV/V	41.96 nV	
128 mV/V	83.92 nV	
256 mV/V	167.85 nV	
Temperature coefficient		
Rev. ≤D1	30 ppm/°C	
Rev. ≥E0	10 ppm/°C	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at altitudes above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Protection in accordance with EN 60529	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	0 to 55°C	
Vertical installation	0 to 50°C	
Derating	-	
Storage	-25 to 70°C	
Transport	-25 to 70°C	

Table 18: X20AI1744, X20AI1744-3 - Technical data

Product ID	X20AI1744	X20AI1744-3
Relative humidity		
Operation	5 to 95%, non-condensing	
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	
Spacing	12.5 $^{+0.2}$ mm	

Table 18: X20AI1744, X20AI1744-3 - Technical data

1) Depends on the full-bridge strain gauge used
2) With 6-wire connections, line compensation does not function. (See section "Connection examples")
3) The maximum current of 90 mA is permitted up to an operating temperature of 45°C.

4.3.2.4 Status LEDs

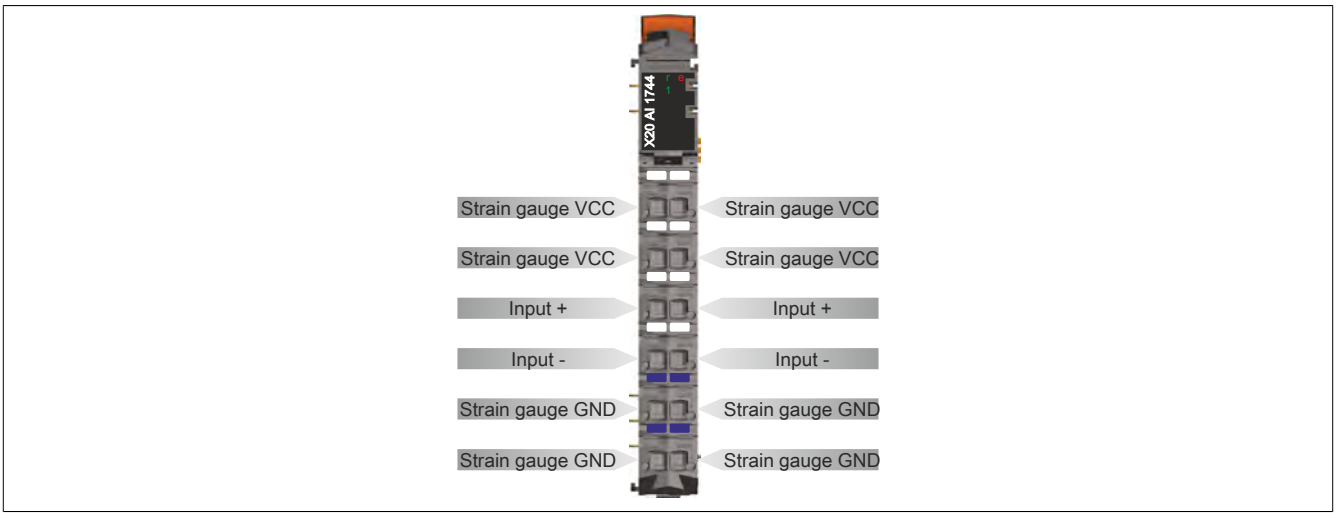
The status LEDs are identical on the X20AI1744 and X20AI1744- 3 modules.

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
	1	Green	Off	Possible causes: • Open line • Sensor is unplugged • Converter is busy
			On	Analog/digital converter running, value OK

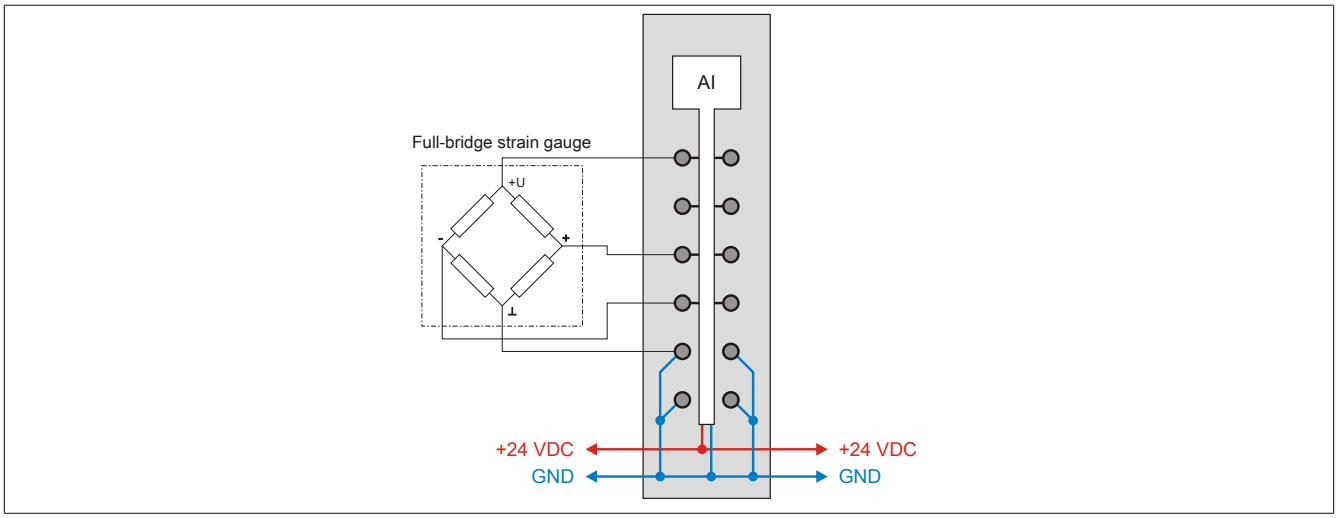
4.3.2.5 Pinout

The pinouts are identical on the X20AI1744 and X20AI1744- 3 modules.



4.3.2.6 Connection examples

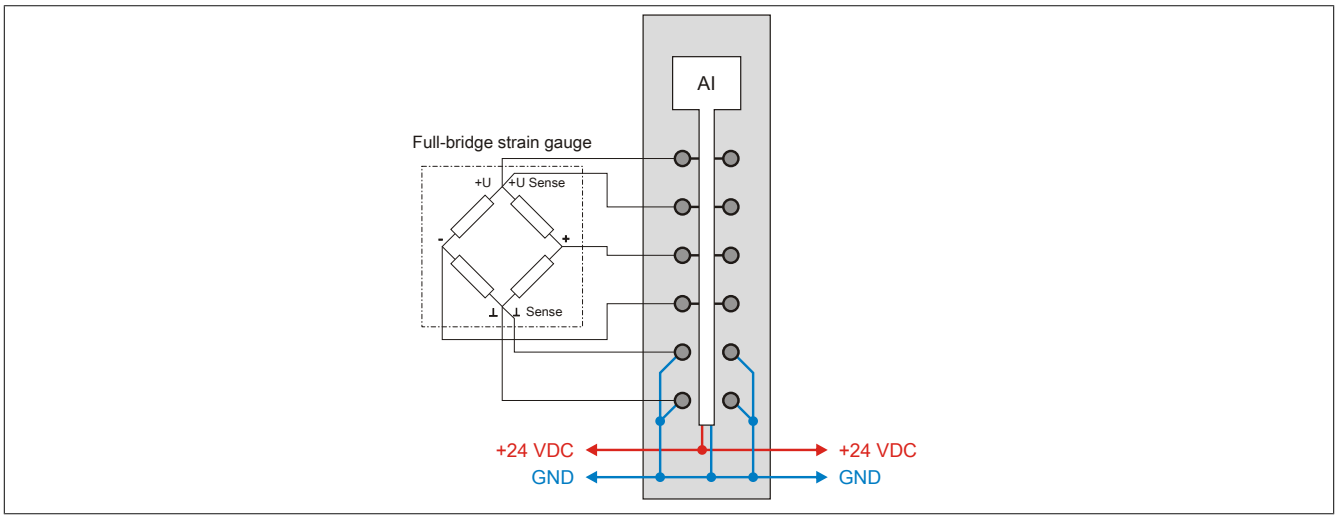
Full-bridge strain gauge with 4-line connection



Full-bridge strain gauge with 6-line connection

Precision can be improved by using strain gauge cells with feedback of the bridge voltage. The additional sensor lines with the strain gauge bridge supply compensate for the thermal resistance change of the feed lines. If a 6-line strain gauge cell is connected to the module, the sense lines are bypassed by the 4 internally linked strain gauge VCC connections (i.e. strain gauge GND). For this reason, the line compensation no longer functions. The measurement precision is therefore affected by changes in operating temperature. Longer cable lengths and smaller cable cross-sections also increase the potential for errors in the measurement system.

In order to reduce cable resistance, the sense lines should be connected in parallel with the strain gauge bridge supply lines. Optimal signal quality can be obtained by using a shielded twisted pair cable. The connections for the strain gauge supply lines, the sensor lines, and the bridge differential voltage lines should each use one twisted pair cable.



Parallel connection of 2 full-bridge strain gauges with 4-line connections

For parallel connection of full-bridge strain gauges, please refer to the manufacturer's guidelines.

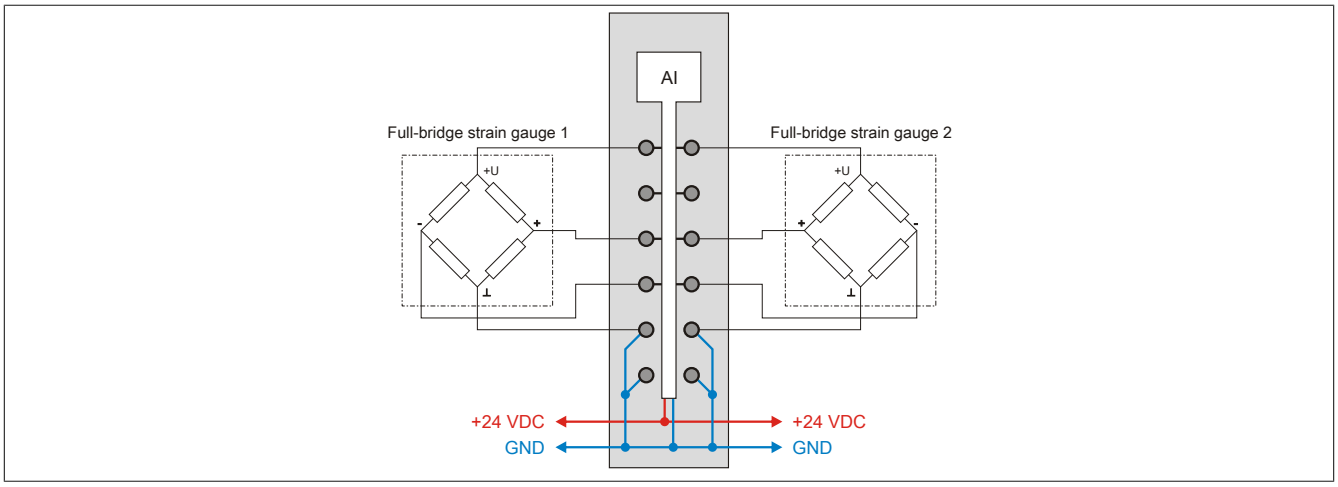
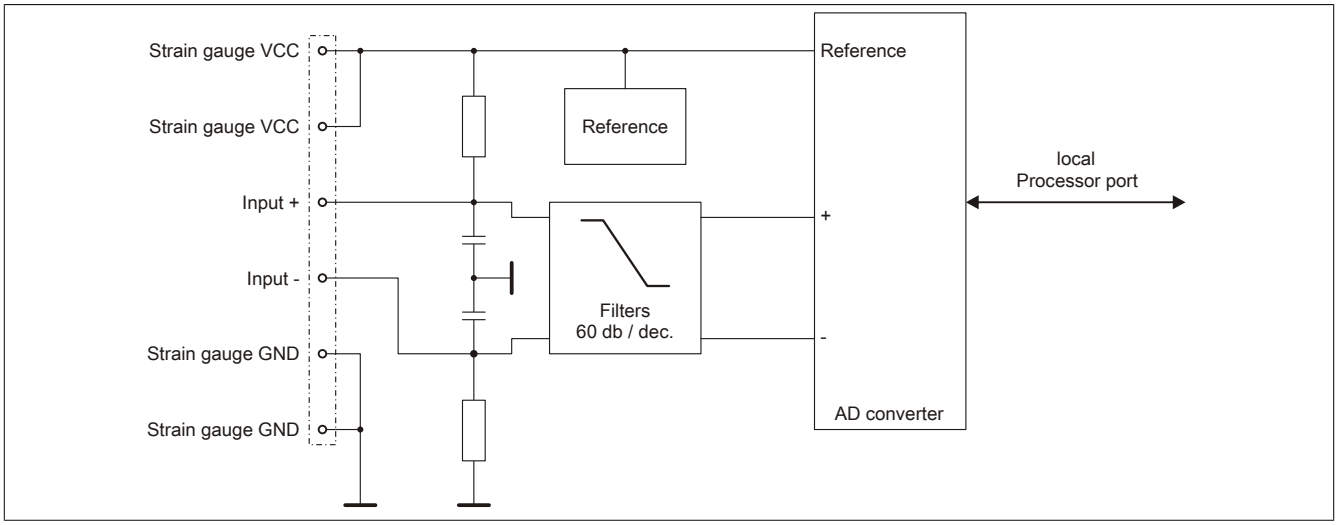


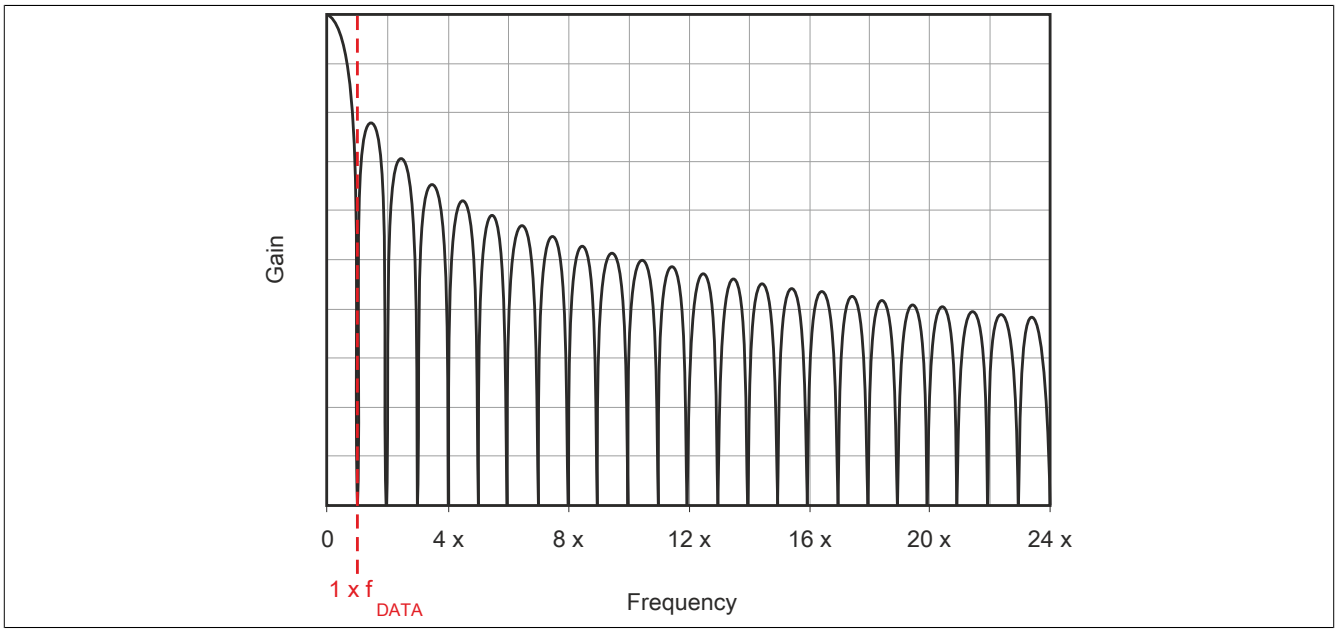
Figure 48: Connection example - Parallel connection of 2 full-bridge strain gauges

When connecting 3 or more full-bridge strain gauges in parallel, two lines must be connected together in an X20 terminal block.

4.3.2.7 Input circuit diagram



4.3.2.8 Filter characteristics of the Sigma-Delta ADC



4.3.2.9 Effective resolution of the AD converter

The AD converter on the AI1744 provides a 24 bit measurement value. However, the actual attainable noise-free resolution is always less than 24 bit. This "effective resolution" depends on the data rate and measurement range.

Example:

Because of the conversion method, a data rate of 2.5 Hz and a specified measurement area of 2 mV/V result in an effective resolution of 18.7 bits:

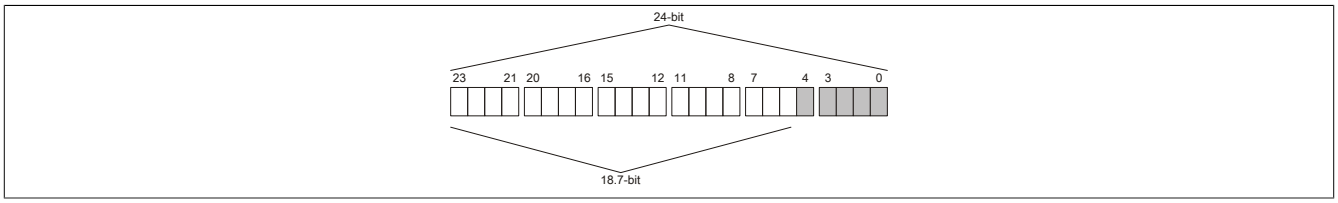


Figure 49: Example for the effective resolution of the AD converter

The low-order bits (grayed out) contain only noise instead of valid values and must therefore not be evaluated.

With the multiple sampling function model, only the highest 16 bits are made available.

4.3.2.10 Calculation example / Quantization

In a weighing application, the corresponding weight located on the connected load cell should be determined from the value derived from the X20AI1744.

The characteristics of the strain gauge load cell are as follows:

- Rated load: 1000 kg
- Bridge factor: 4 mV/V

The value for the positive full-scale deflection at a specified rated load of 1000kg is derived from the bridge factor of the strain gauge load cell (multiplication with the bridge supply voltage from the AI1744 module):

4 mV/V × 5.5 V = 22 mV

With a simple Rule of Three calculation, the corresponding value can be calculated (as seen in the table) from weight to the converter value and vice versa. This simplified theoretical approach is only valid for an ideal measurement system. Calibration of the entire measurement system is recommended because not only the X20AI1744 module, but particularly the strain gauge bridges feature tolerances (offset, gain). When taring, the gradient offset is recalculated and the gain of the linear equation is determined when standardized. In addition to the calculation displayed in the table, these calculations must also be carried out in the application.

24 bit value from the X20AI1744		Quantization	Corresponding weight
0x007F FFFF	8,388,607	22.0 mV	1000 kg
0x0000 0001	1	2.62 nV	0.119 g
0x0000 20C3	8,387	22.0 µV	1 kg
0x0001 0000	65,536	171.9 µV	7.81 kg

Table 19: X20AI1744 - Calculation example / Quantization

The values for each LSB can be found in the technical data of the X20AI1744, under "Quantization" (1 LSB in reference to 16 bit and 1 LSB in reference to 24 bit).

4.3.2.11 Register description

4.3.2.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.2.11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
16	ConfigOutput01	USINT				•
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01[1)]	USINT				•

1) **X20AI744**: from firmware version 8 / upgrade 1.3.0.0; **X20AI744-3**: from firmware version 8 / upgrade 1.2.0.0

4.3.2.11.3 Function model 1 - Multiple sampling

In this function model, the AD converter is operated in synchronization with X2X Link using a fixed ADC cycle time (configurable as 50 or 100 µs).

The module returns between 3 and 10 measured values per X2X cycle depending on the configuration. With an X2X cycle time of 400 µs and ADC cycle time of 50 µs, exactly 8 measurements are performed and the module can return 8 values (strain gauge value 01 to strain gauge value 08).

If a longer cycle time is used, the values returned correspond to the last measurements. If using an X2X cycle time that is not a whole number multiple of the ADC cycle time, then the conversion cannot be synchronized with X2X Link. In this case, the module outputs the invalid value 0x8000.

Example 1

With an X2X cycle time of 800 µs, 16 measurements are performed per X2X cycle. The first 6 measured values are discarded; the last 10 measured values are provided by the module.

With a shorter X2X cycle time, the number of measured values should not exceed the number of measurements that can actually be made. All other measured values are invalid (0x8000). To minimize the load on X2X Link, it is possible to disable unneeded registers (see "Number of measurement values").

Example 2

If using an X2X cycle time of 300 µs, it is possible to perform 6 measurements per X2X cycle if the ADC cycle time equals 50 µs. For this reason, only the first 6 registers are valid. The registers for the 7th through 10th measured value (AnalogInput07 to AnalogInput08) should be disabled by setting "Number of measured values" to "6 measured values" in the I/O configuration.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2	StatusInput01	USINT	•			
1534 + N * 4	AnalogInput0N (N = 1 to 10)	INT	•			
1600	ConfigOutput01 (X20AI1744) ConfigGain01_MultiSample (X20AI1744-3)	USINT				•
1603	ConfigCycletime01_MultiSample	USINT				•

4.3.2.11.4 Function model 254 - Bus Controller

In the bus controller function model, the module behaves as it does in the standard function model, with the exception that it is not synchronized to the X2X Link even if Synchronous mode is activated in the ADC configuration register. Instead, the module behaves as if the set ADC cycle time is not a factor or multiple of the X2X cycle time and attempts to maintain the set ADC cycle time as precisely as possible.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
16	ConfigOutput01	USINT				•
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01[1)]	USINT				•

1) **X20AI744**: from firmware version 8 / upgrade 1.3.0.0; **X20AI744-3**: from firmware version 8 / upgrade 1.2.0.0

4.3.2.11.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.2.11.5 Register for "Standard" and "Bus Controller" function model

4.3.2.11.5.1 Module status

Name:
StatusInput01

The current state of the module is indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	AD converter values	0	ADC value is valid
		1	ADC value is invalid
1	Line monitoring	0	OK
		1	Open line
2	Only valid in synchronous mode	0	ADC runs synchronous to the X2X Link
		1	ADC does not run synchronous to the X2X Link
3 - 7	Reserved	-	

4.3.2.11.5.2 Strain gauge value

Name:
AnalogInput01

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Data type	Values	Information
DINT	0x007FFFFF to 0xFF800001	Valid value range
	0x007FFFFF	Overrun
	0xFF800001	Underflow
	0xFF800000	Invalid value

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and the measurement range (see "Effective resolution of the AD converter").

The following table shows how the effective resolution (in bits), or the effective value range of the strain gauge value depend on the module configuration (data rate, measurement area).

	Measurement range							
	±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	21.3	±1,290,000	20.8	±912,000	19.7	±425,000	18.7	±212,000
5	20.7	±851,000	20.3	±645,000	19.3	±322,000	18.3	±161,000
10	20.4	±691,000	19.9	±490,000	18.9	±244,000	17.9	±122,000
15	20.1	±562,000	19.3	±320,000	18.7	±212,000	17.7	±106,000
25	19.7	±425,000	19.2	±301,000	18.5	±185,000	17.5	±92,000
30	19.6	±397,000	19.0	±262,000	18.1	±140,000	17.1	±72,000
50	19.4	±346,000	18.8	±230,000	17.9	±122,000	16.9	±61,000
60	19.3	±320,000	18.8	±230,000	17.8	±114,000	16.8	±57,000
100	19.1	±280,000	18.5	±185,000	17.4	±86,000	16.4	±43,000
500	18.0	±130,000	17.3	±80,000	16.3	±40,000	15.3	±20,000
1000	17.2	±75,000	16.5	±46,000	15.6	±25,000	14.6	±12,000
2000	16.6	±49,600	16.1	±35,000	15.3	±20,000	14.3	±10,000
3750	16.2	±37,600	15.7	±26,600	14.7	±13,000	13.7	±6,600
7500	15.8	±28,500	15.3	±20,200	14.4	±10,800	13.4	±5,400

Table 20: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

	Measurement range							
	±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	23	±4,194,000	22.6	±3,179,000	22.1	±2,248,000	21.7	±1,703,000
5	22.3	±2,582,000	22.4	±2,767,000	21.9	±1,957,000	21.3	±1,291,000
10	22.3	±2,582,000	22	±2,097,000	21.6	±1,589,000	21	±1,049,000
15	22	±2,097,000	21.7	±1,703,000	21.3	±1,291,000	20.7	±852,000
25	21.7	±1,703,000	21.4	±1,384,000	21.1	±1,124,000	20.5	±741,000
30	21.8	±1,826,000	21.3	±1,291,000	20.8	±913,000	20.4	±692,000
50	21.3	±1,291,000	21.1	±1,124,000	20.4	±692,000	19.9	±489,000
60	21.3	±1,291,000	20.9	±978,000	20.5	±741,000	19.8	±456,000
100	20.9	±978,000	20.7	±852,000	20.2	±602,000	19.6	±397,000
500	20.1	±562,000	19.6	±397,000	19.1	±281,000	18.6	±199,000
1000	19	±262,000	18.6	±199,000	18.1	±140,000	17.5	±93,000
2000	18.5	±185,000	18.1	±140,000	17.8	±114,000	17	±66,000
3750	18.1	±140,000	17.8	±114,000	17.3	±81,000	16.6	±50,000
7500	17.7	±106,000	17.3	±81,000	16.9	±61,000	16.2	±38,000

Table 21: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

4.3.2.11.5.3 ADC configuration

Name:
ConfigOutput01

The sampling rate and measurement range for the AD converter can be configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500
		1110	Synchronous mode[1)]
		1111	Reserved
4 - 5	Standard measurement range (bit 6 = 0)	00	16 mV/V
		01	8 mV/V
		10	4 mV/V
		11	2 mV/V
	Extended measurement range (bit 6 = 1)[2)]	00	256 mV/V
		01	128 mV/V
		10	64 mV/V
		11	32 mV/V
6		0	Standard measurement range (2 to 16 mV/V)
		1	Extended measurement range (32 to 256 mV/V)[2)]
7	Reserved	0	(must be 0)

1) ADC is operated synchronously with the X2X Link, if possible; beginning with firmware 2
2) Starting with Firmware Version 4

Synchronous mode

Beginning with firmware version 2, the analog/digital converter (ADC) on the X20AI1744 module can be operated and read synchronously with the X2X Link. Synchronous mode is activated by selecting the respective operating mode in the *ADC configuration* register. A time between 200 and 2,000 µs must also be set in the *ADC cycle time* register. If this time is a whole number factor or multiple of the configured cycle time of the X2X Link, then the ADC is synchronously read with the X2X Link.

Information:

The ADC cycle time must be ≥1/4 of the X2X cycle time.

The bit 2 in *Module Status* is set (i.e. ADC does not run synchronously), ...

- ... if the configured ADC cycle time cannot be synchronized with the X2X Link.
- ... if the module is still in the settling phase.

Jitter, dead time and settling time:

Jitter	
ADC cycle times <1500 µs	Max. ±1 µs
ADC cycle times >1500 µs	Max. ±4 µs
Dead time on the X2X Link	$50\ \mu s + \frac{\text{X2X cycle time}}{128}$
Settling time	
Firmware Version ≤	Max. 150 x ADC cycle time
Firmware Version ≥5	150 x X2X cycle time

Table 22: Jitter, dead time and settling time

The settling time corresponds to the time needed until the AD converter can be operated after activating the synchronous mode or following conversion of the ADC cycle time.

4.3.2.11.5.4 ADC cycle time

Name:
ConfigCycletime01

This register is only used in "Synchronous mode". If synchronous mode is enabled in the ADC configuration, then the module attempts to operate the ADC synchronously to the X2X Link (based on the ADC cycle time specified in this register). It is necessary for the X2X Link cycle time and the ADC cycle time to have a certain relationship. The following conditions must be adhered to:

1 ADC cycle time ≥ 1/4 X2X cycle time
2 ADC cycle time corresponds to a whole number factor or multiple of the X2X cycle time
3 ADC cycle time must be in the range from 50 to 2000 µs

Data type	Value
UINT	50 to 2000

4.3.2.11.5.5 ADC clock frequency shift

Name:
AdcClkFreqShift01

In rare cases, X20AI1744 connected to neighboring slots can influence one another. This can result in temporary, minimal deviations in measurement values. This can only occur if the SigmaDelta ADCs on the neighboring X20AI1744 modules are operated at exactly the same clock frequency.

In most cases, these clock frequencies vary slightly due to part variances. When they are the same however, this register on the X20AI1744 provides a safe way for an application to prevent this type of mutual influence.

Data type	Value
SINT	-128 to 127

This register can be used to vary the clock frequency in increments of 200 ppm. Setting values from -50 to 50 cover a range of -10000 ppm to 10000 ppm. This corresponds with -1% to 1%.

Values beyond this range will cause activation of a default mode. The frequency shift is derived from the from the last 2 digits of the serial number by the X20AI1744 firmware. This saves time that would otherwise be needed for programming, provided that the last two digits of the serial numbers on the neighboring modules are not the same

Register value	Frequency shift in ppm	Example of a sampling rate[1)]
127	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
50	10000	505
49	9800	504.9
...	...	...
2	400	500.2
1	200	500.1
0	0	500
-1	-200	499.9
-2	-400	499.8
...	...	...
-50	-10000	495
-51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
-128	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number

Table 23: Frequency shift of the ADC clock

1) Nominal sampling rate of 500 samples per second

IMPORTANT:

As shown in the table above, shifting the ADC clock frequency will equally shift the ADC sampling rate. Shifting the ADC clock frequency too much can cause problems with disturbance suppression particularly when a very specific sampling rate has been defined to suppress existing disturbances (e.g: 50 Hz to suppress the 50 Hz hum). Also see "Filter characteristics of the Sigma-Delta ADC".
It's situations like this where the option to manually shift the frequency in the I/O configuration or ASIOACC library should be utilized rather than relying on the default frequency shift that is based on the serial number.

A frequency shift like the one shown below would be sufficient to prevent modules from influencing one another and would not cause any noticeable difference to the filter characteristics.

Slot	1	2	3	4	5	6	...
ADC clock frequency shift	0	2	-1	1	-2	0	...

Information:

- **This register has no effect in synchronous mode because the firmware regulates the ADC clock frequency in such a way that the ADC conversion cycle is synchronous with the X2X cycle.**
- **When writing to this register using the ASIOACC library, only the lowest value byte of the written value is accepted. For example, the value 256 (=0x100) is identical to the value 0 (=0x00).**

4.3.2.11.6 Register for "Multiple Sampling" function model

4.3.2.11.6.1 Module status

Name:
StatusInput01

The current state of the module is indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	AD converter values	0	ADC value is valid
		1	ADC value is invalid
1	Line monitoring	0	OK
		1	Open line An open line was found during at least one measurement in this X2X cycle. This bit is reset if all measurements are OK after correcting this error, i.e. it does not have to be acknowledged.
2	Synchronous mode	0	ADC runs synchronous to the X2X Link
		1	ADC does not run synchronous to the X2X Link
3 - 7	Reserved	-	

4.3.2.11.6.2 Strain gauge value - Multiple

Name:
AnalogInput01 to AnalogInput10

This register contains the raw value determined by the ADC for the full-bridge strain gauge with 16-bit resolution. The module returns between 3 and 10 measured values per X2X cycle depending on the configuration.

Effective resolution

In principle, the effective resolution of the AD converter is dependent on the data rate and the measurement range (see "Effective resolution of the AD converter").

The following table shows how the effective resolution (in bits), or the effective value range of the strain gauge value depend on the module configuration (data rate, measurement area).

Measurement range							
±16mV/V		±8mV/V		±4mV/V		±2mV/V	
Bits	Scope	Bits	Scope	Bits	Scope	Bits	Scope
15.4	22,000	14.6	12,000	13.8	7,000	12.8	4,000

Table 24: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

Measurement range							
±256mV/V		±128mV/V		±64mV/V		±32mV/V	
Bits	Scope	Bits	Scope	Bits	Scope	Bits	Scope
17.1	70,000	16.7	53,000	16.4	43,000	15.9	31,000

Table 25: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

4.3.2.11.6.3 ADC configuration

Name:
ConfigOutput01 (X20AI1744)
ConfigGain01_MultiSample (X20AI1744-3)

The measurement range for the AD converter can be configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Standard measurement range (bit 2 = 0)	00	16 mV/V
		01	8 mV/V
		10	4 mV/V
		11	2 mV/V
	Extended measurement range (bit 2 = 1)[1)]	00	256 mV/V
		01	128 mV/V
		10	64 mV/V
		11	32 mV/V
2		0	Standard measurement range (2 to 16 mV/V)
		1	Extended measurement range (32 to 256 mV/V)[1)]
3 - 7	Reserved	0	(must be 0)

1) Starting with Firmware Version 4. In the standard measurement range (2 to 16 mV/V), open-circuit detection works reliably at all adjustable data rates. In the extended measurement range (32 to 256 mV/V), open-circuit detection does not work reliably (because of the variable input impedance of the amplifier in relation to the set data rate).

4.3.2.11.6.4 ADC cycle time

Name:
ConfigCycletime1_MultiSample

This register can be used to configured the ADC cycle time.

In order for multisampling to work, the X2X cycle time must be divisible by the ADC cycle time (i.e. results in a whole number).

Data type	Value	Information
USINT	0	50 µs (default)
	1	100 µs
	2 - 255	Reserved

4.3.2.11.6.5 Number of measurement values

If the X2X cycle time is too short, then bot all 10 measurements can be performed. To reduce the load on X2X Link, it makes sense to only transfer as many values as measurements that can be made. This is why it is possible to configure the number of measured values to be transferred (see "Function model 1 - Multiple sampling").

Example: ADC cycle time 50 µs

X2X cycle time	Number of measurement values to be transferred
250 µs	5
300 µs	6
350 µs	7
400 µs	8
450 µs	9
≥500 µs	10

Example: ADC cycle time 100 µs

X2X cycle time	Number of measured values to be transferred
300 µs	3
400 µs	4
500 µs	5
600 µs	6
700 µs	7
800 µs	8
900 µs	9
≥1 ms	10

4.3.2.11.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

4.3.2.11.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

There is no limitation and no simple dependency on the bus cycle time. In the "Standard" function model, the I/O update time is defined by the register 4.3.2.11.5.3 "ADC configuration" and 4.3.2.11.5.4 "ADC cycle time".
In the "Multiple Sampling" function model, the update time is 50 µs.

4.3.3 X20AI2222

4.3.3.1 General information

The module is equipped with 2 inputs with 13-bit (including sign) digital converter resolution. It can be used to capture voltage signals in the range from ±10 V.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs ±10 V
- 13-bit digital converter resolution

4.3.3.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2222	X20 analog input module, 2 inputs, ±10 V, 13-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 26: X20AI2222 - Order data

4.3.3.3 Technical data

Product ID	X20AI2222
Short description	
I/O module	2 analog inputs ±10 V
General information	
B&R ID code	0xCAB0
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.8 W [1]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	±10 V
Input type	Differential input
Digital converter resolution	±12-bit
Conversion time	300 µs for all inputs
Output format	
Data type	INT
Voltage	0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Input impedance in signal range	20 MΩ
Input protection	Protection against wiring with supply voltage
Permitted input signal	Max. ±30 V
Output of the digital value during overload	Configurable

Table 27: X20AI2222 - Technical data

Product ID	X20AI2222
Conversion procedure	SAR
Input filter	3rd-order low pass / cut-off frequency 1 kHz
Max. error at 25°C	
Gain	0.08% 3)
Offset	0.015% 4)
Max. gain drift	0.006 %/°C 3)
Max. offset drift	0.002 %/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.025% 4)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 +0.2 mm

Table 27: X20AI2222 - Technical data

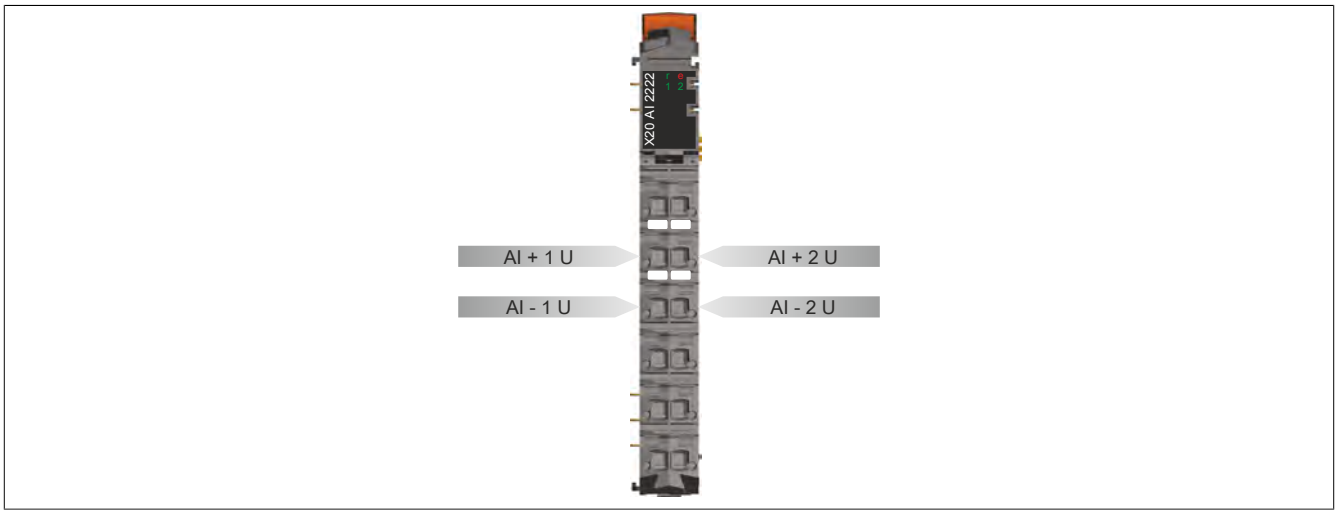
1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 20 V measurement range.

4.3.3.4 LED status indicators

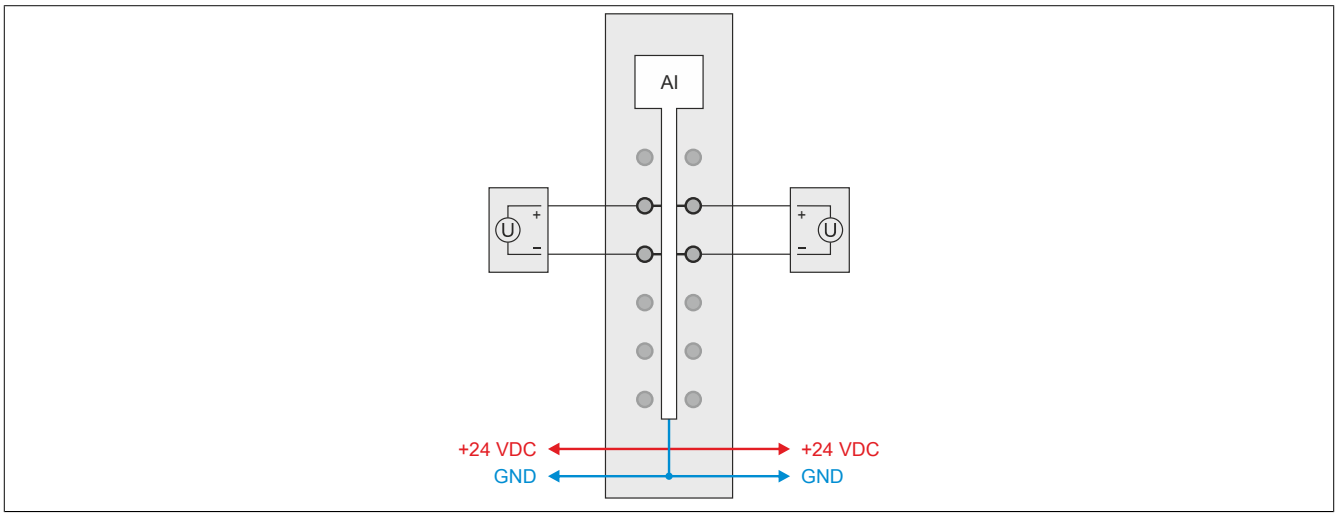
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	Open line or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

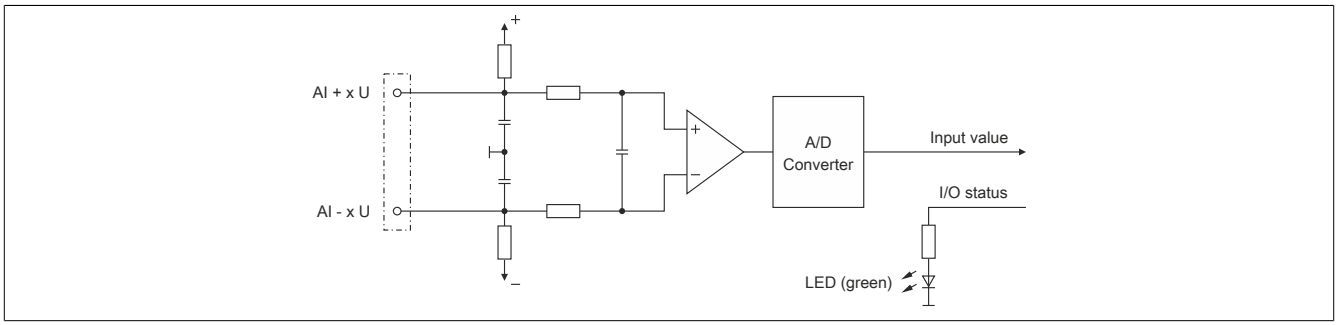
4.3.3.5 Pinout



4.3.3.6 Connection example



4.3.3.7 Input circuit diagram



4.3.3.8 Register description

4.3.3.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.3.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	Configuring the input filter	USINT				•
20	Lower limit value	INT				•
22	Upper limit value	INT				•
Analog signal - Communication						
0	AnalogInput01	INT	•			
2	AnalogInput02	INT	•			
30	Input status	USINT	•			

4.3.3.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	Configuring the input filter	USINT				•
20	-	Lower limit value	INT				•
22	-	Upper limit value	INT				•
Analog signal - Communication							
0	0	AnalogInput01	INT	•			
2	2	AnalogInput02	INT	•			
30	-	Input status	USINT		•		

1) The offset specifies the position of the register within the CAN object.

4.3.3.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.3.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

4.3.3.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput02

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC

4.3.3.8.6 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the scan rate for the channels is measured in ms. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

4.3.3.8.6.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

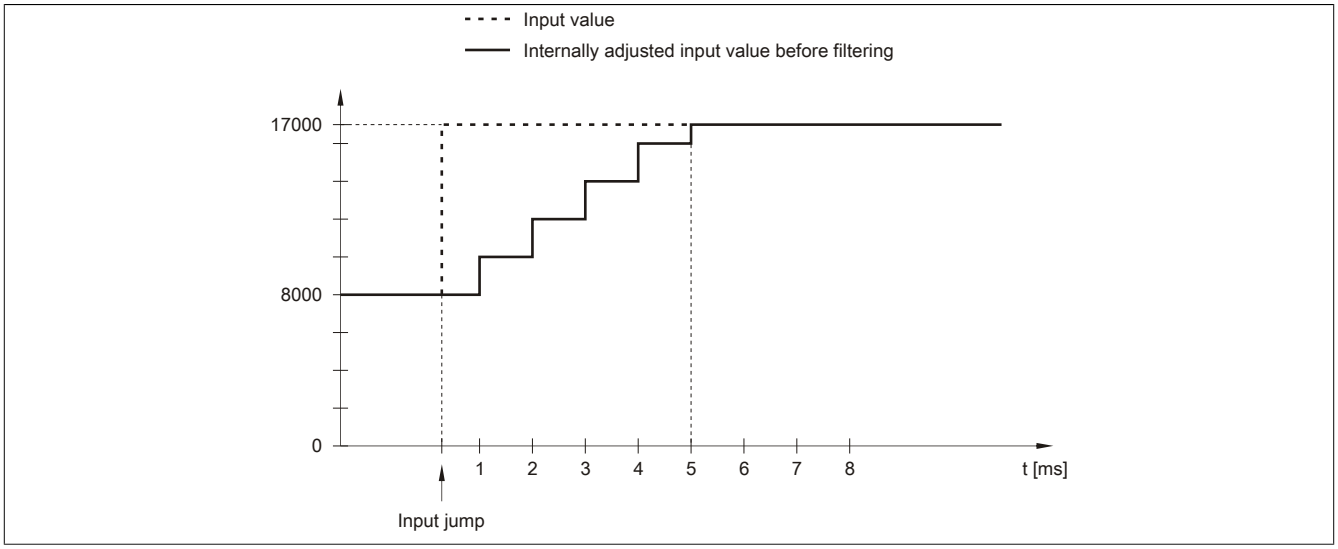


Figure 50: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

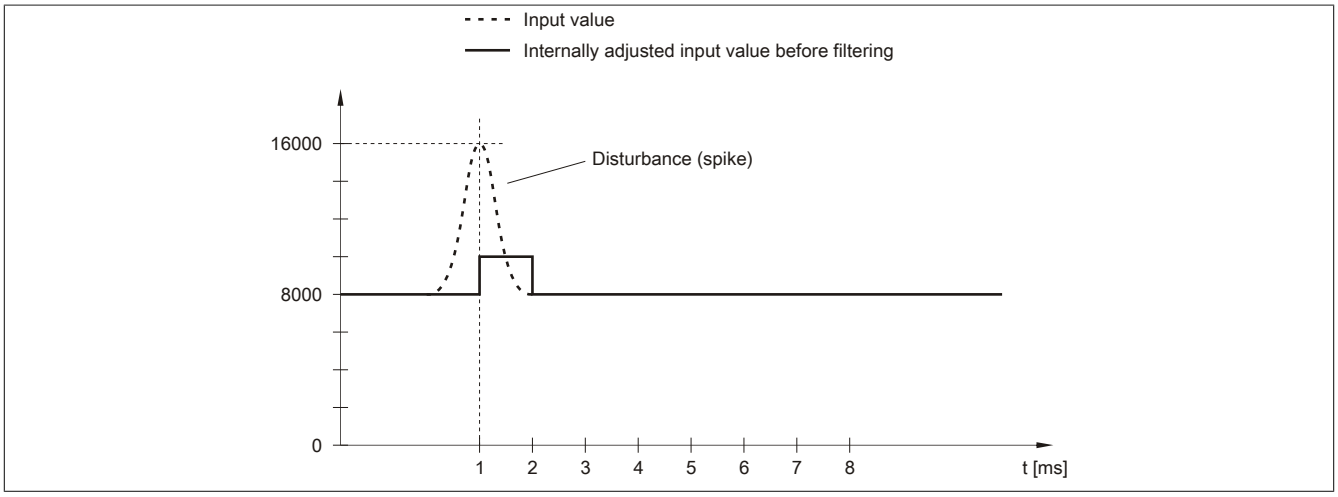


Figure 51: Adjusted input value for disturbance

4.3.3.8.6.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

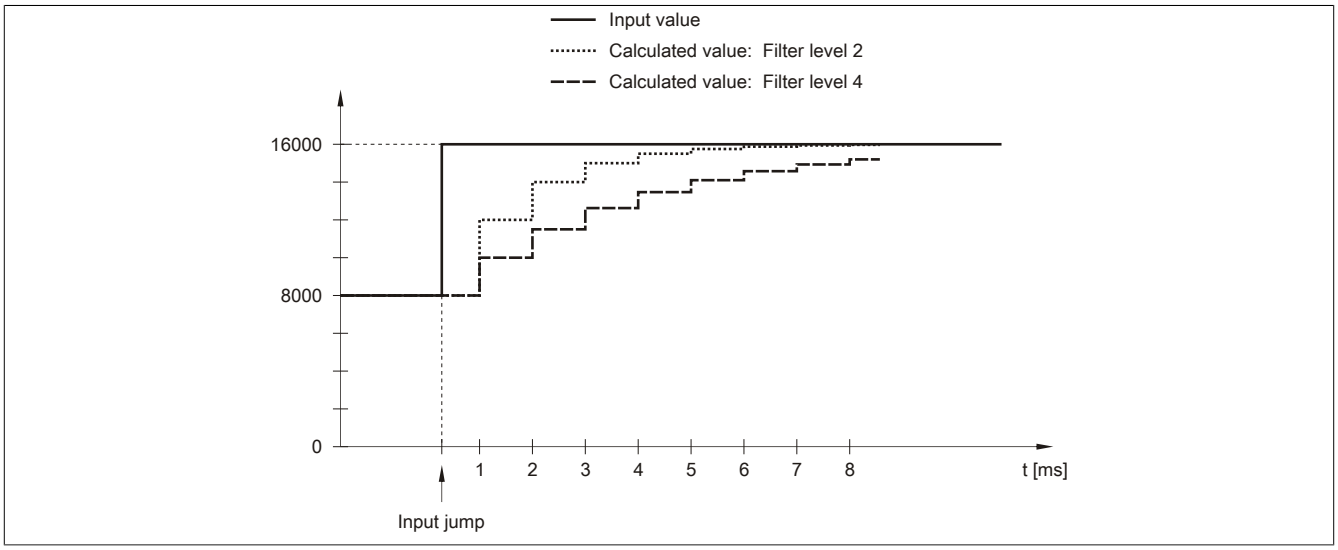


Figure 52: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

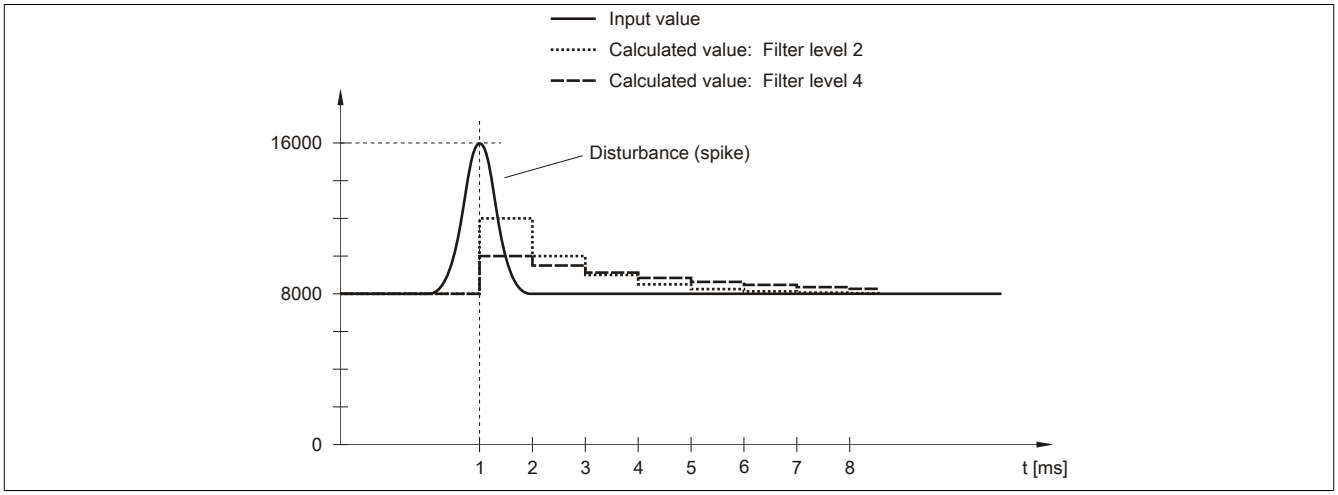


Figure 53: Calculated value during disturbance

4.3.3.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

4.3.3.8.8 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of -32768 corresponds to the minimum default value of -10 VDC.

Keep in mind that this setting applies to all channels!

4.3.3.8.9 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of 32767 corresponds to the maximum default value at +10 VDC.

Keep in mind that this setting applies to all channels!

4.3.3.8.10 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

4.3.3.8.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Inputs without filtering	100 µs
Inputs with filtering	500 µs

4.3.3.8.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Inputs without filtering	300 µs for all inputs
Inputs with filtering	1 ms

4.3.4 X20AI2237

4.3.4.1 General information

The module is equipped with 2 voltage measurement inputs with 16-bit digital converter resolution.

Each voltage input has its own sensor supply. The two channels with their respective sensor supplies are electrically isolated from each other.

- 2 analog voltage inputs
- Electrically isolated analog channels
- Electrically isolated sensor supplies
- 16-bit digital converter resolution
- Very high sampling rate

4.3.4.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2237	X20 analog input module, 2 inputs, ±10 V, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 28: X20AI2237 - Order data

4.3.4.3 Technical data

Product ID	X20AI2237
Short description	
I/O module	2 analog inputs ±10 V
General information	
B&R ID code	0xC9C4
Status indicators	I/O function per channel, operating state, module status, sensor supply per channel
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Sensor supply	Yes, using status LED and software
Power consumption	
Bus	0.05 W
Internal I/O	1.15 W [1]
External I/O	1.5 W [2]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [3]	Yes
GOST-R	Yes
Analog inputs	
Input	±10 V
Input type	Differential input
Digital converter resolution	±15-bit
Data output rate	10,000 samples per second
Output format	
Data type	INT
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Input impedance in signal range	20 MΩ

Table 29: X20AI2237 - Technical data

Product ID	X20AI2237
Input protection	Up to 30 VDC, reverse polarity protection
Open line detection	Yes, using software
Permitted input signal	Max. ±30 V
Output of the digital value during overload	Configurable
Conversion procedure	SAR
Input filter	4th-order low pass / cutoff frequency 10 kHz
Max. error at 25°C	
Gain	0.013% [4]
Offset	0.0035% [5]
Max. gain drift	<0.0008 %/°C [4]
Max. offset drift	<0.0025 %/°C [5]
Common-mode rejection	
DC	84 dB
Up to 60 Hz	84 dB
Up to 10 kHz	82 dB
Common-mode range	±14 V
Nonlinearity	<0.003% [5]
Test voltage between	
Channel and channel	1000 VAC
Channel and bus	1000 VAC
Channel and ground	1000 VAC
Bus and ground	800 VAC
Sensor supply	
Nominal voltage	25 V ±2%
Nominal output current	Max. 30 mA
Short circuit protection	Yes, continuous
Electrical isolation	
Sensor supply - Channel	No
Sensor supply - Sensor supply	Yes
Max. voltage ripple	
Up to 100 kHz	≤2.2 mV
Up to 1 MHz	≤22 mV
Higher	≤100 mV
Short circuit current	
Typical	<50 mA
Maximum	60 mA
Behavior in the event of short circuit	Current limitation
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 29: X20AI2237 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs.
2) Sensor supply
3) Ta min.: 0°C
   Ta max.: See environmental conditions
4) Based on the current measured value.
5) Based on the 20 V measurement range.

4.3.4.4 LED status indicators

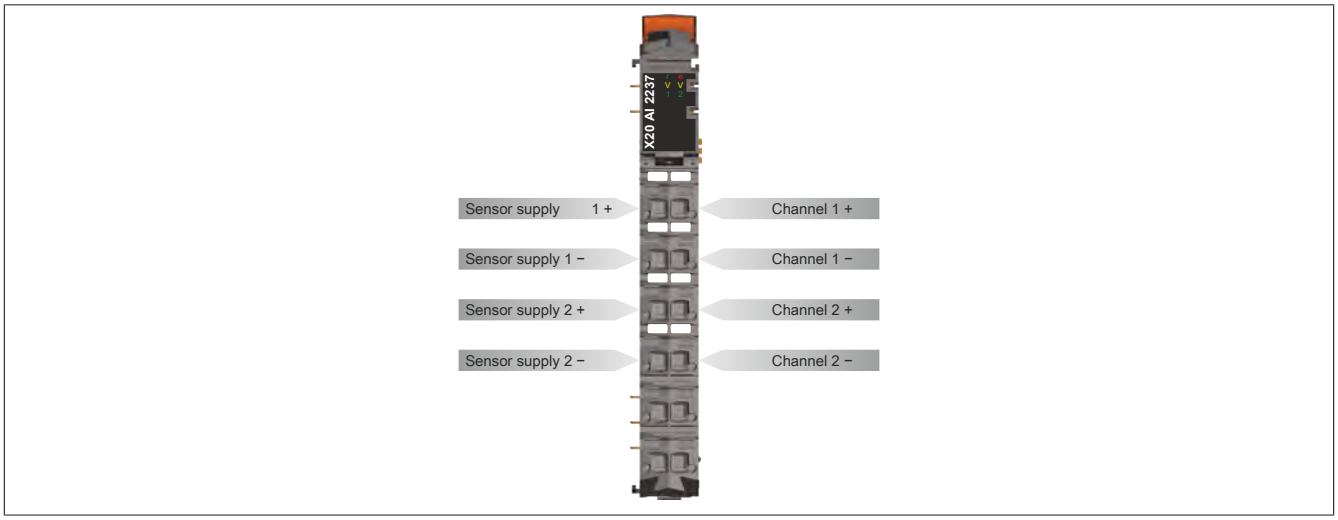
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	**Operating state**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
	Module status			
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	Sensor supply			
	V	Yellow	Off	Module supply not connected or overload
			On	Sensor supply in its normal operating range
	Analog input			
	1 - 2	Green	Off	Indicates one of the following cases: • No power to module • Channel disabled • Open line
			Single flash	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

4.3.4.5 Pinout

Shielded twisted pair cables should be used to minimize coupling disturbances. Use either one cable for each channel or a multiple twisted pair cable for both channels.

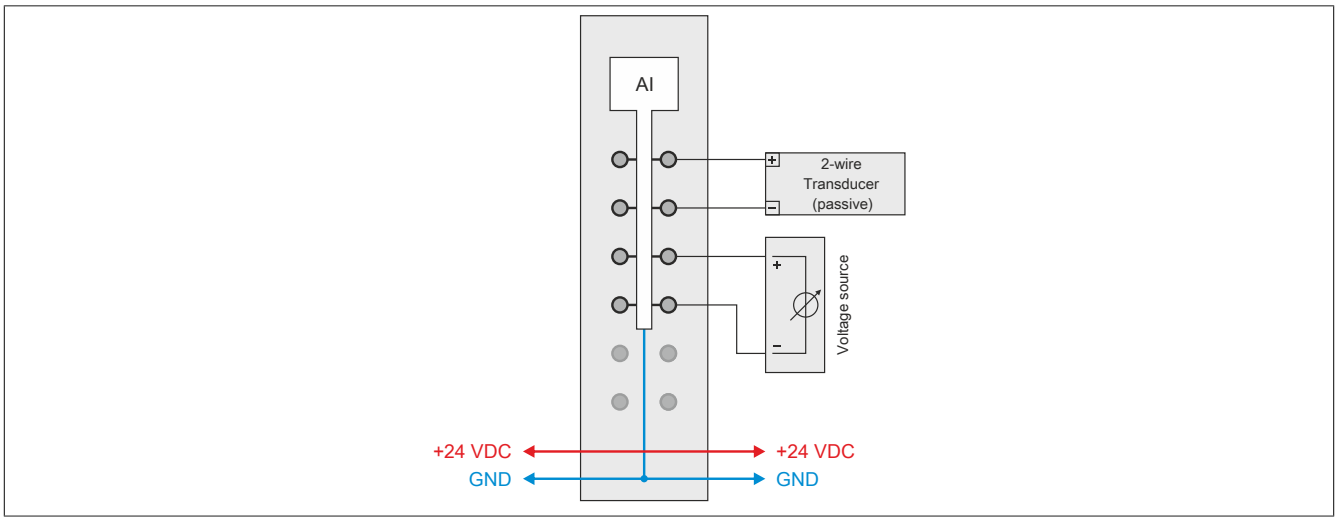


4.3.4.6 Connection examples

2-wire connections

A 2-wire connection can be implemented as follows:

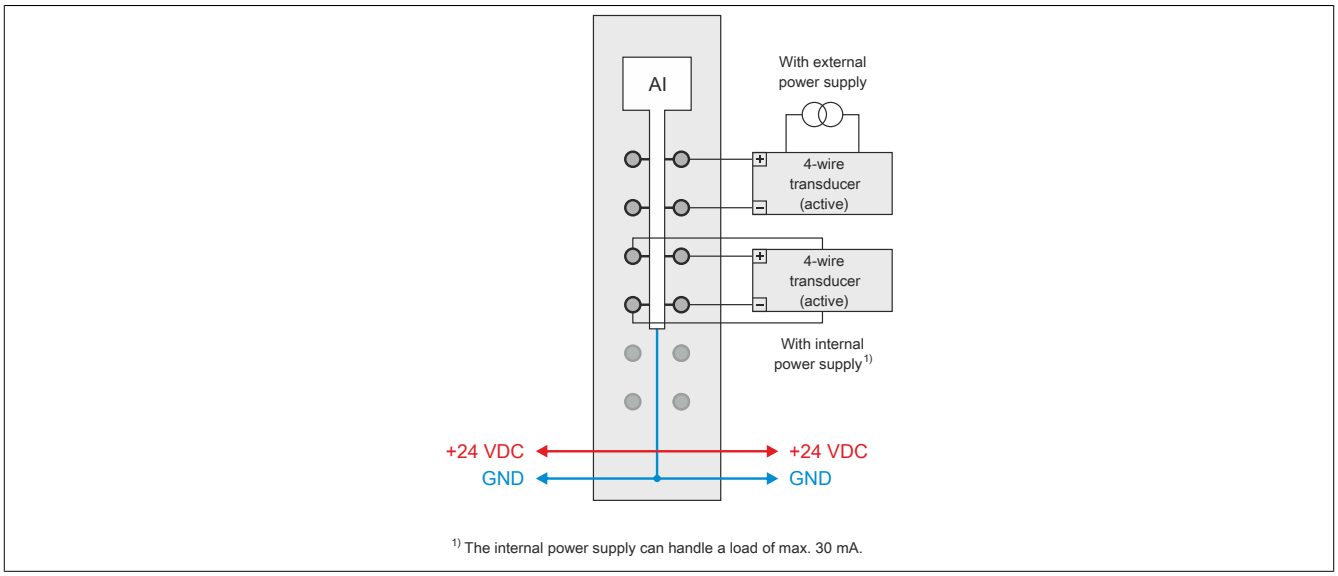
- 2-wire transducer
- Active voltage source



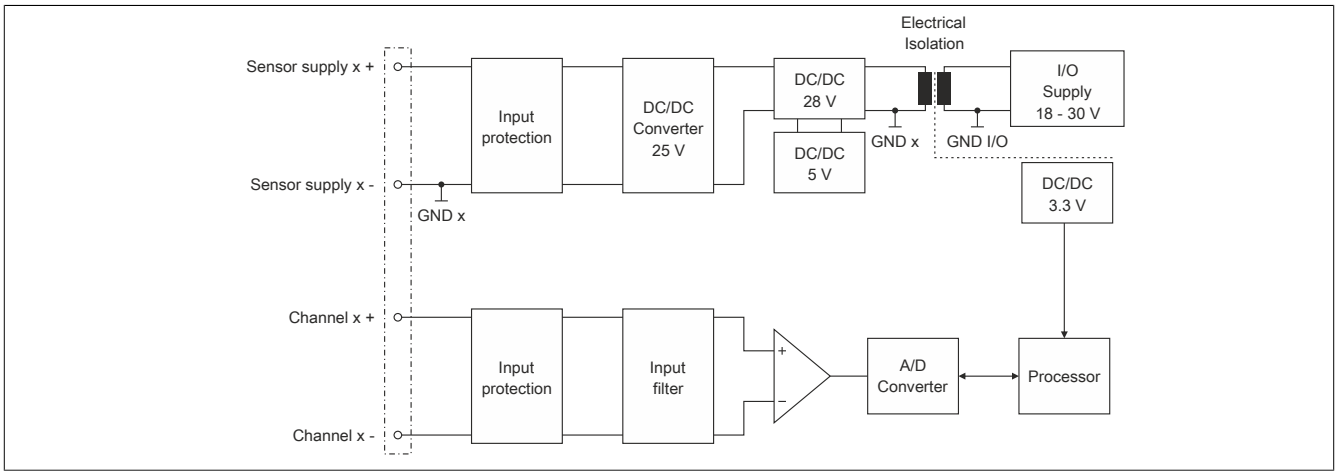
4-wire connections

A 4-wire connection can be implemented as follows:

- 4-wire transducer with external supply
- 4-wire transducer supplied by the module

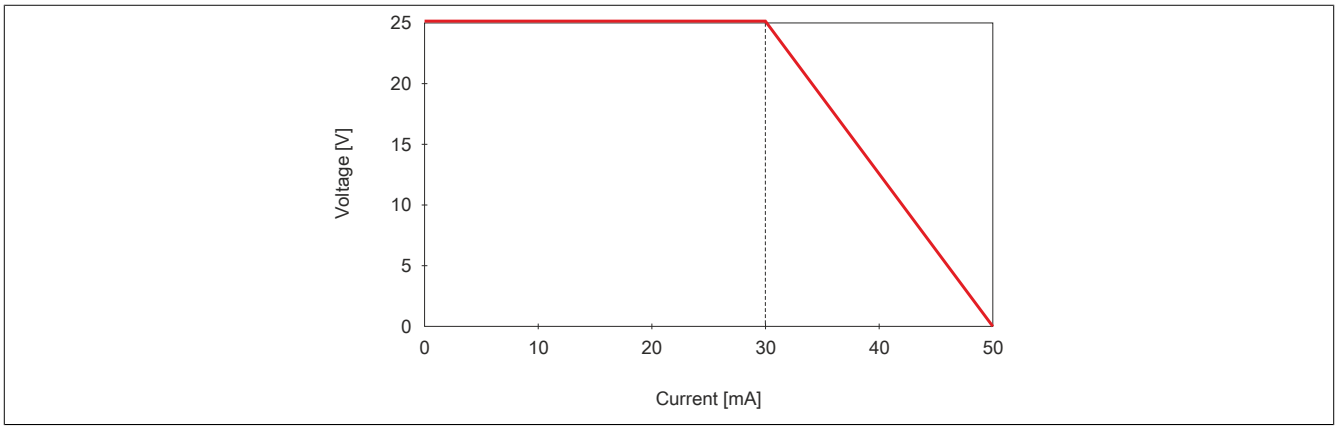


4.3.4.7 Input circuit diagram



4.3.4.8 Behavior in the event of short circuit

In the event of a short circuit, the output current for the sensor supply is limited according to the following diagram.



4.3.4.9 Register description

4.3.4.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.4.9.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog input - Configuration						
390 434	AnalogFilter01 AnalogFilter02	UINT				•
386 430	AnalogMode01 AnalogMode02	UINT				•
402 446	UpperLimit01 UpperLimit02	INT				•
398 442	LowerLimit01 LowerLimit02	INT				•
406 450	Hysteres01 Hysteres02	INT				•
414 458	ReplacementUpper01 ReplacementUpper02	INT				•
410 454	ReplacementLower01 ReplacementLower02	INT				•
426 470	PreparationInterval01 PreparationInterval02	UINT				•
418 462	ErrorDelay01 ErrorDelay02	UINT				•
422 466	SumErrorDelay01 SumErrorDelay02	UINT				•
Analog input - Communication						
0 2	AnalogInput01 (limited) AnalogInput02 (limited)	INT	•			
258 262	AnalogInput01 (original value) AnalogInput02 (original value)	INT	•			
284 292	AnalogSampletime01 (32-bit) AnalogSampletime02 (32-bit)	DINT	•			
282 290	AnalogSampletime01 (16-bit) AnalogSampletime02 (16-bit)	INT	•			
273 275	AnalogStatus01 AnalogStatus02	USINT	•			
	UnderflowAnalogInput01 or 02	Bit 0				
	OverflowAnalogInput01 or 02	Bit 1				
	OpenLineAnalogInput01 or 02	Bit 2				
	SumErrorAnalogInput01 or 02	Bit 4				
	SensorErrorAnalogInput01 or 02	Bit 6				
	IoSuppErrorAnalogInput01 or 02	Bit 7				

4.3.4.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog input - Configuration							
390 434	- -	AnalogFilter01 AnalogFilter02	UINT				•
386 430	- -	AnalogMode01 AnalogMode02	UINT				•
402 446	- -	UpperLimit01 UpperLimit02	INT				•
398 442	- -	LowerLimit01 LowerLimit02	INT				•
406 450	- -	Hysteres01 Hysteres02	INT				•
414 458	- -	ReplacementUpper01 ReplacementUpper02	INT				•
410 454	- -	ReplacementLower01 ReplacementLower02	INT				•
426 470	- -	PreparationInterval01 PreparationInterval02	UINT				•
418 462	- -	ErrorDelay01 ErrorDelay02	UINT				•
422 466	- -	SumErrorDelay01 SumErrorDelay02	UINT				•
Analog input - Communication							
0 2	0 2	AnalogInput01 AnalogInput02	INT	•			
273 275	- -	AnalogStatus01 AnalogStatus02	USINT		•		
		UnderflowAnalogInput01 or 02	Bit 0				
		OverflowAnalogInput01 or 02	Bit 1				
		OpenLineAnalogInput01 or 02	Bit 2				
		SumErrorAnalogInput01 or 02	Bit 4				
		SensorErrorAnalogInput01 or 02	Bit 6				
		IoSuppErrorAnalogInput01 or 02	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.3.4.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.4.9.4 General information

The module provides 2 electrically isolated channels. Each channel can read an electrical voltage signal in the ±10 V range and supply the signal encoder with 24 VDC.

4.3.4.9.5 Analog input - Configuration

Each channel is configured and enabled separately. First, the user must set the scaling of the input value and select a replacement value strategy. Depending on the requirements of the application, the user can also set user-defined limit values and define an input filter.

Scaling

The module's A/D converter works with a resolution of 16 bits (±15 bits). This allows the input value of ±10 V to be mapped using ±32767 steps. To simplify implementation, the user can configure scaling to ±10000 steps. The conversion value corresponds to the voltage in mV, and with a resolution of more than 14 bits (±13 bits) is still precise enough for the many different application that use this technology.

Replacement value strategy

The detected voltage is evaluated in order to ensure the quality of the read value. For example, if a logically impermissible voltage value or an open line is detected, the limit monitor triggers an appropriate response.

The response is determined by the replacement value strategy selected by the user. With the option "Replace with static value", the user defines two values that replace the converted value when the upper and lower limits are exceeded. The alternative "Retain last valid value" keeps the last validated value. However, the evaluation for this option takes more time. Depending on the "preparation interval", the value currently being read may be delayed.

Limit Value Monitoring

In addition to the qualitative evaluation of the input, the module also provides the option of adapting the range of permitted values to the requirements of the application. The registers 4.3.4.9.5.3 "UpperLimit" and 4.3.4.9.5.4 "LowerLimit" can be used to place additional restrictions on the permitted upper and lower limit. When this feature is used, the selected replacement value strategy is implemented according to the new limits.

4.3.4.9.5.1 Input filter

Analog input signals can experience brief disturbances caused by external factors (EMC). The ADC's high sampling rate allows you to filter out these types of signal peaks without hindering the application processes.

2 configuration points are available for interpolating the input signal:

- 4.3.3.8.6.1 "Input ramp limitation"
- 4.3.3.8.6.2 "Filter level"

Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

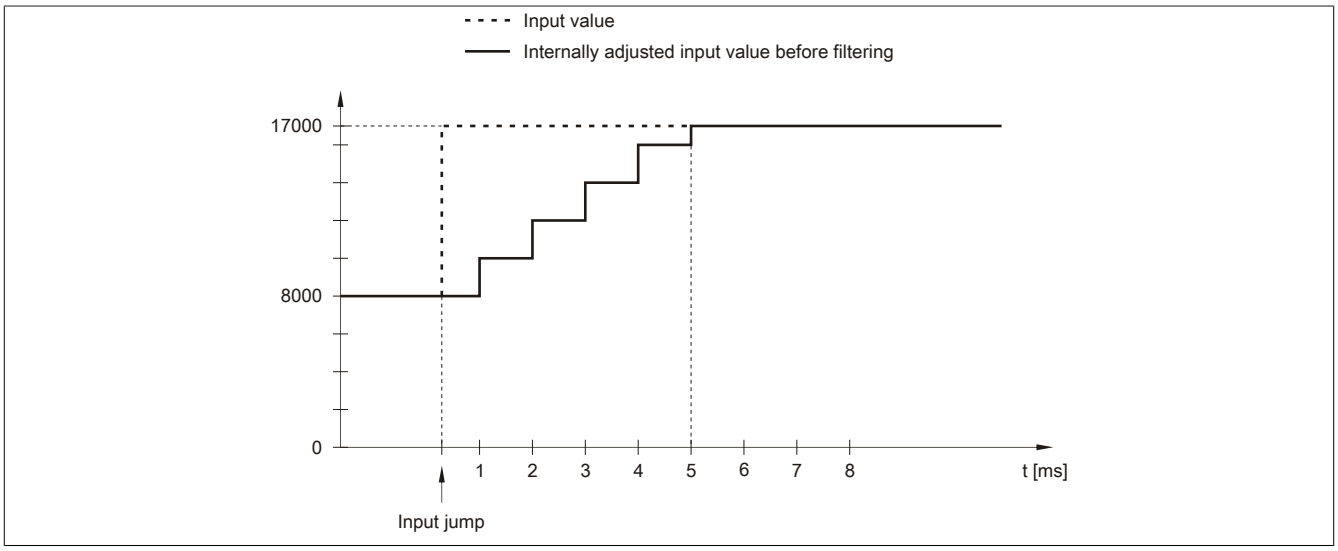


Figure 54: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

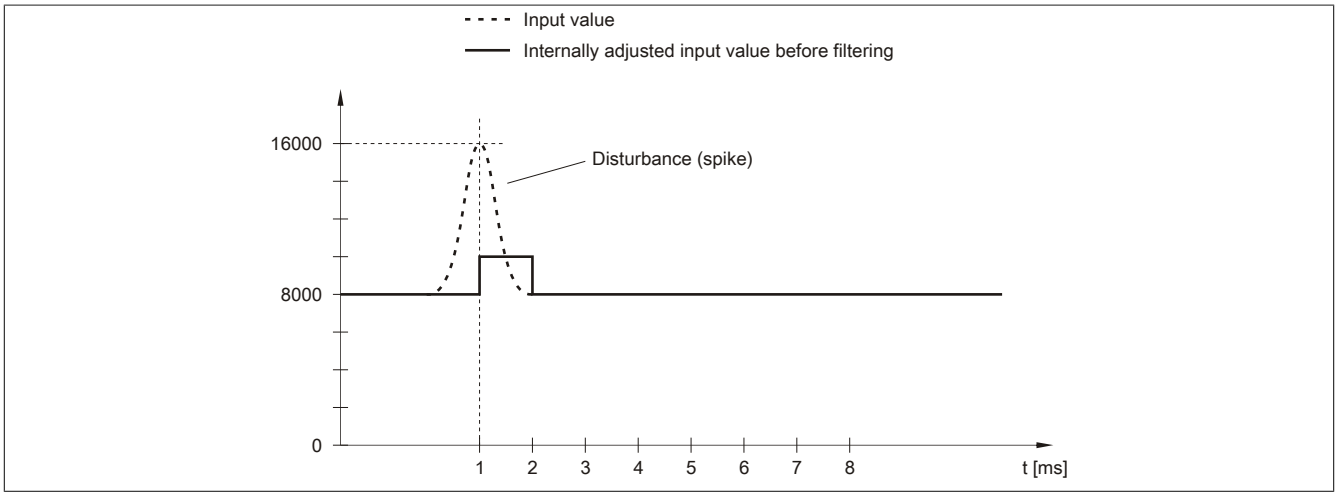


Figure 55: Adjusted input value for disturbance

Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

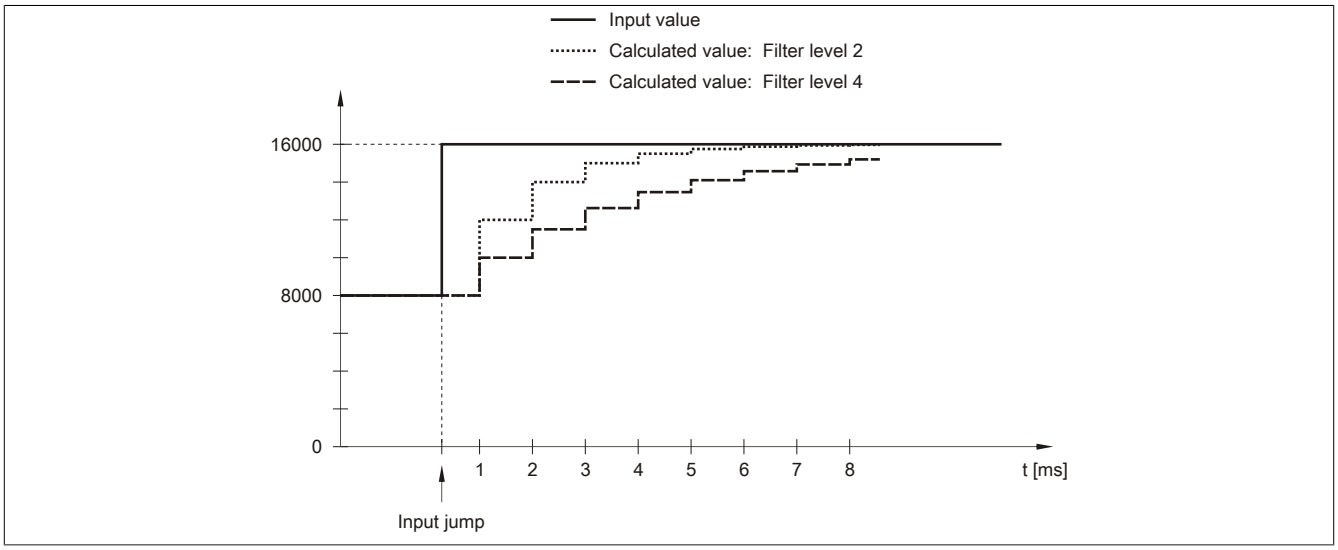


Figure 56: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

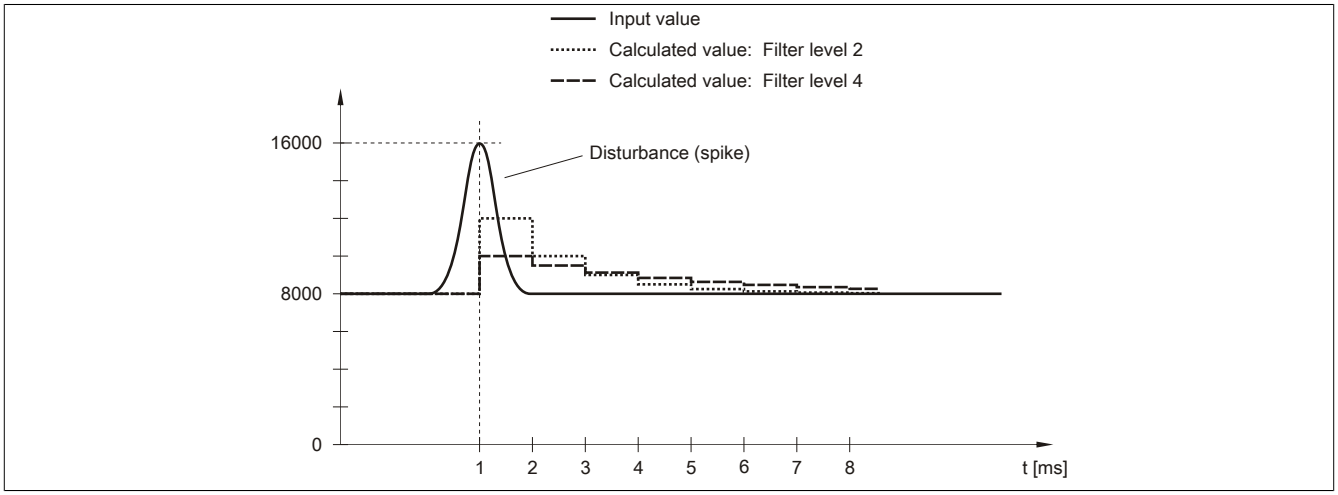


Figure 57: Calculated value during disturbance

Configuring filters

Name:
AnalogFilter01 to AnalogFilter02

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

4.3.4.9.5.2 Channel parameters

Name:
AnalogMode01 to AnalogMode02

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be enabled individually and can be configured and operated independently.

Information:

Different limit values must be configured for any display normalizing that needs to take place.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel (on/off)	0	Disabled
		1	Enabled
1	Limit exceeded	0	Disabled
		1	Enabled
2	Lower limit violation	0	Disabled
		1	Enabled
3	Reserved	0	
4	Replacement value strategy	0	Replace with static value
		1	Retain last valid value
5	Measured value scaling	0	±32767 (resolution: 16-bit)
		1	±10000 (resolution: >14-bit)
6 - 15	Reserved	0	

4.3.4.9.5.3 Upper limit value

Name:
UpperLimit01 to UpperLimit02

If the value range needs to be restricted further, this register can be used to enter new user-specific upper limit values.

Data type	Value
INT	-32767 to 32767
	-10000 to 10000

Information:

The defined limit values must take the configured scaling into consideration.

4.3.4.9.5.4 Lower limit value

Name:
LowerLimit01 to LowerLimit02

If the value range needs to be restricted further, this register can be used to enter new user-specific lower limit values.

Data type	Value
INT	-32767 to 32767
	-10000 to 10000

Information:

The defined limit values must take the configured scaling into consideration.

4.3.4.9.5.5 Hysteresis

Name:
Hysteres01 to Hysteres02

If the user-specific limit values are being used, then a hysteresis range should also be defined. These registers configure how far a limit value can be exceeded before a response is triggered.
The error status is cleared when the scaled input value once again passes the limit by at least the hysteresis value in the permitted direction.

Data type	Value
INT	-32767 to 32767
	-10000 to 10000

Information:

The hysteresis value must take the scaling into consideration.

4.3.4.9.5.6 Upper replacement value

Name:
ReplacementUpper01 to ReplacementUpper02

This register is used to define the static values to be displayed instead of the current measured value when the limit is violated.

Data type	Value
INT	-32767 to 32767

4.3.4.9.5.7 Lower replacement value

Name:
ReplacementLower01 to ReplacementLower02

This register is used to define the lower static values to be displayed instead of the current measured value when the limit is violated.

Data type	Value
INT	-32767 to 32767

4.3.4.9.5.8 Preparation time for the measured values

Name:
PreparationInterval01 to PreparationInterval02

If the last valid measured value should be kept when violating the limit value, then PreparationInterval must be defined. The measured values continue to be acquired and converted according to the configured I/O update time. They are then checked and discarded if they do not meet the specifications. When an error does not occur, therefore, the measured value acquired 2 preparation intervals ago is constantly output.

Data type	Value	Information
UINT	0 to 65535	in 0.1 ms

Functionality:
Measured values are continuously converted and stored to measured value memory depending on the configured input filter. The current contents of the measured value memory are checked within the configured interval. If a permissible value is present, then the contents of the buffer memory are passed to output memory and the contents of the measured value memory are passed to the buffer.
If the check turns up an impermissible value, then the contents of the measured value memory are discarded. The copy direction between output and buffer memory reverses and the last valid value continues to be output.

Information:

If configured to keep the last valid value, the delay time from measuring to outputting the value will be at least twice the preparation interval. In the worst case scenario, this can also take twice the interval time plus the configured conversion rate of the A/D converter.

"Application" Value being measured (analog)	
↓	Condition: - Conversion interval (A/D converter) elapsed
"Measured value memory" Measured value (digital)	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Buffer" Last valid value	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Output memory" Next-to-last valid/ displayed value	

4.3.4.9.5.9 Delaying error messages

Name:
ErrorDelay01 to ErrorDelay02

This register specifies the number of consecutive conversion procedures where an error is pending until the corresponding individual error status bit is set. The delay applies to underflow, overflow and open circuit errors. This delay can be used to hide temporary measured value deviations, for example.

Data type	Value
UINT	0 to 65535

4.3.4.9.5.10 Time for composite error bit

Name:
SumErrorDelay01 to SumErrorDelay02

This register can be used to set the time that an error must remain pending before the composite error bit is set.

Data type	Value
UINT	0 to 65535

4.3.4.9.6 Analog input - Communication

The measured voltage data can be obtained via 2 different registers: The unevaluated measured value contains the scaled converter value. The evaluated measured value also takes the limit values and the configured replacement value strategy into consideration.

4.3.4.9.6.1 Analog input values - Original values

Name:
AnalogInput01 to AnalogInput02

These registers are used to indicate the actual input values after standardization.

Data type	Value
INT	-32767 to 32767
	-10000 to 10000

4.3.4.9.6.2 Analog input values - Limited

Name:
AnalogInput01 to AnalogInput02

This register is used to indicate the values of the Analog input values - Original values register. In addition, the settings for limit value monitoring and replacement value strategy are applied to this register.

Data type	Value
INT	-32767 to 32767
	-10000 to 10000

4.3.4.9.6.3 Sample time

Name:
Sampletime01 to Sampletime02

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	Information
INT	-32,768 to 32767	Nettime timestamp of the current input value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current input value

4.3.4.9.6.4 Status of the inputs

Name:
AnalogStatus01 to AnalogStatus02
UnderflowAnalogInput01 to UnderflowAnalogInput02
OverflowAnalogInput01 to OverflowAnalogInput02
OpenLineAnalogInput01 to OpenLineAnalogInput02
SumErrorAnalogInput01 to SumErrorAnalogInput02
SensorErrorAnalogInput01 to SensorErrorAnalogInput02
IoSuppErrorAnalogInput01 to IoSuppErrorAnalogInput02

The current error status of the module channels is displayed in this register, regardless of the configured replacement value strategy. Some error information may be delayed according to the previously configured condition.

Setting "Format of status information" in Automation Studio allows you to specify whether the status information is transferred as USINT or bitwise.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	UnderflowAnalogInput01 or 02	0	Value equals lower limit
		1	Below lower limit value
1	OverflowAnalogInput01 or 02	0	Value equals upper limit
		1	Above upper limit value
2	OpenLineAnalogInput01 or 02	0	No open line detected
		1	Open line detected
3	Reserved	0	
4	SumErrorAnalogInput01 or 02	0	No error detected
		1	Composite error detected
5	Reserved	0	
6	SensorErrorAnalogInput01 or 02	0	Sensor voltage OK
		1	Sensor load too high
7	IoSuppErrorAnalogInput01 or 02	0	Module voltage OK
		1	Energy supply not permitted

UnderflowAnalogInput

The signal underflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (see 4.3.4.9.5.9 "ErrorDelay" register).

OverflowAnalogInput

The signal overflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (see 4.3.4.9.5.9 "ErrorDelay" register).

SumErrorAnalogInput

This error information derives from the status of individual errors and is only activated after the configurable delay time has passed [ms] (see 4.3.4.9.5.10 "SumErrorDelay" register). Linking this error information to an application makes it possible to hide temporary temperature value overflows and underflows, for example.

SensorErrorAnalogInput

In addition to the analog input, the module also provides the option of supplying the connected encoder with 24 VDC. If the input impedance for the sensor is too high, however, the integrated voltage supply will fail.

IoSuppErrorAnalogInput

This error is activated immediately as soon as the module detects that the necessary supply voltage is no longer being provided (<20 VDC).

4.3.4.9.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.3.4.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 ms

4.3.5 X20AI2322

4.3.5.1 General information

The module is equipped with 2 inputs with 12-bit digital converter resolution. It is possible to select between the two current ranges 0 to 20 mA and 4 to 20 mA.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs, 0 to 20 mA or 4 to 20 mA
- 12-bit digital converter resolution

4.3.5.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2322	X20 analog input module, 2 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 30: X20AI2322 - Order data

4.3.5.3 Technical data

Product ID	X20AI2322
Short description	
I/O module	2 analog inputs 0 to 20 mA / 4 to 20 mA
General information	
B&R ID code	0xCAB2
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.8 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	0 to 20 mA/4 to 20 mA
Input type	Differential input
Digital converter resolution	12-bit
Conversion time	300 µs for all inputs
Output format	
Data type	INT
Current	0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Load	<400 Ω
Input protection	Protection against wiring with supply voltage
Permitted input signal	Max. ±50 mA
Output of the digital value during overload	Configurable

Table 31: X20AI2322 - Technical data

Product ID	X20AI2322
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Gain	
0 to 20 mA	0.08% 2)
4 to 20 mA	0.1% 2)
Offset	
0 to 20 mA	0.03% 3)
4 to 20 mA	0.16% 3)
Max. gain drift	
0 to 20 mA	0.009 %/°C 2)
4 to 20 mA	0.0113 %/°C 2)
Max. offset drift	
0 to 20 mA	0.004 %/°C 3)
4 to 20 mA	0.005 %/°C 3)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.05% 3)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 31: X20AI2322 - Technical data

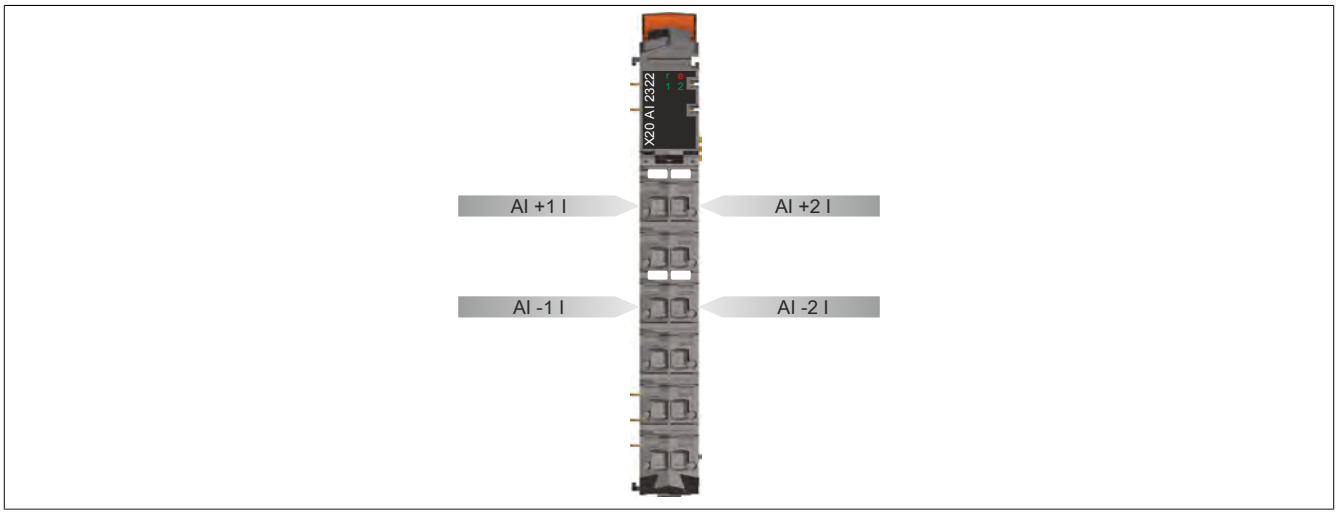
1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current measured value.
3) Based on the 20 mA measurement range.

4.3.5.4 LED status indicators

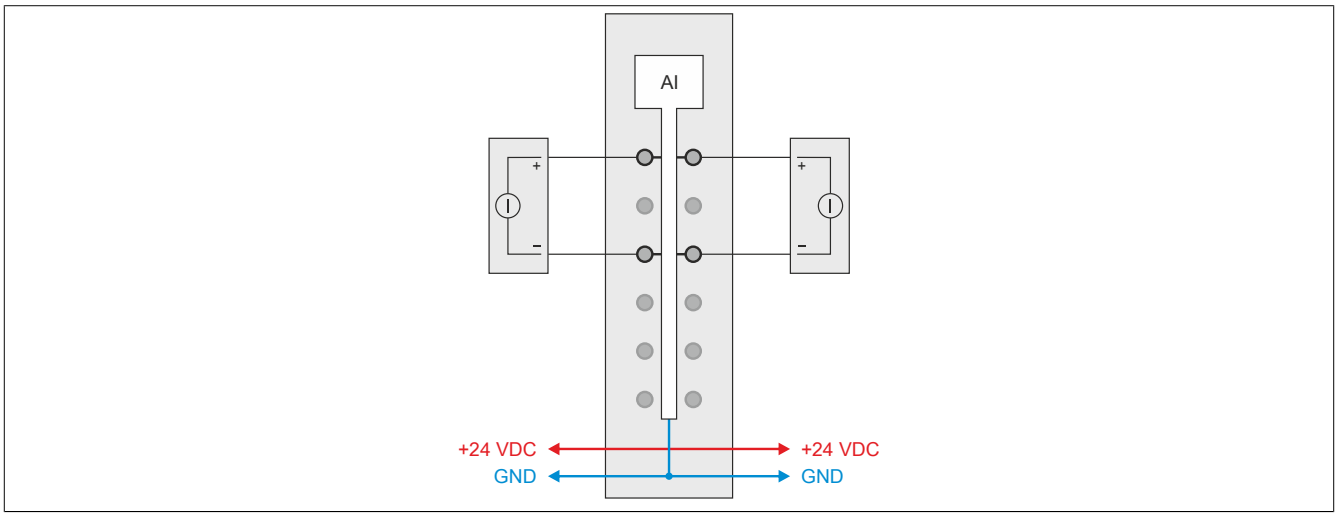
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

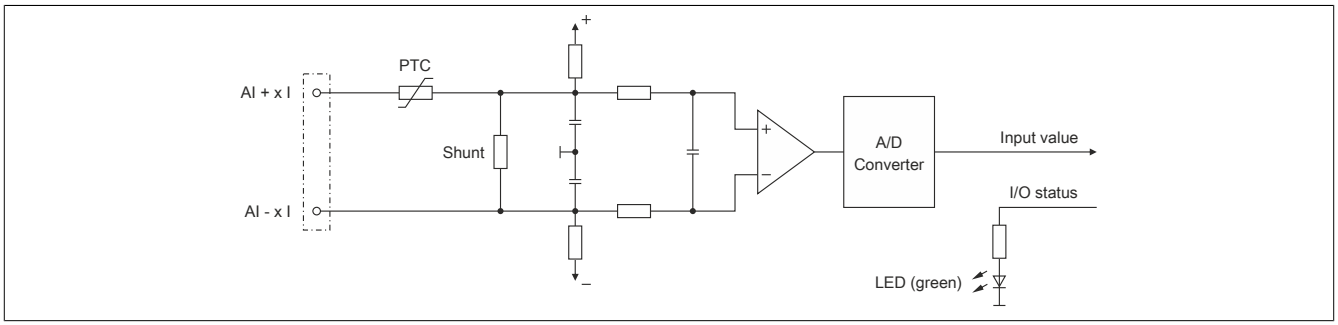
4.3.5.5 Pinout



4.3.5.6 Connection example



4.3.5.7 Input circuit diagram



4.3.5.8 Register description

4.3.5.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.5.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	Configuring the input filter	USINT				●
18	Channel type	USINT				●
20	Lower limit value	INT				●
22	Upper limit value	INT				●
Analog signal - Communication						
0	AnalogInput01	INT	●			
2	AnalogInput02	INT	●			
30	Input status	USINT	●			

4.3.5.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	Configuring the input filter	USINT				●
18	-	Channel type	USINT				●
20	-	Lower limit value	INT				●
22	-	Upper limit value	INT				●
Analog signal - Communication							
0	0	AnalogInput01	INT	●			
2	2	AnalogInput02	INT	●			
30	-	Input status	USINT		●		

1) The offset specifies the position of the register within the CAN object.

4.3.5.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.5.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

4.3.5.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput02

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	0 to 32767	Current signal 0 to 20 mA or 4 to 20 mA

4.3.5.8.6 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the scan rate for the channels is measured in ms. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

4.3.5.8.6.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

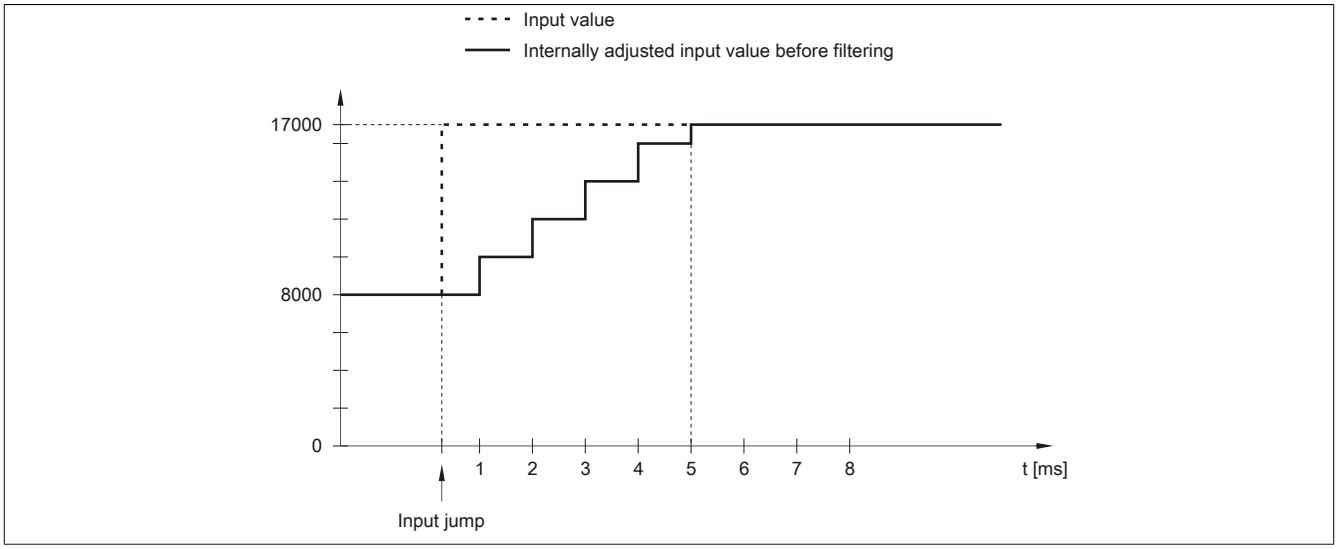


Figure 58: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

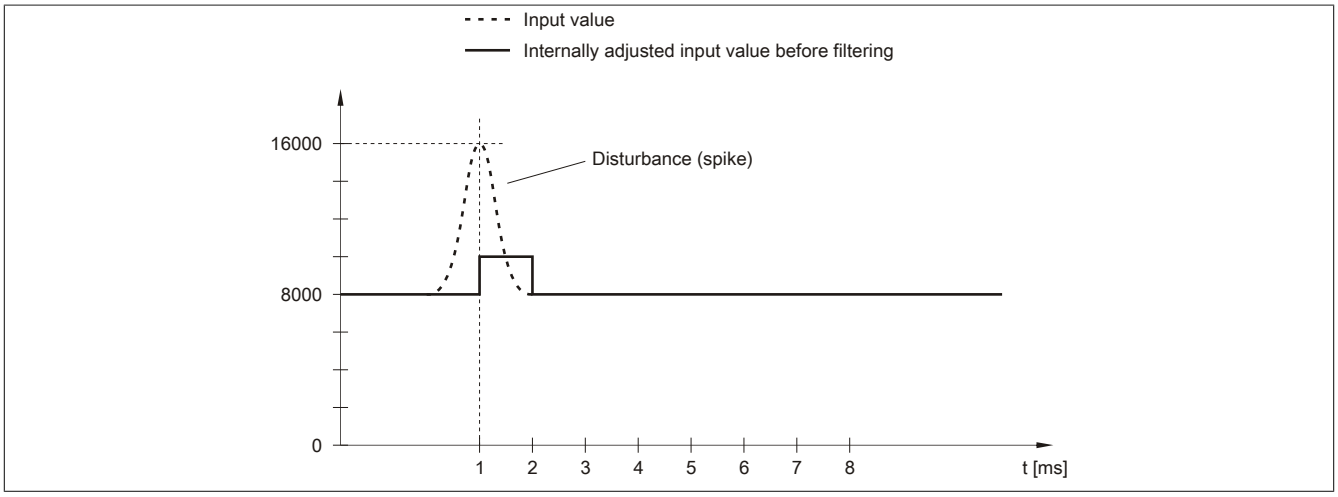


Figure 59: Adjusted input value for disturbance

4.3.5.8.6.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

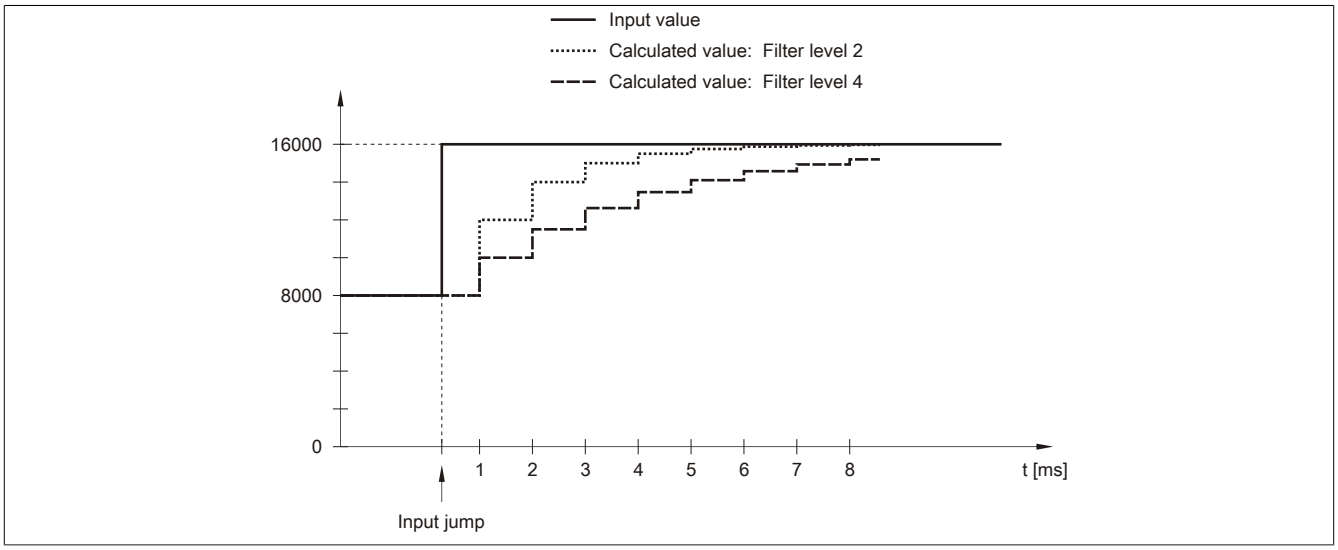


Figure 60: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

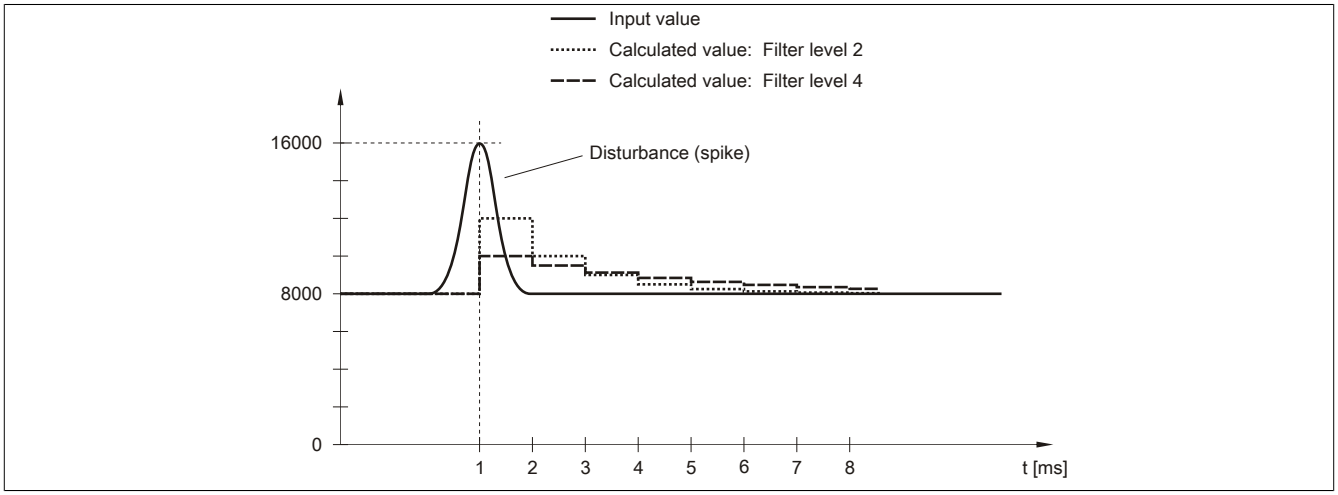


Figure 61: Calculated value during disturbance

4.3.5.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

4.3.5.8.8 Channel type

Name:
ConfigOutput02

This register can be used to set the range of the current signal. This is determined by how they are configured. The following input signals can be set:

- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	1	
2 - 3	Reserved	0	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
6 - 7	Reserved	0	

4.3.5.8.9 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Keep in mind that this setting applies to all channels!

4.3.5.8.10 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of 32767 corresponds to the maximum default value at 20 mA.

Keep in mind that this setting applies to all channels!

4.3.5.8.11 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
4 - 7	Reserved	0	

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	0 to 20 mA	4 to 20 mA
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	0	-8191 (0xE001)

4.3.5.8.12 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Inputs without filtering	100 µs
Inputs with filtering	500 µs

4.3.5.8.13 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Inputs without filtering	300 µs for all inputs
Inputs with filtering	1 ms

4.3.6 X20AI2437

4.3.6.1 General information

The module is equipped with 2 current measurement inputs with 16-bit digital converter resolution.

Each current measurement input has its own sensor supply. The two channels with their respective sensor supplies are electrically isolated from each other. The user can select between the two measurement ranges 4 to 20 mA and 0 to 25 mA.

- 2 analog current measurement inputs
- Electrically isolated analog channels
- Electrically isolated sensor supplies
- 16-bit digital converter resolution

4.3.6.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2437	X20 analog input module, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 32: X20AI2437 - Order data

4.3.6.3 Technical data

Product ID	X20AI2437
Short description	
I/O module	2 analog inputs 4 to 20 mA or 0 to 25 mA
General information	
B&R ID code	0xB784
Status indicators	I/O function per channel, operating state, module status, sensor supply per channel
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Sensor supply	Yes, using status LED and software
Power consumption	
Bus	0.05 W
Internal I/O	1.15 W [1]
External I/O	1.5 W [2]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [3]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	4 to 20 mA or 0 to 25 mA, configurable using software
Input type	Differential input
Digital converter resolution	15-bit
Data output rate	4.7 to 960 samples per second, configurable using software
Output format	INT
Output format	
4 to 20 mA	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 488.281 nA
0 to 25 mA	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 762.939 nA
0 to 25,000 µA	INT 0x0000 - 0x61A8 / 1 LSB = 0x0001 = 1000 nA
Load	<300 Ω
Input protection	Up to 30 VDC, reverse polarity protection (max. 0.1 A)
Open line detection	Yes, using software
Permitted input signal	0 to 25 mA
Output of the digital value during overload	Configurable
Conversion procedure	Sigma-delta
Max. error at 25°C	
Gain	
0 to 25 mA	<0.046% [4]
4 to 20 mA	<0.046% [4]
Offset	
0 to 25 mA	<0.004% [5]
4 to 20 mA	<0.013% [5]
Common-mode rejection	
DC	80 dB
50 Hz	Depends on the sampling rate: e.g. >130 dB for 50 scans per second
Common-mode range	0 to 7 V
Nonlinearity	<0.003% [5]
Input filter	
Hardware	1st-order low pass / cutoff frequency 2.5 kHz
Software	Sinc⁴ filter
Max. gain drift	
0 to 25 mA	0.003 %/°C [4]
4 to 20 mA	0.003 %/°C [4]
Max. offset drift	
0 to 25 mA	0.0002 %/°C [5]
4 to 20 mA	0.0007 %/°C [5]
Test voltage between	
Channel and channel	1000 VAC
Channel and bus	1000 VAC
To ground	1000 VAC
Sensor supply	
Nominal voltage	25 V ±2%
Nominal output current	Max. 30 mA
Short circuit protection	Yes, continuous

Table 33: X20AI2437 - Technical data

Product ID	X20AI2437
Electrical isolation	
Sensor supply - Channel	No
Sensor supply - Sensor supply	Yes
Max. voltage ripple	
Up to 100 kHz	≤2.2 mV
Up to 1 MHz	≤22 mV
Higher	≤100 mV
Short circuit current	
Typical	<50 mA
Maximum	60 mA
Behavior in the event of short circuit	Current limitation
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 33: X20AI2437 - Technical data

1) To reduce power dissipation, B&R recommends leaving unused inputs open.
2) Sensor supply
3) Ta min.: 0°C
   Ta max.: See environmental conditions
4) Based on the current measured value.
5) Based on the 25 mA measurement range.

4.3.6.4 LED status indicators

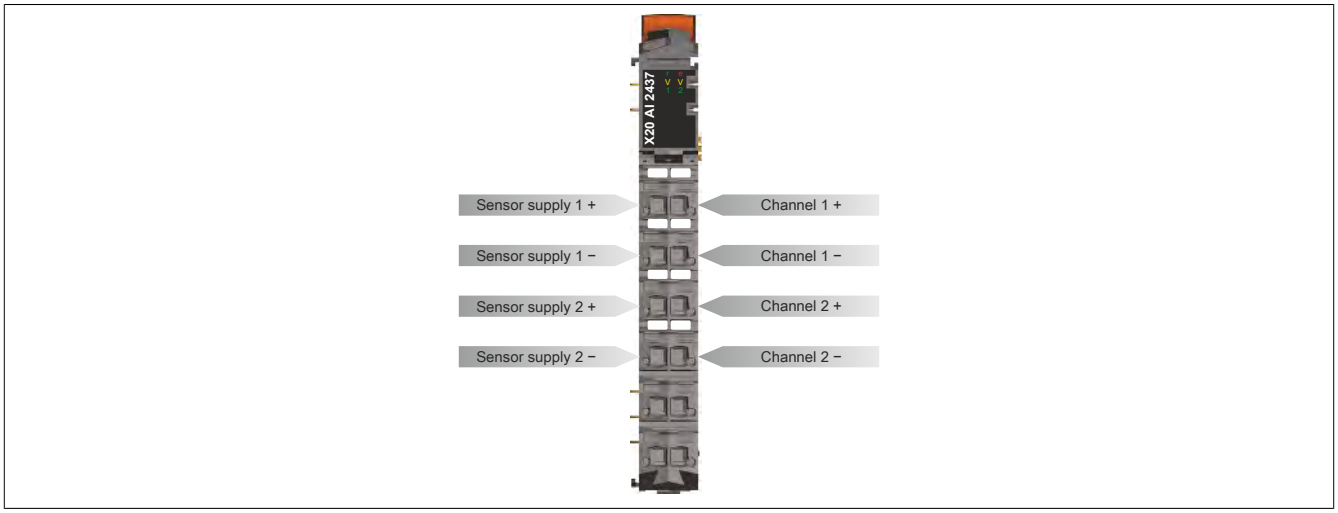
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	**Operating state**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
	Module status			
	e	Red	Off	No power to module or everything OK
			Single flash	A conversion error has occurred. This status is output along with a double flash on the channel LED of the analog input where the error occurs.
			On	Error or reset status
	Sensor supply			
	V	Yellow	Off	Overload
			On	Sensor supply in its normal operating range
	Analog input			
	1 - 2	Green	Off	Indicates one of the following cases: • No power to module • Channel disabled • Open line
			Single flash	Input signal overflow or underflow
			Double flash	A conversion error has occurred. A single flash is output on the red "e" module status LED.
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

4.3.6.5 Pinout

Shielded twisted pair cables should be used to minimize coupling disturbances. Use either one cable for each channel or a multiple twisted pair cable for both channels.

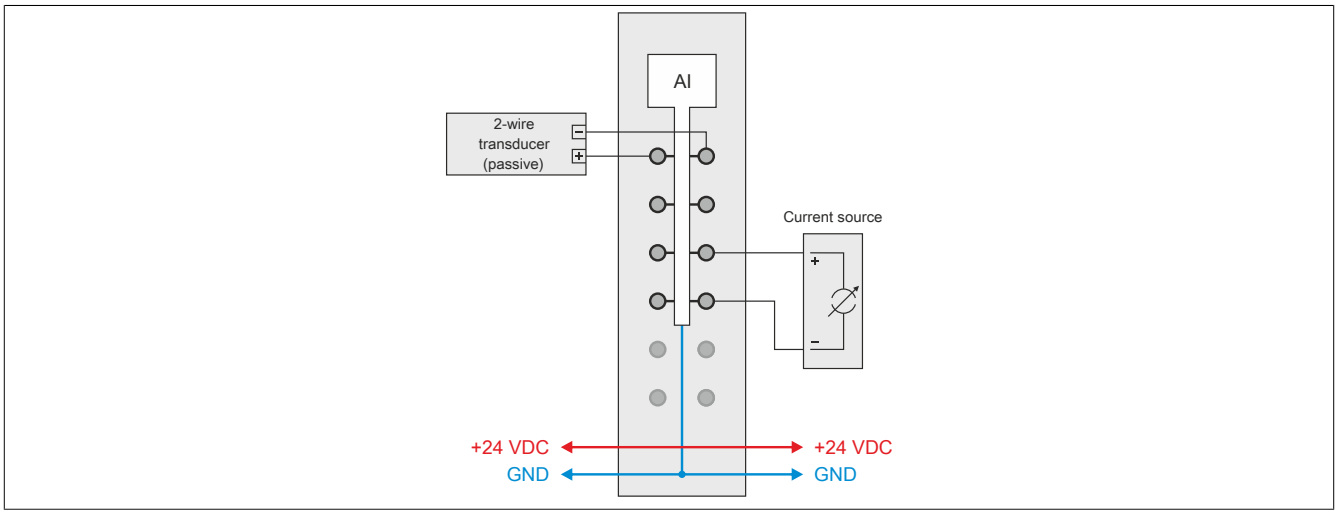


4.3.6.6 Connection examples

2-wire connections

A 2-wire connection can be implemented as follows:

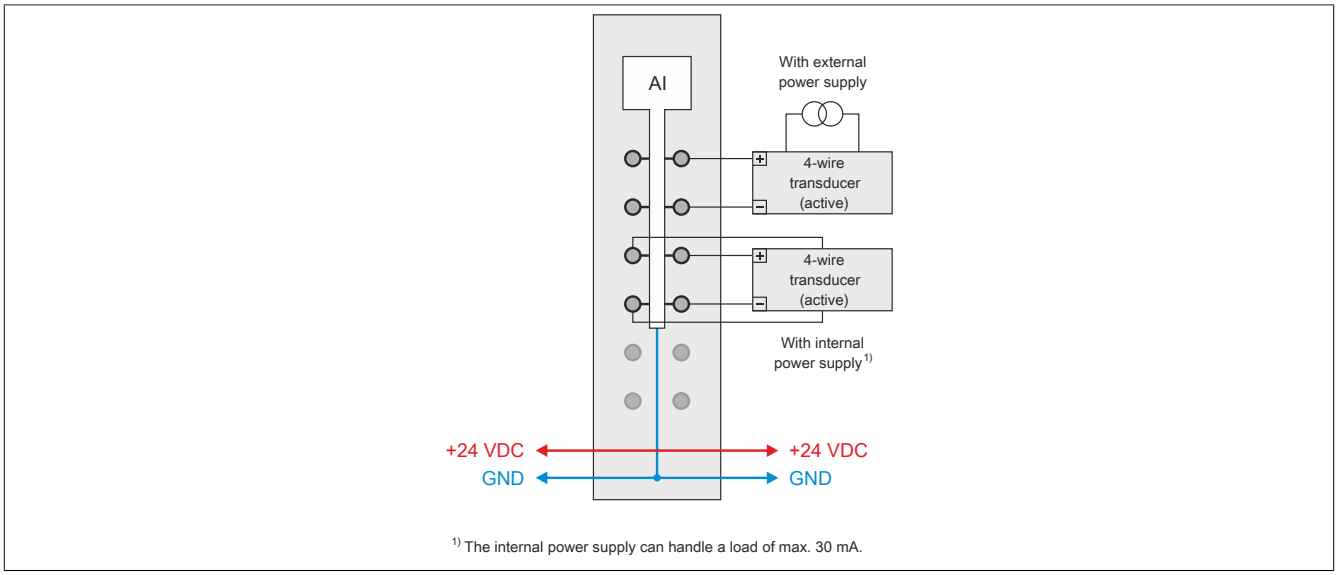
- 2-wire transducer
- Active current source



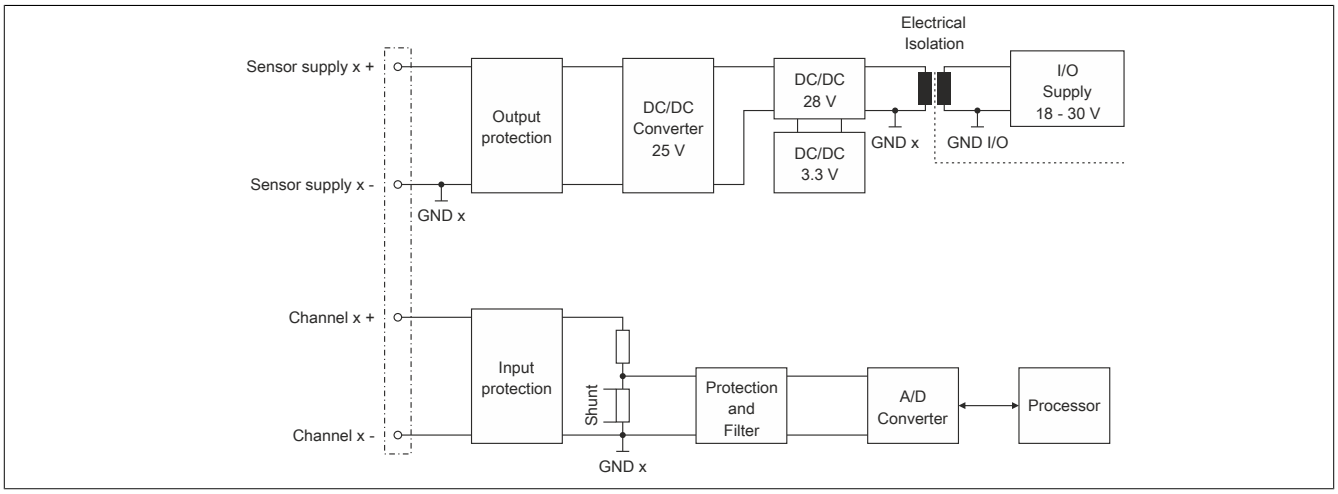
4-wire connections

A 4-wire connection can be implemented as follows:

- 4-wire transducer with external supply
- 4-wire transducer supplied by the module

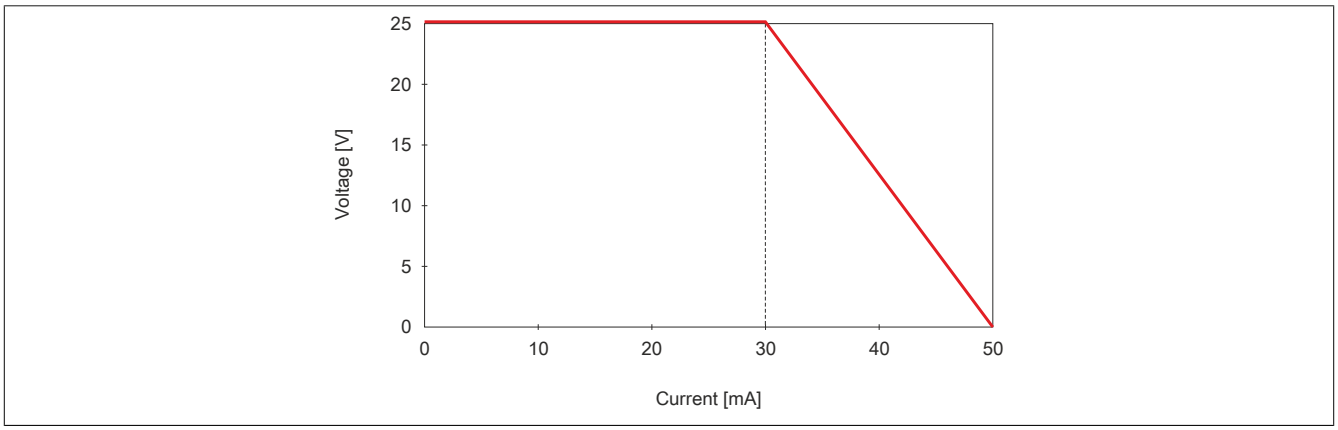


4.3.6.7 Input circuit diagram



4.3.6.8 Behavior in the event of short circuit

In the event of a short circuit, the output current for the sensor supply is limited according to the following diagram.



4.3.6.9 Register description

4.3.6.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.6.9.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
386 426	AnMode_1 AnMode_2	UINT				•
390 430	Samplerate_1 Samplerate_2	UINT				•
394 434	OpenLoopLimit_1 OpenLoopLimit_2	(U)INT				•
398 438	LowerLimit_1 LowerLimit_2	(U)INT				•
402 442	UpperLimit_1 UpperLimit_2	(U)INT				•
406 446	Hysteres_1 Hysteres_2	(U)INT				•
410 450	ReplacementLower_1 ReplacementLower_2	(U)INT				•
414 454	ReplacementUpper_1 ReplacementUpper_2	INT				•
418 458	ErrorDelay_1 ErrorDelay_2	UINT				•
422 462	SumErrorDelay_1 SumErrorDelay_2	UINT				•
466 482	PreparationInterval_1 PreparationInterval_2	UINT				•
Analog signal - Communication						
0 2	AnalogInput01 AnalogInput02	(U)INT	•			
258 262	Measurand01 Measurand02	(U)INT		•		
282 290	AnalogSampletime01 (16-bit) AnalogSampletime02 (16-bit)	INT	•			
284 292	AnalogSampletime01 (32-bit) AnalogSampletime02 (32-bit)	DINT	•			
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	UnderflowAnalogInput01 or 02	Bit 0				
	OverflowAnalogInput01 or 02	Bit 1				
	OpenLineAnalogInput01 or 02	Bit 2				
	ConversionErrorAnalogInput01 or 02	Bit 3				
	SumErrorAnalogInput01 or 02	Bit 4				
	SensorErrorAnalogInput01 or 02	Bit 6				
	IoSuppErrorAnalogInput01 or 02	Bit 7				

4.3.6.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
386 426	- -	AnMode_1 AnMode_2	UINT				•
390 430	- -	Samplerate_1 Samplerate_2	UINT				•
394 434	- -	OpenLoopLimit_1 OpenLoopLimit_2	INT				•
398 438	- -	LowerLimit_1 LowerLimit_2	(U)INT				•
402 442	- -	UpperLimit_1 UpperLimit_2	(U)INT				•
406 446	- -	Hysteres_1 Hysteres_2	(U)INT				•
410 450	- -	ReplacementLower_1 ReplacementLower_2	(U)INT				•
414 454	- -	ReplacementUpper_1 ReplacementUpper_2	(U)INT				•
418 458	- -	ErrorDelay_1 ErrorDelay_2	UINT				•
422 462	- -	SumErrorDelay_1 SumErrorDelay_2	UINT				•
466 482	- -	PreparationInterval_1 PreparationInterval_2	UINT				•
Analog signal - Communication							
0 2	0 2	AnalogInput01 AnalogInput02	(U)INT	•			
30 31	- -	AnalogStatus01 AnalogStatus02	USINT		•		
		UnderflowAnalogInput01 or 02	Bit 0				
		OverflowAnalogInput01 or 02	Bit 1				
		OpenLineAnalogInput01 or 02	Bit 2				
		ConversionErrorAnalogInput01 or 02	Bit 3				
		SumErrorAnalogInput01 or 02	Bit 4				
		SensorErrorAnalogInput01 or 02	Bit 6				
		IoSuppErrorAnalogInput01 or 02	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.3.6.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.6.9.4 General information

The module is equipped with 2 independent electrically isolated channels. Both channels can be used to read in an analog signal. All registers necessary for this have a dual design so that the channels can be configured and operated independently of one another.
The current input signals (0 to 25 mA) can be displayed in different formats.

Specific features:

- Channels electrically isolated
- Internal supply with short circuit protection <30 mA per channel
- Configurable filter (default 50 Hz)
- Selective line monitoring can be enabled for: open line (<2 mA), underflow (<3.6 mA) or overflow (>21 mA) of a configurable threshold
- Selectable error strategy: Replacement value for the respective threshold (default) or use the last valid value

4.3.6.9.5 Analog signal - Configuration

How the analog signal is displayed can be adapted to the requirements of the application. Separate configuration registers per channel are available to aid in this.

4.3.6.9.5.1 Channel parameters

Name:
AnMode_1 to AnMode_2

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be enabled individually and can be configured and operated independently.

Information:

Different limit values must be configured for any display normalizing that needs to take place.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel	0	Channel 0x turned off
		1	Channel 0x enabled (bus controller default setting)
1	Open line detection	0	Open line monitoring turned off
		1	Open line monitoring enabled (bus controller default setting)
2	Underflow detection	0	Underflow detection turned off
		1	Underflow detection enabled (bus controller default setting)
3	Replacement value strategy	0	Use replacement values when an error occurs (bus controller default setting)
		1	Keep the last valid converted value
4 - 5	Normalization	00	Displays 0 to 25 mA as 0 to 32767
		01	Displays 0 to 25 mA as 0 to 25000 [µA] (bus controller default setting)
		10	Displays 4 to 20 mA as 0 to 32767
		11	Displays 0 to 25 mA as 0 to 65535
6 - 15	Reserved	-	

4.3.6.9.5.2 Sample rate

Name:
Samplerate_1 to Samplerate_2

A sample rate can be configured for both analog inputs independently of one another. The following formula for this parameter is derived using the desired sampling frequency:

Sample rate for A/D converter = (4920000/1024)/sampling frequency

Data type	Value	
UINT	4 to 1023	Sample rate **Examples of configurable values** 960 ... 200 ms ... 5 Hz 480 ... 100 ms ... 10 Hz 320 ... 66.7 ms ... 15 Hz 192 ... 40 ms ... 25 Hz 160 ... 33.3 ms ... 30 Hz 96 ... 20 ms ... 50 Hz (bus controller default setting) 80 ... 16.7 ms ... 60 Hz 48 ... 10 ms ... 100 Hz 9 ... 2 ms ... 500 Hz 4 ... 1 ms ... 1000 Hz

Setting to 1000 Hz will result in jitter when acquiring measured values. Jitter-free operation is possible up to 960 Hz (sample rate setting = 5).

4.3.6.9.5.3 Limit value for open line detection

Name:
OpenLoopLimit_1 to OpenLoopLimit_2

The limit value for the respective analog input must be set when open circuit monitoring is enabled and if required by the configured normalization.

Data type	Value	Information
INT	-32767 to 32767	Open circuit limit value
UINT	0 to 65535	Open circuit limit value

If limit value monitoring is active, the corresponding error status is output after a configured delay when falling below this value. Using a default value of 2000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 2000
- Displays 0 to 25 mA as 0 to 32767: 2621, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -4096, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 5243, limit value = ([µA] * 65535) / 25000

4.3.6.9.5.4 Lower limit value

Name:
LowerLimit_1 to LowerLimit_2

If the value range needs to be restricted further, this register can be used to enter new user-specific lower limit values.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

The limit value must be set for the respective analog input depending on the configured normalization. After the configured delay time has passed, the corresponding error status is given if the respective value is overrun or underrun. When this error state occurs, the "AnalogInput0x" channel is evaluated according to the replacement value strategy. Using a default value of 3600 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 3600
- Displays 0 to 25 mA as 0 to 32767: 4718, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -819, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 9437, limit value = ([µA] * 65535) / 25000

4.3.6.9.5.5 Upper limit value

Name:
UpperLimit_1 to UpperLimit_2

If the value range needs to be restricted further, this register can be used to enter new user-specific upper limit values.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

The limit value must be set for the respective analog input depending on the configured normalization. After the configured delay time has passed, the corresponding error status is given if the respective value is overrun or underrun. When this error state occurs, the AnalogInput0x channel is evaluated according to the replacement value strategy. Using a default value of 21000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 21000
- Displays 0 to 25 mA as 0 to 32767: 27524, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 32767, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 55049, limit value = ([µA] * 65535) / 25000

4.3.6.9.5.6 Hysteresis

Name:
Hysteres_1 to Hysteres_2

If the user-specific limit values are being used, then a hysteresis range should also be defined. These registers configure how far a limit value can be exceeded before a response is triggered.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

The hysteresis value must be set for the respective analog input depending on the configured normalization. The error status is cleared if the actual analog value changes by at least this hysteresis value from the limit value in the allowed direction. Using a default value of 100 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 100
- Displays 0 to 25 mA as 0 to 32767: 131, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 156, limit value = [µA] * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 262, limit value = ([µA] * 65535) / 25000

4.3.6.9.5.7 Lower replacement value

Name:
ReplacementLower_1 to ReplacementLower_2

This register is used to define the lower static values to be displayed instead of the current measured value when the lower limit is violated.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

If the replacement strategy "Use replacement values when an error occurs" is enabled, the replacement value must be set for the respective analog input taking the configured normalization into account as well. When an overflow or underflow error status occurs, the "AnalogInput0x" channel is replaced with the corresponding value. Using a default value of 3600 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 3600
- Displays 0 to 25 mA as 0 to 32767: 4718, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -819, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 9437, limit value = ([µA] * 65535) / 25000

4.3.6.9.5.8 Upper replacement value

Name:
ReplacementUpper_1 to ReplacementUpper_2

This register is used to define the static values to be displayed instead of the current measured value when the upper limit is violated.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

If the replacement strategy "Use replacement values when an error occurs" is activated, the replacement value must be set for the respective analog input taking the configured normalization into account as well. When an overflow or underflow error status occurs, the AnalogInput0x channel is replaced with the corresponding value. Using a default value of 21000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 21000
- Displays 0 to 25 mA as 0 to 32767: 27524, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 32767, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 55049, limit value = ([µA] * 65535) / 25000

4.3.6.9.5.9 Delaying error messages

Name:
ErrorDelay_1 to ErrorDelay_2

This register specifies the number of consecutive conversion procedures where an error is pending until the corresponding individual error status bit is set. The delay applies to underflow, overflow and open circuit errors. This delay can be used to hide temporary measured value deviations, for example.

Data type	Value	Information
UINT	0 to 10	Error formation delay in conversion cycles
	2	Default value

4.3.6.9.5.10 Time for composite error bit

Name:
SumErrorDelay_1 to SumErrorDelay_2

This register specifies the time in milliseconds that one of the individual error bits must be pending until the composite error status bit is set.

Data type	Value	Information
UINT	0 to 65535	Composite error bit delay in ms
	4000	Default value

4.3.6.9.5.11 Preparation time for the measured values

Name:
PreparationInterval01 to PreparationInterval02

If the last valid measured value should be kept when violating the limit value, then PreparationInterval must be defined. The measured values continue to be acquired and converted according to the configured I/O update time. They are then checked and discarded if they do not meet the specifications. When an error does not occur, therefore, the measured value acquired 2 preparation intervals ago is constantly output.

Data type	Value	Information
UINT	0 to 65535	in 0.1 ms

Functionality:
Measured values are continuously converted and stored to measured value memory. The current contents of the measured value memory are checked within the configured interval. If a permissible value is present, then the contents of the buffer memory are passed to output memory and the contents of the measured value memory are passed to the buffer.
If the check turns up an impermissible value, then the contents of the measured value memory are discarded. The copy direction between output and buffer memory reverses and the last valid value continues to be output.

Information:

If configured to keep the last valid value, the delay time from measuring to outputting the value will be at least twice the preparation interval. In the worst case scenario, this can also take twice the interval time plus the configured conversion rate of the A/D converter.

"Application" Value being measured (analog)	
↓	Condition: - Conversion interval (A/D converter) elapsed
"Measured value memory" Measured value (digital)	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Buffer" Last valid value	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Output memory" Next-to-last valid/ displayed value	

4.3.6.9.6 Analog signal - Communication

4.3.6.9.6.1 Analog input values - Limited

Name:
AnalogInput01 to AnalogInput02

These registers take the values from the 4.3.6.9.6.2 "Analog input values - Original values" registers and use them to generate the evaluated input values. The configured auxiliary functions are applied to form these values.

Data type	Value	Information
INT	0 to 25000	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 4 to 20 mA
UINT	0 to 65535	Normalizing option 0 to 25 mA

Predefining values and timing
The value 0 (null) is output to the "AnalogInput" registers until a signal short circuit or converter error causes the value to be changed.

The timing for acquiring measured values is determined by the converter hardware and the set sampling rate. The two channels are converted independently of each other and are not synchronized with the X2X Link.

Conversion time
Channel 0x sampling rate

4.3.6.9.6.2 Analog input values - Original values

Name:
Measurand01 to Measurand02

The normalized input values are transferred to these registers. Depending on the normalization selected, the value range and the data type can be adapted to the requirements of the application.

Data type	Value	Information
INT	0 to 25000	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 4 to 20 mA
UINT	0 to 65535	Normalizing option 0 to 25 mA

4.3.6.9.6.3 Sample time

Name:
AnalogSampletime01 to AnalogSampletime02

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	Information
INT	-32,768 to 32767	Nettime timestamp of the current input value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current input value

4.3.6.9.6.4 Status of the inputs

Name:
AnalogStatus01 to AnalogStatus02
UnderflowAnalogInput01 to UnderflowAnalogInput02
OverflowAnalogInput01 to OverflowAnalogInput02
OpenLineAnalogInput01 to OpenLineAnalogInput02
ConversionErrorAnalogInput01 to ConversionErrorAnalogInput02
SumErrorAnalogInput01 to SumErrorAnalogInput02
SensorErrorAnalogInput01 to SensorErrorAnalogInput02
IoSuppErrorAnalogInput01 to IoSuppErrorAnalogInput02

The current error status of the module channels is displayed in this register, regardless of the configured replacement value strategy. Some error information may be delayed according to the previously configured condition.

Setting "Format of status information" in Automation Studio allows you to specify whether the status information is transferred as USINT or bitwise.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	UnderflowAnalogInput01 or 02	0	No error
		1	Underflow on Channel 0x
1	OverflowAnalogInput0101 or 02	0	No error
		1	Overflow on Channel 0x
2	OpenLineAnalogInput0101 or 02	0	No error
		1	Open line on Channel 0x
3	ConversionErrorAnalogInput01 or 02	0	No error
		1	Conversion error on Channel 0x
4	SumErrorAnalogInput0101 or 02	0	No error
		1	Composite error on Channel 0x
5	Reserved	-	
6	SensorErrorAnalogInput01 or 02	0	No error
		1	Sensor error on Channel 0x
7	IoSuppErrorAnalogInput01 or 02	0	No error
		1	I/O supply error on Channel 0x

UnderflowAnalogInput

The signal underflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (see 4.3.6.9.5.9 "ErrorDelay" register).

OverflowAnalogInput01

The signal overflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (see 4.3.6.9.5.9 "ErrorDelay" register).

OpenLineAnalogInput01

Depending on the configuration, measurement information is checked for values <2 mA (4.3.6.9.5.3 "OpenLoopLimit" register) to detect a failure signal. Open line detection takes place using a configurable hysteresis value (default: 100 µA, 4.3.6.9.5.6 "Hysteresis" register). It is possible to disable open line detection ("AnalogMode" (4.3.6.9.5.1 "AnalogMode" register) to suppress alarms when hardware is not present. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (4.3.6.9.5.9 "ErrorDelay" register).

ConversionErrorAnalogInput

This error status is triggered when the hardware exceeds the conversion time.

SumErrorAnalogInput01

This error information derives from the statuses of individual errors and is only activated after the configurable delay time has passed [ms] (see 4.3.6.9.5.10 "SumErrorDelay" register). Linking this error information to an application makes it possible to hide temporary temperature value overflows and underflows, for example.

SensorErrorAnalogInput

This error is activated immediately after a fault is detected in the internal sensor supply.

IoSuppErrorAnalogInput

This error is activated immediately as soon as the module detects that the necessary supply voltage is no longer being provided (<20 VDC).

4.3.6.9.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.3.6.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 ms

4.3.7 X20(c)AI2438

4.3.7.1 General information

The module is equipped with 2 current measurement inputs with 16-bit digital converter resolution. It supports the HART communication standard for data transfer, parameter configuration and diagnostics.

Each current measurement input has its own sensor supply. The two channels with their respective sensor supplies are electrically isolated from each other. The user can select between the two measurement ranges 4 to 20 mA and 0 to 25 mA.

- 2 analog current measurement inputs
- Integrated HART protocol
- Supports HART variables
- Electrically isolated analog channels
- Electrically isolated sensor supplies
- 16-bit digital converter resolution

4.3.7.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.3.7.3 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2438	X20 analog input module, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply, supports HART protocol	
X20cAI2438	X20 analog input module, coated, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply, supports the HART protocol	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 34: X20AI2438, X20cAI2438 - Order data

4.3.7.4 Technical data

Product ID	X20AI2438	X20cAI2438
Short description		
I/O module	2 analog inputs 4 to 20 mA or 0 to 25 mA	
General information		
B&R ID code	0xB3A9	0xE1EE
Status indicators	I/O function per channel, operating state, module status, sensor supply per channel, HART	
Diagnostics		
Module run/error	Yes, using status LED and software	
Inputs	Yes, using status LED and software	
Sensor supply	Yes, using status LED and software	
HART link	Yes, using status LED and software	
HART error	Yes, using status LED and software	
Power consumption		
Bus	0.05 W	
Internal I/O	1.15 W [1]	
External I/O	1.5 W [2]	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [3]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Analog inputs		
Input	4 to 20 mA or 0 to 25 mA, configurable using software	
Input type	Differential input	
Digital converter resolution	15-bit	
Data output rate		
With HART	4.7 to 10 samples per second, configurable using software	
Analog	4.7 to 100 samples per second, configurable using software	
Output format	INT	
Output format		
4 to 20 mA	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 488.281 nA	
0 to 25 mA	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 762.939 nA	
0 to 25,000 µA	INT 0x0000 - 0x61A8 / 1 LSB = 0x0001 = 1000 nA	
Load	<300 Ω	
Input protection	Up to 30 VDC, reverse polarity protection (max. 0.1 A)	
Open line detection	Yes, using software	
Permitted input signal	0 to 25 mA	
Output of the digital value during overload	Configurable	
Conversion procedure	Sigma-delta	
Max. error at 25°C		
Gain		
0 to 25 mA	<0.046% [4]	
4 to 20 mA	<0.046% [4]	
Offset		
0 to 25 mA	<0.004% [5]	
4 to 20 mA	<0.013% [5]	
Common-mode rejection		
DC	80 dB	
50 Hz	Depends on the sampling rate: e.g. >130 dB for 50 scans per second	
Common-mode range	0 to 7 V	
Nonlinearity	<0.003% [5]	
Input filter		
Hardware	1st-order low pass / cutoff frequency 100 Hz	
Software	Sinc⁴ filter	
Max. gain drift		
0 to 25 mA	0.003 %/°C [4]	
4 to 20 mA	0.003 %/°C [4]	
Max. offset drift		
0 to 25 mA	0.0002 %/°C [5]	
4 to 20 mA	0.0007 %/°C [5]	
Test voltage between		
Channel and channel	1000 VAC	
Channel and bus	1000 VAC	
To ground	1000 VAC	

Table 35: X20AI2438, X20cAI2438 - Technical data

Product ID	X20AI2438	X20cAI2438
Sensor supply		
Nominal voltage	25 V ±2%	
Nominal output current	Max. 30 mA	
Short circuit protection	Yes, continuous	
Electrical isolation		
Sensor supply - Channel	No	
Sensor supply - Sensor supply	Yes	
Max. voltage ripple		
Up to 100 kHz	≤2.2 mV	
Up to 1 MHz	≤22 mV	
Higher	≤100 mV	
Short circuit current		
Typical	<50 mA	
Maximum	60 mA	
Behavior in the event of short circuit	Current limitation	
HART		
Transfer rate	1200 bit/s	
Operating frequencies	1200 Hz / 2200 Hz	
Multi-drop operation		
Possible	Yes	
Participants	5	
Burst operation possible	Yes	
Transmission amplitude		
Minimum	400 mV_{pp}	
Typical	500 mV_{pp}	
Maximum	600 mV_{pp}	
Receiving amplitude		
Minimum	120 mV_{pp}	
Maximum	800 mV_{pp}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 35: X20AI2438, X20cAI2438 - Technical data

1) To reduce power dissipation, B&R recommends leaving unused inputs open.
2) Sensor supply
3) Ta min.: 0°C
   Ta max.: See environmental conditions
4) Based on the current measured value.
5) Based on the 25 mA measurement range.

4.3.7.5 LED status indicators

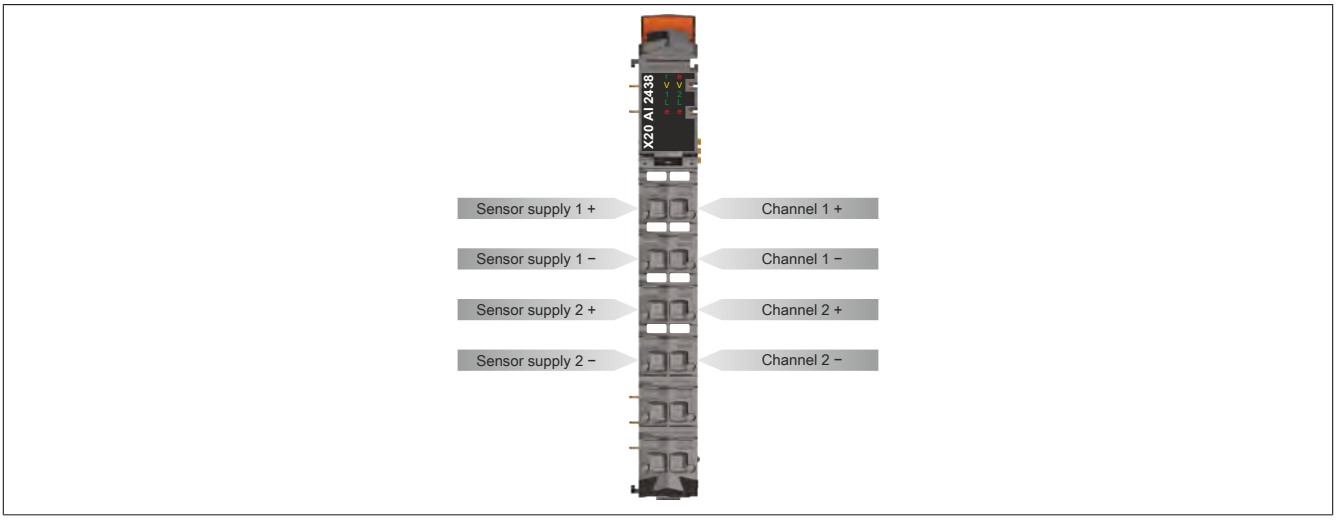
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	**Operating state**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
	Module status			
	e	Red	Off	No power to module or everything OK
			Single flash	A conversion error has occurred. This status is output along with a double flash on the channel LED of the analog input where the error occurs.
			On	Error or reset status
	Sensor supply			
	V	Yellow	Off	Module supply not connected or overload
			On	Sensor supply in its normal operating range
	Analog input			
	1 - 2	Green	Off	Indicates one of the following cases: • No power to module • Channel disabled • Open line
			Single flash	Input signal overflow or underflow
			Double flash	A conversion error has occurred. A single flash is output on the red "e" module status LED.
			On	Analog/digital converter running, value OK
	HART link			
	L	Green	Off	Indicates one of the following cases: • No power to module • HART disabled for the respective channel
			Flickering	Carrier signal active (DCD or RTS)
	HART error			
	e	Red	Off	Indicates one of the following cases: • Communication taking place without errors • No power to module • HART disabled for the respective channel
			On	Communication error

1) Depending on the configuration, a firmware update can take up to several minutes.

4.3.7.6 Pinout

Shielded twisted pair cables should be used to minimize coupling disturbances. Use either one cable for each channel or a multiple twisted pair cable for both channels.

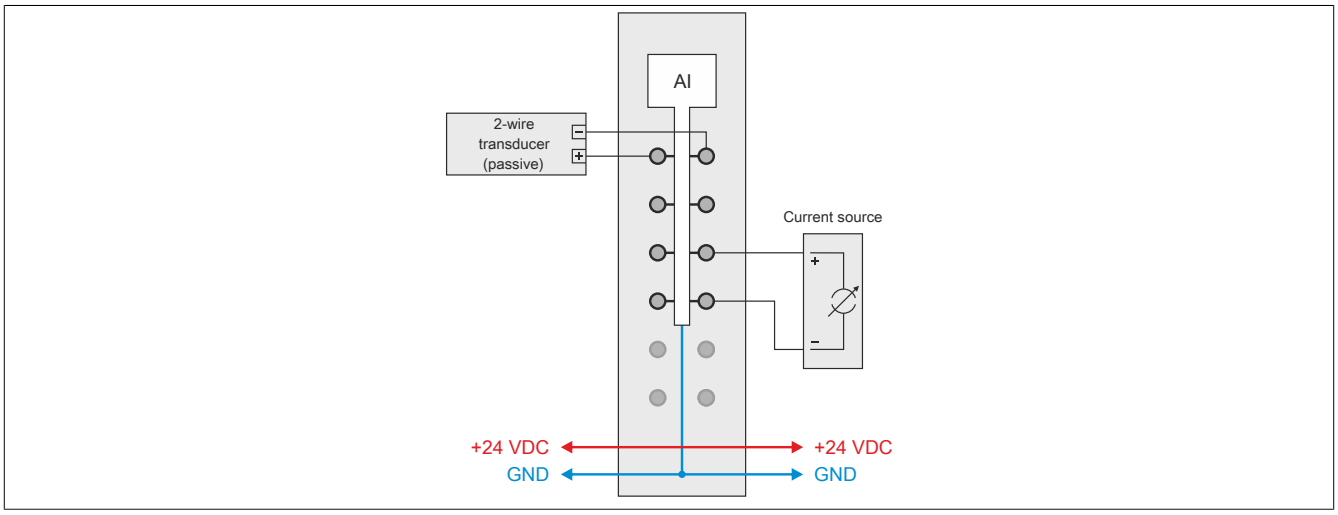


4.3.7.7 Connection examples

2-wire connections

A 2-wire connection can be implemented as follows:

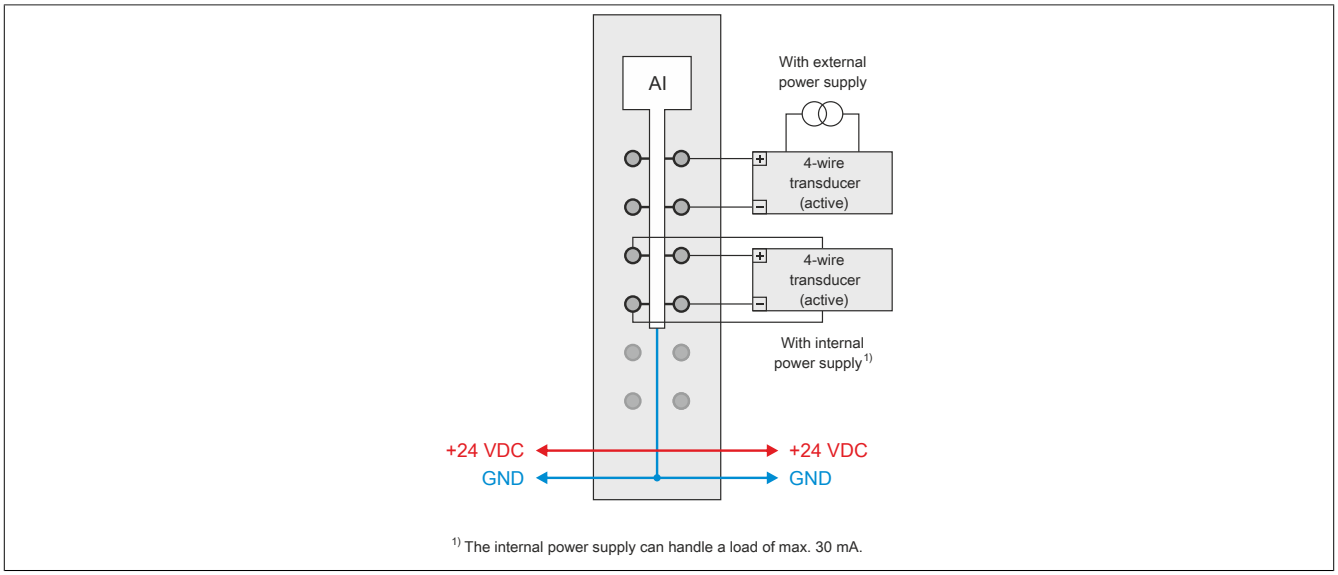
- 2-wire transducer
- Active current source



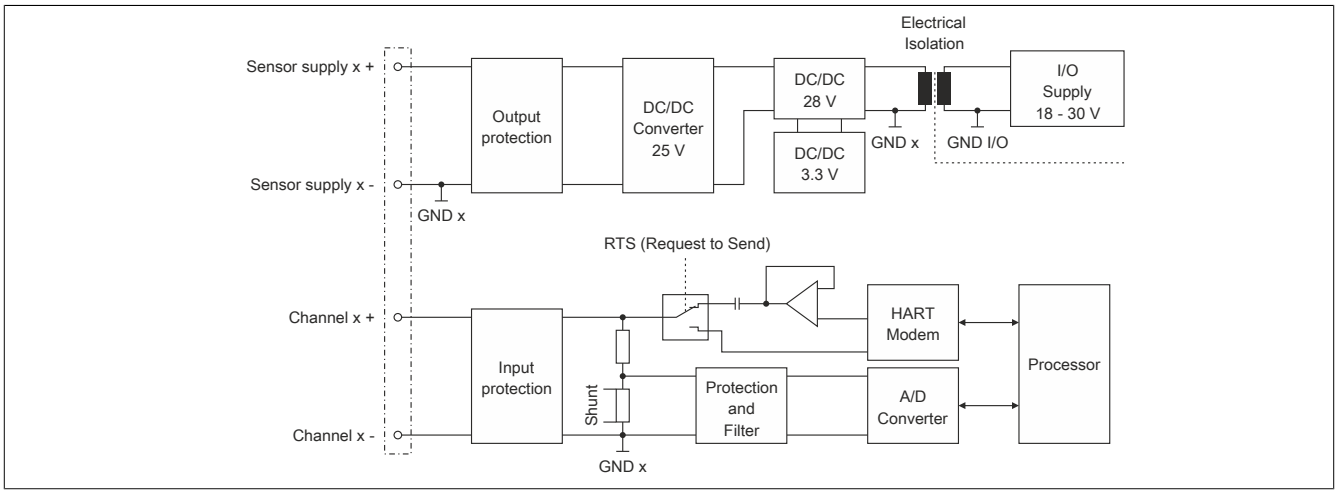
4-wire connections

A 4-wire connection can be implemented as follows:

- 4-wire transducer with external supply
- 4-wire transducer supplied by the module

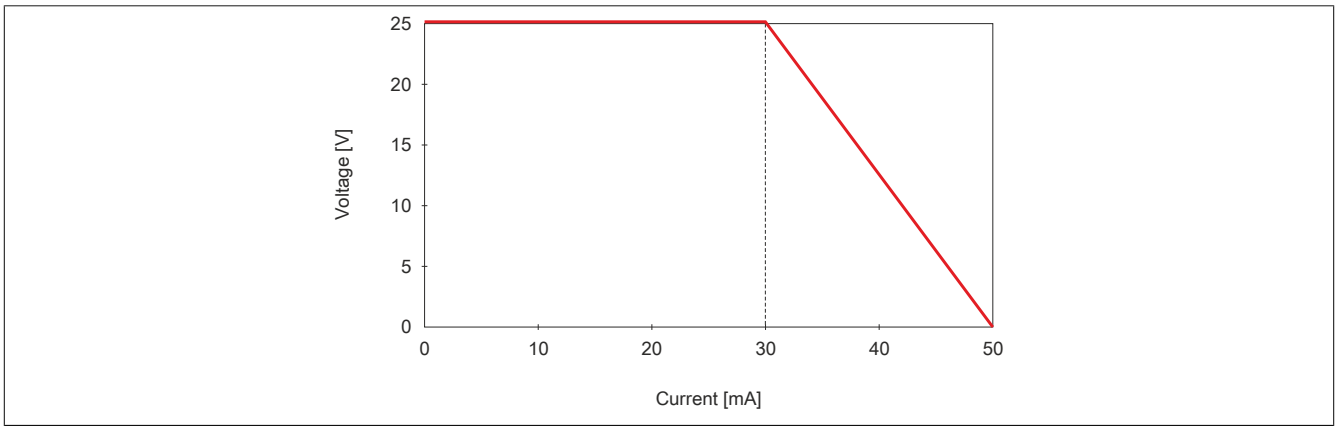


4.3.7.8 Input circuit diagram



4.3.7.9 Behavior in the event of short circuit

In the event of a short circuit, the output current for the sensor supply is limited according to the following diagram.



4.3.7.10 Register description

4.3.7.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.7.10.2 Register overview - Function model 0 (standard)

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
386 426	AnMode_1 AnMode_2	UINT				•
390 430	Samplerate_1 Samplerate_2	UINT				•
394 434	OpenLoopLimit_1 OpenLoopLimit_2	(U)INT				•
398 438	LowerLimit_1 LowerLimit_2	(U)INT				•
402 442	UpperLimit_1 UpperLimit_2	(U)INT				•
406 446	Hysteres_1 Hysteres_2	(U)INT				•
410 450	ReplacementLower_1 ReplacementLower_2	(U)INT				•
414 454	ReplacementUpper_1 ReplacementUpper_2	(U)INT				•
418 458	ErrorDelay_1 ErrorDelay_2	UINT				•
422 462	SumErrorDelay_1 SumErrorDelay_2	UINT				•
466 482	PreparationInterval_1 PreparationInterval_2	UINT				•
Analog signal - Communication						
0 2	AnalogInput01 AnalogInput02	(U)INT	•			
258 262	Measurand01 Measurand02	(U)INT		•		
282 290	AnalogSampletime01 (16-bit) AnalogSampletime02 (16-bit)	INT	•			
284 292	AnalogSampletime01 (32-bit) AnalogSampletime02 (32-bit)	DINT	•			
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	UnderflowAnalogInput01 or 02	Bit 0				
	OverflowAnalogInput01 or 02	Bit 1				
	OpenLineAnalogInput01 or 02	Bit 2				
	ConversionErrorAnalogInput01 or 02	Bit 3				
	SumErrorAnalogInput01 or 02	Bit 4				
	SensorErrorAnalogInput01 or 02	Bit 6				
	IoSuppErrorAnalogInput01 or 02	Bit 7				
HART - Configuration						
1537 1665	HartNodeCnt_1 HartNodeCnt_2	USINT				•
1539 1667	HartMode_1 HartMode_2	USINT				•
1541 1669	HartBurstNode_1 HartBurstNode_2	USINT				•
HART - Extended configuration						
1558 1686	HartNodeDisable_1 HartNodeDisable_2	UINT				•
1546 1674	HartProtTimeOut_1 HartProtTimeOut_2	UINT				•
1550 1678	HartProtRetry_1 HartProtRetry_2	UINT				•
1554 1682	HartPreamble_1 HartPreamble_2	UINT				•
HART - Communication (P2P)						
612 + N*24 1124 + N*24	PvInput01_0N (index N = 1 to 4) PvInput02_0N (index N = 1 to 4)	REAL	•	•		
617 + N*24 1129 + N*24	PvUnit01_0N (index N = 1 to 4) PvUnit02_0N (index N = 1 to 4)	USINT	•	•		
628 1140	PvSampleTime01 PvSampleTime02	DINT	•	•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
626 1138	PvSampleTime01 PvSampleTime02	INT	●			
566 1078	PvNodeComStatus01 PvNodeComStatus02	DINT		●		
HART - Communication (multidrop)						
612 + N*24 1124 + N*24	PvInput01_N (index N = 01 to 15) PvInput02_N (index N = 01 to 15)	REAL	●	●		
617 + N*24 1129 + N*24	PvUnit01_N (index N = 01 to 15) PvUnit02_N (index N = 01 to 15)	USINT	●	●		
604 + N*24 1116 + N*24	PvSampleTime01_N (index N = 01 to 15) PvSampleTime02_N (index N = 01 to 15)	DINT	●	●		
602 + N*24 1114 + N*24	PvSampleTime01_N (index N = 01 to 15) PvSampleTime02_N (index N = 01 to 15)	INT	●			
562 + N*4 1074 + N*4	PvNodeComStatus01_N (index N = 01 to 15) PvNodeComStatus02_N (index N = 01 to 15)	DINT		●		
HART - Extended communication						
522 1034	PvCountHartRequest01 PvCountHartRequest02	UINT	●			
530 1042	PvCountHartTimeout01 PvCountHartTimeout02	UINT	●			
538 1050	PvCountHartRxError01 PvCountHartRxError02	UINT	●			
546 1058	PvCountHartFrameError01 PvCountHartFrameError02	UINT	●			
554 1066	PvNodeFound01 PvNodeFound02	UINT	●			
558 1070	PvNodeError01 PvNodeError02	UINT	●			
Flatstream - Configuration						
1793	OutputMTU	USINT				●
1795	InputMTU	USINT				●
1797	FlatstreamMode	USINT				●
1799	Forward	USINT				●
1801	ForwardDelay	UINT				●
Flatstream - Communication						
1857	InputSequence	USINT	●			
1857 + N*2	RxByteN (index N = 1 to 15)	USINT	●			
1889	OutputSequence	USINT			●	
1889 + N*2	TxByteN (index N = 1 to 15)	USINT			●	

4.3.7.10.3 Register overview - Function model 254 (bus controller)

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
386 426	- -	AnMode_1 AnMode_2	UINT				●
390 430	- -	Samplerate_1 Samplerate_2	UINT				●
394 434	- -	OpenLoopLimit_1 OpenLoopLimit_2	(U)INT				●
398 438	- -	LowerLimit_1 LowerLimit_2	(U)INT				●
402 442	- -	UpperLimit_1 UpperLimit_2	(U)INT				●
406 446	- -	Hysteres_1 Hysteres_2	(U)INT				●
410 450	- -	ReplacementLower_1 ReplacementLower_2	(U)INT				●
414 454	- -	ReplacementUpper_1 ReplacementUpper_2	(U)INT				●
418 458	- -	ErrorDelay_1 ErrorDelay_2	UINT				●
422 462	- -	SumErrorDelay_1 SumErrorDelay_2	UINT				●
466 482	- -	PreparationInterval_1 PreparationInterval_2	UINT				●
Analog signal - Communication							
0 2	0 8	AnalogInput01 AnalogInput02	(U)INT	●			
30 31	- -	AnalogStatus01 AnalogStatus02	USINT		●		
		UnderflowAnalogInput01 or 02	Bit 0				
		OverflowAnalogInput01 or 02	Bit 1				
		OpenLineAnalogInput01 or 02	Bit 2				
		ConversionErrorAnalogInput01 or 02	Bit 3				
		SumErrorAnalogInput01 or 02	Bit 4				
		SensorErrorAnalogInput01 or 02	Bit 6				
		IoSuppErrorAnalogInput01 or 02	Bit 7				
HART - Configuration							
1537 1665	- -	HartNodeCnt_1 HartNodeCnt_2	USINT				●
1539 1667	- -	HartMode_1 HartMode_2	USINT				●
1541 1669	- -	HartBurstNode_1 HartBurstNode_2	USINT				●
HART - Extended configuration							
1558 1686	- -	HartNodeDisable_1 HartNodeDisable_2	UINT				●
1546 1674	- -	HartProtTimeOut_1 HartProtTimeOut_2	UINT				●
1550 1678	- -	HartProtRetry_1 HartProtRetry_2	UINT				●
1554 1682	- -	HartPreamble_1 HartPreamble_2	UINT				●
HART - Communication (P2P)							
636 1148	4 12	PvInput01_01 PvInput02_01	REAL	●			
612 + N*24 1124 + N*24	- -	PvInput01_0N (index N = 2 to 4) PvInput02_0N (index N = 2 to 4)	REAL		●		
641 1153	2 10	PvUnit01_01 PvUnit02_01	USINT	●			
617 + N*24 1129 + N*24	- -	PvUnit01_0N (index N = 2 to 4) PvUnit02_0N (index N = 2 to 4)	USINT		●		
566 1078	- -	PvNodeComStatus01 PvNodeComStatus02	DINT		●		
HART - Communication (multidrop)							
636 1148	4 12	PvInput01_01 PvInput02_01	REAL	●			
612 + N*24 1124 + N*24	- -	PvInput01_N (index N = 02 to 15) PvInput02_N (index N = 02 to 15)	REAL		●		
641 1153	2 10	PvUnit01_01 PvUnit02_01	USINT	●			
617 + N*24 1129 + N*24	- -	PvUnit01_N (index N = 02 to 15) PvUnit02_N (index N = 02 to 15)	USINT		●		
562 + N*4 1074 + N*4	- -	PvNodeComStatus01_N (index N = 01 to 15) PvNodeComStatus02_N (index N = 01 to 15)	DINT		●		
HART - Extended communication							
522 1034	- -	PvCountHartRequest01 PvCountHartRequest02	UINT		●		

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
530 1042	- -	PvCountHartTimeout01 PvCountHartTimeout02	UINT		•		
538 1050	- -	PvCountHartRxError01 PvCountHartRxError02	UINT		•		
546 1058	- -	PvCountHartFrameError01 PvCountHartFrameError02	UINT		•		
554 1066	- -	PvNodeFound01 PvNodeFound02	UINT		•		
558 1070	- -	PvNodeError01 PvNodeError02	UINT		•		

1) The offset specifies the position of the register within the CAN object.

4.3.7.10.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.3.7.10.4 General information

This module is equipped with two independent electrically isolated channels with integrated HART modems. Both channels can be used to read in an analog signal and handle HART communication. All registers necessary for this have a dual design so that the channels can be configured and operated independently of one another.
The current input signals (0 to 25 mA) can be displayed in various formats and used as conventional analog inputs. The integrated HART modems retrieve digital information from the memory on the HART slave using the same physical lines that modulate the HART signals.

When using the 0 to 25 mA current input variant, the module is conceived as a HART master for 2 channels (loops), with FSK modulation of the HART protocol and sensor supply for max. 4 slaves per channel.

Each channel can use one of the following connection variants:

- Connection of one HART node (point-to-point) with evaluation of the analog signal and output of 4 HART process variables OR
- Connection of up to 15 HART nodes in multidrop mode with output of the primary HART variable from activated nodes

Specific features:

- Channels electrically isolated
- Up to 4 or 15 HART input variables per channel
- Configurable sampling rate (input filter) to transfer HART and analog signal without interference (default: 50 Hz or 20 ms)
- Internal supply with short circuit protection <30 mA per channel
- Selective line monitoring can be enabled for: open line (<2 mA), underflow (<3.6 mA) or overflow (>21 mA) of a configurable threshold
- Selectable error strategy (static replacement value or retention of the last permitted value)
- Cyclic "HART status" polling (HART command 0), the status information received is made available for channel diagnostics
- Compatible with an additional secondary master in the HART network (module acts as the primary master)
- "HART communication error bit" (shows loss of HART connection if a connection had already been established successfully)
- Optional: Burst mode for one node per channel
- Optional: Cyclic polling of "HART variables" (HART command 3 or 9)
- Optional: Sensor supply for max. 4 nodes per channel in the multidrop variant
- Optional: Flatstream functionality (module acts as bridge for HART packets)

4.3.7.10.5 Analog signal - Configuration

How the analog signal is displayed can be adapted to the requirements of the application. Separate configuration registers per channel are available to aid in this.

4.3.7.10.5.1 Channel parameters

Name:
AnMode_1 to AnMode_2

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be enabled individually and can be configured and operated independently.

Information:

Different limit values must be configured for any display normalizing that needs to take place.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel	0	Channel 0x turned off
		1	Channel 0x enabled (bus controller default setting)
1	Open line detection	0	Open line monitoring turned off
		1	Open line monitoring enabled (bus controller default setting)
2	Underflow detection	0	Underflow detection turned off
		1	Underflow detection enabled (bus controller default setting)
3	Replacement value strategy	0	Use replacement values when an error occurs (bus controller default setting)
		1	Keep the last valid converted value
4 - 5	Normalization	00	Displays 0 to 25 mA as 0 to 32767
		01	Displays 0 to 25 mA as 0 to 25000 [µA] (bus controller default setting)
		10	Displays 4 to 20 mA as 0 to 32767
		11	Displays 0 to 25 mA as 0 to 65535
6 - 15	Reserved	-	

4.3.7.10.5.2 Sample rate

Name:
Samplerate_1 to Samplerate_2

A sample rate can be configured for both analog inputs independently of one another. The following formula for this parameter is derived using the desired sampling frequency:

Sample rate for A/D converter = (4920000/1024)/sampling frequency

Data type	Value	
UINT	4 to 1023	Sample rate **Examples of configurable values** 960 ... 200 ms ... 5 Hz 480 ... 100 ms ... 10 Hz 320 ... 66.7 ms ... 15 Hz 192 ... 40 ms ... 25 Hz 160 ... 33.3 ms ... 30 Hz 96 ... 20 ms ... 50 Hz (bus controller default setting) 80 ... 16.7 ms ... 60 Hz 48 ... 10 ms ... 100 Hz 9 ... 2 ms ... 500 Hz 4 ... 1 ms ... 1000 Hz

The fastest sample rate of 10 ms for the analog inputs is predefined by the cutoff frequency of the hardware filter. When using HART communication, however, a sample rate not faster than 100 ms is recommended.

4.3.7.10.5.3 Limit value for open line detection

Name:
OpenLoopLimit_1 to OpenLoopLimit_2

The limit value for the respective analog input must be set when open circuit monitoring is enabled and if required by the configured normalization.

Data type	Value	Information
INT	-32767 to 32767	Open circuit limit value
UINT	0 to 65535	Open circuit limit value

If limit value monitoring is active, the corresponding error status is output after a configured delay when falling below this value. Using a default value of 2000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 2000
- Displays 0 to 25 mA as 0 to 32767: 2621, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -4096, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 5243, limit value = ([µA] * 65535) / 25000

4.3.7.10.5.4 Preparation time for the measured values

Name:
PreparationInterval01 to PreparationInterval02

If the last valid measured value should be kept when violating the limit value, then PreparationInterval must be defined. The measured values continue to be acquired and converted according to the configured I/O update time. They are then checked and discarded if they do not meet the specifications. When an error does not occur, therefore, the measured value acquired 2 preparation intervals ago is constantly output.

Data type	Value	Information
UINT	0 to 65535	in 0.1 ms

Functionality:
Measured values are continuously converted and stored to measured value memory. The current contents of the measured value memory are checked within the configured interval. If a permissible value is present, then the contents of the buffer memory are passed to output memory and the contents of the measured value memory are passed to the buffer.
If the check turns up an impermissible value, then the contents of the measured value memory are discarded. The copy direction between output and buffer memory reverses and the last valid value continues to be output.

Information:

If configured to keep the last valid value, the delay time from measuring to outputting the value will be at least twice the preparation interval. In the worst case scenario, this can also take twice the interval time plus the configured conversion rate of the A/D converter.

"Application" Value being measured (analog)	
↓	Condition: - Conversion interval (A/D converter) elapsed
"Measured value memory" Measured value (digital)	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Buffer" Last valid value	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Output memory" Next-to-last valid/ displayed value	

4.3.7.10.5.5 Lower replacement value

Name:
ReplacementLower_1 to ReplacementLower_2

This register is used to define the lower static values to be displayed instead of the current measured value when the lower limit is violated.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

If the replacement strategy "Use replacement values when an error occurs" is enabled, the replacement value must be set for the respective analog input taking the configured normalization into account as well. When an overflow or underflow error status occurs, the "AnalogInput0x" channel is replaced with the corresponding value. Using a default value of 3600 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 3600
- Displays 0 to 25 mA as 0 to 32767: 4718, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -819, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 9437, limit value = ([µA] * 65535) / 25000

4.3.7.10.5.6 Upper replacement value

Name:
ReplacementUpper_1 to ReplacementUpper_2

This register is used to define the static values to be displayed instead of the current measured value when the upper limit is violated.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

If the replacement strategy "Use replacement values when an error occurs" is activated, the replacement value must be set for the respective analog input taking the configured normalization into account as well. When an overflow or underflow error status occurs, the AnalogInput0x channel is replaced with the corresponding value. Using a default value of 21000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 21000
- Displays 0 to 25 mA as 0 to 32767: 27524, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 32767, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 55049, limit value = ([µA] * 65535) / 25000

4.3.7.10.5.7 Lower limit value

Name:
LowerLimit_1 to LowerLimit_2

If the value range needs to be restricted further, this register can be used to enter new user-specific lower limit values.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

The limit value must be set for the respective analog input depending on the configured normalization. After the configured delay time has passed, the corresponding error status is given if the respective value is overrun or underrun. When this error state occurs, the "AnalogInput0x" channel is evaluated according to the replacement value strategy. Using a default value of 3600 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 3600
- Displays 0 to 25 mA as 0 to 32767: 4718, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -819, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 9437, limit value = ([µA] * 65535) / 25000

4.3.7.10.5.8 Upper limit value

Name:
UpperLimit_1 to UpperLimit_2

If the value range needs to be restricted further, this register can be used to enter new user-specific upper limit values.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

The limit value must be set for the respective analog input depending on the configured normalization. After the configured delay time has passed, the corresponding error status is given if the respective value is overrun or underrun. When this error state occurs, the AnalogInput0x channel is evaluated according to the replacement value strategy. Using a default value of 21000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 21000
- Displays 0 to 25 mA as 0 to 32767: 27524, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 32767, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 55049, limit value = ([µA] * 65535) / 25000

4.3.7.10.5.9 Hysteresis

Name:
Hysteres_1 to Hysteres_2

If the user-specific limit values are being used, then a hysteresis range should also be defined. These registers configure how far a limit value can be exceeded before a response is triggered.

Data type	Value
INT	-32767 to 32767
UINT	0 to 65535

The hysteresis value must be set for the respective analog input depending on the configured normalization. The error status is cleared if the actual analog value changes by at least this hysteresis value from the limit value in the allowed direction. Using a default value of 100 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 100
- Displays 0 to 25 mA as 0 to 32767: 131, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 156, limit value = [µA] * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 262, limit value = ([µA] * 65535) / 25000

4.3.7.10.5.10 Delaying error messages

Name:
ErrorDelay_1 to ErrorDelay_2

This register specifies the number of consecutive conversion procedures where an error is pending until the corresponding individual error status bit is set. The delay applies to underflow, overflow and open circuit errors. This delay can be used to hide temporary measured value deviations, for example.

Data type	Value	Information
UINT	0 to 10	Error formation delay in conversion cycles
	2	Default value

4.3.7.10.5.11 Time for composite error bit

Name:
SumErrorDelay_1 to SumErrorDelay_2

This register specifies the time in milliseconds that one of the individual error bits must be pending until the composite error status bit is set.

Data type	Value	Information
UINT	0 to 65535	Composite error bit delay in ms
	4000	Default value

4.3.7.10.6 Analog signal - Communication

4.3.7.10.6.1 Analog input values - Limited

Name:
AnalogInput01 to AnalogInput02

These registers take the values from the 4.3.6.9.6.2 "Analog input values - Original values" registers and use them to generate the evaluated input values. The configured auxiliary functions are applied to form these values.

Data type	Value	Information
INT	0 to 25000	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 4 to 20 mA
UINT	0 to 65535	Normalizing option 0 to 25 mA

Predefining values and timing
The value 0 (null) is output to the "AnalogInput" registers until a signal short circuit or converter error causes the value to be changed.

The timing for acquiring measured values is determined by the converter hardware and the set sampling rate. The two channels are converted independently of each other and are not synchronized with the X2X Link.

Conversion time
Channel 0x sampling rate

4.3.7.10.6.2 Analog input values - Original values

Name:
Measurand01 to Measurand02

The normalized input values are transferred to these registers. Depending on the normalization selected, the value range and the data type can be adapted to the requirements of the application.

Data type	Value	Information
INT	0 to 25000	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 4 to 20 mA
UINT	0 to 65535	Normalizing option 0 to 25 mA

4.3.7.10.6.3 Sample time

Name:
AnalogSampletime01 to AnalogSampletime02

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	Information
INT	-32,768 to 32767	Nettime timestamp of the current input value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current input value

4.3.7.10.6.4 Status of the inputs

Name:
AnalogStatus01 to AnalogStatus02
UnderflowAnalogInput01 to UnderflowAnalogInput02
OverflowAnalogInput01 to OverflowAnalogInput02
OpenLineAnalogInput01 to OpenLineAnalogInput02
ConversionErrorAnalogInput01 to ConversionErrorAnalogInput02
SumErrorAnalogInput01 to SumErrorAnalogInput02
SensorErrorAnalogInput01 to SensorErrorAnalogInput02
IoSuppErrorAnalogInput01 to IoSuppErrorAnalogInput02

The current error status of the module channels is displayed in this register, regardless of the configured replacement value strategy. Some error information may be delayed according to the previously configured condition.

Setting "Format of status information" in Automation Studio allows you to specify whether the status information is transferred as USINT or bitwise.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	UnderflowAnalogInput01 or 02	0	No error
		1	Underflow on Channel 0x
1	OverflowAnalogInput0101 or 02	0	No error
		1	Overflow on Channel 0x
2	OpenLineAnalogInput0101 or 02	0	No error
		1	Open line on Channel 0x
3	ConversionErrorAnalogInput01 or 02	0	No error
		1	Conversion error on Channel 0x
4	SumErrorAnalogInput0101 or 02	0	No error
		1	Composite error on Channel 0x
5	Reserved	-	
6	SensorErrorAnalogInput01 or 02	0	No error
		1	Sensor error on Channel 0x
7	IoSuppErrorAnalogInput01 or 02	0	No error
		1	I/O supply error on Channel 0x

UnderflowAnalogInput

The signal underflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (see 4.3.6.9.5.9 "ErrorDelay" register).

OverflowAnalogInput01

The signal overflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (see 4.3.6.9.5.9 "ErrorDelay" register).

OpenLineAnalogInput01

Depending on the configuration, measurement information is checked for values <2 mA (4.3.6.9.5.3 "OpenLoopLimit" register) to detect a failure signal. Open line detection takes place using a configurable hysteresis value (default: 100 µA, 4.3.6.9.5.6 "Hysteresis" register). It is possible to disable open line detection ("AnalogMode" (4.3.6.9.5.1 "AnalogMode" register) to suppress alarms when hardware is not present. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (4.3.6.9.5.9 "ErrorDelay" register).

ConversionErrorAnalogInput

This error status is triggered when the hardware exceeds the conversion time.

SumErrorAnalogInput01

This error information derives from the statuses of individual errors and is only activated after the configurable delay time has passed [ms] (see 4.3.6.9.5.10 "SumErrorDelay" register). Linking this error information to an application makes it possible to hide temporary temperature value overflows and underflows, for example.

SensorErrorAnalogInput

This error is activated immediately after a fault is detected in the internal sensor supply.

IoSuppErrorAnalogInput

This error is activated immediately as soon as the module detects that the necessary supply voltage is no longer being provided (<20 VDC).

4.3.7.10.7 HART

HART (Highway Addressable Remote Transducer) is a protocol for communicating with intelligent field devices. It was developed in order to more efficiently use the infrastructure for transferring analog signals. The digital HART notifications are modulated to the analog signal using Frequency Shift Keying (FSK). HART can thus use the same physical line as the analog signal without influencing the original function.
HART slaves are able to determine different process data independently and prepare HART concordantly. This protocol supports polling of the value of a process variable as well as its unit and status. Field devices usually supply their information after the master requests it. In newer revisions, it is also possible to transfer configuration data.

There are two different types of HART networks. In a *point-to-point* network, only one slave is connected to a HART master. Here, the analog signal and the HART signal can be transferred over the same line. Managing several slaves with HART requires what is known as a *multidrop* network. Here, each HART slave is assigned and identified by a unique address. Classic analog signals cannot be clearly traced in bus systems. As a result, the HART protocol does not support analog information transfers in multidrop networks up to and including HART Revision 5.

4.3.7.10.7.1 HART - Configuration

HART modules are analog modules equipped with a HART modem. For each channel, a separate HART network can be managed by the module, which acts as a primary master. Once configured successfully, the HART information is stored in the module where it can then be used by the PLC.

The number of HART slaves must be specified in the configuration.
If only one slave is connected to the HART channel, then it is part of a point-to-point network. The module can then prepare up to four process variables from the connected slave.
Multidrop mode allows up to 15 HART slaves to be connected. The primary process variable from each slave is then retrieved.

HartNodeCnt

Name:
HartCodeCnt_1 to HartCodeCnt_2

These registers tell the module how many HART slaves are connected to a channel.

Information:

If a slave is not connected to one of the HART channels, the value "0" should be defined in this register. This shortens the I/O update time and avoids superfluous error messages.

Data type	Value	Information	
USINT	0	HART communication disabled for this channel	
	1	Point-to-point	Standard HART communication (bus controller default)
	2 to 15	Multidrop	Number of HART slave nodes

HartBurstNode

Name:
HartBurstNode_1 to HartBurstNode_2

In addition to the type of network, the user can also choose from two different types of communication behavior. Conventional HART communication relies on polling. The module requests the data from the individual HART slaves and receives the corresponding information from each slave as a response. If a HART node should be queried in short time intervals, the user can configure burst mode for channels on one node. In this case, the slave transmits the node's information cyclically without constant prompting from the master.
The "HartBurstNode" registers are therefore used to enter the node numbers (short address) for the channels whose information should be retrieved using burst mode. Burst mode itself is enabled with the "HartMode" register.

Data type	Value	Information	
USINT	0 to 15	Point-to-point	0 (bus controller default)

HartMode

Name:
HartMode_1 to HartMode_2

The user can use these registers to configure the communication behavior of each of the HART channels. Generally, the HART nodes are polled individually. This register can still be used to start or stop burst mode when needed. In burst mode, a node transmits its information cyclically instead of continuously. As a result, the HART standard allows the simultaneous usage of both burst mode and polling.

Information:

To retrieve information with burst mode, theHartBurstNode register must be configured correctly.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Slave polling mode	0	Polling mode enabled (Bus Controller Default)
		1	Polling mode disabled
1	Start slave burst mode	0	No response to burst (bus controller default)
		1	Enables burst mode in the HartBurstNode node
2	Stop slave burst mode	0	No response to burst (bus controller default)
		1	Disables burst mode, if enabled
3 - 7	Reserved	-	

4.3.7.10.7.2 HART - Communication

Once the configuration has been completed, the information is retrieved automatically and transferred to the module's registers. A separate register in the module is implemented for each piece of information. HART modules are designed to retrieve up to 15 pieces of information per channel. The module reads in the data, stores it in temporary memory and prepares it for retrieval. When the X2X master accesses the module registers, it is irrelevant whether the HART data originates from a point-to-point network or a multidrop network.

Overview of internal module mapping

	Point-to-point network (1 HART slave)	*Multidrop network (2 to 15 HART slaves)*
(Pv)Input_01	Primary piece of information from HART node 1	Primary piece of information from HART node 1
(Pv)Input_02	Secondary piece of information from HART node 1	Primary piece of information from HART node 2
...	...	...
(Pv)Input_04	Quaternary piece of information from HART node 1	Primary piece of information from HART node 4
(Pv)Input_05	Reserved	Primary piece of information from HART node 5
...	...	...
(Pv)Input_15	Reserved	Primary piece of information from HART node 15

The HART specifications stipulates that information from a HART node be split into various pieces. The value of a process variable is stored to the respective "PvInput" register and has a size of 4 bytes (REAL) in accordance with the HART specification. Due to the length limitation of 30 bytes on the X2X link, there are restrictions to the number of possible cyclic variables. It is recommended to only transfer a maximum of 2 "PvInput" registers cyclically to the X2X master. All other information should be transferred in a different way. To access HART information, the user can choose from among the following methods:

- Data points that are configured to be transferred cyclically are read once per bus cycle. This method allows information to be exchanged between the module and the X2X master in real time. Nevertheless, the length limitation may prevent all data from being retrieved within one cycle.
- If the AsIOAcc library is used, information is retrieved acyclically only when it is needed, i.e. communication can be adapted to the application running on the X2X master. In this way, all of the necessary module registers on the X2X link can be polled despite the length limitation.
  This method of information exchange is not real-time capable.
- HART modules are equipped with a FlatStream interface. When using FlatStream communication, the module acts a bridge between the X2X master and the HART slave, i.e. the X2X master communicates directly with the HART slave (see section "FlatStream communication""FlatStream communication").
  FlatStream communication is also not real-time capable. It allows unrestricted access to the HART slave. The user must have sufficient knowledge of the HART protocol command set as well as the capabilities of the HART slave device.

PvInput

Name:
PvInput_01 to PvInput_15
PvInput_01_01 to PvInput_01_15
PvInput_02_01 to PvInput_02_15

These registers return the current value of the process variable that has been read.

Information:

These registers are of data type REAL, which means that the available bytes on the X2X Link are filled more quickly when operated cyclically. If information from several slave nodes is needed, it must be retrieved acyclically or using Flatstream .

Data type	Value	Information
REAL	IEEE745 SPF	32-bit data type with valid value
	0x7FA00000	Not a number (NaN) with invalid value

PvUnit

Name:
PvUnit_01 to PvUnit_15
PvUnit_01_01 to PvUnit_01_15
PvUnit_02_01 to PvUnit_02_15

These registers return a HART-specific code that specifies the unit for the measured value. The coding for this is established in the HART specification.

Data type	Value
USINT	See description of the HART slave See HART specification

PvSampleTime

Name:
PvSampleTime01 to PvSampleTime02
PvSampleTime01_01 to PvSampleTime01_15
PvSampleTime02_01 to PvSampleTime02_15

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	Information
INT	-32,768 to 32767	Nettime timestamp of the current input value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current input value

This refers to the point in time when the HART master receives the slave's response. This is a way to check whether new HART information has been read since the last X2X cycle.

Information:

The cycle times of a HART network are relatively long so that it is not possible to reliably determine when the measured value is retrieved with just this information.

PvNodeComStatus

Name:
PvNodeComStatus01 to PvNodeComStatus02
PvNodeComStatus01_01 to PvNodeComStatus01_15
PvNodeComStatus02_01 to PvNodeComStatus02_15

These registers return information about whether a value that has been read is valid. According to the HART specification, this type of status register consists of two parts. The high byte stores the "response code" and the low byte the "field device status". This makes it possible to check the current status of a read process variable.

These registers can be checked before further processing information in temporary storage. If the current value is 0x0000, an error was not detected during the HART transfer and the information from the checked node can be used. If a different value is present, the situation in the HART network should be checked. This can be done using an extension register, for example.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Quality - Node information 2 to n	0	Digital measured value okay
		1	Measured value outside the permitted range
1	Quality - Node information 1	0	Digital measured value okay
		1	Measured value outside the permitted range
2	Limit violation	0	Parameter okay
		1	Invalid measured value(s) or encoder supply value
3	Static analog signal	0	Normal value change/fluctuation
		1	Constant analog value of Node 1 slave
4	Additional status information (only supported by a few slaves)	0	Not available
		1	Available (only using Flatstream command #48)
5	Restart	0	Normal operation
		1	Field device restarts
6	Device ID	0	Unchanged
		1	Changed
7	Device error	0	Measured value okay
		1	Questionable measured value information
8 - 14	Response code, if relevant	x	See **HART-specific response code**
15	Error - Communication	0	Error-free communication (response code irrelevant)
		1	Faulty communication (response code relevant)

HART-specific response code (excerpt):

0x82 … Receive buffer overflow 0x88 … Checksum incorrect 0x90 … Faulty protocol structure 0xA0 … Overrun 0xC0 … Parity not allowed 0xFF … Timeout	If a HART communication error occurs, the response code is written. Bit 15 is always set.

Retrieving information that has been read

After the node data has been transferred to the module registers, the information can be retrieved from the module. A separate register in the module is implemented for each piece of information.

PvCountHartRequest

The "PvCountHartRequest" registers are increased once the module is ready to transmit a message to the corresponding channel.

Data type	Value
UINT	0 to 65535

PvCountHartTimeout

The "PvCountHartTimeout" registers are increased if the slave exceeds the maximum permitted time before responding to the module's request.

Data type	Value
UINT	0 to 65535

PvCountHartRxError

The "PvCountHartRxError" registers are increased if communication errors occur on Layer 1 of the OSI model (e.g. transmission error as per parity bit).

Data type	Value
UINT	0 to 65535

PvCountHartFrameError

The "PvCountHartFrameError" registers are increased if communication errors occur on Layer 2 of the OSI model (e.g. faulty telegram structure).

Data type	Value
UINT	0 to 65535

PvNodeFound

Name:
PvNodeFound01 to PvNodeFound02

These registers provide information about which nodes were detected on which channel (slave identified successfully).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
1	Node 2 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
...		...	
13	Node 14 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
14	Node 15 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
15	Reserved	-	

PvNodeError

Name:
PvNodeError01 to PvNodeError02

These registers contain the HART communications error bits. These bits are set if the connection to a node was established successfully but the node at some point no longer responds as it should (e.g. the HART slave exceeds the configured timeout / number of retries).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
1	Node 2 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
...		...	
13	Node 14 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
14	Node 15 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
15	Reserved	-	

4.3.7.10.7.3 Extended configuration

The additional configuration registers are specified values when the module is started. In most systems, the user does not need to make any adjustments here. Register values should only be changed if HART network communication is not taking place satisfactorily.

HartNodeDisable

Name:
HartNodeDisable_1 to HartNodeDisable_2

These registers are intended for things like maintenance. They make it possible to cut off configured HART nodes to suppress error messages for a certain period of time. During normal operation, the configured nodes must be switched active to guarantee that the procedure runs smoothly.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Enabled (bus controller default setting)
		1	Disabled
1	Node 2 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default)
...		...	
13	Node 14 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default)
14	Node 15 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default)
15	Reserved	-	

HartProtTimeOut

Name:
HartProtTimeOut_1 to HartProtTimeOut_2

These registers specify the time span within which the slave must respond for the response to be valid.

Data type	Values [ms]	Information
UINT	0 to 65535	Bus controller default: 256 [ms]

HartProtRetry

Name:
HartProtRetry_1 to HartProtRetry_2

These registers determine how many times the master retries a request if it receives an invalid response or no response at all.

Data type	Value	Information
UINT	0 to 65535	Bus controller default: 3 attempts

HartPreamble

Name:
HartPreamble_1 to HartPreamble_2

The length of the preamble can be set in these registers. The preamble is used to synchronize the receiver to the transmitter. The longer the declared preamble, the less chance that a communication error will occur. Nevertheless, a useful signal is not transmitted during synchronization so the preamble should be kept as short as possible.

Data type	Value	Information
UINT	5 to 20	Bus controller default: 20

4.3.7.10.8 FlatStream communication

4.3.7.10.8.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

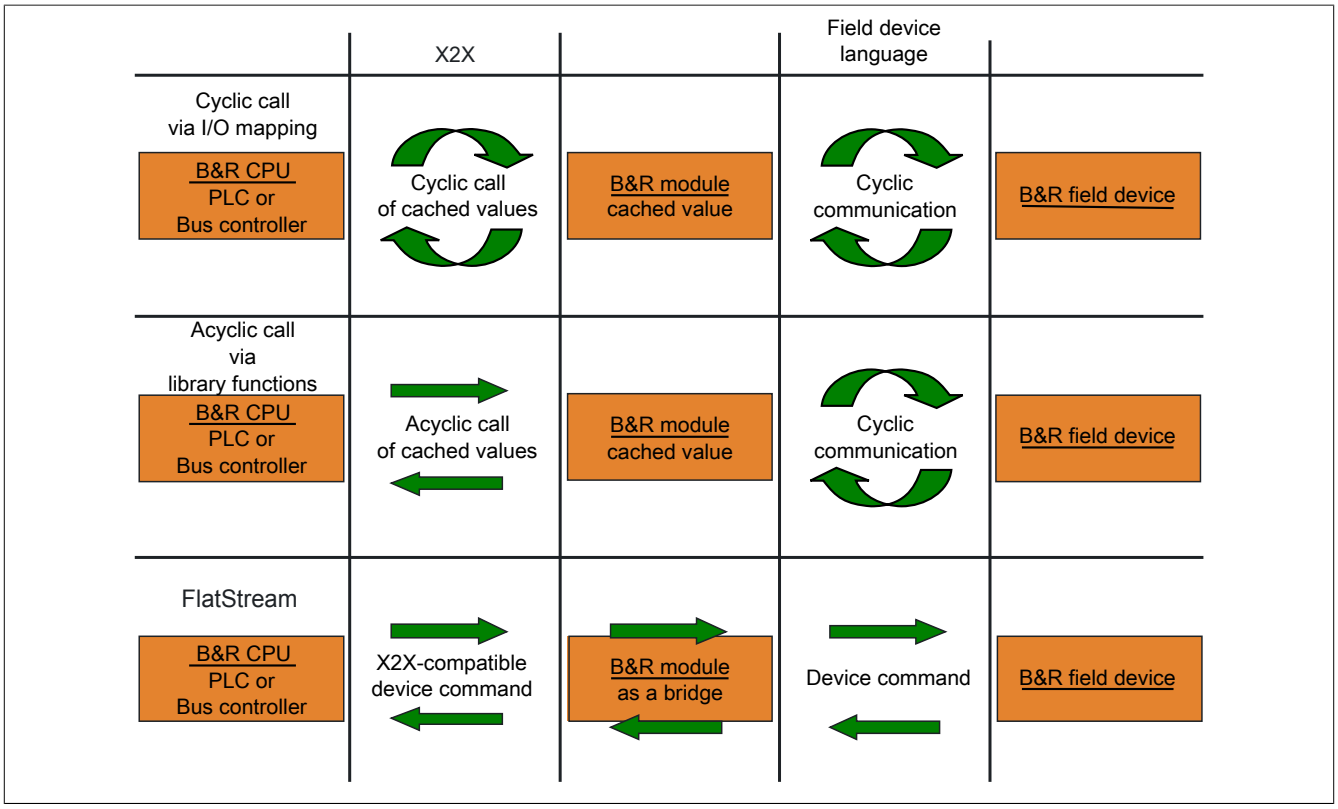


Figure 62: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.3.7.10.8.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.3.7.10.8.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

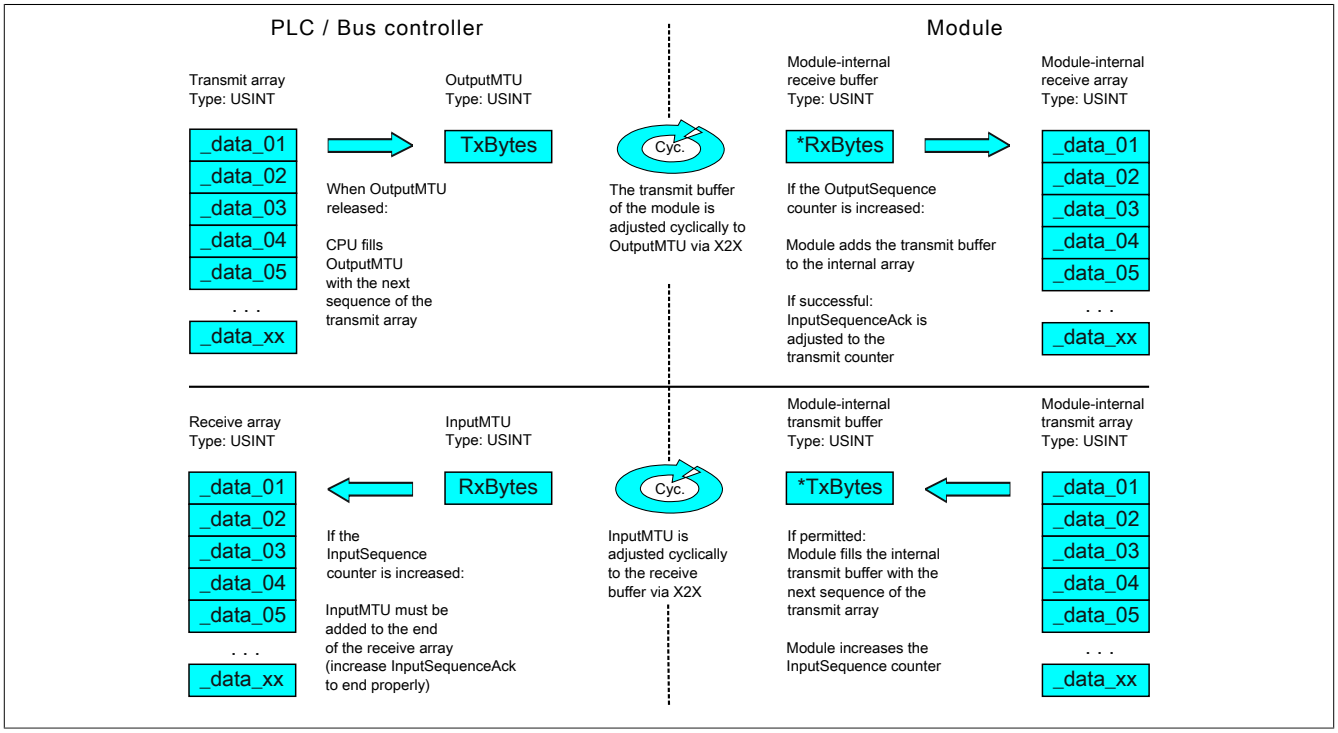


Figure 63: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.3.7.10.8.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

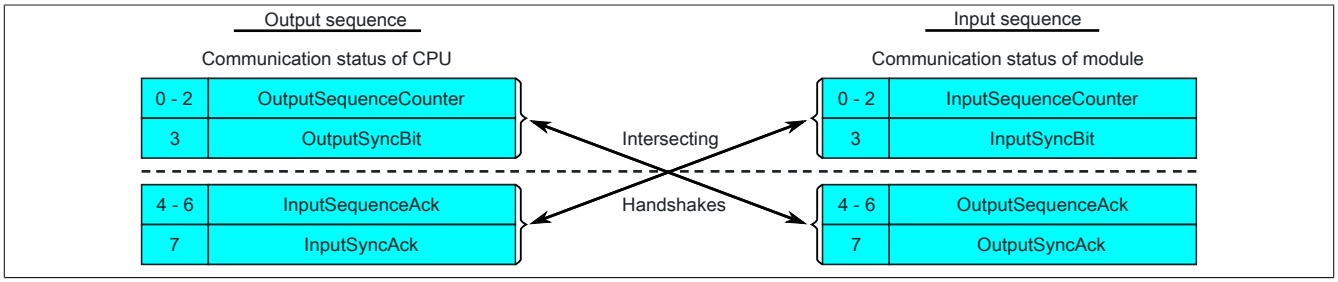


Figure 64: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

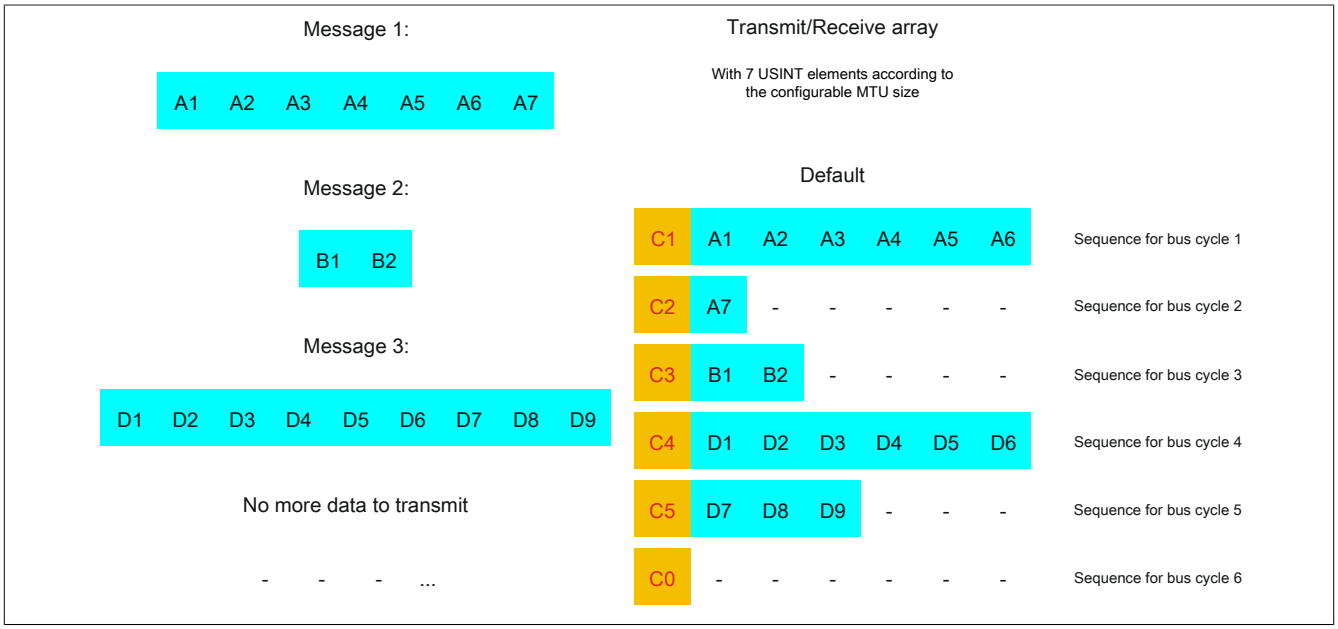


Figure 65: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 36: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 37: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

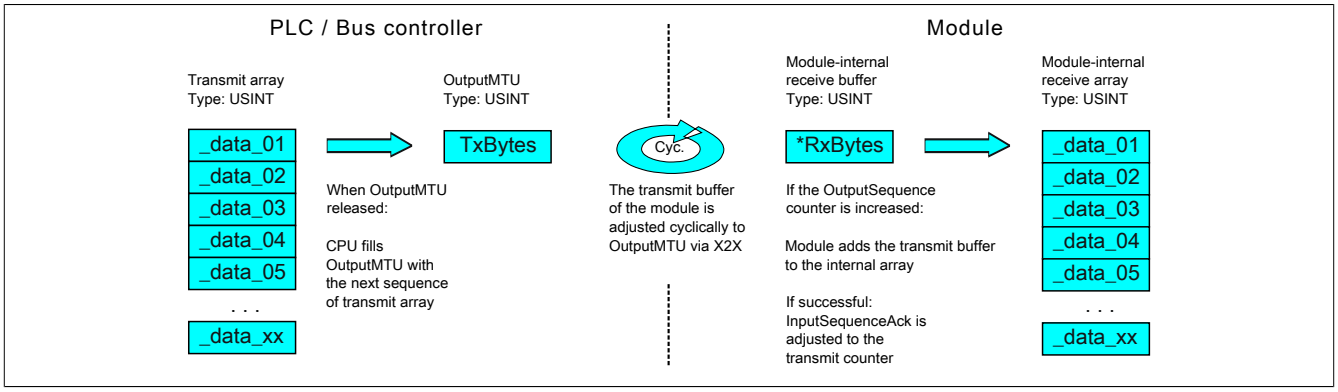


Figure 66: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

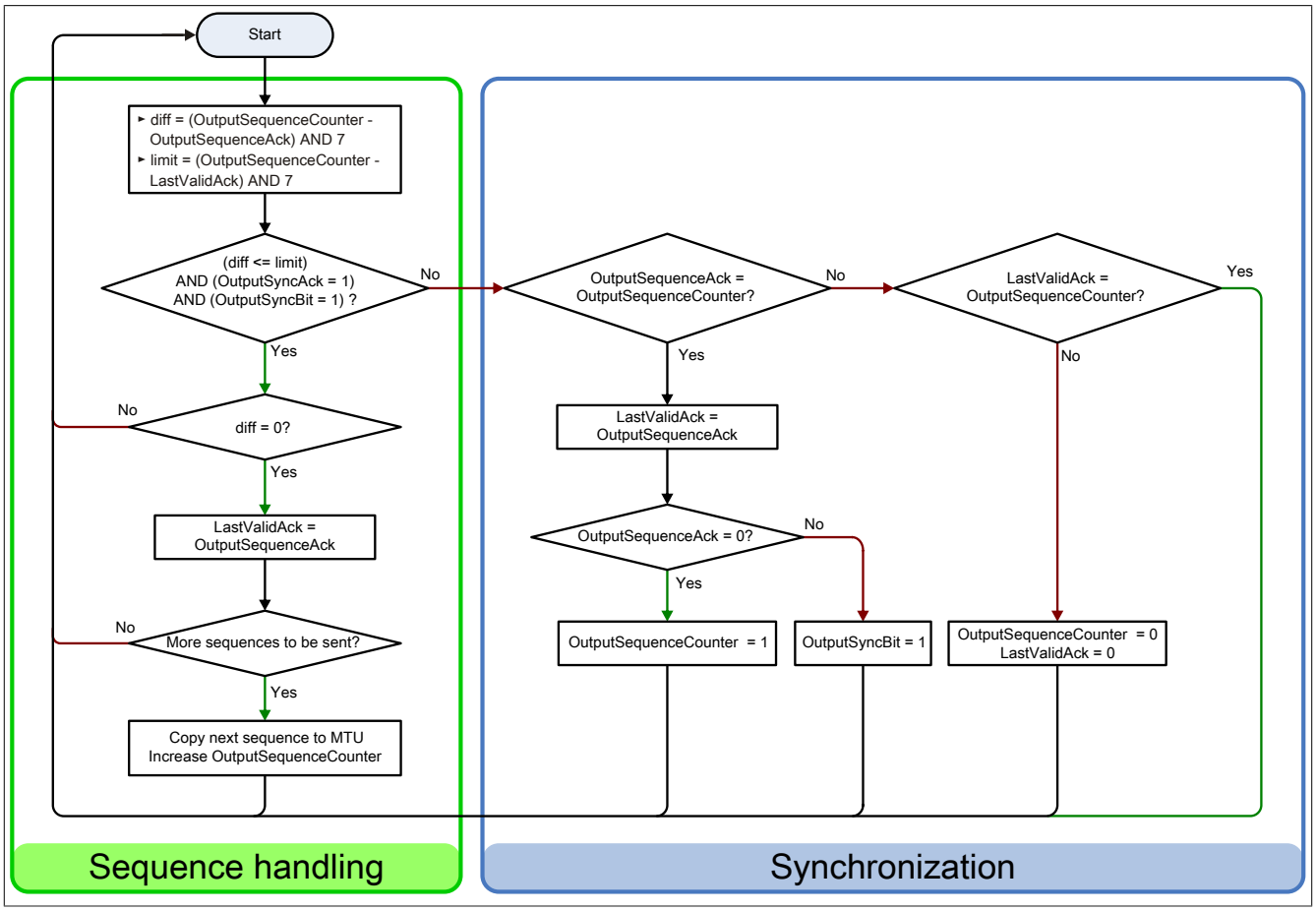


Figure 67: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

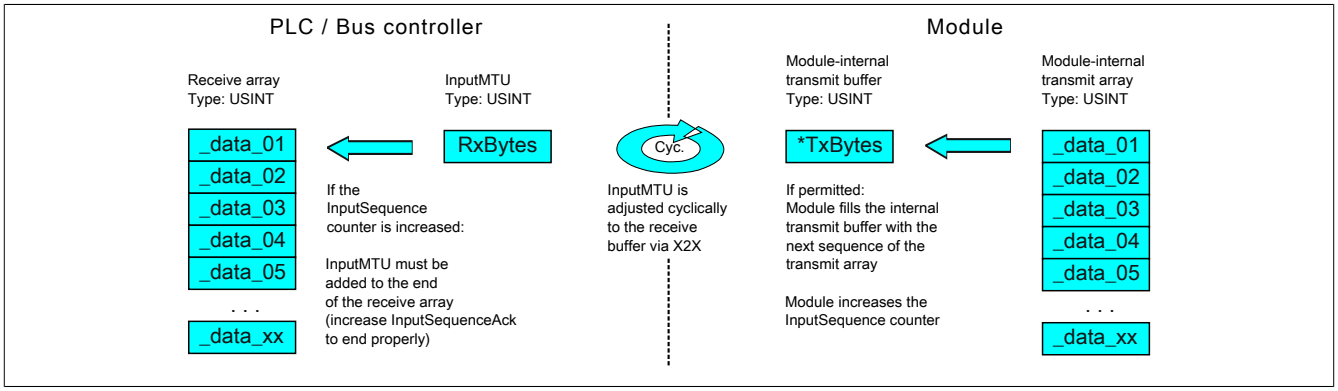


Figure 68: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

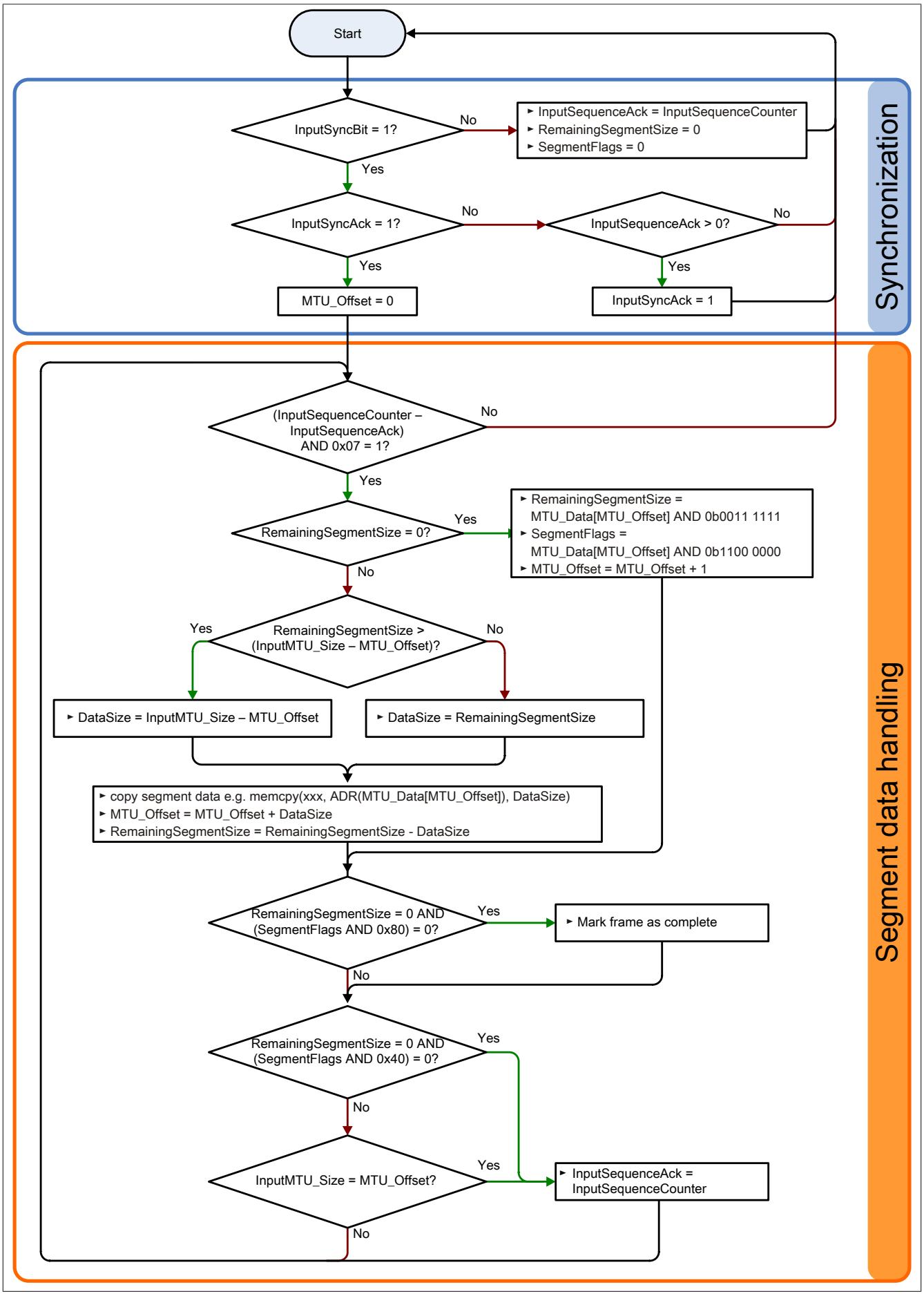


Figure 69: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

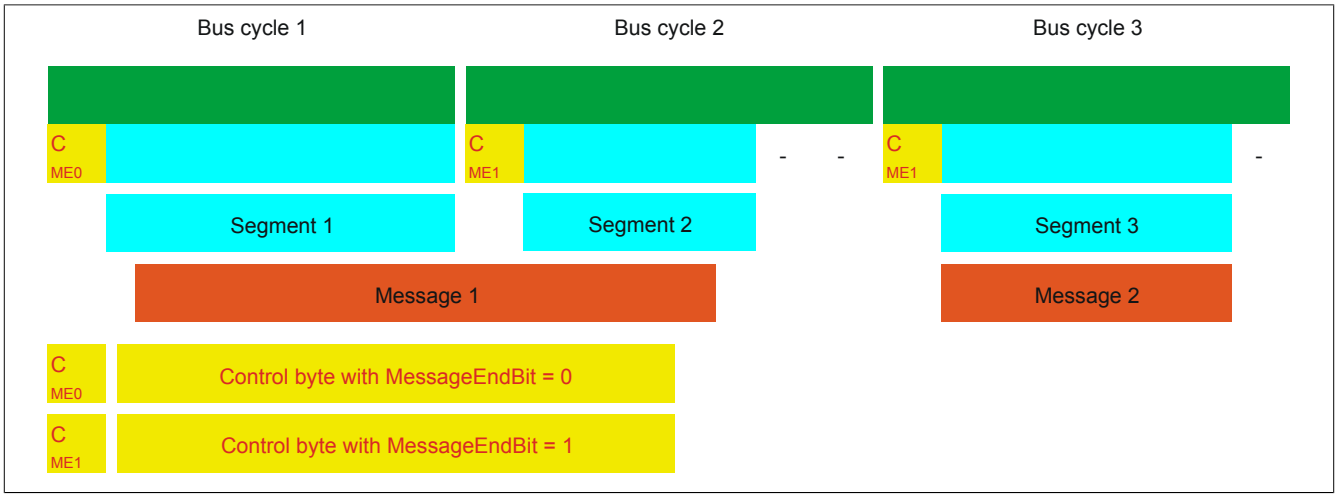


Figure 70: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

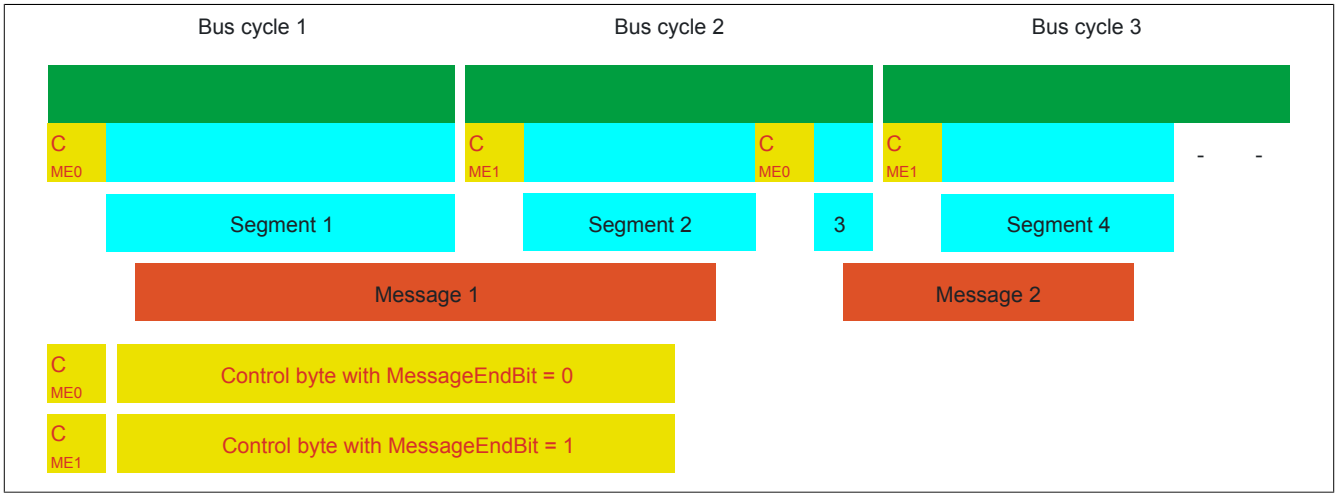


Figure 71: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

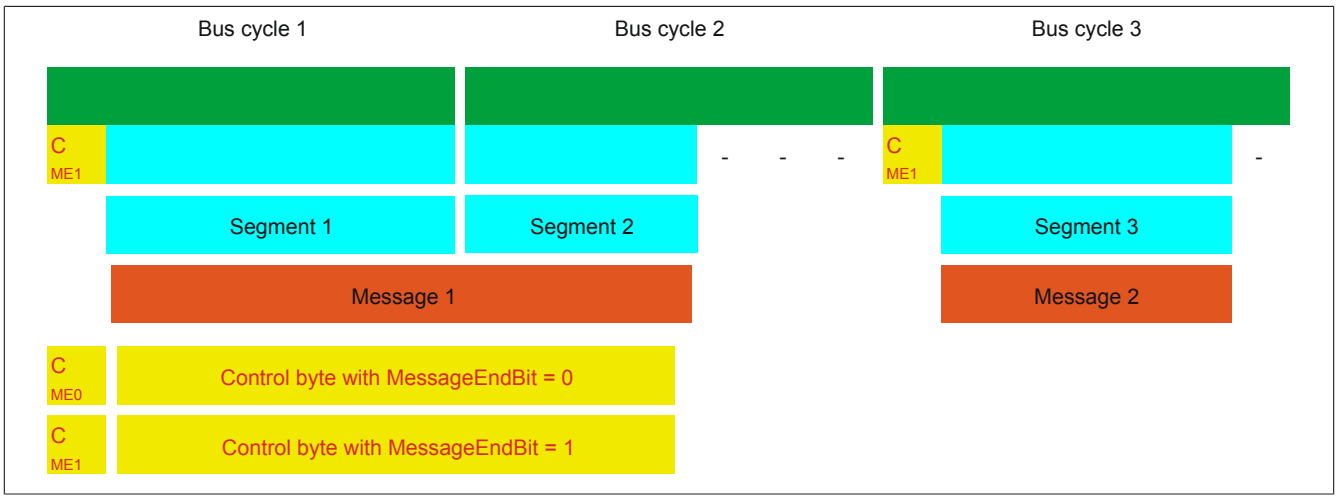


Figure 72: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

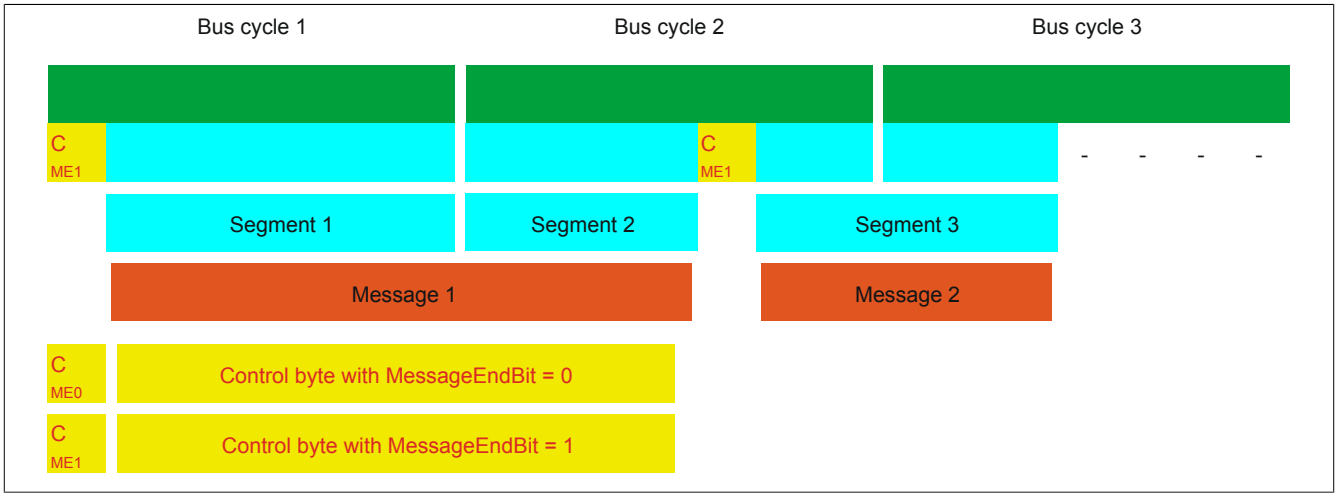


Figure 73: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

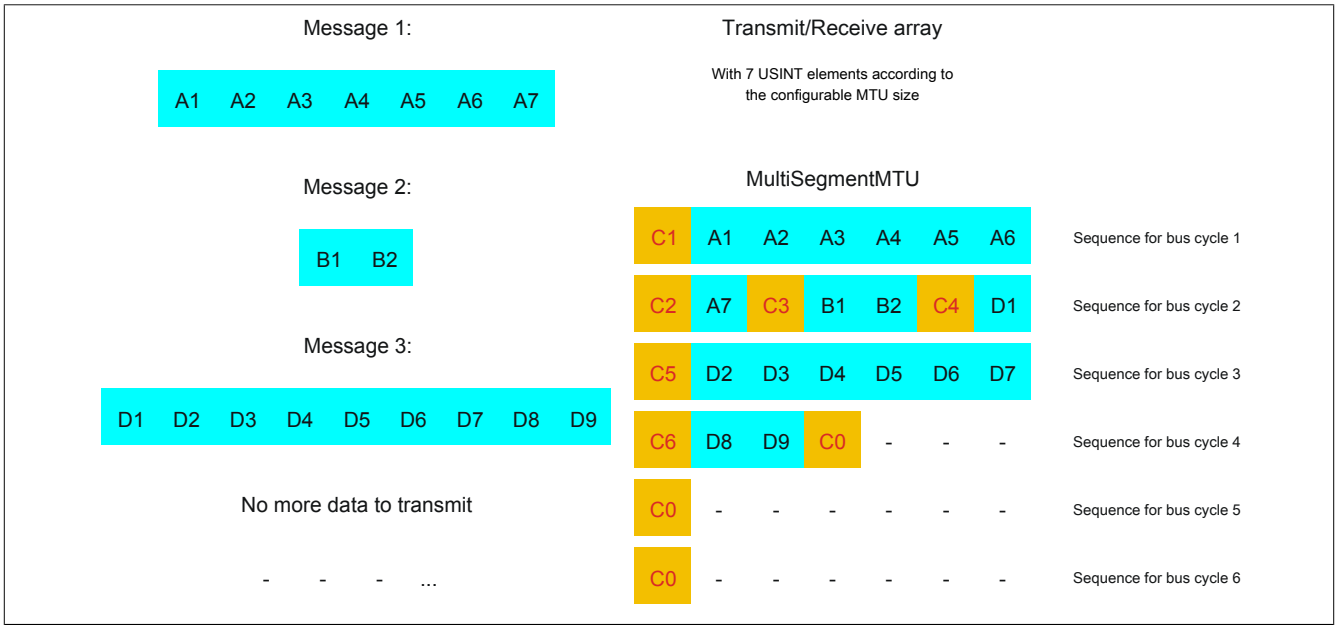


Figure 74: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 38: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 39: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

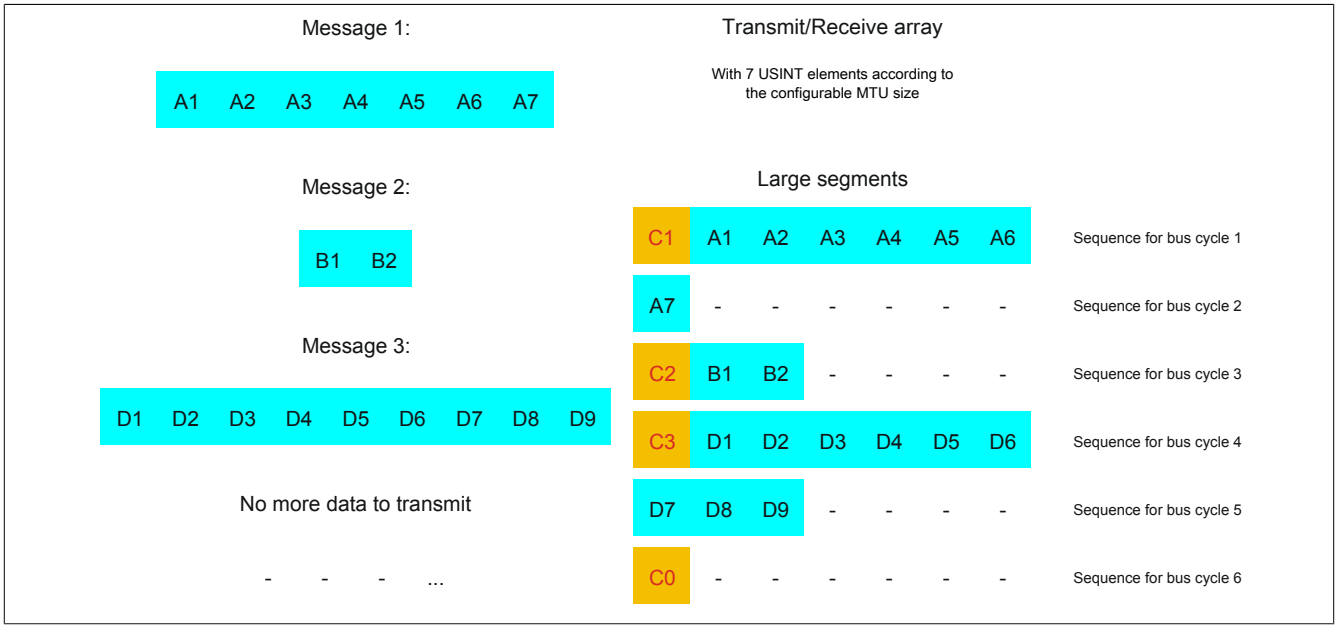


Figure 75: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 40: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

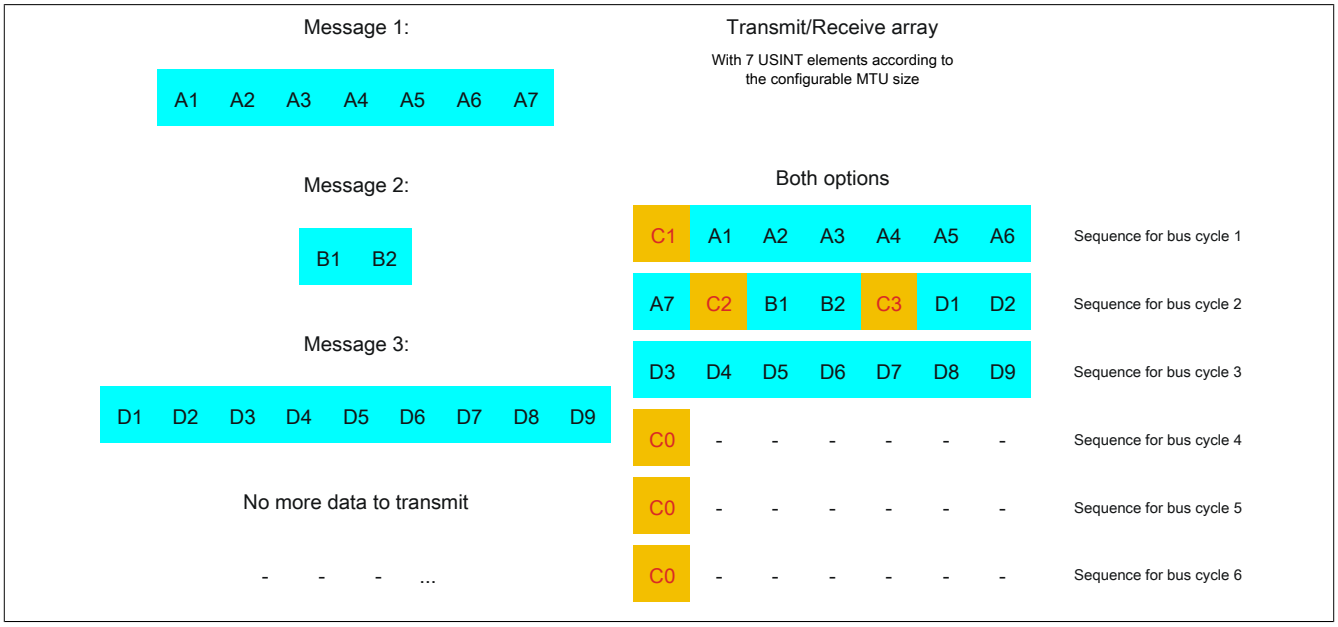


Figure 76: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 41: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.3.7.10.8.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

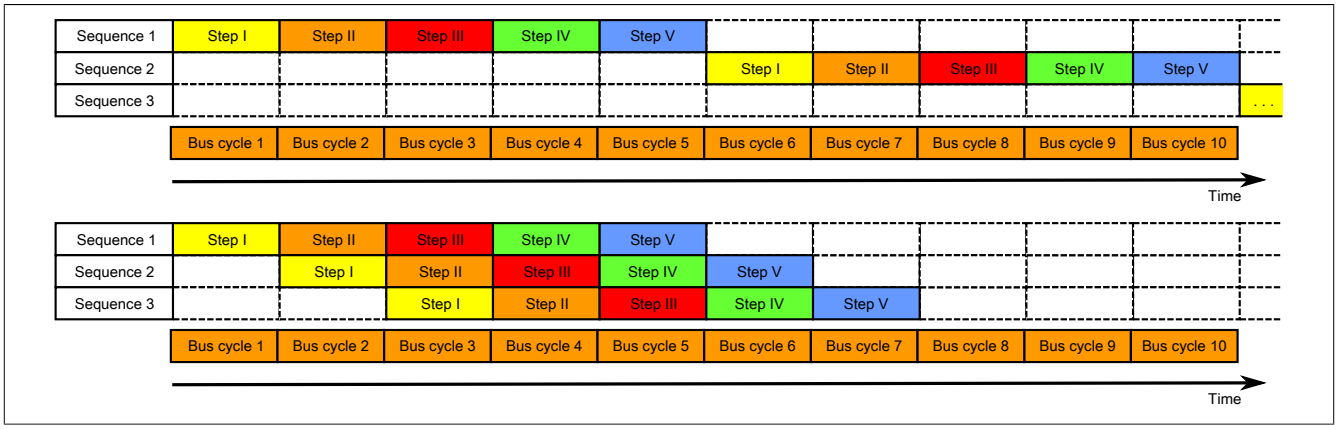


Figure 77: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

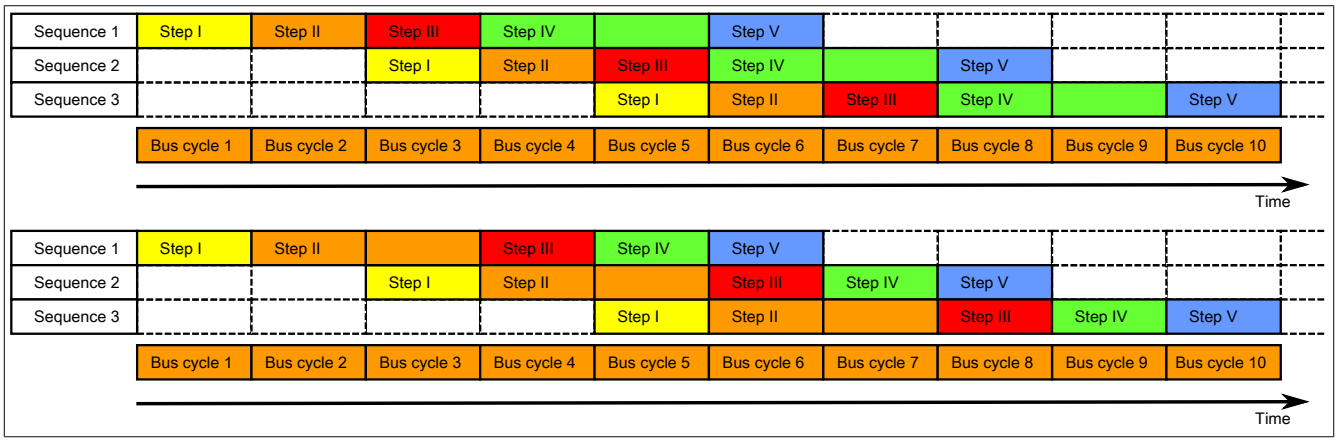


Figure 78: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

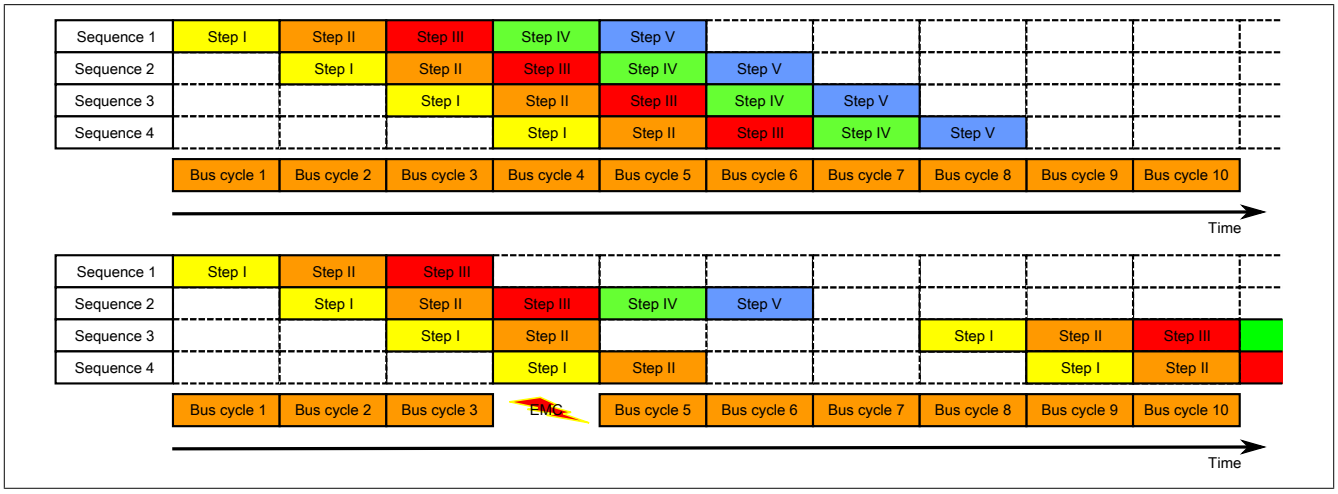


Figure 79: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.3.7.10.9 HART with Flatstream

When using Flatstream communication, the module acts as a bridge between the X2X master and an intelligent field device connected to the module. Flatstream mode can be used for either point-to-point connections as well as for multidrop systems. Specific algorithms such as timeout and checksum monitoring are usually managed automatically. During normal operation, the user does not have access to these details.

HART is considered a master-slave network where half-duplex communication takes place asynchronously. Various features have been included to ensure that signals are transmitted without errors.
For example, the user can increase the length of the preamble, thus making the transmission more secure. However, this also has an effect on the percentage of payload data and overhead.

Additional information about HART can be found at www.HARTcomm.org.

How it works

The module has two independent channels. When using Flatstream , the channel number must therefore be specified. The general structure of a Flatstream frame is extended as follows.

Input/Output sequence	Tx/Rx bytes		
(unchanged)	Control byte (unchanged)	Channel number	HART frame (without preamble and checksum)

HART frame with Flatstream					
Startup	ADDR	CMD	BCNT	(STS)	(DATA)

Startup	Start identification
ADDR	Address within the HART network
CMD	HART command
BCNT	Byte counters (number of remaining bytes)
*STS	Status of the last command received. Information about the working mode of the HART Slave and communication errors (if supported, return data from the HART Slave)
*DATA	Data (if necessary for the command)

Examples of HART commands

Command	Function
0x00	Read slave ID
0x03	Read current value and up to four variables
0x09	Read up to four variables including status
0x21	Read variables

4.3.7.10.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.3.7.10.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Analog inputs	1 ms

Minimum I/O update time for HART communication	
Point-to-point	500 ms
Multidrop	Number of stations * 1000 ms

4.3.8 X20AI2622

4.3.8.1 General information

The module is equipped with 2 inputs with 13-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs
- Either current or voltage signal possible
- 13-bit digital converter resolution

4.3.8.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2622	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 42: X20AI2622 - Order data

4.3.8.3 Technical data

Product ID	X20AI2622
Short description	
I/O module	2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA
General information	
B&R ID code	0x1B9E
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	0.8 W [1]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±12-bit
Current	12-bit
Conversion time	300 µs for all inputs
Output format	
Data type	INT
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permitted input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of the digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Voltage	
Gain	0.08% [3]
Offset	0.015% [4]
Current	
Gain	0 to 20 mA = 0.08 % / 4 to 20 mA = 0.1 % [3]
Offset	0 to 20 mA = 0.03 % / 4 to 20 mA = 0.16 % [5]
Max. gain drift	
Voltage	0.006 %/°C [3]
Current	0 to 20 mA = 0.009 %/°C 4 to 20 mA = 0.0113 %/°C [3]
Max. offset drift	
Voltage	0.002 %/°C [4]
Current	0 to 20 mA = 0.004 %/°C 4 to 20 mA = 0.005 %/°C [5]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB
Nonlinearity	
Voltage	<0.025% [4]
Current	<0.05% [5]

Table 43: X20AI2622 - Technical data

Product ID	X20AI2622
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 43: X20AI2622 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 20 V measurement range.
5) Based on the 20 mA measurement range.

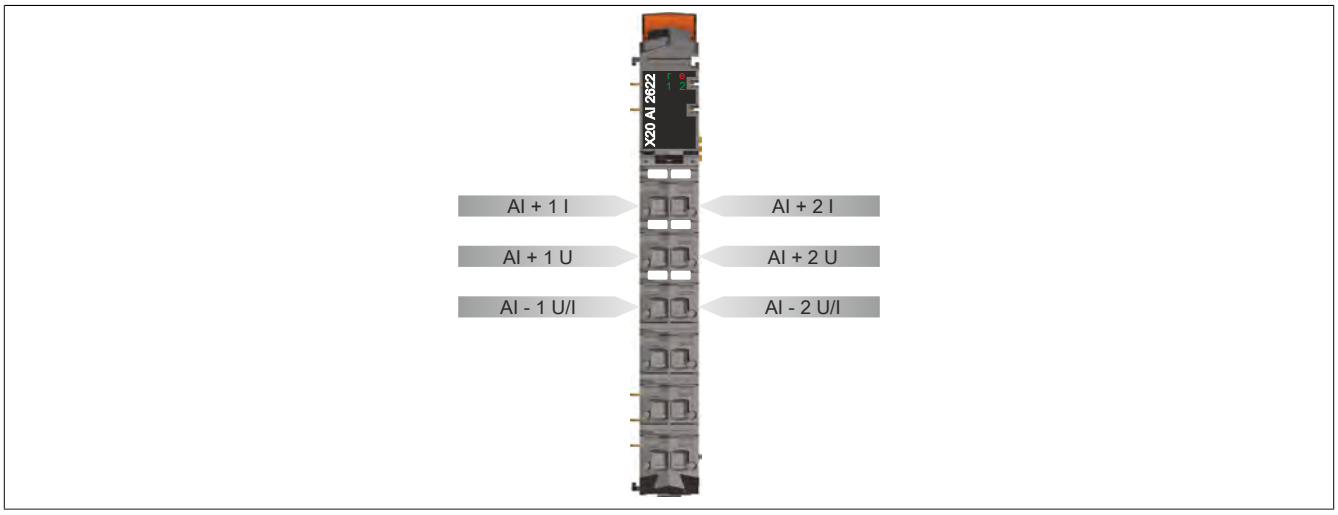
4.3.8.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

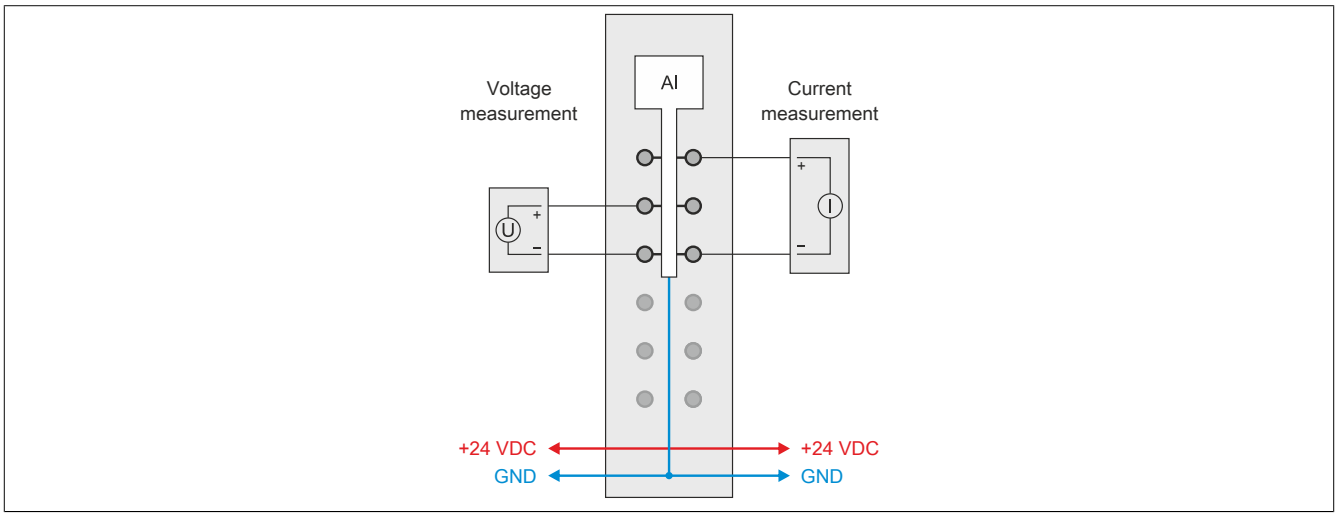
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	Open line[1] or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Open line detection only possible when measuring voltage.

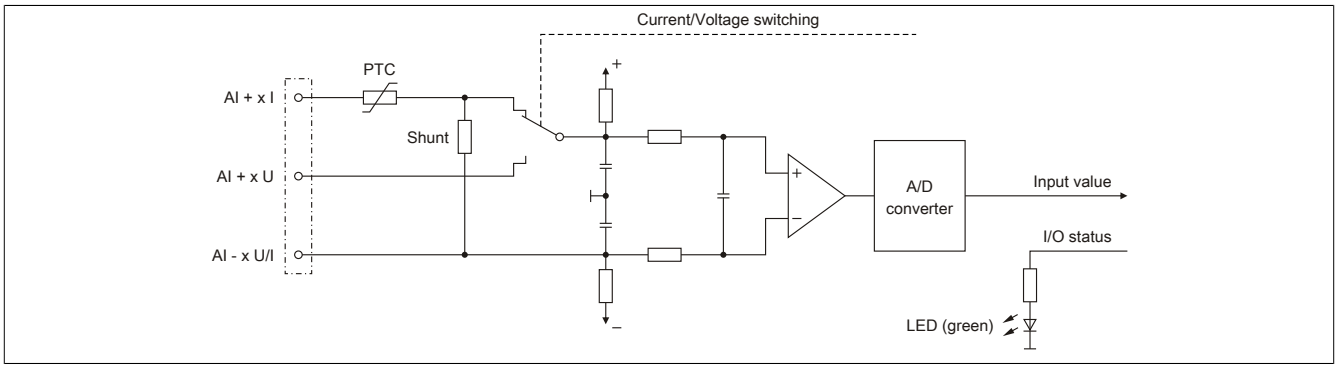
4.3.8.5 Pinout



4.3.8.6 Connection example



4.3.8.7 Input circuit diagram



4.3.8.8 Register description

4.3.8.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.8.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigOutput01	USINT				•
18	ConfigOutput02	USINT				•
20	ConfigOutput03	INT				•
22	ConfigOutput04	INT				•
Communication						
0	AnalogInput01	INT	•			
2	AnalogInput02	INT	•			
30	StatusInput01	USINT	•			

4.3.8.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigOutput01	USINT				•
18	-	ConfigOutput02	USINT				•
20	-	ConfigOutput03	INT				•
22	-	ConfigOutput04	INT				•
Communication							
0	0	AnalogInput01	INT	•			
2	2	AnalogInput02	INT	•			
30	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

4.3.8.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.8.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

4.3.8.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput02

The analog input value are mapped to this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA

4.3.8.8.6 Input filter

This module is equipped with a configurable input filter. The minimum X2X cycle time must be >500 µs. Filtering is disabled for shorter X2X cycle times.

If the input filter is active, then the channels are scanned in 1 ms cycles. The time offset between the channels is 200 µs. Conversion is performed acyclically to the X2X cycle.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

4.3.8.8.6.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

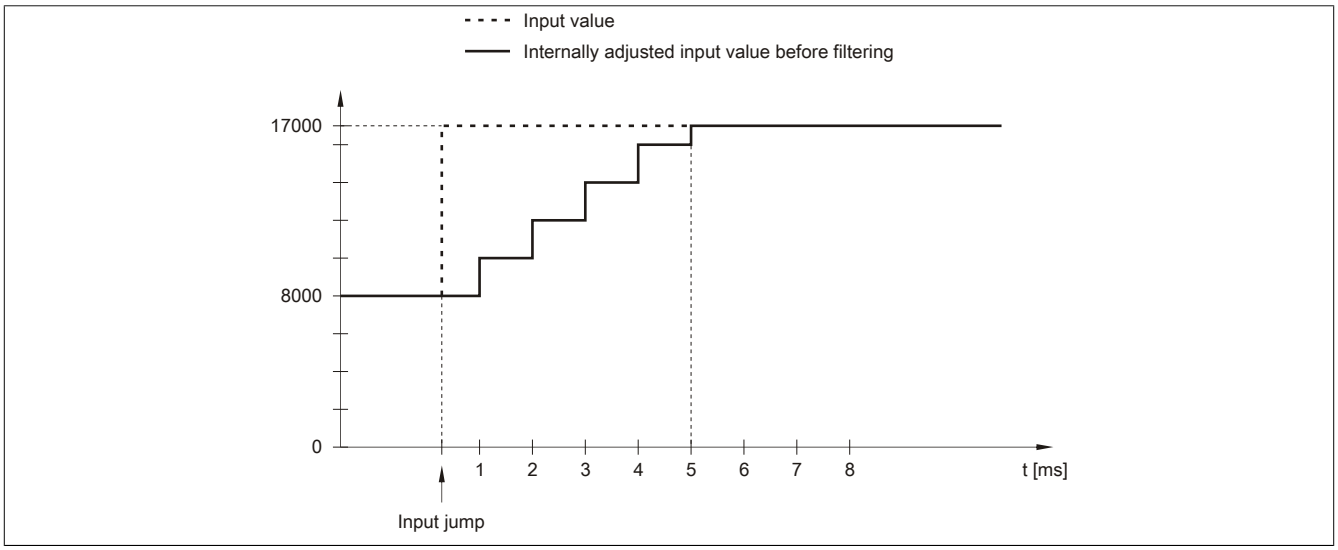


Figure 80: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

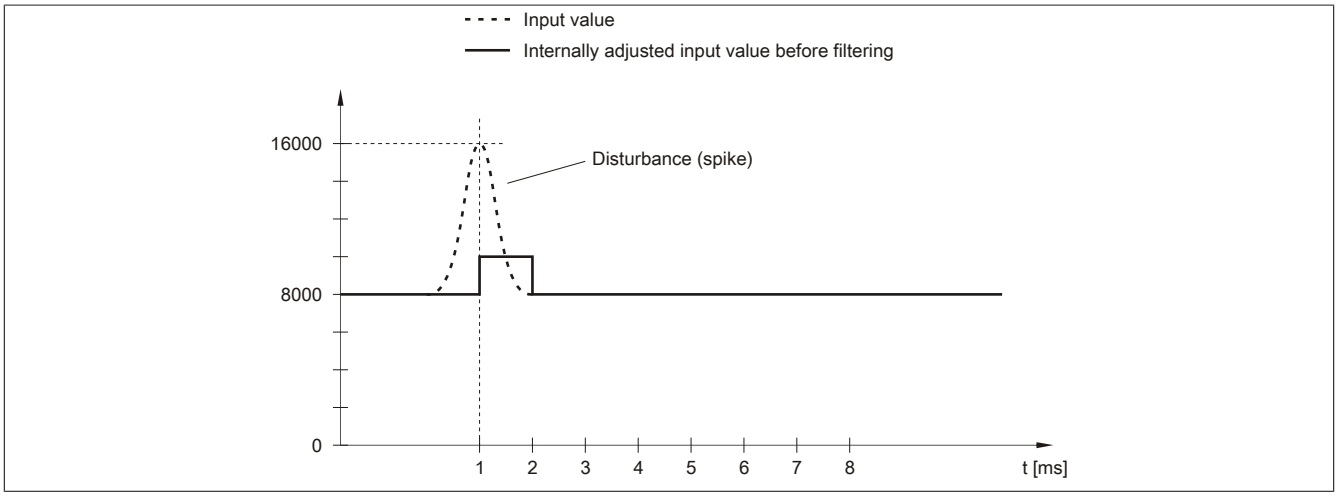


Figure 81: Adjusted input value for disturbance

4.3.8.8.6.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

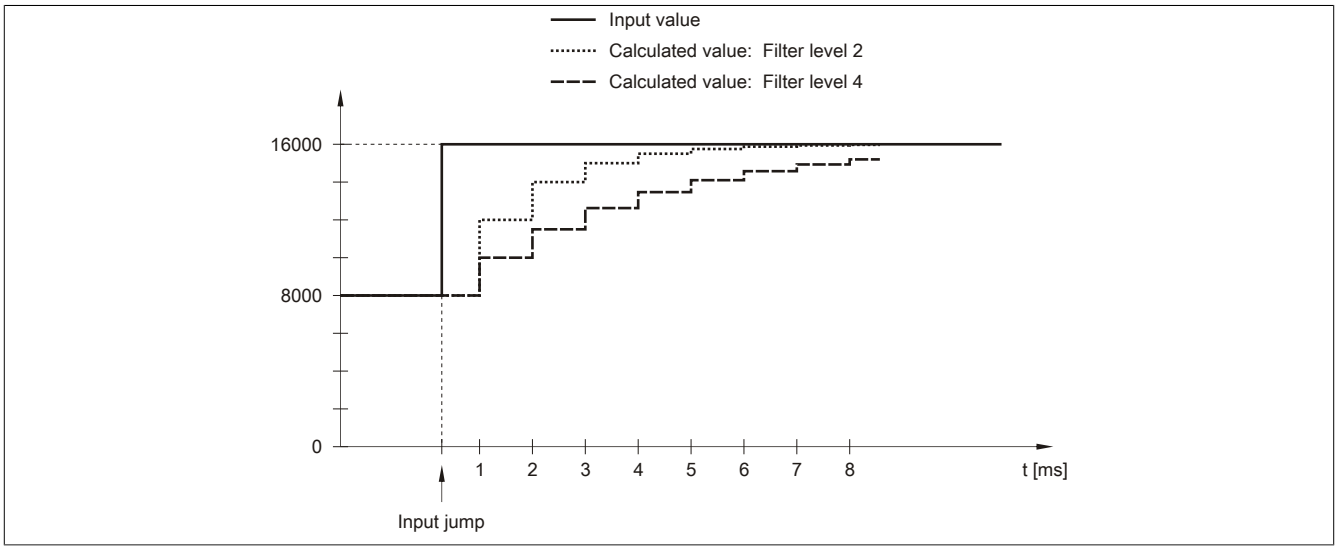


Figure 82: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

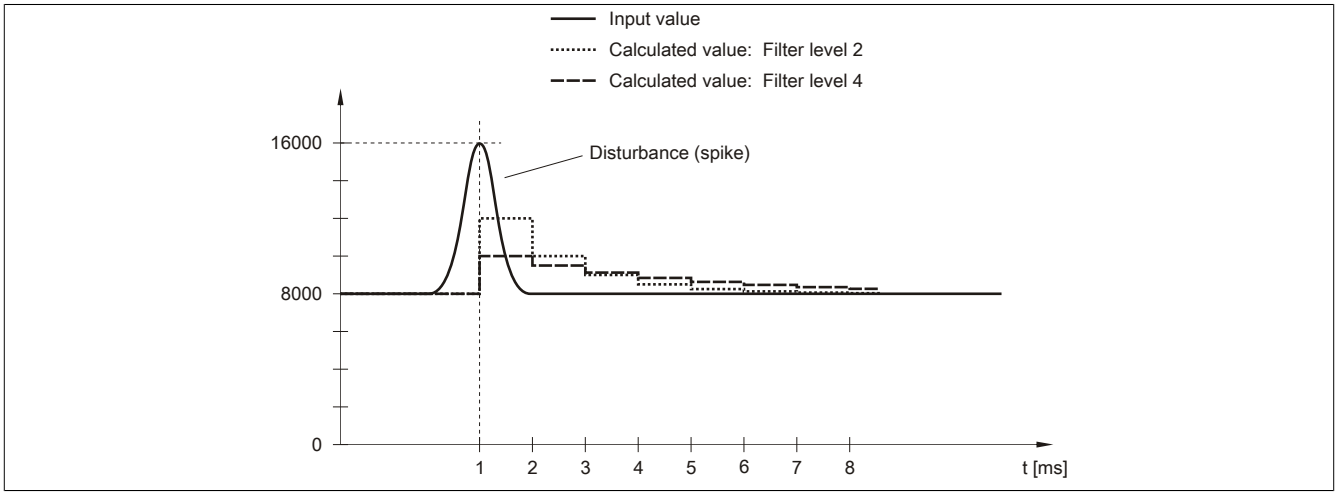


Figure 83: Calculated value during disturbance

4.3.8.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

4.3.8.8.8 Channel type

Name:
ConfigOutput02

This register can be used to define the type and range of signal measurement.

Each channel is capable of handling either current or voltage signals. This differentiation is made using multiple connection terminal points and an integrated switch in the module. The switch is automatically activated by the module depending on the specified configuration. The following input signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 4
1	Channel 2	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 5
2 - 3	Reserved	0	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
6 - 7	Reserved	0	

4.3.8.8.9 Limit values

The input signal is monitored at the upper and lower limit values. These must be defined according to the operating mode:

Limit value (default)	Voltage signal ±10 V		Current signal 0 to 20 mA		Current signal 4 to 20 mA	
Upper maximum limit value	+10 V	+32767 (0x7FFF)	20 mA	+32767 (0x7FFF)	20 mA	+32767 (0x7FFF)
Lower minimum limit value	-10 V	-32767 (0x8001)	0 mA	0[1)]	4 mA	0[2)]

1) The analog value is limited down to 0.
2) The analog value is limited down to 0 at currents <4 mA. The status bit for the lower limit is set.

Other limit values can be defined if necessary. Limit values are valid for all channels and activated automatically by writing to the limit value registers. From this point on, the analog values will be monitored and limited according to the new limits. The results of monitoring are displayed in the status register.

Examples of limit value settings

Application case	Limit value settings
Current signal: 4 to 20 mA	A negative limit value must be configured in order to measure values <4 mA with a current signal of 4 to 20 mA: 0 mA is equal to a value of -8192 (0xE000).
Mixed voltage and current signal	The configured limit values are valid for all channels. Mixed operation (voltage and current signal) therefore requires a compromise. The following configuration has proven effective: Upper limit = +32767, lower limit = -32767 This makes it possible to also measure negative voltage values. A lower limit value of 0 would limit the voltage value to 0.
Current signal on all channels	All channels are configured for measuring current. The limit value setting in Automation Studio is not adjusted automatically. That means that +32767 is configured as the upper limit value and -32767 as the lower limit value. The necessary changes must be made by the user, e.g. lower limit value = 0

4.3.8.8.9.1 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

- **The default value of -32768 corresponds to the minimum default value of -10 VDC.**
- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Information:

Keep in mind that this setting applies to all channels!

4.3.8.8.9.2 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of 32767 corresponds to the maximum default value of 20 mA or +10 VDC.

Information:

Keep in mind that this setting applies to all channels!

4.3.8.8.10 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message. The following states are monitored depending on the settings:

Value	Voltage signal ±10 V	Current signal 0 to 20 mA	Current signal 4 to 20 mA
0	No error	No error	No error
1	Lower limit value exceeded	Default setting The input value has a lower limit of 0x0000. Underflow monitoring is therefore not necessary. After lower limit value change The input value is limited to the configured value. The status bit is set when the lower limit value is passed.	Lower limit value exceeded
2	Upper limit value exceeded	Upper limit value exceeded	Upper limit value exceeded
3	Open line	-	-

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

4.3.8.8.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Inputs without filtering	100 µs
Inputs with filtering	500 µs

4.3.8.8.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Inputs without filtering	300 µs for all inputs
Inputs with filtering	1 ms

4.3.9 X20AI2632

4.3.9.1 General information

The module is equipped with 2 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminal connections.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs
- Either current or voltage signal possible
- 16-bit digital converter resolution
- Simultaneous input conversion
- Very fast conversion time

4.3.9.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2632	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 44: X20AI2632 - Order data

4.3.9.3 Technical data

Product ID	X20AI2632
Short description	
I/O module	2 analog inputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0x1BA0
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W [1]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permitted input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of the digital value during overload	
Below lower limit	
Voltage	0x8001
Current	0x0000
Above upper limit	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - 3rd-order low pass / cutoff frequency 10 kHz
Max. error at 25°C	
Voltage	
Gain	0.08% [2]
Offset	0.01% [3]
Current	
Gain	0.08% [2]
Offset	0.02% [4]
Max. gain drift	
Voltage	0.01 %/°C [2]
Current	0.01 %/°C [2]
Max. offset drift	
Voltage	0.001 %/°C [3]
Current	0.002 %/°C [4]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB

Table 45: X20AI2632 - Technical data

Product ID	X20AI2632
Non-linearity	
Voltage	<0.01% 3)
Current	<0.015% 4)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 45: X20AI2632 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

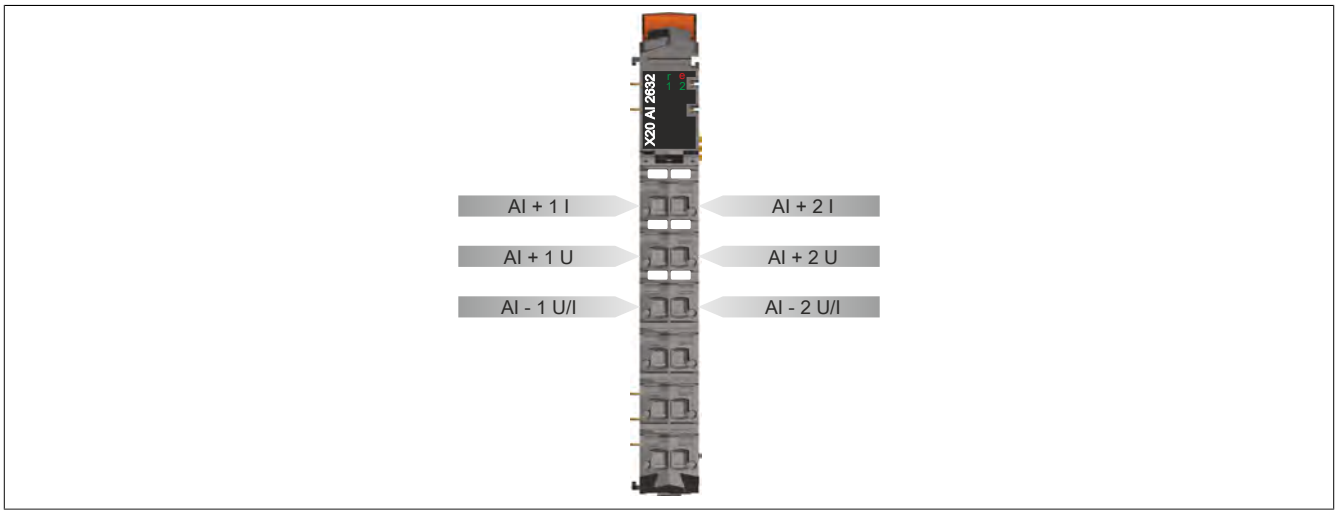
4.3.9.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 2	Green	Off	Open line2) or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

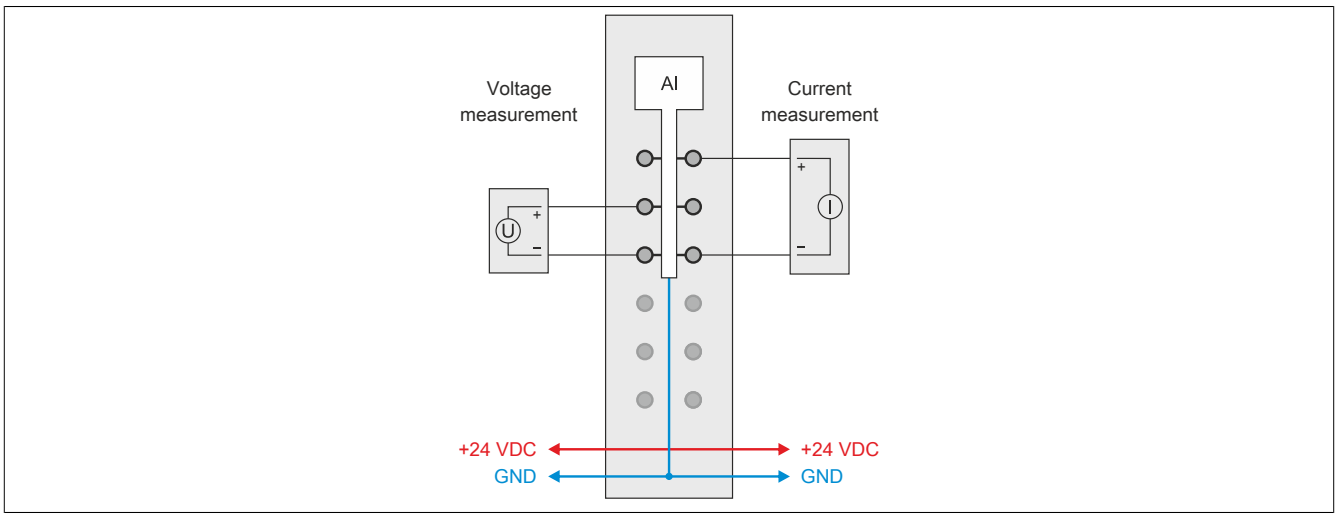
4.3.9.5 Pinout



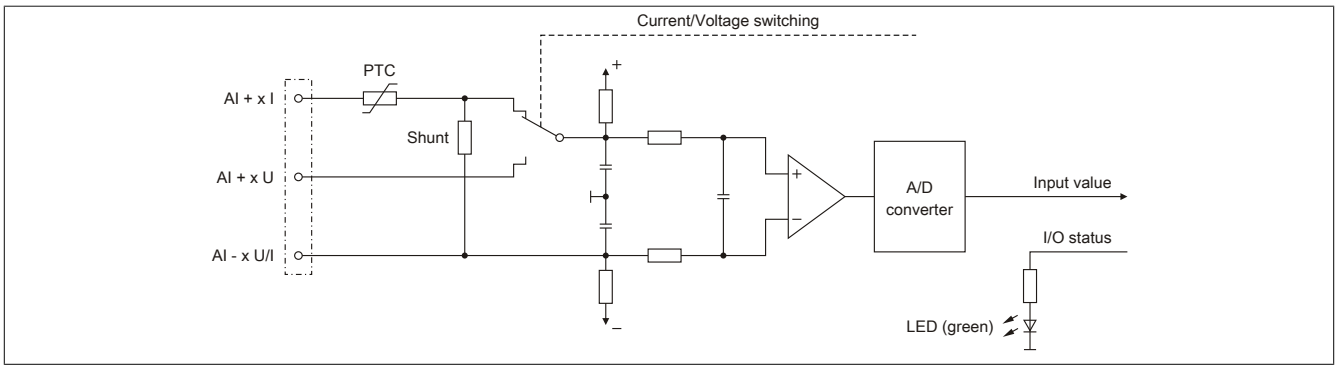
4.3.9.6 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Supply module X20PS9500/X20PS9502
- CPU modules



4.3.9.7 Input circuit diagram



4.3.9.8 Register description

4.3.9.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.9.8.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257	ConfigOutput01 (channel configuration)	USINT				•
289	ConfigOutput06 (channel configuration)	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259	ConfigOutput26 (filter order)	USINT				•
291	ConfigOutput28 (filter order)	USINT				•
262	ConfigOutput27 (filter cutoff frequency)	UINT				•
294	ConfigOutput29 (filter cutoff frequency)	UINT				•
	Scaling					
276	ConfigOutput04 (user-defined gain)	DINT				•
308	ConfigOutput09 (user-defined gain)	DINT				•
284	ConfigOutput05 (user-defined offset)	DINT				•
316	ConfigOutput10 (user-defined offset)	DINT				•
	User-defined limit values					
266	ConfigOutput02 (minimum limit value)	UINT				•
298	ConfigOutput07 (minimum limit value)	UINT				•
270	ConfigOutput03 (maximum limit value)	UINT				•
302	ConfigOutput08 (maximum limit value)	UINT				•
Communication						
0	AnalogInput01	INT	•			
4	AnalogInput02	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	Channel02OK	Bit 1				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	SynchronizationViolationErrorCounter	UINT		•		
2097	Range violation (neg. and pos.)	USINT	•			
	Channel01underflow	Bit 0				
	Channel01overflow	Bit 1				
	Channel02underflow	Bit 4				
	Channel02overflow	Bit 5				
2099	Working range violation (pos.)	USINT	•			
	Channel01outofrange	Bit 0				
	Channel02outofrange	Bit 1				
518	Ch01OutofRange	UINT		•		
550	Ch02OutofRange	UINT		•		
522	Ch01Underflow	UINT		•		
554	Ch02Underflow	UINT		•		
526	Ch01Overflow	UINT		•		
558	Ch02Overflow	UINT		•		
Additional analysis functions						
133	ConfigOutput21 (trigger condition on falling edge)	USINT				•
135	ConfigOutput22 (trigger condition on rising edge)	USINT				•
129	Analysis control byte	USINT			•	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	MinMaxStart02	Bit 5				
129	Analysis status byte	USINT	•			
	MinMaxStart01Readback	Bit 4				
	MinMaxStart02Readback	Bit 5				
	Limit values					
530	MinInput01	INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
562	MinInput02	INT	●			
534	MaxInput01	INT	●			
566	MaxInput02	INT	●			
538	CH01MinMaxLatchCounter	UINT		●		
570	CH02MinMaxLatchCounter	UINT		●		
	Trace configuration					
1026	TraceChannelEnable	USINT				●
1030	TraceSampleDepth	UINT				●
4157	ConfigOutput25 (recording priority)	USINT				●
1037	Starting a recording	USINT			●	
	TraceEnable01	Bit 0				
1089	Recording status	USINT	●			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	●			
1098	TriggerCount	UINT	●			
1102	TriggerFailCount	UINT	●			
	Comparator					
450	cfgComp_LowLimitCh01	INT			(●)	●
458	cfgComp_LowLimitCh02	INT			(●)	●
454	cfgComp_HighLimitCh01	INT			(●)	●
462	cfgComp_HighLimitCh02	INT			(●)	●
662	CompStateCollection	UINT	●			
490	cfgComp_NominalState	UINT				●
482	cfgComp_EnableMask	UINT				●
486	cfgComp_ConditionTypeMask	UINT				●
	Time-offset trace					
1042	TraceTriggerStart	INT				●
1046	TraceTriggerStop	UINT				●

4.3.9.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257	-	ConfigOutput01 (channel configuration)	USINT				●
289	-	ConfigOutput06 (channel configuration)	USINT				●
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				●
	Filtering						
259	-	ConfigOutput26 (filter order)	USINT				●
291	-	ConfigOutput28 (filter order)	USINT				●
262	-	ConfigOutput27 (filter cutoff frequency)	UINT				●
294	-	ConfigOutput29 (filter cutoff frequency)	UINT				●
	Scaling						
276	-	ConfigOutput04 (user-defined gain)	DINT				●
308	-	ConfigOutput09 (user-defined gain)	DINT				●
284	-	ConfigOutput05 (user-defined offset)	DINT				●
316	-	ConfigOutput10 (user-defined offset)	DINT				●
	User-defined limit values						
266	-	ConfigOutput02 (minimum limit value)	UINT				●
298	-	ConfigOutput07 (minimum limit value)	UINT				●
270	-	ConfigOutput03 (maximum limit value)	UINT				●
302	-	ConfigOutput08 (maximum limit value)	UINT				●
Communication							
0	0	AnalogInput01	INT	●			
4	2	AnalogInput02	INT	●			
650	-	SampleCycleCounter	UINT		●		
	Error monitoring and counters						
641	-	Channel status	USINT		●		
		Channel01OK	Bit 0				
		Channel02OK	Bit 1				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		●		
658	-	SynchronizationViolationErrorCounter	UINT		●		
2097	-	Range violation (neg. and pos.)	USINT		●		
		Channel01underflow	Bit 0				
		Channel01overflow	Bit 1				
		Channel02underflow	Bit 4				
		Channel02overflow	Bit 5				
2099	-	Working range violation (pos.)	USINT		●		
		Channel01outofrange	Bit 0				
		Channel02outofrange	Bit 1				
518	-	Ch01OutofRange	UINT		●		
550	-	Ch02OutofRange	UINT		●		
522	-	Ch01Underflow	UINT		●		
554	-	Ch02Underflow	UINT		●		
526	-	Ch01Overflow	UINT		●		
558	-	Ch02Overflow	UINT		●		
Additional analysis functions							
133	-	ConfigOutput21 (trigger condition on falling edge)	USINT				●
135	-	ConfigOutput22 (trigger condition on rising edge)	USINT				●
129	-	Analysis control byte	USINT				●
		TraceTrigger01	Bit 0				
		MinMaxStart01	Bit 4				
		MinMaxStart02	Bit 5				
129	-	Analysis status byte	USINT		●		
		MinMaxStart01Readback	Bit 4				
		MinMaxStart02Readback	Bit 5				
	Limit values						
530	-	MinInput01	INT		●		
562	-	MinInput02	INT		●		
534	-	MaxInput01	INT		●		
566	-	MaxInput02	INT		●		
538	-	CH01MinMaxLatchCounter	UINT		●		
570	-	CH02MinMaxLatchCounter	UINT		●		

1) The offset specifies the position of the register within the CAN object.

4.3.9.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.9.8.4 Configuration

This module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately from one another either on the voltage or current input for the following areas:

- Permitted voltage: ±10 V
- Permitted current: 0 to 20 mA

4.3.9.8.4.1 Channel configuration

Name:
ConfigOutput01 for channel 01
ConfigOutput06 for channel 02

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using the correct terminal block pins.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±10 VDC
		1	Current terminal for 0 to 20 mA
1	Gain selector	0	Voltage ±10 VDC
		1	Current 0 to 20 mA
2 - 3	Reserved	-	
4	Filtering active	0	Inactive
		1	Active
5	Minimum/Maximum analysis active	0	Inactive
		1	Active
6	Error monitoring active	0	Inactive
		1	Active
7	Enables channel	0	Channel enabled
		1	Channel disabled

4.3.9.8.4.2 Sampling and conversion

The analog signal is sampled in 2 steps.

- **Conversion task**
  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.
  The timespan needed for conversion results from the set sampling time.
- **Processing task**
  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Function
UINT	50 to 10,000	Default value = 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

4.3.9.8.4.3 Filtering (optional)

If filtering is enabled in the 4.3.9.8.4.1 "Channel configuration" register, the basic data of the A/D converter is filtered per channel. The following registers are available to specify the filter order and respective cutoff frequency for configuring the low-pass filter:

- "Filter order"
- "Filter cutoff frequency"

Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2

The filter order is specified in this register. The "Filter cutoff frequency" register is used to configure the respective cutoff frequency of the filter.

Data type	Value
USINT	1 to 4

Internal filter orders greater than 1 are implemented as cascaded first-order filters. Since the filter is calculated in the sampling cycle, the filter characteristics are directly related to the settings for the sampling cycle time.

Calculating the cutoff frequency of an nth-order filter:

yn = a * xn + b * y(n-1)

Approximate calculation

a = Sampling time / (Sampling time + 1/Cutoff frequency)

b = 1 - a

Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Description
UINT	1 to 65,535	Cutoff frequency in hertz

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

4.3.9.8.4.4 Scaling (optional)

Scaling A/D converter data is an option for the user. The following registers are available for this:

- "User-defined gain" (= ku)
- "User-defined offset" (= du)

Scaling calculation:

Scaled value = k * A/C value + d

Gain $k = k_{Calibration} * ku$

Offset $d = d_{Calibration} + du$

The value has to be limited since it can exceed the 16-bit constraints. To provide the greatest degree of flexibility, limiting is possible using the registers "Minimum limit value" and "Maximum limit value".

User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65,536 (0x10000) corresponds to a gain of 1.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65,536 (0x10000) corresponds to an offset of 1.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.3.9.8.4.5 User-defined limit values

If the application requires a limitation of the range of values, then the user can define his own limit values. These values will also be use for the module's error statistics. The following registers are available for this:

- "Minimum limit value"
- "Maximum limit value"

Information:

32-bit numbers are used inside the module. A limit value violation can therefore also be determined if the permitted range of values was defined from -32768 to 32767.

Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2

The minimum limit value is configured in this register. This limit value is also used as the lower value in the error statistics (see register "Counter for range exceeded violations (neg.)").

Data type	Value
INT	-32768 to 32767

Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2

The maximum limit value is configured in this register. This limit value is also used as the upper value in the error statistics (see register "Counter for range exceeded violations (pos.)").

Data type	Value
INT	-32768 to 32767

4.3.9.8.5 Communication - General

The module's analog inputs convert current and voltage values with 16-bit resolution. This information can be used by the application with the help of the registers listed here.

4.3.9.8.5.1 Analog inputs

Name:
AnalogInput01 to AnalogInput02

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

4.3.9.8.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Value
UINT	0 to 65535

4.3.9.8.5.3 Error monitoring and counters

Channel status

Name:
Channel01OK to Channel02OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors
1	Channel02OK	0	OK
		1	Errors
2 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "Synchronization error counter".
2) Identical to bit 0 of the registers "Counter for faulty sampling cycles".

Synchronization error counter

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See 4.3.9.8.4.2 "Sampling and conversion".

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Range violation (neg. and pos.)

Name:
Channel01underflow to Channel02underflow
Channel01overflow to Channel02overflow

This register indicates whether a range violation (pos. and/or neg.) of the limit values defined in the registers "Minimum limit value" and "Maximum limit value" has occurred. The individual bits in this register are identical to the values of the lowest bits in the registers "Counter for range exceeded violations (neg.)" and "Counter for range exceeded violations (pos.)".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
1	Channel02underflow	0	No error
		1	Range exceeded (.neg) on channel 2
2 - 3	Reserved	-	
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
5	Channel02overflow	0	No error
		1	Range exceeded (.pos) on channel 2
6 - 7	Reserved	-	

Working range violation (pos.)

Name:
Channel01OutofRange to Channel02OutofRange

This register indicates whether the input value exceeds the module's maximum measurement range. The individual bits in this register are identical to the values of the lowest bits in the register "Counter for work range violations (pos.)".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutofRange	0	No error
		1	Working range violation (pos.) of channel 1
1	Channel02OutofRange	0	No error
		1	Working range violation (pos.) of channel 2
2 - 7	Reserved	-	

Counter for work range violations (pos.)

Name:
CH01OutofRange to CH02OutofRange

Errors outside of the module's maximum possible measurement range are indicated in this register. These errors lead to full-scale deflection of the A/D converter.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.9.8.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (neg.)

Name:
CH01Underflow to CH02Underflow

This register indicates range exceeded violations (neg.) of the value configured in the register "Minimum limit value".

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.9.8.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (pos.)

Name:
CH01Overflow to CH02Overflow

This register indicates range exceeded violations (pos.) of the value configured in the register "Maximum limit value".

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.9.8.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

4.3.9.8.6 Additional analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

- **Limit value analysis**
  If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched internally in the module. A measurement period can be triggered using the control byte. When the respective configured edge is generated by the application, the limit values from the previous measurement period are displayed and the internal latch register is reset.
- **Recording sampled values**
  If recording sampled values has been enabled for a channel, then the sampled values are additionally recorded in the module's internal FIFO memory. If the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

It is only possible to use the recording of sampled values if the module is operated on an X2X master that is an SG4 CPU.

4.3.9.8.6.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register configures whether the falling edge is used to trigger the trace and determination of the input value in the register 4.3.9.8.6.3 "Analysis control byte".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination
		1	Falling edge determines input value of channel 1
5	MinMaxStart02	0	No determination
		1	Falling edge determines input value of channel 2
6 - 7	Reserved	0	

4.3.9.8.6.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register configures whether the rising edge is used to trigger the trace and determination of the input value in the register 4.3.9.8.6.3 "Analysis control byte".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Rising edge does not initiate trigger
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination
		1	Rising edge determines input value of channel 1
5	MinMaxStart02	0	No determination
		1	Rising edge determines input value of channel 2
6 - 7	Reserved	0	

4.3.9.8.6.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart02

The trace function and determination of the minimum/maximum input values can be started in this register.
Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers 4.3.9.8.6.1 "Trigger condition on falling edge" and 4.3.9.8.6.2 "Trigger condition on rising edge".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Does not initiate trigger/trace
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not initiated
		1	Initiates determination of input value of channel 1
5	MinMaxStart02	0	Determination not initiated
		1	Initiates determination of input value of channel 2
6 - 7	Reserved	-	

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

4.3.9.8.6.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart02Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel
5	MinMaxStart02Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel
6 - 7	Reserved	-	

4.3.9.8.7 Limit values

Limit value analysis must be enabled for the desired channel. See 4.3.9.8.4.1 "Channel configuration". The sampled value of the channel is then compared to the minimum and maximum values that are stored internally in the module. If a new measurement period is initiated with the 4.3.9.8.6.3 "Analysis control byte" register, then the values of the previous measurement period can be read from the respective registers intended for this.

4.3.9.8.7.1 Minimum input values

Name:
MinInput01 to MinInput02

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

4.3.9.8.7.2 Maximum input values

Name:
MaxInput01 to MaxInput02

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

4.3.9.8.7.3 Limit value trigger counter

Name:
CH01MinMaxLatchCounter to CH02MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

4.3.9.8.8 Trace

If the module is operated on a SG4 CPU, the digitalized input values are recorded by the module. The module must be operated in "Supervised" mode in order to use the trace function.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism can only be used if the module is connected directly to the CPU, not if it is operated behind a bus controller.

4.3.9.8.8.1 Enable recording

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
1	Channel 2	0	Channel disabled
		1	Channel enabled
2 - 7	Reserved	-	

4.3.9.8.8.2 Number of values to be recorded

Name:
TraceSampleDepth

16 kB are available on the module for the trace. The FIFO memory limitation means that a maximum of 8192 analog values can be recorded. This memory is divided up equally among the enabled channels. The actual number of maximum possible recordings therefore depends on the number of channels enabled for trace:

1 channel enabled: Up to 8192 recordings
2 channels enabled: Up to 4096 recordings per channel

Data type	Value	Function
UINT	2 to 8192	Default value = 1024

4.3.9.8.8.3 Recording priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard (default value)
	6	Trace priority higher than X2X Link communication

4.3.9.8.8.4 Starting a recording

Name:

TraceEnable01

This register starts the recording according to the specifications for edge control or the comparator.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

4.3.9.8.8.5 Recording status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

4.3.9.8.8.6 Free trace buffer

Name:
FreeBufferSize

Specifies the available FIFO memory area in bytes for the trace

Data type	Value
UINT	0 to 65535

4.3.9.8.8.7 Counter for trace triggers

Name:
TriggerCount

The number of trigger events that have occurred since "starting the trace" is indicated in this register.

Data type	Value
UINT	0 to 65535

4.3.9.8.8.8 Counter for faulty recording triggers

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be performed.

Data type	Value
UINT	0 to 65535

4.3.9.8.8.9 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold value bits for all channels are grouped together in the lower-value byte of the "Hysteresis status of the channels" register. In addition, the states of the previous sampling are stored in the higher-value byte.

The 4 status messages of each channel can be linked according to the following logic via a logical connective mask using AND or OR operators and used as a trace trigger:

```
delta = (Current_HysteresisStatus ^ NominalValues) // Different between current status and preset
cond = delta & Selected_HysteresisStatusBits // Eliminate irrelevant status messages
cond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if ((0 == (cond & ~LogicalOperators)) &&
(0 != (~cond & LogicalOperators))) { => Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	cfgComp_EnableMask
Current_HysteresisStatus	CompStateCollection
Nominal values	cfgComp_NominalState
Logical operators	cfgComp_ConditionTypeMask

Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh02

The lower limit value for hysteresis is configured in this register.

Data type	Value
INT	-32768 to 32767

Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh02

The upper limit value for hysteresis is configured in this register.

Data type	Value
INT	-32768 to 32767

Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
12 - 15	Reserved	-	

Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
12 - 15	Reserved	-	

Information:

This is a "whitelist", i.e. the trace starts as soon as the current status message takes on the state predefined here.

One or more matches will be necessary depending on the selection of the relevant hysteresis status bits and logical connective operators.

Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register selects which status bits of the hysteresis comparison should be used to generate the trigger.

For more information about using this register, see 4.3.9.8.8.9 "Comparator for trigger conditions".

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
2	Channel02 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
3	Channel02 InRange status in the current cycle	0	Do not use
		1	Use for generation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
10	Channel02 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
11	Channel02 InRange status in the last cycle	0	Do not use
		1	Use for generation
12 - 15	Reserved	-	

Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

The desired state operators with which the status bits are linked to one another to generate a trigger are selected in this register.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "Selecting the relevant hysteresis status bits" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
2	Channel02 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
3	Channel02 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
10	Channel02 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
11	Channel02 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
12 - 15	Reserved	-	

4.3.9.8.8.10 Time-offset trace

Additional conditions for shifting the starting and stopping points can be defined if the trace should be chronologically offset to the trigger.

Starting the trace

Name:
TraceTriggerStart

The starting position is defined relative to the configured trigger condition in this register. Positive values mean that the trace takes place x samples after the trigger condition. Negative values mean that the trace takes place x samples before the trigger condition.

The value -32768 performs the trace without regard for the configured trigger condition. If the trace memory is completely full, then the oldest recorded value is overwritten (FIFO principle).

"Trace start" in the I/O configuration or the registers 4.3.9.8.6.1 "Trigger condition on falling edge" and 4.3.9.8.6.2 "Trigger condition on rising edge" determine whether a positive, negative or any edge must be triggered.

Data type	Value	Information
INT	-32767 to 32767	
	-32768	Continuous trace without a stopping point

Stopping the trace

Name:
TraceTriggerStop

The stopping position is defined relative to the configured trigger condition in this register.

- When configuring an early trigger event, this value refers to the trigger event.
- When configuring a delayed trigger event, this value refers to the starting event.

Data type	Value
UINT	0 to 65535

4.3.9.8.9 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

4.3.9.8.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard priority	200 µs
High priority with trace function	300 µs

4.3.9.8.11 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

4.3.10 X20AI2632-1

4.3.10.1 General information

The module is equipped with 2 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminal connections.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs
- Either current or voltage signal possible
- Extended signal range
- 16-bit digital converter resolution
- Simultaneous input conversion
- Very fast conversion time

4.3.10.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2632-1	X20 analog input module, 2 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 46: X20AI2632-1 - Order data

4.3.10.3 Technical data

Product ID	X20AI2632-1
Short description	
I/O module	2 analog inputs ±11 V or 0 to 22 mA
General information	
B&R ID code	0xA29E
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W [1]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Analog inputs	
Input	±11 V or 0 to 22 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.387 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permitted input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of the digital value during overload	
Below lower limit	
Voltage	0x8001
Current	0x0000
Above upper limit	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - 3rd-order low pass / cutoff frequency 10 kHz
Max. error at 25°C	
Voltage	
Gain	0.08% [3]
Offset	0.01% [4]
Current	
Gain	0.08% [3]
Offset	0.02% [5]
Max. gain drift	
Voltage	0.01 %/°C [3]
Current	0.01 %/°C [3]
Max. offset drift	
Voltage	0.001 %/°C [4]
Current	0.002 %/°C [5]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB

Table 47: X20AI2632-1 - Technical data

Product ID	X20AI2632-1
Nonlinearity	
Voltage	<0.01% 4)
Current	<0.015% 5)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 47: X20AI2632-1 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 22 V measurement range.
5) Based on the 22 mA measurement range.

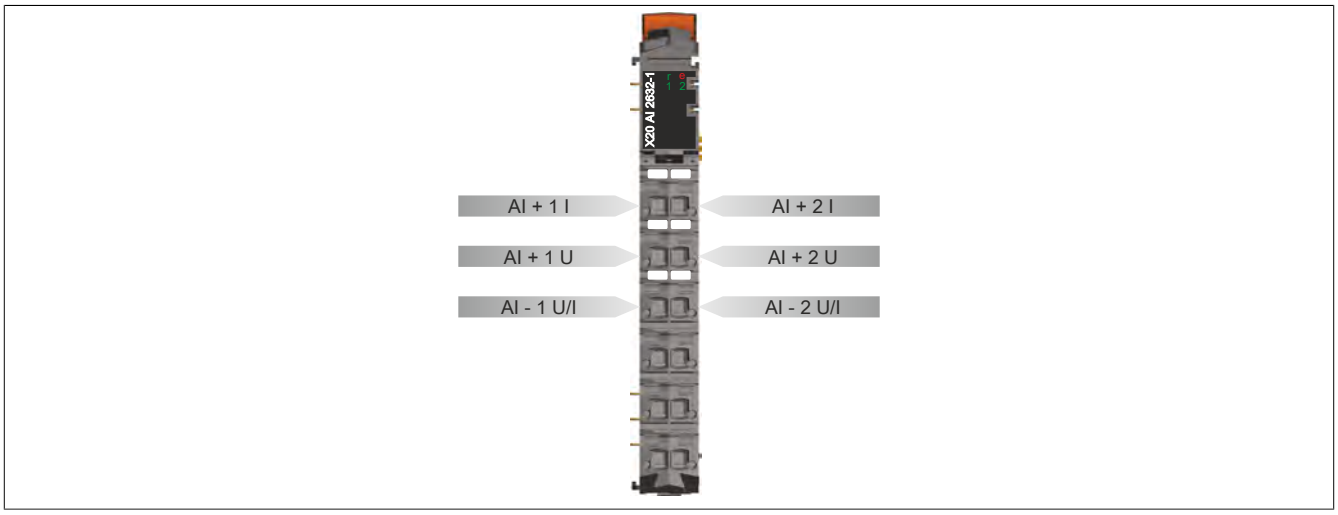
4.3.10.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 2	Green	Off	Open line2) or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

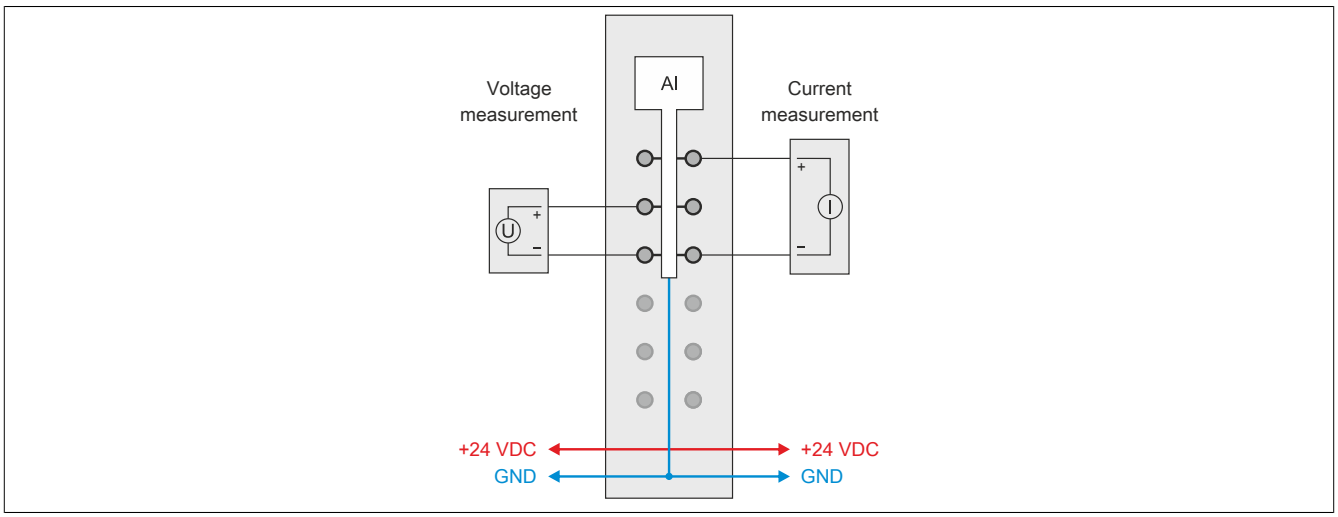
4.3.10.5 Pinout



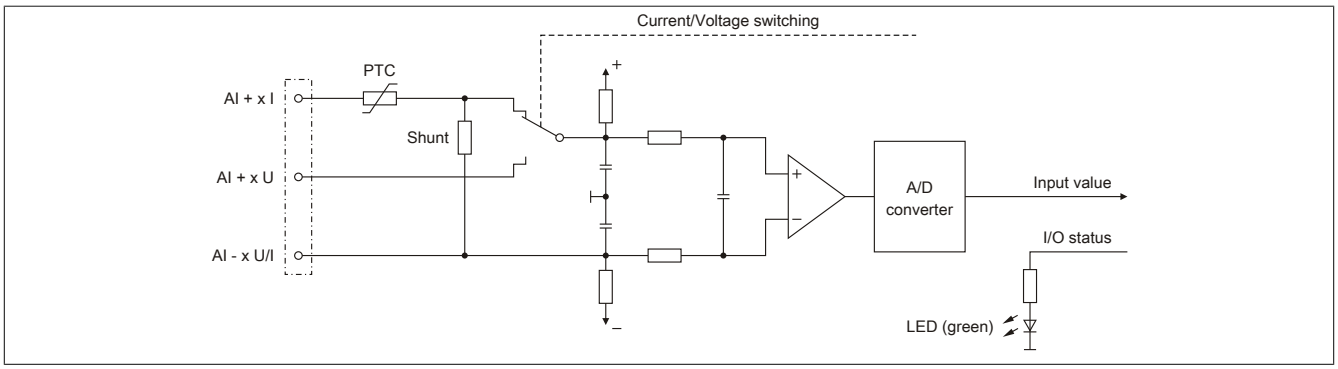
4.3.10.6 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Supply module X20PS9500/X20PS9502
- CPU modules



4.3.10.7 Input circuit diagram



4.3.10.8 Register description

4.3.10.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.10.8.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257	ConfigOutput01 (channel configuration)	USINT				•
289	ConfigOutput06 (channel configuration)	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259	ConfigOutput26 (filter order)	USINT				•
291	ConfigOutput28 (filter order)	USINT				•
262	ConfigOutput27 (filter cutoff frequency)	UINT				•
294	ConfigOutput29 (filter cutoff frequency)	UINT				•
	Scaling					
276	ConfigOutput04 (user-defined gain)	DINT				•
308	CongifOutput09 (user-defined gain)	DINT				•
284	ConfigOutput05 (user-defined offset)	DINT				•
316	ConfigOutput10 (user-defined offset)	DINT				•
	User-defined limit values					
266	ConfigOutput02 (minimum limit value)	UINT				•
298	ConfigOutput07 (minimum limit value)	UINT				•
270	ConfigOutput03 (maximum limit value)	UINT				•
302	ConfigOutput08 (maximum limit value)	UINT				•
Communication						
0	AnalogInput01	INT	•			
4	AnalogInput02	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	Channel02OK	Bit 1				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	SynchronizationViolationErrorCounter	UINT		•		
2097	Range violation (neg. and pos.)	USINT	•			
	Channel01underflow	Bit 0				
	Channel01overflow	Bit 1				
	Channel02underflow	Bit 4				
	Channel02overflow	Bit 5				
2099	Working range violation (pos.)	USINT	•			
	Channel01outofrange	Bit 0				
	Channel02outofrange	Bit 1				
518	Ch01OutofRange	UINT		•		
550	Ch02OutofRange	UINT		•		
522	Ch01Underflow	UINT		•		
554	Ch02Underflow	UINT		•		
526	Ch01Overflow	UINT		•		
558	Ch02Overflow	UINT		•		
Additional analysis functions						
133	ConfigOutput21 (trigger condition on falling edge)	USINT				•
135	ConfigOutput22 (trigger condition on rising edge)	USINT				•
129	Analysis control byte	USINT			•	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	MinMaxStart02	Bit 5				
129	Analysis status byte	USINT	•			
	MinMaxStart01Readback	Bit 4				
	MinMaxStart02Readback	Bit 5				
	Limit values					
530	MinInput01	INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
562	MinInput02	INT	●			
534	MaxInput01	INT	●			
566	MaxInput02	INT	●			
538	CH01MinMaxLatchCounter	UINT		●		
570	CH02MinMaxLatchCounter	UINT		●		
	Trace configuration					
1026	TraceChannelEnable	USINT				●
1030	TraceSampleDepth	UINT				●
4157	ConfigOutput25 (recording priority)	USINT				●
1037	Starting a recording	USINT			●	
	TraceEnable01	Bit 0				
1089	Recording status	USINT	●			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	●			
1098	TriggerCount	UINT	●			
1102	TriggerFailCount	UINT	●			
	Comparator					
450	cfgComp_LowLimitCh01	INT			(●)	●
458	cfgComp_LowLimitCh02	INT			(●)	●
454	cfgComp_HighLimitCh01	INT			(●)	●
462	cfgComp_HighLimitCh02	INT			(●)	●
662	CompStateCollection	UINT	●			
490	cfgComp_NominalState	UINT				●
482	cfgComp_EnableMask	UINT				●
486	cfgComp_ConditionTypeMask	UINT				●
	Time-offset trace					
1042	TraceTriggerStart	INT				●
1046	TraceTriggerStop	UINT				●

4.3.10.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257	-	ConfigOutput01 (channel configuration)	USINT				●
289	-	ConfigOutput06 (channel configuration)	USINT				●
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				●
	Filtering						
259	-	ConfigOutput26 (filter order)	USINT				●
291	-	ConfigOutput28 (filter order)	USINT				●
262	-	ConfigOutput27 (filter cutoff frequency)	UINT				●
294	-	ConfigOutput29 (filter cutoff frequency)	UINT				●
	Scaling						
276	-	ConfigOutput04 (user-defined gain)	DINT				●
308	-	CongifOutput09 (user-defined gain)	DINT				●
284	-	ConfigOutput05 (user-defined offset)	DINT				●
316	-	ConfigOutput10 (user-defined offset)	DINT				●
	User-defined limit values						
266	-	ConfigOutput02 (minimum limit value)	UINT				●
298	-	ConfigOutput07 (minimum limit value)	UINT				●
270	-	ConfigOutput03 (maximum limit value)	UINT				●
302	-	ConfigOutput08 (maximum limit value)	UINT				●
Communication							
0	0	AnalogInput01	INT	●			
4	2	AnalogInput02	INT	●			
650	-	SampleCycleCounter	UINT		●		
	Error monitoring and counters						
641	-	Channel status	USINT		●		
		Channel01OK	Bit 0				
		Channel02OK	Bit 1				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		●		
658	-	SynchronizationViolationErrorCounter	UINT		●		
2097	-	Range violation (neg. and pos.)	USINT		●		
		Channel01underflow	Bit 0				
		Channel01overflow	Bit 1				
		Channel02underflow	Bit 4				
		Channel02overflow	Bit 5				
2099	-	Working range violation (pos.)	USINT		●		
		Channel01outofrange	Bit 0				
		Channel02outofrange	Bit 1				
518	-	Ch01OutofRange	UINT		●		
550	-	Ch02OutofRange	UINT		●		
522	-	Ch01Underflow	UINT		●		
554	-	Ch02Underflow	UINT		●		
526	-	Ch01Overflow	UINT		●		
558	-	Ch02Overflow	UINT		●		
Additional analysis functions							
133	-	ConfigOutput21 (trigger condition on falling edge)	USINT				●
135	-	ConfigOutput22 (trigger condition on rising edge)	USINT				●
129	-	Analysis control byte	USINT				●
		TraceTrigger01	Bit 0				
		MinMaxStart01	Bit 4				
		MinMaxStart02	Bit 5				
129	-	Analysis status byte	USINT		●		
		MinMaxStart01Readback	Bit 4				
		MinMaxStart02Readback	Bit 5				
	Limit values						
530	-	MinInput01	INT		●		
562	-	MinInput02	INT		●		
534	-	MaxInput01	INT		●		
566	-	MaxInput02	INT		●		
538	-	CH01MinMaxLatchCounter	UINT		●		
570	-	CH02MinMaxLatchCounter	UINT		●		

1) The offset specifies the position of the register within the CAN object.

4.3.10.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.10.8.4 Configuration

This module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately from one another either on the voltage or current input for the following areas:

- Permitted voltage: ±11 V at 20 Ω
- Permitted current: 22 mA (maximum 40 mA) (<400 Ω)

4.3.10.8.4.1 Channel configuration

Name:
ConfigOutput01 for channel 01
ConfigOutput06 for channel 02

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using the correct terminal block pins.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±11 VDC
		1	Current terminal for 0 to 22 mA
1	Gain selector	0	Voltage ±11 VDC
		1	Current 0 to 22 mA
2 - 3	Reserved	-	
4	Filtering active (only if bit 7 = 0)	0	Inactive
		1	Active
5	Minimum/Maximum analysis active (only if bit 7 = 0)	0	Inactive
		1	Active
6	Error monitoring active (only if bit 7 = 0)	0	Inactive
		1	Active
7	Enables channel	0	Channel enabled
		1	Channel disabled

4.3.10.8.4.2 Sampling and conversion

The analog signal is sampled in 2 steps.

- **Conversion task**
  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.
  The timespan needed for conversion results from the set sampling time.
- **Processing task**
  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Function
UINT	50 to 10,000	Default value = 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

4.3.10.8.4.3 Filtering (optional)

If filtering is enabled in the 4.3.10.8.4.1 "Channel configuration" register, the basic data of the A/D converter is filtered per channel. The following registers are available to specify the filter order and respective cutoff frequency for configuring the low-pass filter:

- "Filter order"
- "Filter cutoff frequency"

Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2

The filter order is specified in this register. The "Filter cutoff frequency" register is used to configure the respective cutoff frequency of the filter.

Data type	Value
USINT	1 to 4

Internal filter orders greater than 1 are implemented as cascaded first-order filters. Since the filter is calculated in the sampling cycle, the filter characteristics are directly related to the settings for the sampling cycle time.

Calculating the cutoff frequency of an nth-order filter:

yn = a * xn + b * y(n-1)

Approximate calculation

a = Sampling time / (Sampling time + 1/Cutoff frequency)

b = 1 - a

Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Description
UINT	1 to 65,535	Cutoff frequency in hertz

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

4.3.10.8.4.4 Scaling (optional)

Scaling A/D converter data is an option for the user. The following registers are available for this:

- "User-defined gain" (= ku)
- "User-defined offset" (= du)

Scaling calculation:

Scaled value = k * A/C value + d

Gain $k = k_{Calibration} * ku$

Offset $d = d_{Calibration} + du$

The value has to be limited since it can exceed the 16-bit constraints. To provide the greatest degree of flexibility, limiting is possible using the registers "Minimum limit value" and "Maximum limit value".

User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65,536 (0x10000) corresponds to a gain of 1.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65,536 (0x10000) corresponds to an offset of 1.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.3.10.8.4.5 User-defined limit values

If the application requires a limitation of the range of values, then the user can define his own limit values. These values will also be use for the module's error statistics. The following registers are available for this:

- "Minimum limit value"
- "Maximum limit value"

Information:

32-bit numbers are used inside the module. A limit value violation can therefore also be determined if the permitted range of values was defined from -32768 to 32767.

Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2

The minimum limit value is configured in this register. This limit value is also used as the lower value in the error statistics (see register "Counter for range exceeded violations (neg.)").

Data type	Value
INT	-32768 to 32767

Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2

The maximum limit value is configured in this register. This limit value is also used as the upper value in the error statistics (see register "Counter for range exceeded violations (pos.)").

Data type	Value
INT	-32768 to 32767

4.3.10.8.5 Communication - General

The module's analog inputs convert current and voltage values with 16-bit resolution. This information can be used by the application with the help of the registers listed here.

4.3.10.8.5.1 Analog input channels

Name:
AnalogInput01 to AnalogInput02

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal ±11 VDC
	0 to 32,767	Current signal 0 to 22 mA

4.3.10.8.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Value
UINT	0 to 65535

4.3.10.8.5.3 Error monitoring and counters

Channel status

Name:
Channel01OK to Channel02OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors
1	Channel02OK	0	OK
		1	Errors
2 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "Synchronization error counter".
2) Identical to bit 0 of the registers "Counter for faulty sampling cycles".

Synchronization error counter

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See 4.3.9.8.4.2 "Sampling and conversion".

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Range violation (neg. and pos.)

Name:
Channel01underflow to Channel02underflow
Channel01overflow to Channel02overflow

This register indicates whether a range violation (pos. and/or neg.) of the limit values defined in the registers "Minimum limit value" and "Maximum limit value" has occurred. The individual bits in this register are identical to the values of the lowest bits in the registers "Counter for range exceeded violations (neg.)" and "Counter for range exceeded violations (pos.)".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
1	Channel02underflow	0	No error
		1	Range exceeded (.neg) on channel 2
2 - 3	Reserved	-	
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
5	Channel02overflow	0	No error
		1	Range exceeded (.pos) on channel 2
6 - 7	Reserved	-	

Working range violation (pos.)

Name:
Channel01OutofRange to Channel02OutofRange

This register indicates whether the input value exceeds the module's maximum measurement range. The individual bits in this register are identical to the values of the lowest bits in the register "Counter for work range violations (pos.)".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutofRange	0	No error
		1	Working range violation (pos.) of channel 1
1	Channel02OutofRange	0	No error
		1	Working range violation (pos.) of channel 2
2 - 7	Reserved	-	

Counter for work range violations (pos.)

Name:
CH01OutofRange to CH02OutofRange

Errors outside of the module's maximum possible measurement range are indicated in this register. These errors lead to full-scale deflection of the A/D converter.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.10.8.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (neg.)

Name:
CH01Underflow to CH02Underflow

This register indicates range exceeded violations (neg.) of the value configured in the register "Minimum limit value".

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.10.8.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (pos.)

Name:
CH01Overflow to CH02Overflow

This register indicates range exceeded violations (pos.) of the value configured in the register "Maximum limit value".

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.10.8.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

4.3.10.8.6 Additional analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

- **Limit value analysis**
  If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched internally in the module. A measurement period can be triggered using the control byte. When the respective configured edge is generated by the application, the limit values from the previous measurement period are displayed and the internal latch register is reset.
- **Recording sampled values**
  If recording sampled values has been enabled for a channel, then the sampled values are additionally recorded in the module's internal FIFO memory. If the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

It is only possible to use the recording of sampled values if the module is operated on an X2X master that is an SG4 CPU.

4.3.10.8.6.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register configures whether the falling edge is used to trigger the trace and determination of the input value in the register 4.3.9.8.6.3 "Analysis control byte".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination
		1	Falling edge determines input value of channel 1
5	MinMaxStart02	0	No determination
		1	Falling edge determines input value of channel 2
6 - 7	Reserved	0	

4.3.10.8.6.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register configures whether the rising edge is used to trigger the trace and determination of the input value in the register 4.3.9.8.6.3 "Analysis control byte".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Rising edge does not initiate trigger
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination
		1	Rising edge determines input value of channel 1
5	MinMaxStart02	0	No determination
		1	Rising edge determines input value of channel 2
6 - 7	Reserved	0	

4.3.10.8.6.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart02

The trace function and determination of the minimum/maximum input values can be started in this register.
Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers 4.3.9.8.6.1 "Trigger condition on falling edge" and 4.3.9.8.6.2 "Trigger condition on rising edge".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Does not initiate trigger/trace
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not initiated
		1	Initiates determination of input value of channel 1
5	MinMaxStart02	0	Determination not initiated
		1	Initiates determination of input value of channel 2
6 - 7	Reserved	-	

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

4.3.10.8.6.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart02Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel
5	MinMaxStart02Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel
6 - 7	Reserved	-	

4.3.10.8.7 Limit values

Limit value analysis must be enabled for the desired channel. See 4.3.10.8.4.1 "Channel configuration". The sampled value of the channel is then compared to the minimum and maximum values that are stored internally in the module. If a new measurement period is initiated with the 4.3.9.8.6.3 "Analysis control byte" register, then the values of the previous measurement period can be read from the respective registers intended for this.

4.3.10.8.7.1 Maximum input values

Name:
MaxInput01 to MaxInput02

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

4.3.10.8.7.2 Minimum input values

Name:
MinInput01 to MinInput02

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

4.3.10.8.7.3 Limit value trigger counter

Name:
CH01MinMaxLatchCounter to CH02MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

4.3.10.8.8 Trace

If the module is operated on a SG4 CPU, the digitalized input values are recorded by the module. The module must be operated in "Supervised" mode in order to use the trace function.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism can only be used if the module is connected directly to the CPU, not if it is operated behind a bus controller.

4.3.10.8.8.1 Enable recording

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
1	Channel 2	0	Channel disabled
		1	Channel enabled
2 - 7	Reserved	-	

4.3.10.8.8.2 Number of values to be recorded

Name:
TraceSampleDepth

16 kB are available on the module for the trace. The FIFO memory limitation means that a maximum of 8192 analog values can be recorded. This memory is divided up equally among the enabled channels. The actual number of maximum possible recordings therefore depends on the number of channels enabled for trace:

1 channel enabled: Up to 8192 recordings
2 channels enabled: Up to 4096 recordings per channel

Data type	Value	Function
UINT	2 to 8192	Default value = 1024

4.3.10.8.8.3 Recording priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard (default value)
	6	Trace priority higher than X2X Link communication

4.3.10.8.8.4 Starting a recording

Name:

TraceEnable01

This register starts the recording according to the specifications for edge control or the comparator.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

4.3.10.8.8.5 Recording status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

4.3.10.8.8.6 Free trace buffer

Name:
FreeBufferSize

Specifies the available FIFO memory area in bytes for the trace

Data type	Value
UINT	0 to 65535

4.3.10.8.8.7 Counter for trace triggers

Name:
TriggerCount

The number of trigger events that have occurred since "starting the trace" is indicated in this register.

Data type	Value
UINT	0 to 65535

4.3.10.8.8.8 Counter for faulty recording triggers

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be performed.

Data type	Value
UINT	0 to 65535

4.3.10.8.8.9 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold value bits for all channels are grouped together in the lower-value byte of the "Hysteresis status of the channels" register. In addition, the states of the previous sampling are stored in the higher-value byte.

The 4 status messages of each channel can be linked according to the following logic via a logical connective mask using AND or OR operators and used as a trace trigger:

```
delta = (Current_HysteresisStatus ^ NominalValues) // Different between current status and preset
cond = delta & Selected_HysteresisStatusBits // Eliminate irrelevant status messages
cond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if ((0 == (cond & ~LogicalOperators)) &&
(0 != (~cond & LogicalOperators))) { => Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	cfgComp_EnableMask
Current_HysteresisStatus	CompStateCollection
Nominal values	cfgComp_NominalState
Logical operators	cfgComp_ConditionTypeMask

Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh02

The lower limit value for hysteresis is configured in this register.

Data type	Value
INT	-32768 to 32767

Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh02

The upper limit value for hysteresis is configured in this register.

Data type	Value
INT	-32768 to 32767

Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
12 - 15	Reserved	-	

Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
12 - 15	Reserved	-	

Information:

This is a "whitelist", i.e. the trace starts as soon as the current status message takes on the state predefined here.

One or more matches will be necessary depending on the selection of the relevant hysteresis status bits and logical connective operators.

Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register selects which status bits of the hysteresis comparison should be used to generate the trigger.

For more information about using this register, see 4.3.9.8.8.9 "Comparator for trigger conditions".

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
2	Channel02 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
3	Channel02 InRange status in the current cycle	0	Do not use
		1	Use for generation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
10	Channel02 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
11	Channel02 InRange status in the last cycle	0	Do not use
		1	Use for generation
12 - 15	Reserved	-	

Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

The desired state operators with which the status bits are linked to one another to generate a trigger are selected in this register.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "Selecting the relevant hysteresis status bits" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
2	Channel02 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
3	Channel02 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
10	Channel02 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
11	Channel02 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
12 - 15	Reserved	-	

4.3.10.8.8.10 Time-offset trace

Additional conditions for shifting the starting and stopping points can be defined if the trace should be chronologically offset to the trigger.

Starting the trace

Name:
TraceTriggerStart

The starting position is defined relative to the configured trigger condition in this register. Positive values mean that the trace takes place x samples after the trigger condition. Negative values mean that the trace takes place x samples before the trigger condition.

The value -32768 performs the trace without regard for the configured trigger condition. If the trace memory is completely full, then the oldest recorded value is overwritten (FIFO principle).

"Trace start" in the I/O configuration or the registers 4.3.9.8.6.1 "Trigger condition on falling edge" and 4.3.9.8.6.2 "Trigger condition on rising edge" determine whether a positive, negative or any edge must be triggered.

Data type	Value	Information
INT	-32767 to 32767	
	-32768	Continuous trace without a stopping point

Stopping the trace

Name:
TraceTriggerStop

The stopping position is defined relative to the configured trigger condition in this register.

- When configuring an early trigger event, this value refers to the trigger event.
- When configuring a delayed trigger event, this value refers to the starting event.

Data type	Value
UINT	0 to 65535

4.3.10.8.9 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

4.3.10.8.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard priority	200 µs
High priority with trace function	300 µs

4.3.10.8.11 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

4.3.11 X20AI2636

4.3.11.1 General information

The module is equipped with 2 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminal connections. With the oversampling function, up to 16 analog values per channel can be recorded.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs
- Current or voltage signal configuration for the entire module
- 16-bit digital converter resolution
- Minimum conversion time of 40 µs for all inputs
- The conversion time for the entire module can be configured in 0.02 µs steps.
- Maximum 14 samples (16-bit) for the entire module per X2X Link cycle
- Oversampling: Up to 16 analog values per channel (internal)
- Timestamp for the last conversion of an X2X Link cycle

4.3.11.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI2636	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 48: X20AI2636 - Order data

4.3.11.3 Technical data

Product ID	X20AI2636
Short description	
I/O module	2 analog inputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0xB3A7
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W [1]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	40 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permitted input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of the digital value during overload	
Below lower limit	
Voltage	0x8001
Current	0x0000
Above upper limit	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - 3rd-order low pass / cutoff frequency 10 kHz
Max. error at 25°C	
Voltage	
Gain	0.08% [2]
Offset	0.01% [3]
Current	
Gain	0.08% [2]
Offset	0.02% [4]
Max. gain drift	
Voltage	0.01 %/°C [2]
Current	0.01 %/°C [2]
Max. offset drift	
Voltage	0.001 %/°C [3]
Current	0.002 %/°C [4]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB

Table 49: X20AI2636 - Technical data

Product ID	X20AI2636
Non-linearity	
Voltage	<0.01% 3)
Current	<0.015% 4)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5+0.2 mm

Table 49: X20AI2636 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

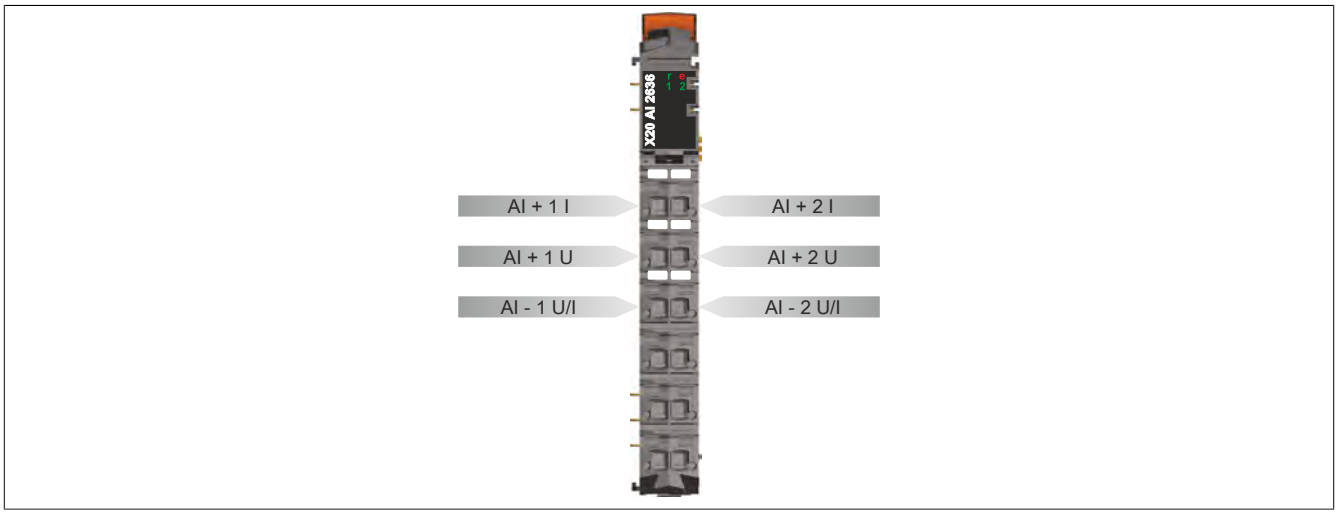
4.3.11.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 2	Green	Off	Open line2) or sensor is disconnected
			Blinking	Channel error: Underflow, overflow or broken connection
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

4.3.11.5 Pinout

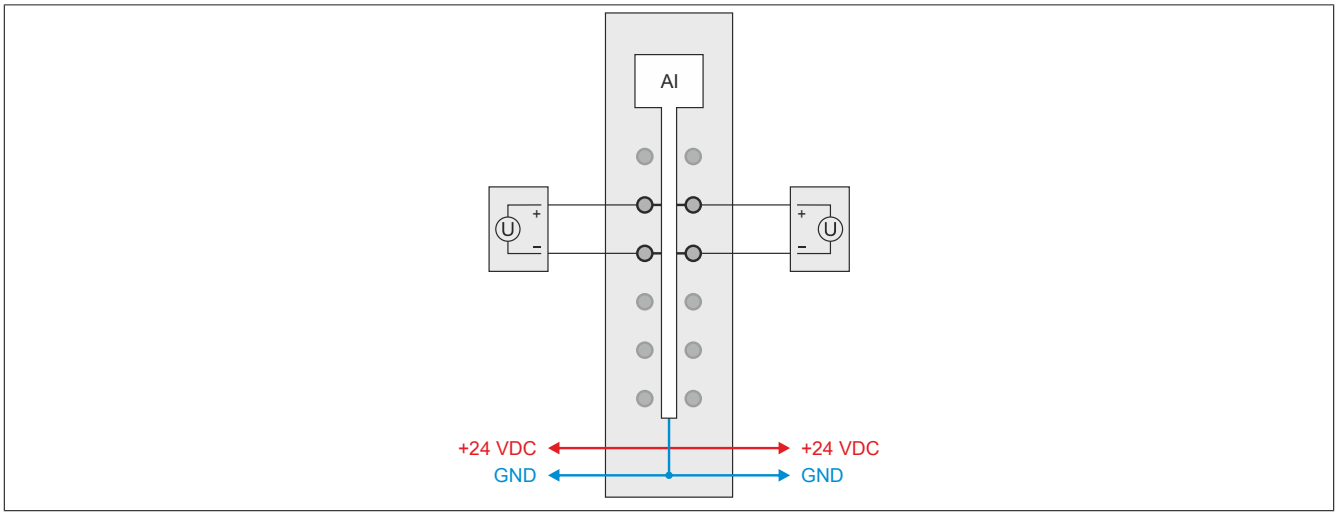


4.3.11.6 Connection example

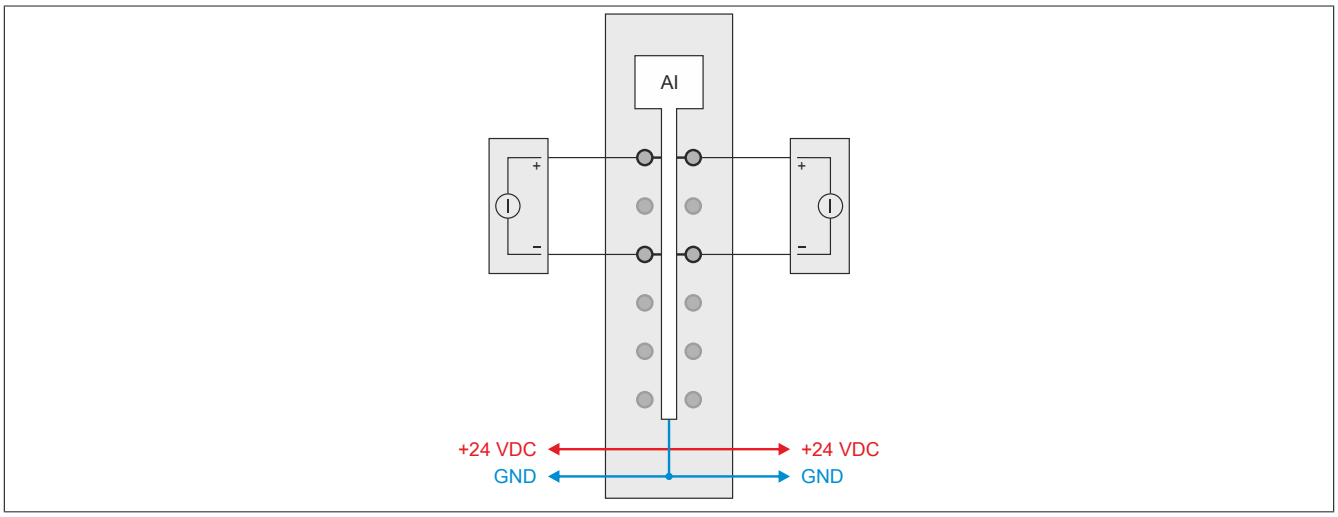
To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Supply module X20PS9500/X20PS9502
- CPU modules

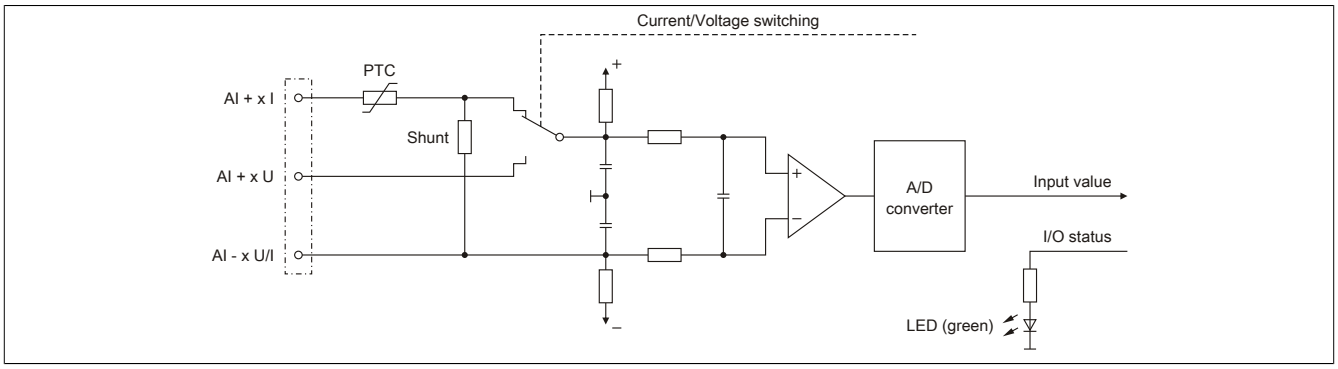
Voltage measurement



Current measurement



4.3.11.7 Input circuit diagram



4.3.11.8 Register description

4.3.11.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.11.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
System configuration						
513	CfO_BaseConfig	USINT				•
15364	CfO_CycleTime	UDINT				•
15370	CfO_SyncOffset	UINT				•
15374	CfO_Prescaler	UINT				•
Error messages - Configuration						
385	CfO_ErrorID0007	USINT				•
389	CfO_ErrorID1017	USINT				•
Physical channel configuration						
8194 8450	CfO_ModeCh01 CfO_ModeCh02	UINT				•
8204 8460	CfO_UserGainCh01 CfO_UserGainCh02	DINT				•
8212 8468	CfO_UserOffsetCh01 CfO_UserOffsetCh02	DINT				•
8220 8476	CfO_Alpha0Ch01 CfO_Alpha0Ch02	DINT				•
8228 8484	CfO_Alpha1Ch01 CfO_Alpha1Ch02	DINT				•
8236 8492	CfO_Alpha2Ch01 CfO_Alpha2Ch02	DINT				•
8244 8500	CfO_Beta1Ch01 CfO_Beta1Ch02	DINT				•
8252 8508	CfO_Beta2Ch01 CfO_Beta2Ch02	DINT				•
8198 8454	CfO_CutOffFrequCh01 CfO_CutOffFrequCh02	UINT				•
Logical channel configuration						
10242 + (N-1) * 256	CfO_LogCh0NMode (index N = 1 to 6)	UINT				•
10245 + (N-1) * 256	CfO_LogCh0NSource00 (index N = 1 to 6)	USINT				•
10247 + (N-1) * 256	CfO_LogCh0NSource01 (index N = 1 to 6)	USINT				•
10260 + (N-1) * 256	CfO_LogCh0NFuncPar00 (index N = 1 to 6)	UDINT				•
10268 + (N-1) * 256	CfO_LogCh0NFuncPar01 (index N = 1 to 6)	UDINT				•
Analog inputs - Communication						
5062 5070	AnalogInput01 AnalogInput02	INT	•			
Error messages - Communication						
261	"StandardErrors" registers	USINT	•			
	Channel01Error	Bit 0				
	Channel02Error	Bit 1				
	PhysicalError	Bit 4				
	LogicalError	Bit 5				
325	"AcknowledgeStandardErrors" registers	USINT			•	
	AckChannel01Error	Bit 0				
	AckChannel01Error	Bit 1				
	AckPhysicalError	Bit 4				
	AckLogicalError	Bit 5				
257	"ExtendedChannelErrorMessages" registers	USINT	•			
	Channel01OutOfRange	Bit 0				
	Channel01FilterError	Bit 1				
	Channel01Underflow	Bit 2				
	Channel01Overflow	Bit 3				
	Channel02OutOfRange	Bit 4				
	Channel02FilterError	Bit 5				
	Channel02Underflow	Bit 6				
	Channel02Overflow	Bit 7				
321	"AcknowledgeExtendedChannelErrorMessages" registers	USINT			•	
	AckChannel01OutOfRange	Bit 0				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
	AckChannel01FilterError	Bit 1				
	AckChannel01Underflow	Bit 2				
	AckChannel01Overflow	Bit 3				
	AckChannel02OutOfRange	Bit 4				
	AckChannel02FilterError	Bit 5				
	AckChannel02Underflow	Bit 6				
	AckChannel02Overflow	Bit 7				
Physical analog sample display						
4102 + (16-N) * 64	PhysCh01SampleN (index N = 1 to 16)	INT	●			
4110 + (16-N) * 64	PhysCh02SampleN (index N = 1 to 16)	INT	●			
5106	PhysTimestamp	INT	●			
5108	PhysTimestamp	DINT	●			
5113	PhysSampleCount	SINT	●			
5114	PhysSampleCount	INT	●			
Logical analog and digital sample display						
6148 + (16-N) * 64	LogicCh01SampleN (index N = 1 to 16) (32-bit)	DINT	●			
6150 + (16-N) * 64	LogicCh01SampleN (index N = 1 to 16) (16-bit)	INT	●			
6156 + (16-N) * 64	LogicCh02SampleN (index N = 1 to 16) (32-bit)	DINT	●			
6158 + (16-N) * 64	LogicCh02SampleN (index N = 1 to 16) (16-bit)	INT	●			
6164 + (16-N) * 64	LogicCh03SampleN (index N = 1 to 16) (32-bit)	DINT	●			
6166 + (16-N) * 64	LogicCh03SampleN (index N = 1 to 16) (16-bit)	INT	●			
6172 + (16-N) * 64	LogicCh04SampleN (index N = 1 to 16) (32-bit)	DINT	●			
6174 + (16-N) * 64	LogicCh04SampleN (index N = 1 to 16) (16-bit)	INT	●			
6180 + (16-N) * 64	LogicCh05SampleN (index N = 1 to 16) (32-bit)	DINT	●			
6182 + (N-16) * 64	LogicCh05SampleN (index N = 1 to 16) (16-bit)	INT	●			
6188 + (16-N) * 64	LogicCh06SampleN (index N = 1 to 16) (32-bit)	DINT	●			
6190 + (16-N) * 64	LogicCh06SampleN (index N = 1 to 16) (16-bit)	INT	●			
7109 + (N-1) * 8	LogicCh0NSample16_9 (index N = 1 to 5)	USINT	●			
7151	LogicCh06Sample16_9	USINT	●			
7111 + (N-1) * 8	LogicCh0NSample8_1 (index N = 1 to 5)	USINT	●			
7149	LogicCh06Sample8_1	USINT	●			
7154	LogicTimestamp	INT	●			
7156	LogicTimestamp	DINT	●			
7161	LogicSampleCount	SINT	●			
7162	LogicSampleCount	INT	●			

4.3.11.8.3 Function model 254

The "Bus controller" function model has the following limitations compared to the "Standard" function model:

- No oversampling function since consistency is not possible when operating CAN-based bus controllers due to the limited data range
- The sampling cycle time is set to 100 µs.
- No timestamp function
- A range of logical functions is available for processing the physical values right on the module:
  - Output of physical values (standard)
  - Addition of two channels with scaling
  - Integral addition of two channels with scaling
  - Multiplication of two channels with scaling
  - Integral multiplication of two channels with scaling

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
System configuration							
513	-	CfO_BaseConfig	USINT				•
15364	-	CfO_CycleTime	UDINT				•
15370	-	CfO_SyncOffset	UINT				•
15374	-	CfO_Prescaler	UINT				•
Error messages - Configuration							
385	-	CfO_ErrorID0007	USINT				•
389	-	CfO_ErrorID1017	USINT				•
Physical channel configuration							
8194 8450	-	CfO_ModeCh01 CfO_ModeCh02	UINT				•
8204 8460	-	CfO_UserGainCh01 CfO_UserGainCh02	DINT				•
8212 8468	-	CfO_UserOffsetCh01 CfO_UserOffsetCh02	DINT				•
8220 8476	-	CfO_Alpha0Ch01 CfO_Alpha0Ch02	DINT				•
8228 8484	-	CfO_Alpha1Ch01 CfO_Alpha1Ch02	DINT				•
8236 8492	-	CfO_Alpha2Ch01 CfO_Alpha2Ch02	DINT				•
8244 8500	-	CfO_Beta1Ch01 CfO_Beta1Ch02	DINT				•
8252 8508	-	CfO_Beta2Ch01 CfO_Beta2Ch02	DINT				•
8198 8454	-	CfO_CutOffFrequCh01 CfO_CutOffFrequCh02	UINT				•
Logical channel configuration							
10242 + (N-1) * 256	-	CfO_LogCh0NMode (index N = 1 to 6)	UINT				•
10245 + (N-1) * 256	-	CfO_LogCh0NSource00 (index N = 1 to 6)	USINT				•
10247 + (N-1) * 256	-	CfO_LogCh0NSource01 (index N = 1 to 6)	USINT				•
10260 + (N-1) * 256	-	CfO_LogCh0NFuncPar00 (index N = 1 to 6)	UDINT				•
10268 + (N-1) * 256	-	CfO_LogCh0NFuncPar01 (index N = 1 to 6)	UDINT				•
Analog inputs - Communication							
5062 5070	0 2	AnalogInput01 AnalogInput02	INT	•			
Error messages - Communication							
261	-	"StandardErrors" registers	USINT		•		
		Channel01Error	Bit 0				
		Channel02Error	Bit 1				
		PhysicalError	Bit 4				
		LogicalError	Bit 5				
325	-	"AcknowledgeStandardErrors" registers	USINT				•
		AckChannel01Error	Bit 0				
		AckChannel01Error	Bit 1				
		AckPhysicalError	Bit 4				
		AckLogicalError	Bit 5				
257	-	"ExtendedChannelErrorMessages" registers	USINT		•		
		Channel01OutOfRange	Bit 0				
		Channel01FilterError	Bit 1				
		Channel01Underflow	Bit 2				

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
		Channel01Overflow	Bit 3				
		Channel02OutOfRange	Bit 4				
		Channel02FilterError	Bit 5				
		Channel02Underflow	Bit 6				
		Channel02Overflow	Bit 7				
321	-	"AcknowledgeExtendedChannelErrorMessages" registers	USINT				•
		AckChannel01OutOfRange	Bit 0				
		AckChannel01FilterError	Bit 1				
		AckChannel01Underflow	Bit 2				
		AckChannel01Overflow	Bit 3				
		AckChannel02OutOfRange	Bit 4				
		AckChannel02FilterError	Bit 5				
		AckChannel02Underflow	Bit 6				
		AckChannel02Overflow	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.3.11.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.11.8.4 General information

There is a difference on the module between physical (default) and logical values:

Physical or default values
The conversion results are transferred to the higher-level system after being scaled and filtered. They are not processed further.

Logical values
The physical values can be further processed with mathematical functions and comparators. In addition, another logical channel can be used as a starting point to further process a logical function.

4.3.11.8.5 Operating mode - Oversampling

The input values are recorded with a configurable sampling cycle time and saved with timestamp to the internal physical data buffer. This data range can then be read out in the cyclic data transfer using a configurable data length.

The recording and transmission system for the logical channels is identical to that for the physical channels. The functions of the logical channels are also executed in the configured sampling cycle time and saved with timestamp to the logical data buffer. The values can also be read out from here using configurable cyclic data points.

The defined sampling cycle time may not be sufficient for the sum of all physical and logical functions if using fast X2X Link cycle times, however. If influencing the physical sampling is not permitted, then a prescaler can be used to slow down the logical processing.

Information:

The ability to adjust the sampling cycle time as needed on the module means there is basically no synchronization with X2X Link, regardless of whether standard inputs or an oversampling function is configured.

If synchronization is required, then the configured sampling cycle time must be a multiple of the X2X Link cycle time!

4.3.11.8.5.1 Analog oversampling

When using analog oversampling, the enabled channels are stored in the module within a configurable time frame independently of the X2X cycle. Space is available for 16 analog values per physical and logical channel.

These samplings are are numbered from 1 to 16 for the registers. The conversions or calculations of individual channels with the same number (i.e. sample line 1 to 16, e.g. PhysCh01Sample**10**, PhysCh02Sample**10**, etc.) are derived from the same sampling cycle or logical computing cycle and therefore have the same timestamp.

The timestamp refers to the newest data value, i.e. always to sample line 1. If a timestamp for older data points is needed, it needs to be back-calculated in the application using the sampling cycle time configured on the module. The prescaler must also be taken into account for logical channels.

Calculation example

Sample line	Calculation	
1	Timestamp	**Newest value**
2	Timestamp - Sampling cycle time	
3	Timestamp - 2 * Sampling cycle time	
4	Timestamp - 3 * Sampling cycle time	
...	...	
10	Timestamp - 9 * Sampling cycle time	
...	...	
16	Timestamp - 15 * Sampling cycle time	**Oldest value**

How the buffer is organized can be seen from this. This is not a FIFO buffer but a static buffer that the values are pushed through. Sample line 1 always contains the newest values, the next line the second newest, all the way up to sample line 16, which contains the oldest values.

The sample counter is a circular counter, with the number of new sample lines derived from the value of the last transfer cycle.

Example

A difference of 3 to the last transfer cycle means:

The data in sample line 1 and all subsequent data from the previous transfer cycle is now shifted in the current cycle beginning with sample line 4. Sample lines 1 through 3 contain the new values for further processing by the application. Sample lines 14 through 16 from the last transfer cycle are no longer in the buffer.

4.3.11.8.5.2 Comparator oversampling

When using comparator oversampling, the results of the enabled channels are stored in the module within a configurable time frame independently of the X2X cycle. 16 bits of memory space are available per logical channel.

These samplings (i.e. event bits) are consecutively numbered from 1 to 8 and 9 to 16 for the two registers. The results of individual channels with the same number (i.e. sample line 1 to 16, e.g. for channel 1 LogicCh01Sample**16_9** and LogicCh01Sample**8_1**) are derived from the same sampling cycle or logical computing cycle and therefore have the same timestamp.

The timestamp refers to the newest data value, i.e. always to sample line 1 (i.e. bit 0 in the LogicCh01Sample8_1 register). If a timestamp for older comparator results is needed, it needs to be back-calculated in the application using the sampling cycle time configured on the module. The prescaler must also be taken into account.

Calculation example

Sample line	(register name)	Calculation	
1	(LogicCh01Sample8_1 bit 0)	Timestamp	**Newest value**
2	(LogicCh01Sample8_1 bit 1)	Timestamp - Sampling cycle time	
3	(LogicCh01Sample8_1 bit 2)	Timestamp - 2 * Sampling cycle time	
4	(LogicCh01Sample8_1 bit 3)	Timestamp - 3 * Sampling cycle time	
...			
10	(LogicCh01Sample16_9 bit 1)	Timestamp - 9 * Sampling cycle time	
...			
16	(LogicCh01Sample16_9 bit 7)	Timestamp - 15 * Sampling cycle time	**Oldest value**

How the buffer is organized can be seen from this. This is not a FIFO buffer but a static buffer that the values are pushed through. Sample line 1 always contains the newest values, the next line the second newest, all the way up to sample line 16, which contains the oldest values.

The sample counter is a circular counter, with the number of new sample lines derived from the value of the last transfer cycle.

Example

A difference of 3 to the last transfer cycle means:

The comparator result in sample line 1 and all subsequent data from the previous transfer cycle is now shifted in the current cycle beginning with sample line 4. Sample lines 1 through 3 contain the new bit values for further processing by the application. Sample lines 14 through 16 from the last transfer cycle are no longer in the buffer.

Data transfer

The analog conversion rate / sampling cycle time can be considerably faster than the X2X Link cycle. Saved analog or comparator data can be transferred to the higher-level system synchronously and consistently.

In the application, it's important that the relationship between cyclic data points, the sampling cycle time on the module and the transfer time is sufficient to read all of the new data points on the higher-level system.

The sample counter can be used to check how many data values are actually new since the last transfer cycle. If the counter difference to the previous cycle is larger than the number of existing cyclic data points, then values have been overlooked and the system needs to be adjusted.

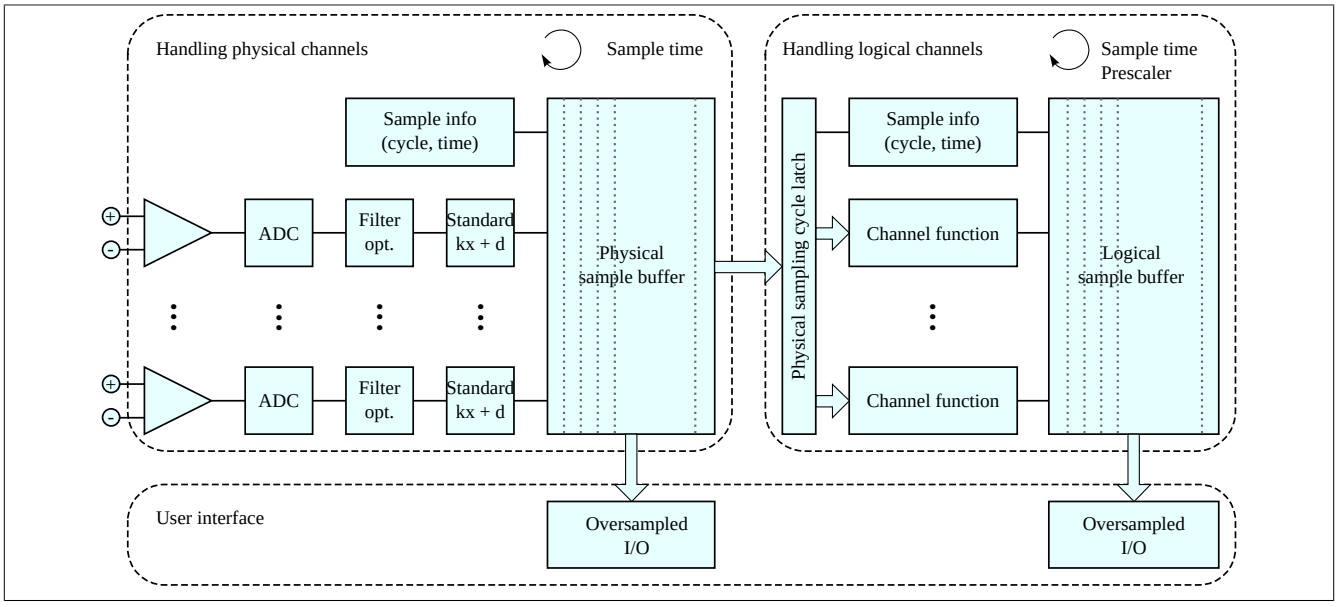
The general guideline is that a cyclic data point should be configured more than is actually required computing-wise.

Example with synchronous settings

- Sampling cycle time = 50 µs
- X2X Link cycle time = 500 µs

Samples 1 to 10 of a channel are possible to calculate in this example. Sample 11 should also be configured as a cyclic data point, however.
The reason for this is the possible jitter in the module caused by interruptions, e.g. from the X2X Link transfer. For the current cycle, this can mean that only 9 new values are available and that 11 values will have to be transferred in the next cycle.

For logical comparator functions, this problem doesn't exist since the maximum number is always transferred in the cycle data range.



4.3.11.8.6 Bus controller operating mode

The input values are recorded with a configurable sampling cycle time and saved with timestamp to the internal physical data buffer. Only the newest value will be transferred in the next possible bus cycle.

Limitations in the bus controller function model:

- No oversampling function since consistency is not possible due to the limited data range
- Sampling cycle time configured to 100 µs by default
- Range of logical functions available for processing physical values directly on the module
- Timestamp not available

4.3.11.8.7 "AnalogInput" registers

Name:
AnalogInput01 to AnalogInput02

This module can be configured and operated as a normal analog input module without logical auxiliary functions. The physical values from the last sampling cycle are used as input values in this case.

The module is operated as a normal analog input module in the bus controller function model. Nevertheless, it is still possible to connect each input channel directly to a logical function. The analog data on the bus controller is mapped using the calculation abilities of the logical channels and configured automatically (see 4.3.11.8.14.2 "Operation in the bus controller function model ").

Analog input values are displayed as signed 16-bit values depending on the configured operating mode.

Data type	Value	Information
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 mA to 20 mA

Information:

It is important to note that the oversampling function is not available in the bus controller function model due to the amount of data and lack of consistency!

4.3.11.8.8 Physical sampling

This module has a data buffer with 16 entries for each of the physical input channels. This buffer is processed according to the configured sampling cycle time.

A maximum of only 30 bytes is available for cyclic transfer on the X2X bus, however. Minus the status and sample counter, this allows only a selection of 14 samples (with a 16-bit data width) from the physical and logical buffer to be transferred.
Data loss can therefore occur with an imprecise selection and configuration.

Example

Displaying continuous sample lines.

- Sampling cycle time = 100 µs
- X2X cycle time = 500 µs

Sample line 1	PhysCh0xSample1
Sample line 2	PhysCh0xSample2
Sample line 3	PhysCh0xSample3
Sample line 4	PhysCh0xSample4
Sample line 5	PhysCh0xSample5
Sample line 6	PhysCh0xSample6
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 2	New values in sample line 1 and sample line 2
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5

Information:

It is important to note that the sample counter refers to the update of the sample lines in the data buffer and not to the number of values transferred cyclically.

Displaying each second sample line to bridge a higher recording duration:

- Sampling cycle time = 100 µs
- X2X cycle time = 1000 µs

Sample line 1	PhysCh0xSample1
Sample line 3	PhysCh0xSample3
Sample line 5	PhysCh0xSample5
Sample line 7	PhysCh0xSample7
Sample line 9	PhysCh0xSample9
Sample line 11	PhysCh0xSample11
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 3	New values in sample line 1 and sample line 3
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5
...	
Difference SampleCount = 9	New values in sample line 1 to sample line 9

4.3.11.8.8.1 "PhysChSample" registers

Name:
PhysCh01Sample1 to PhysCh01Sample16
PhysCh02Sample1 to PhysCh02Sample16

These registers are the physical buffer registers of the analog channels. 16 registers are available for each channel. Sample 1 is the newest value; sample 16 is the oldest.

Data type	Value	Information
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 mA to 20 mA

4.3.11.8.8.2 "PhysSampleCount" register

Name:
PhysSampleCount

This register is an integer counter that is increased as soon as the module has saved a new physical sample line. The number of new sample lines is calculated from the difference to the previous cycle.

Data type	Value
SINT	-128 to 127
INT	-32,768 to 32,767

4.3.11.8.8.3 "PhysTimestamp" register

Name:
PhysTimestamp

This register returns the timestamp of the values currently being determined as signed values in µs. This data point is the timestamp of the physical sample line 1.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.3.11.8.9 Logical sampling

The module has a data buffer with 16 entries for each of the 6 logical channels. This buffer is processed according to the configured sampling cycle time. In addition, it's also possible to adjust the logical execution cycle using a prescaler for the sampling cycle time.

A maximum of only 30 bytes is available for cyclic transfer on the X2X bus, however. Minus the status and sample counter, this allows only a selection of 14 samples (with a 16-bit data width) from the physical and logical buffer to be transferred. For the logical channels, it is also possible to configure a 32-bit data width.
Data loss can therefore occur with an imprecise selection and configuration.

Example

Displaying continuous sample lines.

- Sampling cycle time = 100 µs
- X2X cycle time = 500 µs

Sample line 1	LogicCh0xSample1
Sample line 2	LogicCh0xSample2
Sample line 3	LogicCh0xSample3
Sample line 4	LogicCh0xSample4
Sample line 5	LogicCh0xSample5
Sample line 6	LogicCh0xSample6
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 2	New values in sample line 1 and sample line 2
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5

Information:

It is important to note that the sample counter refers to the update of the sample lines in the data buffer and not to the number of values transferred cyclically.

Displaying each second sample line to bridge a higher recording duration:

- Sampling cycle time = 100 µs
- X2X cycle time = 1000 µs

Sample line 1	LogicCh0xSample1
Sample line 3	LogicCh0xSample3
Sample line 5	LogicCh0xSample5
Sample line 7	LogicCh0xSample7
Sample line 9	LogicCh0xSample9
Sample line 11	LogicCh0xSample11
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 3	New values in sample line 1 and sample line 3
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5
...	
Difference SampleCount = 9	New values in sample line 1 to sample line 9

4.3.11.8.9.1 "LogicChSample" registers

Name:
LogicCh01Sample1 to LogicCh01Sample16
...
LogicCh06Sample1 to LogicCh06Sample16

These registers are the buffer registers of the logical input channels. 16 registers are available for each channel. Sample 1 is the newest value; sample 16 is the oldest.

Calculated values are displayed as signed 16- or 32-bit values depending on the register being used.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.3.11.8.9.2 "LogicChSample16_9" registers

Name:
LogicCh01Sample16_9 to LogicCh06Sample16_9

These registers are used to represent the results of samples 9 to 16 of the logical digital comparator for the logical channels. Each of these bits corresponds to a sample line, with sample 9 the newest and Sample 16 the oldest comparator comparison. The results of samples 1 to 8 are represented in 4.3.11.8.9.3 ""LogicChSample8_1" registers".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator result	x	Sample 9
...	...		
7	Comparator result	x	Sample 16

4.3.11.8.9.3 "LogicChSample8_1" registers

Name:
LogicCh01Sample8_1 to LogicCh06Sample8_1

These registers are used to represent the results of samples 1 to 8 of the logical digital comparator for the logical channels. Each of these bits corresponds to a sample line, with sample 1 the newest and Sample 8 the oldest comparator comparison. The results of samples 9 to 16 are represented in 4.3.11.8.9.2 ""LogicChSample16_9" registers".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator result	x	Sample 1
...	...		
7	Comparator result	x	Sample 8

4.3.11.8.9.4 "LogicSampleCount" register

Name:
LogicSampleCount

This register is an integer counter that is increased as soon as the module has saved a new logical sample line. The number of new sample lines is calculated from the difference to the previous cycle.

Data type	Value
SINT	-128 to 127
INT	-32,768 to 32,767

4.3.11.8.9.5 "LogicTimestamp" register

Name:
LogicTimestamp

This register returns the timestamp of the values currently being determined as signed 2 or 4-byte values in µs. This data point is the timestamp of the logical sample line 1.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.3.11.8.10 System configuration

The following registers are used to configure the module's system settings.

4.3.11.8.10.1 Register "CfO_BaseConfig"

Name:
CfO_BaseConfig

This register can be used to configure settings for handling logical oversampling and data acquisition.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	"Display configuration for logical values active/inactive" in the AS I/O configuration	0	Inactive
		1	Active
1	"Logical handling priority" in the AS I/O configuration	0	Low
		1	High
2 - 3	Reserved	-	
4	"Physical input mode" in the AS I/O configuration	0	Newest value
		1	Referenced value (reference = prescaled system timer)
5	"Logical input mode" in the AS I/O configuration	0	Newest value
		1	Referenced value (reference = prescaled system timer)
6 - 7	Reserved	-	

Priority of logical oversampling

- Low priority setting
  Logical and physical buffers are not processed in the same context. If the calculation time that results in the logical oversampling is higher than the configured sampling cycle time, this setting and a prescaler > 1 can be used to split up the logical processing over several sampling cycles. In this way, the sample lines of the physical and logical oversampling are not automatically acquired or calculated at the same point in time. If the prescaler is configured incorrectly, the logical oversampling cannot be processed successfully.
- High priority setting
  Logical and physical buffers are processed in the same context. The sample lines of the physical and logical oversampling are acquired and calculated at the same point in time. It must be possible to execute all configured functions in the configured sampling cycle time; otherwise, a cycle time violation will occur and the configuration must be changed accordingly. Configuring the logical prescaler doesn't have any effect here; only the data traffic in the logical oversampling is limited.

Current or referenced values for logical or physical oversampling

In a system being used to capacity, jitter in the sampling cycle on the module can also be caused by the necessary processing of functions (X2X Link operation, logical and physical oversampling) when the cycle time is set to synchronous. This results in a varying number of sample lines in the same time period. For this reason, more samples should also be configured in the cyclic image than are actually necessary to compute.

- Current values setting
  Passing on the sample lines to the higher-level system takes place as quickly as possible, with fewer or more sample lines possibly occurring.
- Referenced values setting
  This setting minimizes jitter and makes it possible to expect a constant number of new sample lines per cycle when configured optimally. With regard to response time, however, delays of several sampling cycles may occur.

4.3.11.8.10.2 Register "CfO_CycleTime"

Name:
CfO_CycleTime
"Physical sample time" in the AS I/O configuration.

This register configures the module's sampling cycle time. The format is a 16.16-bit unsigned 4-byte value, with the high word representing the integer part of the µs value and the low word the decimal places. The decimal places allow a closer alignment to the X2X cycle time. The absolute resolution is 1 µs.

Input value = Time in µs * 65536 data type

Data type	Value	Information
UDINT	2,621,440 to 2,147,483,647	40 µs to 32 ms sampling cycle time
	6,553,600	100 µs (default value)

4.3.11.8.10.3 Register "CfO_Prescaler"

Name:
CfO_Prescaler

This register contains the prescaler for configuring the logical channel processing time. The actual logical cycle time will be calculated from the multiple of the sampling cycle time that is defined here. If a very short sampling cycle time is required for physical samples, then the module load can be reduced using the second time base for the logical samples.

Data type	Value	Information
UINT	1 to 10	Multiple of the physical sampling cycle for logical processing
	0	Default value in the standard function model
	2	Default value in the bus controller function model

4.3.11.8.10.4 Register "CfO_SyncOffset"

Name:
CfO_SyncOffset
"Synchronization offset" in the AS I/O configuration.

The system cycle can be offset in 1 µs steps in this register.

Data type	Value	Information
UINT	-32,768 to 32,767	Synchronization offset in µs (default = 0)

4.3.11.8.11 Scaling

Analog input channels are naturally aligned and normalized when delivered (gain = k, offset = d). In addition, user-defined normalization is also available (gain = ku, offset = du). The calculation is optimized by grouping the factors together.

Normalization calculation:

nom = k * RawValue + d

k = k * ku

d = k * d + du

The values calculated here are limited to 16 bits.

4.3.11.8.11.1 "CfO_UserGainCh" registers

Name:
CfO_UserGainCh01 to CfO_UserGainCh02
"Configuration channel 0x / gain" in the AS I/O configuration

These registers are used to configure the gain for the respective channel. The format is a 16.16-bit signed 4-byte value, with the high word the integer part and the low word the decimal places.

Input value = Gain ku * 65536

The value 0x10000 corresponds to a gain of 1.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Gain
	65,535	= 1 (default value)

4.3.11.8.11.2 "CfO_UserOffsetCh" registers

Name:
CfO_UserOffsetCh01 to CfO_UserOffsetCh02
"Configuration channel 0x / offset" in the AS I/O configuration

These registers are used to configure the offset for the respective channel. The format is a 16.16-bit signed 4-byte value, with the high word the integer part and the low word the decimal places.

Input value = Offset du * 65536

The value 0x10000 corresponds to an offset of 1.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Offset (default = 0)

4.3.11.8.12 Input filter

This module is equipped with an individually configurable input filter for each channel. The following filters can be selected:

- 1st-order low pass
- 2nd-order low pass
- 2nd-order IIR

The cutoff frequency can be configured for the 1st-order and 2nd-order low pass filters. The coefficients Alpha0, Alpha1, Alpha2, Beta1 and Beta2 must be configured for the IIR filter.

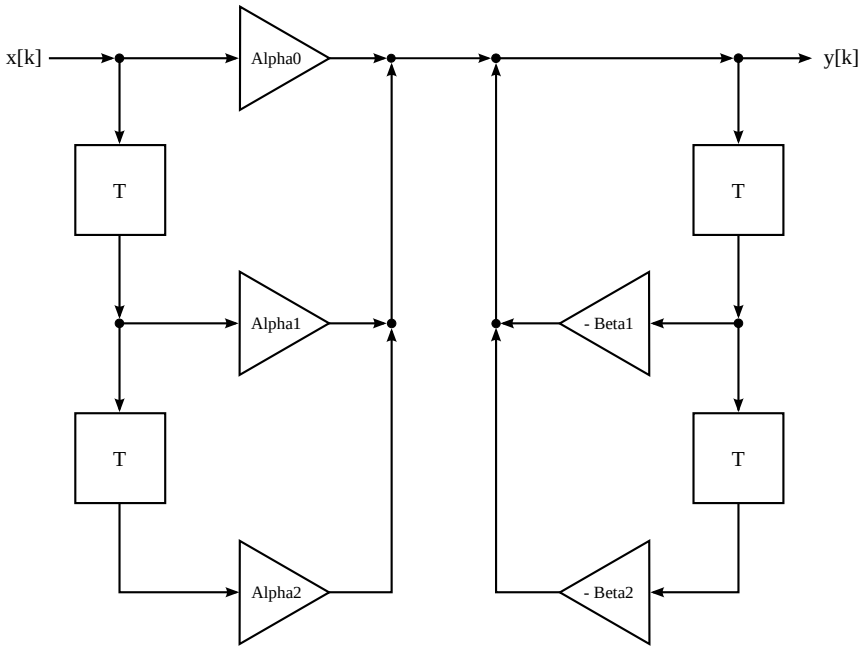
4.3.11.8.12.1 "CfO_AlphaCh" and "CfO_BetaCh" registers

Name:
CfO_Alpha0Ch01 to CfO_Alpha0Ch02
CfO_Alpha1Ch01 to CfO_Alpha1Ch02
CfO_Alpha2Ch01 to CfO_Alpha2Ch02
CfO_Beta1Ch01 to CfO_Beta1Ch02
CfO_Beta1Ch01 to CfO_Beta1Ch02

These registers are used to configure the coefficients for the IIR filter.

Image as a z-transfer function

The 2nd-order z-transfer function is specified in coefficient form (denominator polynomial Beta1, Beta2 and numerator polynomial Alpha0, Alpha1, Alpha2). The transfer method is calculated with the sampling cycle time.



Data type	Value	
DINT	-2,147,483,648 to 2,147,483,647	IIR filter coefficient (default = 0)

4.3.11.8.12.2 "CfO_CutOffFrequCh" register

Name:
CfO_CutOffFrequCh01 to CfO_CutOffFrequCh02

These registers are used to configure the limit frequency in hertz for a 1st- or 2nd-order low pass for the corresponding channel.

Data type	Value	Information
UINT	0 to 65535	Limit frequency for 1st- or 2nd-order low pass [Hz] (default = 0)

4.3.11.8.13 Physical configuration

4.3.11.8.13.1 "CfO_ModeCh" registers

Name:
CfO_ModeCh01 to CfO_ModeCh02

The operating mode for each physical channel can be configured in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Connection configuration **This value must be set the same for each register!**	000	Voltage signal
		111	Current signal
3 - 7	Reserved	0	
8 - 10	Operating mode	000	Channel disabled
		001	No filtering
		010	2nd-order IIR (configurableAlpha and Beta coefficients)
		011	1st-order low pass (configurable limit frequency)
		100	2nd-order low pass (configurable limit frequency)
		101 to 111	Reserved
11 - 15	Reserved	0	

4.3.11.8.14 Logical configuration

4.3.11.8.14.1 Operation in the standard function model

6 logical channels are available on the module. Each channel can be configured with one of the following functions:

- Addition of two channels with scaling
- Integral addition of two channels with scaling
- Multiplication of two channels with scaling
- Integral multiplication of two channels with scaling
- Comparator function of two channels
- Hysteresis comparator of one channel

With logical oversampling, 32-bit data points are available in addition to 16-bit data points due to the possible calculated results. The AS I/O configuration or data point mapping can be opened to select which one to use.

If there is no need to use 32-bit data points, or if this would lead to too large of a limitation in the number of data points, scaling can be used to limit the range to 16 bits.

The buffer depth for the digital comparator is also able to handle 16 results. Since these are Boolean results, these 16 bits are compressed into 2-byte data points and transferred that way.

Addition

This function can be used to determine the sum or difference of two channels. To determine the difference, negative scaling needs to be configured for the channel.

Calculation

Sample line = (Channel 1 * Scaling 1) + (Channel 2 * Scaling 2)

The addition calculation is handled internally as a 32-bit value in 16.16 format; the data from the source channels is evaluated as integers (applied to the high word), with decimal places possible as a result of scaling. When displayed as a logical 32-bit result, these decimal places are visible. When displayed as a 16-bit value, only the integral high word is used.

Example

Channel 1 = 2000
Channel 2 = 1000
Both scalings = 1

Results

3000.x = (2000.x * 1,0) + (1000.x * 1.0)
32-bit representation = 196608000 = 0xBB80000
16-bit representation = 3000 = 0xBB8

Information:

The maximum value channel 1 can take on is 32767; otherwise, an addition overflow occurs. If values greater than 32767 are possible, the value range must be limited with scaling.

Integral of addition

This function can be used in the application to establish the average value of the channels or to calculate the deviation/difference between two channels over n samples. In each cycle, the channels are added together first; then the result is added to the previous value and saved in the current sample line. Depending on the result data type being used (16-bit or 32-bit), eventually the continuous integration will cause the calculation to overflow after n samples. Because the result value is signed, it is important to set the number n of samples small enough so that the integration is less than half of the value range. If this is done, determining the average value can be carried out despite an overflow.

Calculation

Sample line result = Integral ((Channel 1 * Scaling 1) + (Channel 2 * Scaling 2))

The addition calculation is handled internally as a 32-bit value in 16.16 format; the data from the source channels is evaluated as integers (applied to the high word), with decimal places possible as a result of scaling. When displayed as a logical 32-bit result, these decimal places are visible. When displayed as a 16-bit value, only the integral high word is used.

Example

Channel 1 = 2000
Channel 2 = 1000
Both scalings = 1

Results

3000.x = (2000.x * 1,0) + (1000.x * 1.0)
32-bit representation = 196608000 = 0xBB80000
16-bit representation = 3000 = 0xBB8

The average value can now be calculated as follows:

n = Number of samples / sample lines
$Value_x$ = Value from sample line x → Newer value
$Value_x$ = Value from sample line x → Older value, n samples back

Average value = $(Value_x - Value_{(x-n)}) / n$

Information:

The maximum value channel 1 can take on is 32767; otherwise, an addition overflow occurs. If values greater than 32767 are possible, the value range must be limited with scaling.

Multiplication

This function can be used to calculate the current effective power P = U * I.

Calculation

Sample line = Channel 1 * Channel 2 * Scaling

Multiplication is calculated internally as a 32-bit value; the 16-bit data from the source channels is passed to the low word. When displayed as a logical 32-bit value, the entire result is visible (no multiplication overflow possible when scaling ≤1). When displayed as a 16-bit value, only the high word is used. Though there is a loss of precision, the 16-bit values allow more data points to be transferred.

Example

Channel 1 = 2000
Channel 2 = 1000
Scaling = 1

Results

2000000 = (2000 * 1000 * 1.0)
32-bit representation = 2000000 = 0x1E8480
16-bit representation = 30 = 0x1E

Information:

If more precision is needed with the 16-bit value, scaling in steps of 2^n (..., *128, *256, ...) can be employed to shift the bits. Of course, it's important again that the input values of the source channels be limited; otherwise, an overflow will occur in the multiplication operation.

Integral of multiplication

This function can be used in the application to establish the average value of the effective power. In each cycle, the channels are multiplied together first; then the result is added to the previous value and saved in the current sample line. Depending on the result data type being used (16-bit or 32-bit), eventually the continuous integration will cause the calculation to overflow after n samples. Because the result value is signed, it is important to set the number n of samples small enough so that the integration is less than half of the value range. If this is done, determining the average value can be carried out despite an overflow.

Calculation

Sample line = Integral (Channel 1 * Channel 2 * Scaling)

Multiplication is calculated internally as a 32-bit value; the 16-bit data from the source channels is passed to the low word. When displayed as a logical 32-bit value, the entire result is visible (no multiplication overflow possible when scaling ≤1). When displayed as a 16-bit value, only the high word is used. Though there is a loss of precision, the 16-bit values allow more data points to be transferred.

Example

Channel 1 = 2000
Channel 2 = 1000
Scaling = 1

Results

2000000 = (2000 * 1000 * 1.0)
32-bit representation = 2000000 = 0x1E8480
16-bit representation = 30 = 0x1E

The average value can now be calculated as follows:

n = Number of samples / sample lines
$Value_x$ = Value from sample line x → Newer value
$Value_x$ = Value from sample line x → Older value, n samples back

Average value = $(Value_x - Value_{(x-n)}) / n$

Information:

If more precision is needed with the 16-bit value, scaling in steps of 2^n (..., *128, *256, ...) can be employed to shift the bits. Of course, it's important again that the input values of the source channels be limited; otherwise, an overflow will occur in the multiplication operation.

Channel comparator

This function can be used to compare channel values. The following applies:

- Channel 1 > Channel 2 = 1
- Channel 1 < Channel 2 = 0
- Channel 1 = Channel 2 = State before values are the same

Calculation

Sample line (bit) = Comparison (channel value 1 with channel value 2)

Hysteresis comparator

This function can be used to monitor range violations by channels. The following applies:

- Channel > Upper threshold value = 1
- Channel < Lower threshold value = 0
- Channel within threshold = Value before occurrence

Calculation

Sample line (bit) = Comparison (channel value with lower threshold value) and (channel value with upper threshold value))

4.3.11.8.14.2 Operation in the bus controller function model

When used on the bus controller, there are 4 logical functions available for each of the analog input channels in addition to the physical value output. Each channel can be configured with one of the following functions:

- Output of physical values (default setting)
- Addition of two channels with scaling
- Integral addition of two channels with scaling
- Multiplication of two channels with scaling
- Integral multiplication of two channels with scaling
- Comparator function of two channels
- Hysteresis comparator of one channel

In contrast to the standard function model, oversampling and the two digital comparators are not supported. As a result, there is only one newly generated value per channel in each update cycle. Another difference is that there are only 4 logical calculation channels instead of 6.

The logical functions addition, integral of addition, multiplication and integral of multiplication do not differ from the standard function model in their configuration and function when operating on the bus controller.

Physical value display

The physical value display in the bus controller function model is initialized automatically and represents a special form of the logical function "Addition" with defined scaling factors.

Calculation

Result = Channel value
Formula used for addition: Result = (Channel value 1 * 1) + (Channel value 2 * 0)

Information:

In this function model, only the 4 physical input channels are available, and the scaling factors have defined values.

4.3.11.8.14.3 "CfO_LogChMode" register

Name:
CfO_LogCh01Mode to CfO_LogCh06Mode
"Logical configuration channel 0x / Addition" in the AS I/O configuration.
"Logical configuration channel 0x / Integral of addition" in the AS I/O configuration.
"Logical configuration channel 0x / Multiplication" in the AS I/O configuration.
"Logical configuration channel 0x / Integral of multiplication" in the AS I/O configuration.
"Logical configuration channel 0x / Channel comparator" in the AS I/O configuration.
"Logical configuration channel 0x / Hysteresis comparator" in the AS I/O configuration.
"Logical configuration channel 0x / Physical value display" in the AS I/O configuration.

The operating mode for each logical channel can be configured in this register.

The selection of the sources to be used for each logical channel is made using the register 4.3.11.8.14.4 "CfO_LogCh0NSource0x". Any additionally needed function parameters are configured in the 4.3.11.8.14.5 "CfO_LogCh0NFuncPar0x" registers. "N" stands for the logical channel to be used, while "x" stands for either the source or function 0 or 1.

The following links can be made:

- Addition: Result = (Source 0 * Function parameter 0) + (Source 1 * Function parameter 1)
- Integral of addition: Result = Σ(Source 0 * Function parameter 0) + (Source 1 * Function parameter 1)
- Multiplication: Result = Source 0 * Source 1 * Function parameter 0
- Integral of multiplication: Result = Σ(Source 0 * Source 1 * Function parameter 0)
- Channel comparator: Result = Comparison of source 0 with source 1
- Hysteresis comparator: Result = comparison of source 0 with (Lower threshold value = Function parameter 0) and (Upper threshold value = Function parameter 1)
- Physical value display: Result = (Source 0 * 1) + (Source 1 * 0)

Data type	Value	Information
UINT	0	Channel switched off (default)
	256	Addition or physical value display[1)]
	257	Integral of addition
	512	Multiplication
	513	Integral of multiplication
	768	Channel comparator
	1024	Hysteresis comparator

1) Only registers CfO_LogCh01Mode to CfO_LogCh04Mode are used for physical value display.

4.3.11.8.14.4 "CfO_LogChSource" register

Name:
CfO_LogCh01Source00 to CfO_LogCh06Source00
CfO_LogCh01Source01 to CfO_LogCh06Source01

These registers can be used to select the source registers for the operating mode of the logical channel configured in the register 4.3.11.8.14.3 "CfO_LogCh0NMode".
In the name, "Source00" stands for source register 0; "Source01" stands for source register 1.

In "Physical value display" mode, the same channel number is written to both source registers.

Data type	Value	Information
USINT	0	Physical channel 01
	1	Physical channel 02
	8	Logical channel 01[1)]
	...	...
	13	Logical channel 06

1) Logical channels cannot be used in the bus controller function model.

4.3.11.8.14.5 "CfO_LogChFuncPar" register

Name:
CfO_LogCh01FuncPar00 to CfO_LogCh06FuncPar00
CfO_LogCh01FuncPar01 to CfO_LogCh06FuncPar01

These registers can be used to configure additional function parameters for the operating mode of the logical channel configured in the register 4.3.11.8.14.3 "CfO_LogCh0NMode".

The effect of the function parameters is different depending on the operating mode.

Operating mode	Parameter 1	Parameter 2
(Integral of) addition	Scaling factor	Scaling factor
(Integral of) multiplication	Scaling factor	-
Channel comparator	-	-
Hysteresis comparator	Upper threshold value	Lower threshold value
Output of physical values	Defined scaling factor = 65,536	Defined scaling factor = 0

The value 0x10000 (65,536) corresponds to a scaling or a threshold value of 1.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Scaling factor or threshold value
	0	Default
	65,536	1

4.3.11.8.15 Error registers

The registers for displaying and acknowledging errors are transferred either cyclically or acyclically depending on the function model.

4.3.11.8.15.1 "CfO_ErrorID1017" register

Name:
CfO_ErrorID1017
Automatic enabling by the AS I/O configuration.

This register can be used to enable standard error messages. The channels' composite errors are derived from the individual extended error status, e.g. overflow/underflow of the input range for the analog value. Oversampling error statuses result from a cycle time violation of the configured sampling cycle time.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Composite errors on channel 01	0	Error generation disabled
		1	Error generation enabled
1	Composite errors on channel 02	0	Error generation disabled
		1	Error generation enabled
2 - 3	Reserved	0	
4	Physical sample error status	0	Error generation disabled
		1	Error generation enabled
5	Logical sample error status	0	Error generation disabled
		1	Error generation enabled
6 - 7	Reserved	0	

4.3.11.8.15.2 "CfO_ErrorID0x0x" register

Name:
CfO_ErrorID0007
Automatic enabling in the AS I/O configuration by selecting "Extended error status information" and channel activation.

This register can be used to enable extended error messages for analog channels 1 and 2. Meaning of individual bits:

- **Range exceeded violation (pos.):** The analog input signal is outside of the specified working range.
- **Filter error:** The configured filter theorem cannot be calculated (parameter error).
- **Underflow:** The input signal is less than the lower limit value.
- **Overflow:** The input signal is greater than the upper limit value.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1: Range exceeded violation (pos.)	0	Error generation disabled
		1	Range exceeded violation (pos.) enabled
1	Channel 1: Filter error	0	Error generation disabled
		1	Filter error enabled
2	Channel 1: Underflow	0	Error generation disabled
		1	Underflow enabled
3	Channel 1: Overrun	0	Error generation disabled
		1	Overflow enabled
4	Channel 2: Range exceeded violation (pos.)	0	Error generation disabled
		1	Range exceeded violation (pos.) enabled
5	Channel 2: Filter error	0	Error generation disabled
		1	Filter error enabled
6	Channel 2: Underflow	0	Error generation disabled
		1	Underflow enabled
7	Channel 2: Overrun	0	Error generation disabled
		1	Overflow enabled

4.3.11.8.15.3 "StandardErrors" registers

Name:
Channel01Error to Channel02Error
PhysicalError
LogicalError

Composite errors are mapped to this register.

All configured functions of the physical and logical oversampling must be able to be carried out in the configured sampling cycle time; otherwise, these error messages occur. Settings for processing priority and the prescaler can be used to additionally adjust the system for logical oversampling.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01Error	0	No error
		1	Composite errors on channel 1
1	Channel02Error	0	No error
		1	Composite errors on channel 2
2 - 3	Reserved	0	
4	PhysicalError	0	No error
		1	Physical sample error status, sampling cycle time too short
5	LogicalError	0	No error
		1	Logical sample error status, sampling cycle time too short or prescaler configured too low
6 - 7	Reserved	0	

4.3.11.8.15.4 "AcknowledgeStandardErrors" registers

Name:
AckChannel01Error to AckChannel02Error
AckPhysicalError
AckLogicalError

Error messages from the 4.3.11.8.15.3 ""StandardErrors" registers" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	AckChannel01Error	0	No change
		1	Acknowledge error
1	AckChannel02Error	0	No change
		1	Acknowledge error
2 - 3	Reserved	0	
4	AckPhysicalError	0	No change
		1	Acknowledge error
5	AckLogicalError	0	No change
		1	Acknowledge error
6 - 7	Reserved	0	

4.3.11.8.15.5 "ExtendedChannelErrorMessages" registers

Name:
Channel01OutOfRange to Channel02OutOfRange
Channel01FilterError to Channel02FilterError
Channel01Underflow to Channel02Underflow
Channel01Overflow to Channel02Overflow

The error states of input channels 1 and 2 are represented in these registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutOfRange	0	No error
		1	Range exceeded violation (pos.) occurred
1	Channel01FilterError	0	No error
		1	Filter error occurred
2	Channel01Underflow	0	No error
		1	Underflow occurred
3	Channel01Overflow	0	No error
		1	Overflow occurred
4	Channel02OutOfRange	0	No error
		1	Range exceeded violation (pos.) occurred
5	Channel02FilterError	0	No error
		1	Filter error occurred
6	Channel02Underflow	0	No error
		1	Underflow occurred
7	Channel02Overflow	0	No error
		1	Overflow occurred

4.3.11.8.15.6 "AcknowledgeExtendedChannelErrorMessages" registers

Name:
AckChannel01OutOfRange to AckChannel02OutOfRange
AckChannel01FilterError to AckChannel02FilterError
AckChannel01Underflow to AckChannel02Underflow
AckChannel01Overflow to AckChannel02Overflow

These registers can be used to acknowledge the error messages from the 4.3.11.8.15.5 "ExtendedChannelErrorMessages" registers by setting the corresponding bit.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	AckChannel01OutOfRange	0	No change
		1	Acknowledge error
1	AckChannel01FilterError	0	No change
		1	Acknowledge error
2	AckChannel01Underflow	0	No change
		1	Acknowledge error
3	AckChannel01Overflow	0	No change
		1	Acknowledge error
4	AckChannel02OutOfRange	0	No change
		1	Acknowledge error
5	AckChannel02FilterError	0	No change
		1	Acknowledge error
6	AckChannel02Underflow	0	No change
		1	Acknowledge error
7	AckChannel02Overflow	0	No change
		1	Acknowledge error

4.3.11.8.16 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.3.11.8.17 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

4.3.12 X20AI4222

4.3.12.1 General information

The module is equipped with 4 inputs with 13-bit (including sign) digital converter resolution. It can be used to capture voltage signals in the range from ±10 V.

- 4 analog inputs ±10 V
- 13-bit digital converter resolution

4.3.12.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI4222	X20 analog input module, 4 inputs, ±10 V, 13-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 50: X20AI4222 - Order data

4.3.12.3 Technical data

Product ID	X20AI4222
Short description	
I/O module	4 analog inputs ±10 V
General information	
B&R ID code	0xCAB1
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W [1]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	±10 V
Input type	Differential input
Digital converter resolution	±12-bit
Conversion time	400 µs for all inputs
Output format	
Data type	INT
Voltage	0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Input impedance in signal range	20 MΩ
Input protection	Protection against wiring with supply voltage
Permitted input signal	Max. ±30 V
Output of the digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz

Table 51: X20AI4222 - Technical data

Product ID	X20AI4222
Max. error at 25°C	
Gain	0.08% 3)
Offset	0.015% 4)
Max. gain drift	0.006 %/°C 3)
Max. offset drift	0.002 %/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.025% 4)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 51: X20AI4222 - Technical data

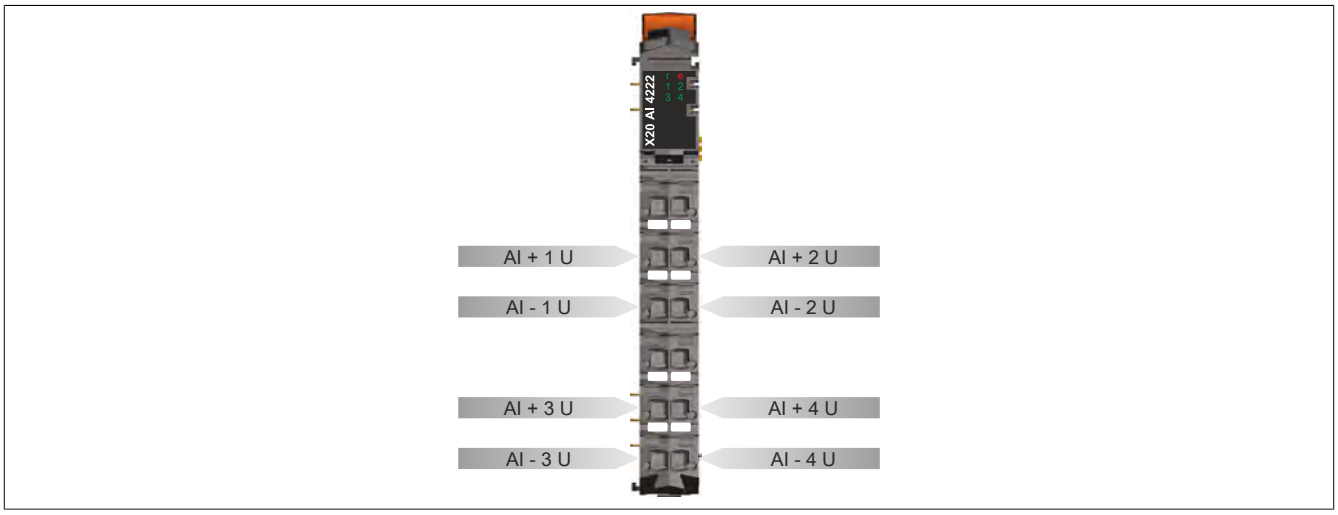
1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 20 V measurement range.

4.3.12.4 LED status indicators

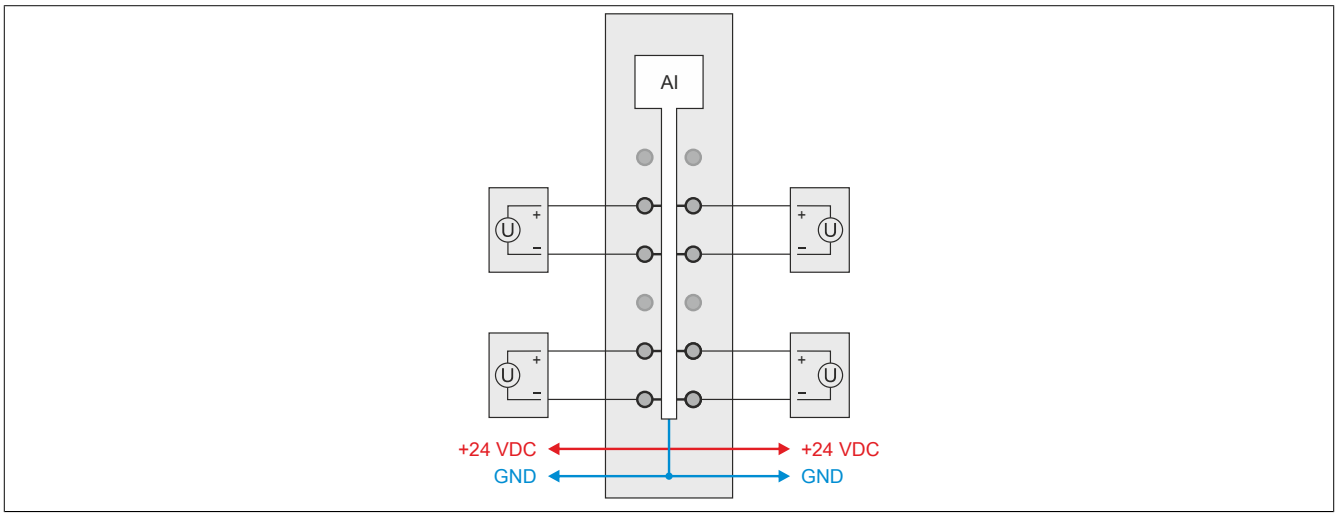
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Off	Open line or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

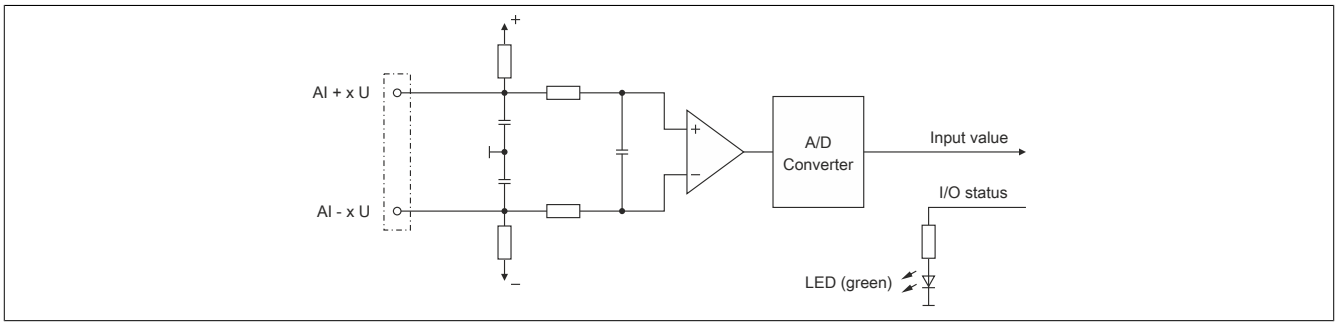
4.3.12.5 Pinout



4.3.12.6 Connection example



4.3.12.7 Input circuit diagram



4.3.12.8 Register description

4.3.12.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.12.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	Configuring the input filter	USINT				•
20	Lower limit value	INT				•
22	Upper limit value	INT				•
Analog signal - Communication						
Index * 2 - 2	AnalogInput0N (Index N = 1 to 4)	INT	•			
30	Input status	USINT	•			

4.3.12.8.3 Function model 254 - Bus controller

Register	Offset	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	Configuring the input filter	USINT				•
20	-	Lower limit value	INT				•
22	-	Upper limit value	INT				•
Analog signal - Communication							
Index * 2 - 2	Index * 2 - 2	AnalogInput0N (Index N = 1 to 4)	INT	•			
30	-	Input status	USINT		•		

1) The offset specifies the position of the register within the CAN object.

4.3.12.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.12.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

4.3.12.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput04

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC

4.3.12.8.6 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the scan rate for the channels is measured in ms. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

4.3.12.8.6.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

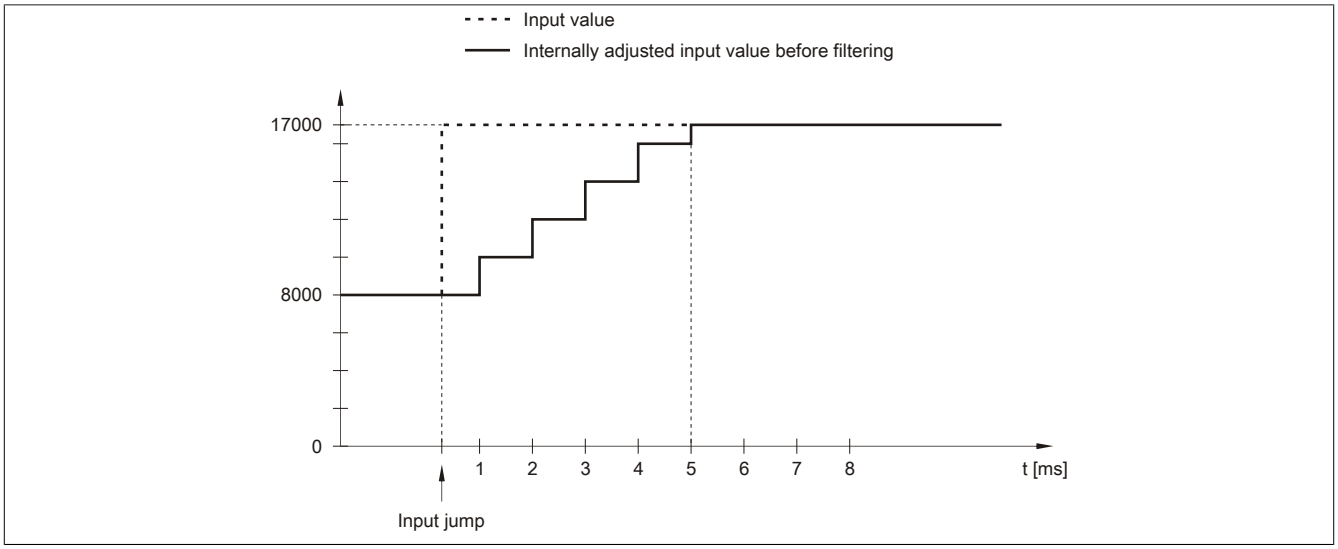


Figure 84: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

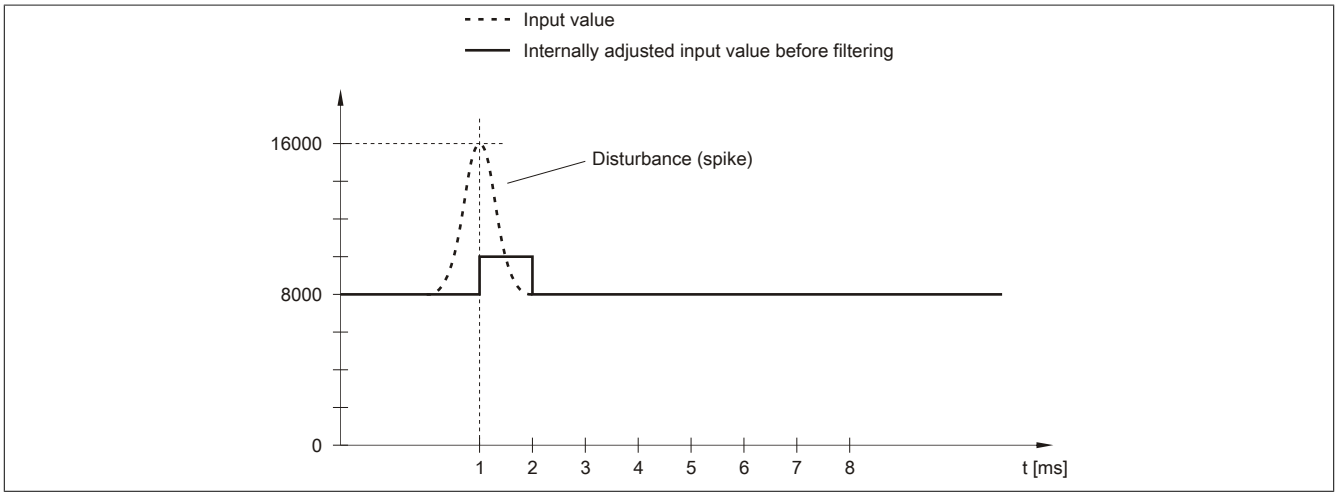


Figure 85: Adjusted input value for disturbance

4.3.12.8.6.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

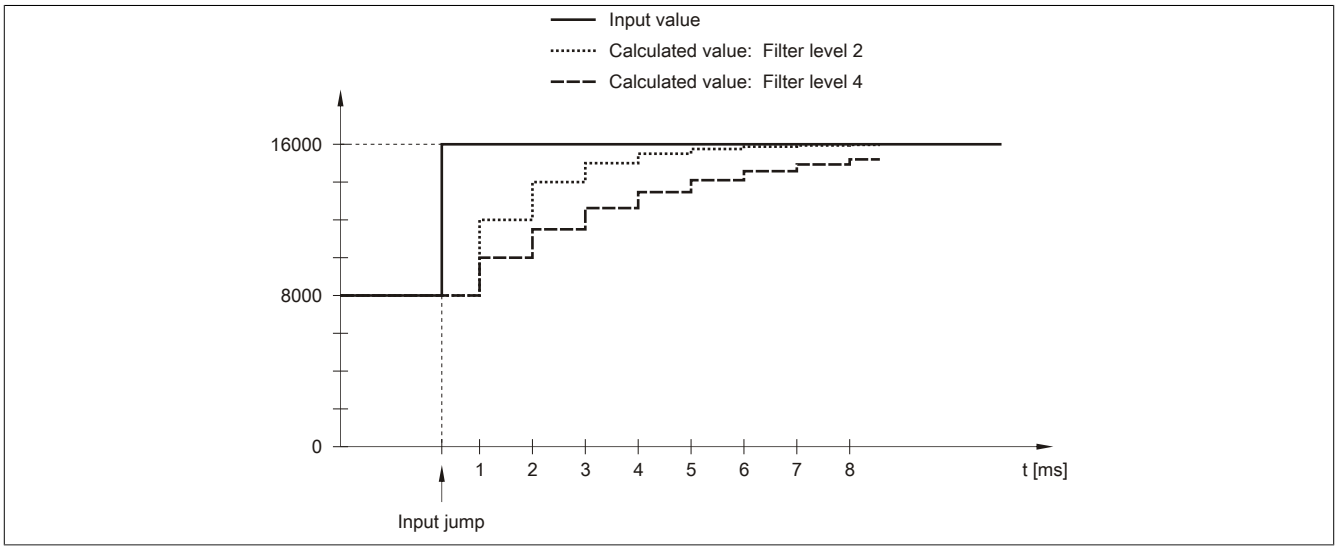


Figure 86: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

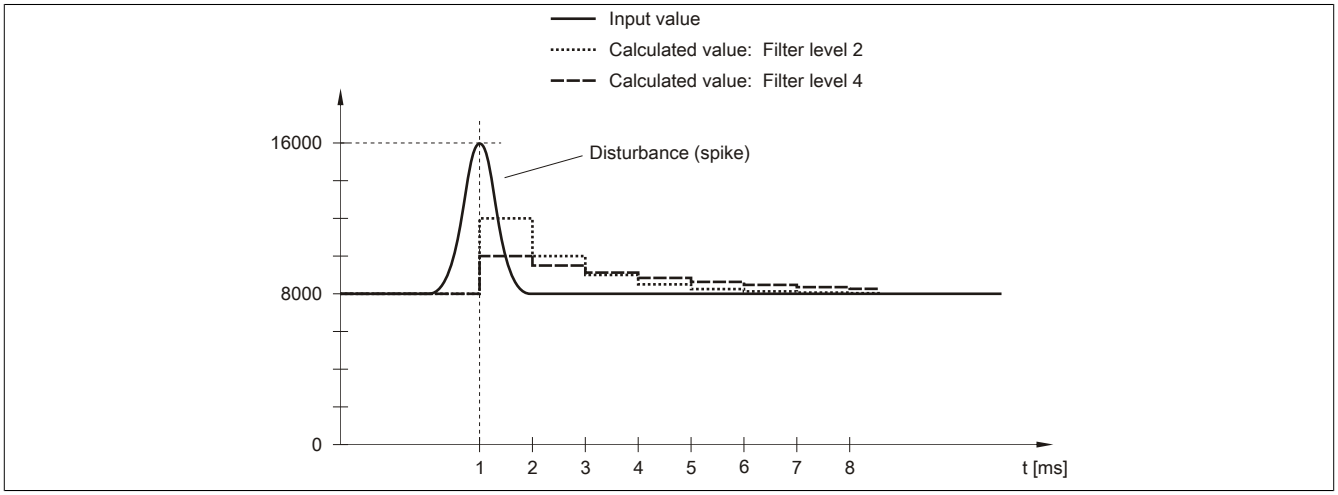


Figure 87: Calculated value during disturbance

4.3.12.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

4.3.12.8.8 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of -32768 corresponds to the minimum default value of -10 VDC.

Keep in mind that this setting applies to all channels!

4.3.12.8.9 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of 32767 corresponds to the maximum default value at +10 VDC.

Keep in mind that this setting applies to all channels!

4.3.12.8.10 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

4.3.12.8.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Inputs without filtering	100 µs
Inputs with filtering	500 µs

4.3.12.8.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Inputs without filtering	400 µs for all inputs
Inputs with filtering	1 ms

4.3.13 X20AI4322

4.3.13.1 General information

The module is equipped with 4 inputs with 12-bit digital converter resolution. It is possible to select between the two current ranges 0 to 20 mA and 4 to 20 mA.

- 4 analog inputs, 0 to 20 mA or 4 to 20 mA
- 12-bit digital converter resolution

4.3.13.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI4322	X20 analog input module, 4 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 52: X20AI4322 - Order data

4.3.13.3 Technical data

Product ID	X20AI4322
Short description	
I/O module	4 analog inputs 0 to 20 mA / 4 to 20 mA
General information	
B&R ID code	0xCAB3
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	0 to 20 mA/4 to 20 mA
Input type	Differential input
Digital converter resolution	12-bit
Conversion time	400 µs for all inputs
Output format	
Data type	INT
Current	0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Load	<400 Ω
Input protection	Protection against wiring with supply voltage
Permitted input signal	Max. ±50 mA
Output of the digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz

Table 53: X20AI4322 - Technical data

Product ID	X20AI4322
Max. error at 25°C	
Gain	
0 to 20 mA	0.08% 2)
4 to 20 mA	0.1% 2)
Offset	
0 to 20 mA	0.03% 3)
4 to 20 mA	0.16% 3)
Max. gain drift	
0 to 20 mA	0.009 %/°C 2)
4 to 20 mA	0.0113 %/°C 2)
Max. offset drift	
0 to 20 mA	0.004 %/°C 3)
4 to 20 mA	0.005 %/°C 3)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.05% 3)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 53: X20AI4322 - Technical data

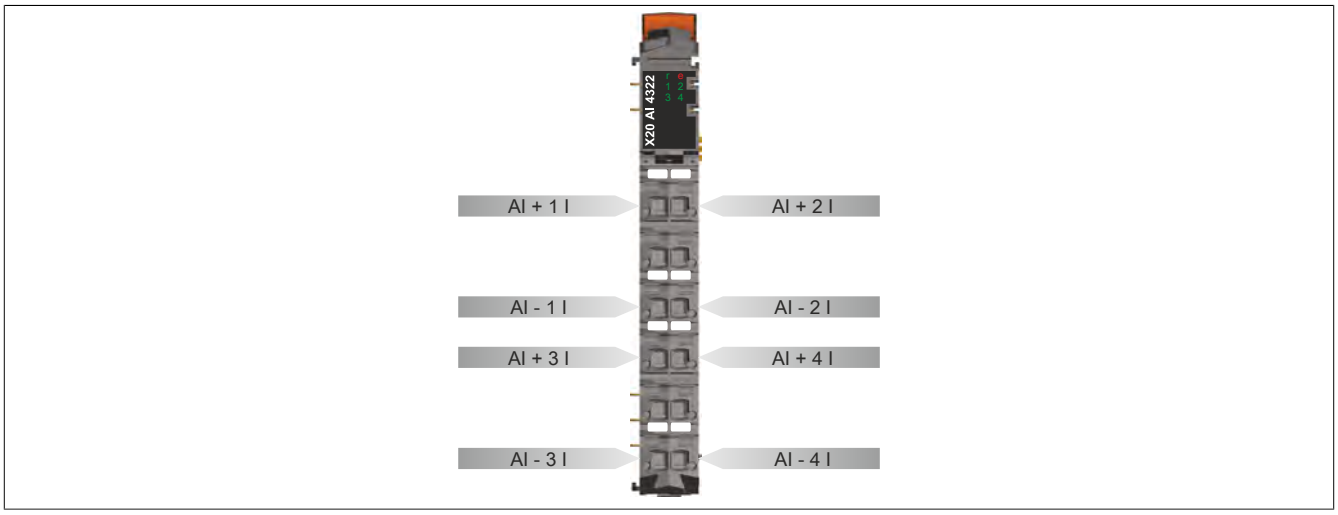
1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current measured value.
3) Based on the 20 mA measurement range.

4.3.13.4 LED status indicators

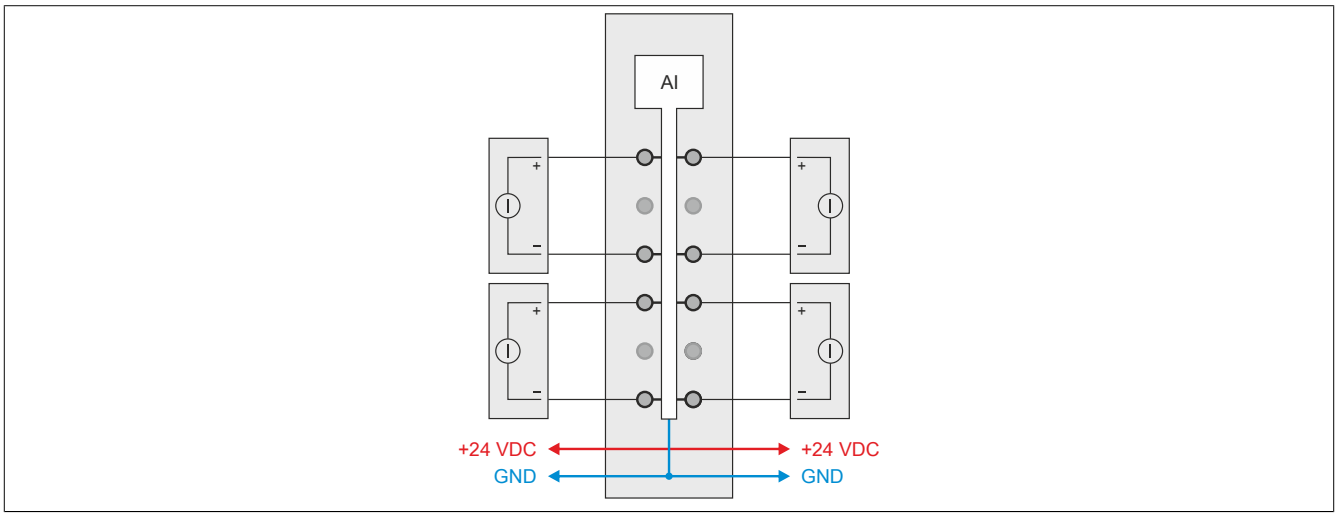
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

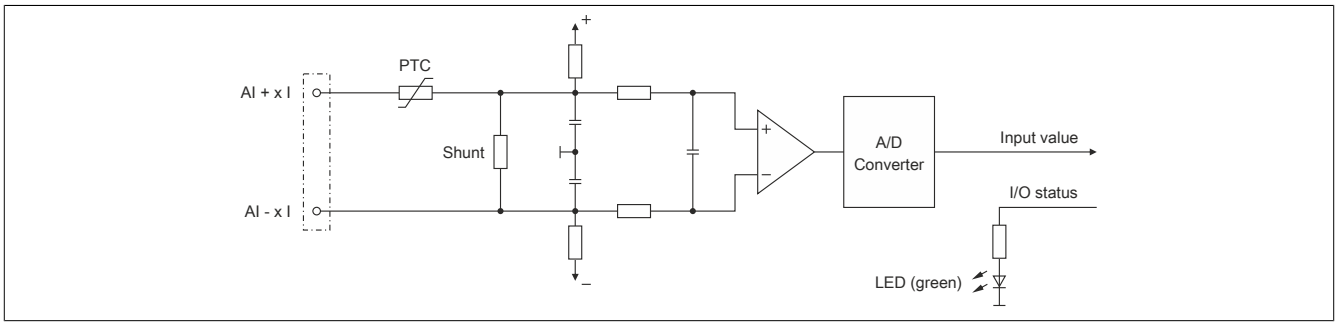
4.3.13.5 Pinout



4.3.13.6 Connection example



4.3.13.7 Input circuit diagram



4.3.13.8 Register description

4.3.13.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.13.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	Configuring the input filter	USINT				●
18	Channel type	USINT				●
20	Lower limit value	INT				●
22	Upper limit value	INT				●
Analog signal - Communication						
Index * 2 - 2	AnalogInput0N (Index N = 1 to 4)	INT	●			
30	Input status	USINT	●			

4.3.13.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	Configuring the input filter	USINT				●
18	-	Channel type	USINT				●
20	-	Lower limit value	INT				●
22	-	Upper limit value	INT				●
Analog signal - Communication							
Index * 2 - 2	Index * 2 - 2	AnalogInput0N (Index N = 1 to 4)	INT	●			
30	-	Input status	USINT		●		

1) The offset specifies the position of the register within the CAN object.

4.3.13.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.13.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

4.3.13.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput04

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	0 to 32767	Current signal 0 to 20 mA or 4 to 20 mA

4.3.13.8.6 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the scan rate for the channels is measured in ms. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

4.3.13.8.6.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

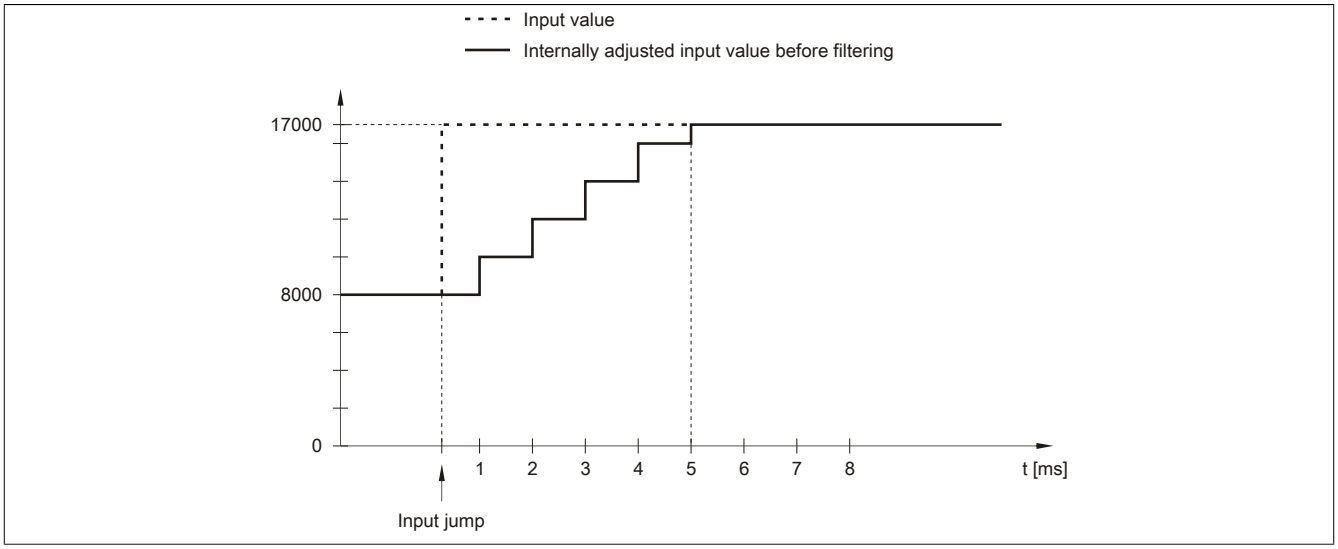


Figure 88: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

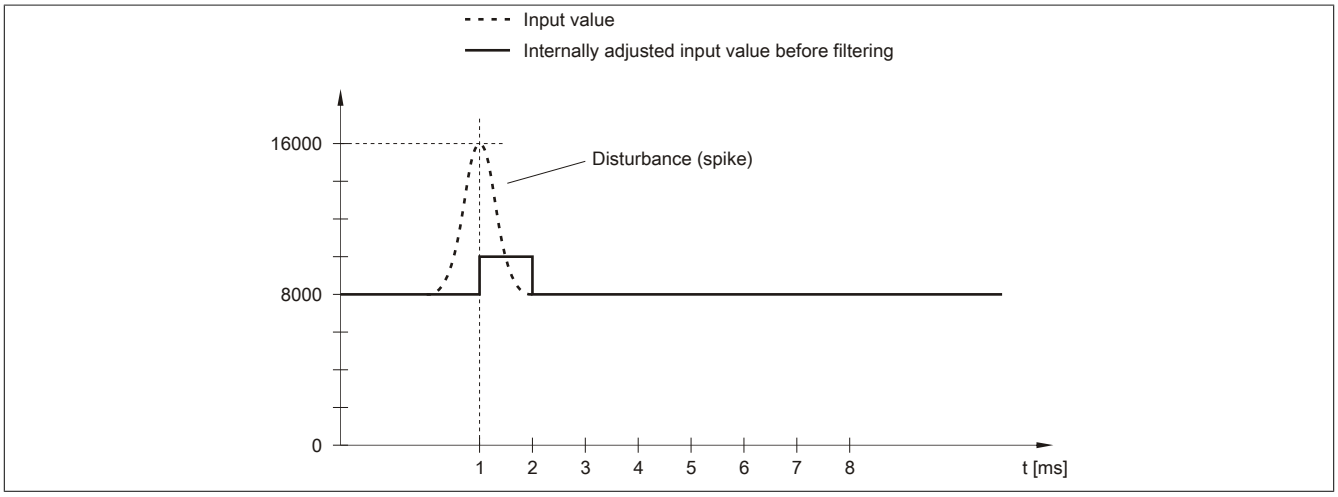


Figure 89: Adjusted input value for disturbance

4.3.13.8.6.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

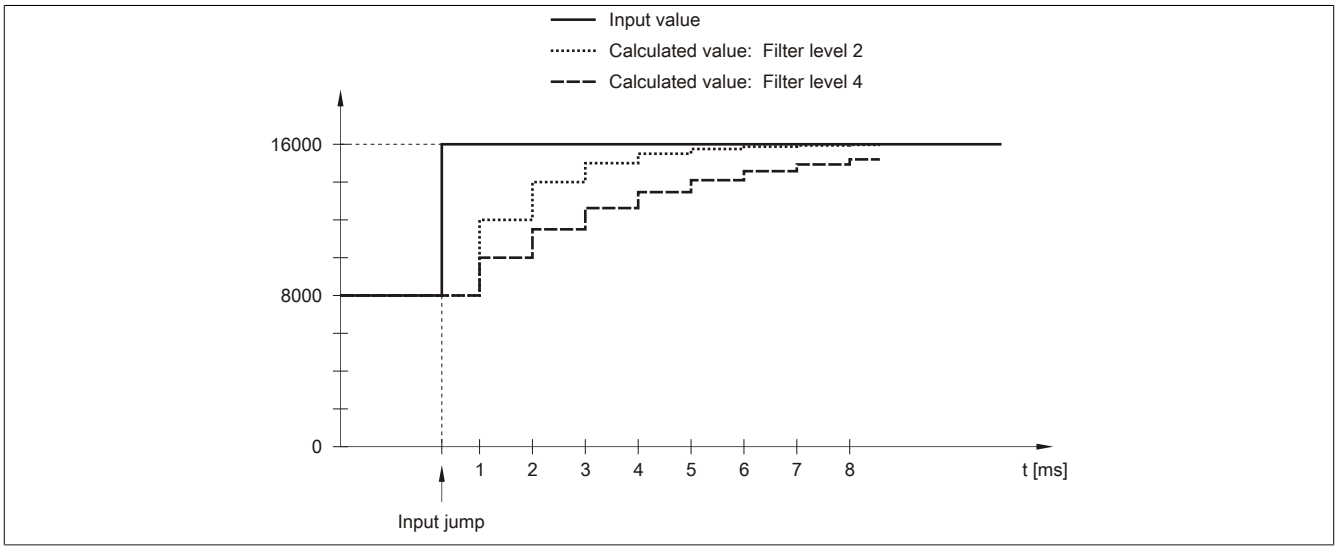


Figure 90: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

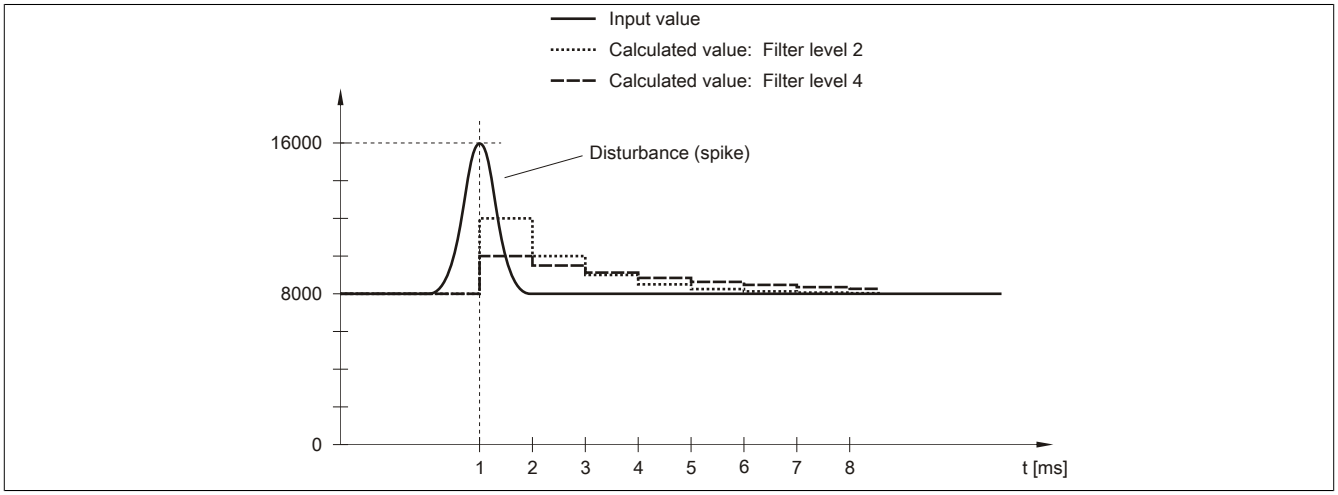


Figure 91: Calculated value during disturbance

4.3.13.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

4.3.13.8.8 Channel type

Name:
ConfigOutput02

This register can be used to set the range of the current signal. This is determined by how they are configured. The following input signals can be set:

- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	1	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
...		...	
7	Channel 4: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal

4.3.13.8.9 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Keep in mind that this setting applies to all channels!

4.3.13.8.10 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of 32767 corresponds to the maximum default value at 20 mA.

Keep in mind that this setting applies to all channels!

4.3.13.8.11 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	0 to 20 mA	4 to 20 mA
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	0	-8191 (0xE001)

4.3.13.8.12 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Inputs without filtering	100 µs
Inputs with filtering	500 µs

4.3.13.8.13 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Inputs without filtering	400 µs for all inputs
Inputs with filtering	1 ms

4.3.14 X20(c)AI4622

4.3.14.1 General information

The module is equipped with 4 inputs with 13-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

- 4 analog inputs
- Either current or voltage signal possible
- 13-bit digital converter resolution

4.3.14.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.3.14.3 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI4622	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	
X20cAI4622	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 54: X20AI4622, X20cAI4622 - Order data

4.3.14.4 Technical data

Product ID	X20AI4622	X20cAI4622
Short description		
I/O module	4 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA	
General information		
B&R ID code	0x1BAA	0xE1EF
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Inputs	Yes, using status LED and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.1 W [1]	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Analog inputs		
Input	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections	
Input type	Differential input	
Digital converter resolution		
Voltage	±12-bit	
Current	12-bit	
Conversion time	400 µs for all inputs	
Output format	INT	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA	
Input impedance in signal range		
Voltage	20 MΩ	
Current	-	
Load		
Voltage	-	
Current	<400 Ω	
Input protection	Protection against wiring with supply voltage	
Permitted input signal		
Voltage	Max. ±30 V	
Current	Max. ±50 mA	
Output of the digital value during overload	Configurable	
Conversion procedure	SAR	
Input filter	3rd-order low pass / cutoff frequency 1 kHz	
Max. error at 25°C		
Voltage		
Gain	0.08% [3]	
Offset	0.015% [4]	
Current		
Gain	0 to 20 mA = 0.08 % / 4 to 20 mA = 0.1 % [3]	
Offset	0 to 20 mA = 0.03 % / 4 to 20 mA = 0.16 % [5]	
Max. gain drift		
Voltage	0.006 %/°C [3]	
Current	0 to 20 mA = 0.009 %/°C 4 to 20 mA = 0.0113 %/°C [3]	
Max. offset drift		
Voltage	0.002 %/°C [4]	
Current	0 to 20 mA = 0.004 %/°C 4 to 20 mA = 0.005 %/°C [5]	
Common-mode rejection		
DC	70 dB	
50 Hz	70 dB	
Common-mode range	±12 V	
Crosstalk between channels	<-70 dB	
Nonlinearity		
Voltage	<0.025% [4]	
Current	<0.05% [5]	
Isolation voltage between channel and bus	500 V_{eff}	

Table 55: X20AI4622, X20cAI4622 - Technical data

Product ID	X20AI4622	X20cAI4622
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	12.5 $^{+0.2}$ mm

Table 55: X20AI4622, X20cAI4622 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 20 V measurement range.
5) Based on the 20 mA measurement range.

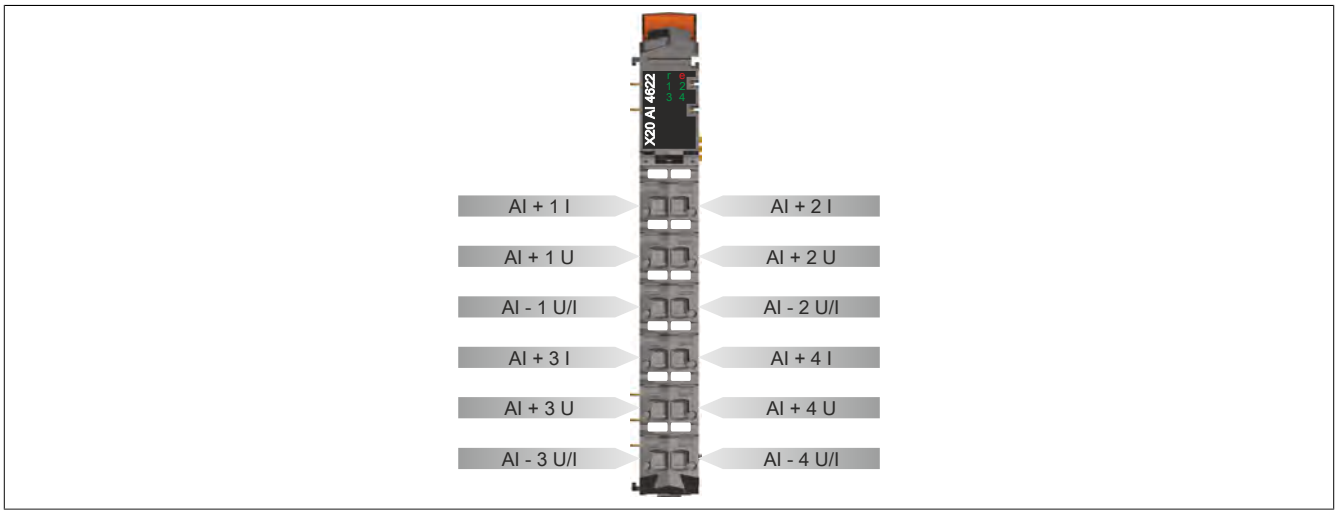
4.3.14.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

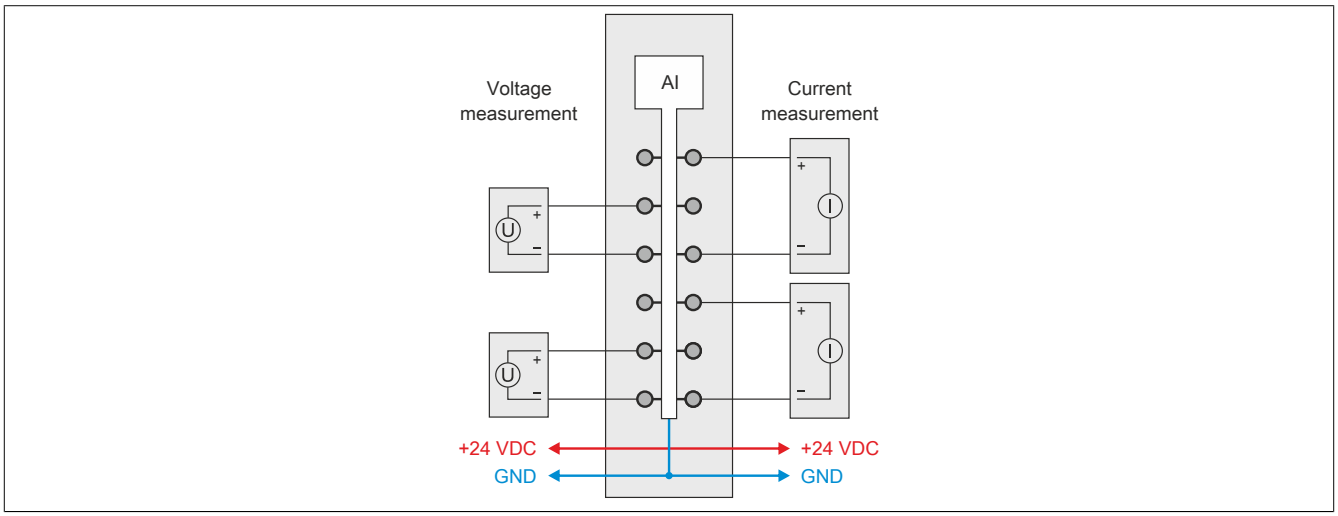
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Off	Open line[1)] or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Open line detection only possible when measuring voltage.

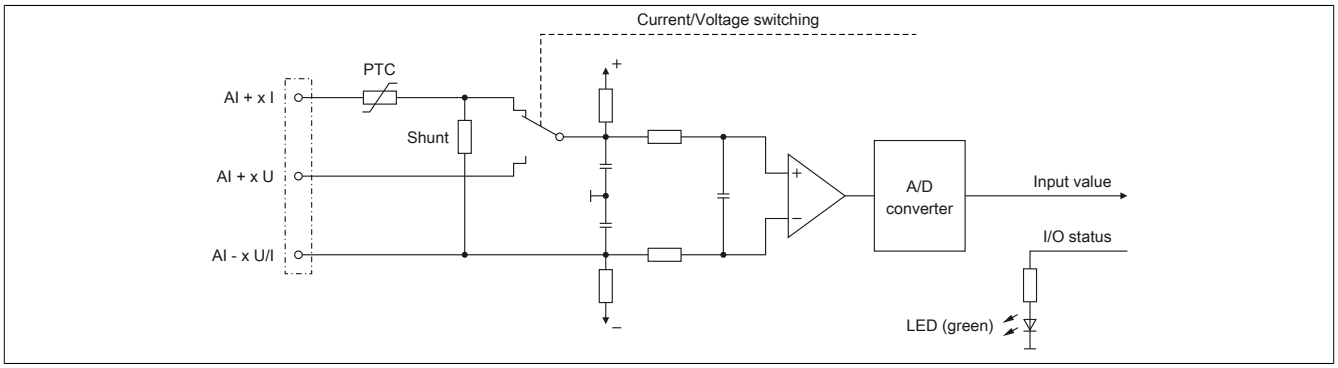
4.3.14.6 Pinout



4.3.14.7 Connection example



4.3.14.8 Input circuit diagram



4.3.14.9 Register description

4.3.14.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.14.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigOutput01	USINT				•
18	ConfigOutput02	USINT				•
20	ConfigOutput03	INT				•
22	ConfigOutput04	INT				•
Communication						
0	AnalogInput01	INT	•			
2	AnalogInput02	INT	•			
4	AnalogInput03	INT	•			
6	AnalogInput04	INT	•			
30	StatusInput01	USINT	•			

4.3.14.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigOutput01	USINT				•
18	-	ConfigOutput02	USINT				•
20	-	ConfigOutput03	INT				•
22	-	ConfigOutput04	INT				•
Communication							
0	0	AnalogInput01	INT	•			
2	2	AnalogInput02	INT	•			
4	4	AnalogInput03	INT	•			
6	6	AnalogInput04	INT	•			
30	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

4.3.14.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.14.9.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

4.3.14.9.5 Analog input values

Name:
AnalogInput01 to AnalogInput04

The analog input value are mapped to this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA

4.3.14.9.6 Input filter

This module is equipped with a configurable input filter. The minimum X2X cycle time must be >500 µs. Filtering is disabled for shorter X2X cycle times.

If the input filter is active, then the channels are scanned in 1 ms cycles. The time offset between the channels is 200 µs. Conversion is performed acyclically to the X2X cycle.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

4.3.14.9.6.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

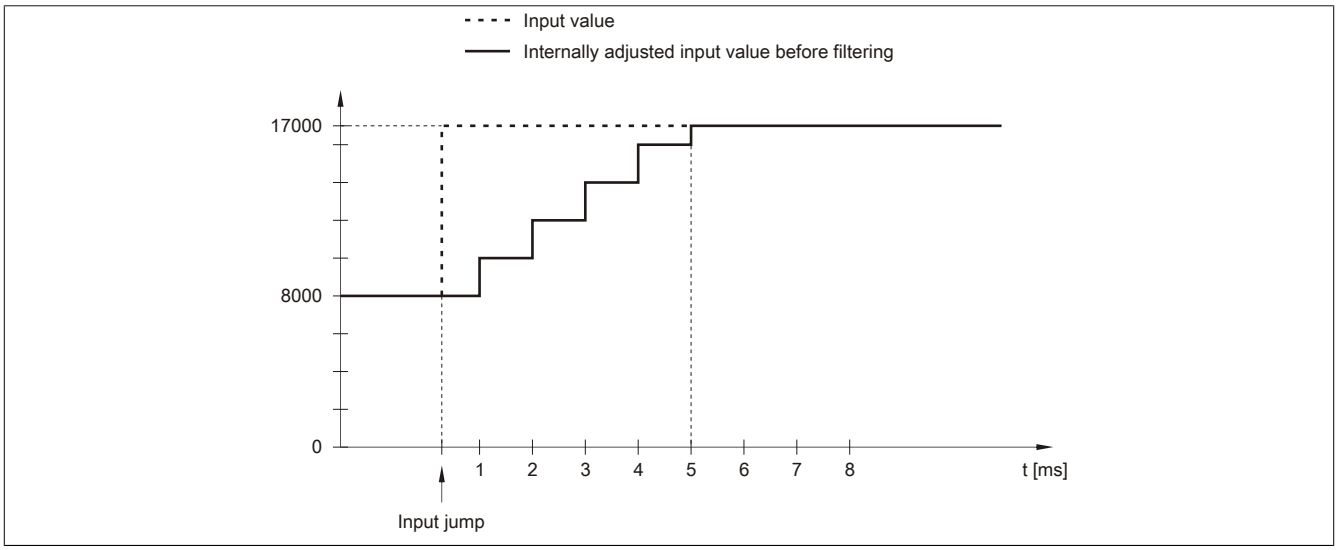


Figure 92: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

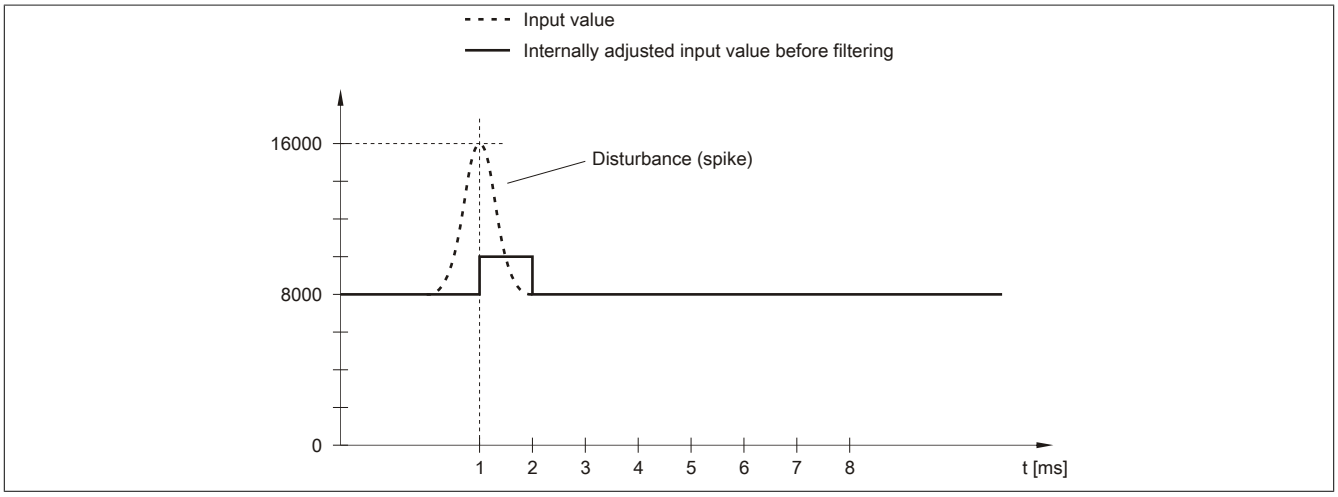


Figure 93: Adjusted input value for disturbance

4.3.14.9.6.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

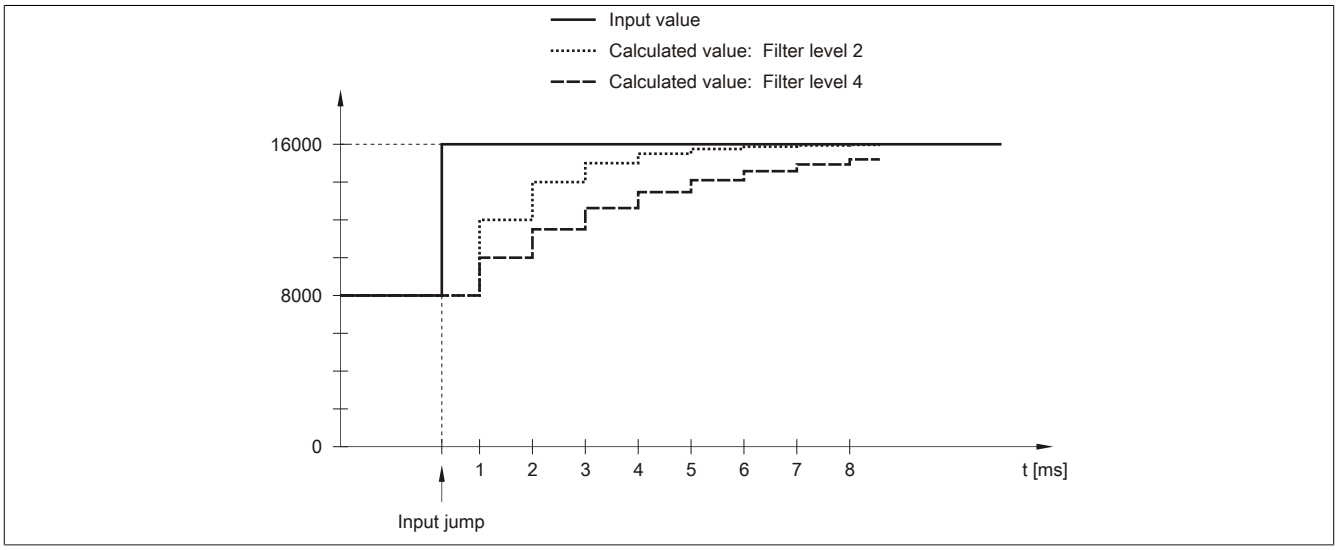


Figure 94: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

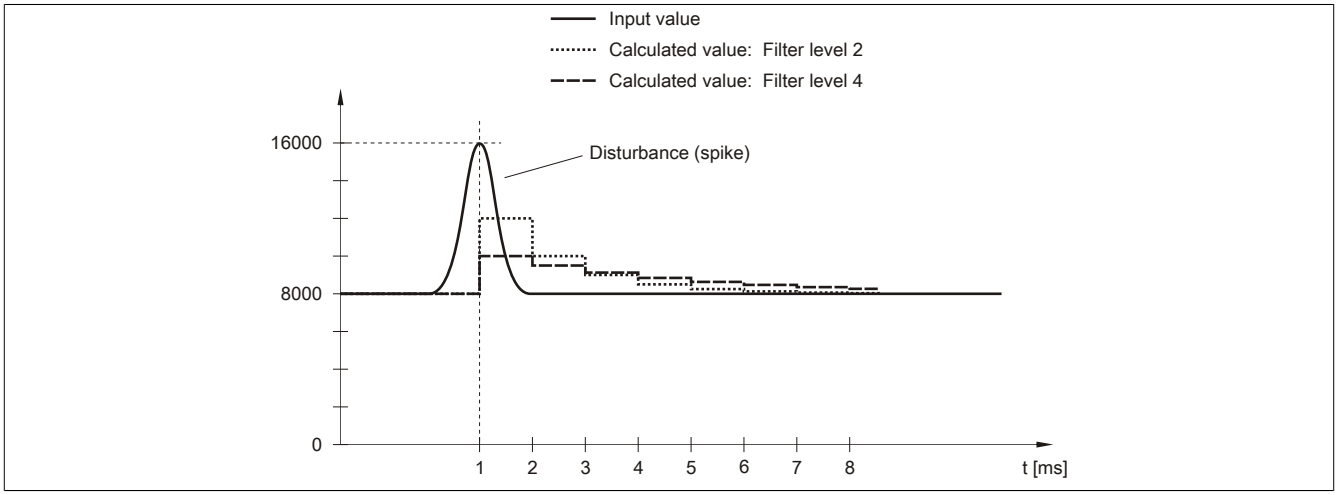


Figure 95: Calculated value during disturbance

4.3.14.9.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

4.3.14.9.8 Channel type

Name:
ConfigOutput02

This register can be used to define the type and range of signal measurement.

Each channel is capable of handling either current or voltage signals. This differentiation is made using multiple connection terminal points and an integrated switch in the module. The switch is automatically activated by the module depending on the specified configuration. The following input signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 4
...		...	
3	Channel 4	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 7
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
...		...	
7	Channel 4: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal

4.3.14.9.9 Limit values

The input signal is monitored at the upper and lower limit values. These must be defined according to the operating mode:

Limit value (default)	Voltage signal ±10 V		Current signal 0 to 20 mA		Current signal 4 to 20 mA	
Upper maximum limit value	+10 V	+32767 (0x7FFF)	20 mA	+32767 (0x7FFF)	20 mA	+32767 (0x7FFF)
Lower minimum limit value	-10 V	-32767 (0x8001)	0 mA	0[1)]	4 mA	0[2)]

1) The analog value is limited down to 0.
2) The analog value is limited down to 0 at currents <4 mA. The status bit for the lower limit is set.

Other limit values can be defined if necessary. Limit values are valid for all channels and activated automatically by writing to the limit value registers. From this point on, the analog values will be monitored and limited according to the new limits. The results of monitoring are displayed in the status register.

Examples of limit value settings

Application case	Limit value settings
Current signal: 4 to 20 mA	A negative limit value must be configured in order to measure values <4 mA with a current signal of 4 to 20 mA: 0 mA is equal to a value of -8192 (0xE000).
Mixed voltage and current signal	The configured limit values are valid for all channels. Mixed operation (voltage and current signal) therefore requires a compromise. The following configuration has proven effective: Upper limit = +32767, lower limit = -32767 This makes it possible to also measure negative voltage values. A lower limit value of 0 would limit the voltage value to 0.
Current signal on all channels	All channels are configured for measuring current. The limit value setting in Automation Studio is not adjusted automatically. That means that +32767 is configured as the upper limit value and -32767 as the lower limit value. The necessary changes must be made by the user, e.g. lower limit value = 0

4.3.14.9.9.1 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

- **The default value of -32768 corresponds to the minimum default value of -10 VDC.**
- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Information:

Keep in mind that this setting applies to all channels!

4.3.14.9.9.2 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of 32767 corresponds to the maximum default value of 20 mA or +10 VDC.

Information:

Keep in mind that this setting applies to all channels!

4.3.14.9.10 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message. The following states are monitored depending on the settings:

Value	Voltage signal ±10 V	Current signal 0 to 20 mA	Current signal 4 to 20 mA
0	No error	No error	No error
1	Lower limit value exceeded	Default setting The input value has a lower limit of 0x0000. Underflow monitoring is therefore not necessary. After lower limit value change The input value is limited to the configured value. The status bit is set when the lower limit value is passed.	Lower limit value exceeded
2	Upper limit value exceeded	Upper limit value exceeded	Upper limit value exceeded
3	Open line	-	-

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

4.3.14.9.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Inputs without filtering	100 µs
Inputs with filtering	500 µs

4.3.14.9.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Inputs without filtering	300 µs for all inputs
Inputs with filtering	1 ms

4.3.15 X20(c)AI4632

4.3.15.1 General information

The module is equipped with 4 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminal connections.

- 4 analog inputs
- Either current or voltage signal possible
- 16-bit digital converter resolution
- Simultaneous input conversion
- Very fast conversion time

4.3.15.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.3.15.3 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI4632	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
X20cAI4632	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 56: X20AI4632, X20cAI4632 - Order data

4.3.15.4 Technical data

Product ID	X20AI4632	X20cAI4632
Short description		
I/O module	4 analog inputs ±10 V or 0 to 20 mA	
General information		
B&R ID code	0x1BA1	0xE1F0
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Inputs	Yes, using status LED and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.5 W [1]	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Analog inputs		
Input	±10 V or 0 to 20 mA, via different terminal connections	
Input type	Differential input	
Digital converter resolution		
Voltage	±15-bit	
Current	15-bit	
Conversion time	50 µs for all inputs	
Output format	INT	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA	
Input impedance in signal range		
Voltage	20 MΩ	
Current	-	
Load		
Voltage	-	
Current	<400 Ω	
Input protection	Protection against wiring with supply voltage	
Permitted input signal		
Voltage	Max. ±30 V	
Current	Max. ±50 mA	
Output of the digital value during overload		
Below lower limit		
Voltage	0x8001	
Current	0x0000	
Above upper limit		
Voltage	0x7FFF	
Current	0x7FFF	
Conversion procedure	SAR	
Input filter	Hardware - 3rd-order low pass / cutoff frequency 10 kHz	
Max. error at 25°C		
Voltage		
Gain	0.08% [3]	
Offset	0.01% [4]	
Current		
Gain	0.08% [3]	
Offset	0.02% [5]	
Max. gain drift		
Voltage	0.01 %/°C [3]	
Current	0.01 %/°C [3]	
Max. offset drift		
Voltage	0.001 %/°C [4]	
Current	0.002 %/°C [5]	
Common-mode rejection		
DC	70 dB	
50 Hz	70 dB	
Common-mode range	±12 V	
Crosstalk between channels	<-70 dB	

Table 57: X20AI4632, X20cAI4632 - Technical data

Product ID	X20AI4632	X20cAI4632
Nonlinearity		
Voltage	<0.01% 4)	
Current	<0.015% 5)	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 57: X20AI4632, X20cAI4632 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 20 V measurement range.
5) Based on the 20 mA measurement range.

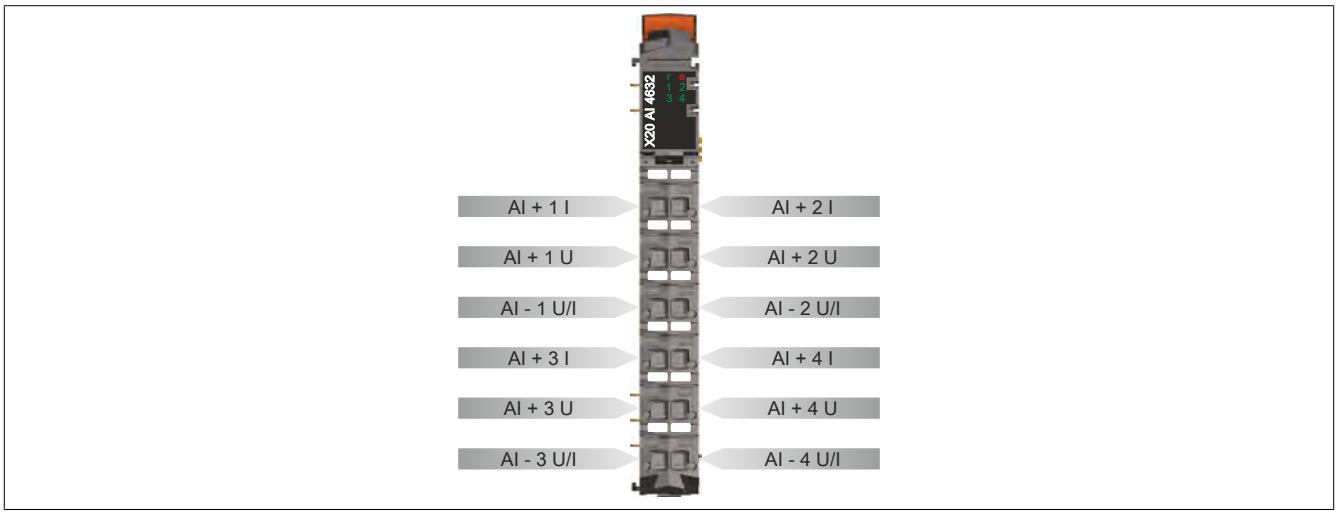
4.3.15.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 4	Green	Off	Open line[2] or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

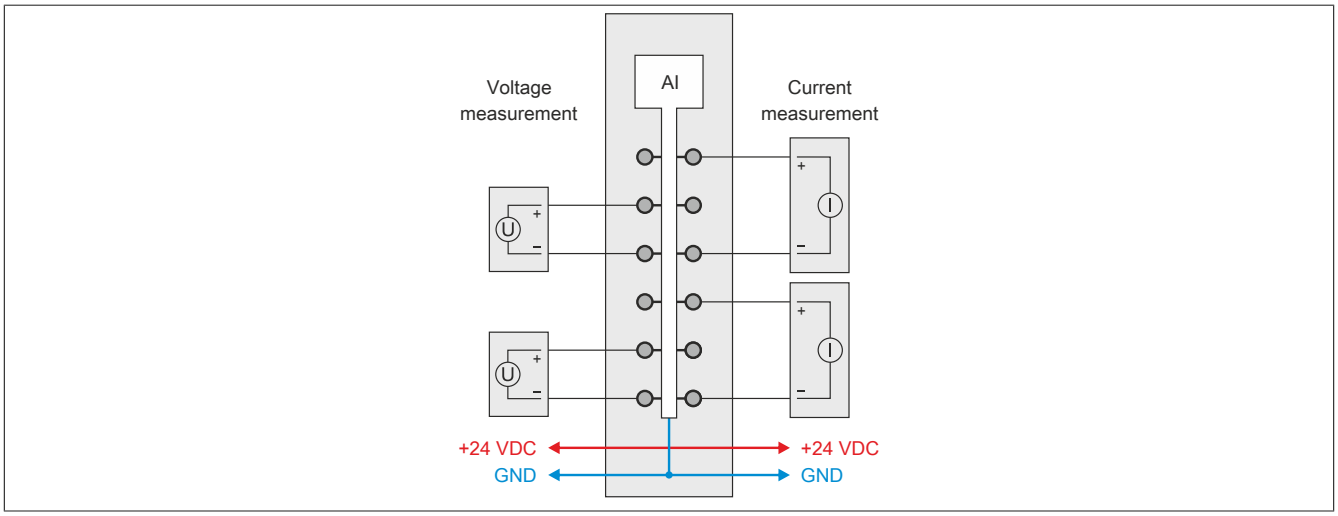
4.3.15.6 Pinout



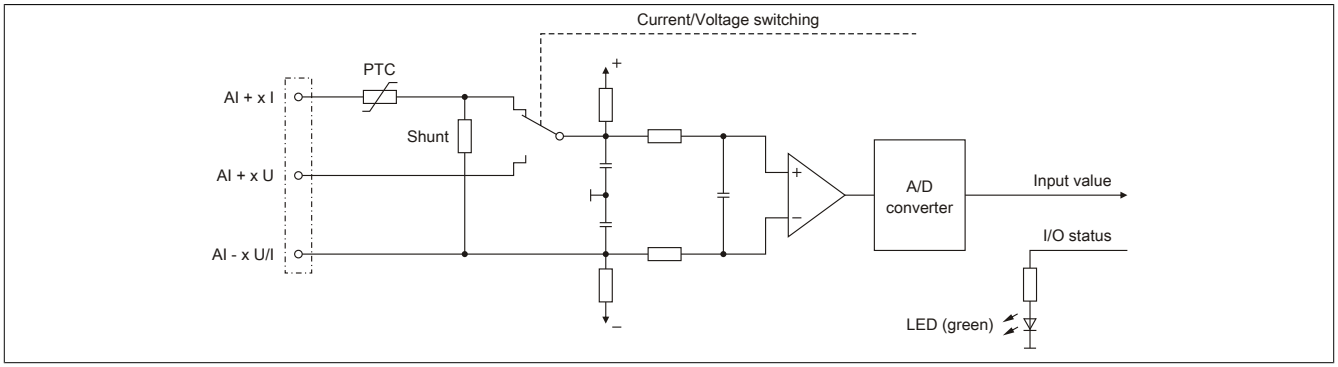
4.3.15.7 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Supply module X20PS9500/X20PS9502
- CPU modules



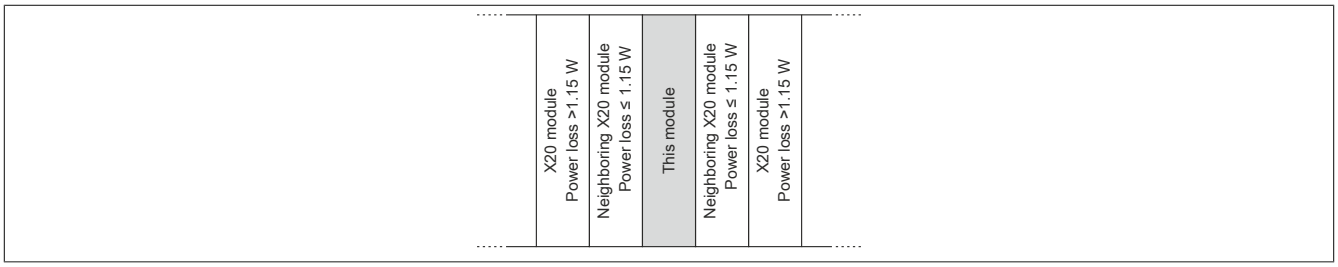
4.3.15.8 Input circuit diagram



4.3.15.9 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.3.15.10 Register description

4.3.15.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.15.10.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257 289 321 353	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259 291 323 355	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling					
276 308 340 372	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values					
266 298 330 362	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication						
0 + (N-1) * 4	AnalogInput0N (index N = 1 to 4)	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	...	...				
	Channel04OK	Bit 3				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	Synchronization error counter	UINT		•		
2097	Range violation (neg. and pos.)	USINT	•			
	Channel01underflow	Bit 0				
	Channel01overflow	Bit 1				
	...	...				
	Channel04underflow	Bit 6				
	Channel04overflow	Bit 7				
2099	Working range violation (pos.)	USINT	•			
	Channel01OutofRange	Bit 0				
	...	...				
	Channel04OutofRange	Bit 3				
518 + (N-1) * 32	Ch0NOutofRange (index N = 1 to 4)	UINT		•		
522 + (N-1) * 32	Ch0NUnderflow (index N = 1 to 4)	UINT		•		
526 + (N-1) * 32	Ch0NOverflow (index N = 1 to 4)	UINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Additional analysis functions						
133	ConfigOutput21 (trigger reaction on falling edge)	USINT				●
135	ConfigOutput22 (trigger reaction on rising edge)	USINT				●
129	Analysis control byte	USINT			●	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	...	...				
	MinMaxStart04	Bit 7				
129	Analysis status byte	USINT	●			
	MinMaxStart01Readback	Bit 4				
	...	...				
	MinMaxStart04Readback	Bit 7				
	Limit values					
530 + (N-1) * 32	MinInput0N (index N = 1 to 4)	INT	●			
534 + (N-1) * 32	MaxInput0N (index N = 1 to 4)	INT	●			
538 + (N-1) * 32	Ch0NMinMaxLatchCounter (index N = 1 to 4)		UINT	●		
	Trace configuration					
1026	TraceChannelEnable	USINT				●
1030	TraceSampleDepth	UINT				●
4157	ConfigOutput25 (trace priority)	USINT				●
1037	Starting a recording	USINT			●	
	TraceEnable01	Bit 0				
1089	Recording status	USINT	●			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	●			
1098	TriggerCount	UINT	●			
1102	TriggerFailCount	UINT	●			
	Comparator					
450 + (N-1) * 8	cfgComp_LowLimitCh0N (index N = 1 to 4)	INT			(●)	●
454 + (N-1) * 8	cfgComp_HighLimitCh0N (index N = 1 to 4)	INT			(●)	●
662	CompStateCollection	UINT	●			
490	cfgComp_NominalState	UINT				●
482	cfgComp_EnableMask	UINT				●
486	cfgComp_ConditionTypeMask	UINT				●
	Time-offset trace					
1042	TraceTriggerStart	INT				●
1046	TraceTriggerStop	UINT				●

4.3.15.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257 289 321 353	-	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				•
	Filtering						
259 291 323 355	-	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	-	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling						
276 308 340 372	-	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	-	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values						
266 298 330 362	-	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	-	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication							
0 + (N-1) * 4	0 + (N-1) * 2	AnalogInput0N (index N = 1 to 4)	INT	•			
650	-	SampleCycleCounter	UINT		•		
	Error monitoring and counters						
641	-	Channel status	USINT		•		
		Channel01OK	Bit 0				
		...	...				
		Channel04OK	Bit 3				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		•		
658	-	Synchronization error counter	UINT		•		
2097	-	Range violation (neg. and pos.)	USINT		•		
		Channel01underflow	Bit 0				
		Channel01overflow	Bit 1				
		...	...				
		Channel04underflow	Bit 6				
		Channel04overflow	Bit 7				
2099	-	Working range violation (pos.)	USINT		•		
		Channel01OutofRange	Bit 0				
		...	...				
		Channel04OutofRange	Bit 3				
522 + (N-1) * 32	-	Ch0NUnderflow (index N = 1 to 4)	UINT		•		
526 + (N-1) * 32	-	Ch0NOverflow (index N = 1 to 4)	UINT		•		
518 + (N-1) * 32	-	Ch0NOutofRange (index N = 1 to 4)	UINT		•		
Additional analysis functions							
133	-	Trigger reaction on falling edge	USINT				•
135	-	Trigger reaction on rising edge	USINT				•
129	-	Analysis control byte	USINT				•
		MinMaxStart01	Bit 4				
		...	...				
		MinMaxStart04	Bit 7				
129	-	Analysis status byte	USINT		•		
		MinMaxStart01Readback	Bit 4				
		...	...				

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
		MinMaxStart04Readback	Bit 7				
	Limit values						
530 + (N-1) * 32	-	MinInput0N (index N = 1 to 4)	INT		•		
534 + (N-1) * 32	-	MaxInput0N (index N = 1 to 4)	INT		•		
538 + (N-1) * 32	-	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		•		

1) The offset specifies the position of the register within the CAN object.

4.3.15.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.15.10.4 Configuration

This module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately from one another either on the voltage or current input for the following areas:

- Permitted voltage: ±10 V
- Permitted current: 0 to 20 mA

4.3.15.10.4.1 Channel configuration

Name:
ConfigOutput01 for channel 1
ConfigOutput06 for channel 2
ConfigOutput11 for channel 3
ConfigOutput16 for channel 4

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using the correct terminal block pins.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±10 VDC
		1	Current terminal for 0 to 20 mA
1	Gain selector	0	Voltage ±10 VDC
		1	Current 0 to 20 mA
2 - 3	Reserved	-	
4	Filtering active	0	Inactive
		1	Active
5	Minimum/Maximum analysis active	0	Inactive
		1	Active
6	Error monitoring active	0	Inactive
		1	Active
7	Enables channel	0	Channel enabled
		1	Channel disabled

4.3.15.10.4.2 Sampling and conversion

The analog signal is sampled in 2 steps.

- **Conversion task**
  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.
  The timespan needed for conversion results from the set sampling time.
- **Processing task**
  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Function
UINT	50 to 10,000	Default value = 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

4.3.15.10.4.3 Filtering (optional)

If filtering is enabled in the 4.3.15.10.4.1 "Channel configuration" register, the basic data of the A/D converter is filtered per channel. The following registers are available to specify the filter order and respective cutoff frequency for configuring the low-pass filter:

- "Filter order"
- "Filter cutoff frequency"

Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2
ConfigOutput30 for channel 3
ConfigOutput32 for channel 4

The filter order is specified in this register. The "Filter cutoff frequency" register is used to configure the respective cutoff frequency of the filter.

Data type	Value
USINT	1 to 4

Internal filter orders greater than 1 are implemented as cascaded first-order filters. Since the filter is calculated in the sampling cycle, the filter characteristics are directly related to the settings for the sampling cycle time.

Calculating the cutoff frequency of an nth-order filter:

yn = a * xn + b * y(n-1)

Approximate calculation

a = Sampling time / (Sampling time + 1/Cutoff frequency)

b = 1 - a

Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2
ConfigOutput31 for channel 3
ConfigOutput33 for channel 4

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Description
UINT	1 to 65,535	Cutoff frequency in hertz

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

4.3.15.10.4.4 Scaling (optional)

Scaling A/D converter data is an option for the user. The following registers are available for this:

- "User-defined gain" (= ku)
- "User-defined offset" (= du)

Scaling calculation:

Scaled value = k * A/C value + d

Gain k = $k_{Calibration}$ * ku

Offset d = $d_{Calibration}$ + du

The value has to be limited since it can exceed the 16-bit constraints. To provide the greatest degree of flexibility, limiting is possible using the registers "Minimum limit value" and "Maximum limit value".

User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2
ConfigOutput14 for channel 3
ConfigOutput19 for channel 4

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65,536 (0x10000) corresponds to a gain of 1.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2
ConfigOutput15 for channel 3
ConfigOutput20 for channel 4

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65,536 (0x10000) corresponds to an offset of 1.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.3.15.10.4.5 Limit values

If the application requires a limitation of the range of values, then the user can define his own limit values. These values will also be use for the module's error statistics. The following registers are available for this:

- "Minimum limit value"
- "Maximum limit value"

Information:

32-bit numbers are used inside the module. A limit value violation can therefore also be determined if the permitted range of values was defined from -32768 to 32767.

Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2
ConfigOutput12 for channel 3
ConfigOutput17 for channel 4

The minimum limit value is configured in this register. This limit value is also used as the lower value in the error statistics (see register "Counter for range exceeded violations (neg.)").

Data type	Value
INT	-32768 to 32767

Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2
ConfigOutput13 for channel 3
ConfigOutput18 for channel 4

The maximum limit value is configured in this register. This limit value is also used as the upper value in the error statistics (see register "Counter for range exceeded violations (pos.)").

Data type	Value
INT	-32768 to 32767

4.3.15.10.5 Communication - General

The module's analog inputs convert current and voltage values with 16-bit resolution. This information can be used by the application with the help of the registers listed here.

4.3.15.10.5.1 Analog input channels

Name:
AnalogInput01 to AnalogInput04

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

4.3.15.10.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Value
UINT	0 to 65535

4.3.15.10.5.3 Error monitoring and counters

Channel status

Name:
Channel01OK to Channel04OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors
...		...	
3	Channel04OK	0	OK
		1	Errors
4 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "Synchronization error counter".
2) Identical to bit 0 of the registers "Counter for faulty sampling cycles".

Synchronization error counter

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See 4.3.9.8.4.2 "Sampling and conversion".

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Range violation (neg. and pos.)

Name:
Channel01underflow to Channel04underflow
Channel01overflow to Channel04overflow

This register indicates whether a range violation (pos. and/or neg.) of the limit values defined in the registers "Minimum limit value" and "Maximum limit value" has occurred. The individual bits in this register are identical to the values of the lowest bits in the registers "Counter for range exceeded violations (neg.)" and "Counter for range exceeded violations (pos.)".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
...		...	
3	Channel04underflow	0	No error
		1	Range exceeded (.neg) on channel 4
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
...		...	
7	Channel04overflow	0	No error
		1	Range exceeded (.pos) on channel 4

Working range violation (pos.)

Name:
Channel01OutofRange to Channel04OutofRange

This register indicates whether the input value exceeds the module's maximum measurement range. The individual bits in this register are identical to the values of the lowest bits in the register "Counter for work range violations (pos.)".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutofRange	0	No error
		1	Working range violation (pos.) of channel 1
...		...	
3	Channel04OutofRange	0	No error
		1	Working range violation (pos.) of channel 4
4 - 7	Reserved	-	

Counter for work range violations (pos.)

Name:
CH01OutofRange to CH04OutofRange

Errors outside of the module's maximum possible measurement range are indicated in this register. These errors lead to full-scale deflection of the A/D converter.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.15.10.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (neg.)

Name:
CH01Underflow to CH04Underflow

This register indicates range exceeded violations (neg.) of the value configured in the register "Minimum limit value".

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.15.10.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (pos.)

Name:
CH01Overflow to CH04Overflow

This register indicates range exceeded violations (pos.) of the value configured in the register "Maximum limit value".

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.15.10.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

4.3.15.10.6 Additional analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

- **Limit value analysis**
  If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched internally in the module. A measurement period can be triggered using the control byte. When the respective configured edge is generated by the application, the limit values from the previous measurement period are displayed and the internal latch register is reset.
- **Recording sampled values**
  If recording sampled values has been enabled for a channel, then the sampled values are additionally recorded in the module's internal FIFO memory. If the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

It is only possible to use the recording of sampled values if the module is operated on an X2X master that is an SG4 CPU.

4.3.15.10.6.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register configures whether the falling edge is used to trigger the trace and determination of the input value in the register 4.3.15.10.6.3 "Analysis control byte".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination
		1	Falling edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination
		1	Falling edge determines input value of channel 4

4.3.15.10.6.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register configures whether the rising edge is used to trigger the trace and determination of the input value in the register 4.3.15.10.6.3 "Analysis control byte".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Rising edge does not initiate trigger
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination
		1	Rising edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination
		1	Rising edge determines input value of channel 4

4.3.15.10.6.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart04

The trace function and determination of the minimum/maximum input values can be started in this register.
Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers 4.3.15.10.6.1 "Trigger condition on falling edge" and 4.3.15.10.6.2 "Trigger condition on rising edge".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Does not initiate trigger/trace
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not initiated
		1	Initiates determination of input value of channel 1
...	...	...	
7	MinMaxStart04	0	Determination not initiated
		1	Initiates determination of input value of channel 4

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

4.3.15.10.6.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart04Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel
...	...	...	
7	MinMaxStart04Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel

4.3.15.10.7 Limit values

Limit value analysis must be enabled for the desired channel (see 4.3.15.10.4.1 "Channel configuration"). The sampled value of the channel is then compared to the minimum and maximum values that are stored internally in the module. If a new measurement period is initiated with the 4.3.15.10.6.3 "Analysis control byte" register, then the values determined from the previous measurement period can be taken from the respective registers intended for this.

4.3.15.10.7.1 Minimum input values

Name:
MinInput01 to MinInput04

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

4.3.15.10.7.2 Maximum input values

Name:
MaxInput01 to MaxInput04

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

4.3.15.10.7.3 Limit value trigger counter

Name:
CH01MinMaxLatchCounter to CH04MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

4.3.15.10.8 Trace

If the module is operated on a SG4 CPU, the digitalized input values are recorded by the module. The module must be operated in "Supervised" mode in order to use the trace function.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism can only be used if the module is connected directly to the CPU, not if it is operated behind a bus controller.

4.3.15.10.8.1 Enable recording

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
...	...	...	
3	Channel 4	0	Channel disabled
		1	Channel enabled
4 - 7	Reserved	-	

4.3.15.10.8.2 Number of values to be recorded

Name:
TraceSampleDepth

16 kB are available on the module for the trace. The FIFO memory limitation means that a maximum of 8192 analog values can be recorded. This memory is divided up equally among the enabled channels. The actual number of maximum possible recordings therefore depends on the number of channels enabled for trace:

1 channel enabled: Up to 8192 recordings
2 channels enabled: Up to 4096 recordings per channel
3 channels enabled: Up to 2730 recordings per channel
4 channels enabled: Up to 2048 recordings per channel

Data type	Value	Function
UINT	2 to 8192	Default value = 1024

4.3.15.10.8.3 Recording priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard (default value)
	6	Trace priority higher than X2X Link communication

4.3.15.10.8.4 Starting a recording

Name:

TraceEnable01

This register starts the recording according to the specifications for edge control or the comparator.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

4.3.15.10.8.5 Recording status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

4.3.15.10.8.6 Free trace buffer

Name:
FreeBufferSize

Specifies the available FIFO memory area in bytes for the trace

Data type	Value
UINT	0 to 65535

4.3.15.10.8.7 Counter for trace triggers

Name:
TriggerCount

This register indicates the number of triggers that have occurred since "starting the trace".

Data type	Value
UINT	0 to 65535

4.3.15.10.8.8 Counter for faulty recording triggers

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be performed.

Data type	Value
UINT	0 to 65535

4.3.15.10.8.9 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold value bits for all channels are grouped together in the lower-value byte of the "Hysteresis status of the channels" register. In addition, the states of the previous sampling are stored in the higher-value byte.

The 4 status messages of each channel can be linked according to the following logic via a logical connective mask using AND or OR operators and used as a trace trigger:

```
delta = (Current_HysteresisStatus ^ NominalValues) // Different between current status and preset
cond = delta & Selected_HysteresisStatusBits // Eliminate irrelevant status messages
ccond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if ((0 == (cond & ~LogicalOperators)) &&
(0 != (~cond & LogicalOperators))) { => Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	cfgComp_EnableMask
Current_HysteresisStatus	CompStateCollection
Nominal values	cfgComp_NominalState
Logical operators	cfgComp_ConditionTypeMask

Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh04

The lower limit value for hysteresis is configured in this register.

Data type	Value
INT	-32768 to 32767

Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh04

The upper limit value for hysteresis is configured in this register.

Data type	Value
INT	-32768 to 32767

Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values

Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values

Information:

This is a "whitelist", i.e. the trace starts as soon as the current status message takes on the state predefined here.

One or more matches will be necessary depending on the selection of the relevant hysteresis status bits and logical connective operators.

Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register selects which status bits of the hysteresis comparison should be used to generate the trigger.

For more information about using this register, see 4.3.15.10.8.9 "Comparator for trigger conditions".

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
7	Channel04 InRange status in the current cycle	0	Do not use
		1	Use for generation
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
15	Channel04 InRange status in the last cycle	0	Do not use
		1	Use for generation

Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

The desired state operators with which the respective status bit is linked to others to generate a trigger are selected in this register.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "Selecting the relevant hysteresis status bits" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
7	Channel04 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
15	Channel04 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation

4.3.15.10.8.10 Time-offset trace

Additional conditions for shifting the starting and stopping points can be defined if the trace should be chronologically offset to the trigger.

Starting the trace

Name:
TraceTriggerStart

The starting position is defined relative to the configured trigger condition (rising/falling edge) in this register. Positive values mean that the trace takes place x samples after the trigger condition. Negative values mean that the trace takes place x samples before the trigger condition.

The value -32768 performs the trace without regard for the configured trigger condition. If the trace memory is completely full, then the oldest recorded value is overwritten (FIFO principle).

"Trace start" in the I/O configuration or the registers 4.3.15.10.6.1 "Trigger condition on falling edge" and 4.3.15.10.6.2 "Trigger condition on rising edge" determine whether a positive, negative or any edge must be triggered.

Data type	Value
INT	-32768 to 32767

Stopping the trace

Name:
TraceTriggerStop

The stopping position is defined relative to the configured trigger condition in this register.

- When configuring an early trigger event, this value refers to the trigger event.
- When configuring a delayed trigger event, this value refers to the starting event.

Data type	Value
UINT	0 to 65535

4.3.15.10.9 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

4.3.15.10.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard priority	200 µs
High priority with trace function	300 µs

4.3.15.10.11 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

4.3.16 X20(c)AI4632-1

4.3.16.1 General information

The module is equipped with 4 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminal connections.

- 4 analog inputs
- Either current or voltage signal possible
- Extended signal range
- 16-bit digital converter resolution
- Simultaneous input conversion
- Very fast conversion time

4.3.16.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.3.16.3 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI4632-1	X20 analog input module, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
X20cAI4632-1	X20 analog input module, coated, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 58: X20AI4632-1, X20cAI4632-1 - Order data

4.3.16.4 Technical data

Product ID	X20AI4632-1	X20cAI4632-1
Short description		
I/O module	4 analog inputs ±11 V or 0 to 22 mA	
General information		
B&R ID code	0xA29D	0xD57A
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Inputs	Yes, using status LED and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.5 W [1]	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GL	Yes	
LR	-	Yes
GOST-R	Yes	
Analog inputs		
Input	±11 V or 0 to 22 mA, via different terminal connections	
Input type	Differential input	
Digital converter resolution		
Voltage	±15-bit	
Current	15-bit	
Conversion time	50 µs for all inputs	
Output format	INT	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.387 nA	
Input impedance in signal range		
Voltage	20 MΩ	
Current	-	
Load		
Voltage	-	
Current	<400 Ω	
Input protection	Protection against wiring with supply voltage	
Permitted input signal		
Voltage	Max. ±30 V	
Current	Max. ±50 mA	
Output of the digital value during overload		
Below lower limit		
Voltage	0x8001	
Current	0x0000	
Above upper limit		
Voltage	0x7FFF	
Current	0x7FFF	
Conversion procedure	SAR	
Input filter	Hardware - 3rd-order low pass / cutoff frequency 10 kHz	
Max. error at 25°C		
Voltage		
Gain	0.08% [3]	
Offset	0.01% [4]	
Current		
Gain	0.08% [3]	
Offset	0.02% [5]	
Max. gain drift		
Voltage	0.01 %/°C [3]	
Current	0.01 %/°C [3]	
Max. offset drift		
Voltage	0.001 %/°C [4]	
Current	0.002 %/°C [5]	
Common-mode rejection		
DC	70 dB	
50 Hz	70 dB	
Common-mode range	±12 V	
Crosstalk between channels	<-70 dB	

Table 59: X20AI4632-1, X20cAI4632-1 - Technical data

Product ID	X20AI4632-1	X20cAI4632-1
Nonlinearity		
Voltage	<0.01% 4)	
Current	<0.015% 5)	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 59: X20AI4632-1, X20cAI4632-1 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 22 V measurement range.
5) Based on the 22 mA measurement range.

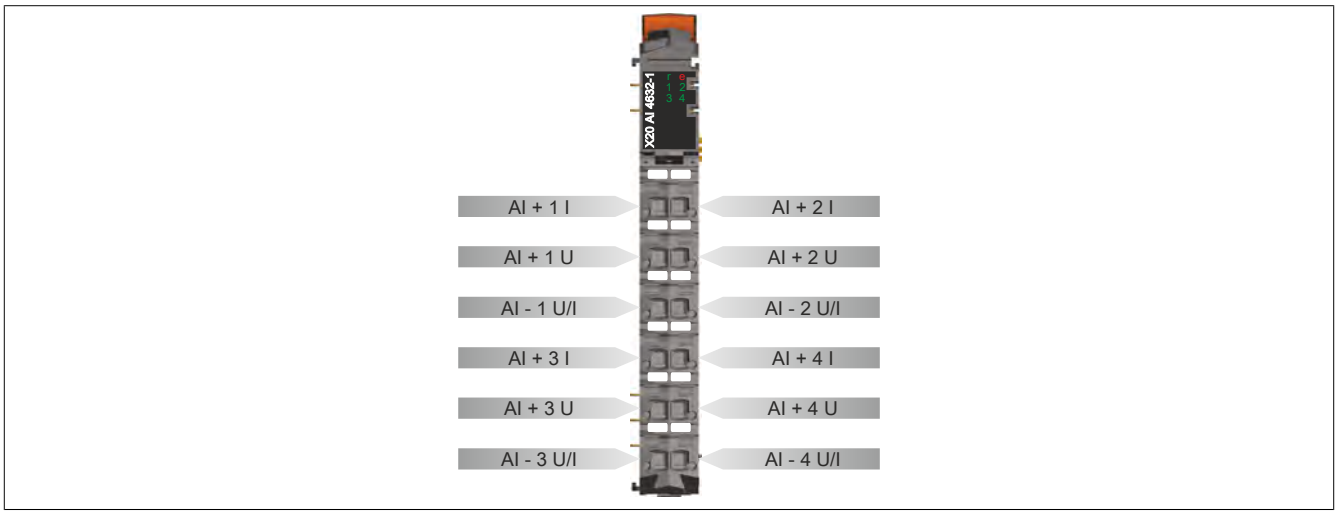
4.3.16.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 4	Green	Off	Open line[2] or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

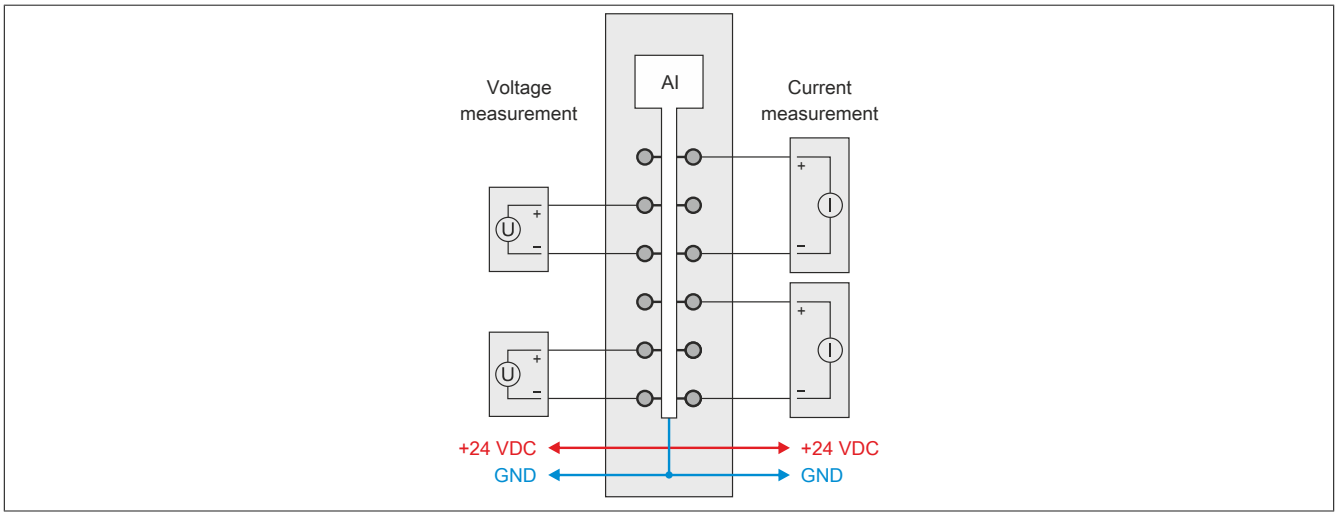
4.3.16.6 Pinout



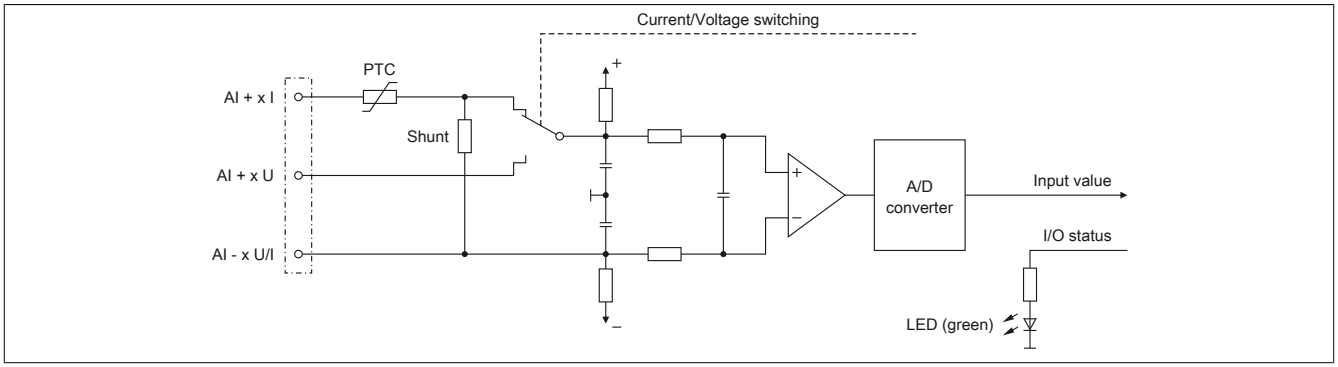
4.3.16.7 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Supply module X20PS9500/X20PS9502
- CPU modules



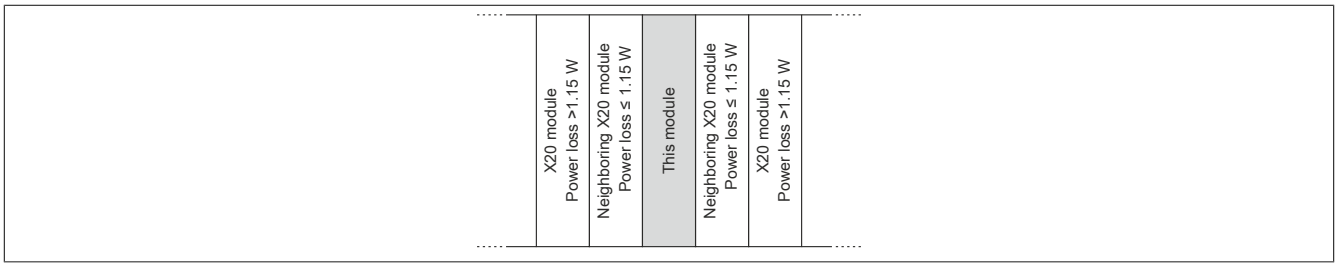
4.3.16.8 Input circuit diagram



4.3.16.9 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.3.16.10 Register description

4.3.16.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.16.10.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257 289 321 353	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259 291 323 355	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling					
276 308 340 372	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values					
266 298 330 362	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication						
0 + (N-1) * 4	AnalogInput0N (index N = 1 to 4	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	...	...				
	Channel04OK	Bit 3				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	Synchronization error counter	UINT		•		
2097	Range violation (neg. and pos.)	USINT	•			
	Channel01underflow	Bit 0				
	Channel01overflow	Bit 1				
	...	...				
	Channel04underflow	Bit 6				
	Channel04overflow	Bit 7				
2099	Working range violation (pos.)	USINT	•			
	Channel01OutofRange	Bit 0				
	...	...				
	Channel04OutofRange	Bit 3				
518 + (N-1) * 32	Ch0NOverflow (index N = 1 to 4)	UINT		•		
522 + (N-1) * 32	Ch0NUnderflow (index N = 1 to 4)	UINT		•		
526 + (N-1) * 32	Ch0NOutofRange (index N = 1 to 4)	UINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Additional analysis functions						
133	ConfigOutput21 (trigger reaction on falling edge)	USINT				●
135	ConfigOutput22 (trigger reaction on rising edge)	USINT				●
129	Analysis control byte	USINT			●	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	...	...				
	MinMaxStart04	Bit 7				
129	Analysis status byte	USINT	●			
	MinMaxStart01Readback	Bit 4				
	...	...				
	MinMaxStart04Readback	Bit 7				
	Limit values					
530 + (N-1) * 32	MinInput0N (index N = 1 to 4)	INT	●			
534 + (N-1) * 32	MaxInput0N (index N = 1 to 4)	INT	●			
538 + (N-1) * 32	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		●		
	Trace configuration					
1026	TraceChannelEnable	USINT				●
1030	TraceSampleDepth	UINT				●
4157	ConfigOutput25 (trace priority)	USINT				●
1037	Starting a recording	USINT			●	
	TraceEnable01	Bit 0				
1089	Recording status	USINT	●			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	●			
1098	TriggerCount	UINT	●			
1102	TriggerFailCount	UINT	●			
	Comparator					
450 + (N-1) * 8	cfgComp_LowLimitCh0N (index N = 1 to 4)	INT			(●)	●
454 + (N-1) * 8	cfgComp_HighLimitCh0N (index N = 1 to 4)	INT			(●)	●
662	CompStateCollection	UINT	●			
490	cfgComp_NominalState	UINT				●
482	cfgComp_EnableMask	UINT				●
486	cfgComp_ConditionTypeMask	UINT				●
	Time-offset trace					
1042	TraceTriggerStart	INT				●
1046	TraceTriggerStop	UINT				●

4.3.16.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257 289 321 353	-	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				•
	Filtering						
259 291 323 355	-	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	-	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling						
276 308 340 372	-	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	-	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values						
266 298 330 362	-	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	-	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication							
0 + (N-1) * 4	0 + (N-1) * 2	AnalogInput0N (index N = 1 to 4)	INT	•			
650	-	SampleCycleCounter	UINT		•		
	Error monitoring and counters						
641	-	Channel status	USINT		•		
		Channel01OK	Bit 0				
		...	...				
		Channel04OK	Bit 3				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		•		
658	-	Synchronization error counter	UINT		•		
2097	-	Range violation (neg. and pos.)	USINT		•		
		Channel01underflow	Bit 0				
		Channel01overflow	Bit 1				
		...	...				
		Channel04underflow	Bit 6				
		Channel04overflow	Bit 7				
2099	-	Working range violation (pos.)	USINT		•		
		Channel01OutofRange	Bit 0				
		...	...				
		Channel04OutofRange	Bit 3				
518 + (N-1) * 32	-	Ch0NOverflow (index N = 1 to 4)	UINT		•		
522 + (N-1) * 32	-	Ch0NUnderflow (index N = 1 to 4)	UINT		•		
526 + (N-1) * 32	-	Ch0NOutofRange (index N = 1 to 4)	UINT		•		
Additional analysis functions							
133	-	ConfigOutput21 (trigger reaction on falling edge)	USINT				•
135	-	ConfigOutput22 (trigger reaction on rising edge)	USINT				•
129	-	Analysis control byte	USINT				•
		MinMaxStart01	Bit 4				
		...	...				
		MinMaxStart04	Bit 7				
129	-	Analysis status byte	USINT		•		

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
		MinMaxStart01Readback	Bit 4				
		...	...				
		MinMaxStart04Readback	Bit 7				
	Limit values						
530 + (N-1) * 32	-	MinInput0N (index N = 1 to 4)	INT		•		
534 + (N-1) * 32	-	MaxInput0N (index N = 1 to 4)	INT		•		
538 + (N-1) * 32	-	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		•		

1) The offset specifies the position of the register within the CAN object.

4.3.16.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.16.10.4 Configuration

This module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately from one another either on the voltage or current input for the following areas:

- Permitted voltage: ±11 V at 20 Ω
- Permitted current: 22 mA (maximum 40 mA) (<400 Ω)

4.3.16.10.4.1 Channel configuration

Name:
ConfigOutput01 for channel 01
ConfigOutput06 for channel 02
ConfigOutput11 for channel 03
ConfigOutput16 for channel 04

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using the correct terminal block pins.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±11 VDC
		1	Current terminal for 0 to 22 mA
1	Gain selector	0	Voltage ±11 VDC
		1	Current 0 to 22 mA
2 - 3	Reserved	-	
4	Filtering active (only if bit 7 = 0)	0	Inactive
		1	Active
5	Minimum/Maximum analysis active (only if bit 7 = 0)	0	Inactive
		1	Active
6	Error monitoring active (only if bit 7 = 0)	0	Inactive
		1	Active
7	Enables channel	0	Channel enabled
		1	Channel disabled

4.3.16.10.4.2 Sampling and conversion

The analog signal is sampled in 2 steps.

- **Conversion task**
  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.
  The timespan needed for conversion results from the set sampling time.
- **Processing task**
  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Function
UINT	50 to 10,000	Default value = 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

4.3.16.10.4.3 Filtering (optional)

If filtering is enabled in the 4.3.16.10.4.1 "Channel configuration" register, the basic data of the A/D converter is filtered per channel. The following registers are available to specify the filter order and respective cutoff frequency for configuring the low-pass filter:

- "Filter order"
- "Filter cutoff frequency"

Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2
ConfigOutput30 for channel 3
ConfigOutput32 for channel 4

The filter order is specified in this register. The "Filter cutoff frequency" register is used to configure the respective cutoff frequency of the filter.

Data type	Value
USINT	1 to 4

Internal filter orders greater than 1 are implemented as cascaded first-order filters. Since the filter is calculated in the sampling cycle, the filter characteristics are directly related to the settings for the sampling cycle time.

Calculating the cutoff frequency of an nth-order filter:

yn = a * xn + b * y(n-1)

Approximate calculation

a = Sampling time / (Sampling time + 1/Cutoff frequency)

b = 1 - a

Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2
ConfigOutput31 for channel 3
ConfigOutput33 for channel 4

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Description
UINT	1 to 65,535	Cutoff frequency in hertz

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

4.3.16.10.4.4 User-defined scaling

The raw and filtered A/D converter data is compared and normalized (gain = k, offset = d). In addition, user-defined normalization is available using the following registers:

- "User-defined gain" (= ku)
- "User-defined offset" (= du)

The execution time is optimized by grouping the factors together.

System scaling calculation:

nom = k * RawValue + d

k = k * ku

d = k * d + du

The value has to be limited since it can exceed the 16-bit constraints. To provide the greatest degree of flexibility, limiting is possible using the registers "Minimum limit value" and "Maximum limit value".

User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2
ConfigOutput14 for channel 3
ConfigOutput19 for channel 4

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65,536 (0x10000) corresponds to a gain of 1.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2
ConfigOutput15 for channel 3
ConfigOutput20 for channel 4

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65,536 (0x10000) corresponds to an offset of 1.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.3.16.10.4.5 Limit values

If the application requires a limitation of the range of values, then the user can define his own limit values. These values will also be use for the module's error statistics. The following registers are available for this:

- "Minimum limit value"
- "Maximum limit value"

Information:

32-bit numbers are used inside the module. A limit value violation can therefore also be determined if the permitted range of values was defined from -32768 to 32767.

Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2
ConfigOutput12 for channel 3
ConfigOutput17 for channel 4

The minimum limit value is configured in this register. This limit value is also used as the lower value in the error statistics (see register "Counter for range exceeded violations (neg.)").

Data type	Value
INT	-32768 to 32767

Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2
ConfigOutput13 for channel 3
ConfigOutput18 for channel 4

The maximum limit value is configured in this register. This limit value is also used as the upper value in the error statistics (see register "Counter for range exceeded violations (pos.)").

Data type	Value
INT	-32768 to 32767

4.3.16.10.5 Communication - General

The module's analog inputs convert current and voltage values with 16-bit resolution. This information can be used by the application with the help of the registers listed here.

4.3.16.10.5.1 Analog input channels

Name:
AnalogInput01 to AnalogInput04

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal ±11 VDC
	0 to 32,767	Current signal 0 to 22 mA

4.3.16.10.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Value
UINT	0 to 65535

4.3.16.10.5.3 Error monitoring and counters

Channel status

Name:
Channel01OK to Channel04OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors
...		...	
3	Channel04OK	0	OK
		1	Errors
4 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "Synchronization error counter".
2) Identical to bit 0 of the registers "Counter for faulty sampling cycles".

Synchronization error counter

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See 4.3.9.8.4.2 "Sampling and conversion".

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Range violation (neg. and pos.)

Name:
Channel01underflow to Channel04underflow
Channel01overflow to Channel04overflow

This register indicates whether a range violation (pos. and/or neg.) of the limit values defined in the registers "Minimum limit value" and "Maximum limit value" has occurred. The individual bits in this register are identical to the values of the lowest bits in the registers "Counter for range exceeded violations (neg.)" and "Counter for range exceeded violations (pos.)".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
...		...	
3	Channel04underflow	0	No error
		1	Range exceeded (.neg) on channel 4
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
...		...	
7	Channel04overflow	0	No error
		1	Range exceeded (.pos) on channel 4

Working range violation (pos.)

Name:
Channel01OutofRange to Channel04OutofRange

This register indicates whether the input value exceeds the module's maximum measurement range. The individual bits in this register are identical to the values of the lowest bits in the register "Counter for work range violations (pos.)".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutofRange	0	No error
		1	Working range violation (pos.) of channel 1
...		...	
3	Channel04OutofRange	0	No error
		1	Working range violation (pos.) of channel 4
4 - 7	Reserved	-	

Counter for work range violations (pos.)

Name:
CH01OutofRange to CH04OutofRange

Errors outside of the module's maximum possible measurement range are indicated in this register. These errors lead to full-scale deflection of the A/D converter.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.16.10.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (neg.)

Name:
CH01Underflow to CH04Underflow

This register indicates range exceeded violations (neg.) of the value configured in the register "Minimum limit value".

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.16.10.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (pos.)

Name:
CH01Overflow to CH04Overflow

This register indicates range exceeded violations (pos.) of the value configured in the register "Maximum limit value".

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register 4.3.16.10.4.1 "Channel configuration").

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

4.3.16.10.6 Additional analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

- **Limit value analysis**
  If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched internally in the module. A measurement period can be triggered using the control byte. When the respective configured edge is generated by the application, the limit values from the previous measurement period are displayed and the internal latch register is reset.
- **Recording sampled values**
  If recording sampled values has been enabled for a channel, then the sampled values are additionally recorded in the module's internal FIFO memory. If the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

It is only possible to use the recording of sampled values if the module is operated on an X2X master that is an SG4 CPU.

4.3.16.10.6.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register configures whether the falling edge is used to trigger the trace and determination of the input value in the register 4.3.15.10.6.3 "Analysis control byte".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination
		1	Falling edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination
		1	Falling edge determines input value of channel 4

4.3.16.10.6.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register configures whether the rising edge is used to trigger the trace and determination of the input value in the register 4.3.15.10.6.3 "Analysis control byte".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Rising edge does not initiate trigger
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination
		1	Rising edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination
		1	Rising edge determines input value of channel 4

4.3.16.10.6.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart04

The trace function and determination of the minimum/maximum input values can be started in this register.
Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers 4.3.15.10.6.1 "Trigger condition on falling edge" and 4.3.15.10.6.2 "Trigger condition on rising edge".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Does not initiate trigger/trace
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not initiated
		1	Initiates determination of input value of channel 1
...	...	...	
7	MinMaxStart04	0	Determination not initiated
		1	Initiates determination of input value of channel 4

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

4.3.16.10.6.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart04Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel
...	...	...	
7	MinMaxStart04Readback	0 or 1	Current state of the trigger bits for determining the limit values on the channel

4.3.16.10.7 Limit values

Limit value analysis must be enabled for the desired channel (see 4.3.16.10.4.1 "Channel configuration"). The sampled value of the channel is then compared to the minimum and maximum values that are stored internally in the module. If a new measurement period is initiated with the 4.3.15.10.6.3 "Analysis control byte" register, then the values determined from the previous measurement period can be taken from the respective registers intended for this.

4.3.16.10.7.1 Minimum input values

Name:
MinInput01 to MinInput04

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

4.3.16.10.7.2 Maximum input values

Name:
MaxInput01 to MaxInput04

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

4.3.16.10.7.3 Limit value trigger counter

Name:
CH01MinMaxLatchCounter to CH04MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

4.3.16.10.8 Trace

If the module is operated on a SG4 CPU, the digitalized input values are recorded by the module. The module must be operated in "Supervised" mode in order to use the trace function.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism can only be used if the module is connected directly to the CPU, not if it is operated behind a bus controller.

4.3.16.10.8.1 Enable recording

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
...	...	...	
3	Channel 4	0	Channel disabled
		1	Channel enabled
4 - 7	Reserved	-	

4.3.16.10.8.2 Number of values to be recorded

Name:
TraceSampleDepth

16 kB are available on the module for the trace. The FIFO memory limitation means that a maximum of 8192 analog values can be recorded. This memory is divided up equally among the enabled channels. The actual number of maximum possible recordings therefore depends on the number of channels enabled for trace:

1 channel enabled: Up to 8192 recordings
2 channels enabled: Up to 4096 recordings per channel
3 channels enabled: Up to 2730 recordings per channel
4 channels enabled: Up to 2048 recordings per channel

Data type	Value	Function
UINT	2 to 8192	Default value = 1024

4.3.16.10.8.3 Recording priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard (default value)
	6	Trace priority higher than X2X Link communication

4.3.16.10.8.4 Starting a recording

Name:

TraceEnable01

This register starts the recording according to the specifications for edge control or the comparator.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

4.3.16.10.8.5 Recording status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

4.3.16.10.8.6 Free trace buffer

Name:
FreeBufferSize

Specifies the available FIFO memory area in bytes for the trace

Data type	Value
UINT	0 to 65535

4.3.16.10.8.7 Counter for trace triggers

Name:
TriggerCount

This register indicates the number of triggers that have occurred since "starting the trace".

Data type	Value
UINT	0 to 65535

4.3.16.10.8.8 Counter for faulty recording triggers

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be performed.

Data type	Value
UINT	0 to 65535

4.3.16.10.8.9 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold value bits for all channels are grouped together in the lower-value byte of the "Hysteresis status of the channels" register. In addition, the states of the previous sampling are stored in the higher-value byte.

The 4 status messages of each channel can be linked according to the following logic via a logical connective mask using AND or OR operators and used as a trace trigger:

```
delta = (Current_HysteresisStatus ^ NominalValues) // Different between current status and preset
cond = delta & Selected_HysteresisStatusBits // Eliminate irrelevant status messages
ccond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if ((0 == (cond & ~LogicalOperators)) &&
(0 != (~cond & LogicalOperators))) { => Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	cfgComp_EnableMask
Current_HysteresisStatus	CompStateCollection
Nominal values	cfgComp_NominalState
Logical operators	cfgComp_ConditionTypeMask

Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh04

The lower limit value for hysteresis is configured in this register.

Data type	Value
INT	-32768 to 32767

Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh04

The upper limit value for hysteresis is configured in this register.

Data type	Value
INT	-32768 to 32767

Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values

Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values

Information:

This is a "whitelist", i.e. the trace starts as soon as the current status message takes on the state predefined here.

One or more matches will be necessary depending on the selection of the relevant hysteresis status bits and logical connective operators.

Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register selects which status bits of the hysteresis comparison should be used to generate the trigger.

For more information about using this register, see 4.3.15.10.8.9 "Comparator for trigger conditions".

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
7	Channel04 InRange status in the current cycle	0	Do not use
		1	Use for generation
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
15	Channel04 InRange status in the last cycle	0	Do not use
		1	Use for generation

Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

The desired state operators with which the respective status bit is linked to others to generate a trigger are selected in this register.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "Selecting the relevant hysteresis status bits" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
7	Channel04 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
15	Channel04 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation

4.3.16.10.8.10 Time-offset trace

Additional conditions for shifting the starting and stopping points can be defined if the trace should be chronologically offset to the trigger.

Starting the trace

Name:
TraceTriggerStart

The starting position is defined relative to the configured trigger condition (rising/falling edge) in this register. Positive values mean that the trace takes place x samples after the trigger condition. Negative values mean that the trace takes place x samples before the trigger condition.

The value -32768 performs the trace without regard for the configured trigger condition. If the trace memory is completely full, then the oldest recorded value is overwritten (FIFO principle).

"Trace start" in the I/O configuration or the registers 4.3.15.10.6.1 "Trigger condition on falling edge" and 4.3.15.10.6.2 "Trigger condition on rising edge" determine whether a positive, negative or any edge must be triggered.

Data type	Value
INT	-32768 to 32767

Stopping the trace

Name:
TraceTriggerStop

The stopping position is defined relative to the configured trigger condition in this register.

- When configuring an early trigger event, this value refers to the trigger event.
- When configuring a delayed trigger event, this value refers to the starting event.

Data type	Value
UINT	0 to 65535

4.3.16.10.9 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

4.3.16.10.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Standard priority	200 µs
High priority with trace function	300 µs

4.3.16.10.11 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

4.3.17 X20AI4636

4.3.17.1 General information

The module is equipped with 4 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminal connections. With the oversampling function, up to 16 analog values per channel can be recorded.

- 4 analog inputs
- Current or voltage signal configuration for the entire module
- 16-bit digital converter resolution
- Minimum conversion time of 40 µs for all inputs
- The conversion time for the entire module can be configured in 0.02 µs steps.
- Maximum 14 samples (16-bit) for the entire module per X2X Link cycle
- Oversampling: Up to 16 analog values per channel (internal)
- Timestamp for the last conversion of an X2X Link cycle

4.3.17.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI4636	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 60: X20AI4636 - Order data

4.3.17.3 Technical data

Product ID	X20AI4636
Short description	
I/O module	4 analog inputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0xB3A8
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W [1]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	40 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permitted input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of the digital value during overload	
Below lower limit	
Voltage	0x8001
Current	0x0000
Above upper limit	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - 3rd-order low pass / cutoff frequency 10 kHz
Max. error at 25°C	
Voltage	
Gain	0.08% [3]
Offset	0.01% [4]
Current	
Gain	0.08% [3]
Offset	0.02% [5]
Max. gain drift	
Voltage	0.01 %/°C [3]
Current	0.01 %/°C [3]
Max. offset drift	
Voltage	0.001 %/°C [4]
Current	0.002 %/°C [5]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB

Table 61: X20AI4636 - Technical data

Product ID	X20AI4636
Nonlinearity	
Voltage	<0.01% 4)
Current	<0.015% 5)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 61: X20AI4636 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 20 V measurement range.
5) Based on the 20 mA measurement range.

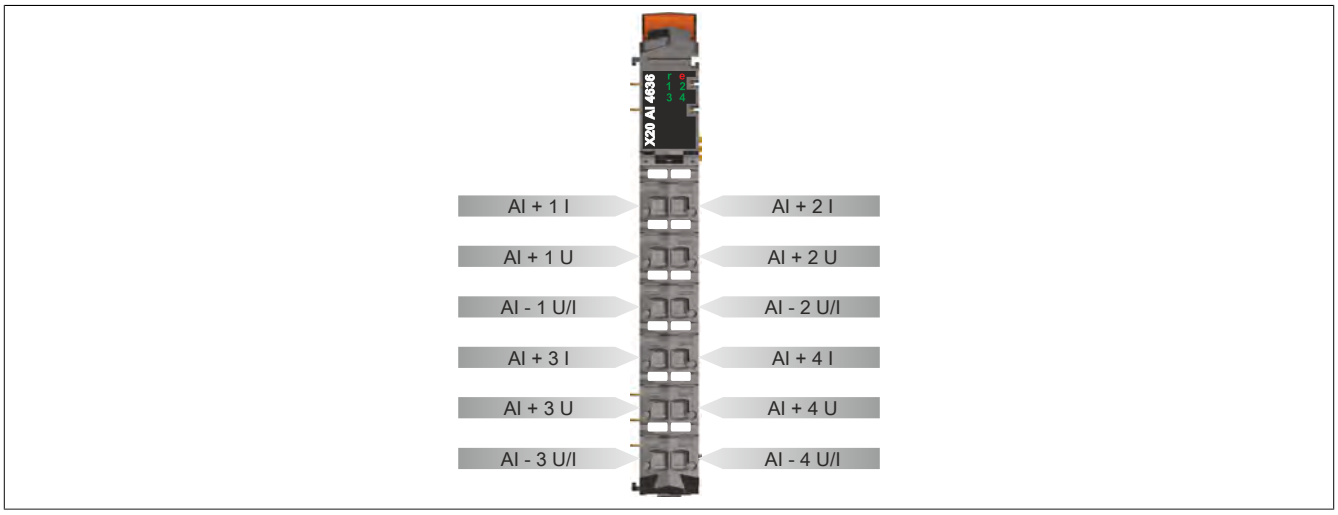
4.3.17.4 Status LEDs

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the sampling cycle time • Synchronization error
		Green	Off	Open line2) or sensor is disconnected
			Blinking	Channel error: Underflow, overflow or broken connection
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

4.3.17.5 Pinout

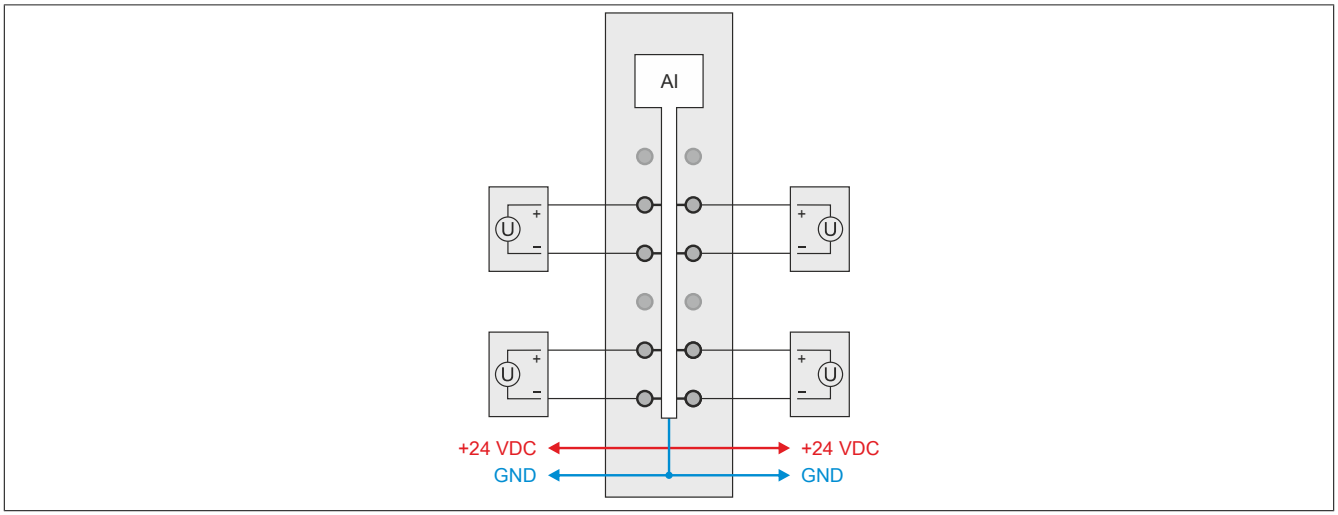


4.3.17.6 Connection example

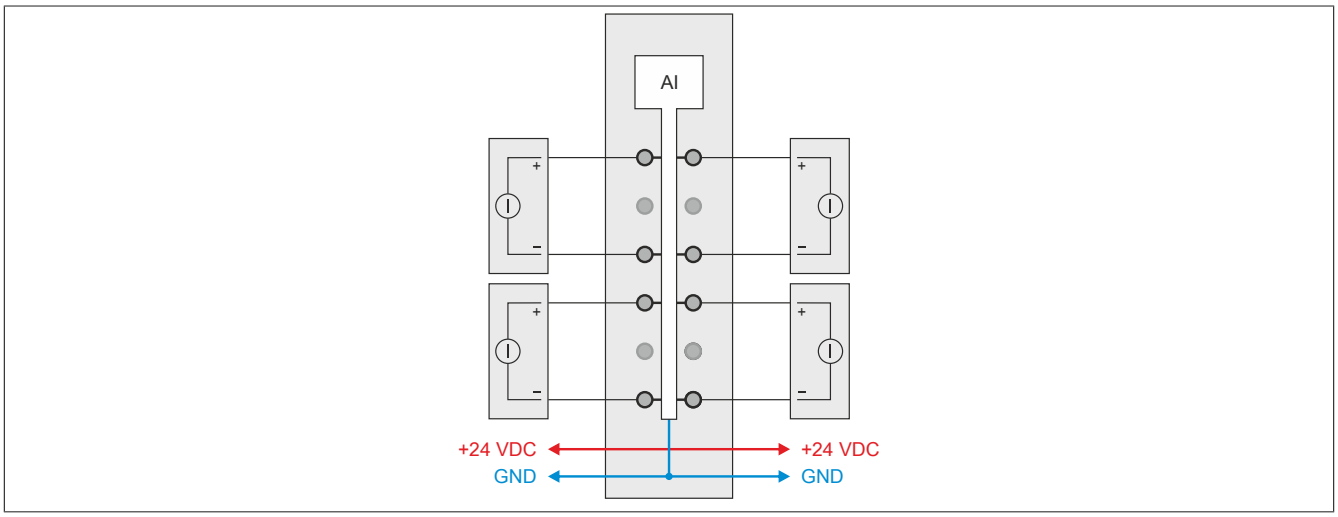
To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Supply module X20PS9500/X20PS9502
- CPU modules

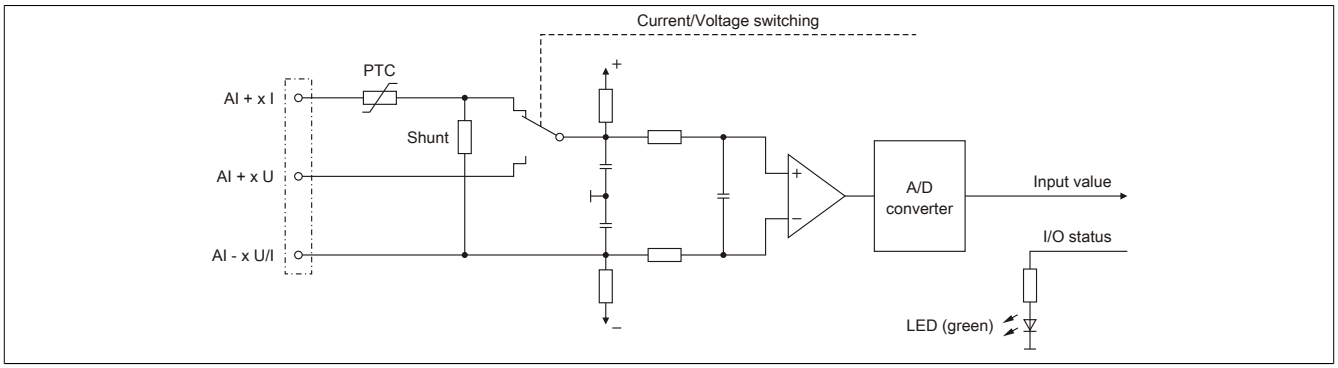
Voltage measurement



Current measurement



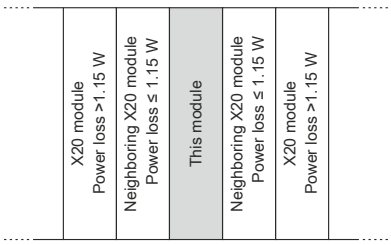
4.3.17.7 Input circuit diagram



4.3.17.8 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.3.17.9 Register description

4.3.17.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.17.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
System configuration						
513	CfO_BaseConfig	USINT				•
15364	CfO_CycleTime	UDINT				•
15370	CfO_SyncOffset	UINT				•
15374	CfO_Prescaler	UINT				•
Error messages - Configuration						
385	CfO_ErrorID0007	USINT				•
387	CfO_ErrorID080F	USINT				•
389	CfO_ErrorID1017	USINT				•
Physical channel configuration						
8194 + (N-1) * 256	CfO_ModeCh0N (index N = 1 to 4)	UINT				•
8204 + (N-1) * 256	CfO_UserGainCh0N (index N = 1 to 4)	DINT				•
8212 + (N-1) * 256	CfO_UserOffsetCh0N (index N = 1 to 4)	DINT				•
8220 + (N-1) * 256	CfO_Alpha0Ch0N (index N = 1 to 4)	DINT				•
8228 + (N-1) * 256	CfO_Alpha1Ch0N (index N = 1 to 4)	DINT				•
8236 + (N-1) * 256	CfO_Alpha2Ch0N (index N = 1 to 4)	DINT				•
8244 + (N-1) * 256	CfO_Beta1Ch0N (index N = 1 to 4)	DINT				•
8252 + (N-1) * 256	CfO_Beta2Ch0N (index N = 1 to 4)	DINT				•
8198 + (N-1) * 256	CfO_CutOffFrequCh0N (index N = 1 to 4)	UINT				•
Logical channel configuration						
10242 + (N-1) * 256	CfO_LogCh0NMode (index N = 1 to 6)	UINT				•
10245 + (N-1) * 256	CfO_LogCh0NSource00 (index N = 1 to 6)	USINT				•
10247 + (N-1) * 256	CfO_LogCh0NSource01 (index N = 1 to 6)	USINT				•
10260 + (N-1) * 256	CfO_LogCh0NFuncPar00 (index N = 1 to 6)	UDINT				•
10268 + (N-1) * 256	CfO_LogCh0NFuncPar01 (index N = 1 to 6)	UDINT				•
Analog inputs - Communication						
5062 + (N-1) * 8	AnalogInput0N (index N = 1 to 4)	INT	•			
Error messages - Communication						
261	"StandardErrors" registers	USINT	•			
	Channel01Error	Bit 0				
	...	...				
	Channel04Error	Bit 3				
	PhysicalError	Bit 4				
	LogicalError	Bit 5				
325	"AcknowledgeStandardErrors" registers	USINT			•	
	AckChannel01Error	Bit 0				
	...	...				
	AckChannel04Error	Bit 3				
	AckPhysicalError	Bit 4				
	AckLogicalError	Bit 5				
257	"ExtendedChannelErrorMessages" registers	USINT	•			
	Channel01OutOfRange	Bit 0				
	Channel01FilterError	Bit 1				
	Channel01Underflow	Bit 2				
	Channel01Overflow	Bit 3				
	Channel02OutOfRange	Bit 4				
	Channel02FilterError	Bit 5				
	Channel02Underflow	Bit 6				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
	Channel02Overflow	Bit 7				
321	"AcknowledgeExtendedChannelErrorMessages" registers	USINT			•	
	AckChannel01OutOfRange	Bit 0				
	AckChannel01FilterError	Bit 1				
	AckChannel01Underflow	Bit 2				
	AckChannel01Overflow	Bit 3				
	AckChannel02OutOfRange	Bit 4				
	AckChannel02FilterError	Bit 5				
	AckChannel02Underflow	Bit 6				
	AckChannel02Overflow	Bit 7				
259	"ExtendedChannelErrorMessages" registers	USINT	•			
	Channel03OutOfRange	Bit 0				
	Channel03FilterError	Bit 1				
	Channel03underflow	Bit 2				
	Channel03Overflow	Bit 3				
	Channel04OutOfRange	Bit 4				
	Channel04FilterError	Bit 5				
	Channel04Underflow	Bit 6				
	Channel04Overflow	Bit 7				
323	"AcknowledgeExtendedChannelErrorMessages" registers	USINT			•	
	AckChannel03OutOfRange	Bit 0				
	AckChannel03FilterError	Bit 1				
	AckChannel03Underflow	Bit 2				
	AckChannel03Overflow	Bit 3				
	AckChannel04OutOfRange	Bit 4				
	AckChannel04FilterError	Bit 5				
	AckChannel04Underflow	Bit 6				
	AckChannel04Overflow	Bit 7				
Physical analog sample display						
4102 + (16-N) * 64	PhysCh01SampleN (index N = 1 to 16)	INT	•			
4110 + (16-N) * 64	PhysCh02SampleN (index N = 1 to 16)	INT	•			
4118 + (16-N) * 64	PhysCh03SampleN (index N = 1 to 16)	INT	•			
4126 + (16-N) * 64	PhysCh04SampleN (index N = 1 to 16)	INT	•			
5106	PhysTimestamp	INT	•			
5108	PhysTimestamp	DINT	•			
5113	PhysSampleCount	SINT	•			
5114	PhysSampleCount	INT	•			
Logical analog and digital sample display						
6148 + (16-N) * 64	LogicCh01SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6150 + (16-N) * 64	LogicCh01SampleN (index N = 1 to 16) (16-bit)	INT	•			
6156 + (16-N)*64	LogicCh02SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6158 + (16-N)*64	LogicCh02SampleN (index N = 1 to 16) (16-bit)	INT	•			
6164 + (16-N)*64	LogicCh03SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6166 + (16-N)*64	LogicCh03SampleN (index N = 1 to 16) (16-bit)	INT	•			
6172 + (16-N)*64	LogicCh04SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6174 + (16-N)*64	LogicCh04SampleN (index N = 1 to 16) (16-bit)	INT	•			
6180 + (16-N)*64	LogicCh05SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6182 + (N-16)*64	LogicCh05SampleN (index N = 1 to 16) (16-bit)	INT	•			
6188 + (16-N)*64	LogicCh06SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6190 + (16-N)*64	LogicCh06SampleN (index N = 1 to 16) (16-bit)	INT	•			
7109 + (N-1) * 8	LogicCh0NSample16_9 (index N = 1 to 5)	USINT	•			
7151	LogicCh06Sample16_9	USINT	•			
7111 + (N-1) * 8	LogicCh0NSample8_1 (index N = 1 to 5)	USINT	•			
7149	LogicCh06Sample8_1	USINT	•			
7154	LogicTimestamp	INT	•			
7156	LogicTimestamp	DINT	•			
7161	LogicSampleCount	SINT	•			
7162	LogicSampleCount	INT	•			

4.3.17.9.3 Function model 254 - Bus controller

The "Bus controller" function model has the following limitations compared to the "Standard" function model:

- No oversampling function since consistency is not possible when operating CAN-based bus controllers due to the limited data range
- The sampling cycle time is set to 100 µs.
- No timestamp function
- A range of logical functions is available for processing the physical values right on the module:
  - Output of physical values (standard)
  - Addition of two channels with scaling
  - Integral addition of two channels with scaling
  - Multiplication of two channels with scaling
  - Integral multiplication of two channels with scaling

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
System configuration							
513	-	CfO_BaseConfig	USINT				•
15364	-	CfO_CycleTime	UDINT				•
15370	-	CfO_SyncOffset	UINT				•
15374	-	CfO_Prescaler	UINT				•
Error messages - Configuration							
385	-	CfO_ErrorID0007	USINT				•
387	-	CfO_ErrorID080F	USINT				•
389	-	CfO_ErrorID1017	USINT				•
Physical channel configuration							
8194 + (N-1) * 256	-	CfO_ModeCh0N (index N = 1 to 4)	UINT				•
8204 + (N-1) * 256	-	CfO_UserGainCh0N (index N = 1 to 4)	DINT				•
8212 + (N-1) * 256	-	CfO_UserOffsetCh0N (index N = 1 to 4)	DINT				•
8220 + (N-1) * 256	-	CfO_Alpha0Ch0N (index N = 1 to 4)	DINT				•
8236 + (N-1) * 256	-	CfO_Alpha2Ch0N (index N = 1 to 4)	DINT				•
8244 + (N-1) * 256	-	CfO_Beta1Ch0N (index N = 1 to 4)	DINT				•
8252 + (N-1) * 256	-	CfO_Beta2Ch0N (index N = 1 to 4)	DINT				•
8198 + (N-1) * 256	-	CfO_CutOffFrequCh0N (index N = 1 to 4)	UINT				•
Logical channel configuration							
10242 + (N-1) * 256	-	CfO_LogCh0NMode (index N = 1 to (index N = 1 to 4))	UINT				•
10245 + (N-1) * 256	-	CfO_LogCh0NSource00 (index N = 1 to 6)	USINT				•
10247 + (N-1) * 256	-	CfO_LogCh0NSource01 (index N = 1 to 6)	USINT				•
10260 + (N-1) * 256	-	CfO_LogCh0NFuncPar00 (index N = 1 to 6)	UDINT				•
10268 + (N-1) * 256	-	CfO_LogCh0NFuncPar01 (index N = 1 to 6)	UDINT				•
Analog inputs - Communication							
5062 + (N-1) * 8	(N-1) * 2	AnalogInput0N (index N = 1 to 4)	INT	•			
Error messages - Communication							
261	-	"StandardErrors" registers	USINT		•		
		Channel01Error	Bit 0				
		...	...				
		Channel04Error	Bit 3				
		PhysicalError	Bit 4				
		LogicalError	Bit 5				
325	-	"AcknowledgeStandardErrors" registers	USINT				•
		AckChannel01Error	Bit 0				
		...	...				
		AckChannel04Error	Bit 3				
		AckPhysicalError	Bit 4				
		AckLogicalError	Bit 5				
257	-	"ExtendedChannelErrorMessages" registers	USINT		•		
		Channel01OutOfRange	Bit 0				
		Channel01FilterError	Bit 1				

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
		Channel01Underflow	Bit 2				
		Channel01Overflow	Bit 3				
		Channel02OutOfRange	Bit 4				
		Channel02FilterError	Bit 5				
		Channel02Underflow	Bit 6				
		Channel02Overflow	Bit 7				
321	-	"AcknowledgeExtendedChannelErrorMessages" registers	USINT				•
		AckChannel01OutOfRange	Bit 0				
		AckChannel01FilterError	Bit 1				
		AckChannel01Underflow	Bit 2				
		AckChannel01Overflow	Bit 3				
		AckChannel02OutOfRange	Bit 4				
		AckChannel02FilterError	Bit 5				
		AckChannel02Underflow	Bit 6				
		AckChannel02Overflow	Bit 7				
259	-	"ExtendedChannelErrorMessages" registers	USINT		•		
		Channel03OutOfRange	Bit 0				
		Channel03FilterError	Bit 1				
		Channel03underflow	Bit 2				
		Channel03Overflow	Bit 3				
		Channel04OutOfRange	Bit 4				
		Channel04FilterError	Bit 5				
		Channel04Underflow	Bit 6				
		Channel04Overflow	Bit 7				
323	-	"AcknowledgeExtendedChannelErrorMessages" registers	USINT				•
		AckChannel03OutOfRange	Bit 0				
		AckChannel03FilterError	Bit 1				
		AckChannel03Underflow	Bit 2				
		AckChannel03Overflow	Bit 3				
		AckChannel04OutOfRange	Bit 4				
		AckChannel04FilterError	Bit 5				
		AckChannel04Underflow	Bit 6				
		AckChannel04Overflow	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.3.17.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.3.17.9.4 General information

There is a difference on the module between physical (default) and logical values:

Physical or default values
The conversion results are transferred to the higher-level system after being scaled and filtered. They are not processed further.

Logical values
The physical values can be further processed with mathematical functions and comparators. In addition, another logical channel can be used as a starting point to further process a logical function.

4.3.17.9.5 Operating mode - Oversampling

The input values are recorded with a configurable sampling cycle time and saved with timestamp to the internal physical data buffer. This data range can then be read out in the cyclic data transfer using a configurable data length.

The recording and transmission system for the logical channels is identical to that for the physical channels. The functions of the logical channels are also executed in the configured sampling cycle time and saved with timestamp to the logical data buffer. The values can also be read out from here using configurable cyclic data points.

The defined sampling cycle time may not be sufficient for the sum of all physical and logical functions if using fast X2X Link cycle times, however. If influencing the physical sampling is not permitted, then a prescaler can be used to slow down the logical processing.

Information:

The ability to adjust the sampling cycle time as needed on the module means there is basically no synchronization with X2X Link, regardless of whether standard inputs or an oversampling function is configured.

If synchronization is required, then the configured sampling cycle time must be a multiple of the X2X Link cycle time!

4.3.17.9.5.1 Analog oversampling

When using analog oversampling, the enabled channels are stored in the module within a configurable time frame independently of the X2X cycle. Space is available for 16 analog values per physical and logical channel.

These samplings are are numbered from 1 to 16 for the registers. The conversions or calculations of individual channels with the same number (i.e. sample line 1 to 16, e.g. PhysCh01Sample**10**, PhysCh02Sample**10**, etc.) are derived from the same sampling cycle or logical computing cycle and therefore have the same timestamp.

The timestamp refers to the newest data value, i.e. always to sample line 1. If a timestamp for older data points is needed, it needs to be back-calculated in the application using the sampling cycle time configured on the module. The prescaler must also be taken into account for logical channels.

Calculation example

Sample line	Calculation	
1	Timestamp	**Newest value**
2	Timestamp - Sampling cycle time	
3	Timestamp - 2 * Sampling cycle time	
4	Timestamp - 3 * Sampling cycle time	
...	...	
10	Timestamp - 9 * Sampling cycle time	
...	...	
16	Timestamp - 15 * Sampling cycle time	**Oldest value**

How the buffer is organized can be seen from this. This is not a FIFO buffer but a static buffer that the values are pushed through. Sample line 1 always contains the newest values, the next line the second newest, all the way up to sample line 16, which contains the oldest values.

The sample counter is a circular counter, with the number of new sample lines derived from the value of the last transfer cycle.

Example

A difference of 3 to the last transfer cycle means:

The data in sample line 1 and all subsequent data from the previous transfer cycle is now shifted in the current cycle beginning with sample line 4. Sample lines 1 through 3 contain the new values for further processing by the application. Sample lines 14 through 16 from the last transfer cycle are no longer in the buffer.

4.3.17.9.5.2 Comparator oversampling

When using comparator oversampling, the results of the enabled channels are stored in the module within a configurable time frame independently of the X2X cycle. 16 bits of memory space are available per logical channel.

These samplings (i.e. event bits) are consecutively numbered from 1 to 8 and 9 to 16 for the two registers. The results of individual channels with the same number (i.e. sample line 1 to 16, e.g. for channel 1 LogicCh01Sample**16_9** and LogicCh01Sample**8_1**) are derived from the same sampling cycle or logical computing cycle and therefore have the same timestamp.

The timestamp refers to the newest data value, i.e. always to sample line 1 (i.e. bit 0 in the LogicCh01Sample8_1 register). If a timestamp for older comparator results is needed, it needs to be back-calculated in the application using the sampling cycle time configured on the module. The prescaler must also be taken into account.

Calculation example

Sample line	(register name)	Calculation	
1	(LogicCh01Sample8_1 bit 0)	Timestamp	**Newest value**
2	(LogicCh01Sample8_1 bit 1)	Timestamp - Sampling cycle time	
3	(LogicCh01Sample8_1 bit 2)	Timestamp - 2 * Sampling cycle time	
4	(LogicCh01Sample8_1 bit 3)	Timestamp - 3 * Sampling cycle time	
...			
10	(LogicCh01Sample16_9 bit 1)	Timestamp - 9 * Sampling cycle time	
...			
16	(LogicCh01Sample16_9 bit 7)	Timestamp - 15 * Sampling cycle time	**Oldest value**

How the buffer is organized can be seen from this. This is not a FIFO buffer but a static buffer that the values are pushed through. Sample line 1 always contains the newest values, the next line the second newest, all the way up to sample line 16, which contains the oldest values.

The sample counter is a circular counter, with the number of new sample lines derived from the value of the last transfer cycle.

Example

A difference of 3 to the last transfer cycle means:

The comparator result in sample line 1 and all subsequent data from the previous transfer cycle is now shifted in the current cycle beginning with sample line 4. Sample lines 1 through 3 contain the new bit values for further processing by the application. Sample lines 14 through 16 from the last transfer cycle are no longer in the buffer.

Data transfer

The analog conversion rate / sampling cycle time can be considerably faster than the X2X Link cycle. Saved analog or comparator data can be transferred to the higher-level system synchronously and consistently.

In the application, it's important that the relationship between cyclic data points, the sampling cycle time on the module and the transfer time is sufficient to read all of the new data points on the higher-level system.

The sample counter can be used to check how many data values are actually new since the last transfer cycle. If the counter difference to the previous cycle is larger than the number of existing cyclic data points, then values have been overlooked and the system needs to be adjusted.

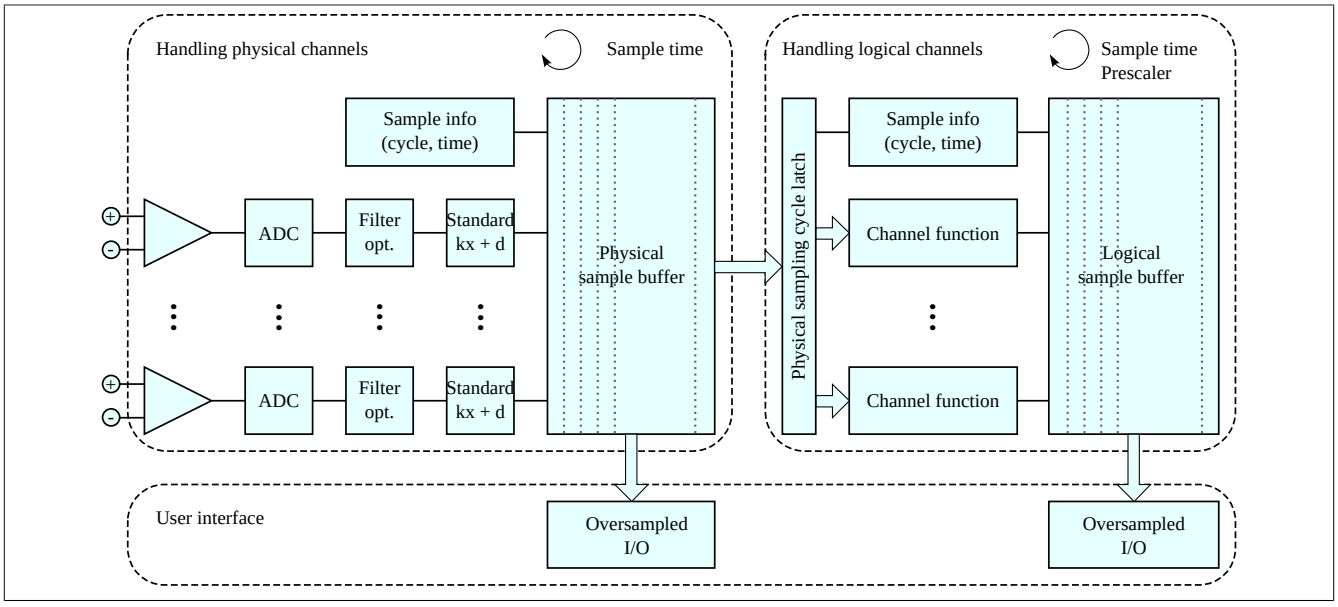
The general guideline is that a cyclic data point should be configured more than is actually required computing-wise.

Example with synchronous settings

- Sampling cycle time = 50 µs
- X2X Link cycle time = 500 µs

Samples 1 to 10 of a channel are possible to calculate in this example. Sample 11 should also be configured as a cyclic data point, however.
The reason for this is the possible jitter in the module caused by interruptions, e.g. from the X2X Link transfer. For the current cycle, this can mean that only 9 new values are available and that 11 values will have to be transferred in the next cycle.

For logical comparator functions, this problem doesn't exist since the maximum number is always transferred in the cycle data range.



4.3.17.9.6 Bus controller operating mode

The input values are recorded with a configurable sampling cycle time and saved with timestamp to the internal physical data buffer. Only the newest value will be transferred in the next possible bus cycle.

Limitations in the bus controller function model:

- No oversampling function since consistency is not possible due to the limited data range
- Sampling cycle time configured to 100 µs by default
- Range of logical functions available for processing physical values directly on the module
- Timestamp not available

4.3.17.9.7 "AnalogInput" registers

Name:
AnalogInput01 to AnalogInput04

This module can be configured and operated as a normal analog input module without logical auxiliary functions. The physical values from the last sampling cycle are used as input values in this case.

The module is operated as a normal analog input module in the bus controller function model. Nevertheless, it is still possible to connect each input channel directly to a logical function. The analog data on the bus controller is mapped using the calculation abilities of the logical channels and configured automatically (see 4.3.11.8.14.2 "Operation in the bus controller function model ").

Analog input values are displayed as signed 16-bit values depending on the configured operating mode.

Data type	Value	Information
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 mA to 20 mA

Information:

It is important to note that the oversampling function is not available in the bus controller function model due to the amount of data and lack of consistency!

4.3.17.9.8 Physical sampling

This module has a data buffer with 16 entries for each of the physical input channels. This buffer is processed according to the configured sampling cycle time.

A maximum of only 30 bytes is available for cyclic transfer on the X2X bus, however. Minus the status and sample counter, this allows only a selection of 14 samples (with a 16-bit data width) from the physical and logical buffer to be transferred.
Data loss can therefore occur with an imprecise selection and configuration.

Example

Displaying continuous sample lines.

- Sampling cycle time = 100 µs
- X2X cycle time = 500 µs

Sample line 1	PhysCh0xSample1
Sample line 2	PhysCh0xSample2
Sample line 3	PhysCh0xSample3
Sample line 4	PhysCh0xSample4
Sample line 5	PhysCh0xSample5
Sample line 6	PhysCh0xSample6
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 2	New values in sample line 1 and sample line 2
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5

Information:

It is important to note that the sample counter refers to the update of the sample lines in the data buffer and not to the number of values transferred cyclically.

Displaying each second sample line to bridge a higher recording duration:

- Sampling cycle time = 100 µs
- X2X cycle time = 1000 µs

Sample line 1	PhysCh0xSample1
Sample line 3	PhysCh0xSample3
Sample line 5	PhysCh0xSample5
Sample line 7	PhysCh0xSample7
Sample line 9	PhysCh0xSample9
Sample line 11	PhysCh0xSample11
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 3	New values in sample line 1 and sample line 3
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5
...	
Difference SampleCount = 9	New values in sample line 1 to sample line 9

4.3.17.9.8.1 "PhysChSample" registers

Name:
PhysCh01Sample1 to PhysCh01Sample16
...
PhysCh04Sample1 to PhysCh04Sample16

These registers are the physical buffer registers of the analog channels. 16 registers are available for each channel. Sample 1 is the newest value; sample 16 is the oldest.

Analog input values are displayed as signed 16-bit values.

Data type	Value	Information
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 mA to 20 mA

4.3.17.9.8.2 "PhysSampleCount" register

Name:
PhysSampleCount

This register is an integer counter that is increased as soon as the module has saved a new physical sample line. The number of new sample lines is calculated from the difference to the previous cycle.

Data type	Value
SINT	-128 to 127
INT	-32,768 to 32,767

4.3.17.9.8.3 "PhysTimestamp" register

Name:
PhysTimestamp

This register returns the timestamp of the values currently being determined as signed values in µs. This data point is the timestamp of the physical sample line 1.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.3.17.9.9 Logical sampling

The module has a data buffer with 16 entries for each of the 6 logical channels. This buffer is processed according to the configured sampling cycle time. In addition, it's also possible to adjust the logical execution cycle using a prescaler for the sampling cycle time.

A maximum of only 30 bytes is available for cyclic transfer on the X2X bus, however. Minus the status and sample counter, this allows only a selection of 14 samples (with a 16-bit data width) from the physical and logical buffer to be transferred. For the logical channels, it is also possible to configure a 32-bit data width.
Data loss can therefore occur with an imprecise selection and configuration.

Example

Displaying continuous sample lines.

- Sampling cycle time = 100 µs
- X2X cycle time = 500 µs

Sample line 1	LogicCh0xSample1
Sample line 2	LogicCh0xSample2
Sample line 3	LogicCh0xSample3
Sample line 4	LogicCh0xSample4
Sample line 5	LogicCh0xSample5
Sample line 6	LogicCh0xSample6
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 2	New values in sample line 1 and sample line 2
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5

Information:

It is important to note that the sample counter refers to the update of the sample lines in the data buffer and not to the number of values transferred cyclically.

Displaying each second sample line to bridge a higher recording duration:

- Sampling cycle time = 100 µs
- X2X cycle time = 1000 µs

Sample line 1	LogicCh0xSample1
Sample line 3	LogicCh0xSample3
Sample line 5	LogicCh0xSample5
Sample line 7	LogicCh0xSample7
Sample line 9	LogicCh0xSample9
Sample line 11	LogicCh0xSample11
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 3	New values in sample line 1 and sample line 3
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5
...	
Difference SampleCount = 9	New values in sample line 1 to sample line 9

4.3.17.9.9.1 "LogicChSample8_1" registers

Name:
LogicCh01Sample8_1 to LogicCh06Sample8_1

These registers are used to represent the results of samples 1 to 8 of the logical digital comparator for the logical channels. Each of these bits corresponds to a sample line, with sample 1 the newest and Sample 8 the oldest comparator comparison. The results of samples 9 to 16 are represented in 4.3.11.8.9.2 ""LogicChSample16_9" registers".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator result	x	Sample 1
...	...		
7	Comparator result	x	Sample 8

4.3.17.9.9.2 "LogicChSample16_9" registers

Name:
LogicCh01Sample16_9 to LogicCh06Sample16_9

These registers are used to represent the results of samples 9 to 16 of the logical digital comparator for the logical channels. Each of these bits corresponds to a sample line, with sample 9 the newest and Sample 16 the oldest comparator comparison. The results of samples 1 to 8 are represented in 4.3.11.8.9.3 ""LogicChSample8_1" registers".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator result	x	Sample 9
...	...		
7	Comparator result	x	Sample 16

4.3.17.9.9.3 "LogicChSample" registers

Name:
LogicCh01Sample1 to LogicCh01Sample16
...
LogicCh06Sample1 to LogicCh06Sample16

These registers are the buffer registers of the logical input channels. 16 registers are available for each channel. Sample 1 is the newest value; sample 16 is the oldest.

Calculated values are displayed as signed 16- or 32-bit values depending on the register being used.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.3.17.9.9.4 "LogicSampleCount" register

Name:
LogicSampleCount

This register is an integer counter that is increased as soon as the module has saved a new logical sample line. The number of new sample lines is calculated from the difference to the previous cycle.

Data type	Value
SINT	-128 to 127
INT	-32,768 to 32,767

4.3.17.9.9.5 "LogicTimestamp" register

Name:
LogicTimestamp

This register returns the timestamp of the values currently being determined as signed 2 or 4-byte values in µs. This data point is the timestamp of the logical sample line 1.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.3.17.9.10 System configuration

The following registers are used to configure the module's system settings.

4.3.17.9.10.1 Register "CfO_BaseConfig"

Name:
CfO_BaseConfig

This register can be used to configure settings for handling logical oversampling and data acquisition.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	"Display configuration for logical values active/inactive" in the AS I/O configuration	0	Inactive
		1	Active
1	"Logical handling priority" in the AS I/O configuration	0	Low
		1	High
2 - 3	Reserved	-	
4	"Physical input mode" in the AS I/O configuration	0	Newest value
		1	Referenced value (reference = prescaled system timer)
5	"Logical input mode" in the AS I/O configuration	0	Newest value
		1	Referenced value (reference = prescaled system timer)
6 - 7	Reserved	-	

Priority of logical oversampling

- Low priority setting
  Logical and physical buffers are not processed in the same context. If the calculation time that results in the logical oversampling is higher than the configured sampling cycle time, this setting and a prescaler > 1 can be used to split up the logical processing over several sampling cycles. In this way, the sample lines of the physical and logical oversampling are not automatically acquired or calculated at the same point in time. If the prescaler is configured incorrectly, the logical oversampling cannot be processed successfully.
- High priority setting
  Logical and physical buffers are processed in the same context. The sample lines of the physical and logical oversampling are acquired and calculated at the same point in time. It must be possible to execute all configured functions in the configured sampling cycle time; otherwise, a cycle time violation will occur and the configuration must be changed accordingly. Configuring the logical prescaler doesn't have any effect here; only the data traffic in the logical oversampling is limited.

Current or referenced values for logical or physical oversampling

In a system being used to capacity, jitter in the sampling cycle on the module can also be caused by the necessary processing of functions (X2X Link operation, logical and physical oversampling) when the cycle time is set to synchronous. This results in a varying number of sample lines in the same time period. For this reason, more samples should also be configured in the cyclic image than are actually necessary to compute.

- Current values setting
  Passing on the sample lines to the higher-level system takes place as quickly as possible, with fewer or more sample lines possibly occurring.
- Referenced values setting
  This setting minimizes jitter and makes it possible to expect a constant number of new sample lines per cycle when configured optimally. With regard to response time, however, delays of several sampling cycles may occur.

4.3.17.9.10.2 Register "CfO_CycleTime"

Name:
CfO_CycleTime
"Physical sample time" in the AS I/O configuration.

This register configures the module's sampling cycle time. The format is a 16.16-bit unsigned 4-byte value, with the high word representing the integer part of the µs value and the low word the decimal places. The decimal places allow a closer alignment to the X2X cycle time. The absolute resolution is 1 µs.

Input value = Time in µs * 65536 data type

Data type	Value	Information
UDINT	2,621,440 to 2,147,483,647	40 µs to 32 ms sampling cycle time
	6,553,600	100 µs (default value)

4.3.17.9.10.3 Register "CfO_Prescaler"

Name:
CfO_Prescaler

This register contains the prescaler for configuring the logical channel processing time. The actual logical cycle time will be calculated from the multiple of the sampling cycle time that is defined here. If a very short sampling cycle time is required for physical samples, then the module load can be reduced using the second time base for the logical samples.

Data type	Value	Information
UINT	1 to 10	Multiple of the physical sampling cycle for logical processing
	0	Default value in the standard function model
	2	Default value in the bus controller function model

4.3.17.9.10.4 Register "CfO_SyncOffset"

Name:
CfO_SyncOffset
"Synchronization offset" in the AS I/O configuration.

The system cycle can be offset in 1 µs steps in this register.

Data type	Value	Information
UINT	-32,768 to 32,767	Synchronization offset in µs (default = 0)

4.3.17.9.11 Scaling

Analog input channels are naturally aligned and normalized when delivered (gain = k; offset = d). In addition, user-defined standardization is also available (gain = ku, offset = du). The calculation is optimized by grouping the factors together.

Normalization calculation:

nom = k * RawValue + d

k = k * ku

d = k * d + du

The values calculated here are limited to 16 bits.

4.3.17.9.11.1 "CfO_UserGainCh" registers

Name:
CfO_UserGainCh01 to CfO_UserGainCh04
"Configuration channel 0x / gain" in the AS I/O configuration

These registers are used to configure the gain for the respective channel. The format is a 16.16-bit signed 4-byte value, with the high word the integer part and the low word the decimal places.

Input value = Gain ku * 65536

The value 0x10000 corresponds to a gain of 1.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Gain
	65,535	= 1 (default value)

4.3.17.9.11.2 "CfO_UserOffsetCh" registers

Name:
CfO_UserOffsetCh01 to CfO_UserOffsetCh04
"Configuration channel 0x / offset" in the AS I/O configuration

These registers are used to configure the offset for the respective channel. The format is a 16.16-bit signed 4-byte value, with the high word the integer part and the low word the decimal places.

Input value = Offset du * 65536

The value 0x10000 corresponds to an offset of 1.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Offset (default = 0)

4.3.17.9.12 Input filter

This module is equipped with an individually configurable input filter for each channel. The following filters can be selected:

- 1st-order low pass
- 2nd-order low pass
- 2nd-order IIR

The cutoff frequency can be configured for the 1st-order and 2nd-order low pass filters. The coefficients Alpha0, Alpha1, Alpha2, Beta1 and Beta2 must be configured for the IIR filter.

4.3.17.9.12.1 "CfO_CutOffFrequCh" register

Name:
CfO_CutOffFrequCh01 to CfO_CutOffFrequCh04

These registers are used to configure the limit frequency in hertz for a 1st- or 2nd-order low pass for the corresponding channel.

Data type	Value	Information
UINT	0 to 65535	Limit frequency for 1st- or 2nd-order low pass [Hz] (default = 0)

4.3.17.9.12.2 "CfO_AlphaCh" and "CfO_BetaCh" registers

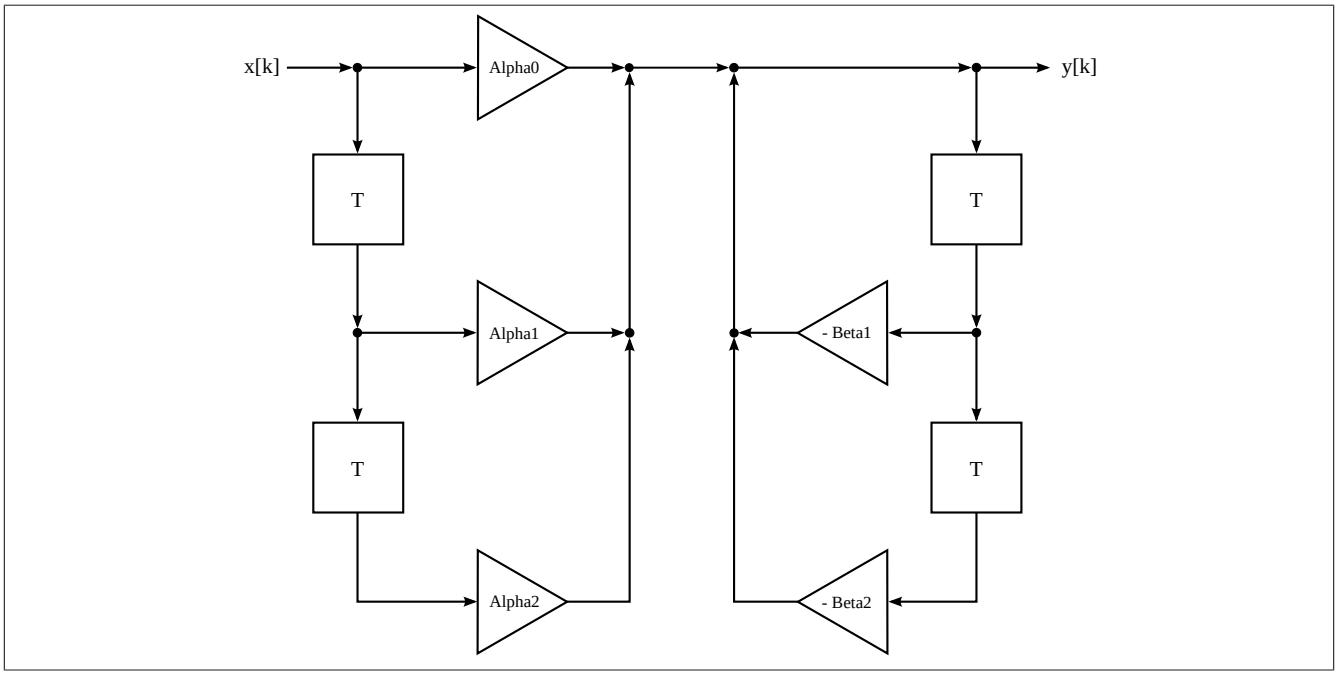
Name:
CfO_Alpha0Ch01 to CfO_Alpha0Ch04
CfO_Alpha1Ch01 to CfO_Alpha1Ch04
CfO_Alpha2Ch01 to CfO_Alpha2Ch04
CfO_Beta1Ch01 to CfO_Beta1Ch04
CfO_Beta1Ch01 to CfO_Beta1Ch04

These registers are used to configure the coefficients for the IIR filter.

Image as a z-transfer function

The 2nd-order z-transfer function is specified in coefficient form (denominator polynomial Beta1, Beta2 and numerator polynomial Alpha0, Alpha1, Alpha2). The transfer method is calculated with the sampling cycle time.

$$S(Z) = \frac{a(Z)}{b(Z)} = \frac{Alpha0 + Alpha1 * Z^{-1} + Alpha2 * Z^{-2}}{1 + Beta1 * Z^{-1} + Beta2 * Z^{-2}}$$



Data type	Value	
DINT	-2,147,483,648 to 2,147,483,647	IIR filter coefficient (default = 0)

4.3.17.9.13 Physical configuration

4.3.17.9.13.1 "CfO_ModeCh" registers

Name:
CfO_ModeCh01 to CfO_ModeCh04

The operating mode for each physical channel can be configured in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Connection configuration **This value must be set the same for each register!**	000	Voltage signal
		111	Current signal
3 - 7	Reserved	0	
8 - 10	Operating mode	000	Channel disabled
		001	No filtering
		010	2nd-order IIR (configurableAlpha and Beta coefficients)
		011	1st-order low pass (configurable limit frequency)
		100	2nd-order low pass (configurable limit frequency)
		101 to 111	Reserved
11 - 15	Reserved	0	

4.3.17.9.14 Logical configuration

4.3.17.9.14.1 Operation in the standard function model

6 logical channels are available on the module. Each channel can be configured with one of the following functions:

- Addition of two channels with scaling
- Integral addition of two channels with scaling
- Multiplication of two channels with scaling
- Integral multiplication of two channels with scaling
- Comparator function of two channels
- Hysteresis comparator of one channel

With logical oversampling, 32-bit data points are available in addition to 16-bit data points due to the possible calculated results. The AS I/O configuration or data point mapping can be opened to select which one to use.

If there is no need to use 32-bit data points, or if this would lead to too large of a limitation in the number of data points, scaling can be used to limit the range to 16 bits.

The buffer depth for the digital comparator is also able to handle 16 results. Since these are Boolean results, these 16 bits are compressed into 2-byte data points and transferred that way.

Addition

This function can be used to determine the sum or difference of two channels. To determine the difference, negative scaling needs to be configured for the channel.

Calculation

Sample line = (Channel 1 * Scaling 1) + (Channel 2 * Scaling 2)

The addition calculation is handled internally as a 32-bit value in 16.16 format; the data from the source channels is evaluated as integers (applied to the high word), with decimal places possible as a result of scaling. When displayed as a logical 32-bit result, these decimal places are visible. When displayed as a 16-bit value, only the integral high word is used.

Example

Channel 1 = 2000
Channel 2 = 1000
Both scalings = 1

Results

3000.x = (2000.x * 1,0) + (1000.x * 1.0)
32-bit representation = 196608000 = 0xBB80000
16-bit representation = 3000 = 0xBB8

Information:

The maximum value channel 1 can take on is 32767; otherwise, an addition overflow occurs. If values greater than 32767 are possible, the value range must be limited with scaling.

Integral of addition

This function can be used in the application to establish the average value of the channels or to calculate the deviation/difference between two channels over n samples. In each cycle, the channels are added together first; then the result is added to the previous value and saved in the current sample line. Depending on the result data type being used (16-bit or 32-bit), eventually the continuous integration will cause the calculation to overflow after n samples. Because the result value is signed, it is important to set the number n of samples small enough so that the integration is less than half of the value range. If this is done, determining the average value can be carried out despite an overflow.

Calculation

Sample line result = Integral ((Channel 1 * Scaling 1) + (Channel 2 * Scaling 2))

The addition calculation is handled internally as a 32-bit value in 16.16 format; the data from the source channels is evaluated as integers (applied to the high word), with decimal places possible as a result of scaling. When displayed as a logical 32-bit result, these decimal places are visible. When displayed as a 16-bit value, only the integral high word is used.

Example

Channel 1 = 2000
Channel 2 = 1000
Both scalings = 1

Results

3000.x = (2000.x * 1,0) + (1000.x * 1.0)
32-bit representation = 196608000 = 0xBB80000
16-bit representation = 3000 = 0xBB8

The average value can now be calculated as follows:

n = Number of samples / sample lines
$Value_x$ = Value from sample line x → Newer value
$Value_x$ = Value from sample line x → Older value, n samples back

Average value = $(Value_x - Value_{(x-n)}) / n$

Information:

The maximum value channel 1 can take on is 32767; otherwise, an addition overflow occurs. If values greater than 32767 are possible, the value range must be limited with scaling.

Multiplication

This function can be used to calculate the current effective power P = U * I.

Calculation

Sample line = Channel 1 * Channel 2 * Scaling

Multiplication is calculated internally as a 32-bit value; the 16-bit data from the source channels is passed to the low word. When displayed as a logical 32-bit value, the entire result is visible (no multiplication overflow possible when scaling ≤1). When displayed as a 16-bit value, only the high word is used. Though there is a loss of precision, the 16-bit values allow more data points to be transferred.

Example

Channel 1 = 2000
Channel 2 = 1000
Scaling = 1

Results

2000000 = (2000 * 1000 * 1.0)
32-bit representation = 2000000 = 0x1E8480
16-bit representation = 30 = 0x1E

Information:

If more precision is needed with the 16-bit value, scaling in steps of 2^n (..., *128, *256, ...) can be employed to shift the bits. Of course, it's important again that the input values of the source channels be limited; otherwise, an overflow will occur in the multiplication operation.

Integral of multiplication

This function can be used in the application to establish the average value of the effective power. In each cycle, the channels are multiplied together first; then the result is added to the previous value and saved in the current sample line. Depending on the result data type being used (16-bit or 32-bit), eventually the continuous integration will cause the calculation to overflow after n samples. Because the result value is signed, it is important to set the number n of samples small enough so that the integration is less than half of the value range. If this is done, determining the average value can be carried out despite an overflow.

Calculation

Sample line = Integral (Channel 1 * Channel 2 * Scaling)

Multiplication is calculated internally as a 32-bit value; the 16-bit data from the source channels is passed to the low word. When displayed as a logical 32-bit value, the entire result is visible (no multiplication overflow possible when scaling ≤1). When displayed as a 16-bit value, only the high word is used. Though there is a loss of precision, the 16-bit values allow more data points to be transferred.

Example

Channel 1 = 2000
Channel 2 = 1000
Scaling = 1

Results

2000000 = (2000 * 1000 * 1.0)
32-bit representation = 2000000 = 0x1E8480
16-bit representation = 30 = 0x1E

The average value can now be calculated as follows:

n = Number of samples / sample lines
$Value_x$ = Value from sample line x → Newer value
$Value_x$ = Value from sample line x → Older value, n samples back

Average value = $(Value_x - Value_{(x-n)}) / n$

Information:

If more precision is needed with the 16-bit value, scaling in steps of 2^n (..., *128, *256, ...) can be employed to shift the bits. Of course, it's important again that the input values of the source channels be limited; otherwise, an overflow will occur in the multiplication operation.

Channel comparator

This function can be used to compare channel values. The following applies:

- Channel 1 > Channel 2 = 1
- Channel 1 < Channel 2 = 0
- Channel 1 = Channel 2 = State before values are the same

Calculation

Sample line (bit) = Comparison (channel value 1 with channel value 2)

Hysteresis comparator

This function can be used to monitor range violations by channels. The following applies:

- Channel > Upper threshold value = 1
- Channel < Lower threshold value = 0
- Channel within threshold = Value before occurrence

Calculation

Sample line (bit) = Comparison (channel value with lower threshold value) and (channel value with upper threshold value))

4.3.17.9.14.2 Operation in the bus controller function model

When used on the bus controller, there are 4 logical functions available for each of the analog input channels in addition to the physical value output. Each channel can be configured with one of the following functions:

- Output of physical values (default setting)
- Addition of two channels with scaling
- Integral addition of two channels with scaling
- Multiplication of two channels with scaling
- Integral multiplication of two channels with scaling
- Comparator function of two channels
- Hysteresis comparator of one channel

In contrast to the standard function model, oversampling and the two digital comparators are not supported. As a result, there is only one newly generated value per channel in each update cycle. Another difference is that there are only 4 logical calculation channels instead of 6.

The logical functions addition, integral of addition, multiplication and integral of multiplication do not differ from the standard function model in their configuration and function when operating on the bus controller.

Physical value display

The physical value display in the bus controller function model is initialized automatically and represents a special form of the logical function "Addition" with defined scaling factors.

Calculation

Result = Channel value
Formula used for addition: Result = (Channel value 1 * 1) + (Channel value 2 * 0)

Information:

In this function model, only the 4 physical input channels are available, and the scaling factors have defined values.

4.3.17.9.14.3 "CfO_LogChMode" register

Name:
CfO_LogCh01Mode to CfO_LogCh06Mode
"Logical configuration channel 0x / Addition" in the AS I/O configuration.
"Logical configuration channel 0x / Integral of addition" in the AS I/O configuration.
"Logical configuration channel 0x / Multiplication" in the AS I/O configuration.
"Logical configuration channel 0x / Integral of multiplication" in the AS I/O configuration.
"Logical configuration channel 0x / Channel comparator" in the AS I/O configuration.
"Logical configuration channel 0x / Hysteresis comparator" in the AS I/O configuration.
"Logical configuration channel 0x / Physical value display" in the AS I/O configuration.

The operating mode for each logical channel can be configured in this register.

The selection of the sources to be used for each logical channel is made using the register 4.3.17.9.14.4 "CfO_LogCh0NSource0x". Any additionally needed function parameters are configured in the 4.3.17.9.14.5 "CfO_LogCh0NFuncPar0x" registers. "N" stands for the logical channel to be used, while "x" stands for either the source or function 0 or 1.

The following links can be made:

- Addition: Result = (Source 0 * Function parameter 0) + (Source 1 * Function parameter 1)
- Integral of addition: Result = Σ(Source 0 * Function parameter 0) + (Source 1 * Function parameter 1)
- Multiplication: Result = Source 0 * Source 1 * Function parameter 0
- Integral of multiplication: Result = Σ(Source 0 * Source 1 * Function parameter 0)
- Channel comparator: Result = Comparison of source 0 with source 1
- Hysteresis comparator: Result = comparison of source 0 with (Lower threshold value = Function parameter 0) and (Upper threshold value = Function parameter 1)
- Physical value display: Result = (Source 0 * 1) + (Source 1 * 0)

Data type	Value	Information
UINT	0	Channel switched off (default)
	256	Addition or physical value display[1)]
	257	Integral of addition
	512	Multiplication
	513	Integral of multiplication
	768	Channel comparator
	1024	Hysteresis comparator

1) Only registers CfO_LogCh01Mode to CfO_LogCh04Mode are used for physical value display.

4.3.17.9.14.4 "CfO_LogChSource" register

Name:
CfO_LogCh01Source00 to CfO_LogCh06Source00
CfO_LogCh01Source01 to CfO_LogCh06Source01

These registers can be used to select the source registers for the operating mode of the logical channel configured in the register 4.3.17.9.14.3 "CfO_LogCh0NMode".
In the name, "Source00" stands for source register 0; "Source01" stands for source register 1.

In "Physical value display" mode, the same channel number is written to both source registers.

Data type	Value	Information
USINT	0	Physical channel 01
	...	...
	3	Physical channel 04
	8	Logical channel 01[1)]
	...	...
	13	Logical channel 06

1) Logical channels cannot be used in the bus controller function model.

4.3.17.9.14.5 "CfO_LogChFuncPar" register

Name:
CfO_LogCh01FuncPar00 to CfO_LogCh06FuncPar00
CfO_LogCh01FuncPar01 to CfO_LogCh06FuncPar01

These registers can be used to configure additional function parameters for the operating mode of the logical channel configured in the register 4.3.17.9.14.3 "CfO_LogCh0NMode".

The effect of the function parameters is different depending on the operating mode.

Operating mode	Parameter 1	Parameter 2
(Integral of) addition	Scaling factor	Scaling factor
(Integral of) multiplication	Scaling factor	-
Channel comparator	-	-
Hysteresis comparator	Upper threshold value	Lower threshold value
Output of physical values	Defined scaling factor = 65,536	Defined scaling factor = 0

The value 0x10000 (65,536) corresponds to a scaling or a threshold value of 1.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Scaling factor or threshold value
	0	Default
	65,536	1

4.3.17.9.15 Error registers

The registers for displaying and acknowledging errors are transferred either cyclically or acyclically depending on the function model.

4.3.17.9.15.1 "CfO_ErrorID1017" register

Name:
CfO_ErrorID1017
Automatic enabling by the AS I/O configuration.

This register can be used to enable standard error messages. The channels' composite errors are derived from the individual extended error status, e.g. overflow/underflow of the input range for the analog value. Oversampling error statuses result from a cycle time violation of the configured sampling cycle time.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Composite errors on channel 01	0	Error generation disabled
		1	Error generation enabled
...		...	
3	Composite errors on channel 04	0	Error generation disabled
		1	Error generation enabled
4	Physical sample error status	0	Error generation disabled
		1	Error generation enabled
5	Logical sample error status	0	Error generation disabled
		1	Error generation enabled
6 - 7	Reserved	0	

4.3.17.9.15.2 "CfO_ErrorID0x0x" register

Name:
CfO_ErrorID0007 (for channels 1 and 2)
CfO_ErrorID080F (for channels 3 and 4)
Automatic enabling in the AS I/O configuration by selecting "Extended error status information" and channel activation.

These registers can be used to enable extended error messages for analog channels 1 and 2 as well as channels 3 and 4. Meaning of individual bits:

- **Range exceeded violation (pos.):** The analog input signal is outside of the specified working range.
- **Filter error:** The configured filter theorem cannot be calculated (parameter error).
- **Underflow:** The input signal is less than the lower limit value.
- **Overflow:** The input signal is greater than the upper limit value.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1 or 3: Range exceeded violation (pos.)	0	Error generation disabled
		1	Range exceeded violation (pos.) enabled
1	Channel 1 or 3: Filter error	0	Error generation disabled
		1	Filter error enabled
2	Channel 1 or 3: Underflow	0	Error generation disabled
		1	Underflow enabled
3	Channel 1 or 3: Overrun	0	Error generation disabled
		1	Overflow enabled
4	Channel 2 or 4: Range exceeded violation (pos.)	0	Error generation disabled
		1	Range exceeded violation (pos.) enabled
5	Channel 2 or 4: Filter error	0	Error generation disabled
		1	Filter error enabled
6	Channel 2 or 4: Underflow	0	Error generation disabled
		1	Underflow enabled
7	Channel 2 or 4: Overrun	0	Error generation disabled
		1	Overflow enabled

4.3.17.9.15.3 "StandardErrors" registers

Name:
Channel01Error to Channel04Error
PhysicalError
LogicalError

Composite errors are mapped to this register.

All configured functions of the physical and logical oversampling must be able to be carried out in the configured sampling cycle time; otherwise, these error messages occur. Settings for processing priority and the prescaler can be used to additionally adjust the system for logical oversampling.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01Error	0	No error
		1	Composite errors on channel 1
...		...	
3	Channel04Error	0	No error
		1	Composite errors on channel 4
4	PhysicalError	0	No error
		1	Physical sample error status, sampling cycle time too short
5	LogicalError	0	No error
		1	Logical sample error status, sampling cycle time too short or prescaler configured too low

4.3.17.9.15.4 "AcknowledgeStandardErrors" registers

Name:
AckChannel01Error to AckChannel04Error
AckPhysicalError
AckLogicalError

Error messages from the 4.3.17.9.15.3 "StandardErrors" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	AckChannel01Error	0	No change
		1	Acknowledge error
...		...	
3	AckChannel04Error	0	No change
		1	Acknowledge error
4	AckPhysicalError	0	No change
		1	Acknowledge error
5	AckLogicalError	0	No change
		1	Acknowledge error

4.3.17.9.15.5 "ExtendedChannelErrorMessages" registers

Name:
Channel01OutOfRange to Channel04OutOfRange
Channel01FilterError to Channel04FilterError
Channel01Underflow to Channel04Underflow
Channel01Overflow to Channel04Overflow

The error states of the input channels are represented in these registers. Input channels 1 and 2 as well as 3 and 4 are each grouped together in one register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutOfRange or Channel03OutOfRange	0	No error
		1	Range exceeded violation (pos.) occurred
1	Channel01FilterError or Channel03FilterError	0	No error
		1	Filter error occurred
2	Channel01Underflow or Channel03underflow	0	No error
		1	Underflow occurred
3	Channel01Overflow or Channel03Overflow	0	No error
		1	Overflow occurred
4	Channel02OutOfRange or Channel04OutOfRange	0	No error
		1	Range exceeded violation (pos.) occurred
5	Channel02FilterError or Channel04FilterError	0	No error
		1	Filter error occurred
6	Channel02Underflow or Channel04Underflow	0	No error
		1	Underflow occurred
7	Channel02Overflow or Channel04Overflow	0	No error
		1	Overflow occurred

4.3.17.9.15.6 "AcknowledgeExtendedChannelErrorMessages" registers

Name:
AckChannel01OutOfRange to AckChannel04OutOfRange
AckChannel01FilterError to AckChannel04FilterError
AckChannel01Underflow to AckChannel04Underflow
AckChannel01Overflow to AckChannel04Overflow

These registers can be used to acknowledge the error messages from the 4.3.17.9.15.5 "ExtendedChannelErrorMessages" registers by setting the corresponding bit. The acknowledgment of input channels 1 and 2 as well as 3 and 4 are each grouped together in one register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	AckChannel01OutOfRange or AckChannel03OutOfRange	0	No change
		1	Acknowledge error
1	AckChannel01FilterError or AckChannel03FilterError	0	No change
		1	Acknowledge error
2	AckChannel01Underflow or AckChannel03Underflow	0	No change
		1	Acknowledge error
3	AckChannel01Overflow or AckChannel03Overflow	0	No change
		1	Acknowledge error
4	AckChannel02OutOfRange or AckChannel04OutOfRange	0	No change
		1	Acknowledge error
5	AckChannel02FilterError or AckChannel04FilterError	0	No change
		1	Acknowledge error
6	AckChannel02Underflow or AckChannel04Underflow	0	No change
		1	Acknowledge error
7	AckChannel02Overflow or AckChannel04Overflow	0	No change
		1	Acknowledge error

4.3.17.9.16 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.3.17.9.17 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

4.3.18 X20AI8221

4.3.18.1 General information

The module is equipped with 8 inputs with 13-bit (including sign) digital converter resolution. It can be used to capture voltage signals in the range from ±10 V.

- 8 analog inputs ±10 V
- 13-bit digital converter resolution

4.3.18.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI8221	X20 analog input module, 8 inputs, ±10 V, 13-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 62: X20AI8221 - Order data

4.3.18.3 Technical data

Product ID	X20AI8221
Short description	
I/O module	8 analog inputs ±10 V
General information	
B&R ID code	0xD82F
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.04 W [1]
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	±10 V
Input type	Differential input
Digital converter resolution	±12-bit
Conversion time	1 ms for all inputs
Output format	
Data type	INT
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Input impedance in signal range	20 MΩ
Input protection	Protection against wiring with supply voltage
Open line detection	Yes, using software
Reverse polarity protection	Yes
Permitted input signal	Max. ±30 V
Output of the digital value during overload	Configurable

Table 63: X20AI8221 - Technical data

Product ID	X20AI8221
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Gain	0.08% 3)
Offset	0.015% 4)
Max. gain drift	0.006 %/°C 3)
Max. offset drift	0.002 %/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.025% 4)
Isolation voltage between channel and bus	500 VDC, 1 min
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 63: X20AI8221 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current measured value.
4) Based on the 20 V measurement range.

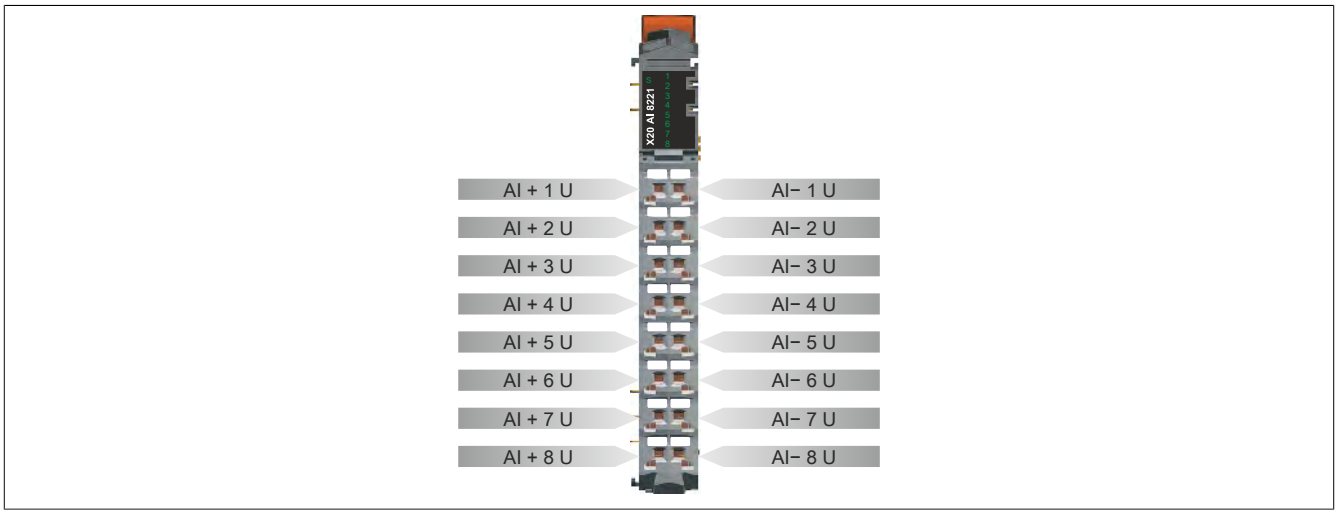
4.3.18.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

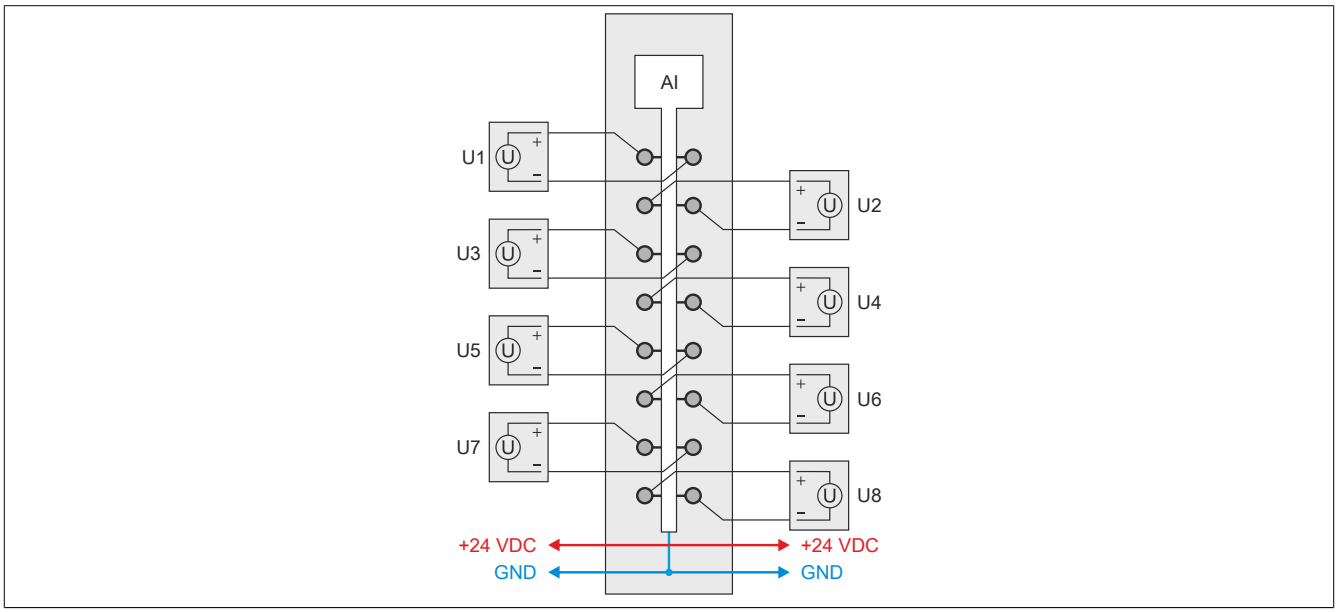
Figure	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 8	Green	Off	Indicates one of the following cases: • No power to module • Open line
			Single flash	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

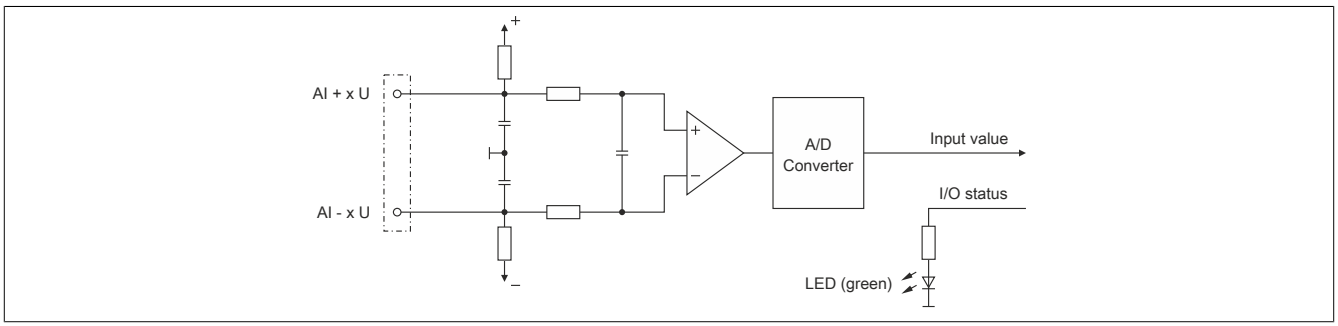
4.3.18.5 Pinout



4.3.18.6 Connection example



4.3.18.7 Input circuit diagram



4.3.18.8 Register description

4.3.18.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.18.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	Configuring the input filter	USINT				●
20	Lower limit value	INT				●
22	Upper limit value	INT				●
Analog signal - Communication						
Index * 2 - 2	AnalogInput0N (Index N = 1 to 8)	INT	●			
30	StatusInput01	USINT	●			
31	StatusInput02	USINT	●			

4.3.18.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	Configuring the input filter	USINT				●
20	-	Lower limit value	INT				●
22	-	Upper limit value	INT				●
Analog signal - Communication							
Index * 2 - 2	Index * 2 - 2	AnalogInput0N (Index N = 1 to 8)	INT	●			
30	-	StatusInput01	USINT		●		
31	-	StatusInput02	USINT		●		

1) The offset specifies the position of the register within the CAN object.

4.3.18.8.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.3.18.8.4 Analog inputs

Input signals are converted asynchronously in a 1 ms interval.

4.3.18.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput08

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC

4.3.18.8.6 Input filter

This module is equipped with a configurable input filter.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

4.3.18.8.6.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

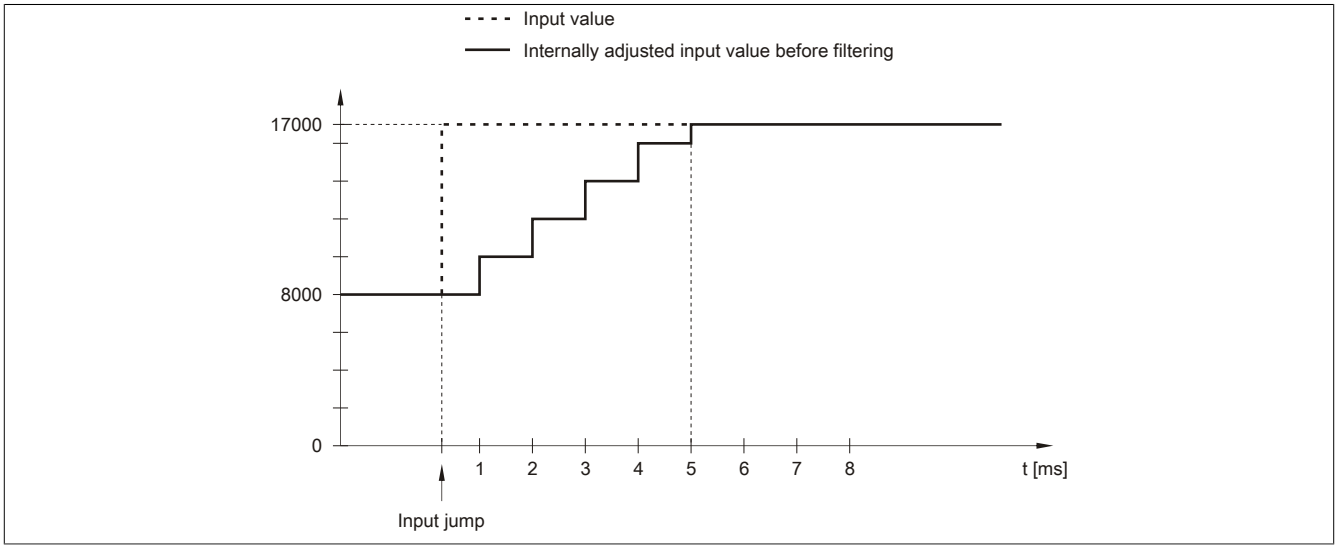


Figure 96: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

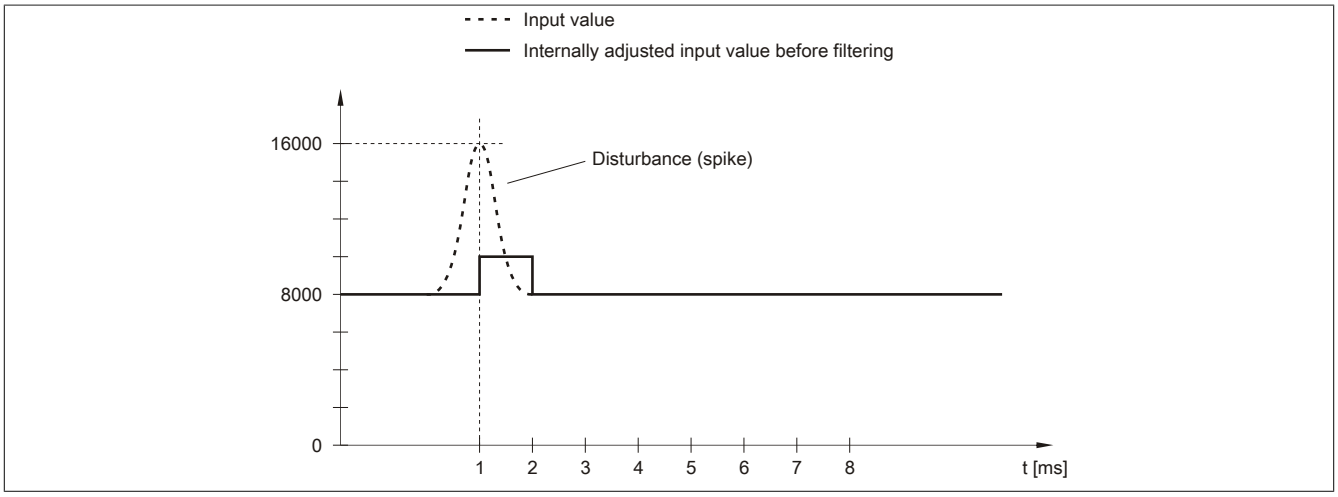


Figure 97: Adjusted input value for disturbance

4.3.18.8.6.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

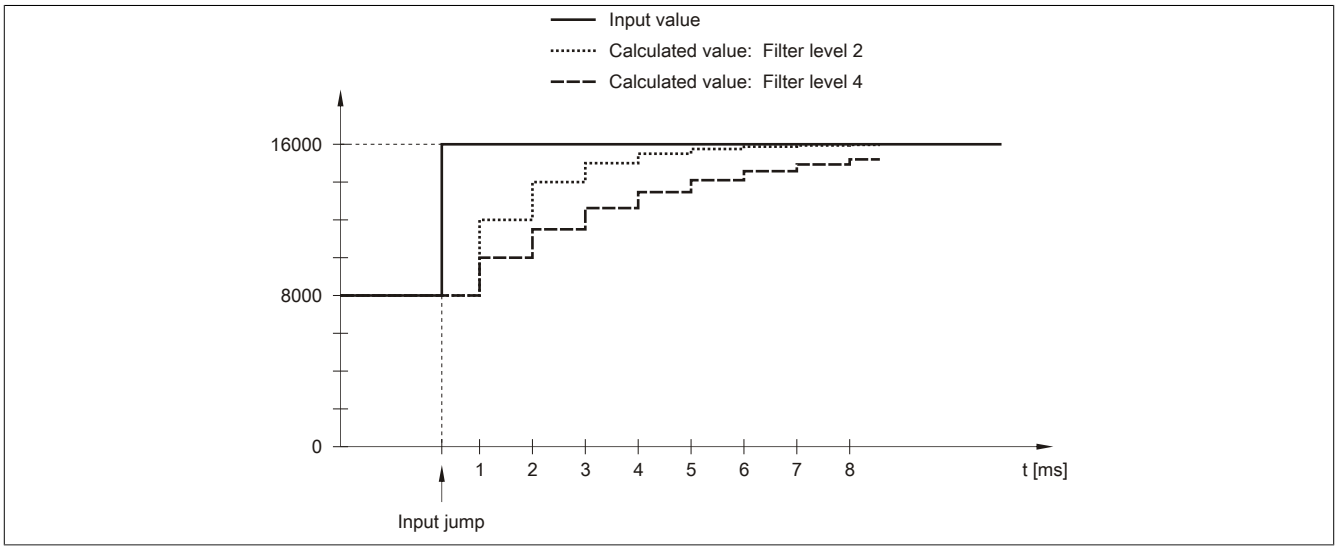


Figure 98: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

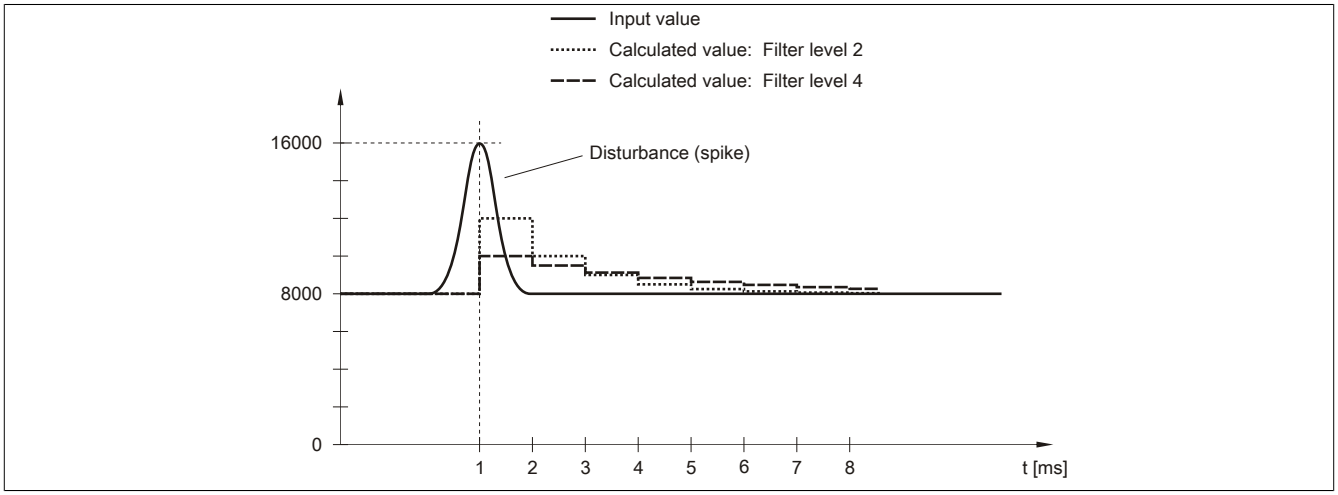


Figure 99: Calculated value during disturbance

4.3.18.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7 - 15	Reserved	0	

4.3.18.8.8 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of -32768 corresponds to the minimum default value of -10 VDC.

Keep in mind that this setting applies to all channels!

4.3.18.8.9 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of 32767 corresponds to the maximum default value at +10 VDC.

Keep in mind that this setting applies to all channels!

4.3.18.8.10 Input status

Name:
StatusInput01 to StatusInput02

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

StatusInput01 monitors Channels 1 to 4
StatusInput02 monitors Channels 5 to 8

Bit	Description	Value	Information
0 - 1	Channel 1 or 5	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4 or 8	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

4.3.18.8.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.3.18.8.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 ms

4.3.19 X20AI8321

4.3.19.1 General information

The module is equipped with 8 inputs with 12-bit digital converter resolution. It is possible to select between the two current ranges 0 to 20 mA and 4 to 20 mA.

- 8 analog inputs, 0 to 20 mA or 4 to 20 mA
- 12-bit digital converter resolution

4.3.19.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI8321	X20 analog input module, 8 inputs, 0 to 20 mA, 12-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 64: X20AI8321 - Order data

4.3.19.3 Technical data

Product ID	X20AI8321
Short description	
I/O module	8 analog inputs 0 to 20 mA / 4 to 20 mA
General information	
B&R ID code	0xD831
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.37 W (Rev. ≥ D0), 1.24 W (Rev. < D0)
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog inputs	
Input	0 to 20 mA/4 to 20 mA
Input type	Differential input
Digital converter resolution	12-bit
Conversion time	1 ms for all inputs
Output format	
Data type	INT
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Load	<300 Ω
Input protection	Protection against wiring with supply voltage
Reverse polarity protection	Yes
Permitted input signal	Max. ±50 mA
Output of the digital value during overload	Configurable
Conversion procedure	SAR

Table 65: X20AI8321 - Technical data

Product ID	X20AI8321
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Gain	
0 to 20 mA	0.08% 2)
4 to 20 mA	0.1% 2)
Offset	
0 to 20 mA	0.03% 3)
4 to 20 mA	0.16% 3)
Max. gain drift	
0 to 20 mA	0.009 %/°C 2)
4 to 20 mA	0.0113 %/°C 2)
Max. offset drift	
0 to 20 mA	0.005 %/°C 3)
4 to 20 mA	0.006 %/°C 3)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.05% 3)
Isolation voltage between channel and bus	500 VDC, 1 min
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 65: X20AI8321 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Based on the current measured value.
3) Based on the 20 mA measurement range.

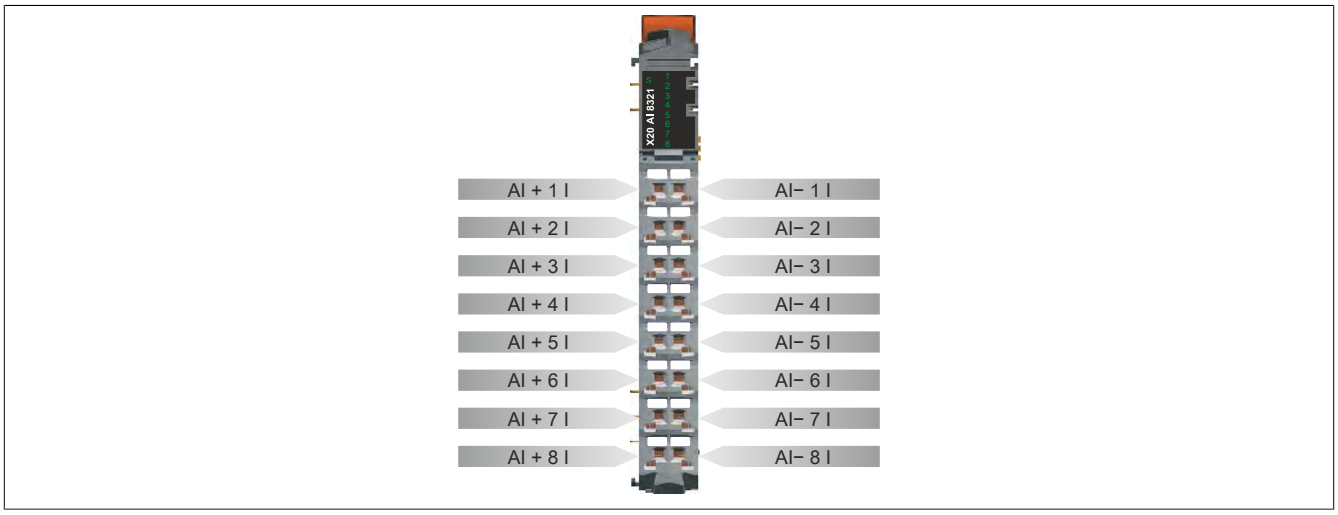
4.3.19.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

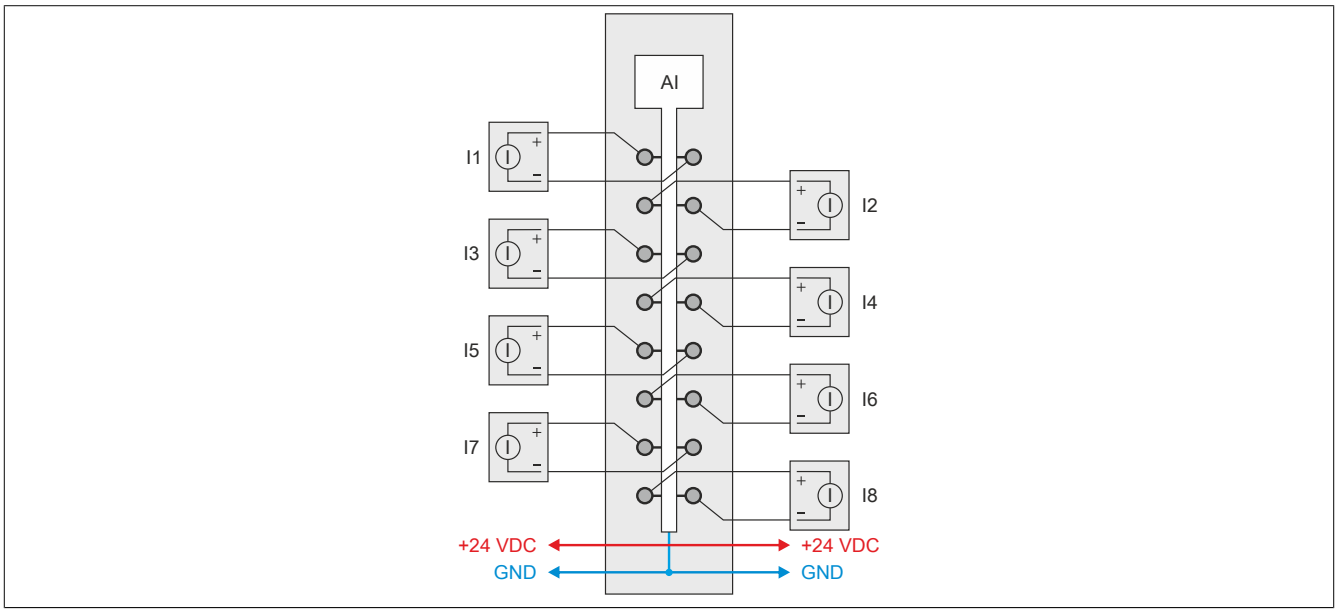
Figure	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 8	Green	Off	No power to module
			Single flash	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

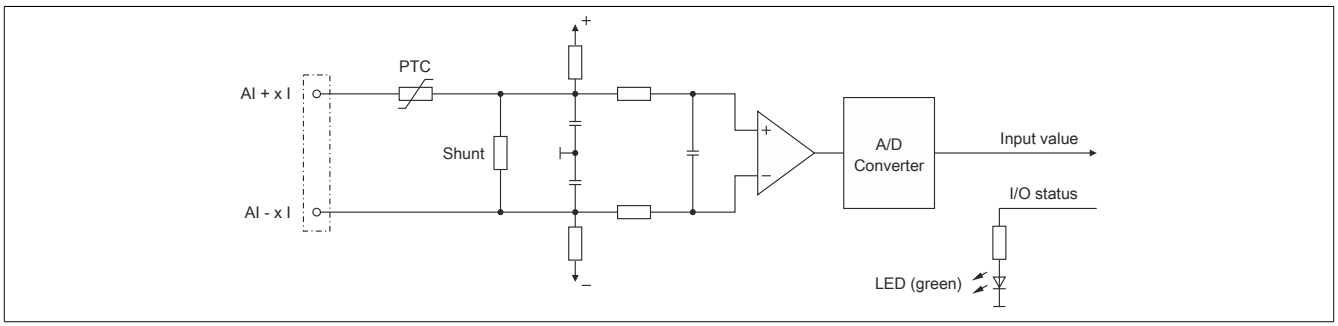
4.3.19.5 Pinout



4.3.19.6 Connection example



4.3.19.7 Input circuit diagram



4.3.19.8 Register description

4.3.19.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.19.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	Configuring the input filter	USINT				●
18	Channel type	UINT				●
20	Lower limit value	INT				●
22	Upper limit value	INT				●
Analog signal - Communication						
Index * 2 - 2	AnalogInput0N (Index N = 1 to 8)	INT	●			
30	StatusInput01	USINT	●			
31	StatusInput02	USINT	●			

4.3.19.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	Configuring the input filter	USINT				●
18	-	Channel type	UINT				●
20	-	Lower limit value	INT				●
22	-	Upper limit value	INT				●
Analog signal - Communication							
Index * 2 - 2	Index * 2 - 2	AnalogInput0N (Index N = 1 to 8)	INT	●			
30	-	StatusInput01	USINT		●		
31	-	StatusInput02	USINT		●		

1) The offset specifies the position of the register within the CAN object.

4.3.19.8.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.3.19.8.4 Analog inputs

Input signals are converted asynchronously in a 1 ms interval.

4.3.19.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput08

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	0 to 32767	Current signal 0 to 20 mA or 4 to 20 mA

4.3.19.8.6 Input filter

This module is equipped with a configurable input filter.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

4.3.19.8.6.1 Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

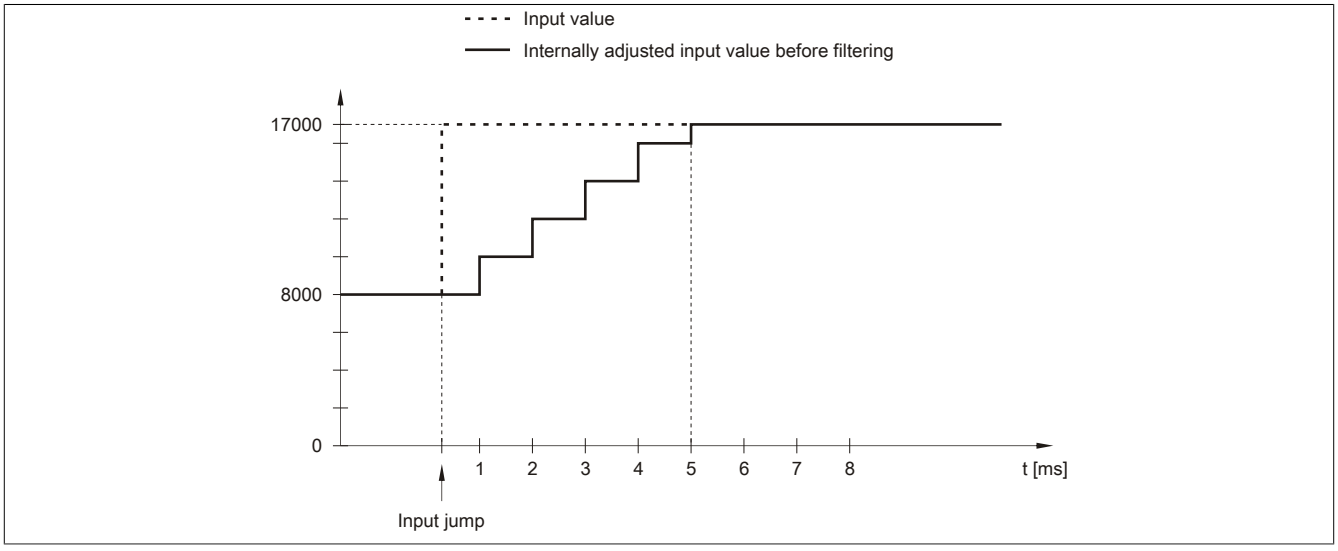


Figure 100: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

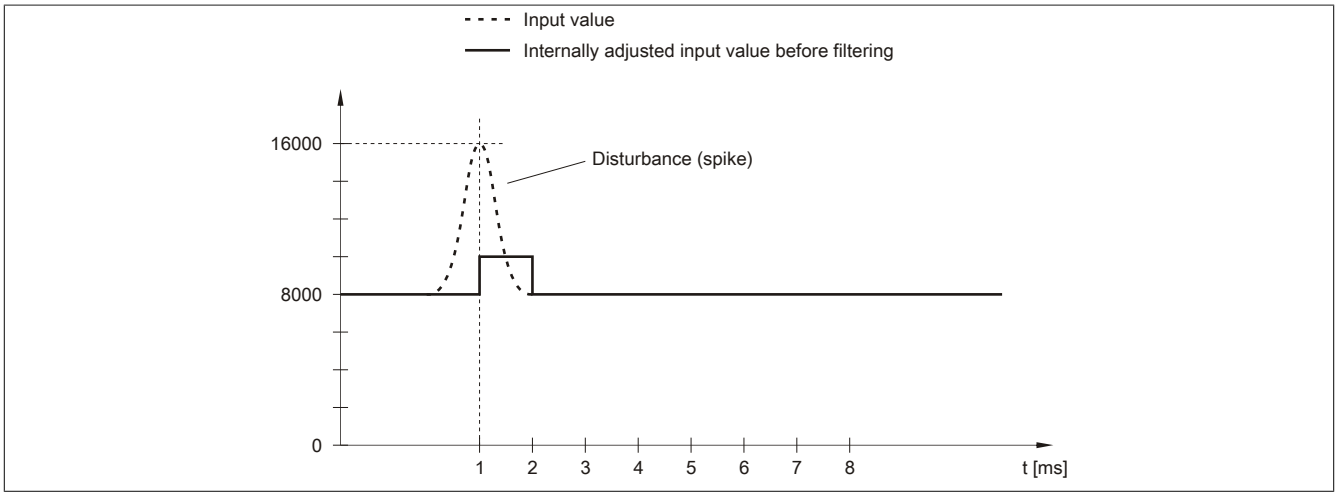


Figure 101: Adjusted input value for disturbance

4.3.19.8.6.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

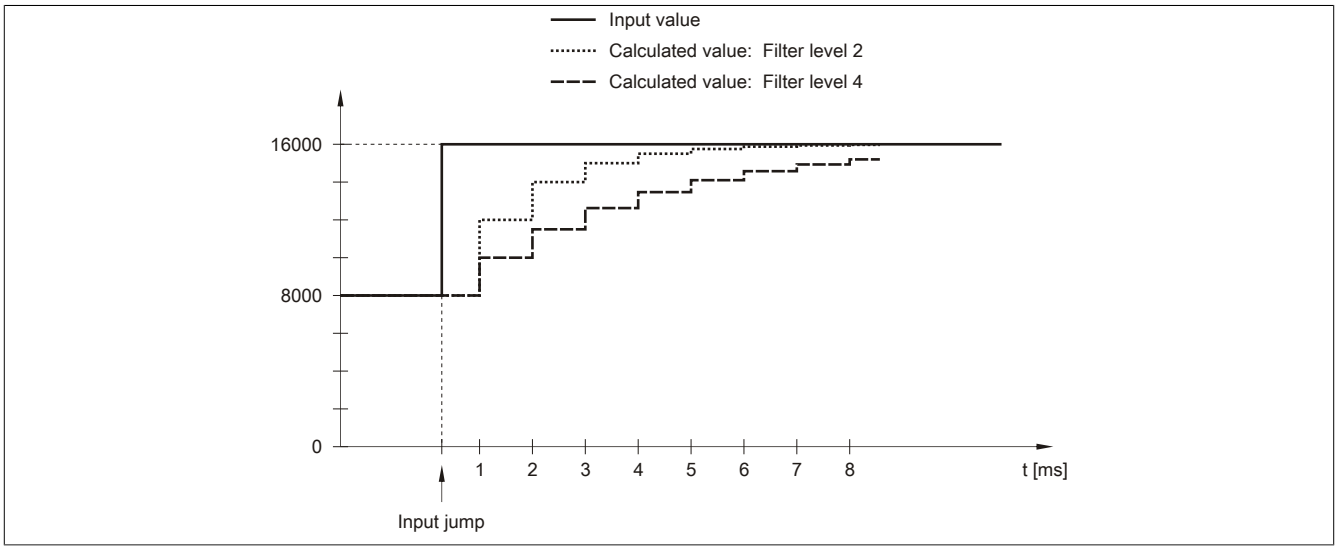


Figure 102: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

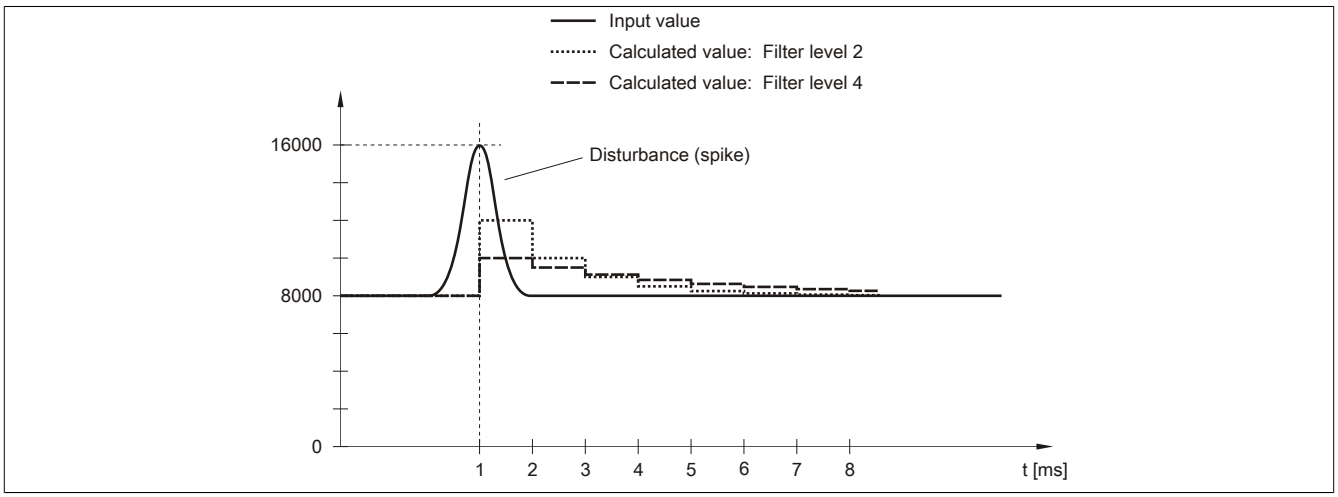


Figure 103: Calculated value during disturbance

4.3.19.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7 - 15	Reserved	0	

4.3.19.8.8 Channel type

Name:
ConfigOutput02

This register can be used to set the range of the current signal. This is determined by how they are configured. The following input signals can be set:

- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
...		...	
7	Channel 8: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal

4.3.19.8.9 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Keep in mind that this setting applies to all channels!

4.3.19.8.10 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Value
INT	-32768 to 32767

Information:

The default value of 32767 corresponds to the maximum default value at 20 mA.

Keep in mind that this setting applies to all channels!

4.3.19.8.11 Input status

Name:
StatusInput01 to StatusInput02

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

StatusInput01 monitors Channels 1 to 4
StatusInput02 monitors Channels 5 to 8

Bit	Description	Value	Information
0 - 1	Channel 1 or 5	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
...		...	
6 - 7	Channel 4 or 8	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	0 to 20 mA	4 to 20 mA
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	0	-8191 (0xE001)

4.3.19.8.12 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.3.19.8.13 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 ms

4.3.20 X20AIA744

4.3.20.1 General information

This module works with 4-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage or zero offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 2 full-bridge strain gauge inputs
- 5 kHz data output rate for both channels
- Independently configurable strain gauge factor and filter level for each of the 2 channels

4.3.20.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AIA744	X20 analog input module, 2 full-bridge strain gauge inputs, 24-bit converter resolution, 2.5 kHz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 66: X20AIA744 - Order data

4.3.20.3 Technical data

Product ID	X20AIA744
Short description	
I/O module	2 full-bridge strain gauge inputs
General information	
B&R ID code	0xE50C
Status indicators	Channel status, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Open line	Yes, using status LED and software
Input	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.7 W
Additional power dissipation caused by the actuators (resistive) [W]	+0.72 [1)]
Electrical isolation	
Bus - Analog input	Yes
Bus - Bridge supply voltage	Yes
Channel - Channel	No
Channel - I/O supply	No
Certification	
CE	Yes
ATEX Zone 2 [2)]	Yes
GOST-R	Yes
Full-bridge strain gauge	
Strain gauge factor	2 to 256 mV/V, configurable using software
Connection	4-wire connections
Input type	Differential, used to evaluate a full-bridge strain gauge
Digital converter resolution	24-bit
Conversion time	200 µs
Data output rate	5000 samples per second and per channel (f_{DATA})
Input filter	
Cutoff frequency	2.5 kHz
Orderliness	3
Slope	60 dB

Table 67: X20AIA744 - Technical data

Product ID	X20AIA744
ADC filter characteristics	Sigma-delta, see section "Filter"
Operating range / Measurement sensor	85 to 5000 Ω
Influence of cable length	The shielded twisted pair cable should be as short as possible and run separately to the sensor (isolated from load circuit) without intermediate terminals
Input protection	RC protection
Common-mode range	0.6 to 3.8 VDC Permissible input voltage range (with regard to the potential strain gauge GND) on the inputs "Input +" and "Input -"
Isolation voltage between input and bus	500 V_{eff}
Conversion procedure	Sigma-delta
Output of the digital value	
Broken bridge supply line	Value approaches 0
Broken sensor line	Value approaches ±end value ("open circuit" status bit is set in the *Module status* register)
Valid value range	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)
Strain gauge supply	
Voltage	5.5 VDC / max. 65 mA per channel
Short circuit protection, overload protection	Yes
Quantization [3]	
LSB value	
2 mV/V	1.31 nV
4 mV/V	2.62 nV
8 mV/V	5.25 nV
16 mV/V	10.49 nV
32 mV/V	20.98 nV
64 mV/V	41.96 nV
128 mV/V	83.92 nV
256 mV/V	167.85 nV
Max. gain drift	35 ppm/°C [4]
Max. offset drift	15 ppm/°C [5]
Nonlinearity	<10 ppm [5]
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 67: X20AIA744 - Technical data

1) Depends on the full-bridge strain gauge used
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Quantization depends on the strain gauge factor.
4) Based on the current measured value.
5) Based on the entire measurement range.

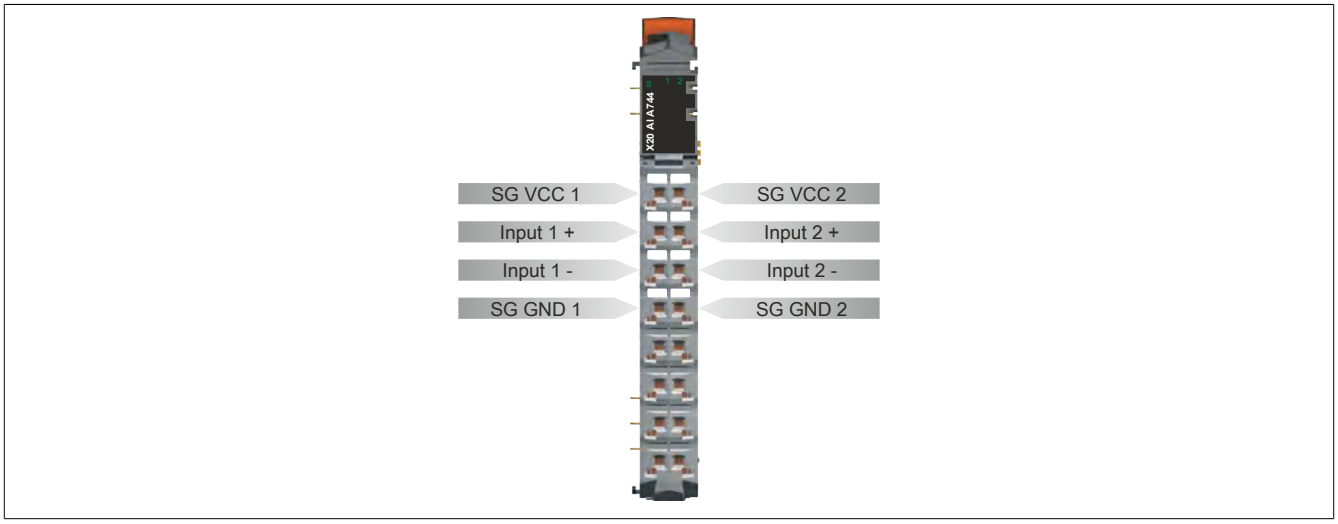
4.3.20.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

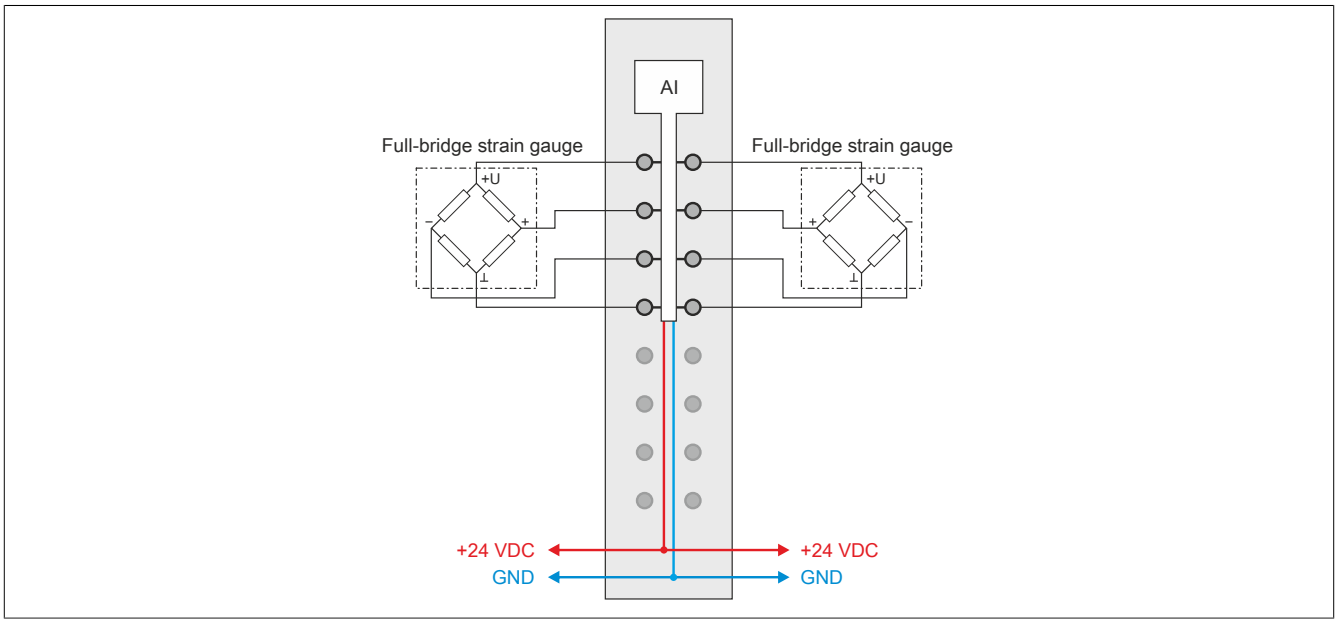
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	I/O supply outside limits
			On	Error or reset status
	1 - 2	Green	Off	Possible causes: • Supply error • Channel not yet configured
			Blinking	Possible causes: • Open line • Overvoltage • Undervoltage
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

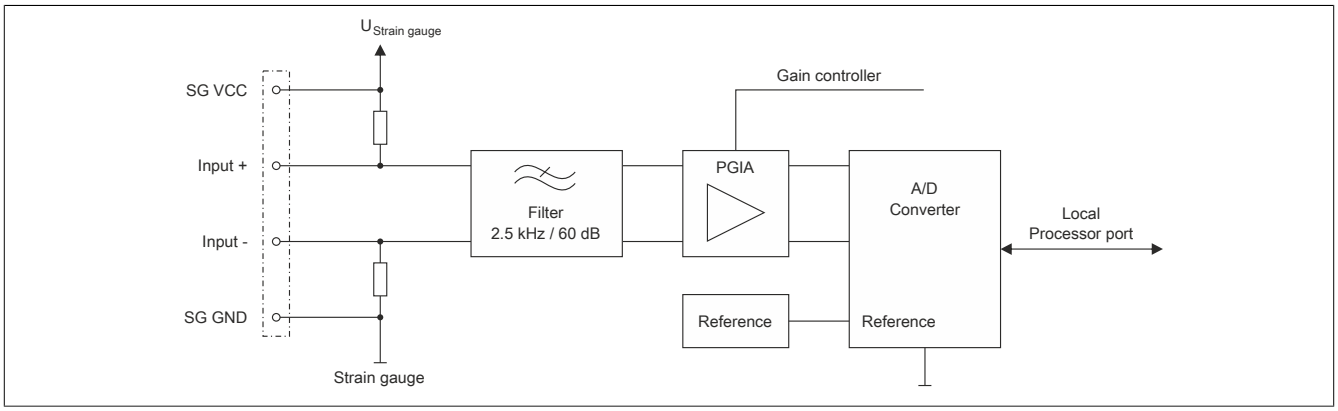
4.3.20.5 Pinout



4.3.20.6 Connection example



4.3.20.7 Input circuit diagram

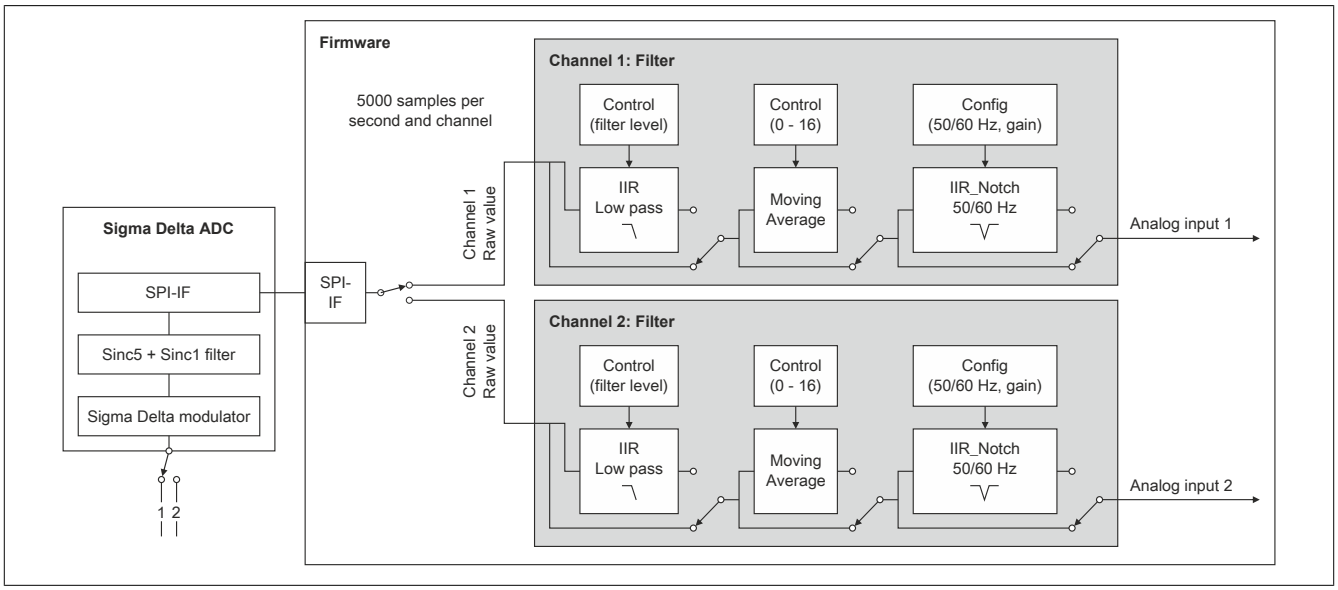


4.3.20.8 Filter

An independent cascade of filters is available for each channel. They can be individually enabled and configured at runtime. By default, all filters are disabled when the device is switched on. Filters are controlled and configured using the "ControlPacked0N" and "ConfigChannel0N" (N = 1 to 2) registers.

In order to allow the filter behavior to be adapted to the measuring situation or machine cycle (high dynamics and low precision or low dynamics and high precision), the filter characteristics of both the IIR low-pass filter as well as the moving average filter can be changed synchronously at any time.

Filter diagram



4.3.20.8.1 IIR low-pass filter

4.3.20.8.1.1 General information

The IIR low-pass filter is used to generally smooth and increase the resolution of the analog value. The filter works according to the following formula:

$$y = y_{Old} + \frac{x - y_{Old}}{2^{Filter\ level}}$$

x ... current filter input value
y_{Old} ... Old filter output value
y ... new filter output value

The "Filter level" parameter in the formula above is configured with the help of the "ControlPacked0N" register. "Filter level" = 0 if the IIR low-pass filter is disabled.

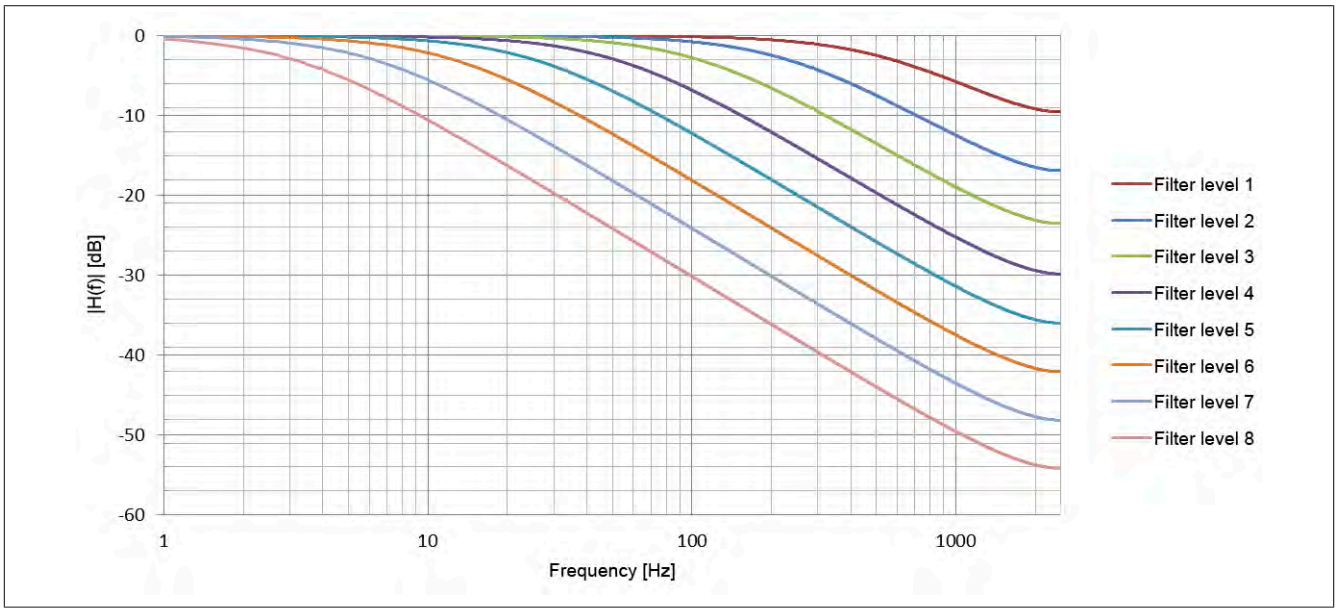
4.3.20.8.1.2 Filter characteristics of the 1st-order IIR low-pass filter

Limit frequency f_c

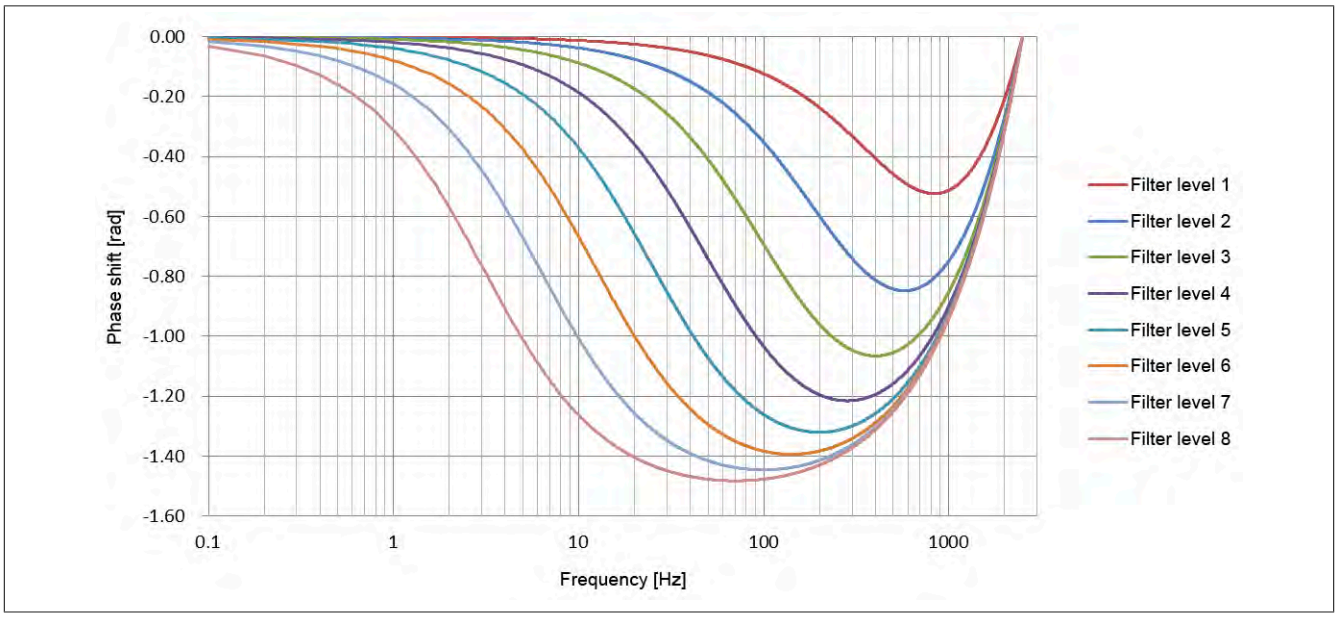
The following table provides an overview of the -3 dB limit frequency f_c depending on the configured filter level.

IIR low-pass filter level	f_c [Hz]
1	575
2	230
3	106
4	51
5	25
6	12.5
7	6.2
8	3.1

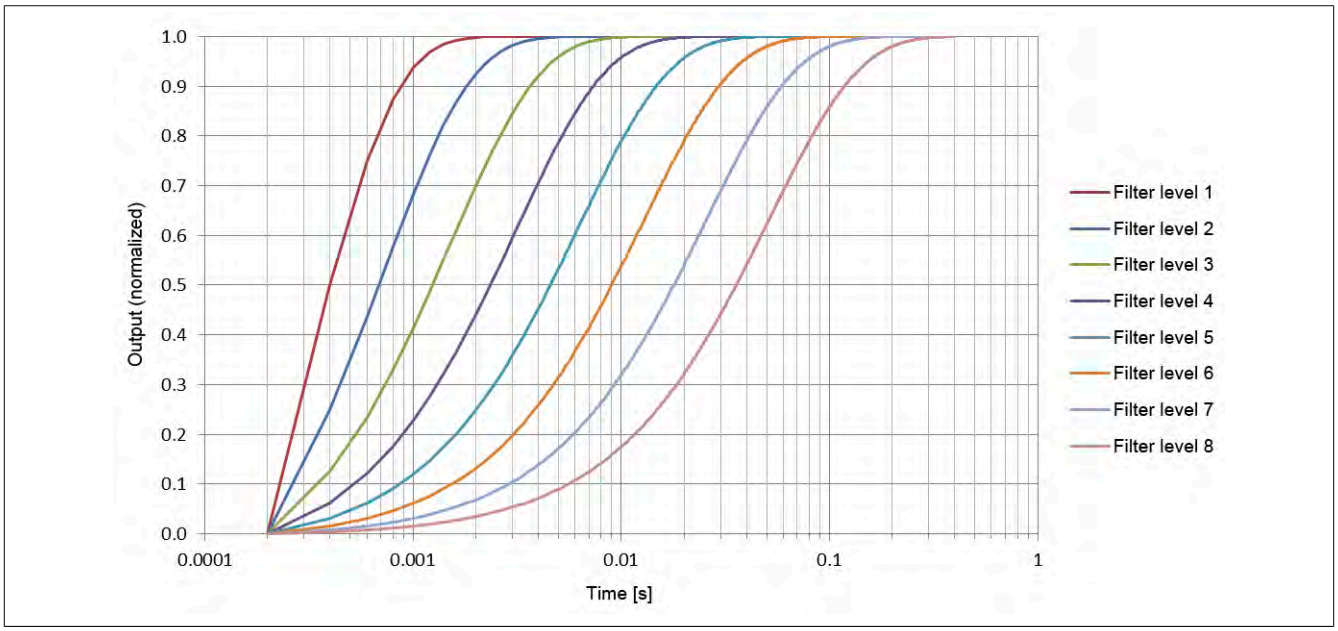
Gain of the IIR low-pass filter



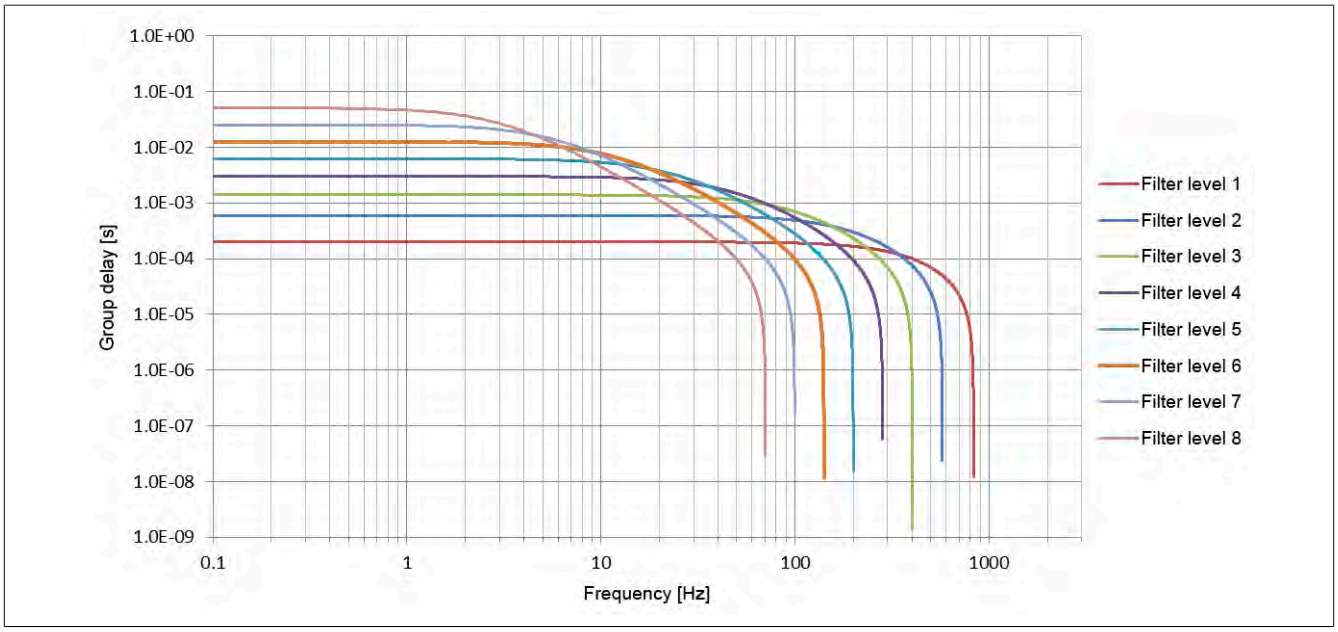
Phase shift of the IIR low-pass filter



Step response of the IIR low-pass filter



Group delay of the IIR low-pass filter



4.3.20.8.2 Sinc1 / Moving average filter

Like the low-pass filter, the moving average filter can also be used to smooth out the signal and increase its resolution. In addition, configuring the filter length accordingly makes it possible to target and efficiently filter out individual interference frequencies. The source of these interference frequencies may be mechanical or electromagnetic. Multiples of these are also filtered out (as long as they are a whole-number factor of the data output rate of 5000 samples per second and channel).

Example:
Data output rate = 5000 samples/s/channel, averaging over 4 values -> "Notch" at 1.25 kHz (and 2.5 kHz)

When reconfiguring the filter length from "n" to "m", it takes |m-n| * 200 µs until the desired filter length setpoint is reached again. As long as the filter length setpoint is not reached, this situation will be indicated by the bit 7 status bit in the "StatusPacked0N" register.

4.3.20.8.2.1 Filter characteristics of the moving average filter

Filter configuration	Filter length	f_{Notch} [Hz] 1)	f_c [Hz] 2)
0	1		
1	2	2500	1244
2	4	1250	568
3	5	1000	450
4	10	500	222
5	20	250	111
6	25	200	88.4
7	50	100	44.0
8	83	60.24	26.5
9	100	50	21.9
10	125	40	17.5
11	167	29.94	13.0
12	200	25	10.9
13	250	20	8.6
14	300	16.67	7.1
15	500	10	4.3
16	1000	5	2.0

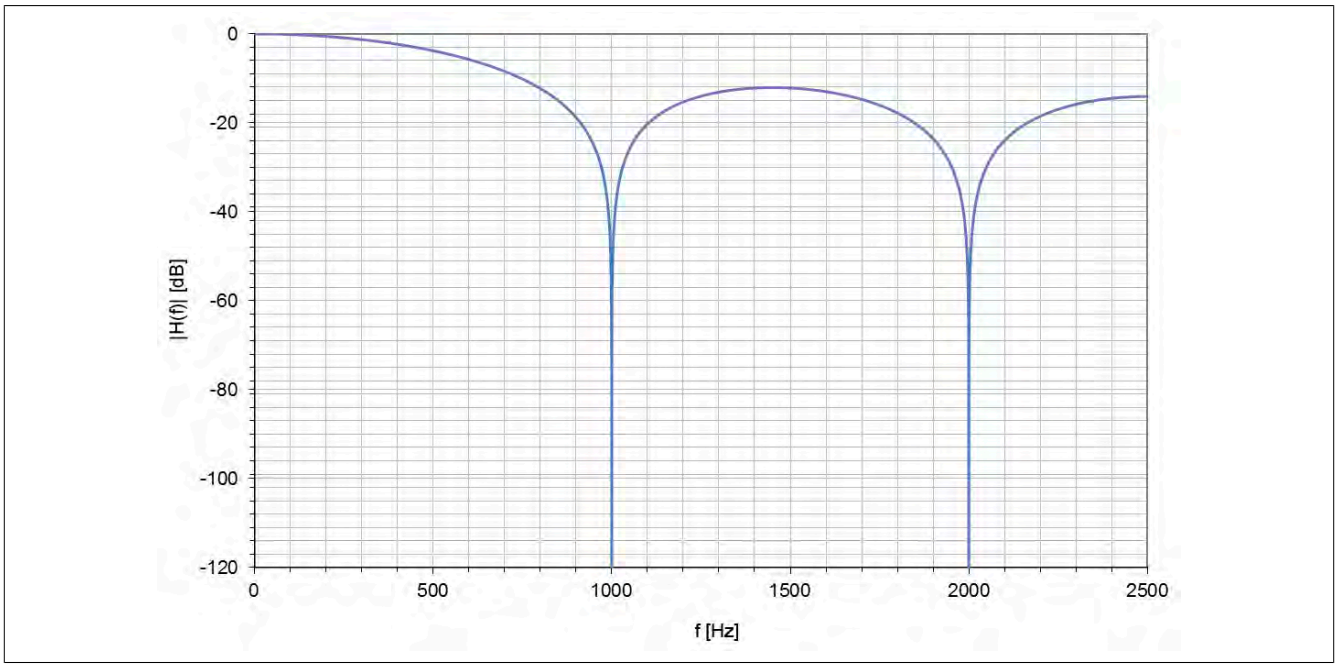
1) Mid-band frequency of the first attenuation maximum.
2) -3 dB limit frequency.

4.3.20.8.2.2 Examples for the gain of the moving average filter

Example 1

Filter setting = 3:

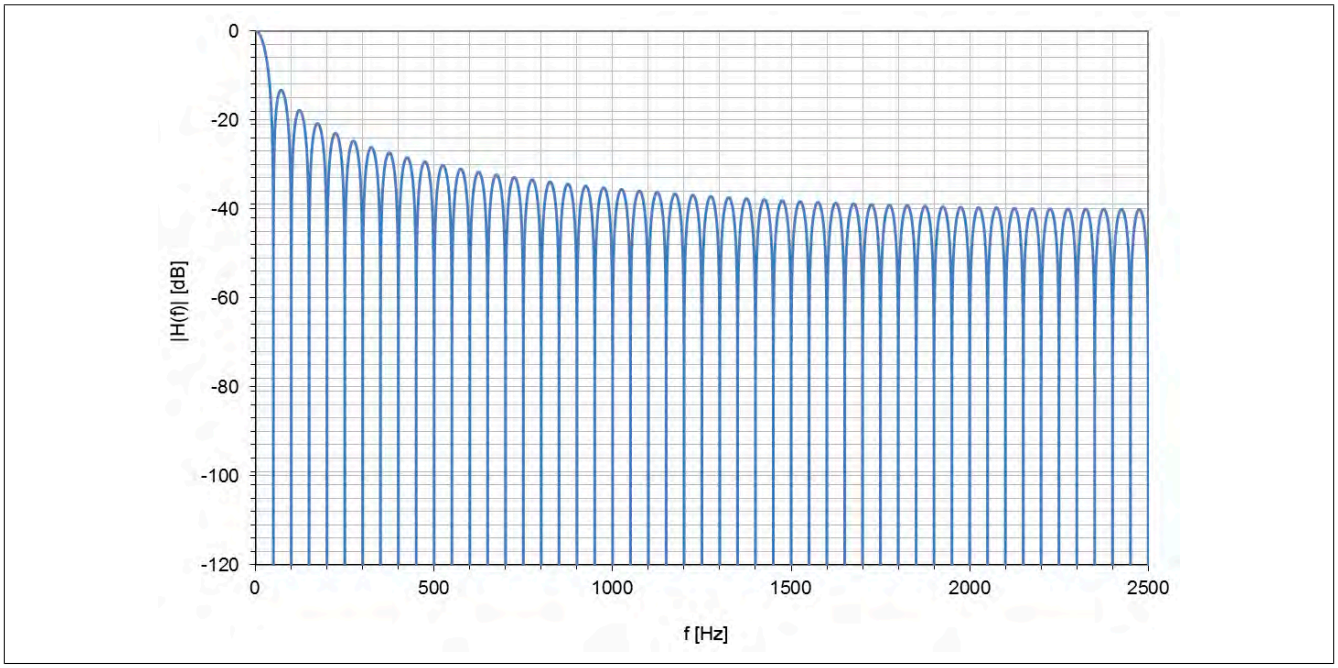
- f_{Notch} = 1000 Hz
- f_c = 449.6 Hz



Example 2

Filter setting = 9:

- f_{Notch} = 50 Hz
- f_c = 21.9 Hz



4.3.20.8.3 50/60 Hz IIR notch filter

The IIR notch filter is used for narrow-band suppression of interference caused by the mains frequency.

This is an 8th-order IIR notch filter implemented in the form of a cascade of 4 2nd-order IIR notch filters.

Information:

The IIR notch filter should only be enabled if there is actually interference being caused by the mains frequency. You should always check whether sufficiently low and sufficiently narrow band filtering at 50 Hz / 60 Hz can be implemented using a moving average filter (see section 4.3.20.8.2.1 "Filter characteristics of the moving average filter").

This is because, like every higher-order IIR notch filter, this filter also has a tendency to respond to an input step with an attenuating vibration. The higher the dynamics of the expected measurement signal, the greater the potential interfering effect of this vibration tendency. In extreme cases, the vibration can temporarily be greater than the mains interference that is supposed to be filtered out.

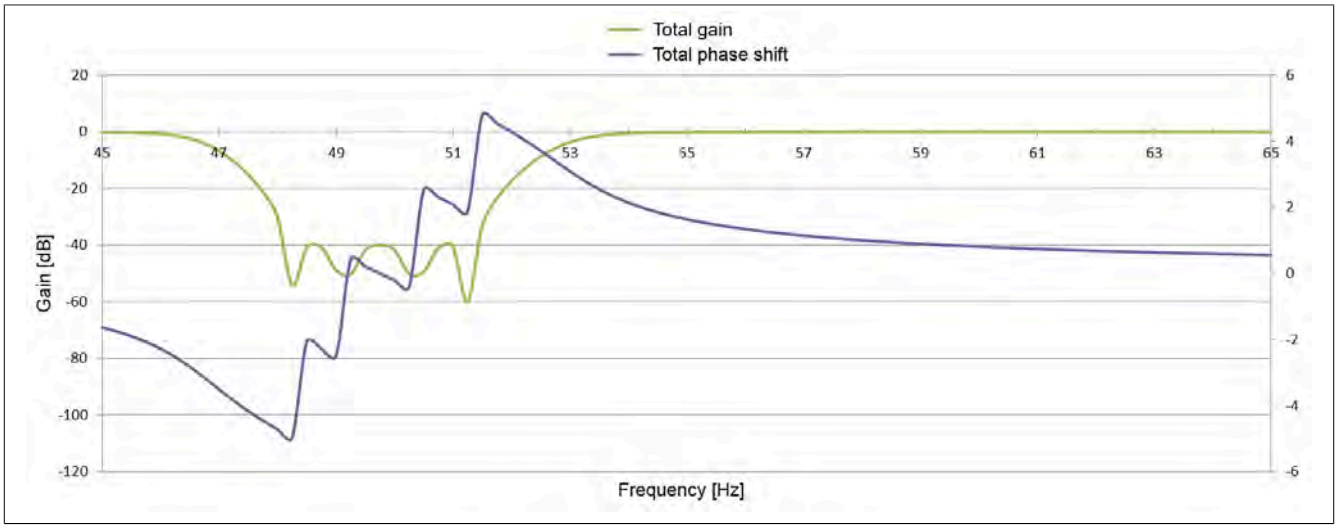
4.3.20.8.3.1 Filter characteristics of the IIR notch filter

There are three different filter characteristics that can be selected for both 50 Hz and 60 Hz (-40 dB, -60 dB and -80 dB). The higher the attenuation, the narrower the stopband.

Example 1

Filter characteristics for the following settings:

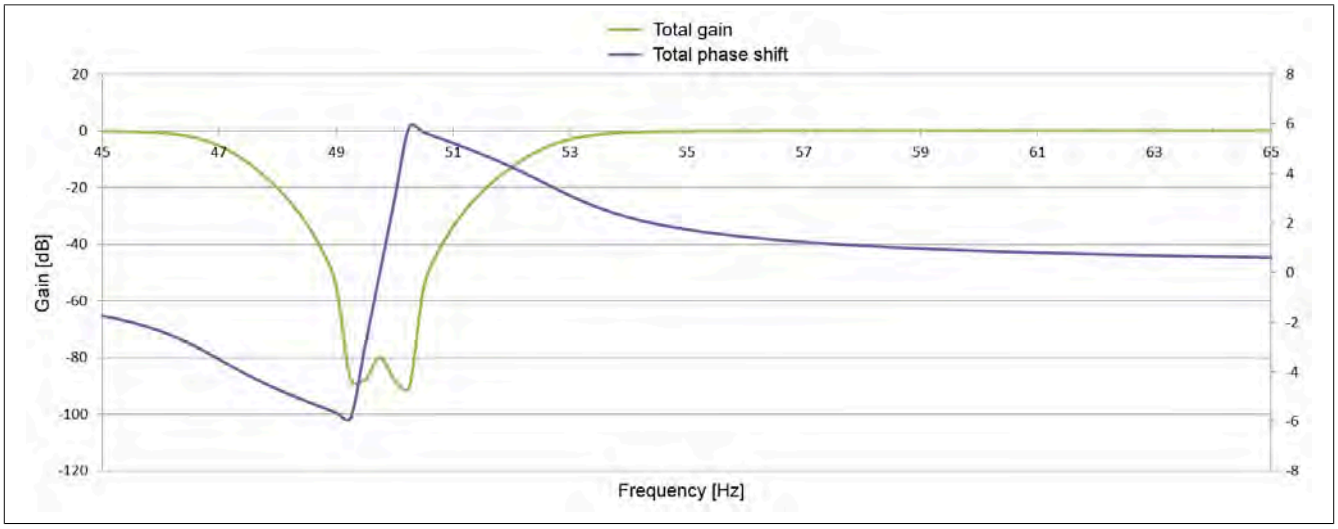
- Gain = -40 dB
- Frequency = 50 Hz
- Passband = 5 Hz
- Stopband = ±1 Hz



Example 2

Filter characteristics for the following settings:

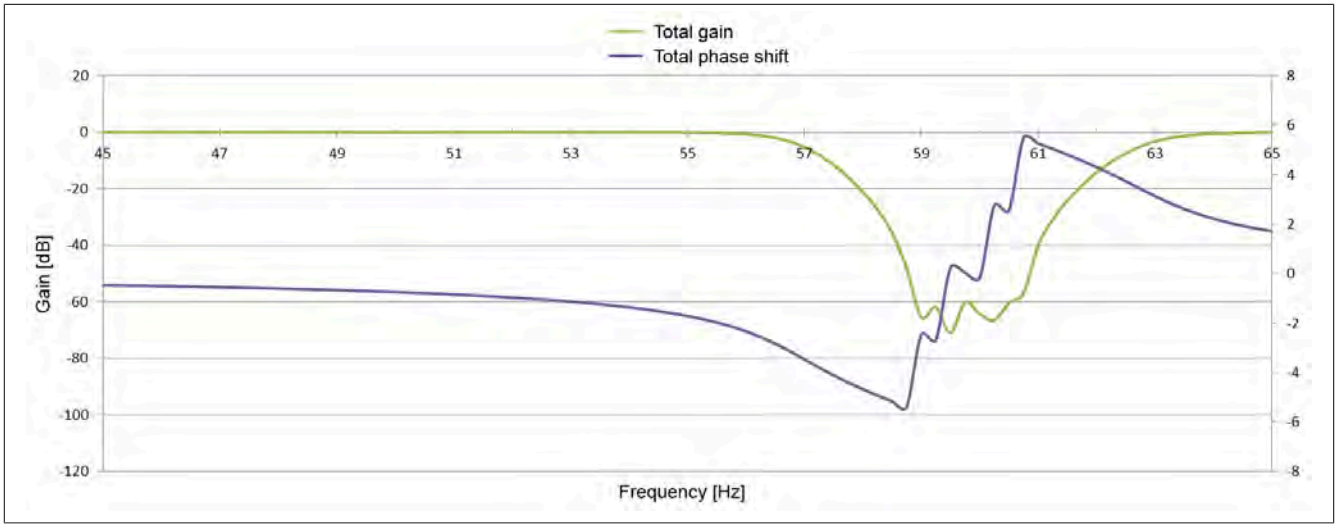
- Gain = -80 dB
- Frequency = 50 Hz
- Passband = 5 Hz
- Stopband = ±0.25 Hz



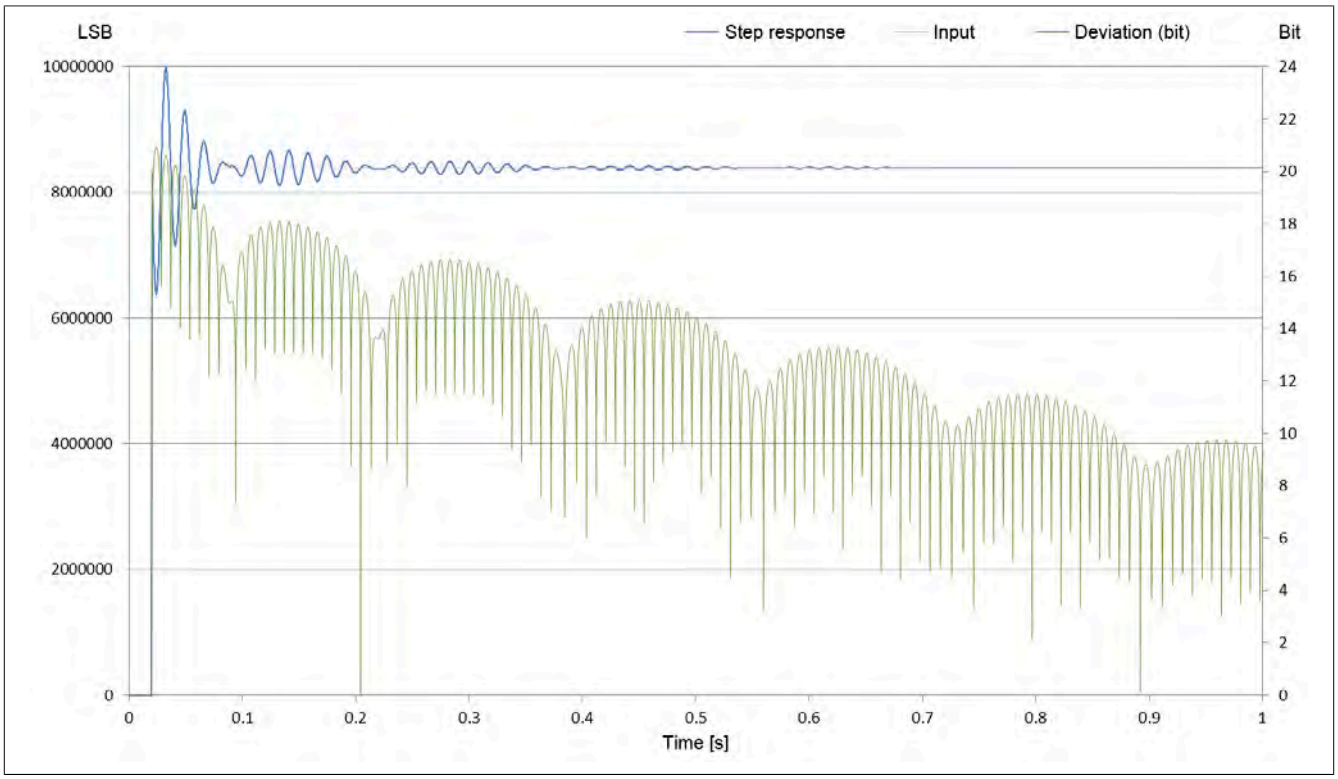
Example 3

Filter characteristics for the following settings:

- Gain = -60 dB
- Frequency = 60 Hz
- Passband = 5 Hz
- Stopband = ±0.5 Hz



Step response of an 8th-order IIR notch filter, including the deviation in bits:



4.3.20.9 Register description

4.3.20.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.20.9.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
2	ControlPacked01	UINT			•	
6	ControlPacked02	UINT			•	
514	ConfigChannel01	UINT				•
578	ConfigChannel02	UINT				•
Analog signal - Communication						
4	AnalogInput01	DINT	•			
12	AnalogInput02	DINT	•			
33	StatusPacked01	USINT	•			
35	StatusPacked02	USINT	•			
257	AdcConvCtr01	SINT	•			
268	AdcConvTimeStamp01	DINT	•			

4.3.20.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
2	2	ControlPacked01	UINT			•	
6	10	ControlPacked02	UINT			•	
514	514	ConfigChannel01	UINT				•
578	578	ConfigChannel02	UINT				•
Analog signal - Communication							
4	4	AnalogInput01	DINT	•			
12	12	AnalogInput02	DINT	•			
33	0	StatusPacked01	USINT	•			
35	8	StatusPacked02	USINT	•			

1) The offset specifies the position of the register within the CAN object.

4.3.20.9.3.1 CAN I/O bus controller

The module occupies 4 analog logical slots on CAN-I/O.

4.3.20.9.4 Configuration

4.3.20.9.4.1 Configuration of strain gauge inputs

Name:
ControlPacked01 and ControlPacked02

The strain gauge inputs are configured in these registers:

- Strain gauge factor factor of strain gauge load cell
- Enabling of filters

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information	
0 - 2	Strain gauge factor	000	Default: 256 mV/V	
		001	128 mV/V	
		010	64 mV/V	
		011	32 mV/V	
		100	16 mV/V	
		101	8 mV/V	
		110	4 mV/V	
		111	2 mV/V	
			Averaging	1. Notch frequency [Hz]
3 - 7	Moving average	00000	Default: Moving average disabled (bypass)	
		00001	2	2500
		00010	4	1250
		00011	5	1000
		00100	10	500
		00101	20	250
		00110	25	200
		00111	50	100
		01000	83	60
		01001	100	50
		01010	125	40
		01011	167	30
		01100	200	25
		01101	250	20
		01110	300	16.66
		01111	500	10
		10000	1000	5
		10001 to 11111	Reserved (firmware limited to 1000)	
8	Notch filter	0	Default: IIR notch filter disabled (bypass)	
		1	IIR notch filter enabled	
9	Reserved	0		
10 - 11	Low-pass filter mode	00	IIR low-pass filter disabled (bypass)	
		01	1st-order IIR low-pass filter (see section 4.3.20.8.1 "IIR low-pass filter")	
		10 - 11	Reserved: No IIR low-pass filter active	
			Filter level	-3 db frequency [Hz]
12 - 14	Low-pass filter level	000	1	575
		001	2	230
		010	3	106
		011	4	51
		100	5	25
		101	6	12.5
		110	7	6.2
		111	8	3.1
15	Reserved	0		

4.3.20.9.4.2 Channel configuration

Name:
ConfigChannel01 and ConfigChannel02

The IIR notch filter is configured individually for each channel in these registers.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 11	Reserved	0	
12 - 13	Notch filter attenuation	00	Gain: -40 dB Pass: ±5 Hz Stop: ±1 Hz
		01	Gain: -60 dB Pass: ±5 Hz Stop: ±0.5 Hz
		10	Gain: -80 dB Pass: ±5 Hz Stop: ±0.25 Hz
		11	Reserved
14	Notch filter frequency	0	At 50 Hz
		1	At 60 Hz
15	Reserved	0	

4.3.20.9.5 Communication

4.3.20.9.5.1 Analog input values

Name:
AnalogInput01 and AnalogInput02

The analog input value is mapped in this register.

Data type	Value	Input signal:
DINT	<-8,388,607	Negative invalid range
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8,388,606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open line
	>8,388,607	Positive invalid range

4.3.20.9.5.2 Status of analog inputs

Name:
StatusPacked01 and StatusPacked02

The status of analog inputs is mapped in these registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	I/O power supply	0	No error
		1	Error in power supply
1	Bypass current	0	No error
		1	Overcurrent (sum from all sensors)
2 - 3	Reserved	0	
4	ADC configuration	0	Already configured
		1	Not yet configured
5	Analog values	0	Analog value valid
		1	Analog value invalid (analog value = 0xFF800000). Possible causes: • Internal transfer error (XOR checksum verification) • Error in strain gauge supply (bit 1) • Error in I/O voltage supply (bit 0) • ADC not (yet) configured
6	Analog value range overrun	0	Analog value valid
		1	Analog value invalid. Possible causes: • Overflow / Open line (analog value = 0x007FFFFF) • Underflow (analog value = 0xFF800001)
7	Moving average filter	0	Moving average filter engaged
		1	Moving average filter not engaged Possible causes: • After changing the filter length • Consequence of the filter being reset by another error

4.3.20.9.5.3 ADC conversion counter

Name:
AdcConvCtr01

Instead of being measured simultaneously, the strain gauge channels of the module are measured according to the multiplexing procedure. The "AdcConvTimestamp01" register contains the timestamp of the encoded last channel converted in the "AdcConvCtr01" register. The timestamp of the other channels can then be calculated later using this information.

Data type	Value
SINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Index of the last converted channel	0	Analog input 1
		1	Analog input 2
		2	Reserved
		3	Reserved
2 - 7	Rotating cycle counter	x	Incremented at the end of a conversion cycle. All channels are converted in a conversion cycle.

4.3.20.9.5.4 ADC conversion timestamp

Name:
AdcConvTimestamp01

The timestamp of the last converted channel is stored in this register (see bits 0 and 1 in the "AdcConvCtr01" register). This is always the point in time (in µs) at which the conversion of the latest ADC raw value is completed.

Data type	Value	Function
DINT	-2,147,483,648 to 2,147,483,647	Timestamp (in µs) of the last converted channel (see bits 0 and 1 in the ADC conversion counter)

The timestamp of the remaining channels can be determined in the application using the number and timestamp of the last converted channel according to the following table.

Channel	Age difference
2 - 1	47 µs
1 - 2	153 µs

Example 1:

- Latest channel (bit 0 - 1 in the "AdcConvCtr01" register) = 01 (analog input 2):
- Timestamp: "AdcConvTimestamp01" register = 0 µs

Channel	Timestamp
2	0 µs
1	-47 µs

Example 2:

- Latest channel (bit 0 - 1 in the "AdcConvCtr01" register) = 00 (analog input 1):
- Timestamp: "AdcConvTimestamp01" register = 0 µs

Channel	Timestamp
1	0 µs
2	-153 µs

4.3.20.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.3.20.9.7 I/O update time

I/O update time
200 µs

4.3.21 X20AIB744

4.3.21.1 General information

This module works with 4-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage, or zero offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 4 full-bridge strain gauge inputs
- 5 kHz data output rate for all 4 channels
- Independently configurable strain gauge factor and filter level for each of the 4 channels

4.3.21.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AIB744	X20 analog input module, 4 full-bridge strain gauge inputs, 24-bit converter resolution, 2.5 kHz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 68: X20AIB744 - Order data

4.3.21.3 Technical data

Product ID	X20AIB744
Short description	
I/O module	4 full-bridge strain gauge inputs
General information	
B&R ID code	0xE286
Status indicators	Channel status, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Open line	Yes, using status LED and software
Input	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1 W
Additional power dissipation caused by the actuators (resistive) [W]	+1.43 [1]
Electrical isolation	
Bus - Analog input	Yes
Bus - Bridge supply voltage	Yes
Channel - Channel	No
Channel - I/O supply	No
Certification	
CE	Yes
ATEX Zone 2 [2]	Yes
GOST-R	Yes
Full-bridge strain gauge	
Strain gauge factor	2 to 256 mV/V, configurable using software
Connection	4-wire connections
Input type	Differential, used to evaluate a full-bridge strain gauge
Digital converter resolution	24-bit
Conversion time	200 µs
Data output rate	5000 samples per second and per channel (f_{DATA})
Input filter	
Cutoff frequency	2.5 kHz
Orderliness	3
Slope	60 dB

Table 69: X20AIB744 - Technical data

Product ID	X20AIB744
ADC filter characteristics	Sigma-delta, see section "Filter"
Operating range / Measurement sensor	85 to 5000 Ω
Influence of cable length	The shielded twisted pair cable should be as short as possible and run separately to the sensor (isolated from load circuit) without intermediate terminals
Input protection	RC protection
Common-mode range	0.6 to 3.8 VDC Permissible input voltage range (with regard to the potential strain gauge GND) on the inputs "Input +" and "Input -"
Isolation voltage between input and bus	500 V_{eff}
Conversion procedure	Sigma-delta
Output of the digital value	
Broken bridge supply line	Value approaches 0
Broken sensor line	Value approaches ±end value ("open circuit" status bit is set in the *Module status* register)
Valid value range	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)
Strain gauge supply	
Voltage	5.5 VDC / max. 65 mA per channel
Short circuit protection, overload protection	Yes
Quantization [3]	
LSB value	
2 mV/V	1.31 nV
4 mV/V	2.62 nV
8 mV/V	5.25 nV
16 mV/V	10.49 nV
32 mV/V	20.98 nV
64 mV/V	41.96 nV
128 mV/V	83.92 nV
256 mV/V	167.85 nV
Max. gain drift	35 ppm/°C [4]
Max. offset drift	15 ppm/°C [5]
Nonlinearity	<10 ppm [5]
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 69: X20AIB744 - Technical data

1) Depends on the full-bridge strain gauge used
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Quantization depends on the strain gauge factor.
4) Based on the current measured value.
5) Based on the entire measurement range.

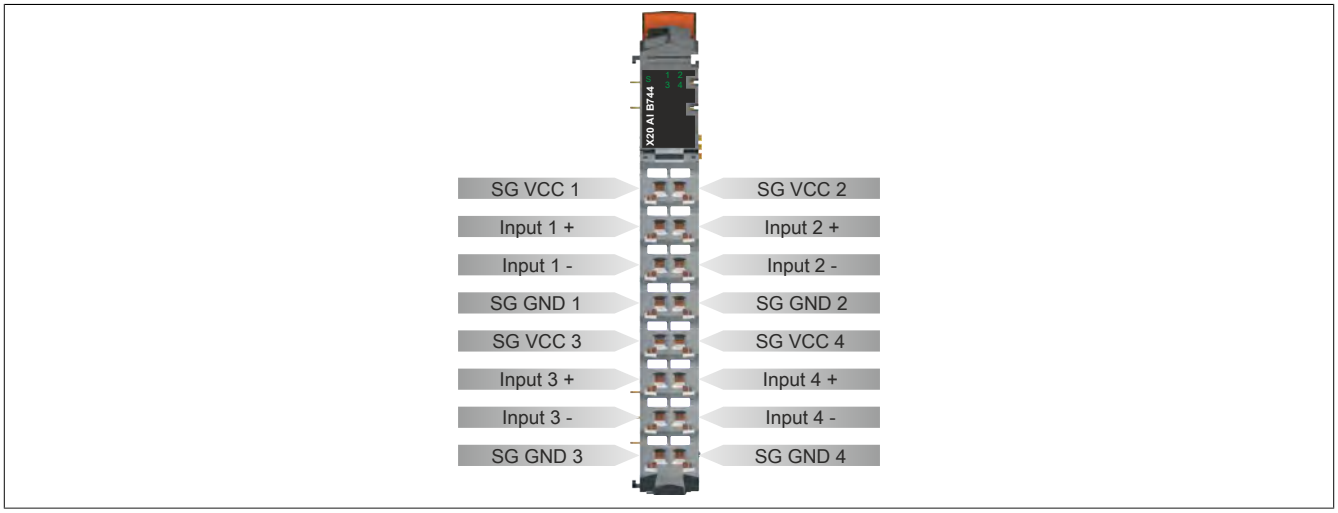
4.3.21.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

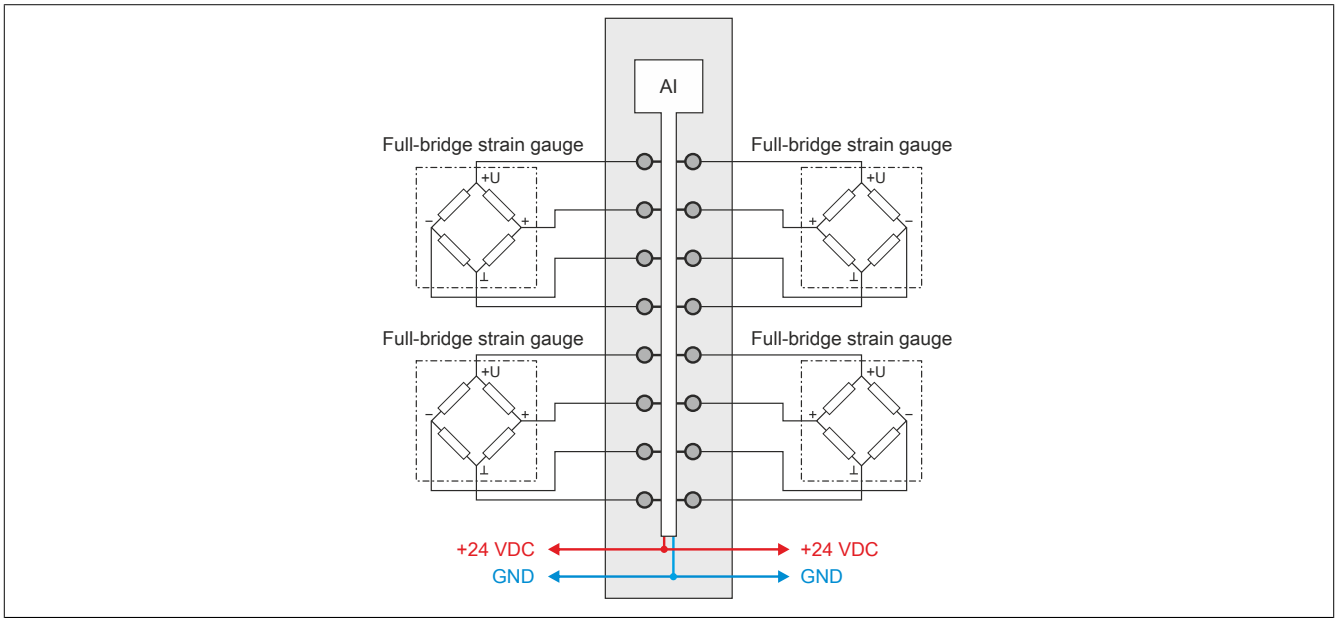
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	I/O supply outside limits
			On	Error or reset status
	1 - 4	Green	Off	Possible causes: • Supply error • Channel not yet configured
			Blinking	Possible causes: • Open line • Overvoltage • Undervoltage
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

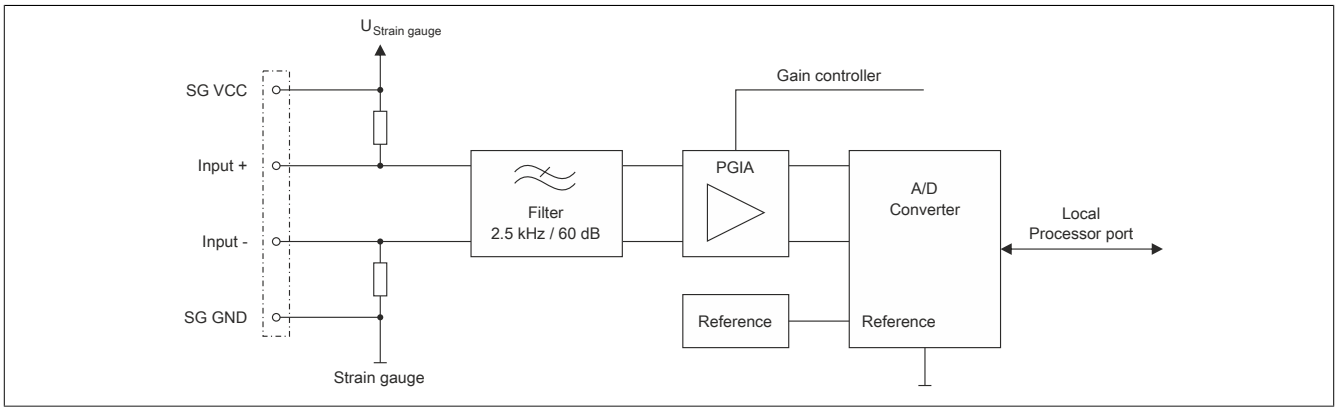
4.3.21.5 Pinout



4.3.21.6 Connection example



4.3.21.7 Input circuit diagram

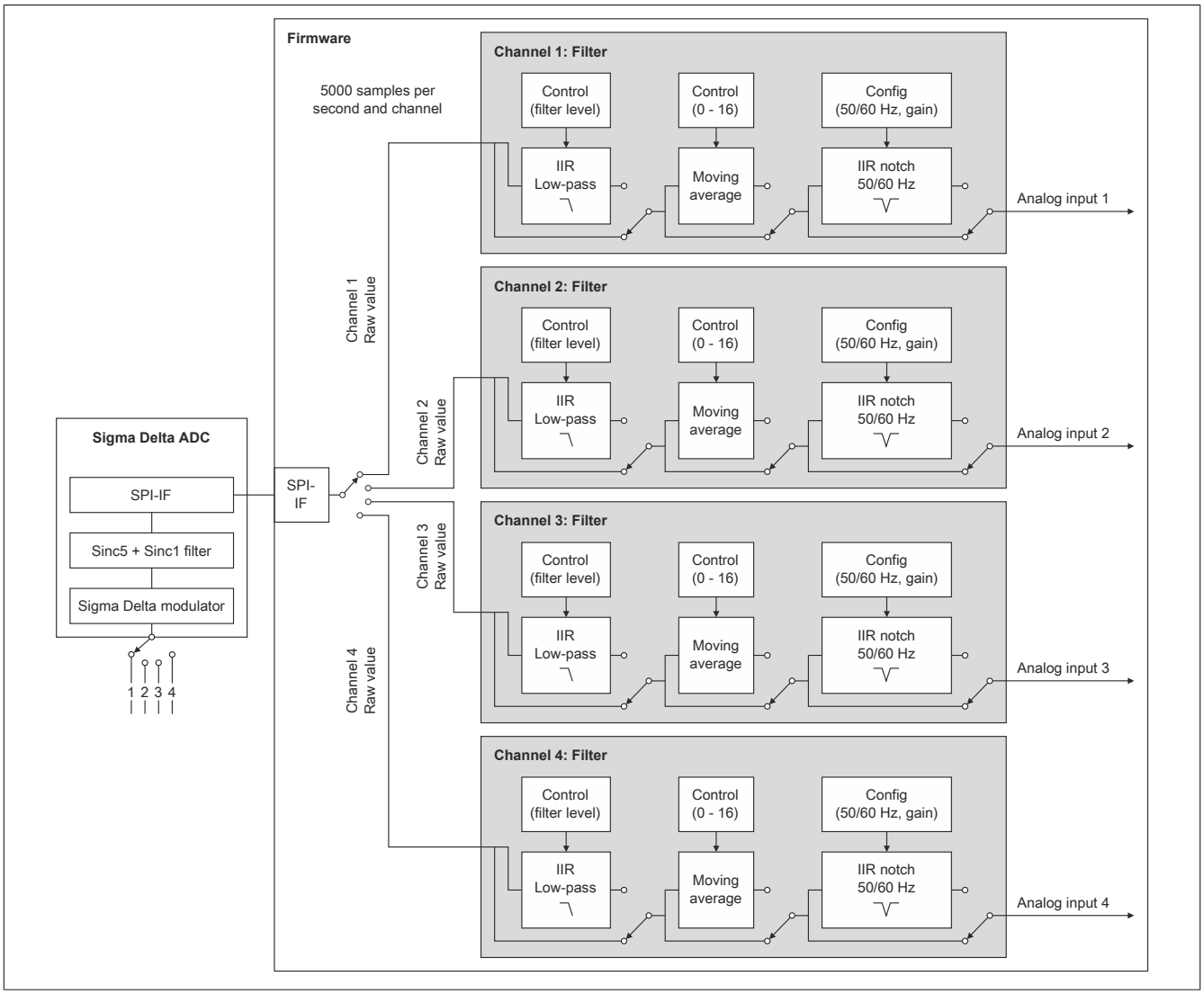


4.3.21.8 Filter

An independent cascade of filters is available for each channel. They can be individually enabled and configured at runtime. By default, all filters are disabled when the device is switched on. Filters are controlled and configured using the "ControlPacked0N" and "ConfigChannel0N" (N = 1 to 4) registers.

In order to allow the filter behavior to be adapted to the measuring situation or machine cycle (high dynamics and low precision or low dynamics and high precision), the filter characteristics of both the IIR low-pass filter as well as the moving average filter can be changed synchronously at any time.

Filter diagram



4.3.21.8.1 IIR low-pass filter

4.3.21.8.1.1 General information

The IIR low-pass filter is used to generally smooth and increase the resolution of the analog value. The filter works according to the following formula:

$$y = y_{Old} + \frac{x - y_{Old}}{2^{Filter\ level}}$$

x ... current filter input value
y_{Old} ... Old filter output value
y ... new filter output value

The "Filter level" parameter in the formula above is configured with the help of the "ControlPacked0N" register. "Filter level" = 0 if the IIR low-pass filter is disabled.

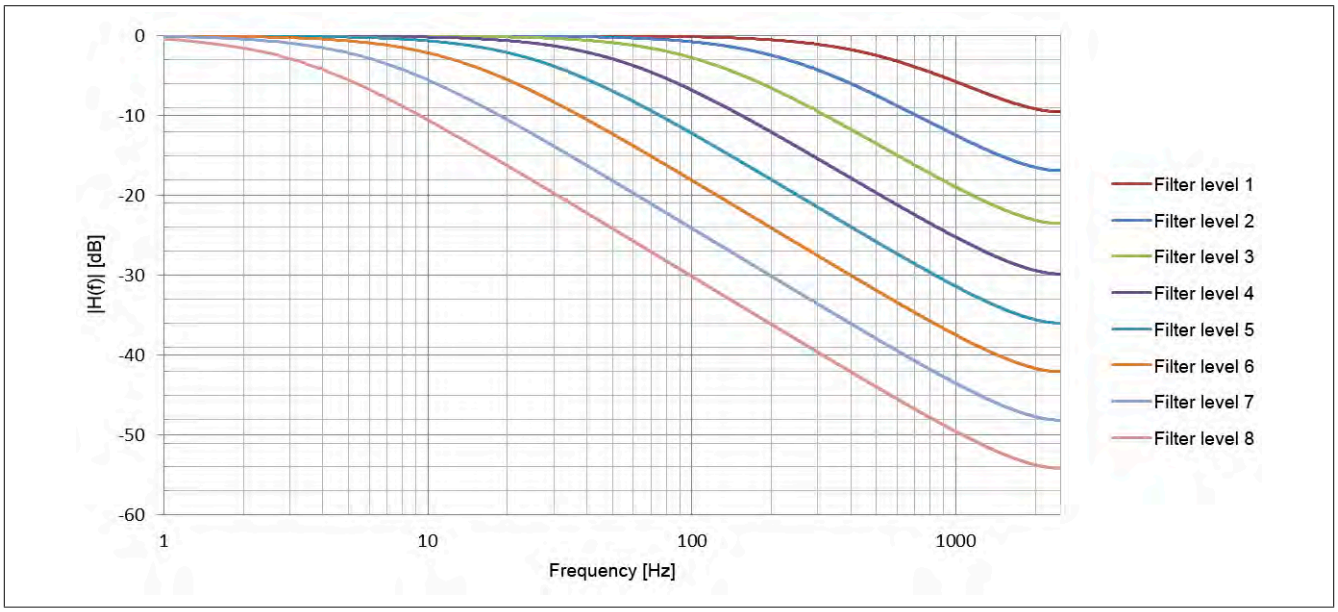
4.3.21.8.1.2 Filter characteristics of the 1st-order IIR low-pass filter

Limit frequency f_c

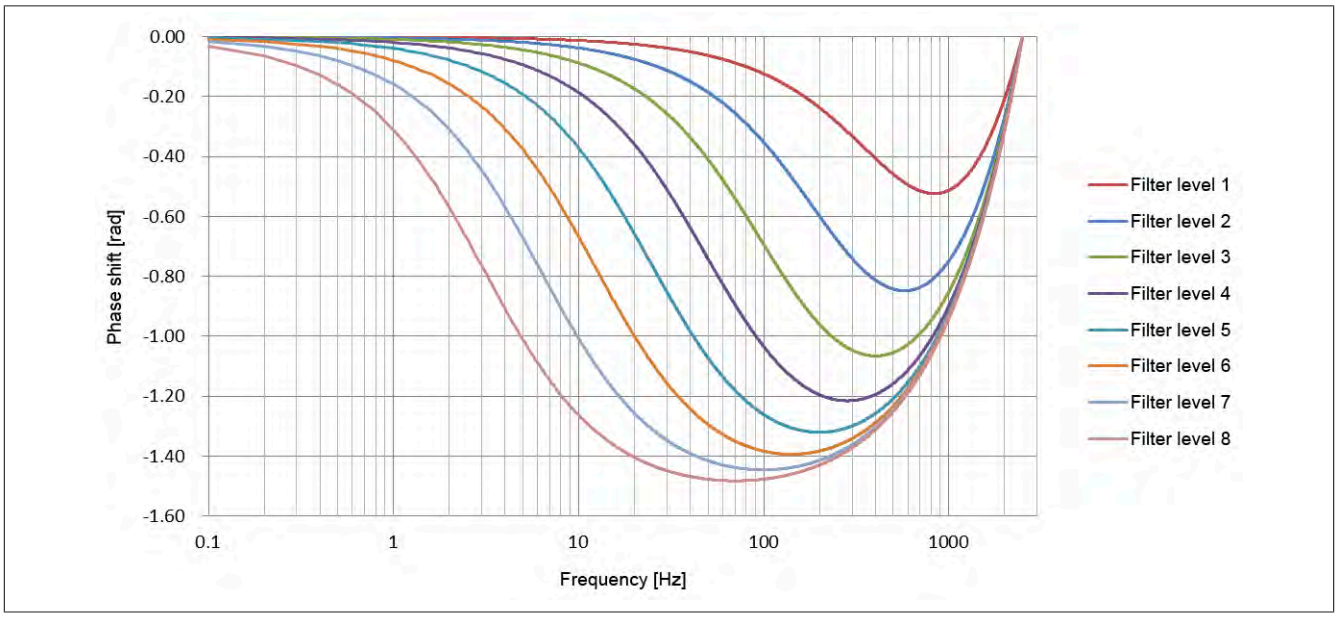
The following table provides an overview of the -3 dB limit frequency f_c depending on the configured filter level.

IIR low-pass filter level	f_c [Hz]
1	575
2	230
3	106
4	51
5	25
6	12.5
7	6.2
8	3.1

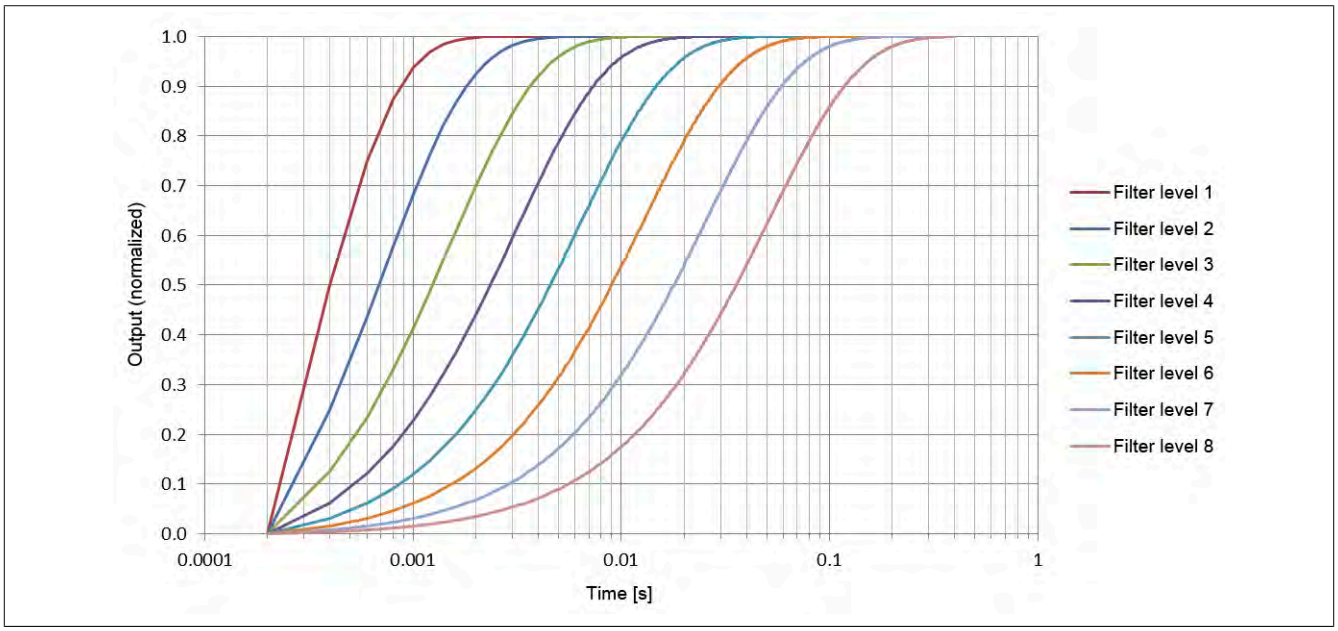
Gain of the IIR low-pass filter



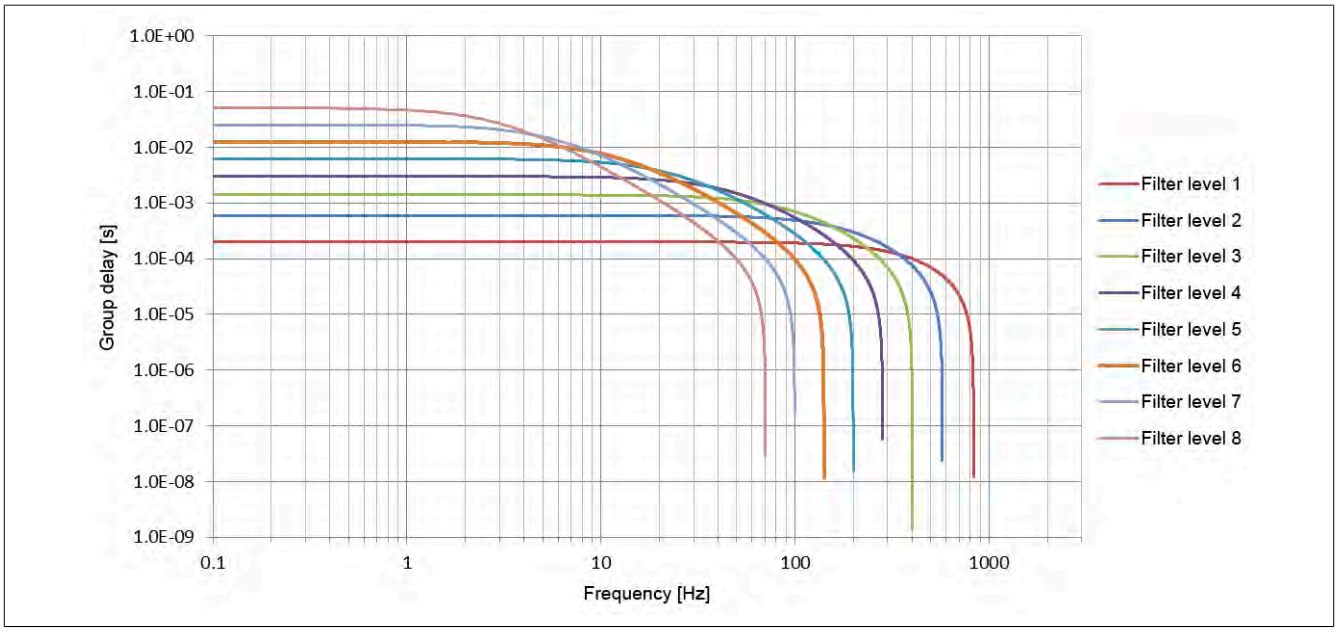
Phase shift of the IIR low-pass filter



Step response of the IIR low-pass filter



Group delay of the IIR low-pass filter



4.3.21.8.2 Sinc1 / Moving average filter

Like the low-pass filter, the moving average filter can also be used to smooth out the signal and increase its resolution. In addition, configuring the filter length accordingly makes it possible to target and efficiently filter out individual interference frequencies. The source of these interference frequencies may be mechanical or electromagnetic. Multiples of these are also filtered out (as long as they are a whole-number factor of the data output rate of 5000 samples per second and channel).

Example:
Data output rate = 5000 samples/s/channel, averaging over 4 values -> "Notch" at 1.25 kHz (and 2.5 kHz)

When reconfiguring the filter length from "n" to "m", it takes |m-n| * 200 µs until the desired filter length setpoint is reached again. As long as the filter length setpoint is not reached, this situation will be indicated by the bit 7 status bit in the "StatusPacked0N" register.

4.3.21.8.2.1 Filter characteristics of the moving average filter

Filter configuration	Filter length	f_{Notch} [Hz] 1)	f_c [Hz] 2)
0	1		
1	2	2500	1244
2	4	1250	568
3	5	1000	450
4	10	500	222
5	20	250	111
6	25	200	88.4
7	50	100	44.0
8	83	60.24	26.5
9	100	50	21.9
10	125	40	17.5
11	167	29.94	13.0
12	200	25	10.9
13	250	20	8.6
14	300	16.67	7.1
15	500	10	4.3
16	1000	5	2.0

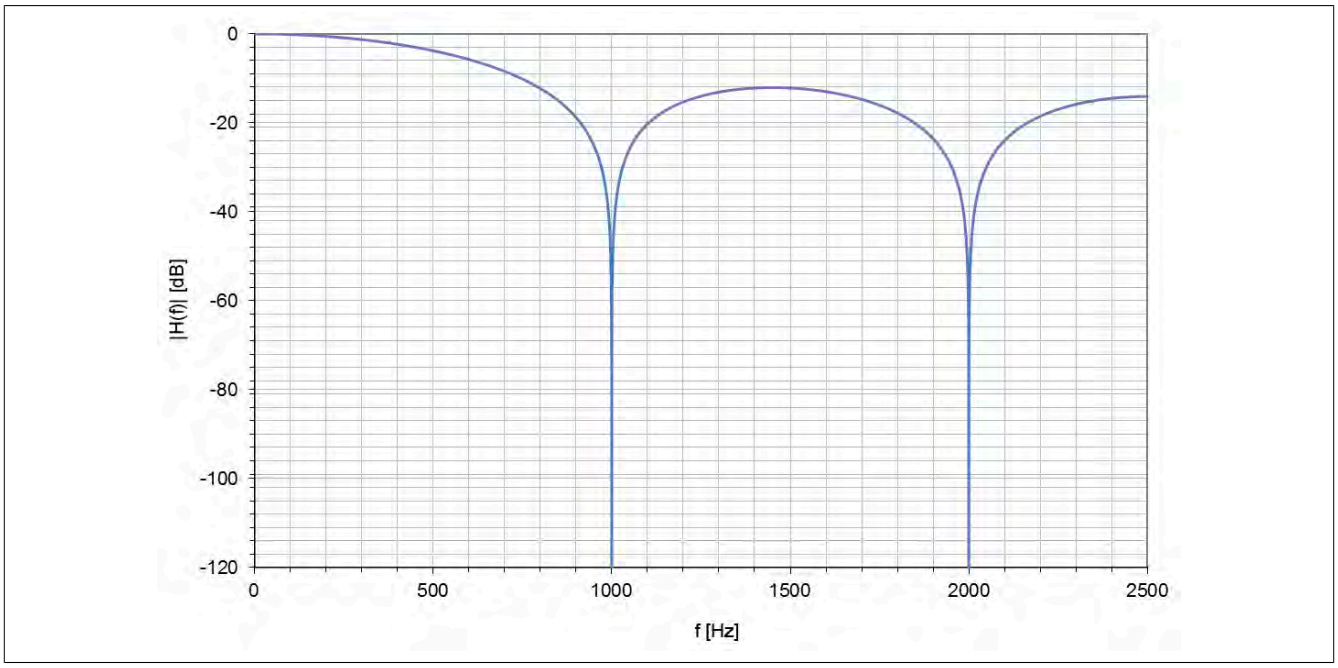
1) Mid-band frequency of the first attenuation maximum.
2) -3 dB limit frequency.

4.3.21.8.2.2 Examples for the gain of the moving average filter

Example 1

Filter setting = 3:

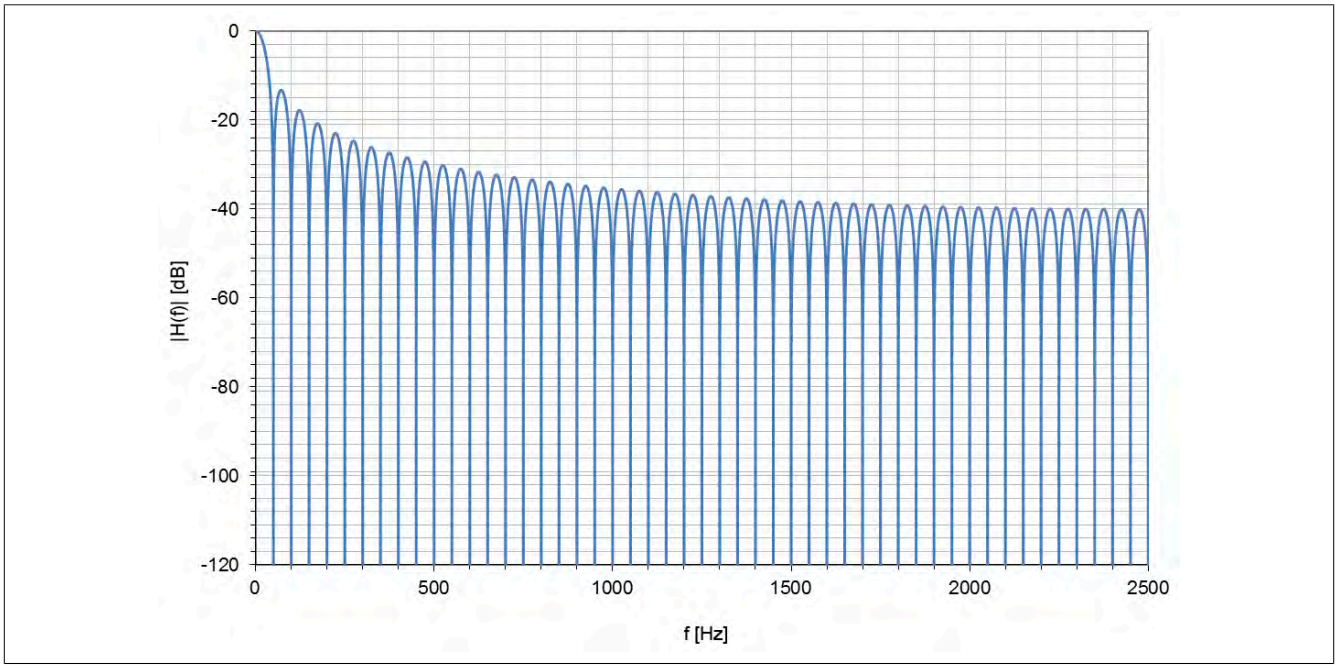
- f_{Notch} = 1000 Hz
- f_c = 449.6 Hz



Example 2

Filter setting = 9:

- f_{Notch} = 50 Hz
- f_c = 21.9 Hz



4.3.21.8.3 50/60 Hz IIR notch filter

The IIR notch filter is used for narrow-band suppression of interference caused by the mains frequency.

This is an 8th-order IIR notch filter implemented in the form of a cascade of 4 2nd-order IIR notch filters.

Information:

The IIR notch filter should only be enabled if there is actually interference being caused by the mains frequency. You should always check whether sufficiently low and sufficiently narrow band filtering at 50 Hz / 60 Hz can be implemented using a moving average filter (see section 4.3.20.8.2.1 "Filter characteristics of the moving average filter").

This is because, like every higher-order IIR notch filter, this filter also has a tendency to respond to an input step with an attenuating vibration. The higher the dynamics of the expected measurement signal, the greater the potential interfering effect of this vibration tendency. In extreme cases, the vibration can temporarily be greater than the mains interference that is supposed to be filtered out.

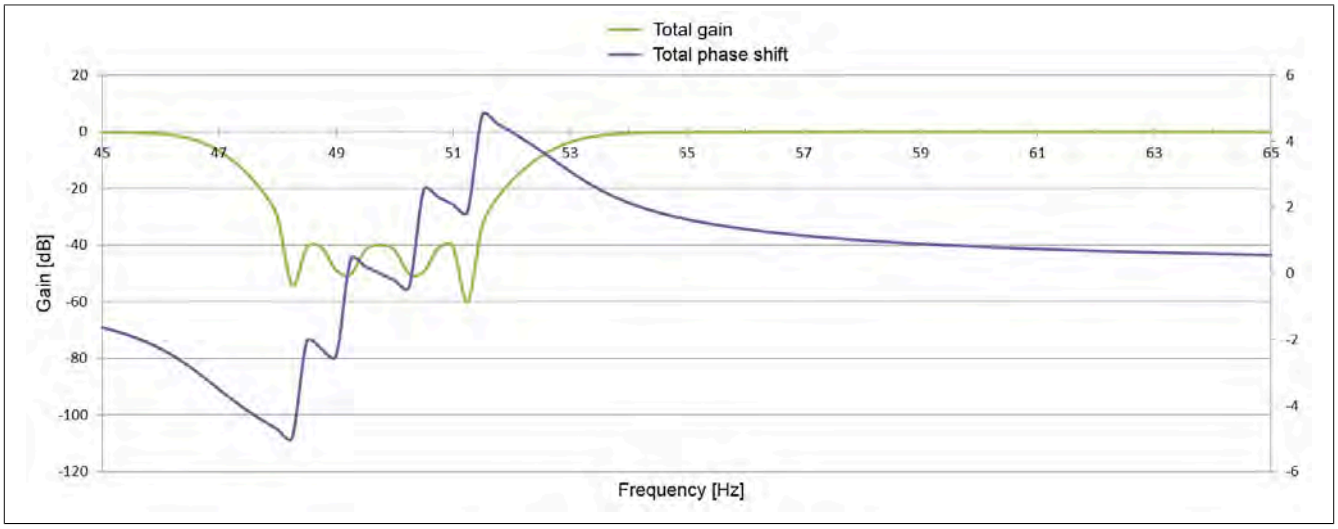
4.3.21.8.3.1 Filter characteristics of the IIR notch filter

There are three different filter characteristics that can be selected for both 50 Hz and 60 Hz (-40 dB, -60 dB and -80 dB). The higher the attenuation, the narrower the stopband.

Example 1

Filter characteristics for the following settings:

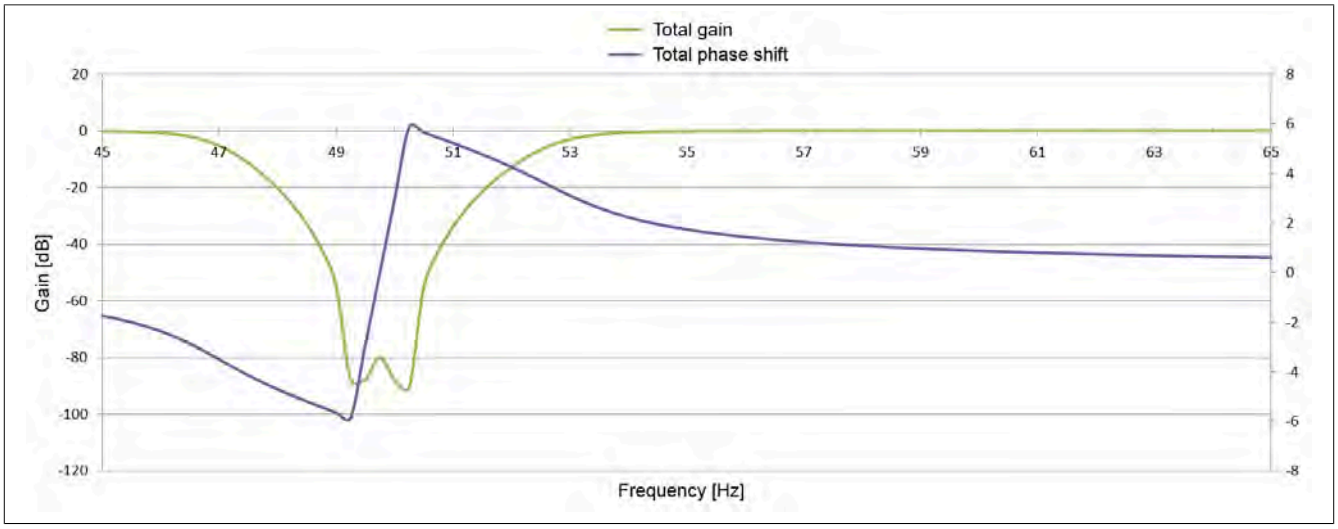
- Gain = -40 dB
- Frequency = 50 Hz
- Passband = 5 Hz
- Stopband = ±1 Hz



Example 2

Filter characteristics for the following settings:

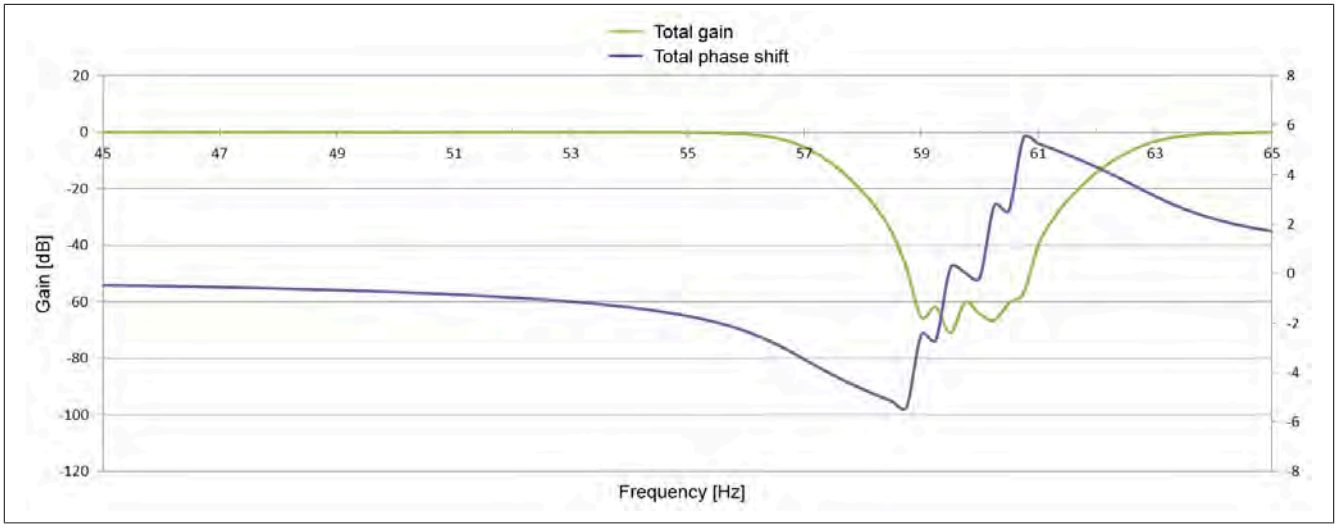
- Gain = -80 dB
- Frequency = 50 Hz
- Passband = 5 Hz
- Stopband = ±0.25 Hz



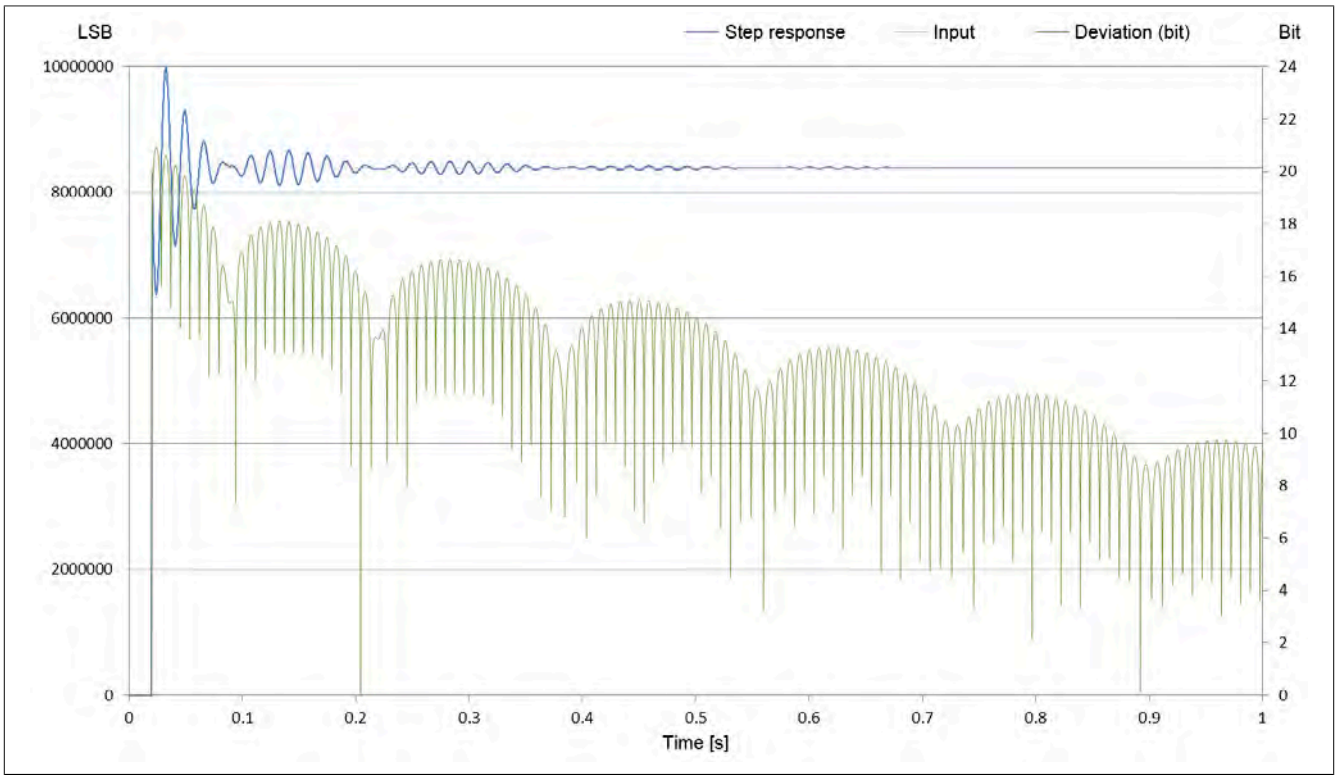
Example 3

Filter characteristics for the following settings:

- Gain = -60 dB
- Frequency = 60 Hz
- Passband = 5 Hz
- Stopband = ±0.5 Hz



Step response of an 8th-order IIR notch filter, including the deviation in bits:



4.3.21.9 Register description

4.3.21.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.21.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
2	ControlPacked01	UINT			●	
6	ControlPacked02	UINT			●	
10	ControlPacked03	UINT			●	
14	ControlPacked04	UINT			●	
514	ConfigChannel01	UINT				●
578	ConfigChannel02	UINT				●
642	ConfigChannel03	UINT				●
706	ConfigChannel04	UINT				●
Analog signal - Communication						
4	AnalogInput01	DINT	●			
12	AnalogInput02	DINT	●			
20	AnalogInput03	DINT	●			
28	AnalogInput04	DINT	●			
33	StatusPacked01	USINT	●			
35	StatusPacked02	USINT	●			
37	StatusPacked03	USINT	●			
39	StatusPacked04	USINT	●			
257	AdcConvCtr01	SINT	●			
268	AdcConvTimeStamp01	DINT	●			

4.3.21.9.3 Function model 254 - Bus controller

Register	Offset [1]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
2	2	ControlPacked01	UINT			●	
6	10	ControlPacked02	UINT			●	
10	18	ControlPacked03	UINT			●	
14	26	ControlPacked04	UINT			●	
514	514	ConfigChannel01	UINT				●
578	578	ConfigChannel02	UINT				●
642	642	ConfigChannel03	UINT				●
706	706	ConfigChannel04	UINT				●
Analog signal - Communication							
4	4	AnalogInput01	DINT	●			
12	12	AnalogInput02	DINT	●			
20	20	AnalogInput03	DINT	●			
28	28	AnalogInput04	DINT	●			
33	0	StatusPacked01	USINT	●			
35	8	StatusPacked02	USINT	●			
37	16	StatusPacked03	USINT	●			
39	24	StatusPacked04	USINT	●			

1) The offset specifies the position of the register within the CAN object.

4.3.21.9.3.1 CAN I/O bus controller

The module occupies 4 analog logical slots on CAN-I/O.

4.3.21.9.4 Configuration

4.3.21.9.4.1 Configuration of strain gauge inputs

Name:
ControlPacked01 to ControlPacked04

The strain gauge inputs are configured in these registers:

- Strain gauge factor factor of strain gauge load cell
- Enabling of filters

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information	
0 - 2	Strain gauge factor	000	Default: 256 mV/V	
		001	128 mV/V	
		010	64 mV/V	
		011	32 mV/V	
		100	16 mV/V	
		101	8 mV/V	
		110	4 mV/V	
		111	2 mV/V	
			Averaging	1. Notch frequency [Hz]
3 - 7	Moving average	00000	Default: Moving average disabled (bypass)	
		00001	2	2500
		00010	4	1250
		00011	5	1000
		00100	10	500
		00101	20	250
		00110	25	200
		00111	50	100
		01000	83	60
		01001	100	50
		01010	125	40
		01011	167	30
		01100	200	25
		01101	250	20
		01110	300	16.66
		01111	500	10
		10000	1000	5
		10001 to 11111	Reserved (firmware limited to 1000)	
8	Notch filter	0	Default: IIR notch filter disabled (bypass)	
		1	IIR notch filter enabled	
9	Reserved	0		
10 - 11	Low-pass filter mode	00	IIR low-pass filter disabled (bypass)	
		01	1st-order IIR low-pass filter (see section 4.3.20.8.1 "IIR low-pass filter")	
		10 - 11	Reserved: No IIR low-pass filter active	
			Filter level	-3 db frequency [Hz]
12 - 14	Low-pass filter level	000	1	575
		001	2	230
		010	3	106
		011	4	51
		100	5	25
		101	6	12.5
		110	7	6.2
		111	8	3.1
15	Reserved	0		

4.3.21.9.4.2 Channel configuration

Name:
ConfigChannel01 to ConfigChannel04

The IIR notch filter is configured individually for each channel in these registers.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 11	Reserved	0	
12 - 13	Notch filter attenuation	00	Gain: -40 dB Pass: ±5 Hz Stop: ±1 Hz
		01	Gain: -60 dB Pass: ±5 Hz Stop: ±0.5 Hz
		10	Gain: -80 dB Pass: ±5 Hz Stop: ±0.25 Hz
		11	Reserved
14	Notch filter frequency	0	At 50 Hz
		1	At 60 Hz
15	Reserved	0	

4.3.21.9.5 Communication

4.3.21.9.5.1 Analog input values

Name:
AnalogInput01 to AnalogInput04

The analog input value is mapped in this register.

Data type	Value	Input signal:
DINT	<-8,388,607	Negative invalid range
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8,388,606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open line
	>8,388,607	Positive invalid range

4.3.21.9.5.2 Status of analog inputs

Name:
StatusPacked01 to StatusPacked04

The status of analog inputs is mapped in these registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	I/O power supply	0	No error
		1	Error in power supply
1	Bypass current	0	No error
		1	Overcurrent (sum from all sensors)
2 - 3	Reserved	0	
4	ADC configuration	0	Already configured
		1	Not yet configured
5	Analog values	0	Analog value valid
		1	Analog value invalid (analog value = 0xFF800000). Possible causes: • Internal transfer error (XOR checksum verification) • Error in strain gauge supply (bit 1) • Error in I/O voltage supply (bit 0) • ADC not (yet) configured
6	Analog value range overrun	0	Analog value valid
		1	Analog value invalid. Possible causes: • Overflow / Open line (analog value = 0x007FFFFF) • Underflow (analog value = 0xFF800001)
7	Moving average filter	0	Moving average filter engaged
		1	Moving average filter not engaged Possible causes: • After changing the filter length • Consequence of the filter being reset by another error

4.3.21.9.5.3 ADC conversion counter

Name:
AdcConvCtr01

Instead of being measured simultaneously, the strain gauge channels of the module are measured according to the multiplexing procedure. The "AdcConvTimestamp01" register contains the timestamp of the encoded last channel converted in the "AdcConvCtr01" register. The timestamp of the other channels can then be calculated later using this information.

Data type	Value
SINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Index of the last converted channel	0	Analog input 1
		1	Analog input 2
		2	Analog input 3
		3	Analog input 4
2 - 7	Rotating cycle counter	x	Incremented at the end of a conversion cycle. All channels are converted in a conversion cycle.

4.3.21.9.5.4 ADC conversion timestamp

Name:
AdcConvTimestamp01

The timestamp of the last converted channel is stored in this register (see bits 0 and 1 in the "AdcConvCtr01" register). This is always the point in time (in µs) at which the conversion of the latest ADC raw value is completed.

Data type	Value	Function
DINT	-2,147,483,648 to 2,147,483,647	Timestamp (in µs) of the last converted channel (see bits 0 and 1 in the ADC conversion counter)

The timestamp of the remaining channels can be determined in the application using the number and timestamp of the last converted channel according to the following table.

Channel	Age difference
4 - 3	47 µs
3 - 2	47 µs
2 - 1	47 µs
1 - 4	59 µs

Example:

- Latest channel (bit 0 - 1 in the "AdcConvCtr01" register) = 01 (analog input 2):
- Timestamp: "AdcConvTimestamp01" register = 0 µs

Channel	Timestamp
2	0 µs
1	-47 µs
4	-47-59 = -106 µs
3	-47-59-47 = -153 µs

4.3.21.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.3.21.9.7 I/O update time

I/O update time
200 µs

4.3.22 X20(c)AP31x1

4.3.22.1 General information

Power monitoring

These modules measure active, reactive and apparent power individually for each of the three phases and for all of them collectively. The power consumption of each phase and the total sum is also recorded. In addition, the modules provide the RMS values for voltage and current on the three phases. When measuring the current, the value of the current through the neutral line can also be detected and monitored. Measurement of the mains frequency and the phase angle of the three phases (current and voltage) complete the power measurement data.

Energy management

The integrated functions on the modules map the immediate power requirements of the machine in detail and also record its total power consumption. For the user, all relevant data is prepared and made available in the process image.

The ability to measure currents and voltages up to the 31st harmonic enables higher precision recording of RMS values. This allows the modules to easily cope with irregular sine curves, and makes them well-suited to renewable energy applications. In these types of applications, being able to accurately measure the frequency at a resolution of 0.01 Hz between 45-65 Hz is a great advantage. In general, the modules are suitable for use with 1-phase, 2-phase or 3-phase power mains.

Features

- Calculate RMS values from currents and voltages
- Calculate active, reactive and apparent power
- Calculate active, reactive and apparent energy
- Phasing detection
- Measure individual phases and calculate cumulative values
- Optionally measure current through the neutral line
- Calculate frequency and harmonics with high precision

4.3.22.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.3.22.3 Order data

Model number	Short description	Figure
	Analog inputs	
X20AP3111	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 20 mA AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	
X20AP3121	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	
X20cAP3121	X20 energy metering module, coated, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	
X20AP3131	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 5 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	
X20AP3161	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 333 mV AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed	
	Required accessories	
	Bus modules	
X20BM32	X20 bus module for double-width modules, 240 VAC keyed, internal I/O supply continuous	
X20cBM32	X20 bus module, coated, for double-width modules, 240 VAC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 70: X20AP3111, X20AP3121, X20cAP3121, X20AP3131, X20AP3161 - Order data

4.3.22.4 Technical data - X20AP3111, X20AP3121, X20P3131 and X20cAP3121

Product ID	X20AP3111	X20AP3121	X20cAP3121	X20AP3131	X20AP3161
Short description					
I/O module	3-phase power and energy metering module for current/current transformers				3-phase power and energy metering module for current/voltage transformers
General information					
B&R ID code	0xC9DA	0xC9DB	0xE214	0xC9DC	0xE17B
Status indicators	I/O function per channel, operating state, module status				
Diagnostics					
Module run/error	Yes, using status LED and software				
Inputs	Yes, using status LED and software				
Power consumption					
Bus	0.85 W				
Internal I/O	-				
Additional module power dissipation [W]	40 mW [1]	2 W [1]			- [2]
Electrical isolation					
Channel - Bus	Yes				
Channel - Channel	No				
Isolation voltage					
Inputs - Bus / I/O supply	Tested at 5500 VDC, 1 min				
Inputs - Ground	Tested at 5500 VDC, 1 min				
Bus / I/O supply - Ground	Tested at 510 VAC, 1 min				
Certification					
CE	Yes				
cULus	Yes				
ATEX Zone 2 [3]	Yes				
GOST-R	Yes				
Voltage inputs					
Number of phases	3				
Nominal voltage					
Between phases	Max. 480 VAC				
Phase to N	Max. 277 VAC				
Max. overload voltage	1.25 x U_N for 10 min 2 x U_N for 1 min				
Max. display value	655 VAC				
Resolution	10 mV, with voltage connected directly				
Rated frequency	50 and 60 Hz				
Current inputs					
Quantity	4 AC inputs				
Nominal current					
Secondary	20 mA	1 A		5 A	333 mV
Primary	65 A directly configurable, larger values through conversion in the application [4]				
Max. overload current	20 x I_N for 0.5 s	8 x I_N for 0.5 s			-
Max. measurement current	20 mA	1 A		5 A	333 mV
Resolution	1 mA, based on the primary current [4]				
Load	25 Ω	500 mΩ		20 mΩ	-
Measurement precision					
U_{RMS} and I_{RMS}	<0.5%				
Effective, reactive and apparent power	<0.5% on average				
Frequency, power factor and phase angle	<0.5% [5]				
Calibration accuracy	<0.15 %				
Active energy per phase and total					
Power factor = 1.0	0.1% [6]				
Power factor = 0.5 L	0.1% [7]				
Power factor = 0.8 C	0.1% [5]				
Active energy of fundamental frequency per phase and total					
Power factor = 1.0	0.2% [6]				
Power factor = 0.5 L	0.2% [7]				
Power factor = 0.8 C	0.2% [5]				
Active energy of harmonics per phase and total					
sin ϕ = 1.0	0.5% [6]				
sin ϕ = 0.5 L	0.5% [7]				
sin ϕ = 0.8 C	0.5% [5]				
Reactive energy per phase and total					
sin ϕ = 1.0	0.2% [6]				
sin ϕ = 0.5 L	0.2% [7]				
sin ϕ = 0.8 C	0.2% [5]				

Table 71: X20AP3111, X20AP3121, X20cAP3121, X20AP3131, X20AP3161 - Technical data

Product ID	X20AP3111	X20AP3121	X20cAP3121	X20AP3131	X20AP3161
Apparent energy					
Per phase and arithmetic total	0.2%				
Vector sum	0.5%				
Operating conditions					
Mounting orientation					
Horizontal	Yes				
Vertical	Yes				
Installation at elevations above sea level					
0 to 2000 m	No limitations				
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m				
EN 60529 protection	IP20				
Environmental conditions					
Temperature					
Operation					
Horizontal installation	-25 to 60°C				
Vertical installation	-25 to 50°C				
Derating	-	See section "Derating"			-
Storage	-40 to 85°C				
Transport	-40 to 85°C				
Relative humidity					
Operation	5 to 95%, non-condensing		Up to 100%, condensing	5 to 95%, non-condensing	
Storage	5 to 95%, non-condensing				
Transport	5 to 95%, non-condensing				
Mechanical characteristics					
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM32 bus module separately		Order 1x X20TB32 terminal block separately Order 1x X20cBM32 bus module separately	Order 1x X20TB32 terminal block separately Order 1x X20BM32 bus module separately	
Spacing	25 $^{+0.2}$ mm				

Table 71: X20AP3111, X20AP3121, X20cAP3121, X20AP3131, X20AP3161 - Technical data

1) Power dissipation of current measurement shunts.
2) Shunts are external current transformers
3) Ta min.: 0°C
   Ta max.: See environmental conditions
4) For measuring higher current values, see section "Current transformer - Pinout".
5) From 0.151 VAC to 480 VAC
6) From 0.101 VAC to 480 VAC
7) From 0.126 VAC to 480 VAC

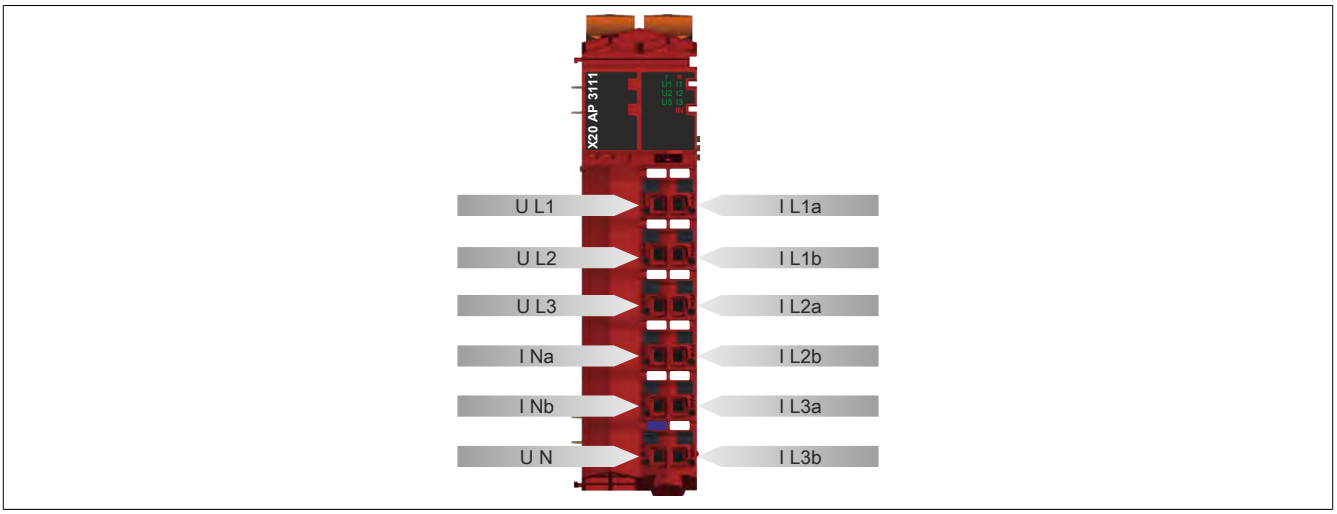
4.3.22.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	**Operating status**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
	Module status			
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	Analog input voltage			
	U1 - U3	Green / yellow	Off	Display disabled or U_{RMS} < "Fail" threshold value
		Green	Blinking	Phase sequence is correct and U_{RMS} < "Warning" threshold value
			On	Phase sequence is correct and U_{RMS} > "Warning" threshold value
		Yellow	Blinking	Phase sequence is incorrect and U_{RMS} < "Warning" threshold value
			On	Phase sequence is incorrect and U_{RMS} > "Warning" threshold value
	Analog input current			
	I1 - I3	Green / yellow	Off	Display disabled or I_{RMS} < "Display" threshold value
		Green	On	Active power positive
		Yellow	On	Active power negative
	Analog input neutral current			
	IN	Red	Off	Neutral current monitoring disabled
			On	Neutral current > threshold value

1) Depending on the configuration, a firmware update can take up to several minutes.

4.3.22.6 Pinout



Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.3.22.6.1 Current transformer connections

In order to be able to properly calculate values that reference all 3 phases (e.g. total active power, total reactive power, etc.), it is important for the current transformer phases to be connected correctly.

- A output on the transformer to the respective Ixa input on the module
- B output on the transformer to the respective Ixb input on the module

Converter	Input	Output
1	I L1a	
2	I L	
3		

4.3.22.7 Current transformer

Potential-free measurement of the AC current requires a current transformer. The current transformer is a transducer that delivers a secondary signal proportional to the primary current. This secondary signal is measured by the module. The maximum directly configurable primary current is 65 A. Values higher than 65 A can also be measured by implementing a transformation in the software application (see explanation and example provided below).

The maximum secondary signal depends on the module:

Module	Secondary current/voltage
X20AP3111	20 mA
X20AP3121	1 A
X20AP3131	5 A
X20AP3161	333 mV

The rated transformation ratio is calculated using the following formula:

X20AP3111 - X20AP3221 - X20AP3131	Rated transformation ratio $K_n = \frac{\text{primary nominal current}}{\text{secondary nominal current}}$
X20AP3161	No transformation; the maximum primary current corresponds to the 333 mV

A smaller transformation ratio should be defined for measuring higher primary currents. The values calculated by the module must be converted in the application according to the real rated transformation ratio that must be defined.

Example: Currents of up to 100 A are flowing on the primary side. A current transformer with a rated transformation ratio of 100/1 A is used. A rated transformation ratio of 50/1 A is defined in the module to match the current transformer. If the primary current calculated by the module is 40 A, then the actual value will be calculated as follows:

Actual primary current = 40 A * 100 / 50 = 80 A
Actual resolution = 1 mA * 100 / 50 = 2 mA

Note: **The same factor must be used for all power ratings and energy values when making the transformation.**

Caution!

To prevent damaging the module, you must ensure the current inputs are electrically isolated. This is done by connecting one transformer for each current input that is being used.

The current inputs on the module are not electrically isolated, so the secondary circuit between the transformer and the module must not be grounded. Grounding would distort the measurement and show current values that are too low!

Any other devices connected to this secondary circuit must also be electrically isolated (see also Fig. 105 "Input circuit diagram of current inputs")!

4.3.22.8 Voltage transformer

Voltage transformers are not provided in the configuration by default (e.g. by setting the transformation ratio).

They can, however, be used to measure higher voltages than the nominal voltages specified in the technical data. Similar to current value correction (see 4.3.22.7 "Current transformer") the rated transformation ratio between primary and secondary voltage should be calculated and applied.

Information:

The same factor must be used for all voltage values, power ratings and energy values when making the transformation.

4.3.22.9 Input circuit diagram

AC voltage inputs

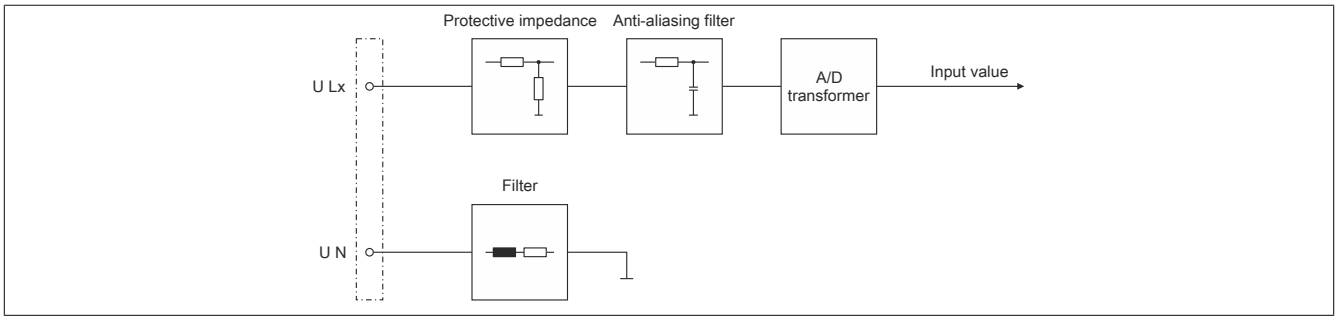


Figure 104: Input circuit diagram of voltage inputs

AC current inputs

AP3111, AP3121, AP3131: (Current measurement)

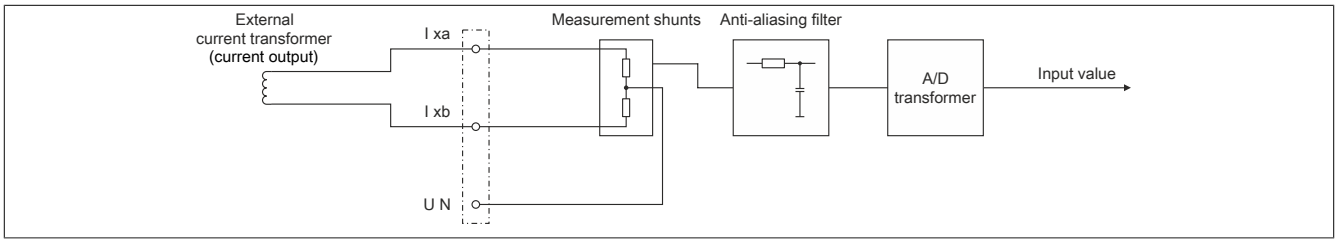
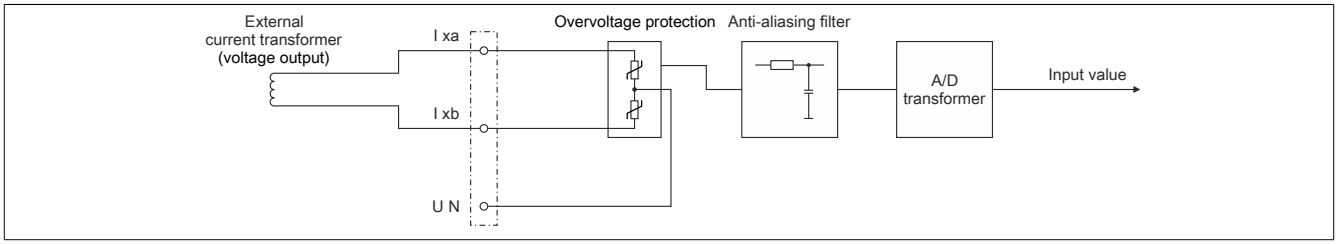


Figure 105: Input circuit diagram of current inputs

AP3161: (Voltage measurement)



4.3.22.10 Typical connection examples for different mains configurations

General information

There are many different mains configurations around the world. This section will present a few typical connection examples.

Connection example 1 - Mains A

This example involves a 3-element, 3-phase, 4-line star measurement with grounded neutral conductor and optional fault current detection.

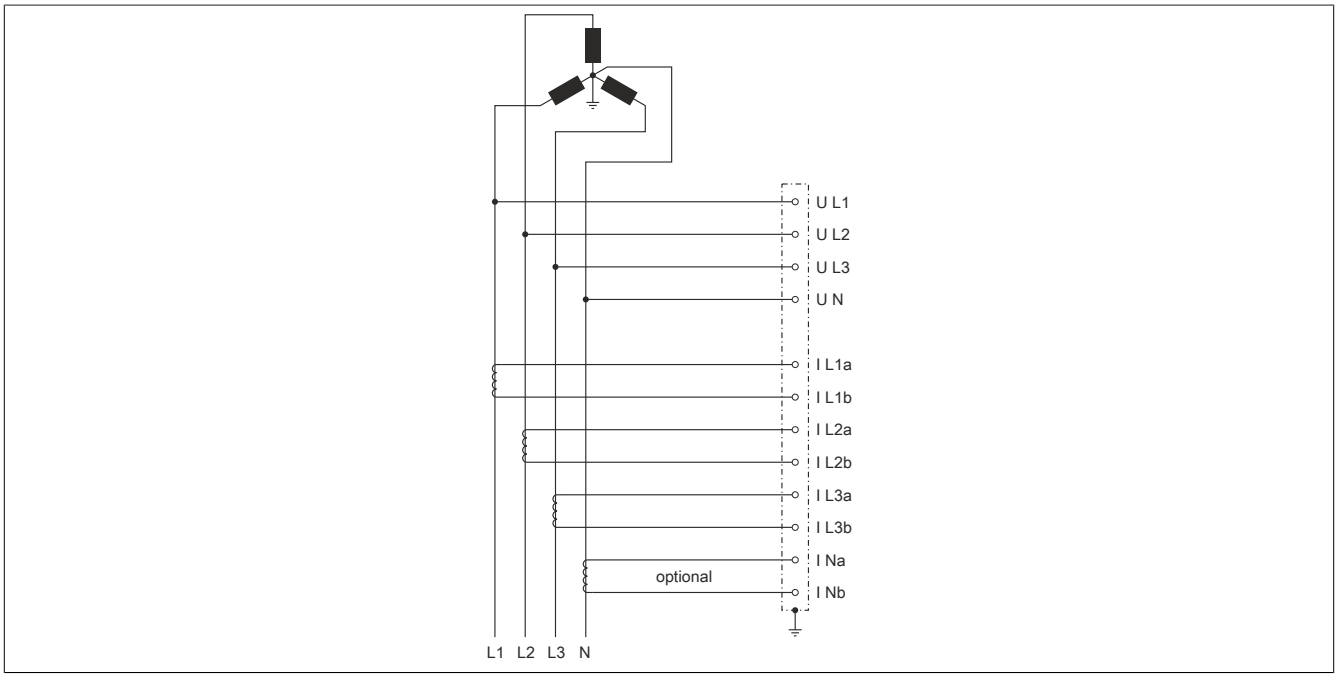


Figure 106: Supported mains configuration A

Connection example 2 - Mains B

This example involves a 3-element, 3-phase, 3-line star measurement.

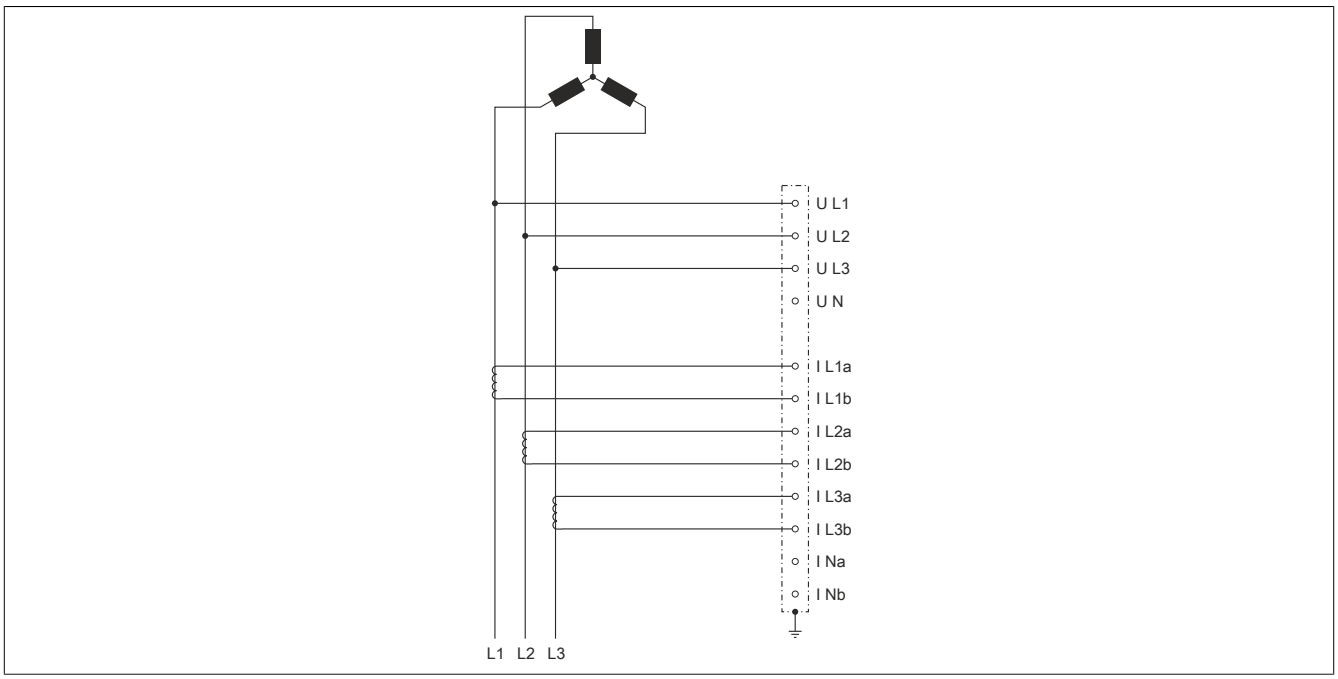


Figure 107: Supported mains configuration B

Connection example 3 - Mains C

This example involves a 3-element, 3-phase, 3-line star measurement with grounded neutral conductor and optional fault current detection.

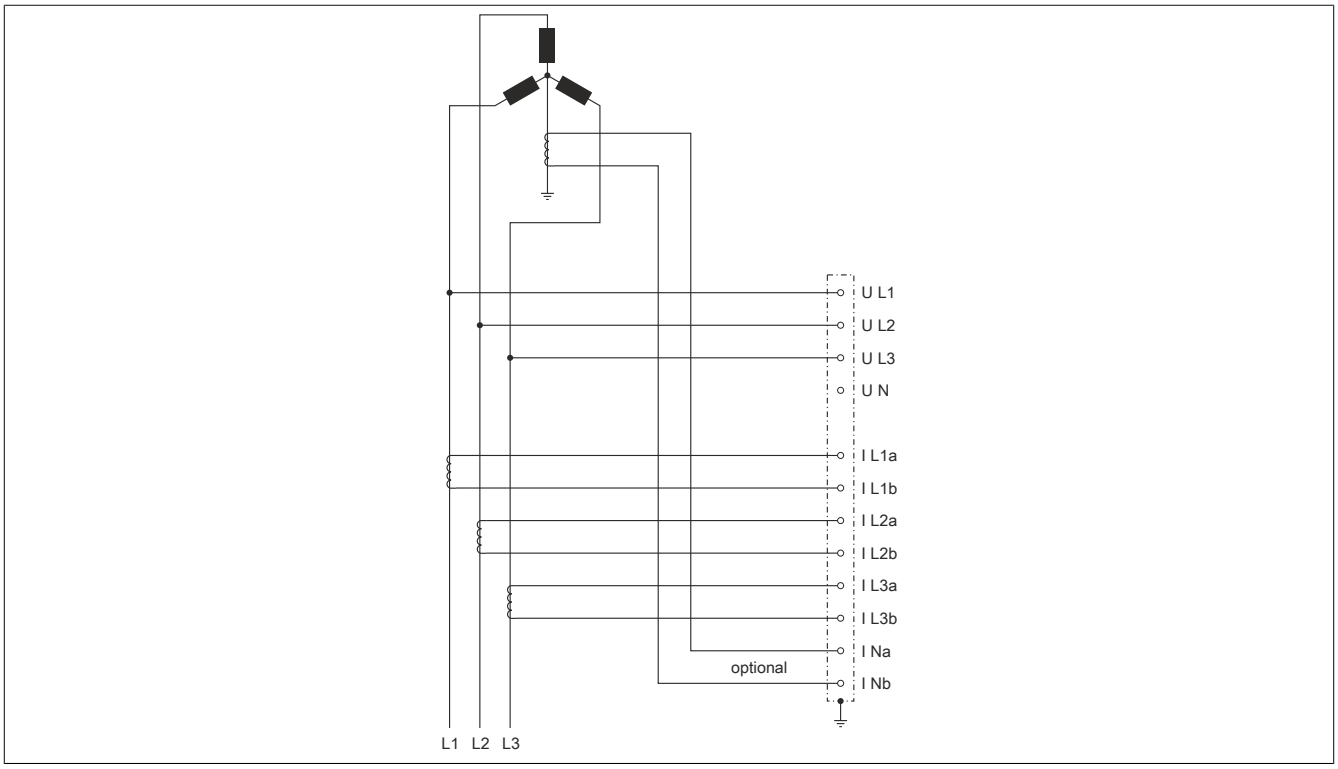


Figure 108: Supported mains configuration C

Connection example 4 - Mains D

This example involves a 3-element, 3-phase, 4-line star measurement with optional fault current detection.

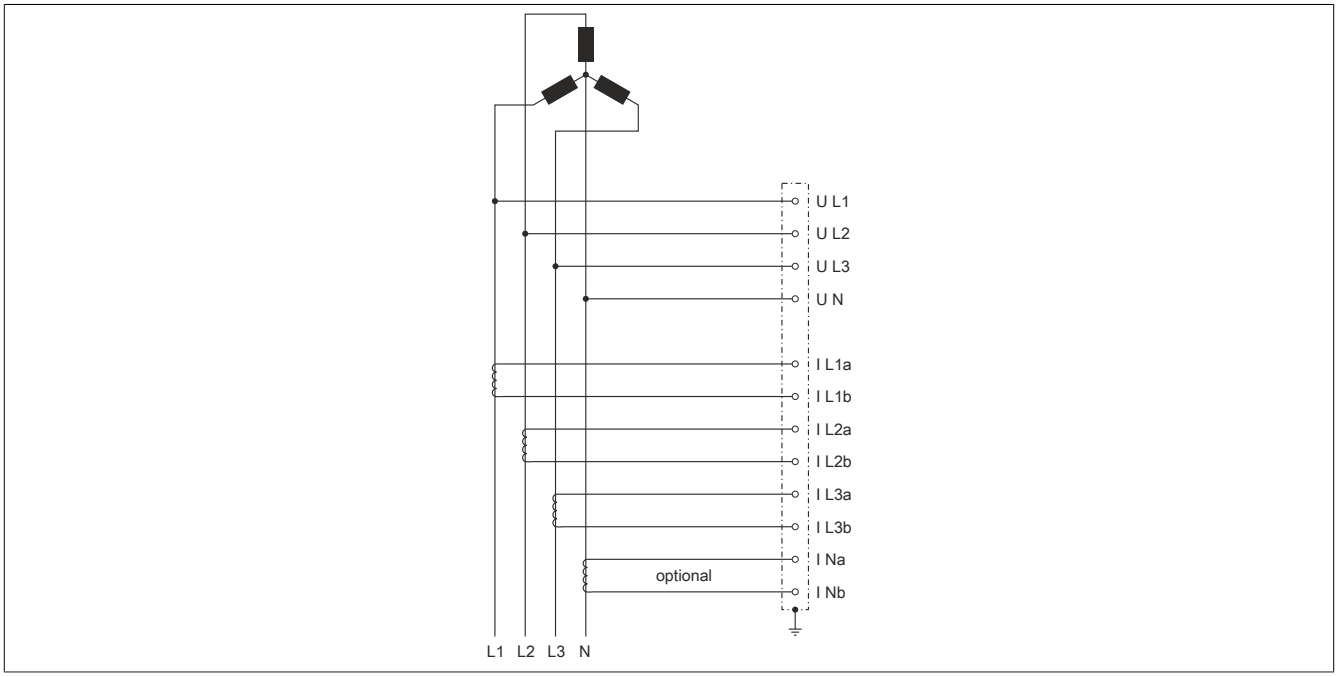


Figure 109: Supported mains configuration D

Connection example 5 - Mains E

This example involves a 2-element, 2-phase, 3-line star measurement with grounded neutral line conductor.

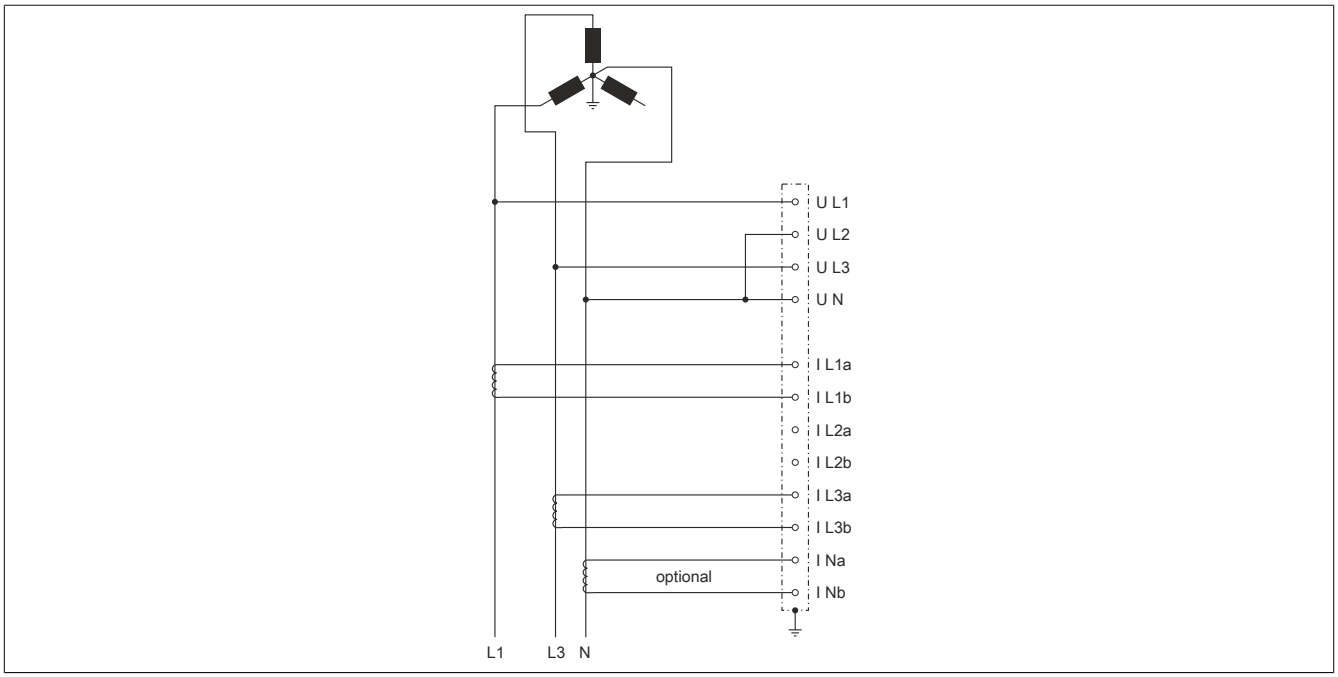


Figure 110: Supported mains configuration E

Connection example 6 - Mains F

This example involves a 3-element, 3-phase, 3-line delta measurement.

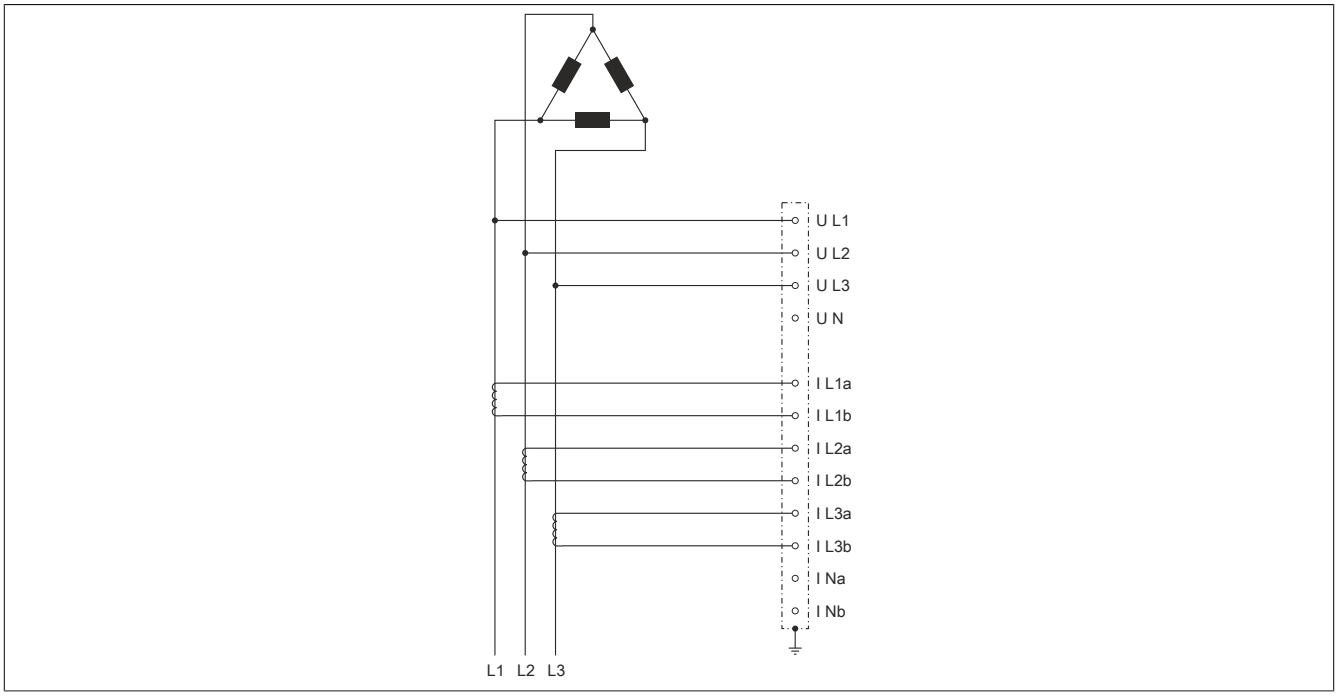


Figure 111: Supported mains configuration F

Connection example 7 - Mains G

This example involves a 3-element, 3-phase, 4-line delta measurement with grounded neutral.

Information:

The maximum voltage value specified in the data sheet must not be exceeded!

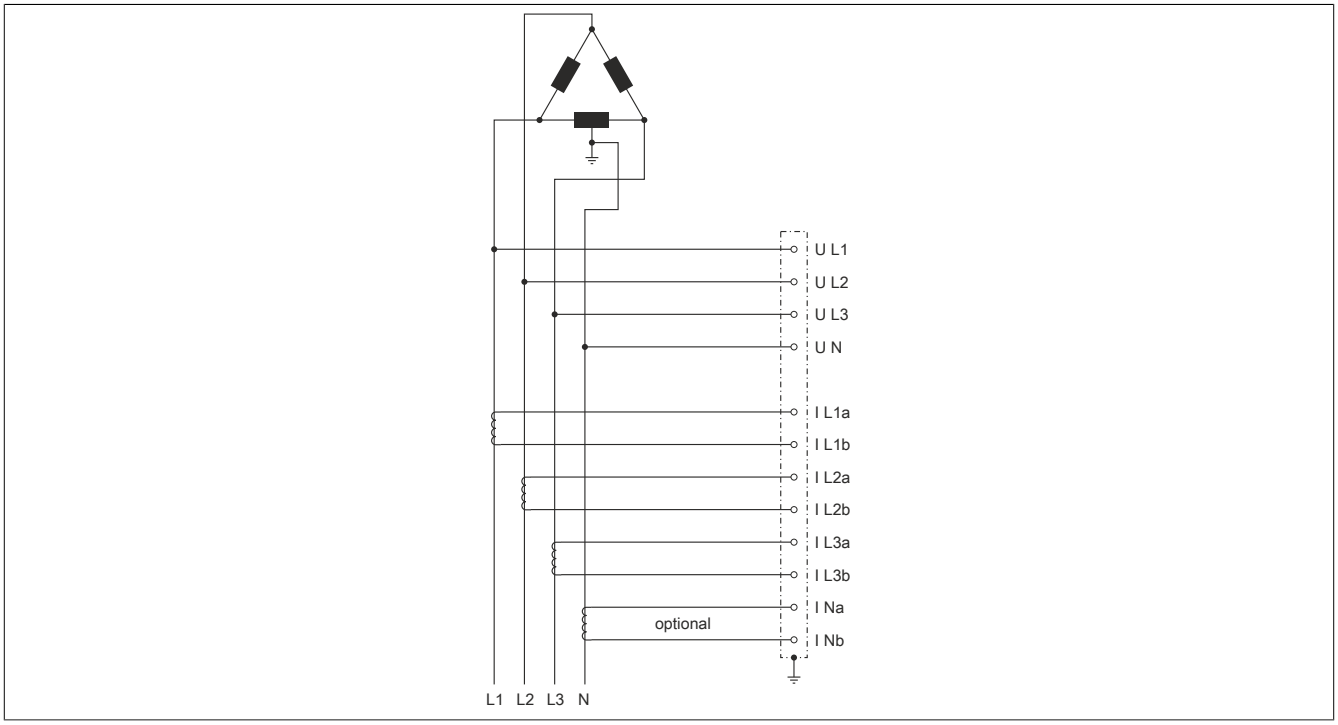


Figure 112: Supported mains configuration G

4.3.22.11 Register description

4.3.22.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.3.22.11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Standard register						
2	PmeanT	INT	•			
4	QmeanT	INT	•			
6	SmeanT	INT	•			
8	AEnergyT	DINT	•			
12	REnergyT	DINT	•			
130	StatusInput	UINT	•			
	CntPulseActive	Bit 0				
	CntPulseApparent	Bit 1				
	CntPulseActiveFund	Bit 2				
	CntPulseActiveHarm	Bit 3				
	ZeroCrossA	Bit 4				
	ZeroCrossB	Bit 5				
	ZeroCrossC	Bit 6				
	RBTrigDFT	Bit 8				
	RBUpdateEnergy	Bit 9				
	RBClearEnergy	Bit 10				
	RBForceEnergy	Bit 11				
194	ControlOutput	UINT			•	
	TrigDFT	Bit 0				
	EnabEnergy	Bit 1				
	ClearEnergy	Bit 2				
	ForceEnergy	Bit 3				
Analog status registers						
266	SysStatus1	UINT	•			
270	SysStatus2	UINT	•			
274	SysStatus3	UINT	•			
278	SysStatus4	UINT	•			
265	SystemStatusSel01	USINT	•			
	SumStatusPhaseLoss	Bit 2				
	SumStatusPhaseWarning	Bit 3				
	ErrOrderPhasecurrent	Bit 6				
	ErrOrderPhaseVoltage	Bit 7				
271	SystemStatusSel02	USINT	•			
	SumStatusWarningTHDCurrent	Bit 2				
	SumStatusWarningTHDVoltage	Bit 3				
	ErrIrmsNCalc	Bit 6				
	ErrIrmsNMeas	Bit 7				
278	PhaseStatus	UINT	•			
	LossPhaseC	Bit 0				
	LossPhaseB	Bit 1				
	LossPhaseA	Bit 2				
	WarningPhaseC	Bit 4				
	WarningPhaseB	Bit 5				
	WarningPhaseA	Bit 6				
Analog RMS registers						
290	IrmsN (measured)	UINT	•			
294	UrmsA	UINT	•			
298	UrmsB	UINT	•			
302	UrmsC	UINT	•			
306	IrmsNcalc (calculated)	UINT	•			
310	IrmsA	UINT	•			
314	IrmsB	UINT	•			
318	IrmsC	UINT	•			
Analog THD and angle registers						
538	Freq	UINT	•			
542	PAngleA	INT	•			
546	PAngleB	INT	•			
550	PAngleC	INT	•			
554	Temperature	INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
558	UAngleA	INT	●			
562	UAngleB	INT	●			
564	UAngleC	INT	●			
Analog power registers						
778	PmeanT	INT	●			
782	PmeanA	INT	●			
786	PmeanB	INT	●			
790	PmeanC	INT	●			
794	QmeanT	INT	●			
798	QmeanA	INT	●			
802	QmeanB	INT	●			
806	QmeanC	INT	●			
810	SmeanT	INT	●			
814	SmeanA	INT	●			
818	SmeanB	INT	●			
822	SmeanC	INT	●			
826	PFmeanT	INT	●			
830	PFmeanA	INT	●			
834	PFmeanB	INT	●			
838	PFmeanC	INT	●			
Analog energy registers						
4108	APenergyT	UDINT	●			
4116	APenergyA	UDINT	●			
4124	APenergyB	UDINT	●			
4132	APenergyC	UDINT	●			
4140	ANenergyT	UDINT	●			
4148	ANenergyA	UDINT	●			
4156	ANenergyB	UDINT	●			
4164	ANenergyC	UDINT	●			
4172	RPenergyT	UDINT	●			
4180	RPenergyA	UDINT	●			
4188	RPenergyB	UDINT	●			
4196	RPenergyC	UDINT	●			
4204	RNenergyT	UDINT	●			
4212	RNenergyA	UDINT	●			
4220	RNenergyB	UDINT	●			
4228	RNenergyC	UDINT	●			
4236	SAenergyT	UDINT	●			
4244	SenergyA	UDINT	●			
4252	SenergyB	UDINT	●			
4260	SenergyC	UDINT	●			
4268	SVenergyT	UDINT	●			
4404	AEnergyT	DINT	●			
4412	REnergyT	DINT	●			
Module configuration						
1026	ChanControl	UINT				●
1030	IDispTh	UINT				●
1034	I_RatioA	UINT				●
1038	I_RatioB	UINT				●
1042	I_RatioC	UINT				●
1046	I_RatioN	UINT				●
1050	CfgUpdate	UINT				●
1054	Cs0Update	UINT				●
1058	Cs1Update	UINT				●
1066	Cs3Update	UINT				●
1570	Cs1UpdateFB	UINT		●		
1578	Cs3UpdateFB	UINT		●		
ADC status configuration						
1090	ZXConfig	UINT				●
1094	SagTh	UINT				●
1098	PhaseLoseTh	UINT				●
1102	INWarnTh0	UINT				●
1106	INWarnTh1	UINT				●
1110	THDNUTh	UINT				●
1114	THDNITh	UINT				●
ADC measurement configuration checksum 0						
1154	PLconstH	UINT				●
1158	PLconstL	UINT				●
1162	MeteringMode	UINT				●
ADC power calibration checksum 1						
1246	PhiA_W	UINT				●
1254	PhiB_W	UINT				●
1262	PhiC_W	UINT				●

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
ADC RMS comparison checksum 3						
1346	UGainA_W	UINT				●
1350	IGainA_W	UINT				●
1354	UoffsetA_W	INT				●
1358	IoffsetA_W	INT				●
1362	UGainB_W	UINT				●
1366	IGainB_W	UINT				●
1370	UoffsetB_W	INT				●
1374	IoffsetB_W	INT				●
1378	UGainC_W	UINT				●
1382	IGainC_W	UINT				●
1386	UoffsetC_W	INT				●
1390	IoffsetC_W	INT				●
1394	IGainN_W	UINT				●
1398	IoffsetN_W	INT				●
ADC power calibration – read						
1758	PhiA_R	UINT		●		
1766	PhiB_R	UINT		●		
1774	PhiC_R	UINT		●		
ADC RMS comparison – read						
1858	UGainA_R	UINT		●		
1862	IGainA_R	UINT		●		
1866	UoffsetA_R	INT		●		
1870	IoffsetA_R	INT		●		
1874	UGainB_R	UINT		●		
1878	IGainB_R	UINT		●		
1882	UoffsetB_R	INT		●		
1886	IoffsetB_R	INT		●		
1890	UGainC_R	UINT		●		
1894	IGainC_R	UINT		●		
1898	UoffsetC_R	INT		●		
1902	IoffsetC_R	INT		●		
1906	IGainN_R	UINT		●		
1910	IoffsetN_R	INT		●		
FlatStream interface						
2049	OutputMTU	USINT				●
2051	InputMTU	USINT				●
2055	FlatstreamMode	USINT				●
2057	Forward	USINT				●
2059	ForwardDelay	USINT				●
2113	InputSequence	USINT	●			
2113 + 2*N	RxByteN (index N = 1 to 27)	USINT	●			
2177	OutputSequence	USINT			●	
2177 + 2*N	TxByteN (index N = 1 to 15)	USINT			●	
Force analog energy registers						
2316	Frc_APenergyT	UDINT				●
2324	Frc_APenergyA	UDINT				●
2332	Frc_APenergyB	UDINT				●
2340	Frc_APenergyC	UDINT				●
2348	Frc_ANenergyT	UDINT				●
2356	Frc_ANenergyA	UDINT				●
2364	Frc_ANenergyB	UDINT				●
2372	Frc_ANenergyC	UDINT				●
2380	Frc_RPenergyT	UDINT				●
2388	Frc_RPenergyA	UDINT				●
2396	Frc_RPenergyB	UDINT				●
2404	Frc_RPenergyC	UDINT				●
2412	Frc_RNenergyT	UDINT				●
2420	Frc_RNenergyA	UDINT				●
2428	Frc_RNenergyB	UDINT				●
2436	Frc_RNenergyC	UDINT				●
2444	Frc_SAenergyT	UDINT				●
2452	Frc_SenergyA	UDINT				●
2460	Frc_SenergyB	UDINT				●
2468	Frc_SenergyC	UDINT				●
2476	Frc_SVenergyT	UDINT				●
2484	Frc_APenergyTF	UDINT				●
2492	Frc_APenergyAF	UDINT				●
2500	Frc_APenergyBF	UDINT				●
2508	Frc_APenergyCF	UDINT				●
2516	Frc_ANenergyTF	UDINT				●
2524	Frc_ANenergyAF	UDINT				●
2532	Frc_ANenergyBF	UDINT				●

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
2540	Frc_ANenergyCF	UDINT				●
2548	Frc_APenergyTH	UDINT				●
2556	Frc_APenergyAH	UDINT				●
2564	Frc_APenergyBH	UDINT				●
2572	Frc_APenergyCH	UDINT				●
2580	Frc_ANenergyTH	UDINT				●
2588	Frc_ANenergyAH	UDINT				●
2596	Frc_ANenergyBH	UDINT				●
2604	Frc_ANenergyCH	UDINT				●
Oversampling buffer						
Oversampling array[16]: Oversampling line						
6146 + ((16-N)*40)	IactN_SampleN (Index N = 1 to 16)	INT	●			
6150 + ((16-N)*40)	IactA_SampleN (Index N = 1 to 16)	INT	●			
6154 + ((16-N)*40)	UactA_SampleN (Index N = 1 to 16)	INT	●			
6158 + ((16-N)*40)	IactB_SampleN (Index N = 1 to 16)	INT	●			
6162 + ((16-N)*40)	UactB_SampleN (Index N = 1 to 16)	INT	●			
6166 + ((16-N)*40)	IactC_SampleN (Index N = 1 to 16)	INT	●			
6170 + ((16-N)*40)	UactC_SampleN (Index N = 1 to 16)	INT	●			
6773	SampleCountN	SINT	●			
6774		INT				
6778	Timestamp	INT	●			
6780		DINT				

4.3.22.11.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Standard register							
778	2	PmeanT	INT	●			
794	4	QmeanT	INT	●			
810	6	SmeanT	INT	●			
4404	8	AEnergyT	DINT	●			
4412	12	REnergyT	DINT	●			
130	0	StatusInput	UINT	●			
		CntPulseActive	Bit 0				
		CntPulseApparent	Bit 1				
		CntPulseActiveFund	Bit 2				
		CntPulseActiveHarm	Bit 3				
		ZeroCrossA	Bit 4				
		ZeroCrossB	Bit 5				
		ZeroCrossC	Bit 6				
		RBTrigDFT	Bit 8				
		RBUpdateEnergy	Bit 9				
		RBClearEnergy	Bit 10				
		RBForceEnergy	Bit 11				
194	0	ControlOutput	UINT			●	
		TrigDFT	Bit 0				
		EnabEnergy	Bit 1				
		ClearEnergy	Bit 2				
		ForceEnergy	Bit 3				
Analog status registers							
266	-	SysStatus1	UINT	●			
270	-	SysStatus2	UINT	●			
274	-	SysStatus3	UINT	●			
278	-	SysStatus4	UINT	●			
265	-	SystemStatusSel01	USINT	●			
		SumStatusPhaseLoss	Bit 2				
		SumStatusPhaseWarning	Bit 3				
		ErrOrderPhasecurrent	Bit 6				
		ErrOrderPhaseVoltage	Bit 7				
271	-	SystemStatusSel02	USINT	●			
		SumStatusWarningTHDCurrent	Bit 2				
		SumStatusWarningTHDVoltage	Bit 3				
		ErrIrmsNCalc	Bit 6				
		ErrIrmsNMeas	Bit 7				
278	-	PhaseStatus	UINT	●			
		LossPhaseC	Bit 0				
		LossPhaseB	Bit 1				
		LossPhaseA	Bit 2				
		WarningPhaseC	Bit 4				
		WarningPhaseB	Bit 5				
		WarningPhaseA	Bit 6				
Analog RMS registers							
290	-	IrmsN (measured)	UINT	●			
294	-	UrmsA	UINT	●			
298	-	UrmsB	UINT	●			
302	-	UrmsC	UINT	●			
306	-	IrmsNcalc (calculated)	UINT	●			
310	-	IrmsA	UINT	●			
314	-	IrmsB	UINT	●			
318	-	IrmsC	UINT	●			
Analog THD and angle registers							
538	-	Freq	UINT	●			
542	-	PAngleA	INT	●			
546	-	PAngleB	INT	●			
550	-	PAngleC	INT	●			
554	-	Temperature	INT	●			
558	-	UAngleA	INT	●			
562	-	UAngleB	INT	●			
564	-	UAngleC	INT	●			
Analog power registers							
778	-	PmeanT	INT	●			
782	-	PmeanA	INT	●			
786	-	PmeanB	INT	●			
790	-	PmeanC	INT	●			
794	-	QmeanT	INT	●			
798	-	QmeanA	INT	●			
802	-	QmeanB	INT	●			

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
806	-	QmeanC	INT	●			
810	-	SmeanT	INT	●			
814	-	SmeanA	INT	●			
818	-	SmeanB	INT	●			
822	-	SmeanC	INT	●			
826	-	PFmeanT	INT	●			
830	-	PFmeanA	INT	●			
834	-	PFmeanB	INT	●			
838	-	PFmeanC	INT	●			
Analog energy registers							
4108	-	APenergyT	UDINT	●			
4116	-	APenergyA	UDINT	●			
4124	-	APenergyB	UDINT	●			
4132	-	APenergyC	UDINT	●			
4140	-	ANenergyT	UDINT	●			
4148	-	ANenergyA	UDINT	●			
4156	-	ANenergyB	UDINT	●			
4164	-	ANenergyC	UDINT	●			
4172	-	RPenergyT	UDINT	●			
4180	-	RPenergyA	UDINT	●			
4188	-	RPenergyB	UDINT	●			
4196	-	RPenergyC	UDINT	●			
4204	-	RNenergyT	UDINT	●			
4212	-	RNenergyA	UDINT	●			
4220	-	RNenergyB	UDINT	●			
4228	-	RNenergyC	UDINT	●			
4236	-	SAenergyT	UDINT	●			
4244	-	SenergyA	UDINT	●			
4252	-	SenergyB	UDINT	●			
4260	-	SenergyC	UDINT	●			
4268	-	SVenergyT	UDINT	●			
4404	-	AEnergyT	DINT	●			
4412	-	REnergyT	DINT	●			
Module configuration							
1026	-	ChanControl	UINT				●
1030	-	IDispTh	UINT				●
1034	-	I_RatioA	UINT				●
1038	-	I_RatioB	UINT				●
1042	-	I_RatioC	UINT				●
1046	-	I_RatioN	UINT				●
1050	-	CfgUpdate	UINT				●
1054	-	Cs0Update	UINT				●
1058	-	Cs1Update	UINT				●
1066	-	Cs3Update	UINT				●
1570	-	Cs1UpdateFB	UINT		●		
1578	-	Cs3UpdateFB	UINT		●		
ADC status configuration							
1090	-	ZXConfig	UINT				●
1094	-	SagTh	UINT				●
1098	-	PhaseLoseTh	UINT				●
1102	-	INWarnTh0	UINT				●
1106	-	INWarnTh1	UINT				●
1110	-	THDNUTh	UINT				●
1114	-	THDNITh	UINT				●
ADC measurement configuration checksum 0							
1154	-	PLconstH	UINT				●
1158	-	PLconstL	UINT				●
1162	-	MeteringMode	UINT				●
ADC power calibration checksum 1							
1246	-	PhiA_W	UINT				●
1254	-	PhiB_W	UINT				●
1262	-	PhiC_W	UINT				●
ADC RMS comparison checksum 3							
1346	-	UGainA_W	UINT				●
1350	-	IGainA_W	UINT				●
1354	-	UoffsetA_W	INT				●
1358	-	IoffsetA_W	INT				●
1362	-	UGainB_W	UINT				●
1366	-	IGainB_W	UINT				●
1370	-	UoffsetB_W	INT				●
1374	-	IoffsetB_W	INT				●
1378	-	UGainC_W	UINT				●
1382	-	IGainC_W	UINT				●

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
1386	-	UoffsetC_W	INT				●
1390	-	IoffsetC_W	INT				●
1394	-	IGainN_W	UINT				●
1398	-	IoffsetN_W	INT				●
ADC power calibration – read							
1758	-	PhiA_R	UINT		●		
1766	-	PhiB_R	UINT		●		
1774	-	PhiC_R	UINT		●		
ADC RMS comparison – read							
1858	-	UGainA_R	UINT		●		
1862	-	IGainA_R	UINT		●		
1866	-	UoffsetA_R	INT		●		
1870	-	IoffsetA_R	INT		●		
1874	-	UGainB_R	UINT		●		
1878	-	IGainB_R	UINT		●		
1882	-	UoffsetB_R	INT		●		
1886	-	IoffsetB_R	INT		●		
1890	-	UGainC_R	UINT		●		
1894	-	IGainC_R	UINT		●		
1898	-	UoffsetC_R	INT		●		
1902	-	IoffsetC_R	INT		●		
1906	-	IGainN_R	UINT		●		
1910	-	IoffsetN_R	INT		●		
FlatStream interface							
2049	-	OutputMTU	USINT				●
2051	-	InputMTU	USINT				●
2055	-	FlatstreamMode	USINT				●
2057	-	Forward	USINT				●
2059	-	ForwardDelay	USINT				●
2113	16	InputSequence	USINT	●			
2113 + 2*N	16 + N	RxByteN (index N = 1 to 7)	USINT	●			
2177	16	OutputSequence	USINT			●	
2177 + 2*N	16 + N	TxByteN (index N = 1 to 7)	USINT			●	
Force analog energy registers							
2316	-	Frc_APenergyT	UDINT				●
2324	-	Frc_APenergyA	UDINT				●
2332	-	Frc_APenergyB	UDINT				●
2340	-	Frc_APenergyC	UDINT				●
2348	-	Frc_ANenergyT	UDINT				●
2356	-	Frc_ANenergyA	UDINT				●
2364	-	Frc_ANenergyB	UDINT				●
2372	-	Frc_ANenergyC	UDINT				●
2380	-	Frc_RPenergyT	UDINT				●
2388	-	Frc_RPenergyA	UDINT				●
2396	-	Frc_RPenergyB	UDINT				●
2404	-	Frc_RPenergyC	UDINT				●
2412	-	Frc_RNenergyT	UDINT				●
2420	-	Frc_RNenergyA	UDINT				●
2428	-	Frc_RNenergyB	UDINT				●
2436	-	Frc_RNenergyC	UDINT				●
2444	-	Frc_SAenergyT	UDINT				●
2452	-	Frc_SenergyA	UDINT				●
2460	-	Frc_SenergyB	UDINT				●
2468	-	Frc_SenergyC	UDINT				●
2476	-	Frc_SVenergyT	UDINT				●
2484	-	Frc_APenergyTF	UDINT				●
2492	-	Frc_APenergyAF	UDINT				●
2500	-	Frc_APenergyBF	UDINT				●
2508	-	Frc_APenergyCF	UDINT				●
2516	-	Frc_ANenergyTF	UDINT				●
2524	-	Frc_ANenergyAF	UDINT				●
2532	-	Frc_ANenergyBF	UDINT				●
2540	-	Frc_ANenergyCF	UDINT				●
2548	-	Frc_APenergyTH	UDINT				●
2556	-	Frc_APenergyAH	UDINT				●
2564	-	Frc_APenergyBH	UDINT				●
2572	-	Frc_APenergyCH	UDINT				●
2580	-	Frc_ANenergyTH	UDINT				●
2588	-	Frc_ANenergyAH	UDINT				●
2596	-	Frc_ANenergyBH	UDINT				●
2604	-	Frc_ANenergyCH	UDINT				●

1) The offset specifies the position of the register within the CAN object.

4.3.22.11.3.1 CAN I/O bus controller

The module occupies 3 analog logical slots on CAN-I/O.

4.3.22.11.4 General information

The modules are used for power monitoring and for a machine's energy management. Examples of where this would be used:

- Multi-phase energy measurement for class 0.5S or class 1 for
  - 3-phase, 4-line applications with neutral line (with/without grounding)
  - 3-phase, 3-line applications (with/without grounding)
  - 2-phase mains networks with grounded phase B connection
  - ARON connection
- Single-phase measurement by disabling inputs that are not needed
- Mains analysis according to harmonic content
- Signal trace by 8 kHz recording of the 3 voltage channels and 4 current channels with FIFO

4.3.22.11.4.1 Measured value preparation

The modules provide the following possibilities for measured value preparation:

- Precision of ±0.1% for real energy and ±0.2% for reactive energy
- Temperature coefficient of internal reference of 6 ppm/°C
- Error ≤±0.5% for voltage, current, active-, reactive-, apparent power, frequency active power factor and phase angle
- Energy registers for active, reactive and apparent energy, separated for forward and backward, fundamental waves and harmonics
- Threshold register for status signal generation and activation of power and energy measurement
- Determining the THD harmonic component
- Discrete Fourier Transformation (DFT) up to 31st harmonic component per phase for voltage and current
- Status signals for voltage dip, loss of voltage, phase sequence, energy flow, neutral current monitor, harmonic component monitor

4.3.22.11.4.2 Additional information

Information	Description
Measurement range monitoring	Due to the majority of registers consisting of 16 bit values (exception: energy registers, which are interpolated to 32 bit by the FW), the measurement ranges are subject to limitations, e.g. voltage 650.00 Vrms and current 65,000 Arms (after accounting for the transfer factor of the current transformer).
Extended measurement ranges	Extended measurement ranges can be achieved with the software application by upscaling the measured values.
Frozen values	Sample time register: A NetTime is assigned to the group of measured values when read from the power meter. This NetTime can be used to determine if the values have been frozen.
Environment variables	The values for duty cycle, boot counter, and minimum / maximum transformer temperature are recorded.

4.3.22.11.4.3 Measurement function

The values measured for RMS, power, active power factor, phase angle and frequency are mean values over 16 full waves, the update rate is ~3 Hz.

The following represents the measurement time over 16 full waves at the corresponding frequency:

50 Hz ... 320 ms
60 Hz ... 267 ms

Energy measurement

The power measurement (energy measurement) is based on the integration of the measured values with a sampling rate of 1 MHz.

The collected energy values are made available as energy pulses with an adjustable resolution of 0.1 CF or 0.01 CF values in the energy registers and with a resolution of 1 CF on the CF status flags.

The conversion can be defined using the PL constant. The default value 0x4A817C80 = 1.250.000.000 is equal to 360 CF/kWh or 0.1 CF/kWs. Increasing the value causes the CF amount to decrease per energy unit (e.g. 0x53D1AC10 = 1.406.250.000 is equal to 320 CF/kWh). When choosing to display the values as kWh, a resolution of 0.08789 CF/kWs is set internally and the register values are converted with a factor of 1/4096.

The energy threshold register (e.g. PStartTh) can be used to set the amount of energy needed to start an accumulation or to reset the "no load" signals in the status registers. The length of the CF pulse can vary according to the resulting output rate.

Automatic reading of the energy meter from the transformer must be enabled because valid values are only available after the transformer has been configured. It is possible to clear the energy register or to set it with a block of the register written in the software application.

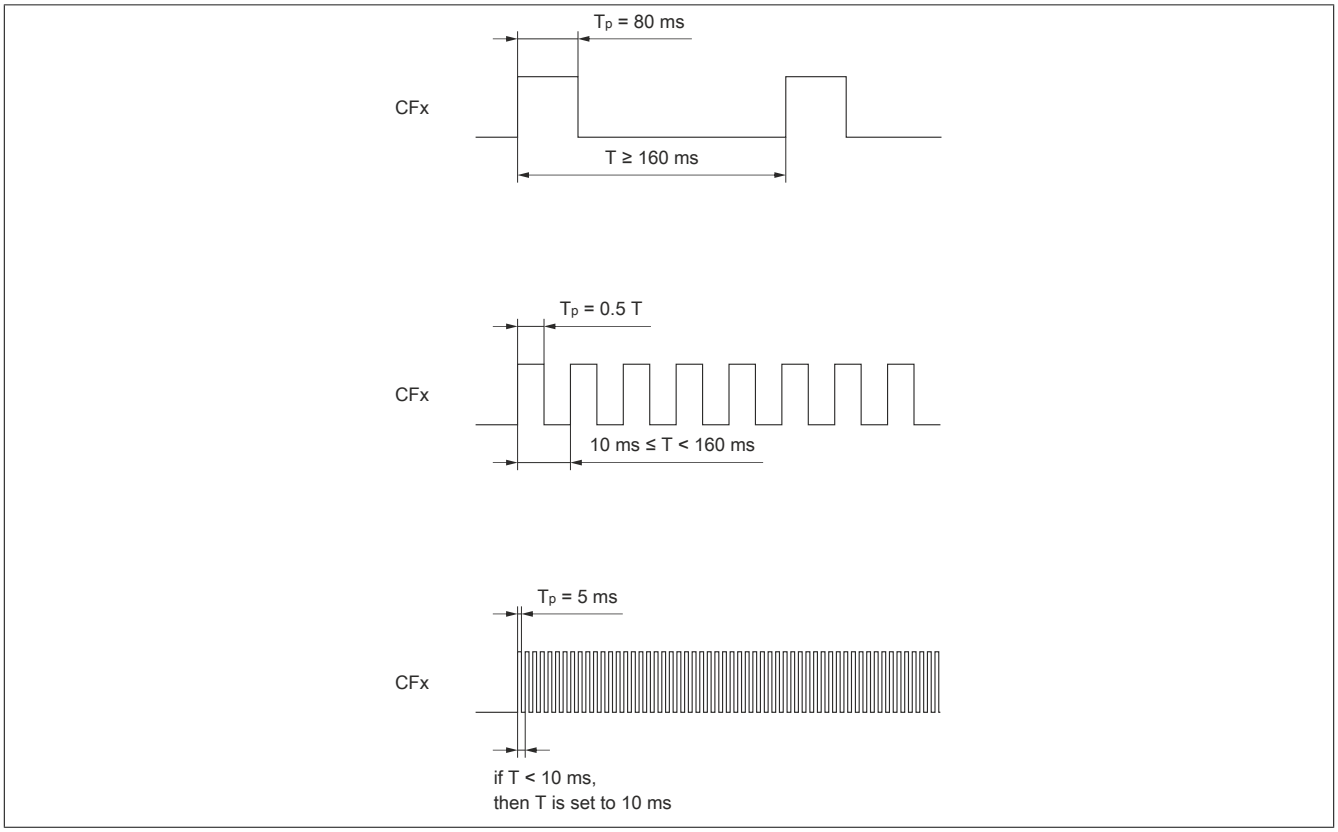


Figure 113: The length of the CF pulse can vary according to the resulting output rate

Power measurement

The phase power ratings are calculated by the module and stored in the corresponding registers.

The total power ratings are equal to the sum of the phase power ratings. To prevent the number range from being exceeded, the value in the registers is equal to a fourth of the actual power. This value must be multiplied by 4 by the application.

The vector-based total apparent power (complex total apparent power) is calculated according to IEEE1459.

Power factor

The phase power factor is calculated by dividing the phase active power by the phase apparent power.

The total power factor is calculated by dividing the total active power by the total apparent power.

Neutral current

The neutral current can be measured or calculated. Both values are available.

The user can configure which one to use for displaying the status.

Phase angle

The phase angle is calculated based on the zero-crossing detection.

Frequency

Frequency measurement is based on Phase A. If A fails, then Phase C is used. If both A and C fail, then Phase B is used.

Temperature

The Chip-Junction temperature is measured approximately every 100 ms using the sensor integrated in the transformer.

THD+N - Sum of interference power of the harmonic (THD) + interference power of the noise (N)

The THD+N measurement is used to monitor the percentage of harmonics in the network.

If this percentage falls below 10%, then an accuracy of 0.01% can no longer be guaranteed.

This is calculated as follows: (SQR (RMS_{total}^2 - $RMS_{fundamental\ wave}$^2)) / $RMS_{fundamental\ wave}$

Fourier analysis

The harmonic component from the 2nd to the 31st harmonic is calculated for voltage and current and the THD (Total Harmonic Distortion) of each phase.

The DFT period is 0.5 s. This corresponds to a resolution of 2 Hz. The input samples are recorded at a sampling rate of 8 kHz and can be optionally multiplied with a "Hann window" before being evaluated. This is initiated when requested by the application.

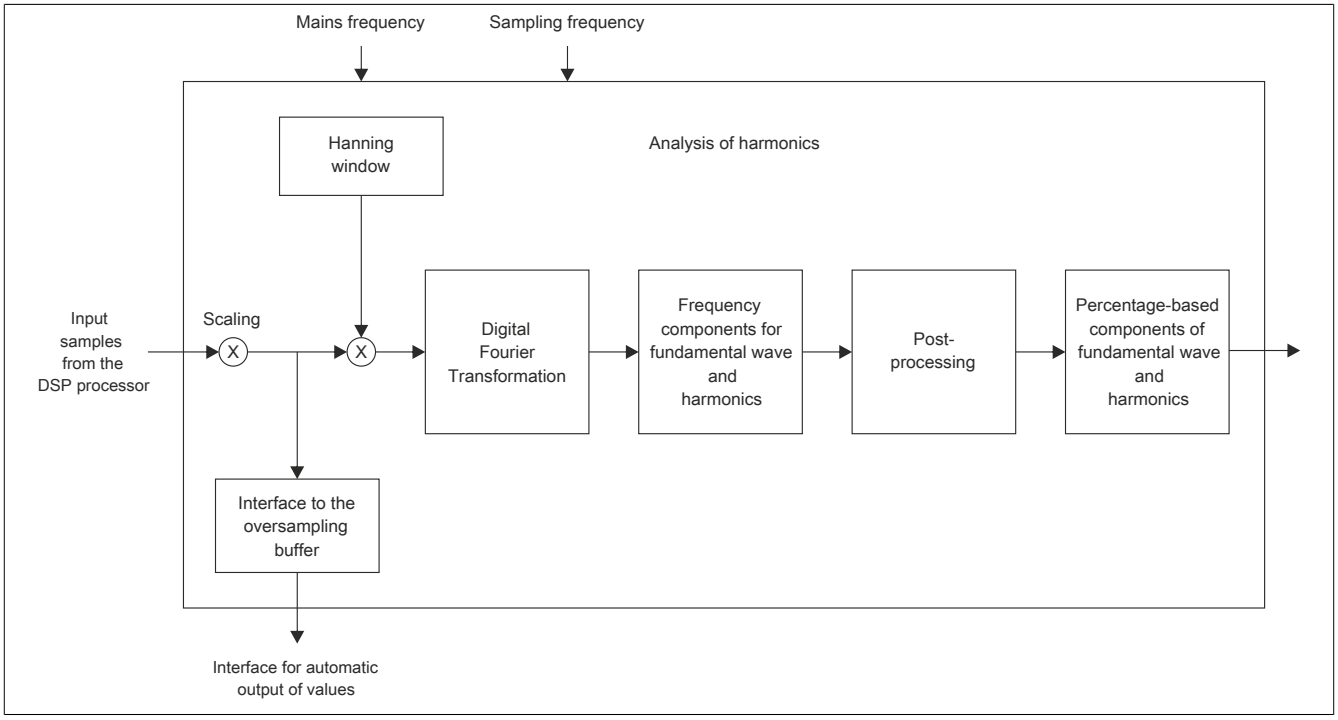


Figure 114: Diagram of Fourier analysis

4.3.22.11.4.4 Event generation

Zero-crossing detection

Zero-crossing detection can be configured for each phase for cu or voltage and edge and forms the basis for frequency and angle measurements and subsequently also for active and reactive power calculations.

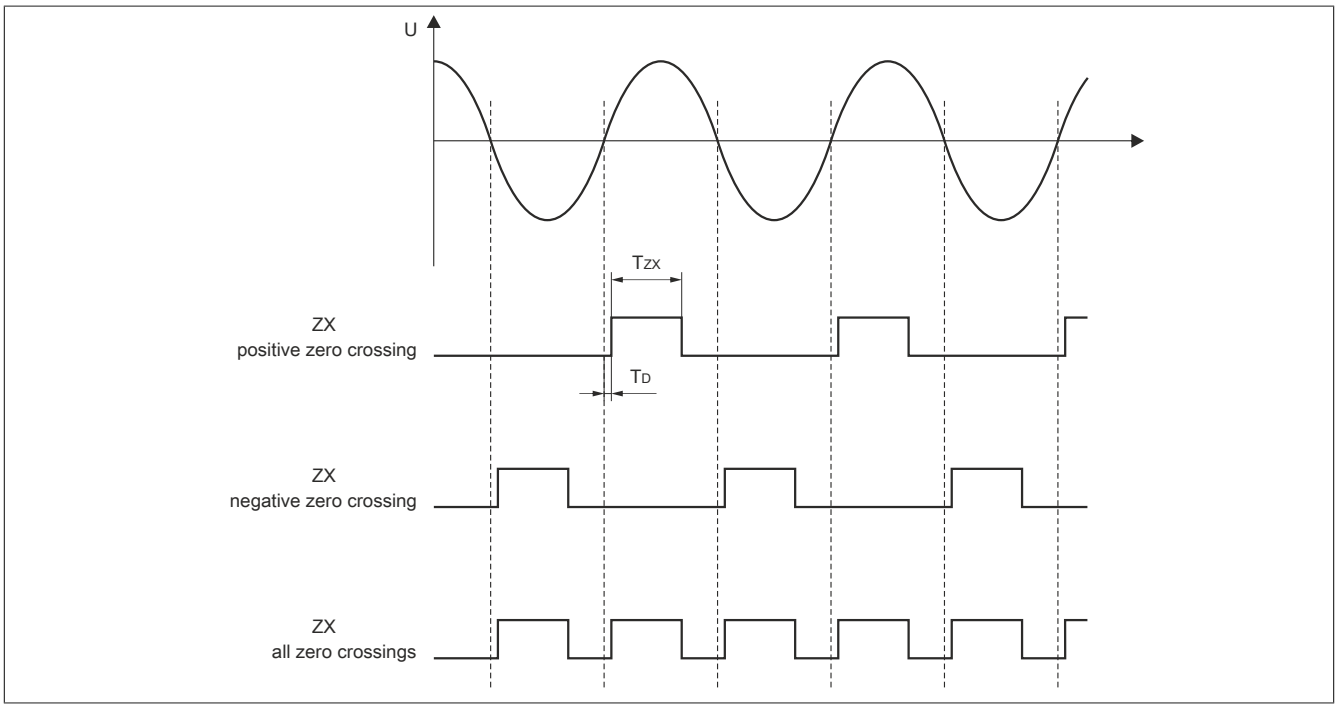


Figure 115: Time diagram of zero-crossing detection per phase

Icon	Description	Minimum	Typical	Maximum	Unit
T_{ZX}	Length of high signal		5		ms
T_D	Delay time		0.2	0.5	ms

Table 72: Specification of zero-crossing detection

Detection of voltage dip or power failure

Event	Description
Voltage dip	The threshold for voltage dips is typically set to 78% of the standard voltage (approx. 170 Vrms). The status flag is set if more than three 8 kHz samples are below the threshold value within 2 consecutive 11 ms windows.
Power failure	The threshold for voltage dips is typically set to 10% of the standard voltage (approx. 22 Vrms). The status flag is set if more than three 8 kHz samples are below the threshold value within 2 consecutive 11 ms windows. If a power failure is detected, then zero-crossing detection is disabled for voltage and current for this phase.

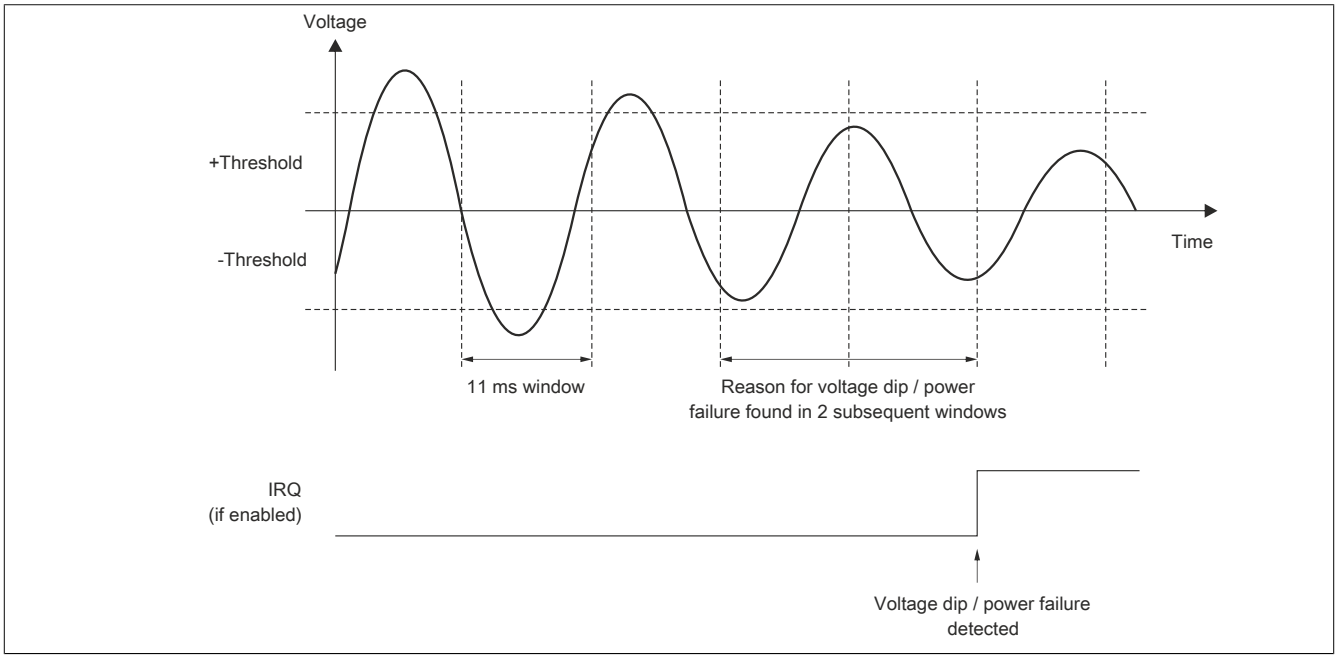


Figure 116: Time diagram for detecting a voltage dip or power failure

Neutral current monitoring

Neutral current monitoring of the measured and the calculated value is done with separate threshold value registers and status flags.

Phase sequence monitoring

3 phase and 2 phase applications are handled differently:

Application	Description
3 phases	Zero cross-overs of voltage and current must follow the sequence Phase A before Phase B before Phase C
2 phases	Zero cross-overs of voltage and current must follow the sequence Phase A at least 180° before Phase C

Table 73: Phase sequence monitoring according to the application

4.3.22.11.4.5 Configuration registers

The configuration and calibration registers are each composed of blocks and employ a checksum feature to highlight undesired changes. In order to apply this register to the transformer, the respective transfer register must be changed after the data is transferred to the module (incrementing, bit toggling, etc.). The start value of the transfer register is 0 after startup.

4.3.22.11.5 Interface for transferring process variable mapping

Due to the amount of potential cyclic input data and the limitation to 30 byte cyclic X2X data, the extended Flat Stream interface, DPS = Data Point Stream, has been defined as the mechanism for transferring the process variables. DPS is based on the Flat Streaming Interface (FSI) for serial interface modules. The FSI was expanded to include the block number as the first byte of the user data frame and implements the termination of a frame (data image of the channel) with a zero segment.

The data blocks are re-transferred if a read request is triggered after a transfer has been completed. A block number can be sent via the DPS to set a different block or transfer the entire image (default: block number 0).

It should be possible to adapt the DPS interface to the available buffer size. However, the higher-level fieldbus must be taken into account when doing so (e.g.: CAN 8 byte object, InputMTU size 7). The block number is added to the front of the actual payload data as a means to differentiate the blocks.

```
#define ADC_BLK_ALL        0   // struct ADC_REG
#define ADC_BLK_STATUS     1   // long NetTimeReg + struct ADC_REG_STATUS
#define ADC_BLK_RMS        2   // struct ADC_REG_RMS
#define ADC_BLK_POWER      3   // struct ADC_REG_POWER
#define ADC_BLK_THD_ANGLE  4   // struct THD_ANGLE
#define ADC_BLK_ENERGY     5   // long NetTimeEnergy + struct ADC_REG_ENERGY
#define ADC_BLK_DFT        6   // long NetTimeDft + struct ADC_REG_DFT
#define ADC_BLK_CFGACT     7   // struct ADC_REG_CFGACT
#define ADC_BLK_ENVREG     8   // struct ENV_STATUS
```

Information:

- **Consistency of the data is only provided for the individual variables because the data is transferred from the AD converter asynchronously to the conversion.**
- **Make sure that the byte sequence of the register is in accordance with the Little Endian model (Intel format).**

The NetTime timestamps are always updated after the blocks are generated when preparing a new alternating buffer.

4.3.22.11.5.1 Data block structure

ADC_REG

```
typedef struct ADC_REG     ADC_REG;
struct ADC_REG
{
 long              NetTimeReg;  // Time of Section copy to Buffer
 ADC_REG_STATUS    Status;      // Status registers
 ADC_REG_RMS       Rms;         // RMS Registers
 ADC_REG_POWER     Power;       // Power Registers
 ADC_REG_THD_ANGLE ThdAngle;    // THD + Angle Registers

// Regular Energy Registers
 long            NetTimeEnergy; // Time of Section copy to Buffer
 ADC_REG_ENERGY  Energy;        // Energy Registers

 long            NetTimeDft;    // Time of Section copy to Buffer
 ADC_REG_DFT     Dft;           // DFT Registers
// Read Back selected CFG Registers
  ADC_REG_CFGACT  CfgAct;       // Config read back
// Read Back Environment Registers
  ENV_STATUS      EnvReg;
};
```

ADC_REG_STATUS

```
typedef struct ADC_REG_STATUS  ADC_REG_STATUS;
struct ADC_REG_STATUS
{
  unsigned short SysStatus0;   // System Status 0
  unsigned short SysStatus1;   // System Status 1
  unsigned short EnStatus0;    // Metering Status 0
  unsigned short EnStatus1;    // Metering Status 1
};
```

ADC_REG_RMS

```
typedef struct ADC_REG_RMS  ADC_REG_RMS;
struct ADC_REG_RMS
{
  unsigned short IrmsN1;   // N Line Sampled current RMS
  unsigned short UrmsA;    // phase A voltage RMS
  unsigned short UrmsB;    // phase B voltage RMS
  unsigned short UrmsC;    // phase C voltage RMS
  unsigned short IrmsN0;   // N Line calculated current RMS
  unsigned short IrmsA;    // phase A voltage RMS
  unsigned short IrmsB;    // phase B voltage RMS
  unsigned short IrmsC;    // phase C voltage RMS
};
```

ADC_REG_POWER

```
typedef struct ADC_REG_POWER  ADC_REG_POWER;
struct ADC_REG_POWER
{
  unsigned short SVmeanTLSB;  // LSB of (Vector Sum) Total Apparent Power
  unsigned short SVmeanT;     // (Vector Sum) Total Apparent Power

  // Power and Power Factor Register
  signed short PmeanT;   // Total Active Power
  signed short PmeanA;   // Phase A Active Power
  signed short PmeanB;   // Phase B Active Power
  signed short PmeanC;   // Phase C Active Power
  signed short QmeanT;   // Total Reactive Power
  signed short QmeanA;   // Phase A Reactive Power
  signed short QmeanB;   // Phase B Reactive Power
  signed short QmeanC;   // Phase C Reactive Power
  signed short SAmeanT;  // (Arithmetic Sum) Total apparent power
  signed short SmeanA;   // phase A apparent power
  signed short SmeanB;   // phase B apparent power
  signed short SmeanC;   // phase C apparent power
  signed short PFmeanT;  // Total power factor
  signed short PFmeanA;  // phase A power factor
  signed short PFmeanB;  // phase A power factor
  signed short PFmeanC;  // phase A power factor

  // Fundamental/ Harmonic Power and Voltage/ Current RMS Registers
  signed short PmeanTF;  // Total active fundamental power
  signed short PmeanAF;  // phase A active fundamental power
  signed short PmeanBF;  // phase B active fundamental power
  signed short PmeanCF;  // phase C active fundamental power
  signed short PmeanTH;  // Total active harmonic power
  signed short PmeanAH;  // phase A active harmonic power
  signed short PmeanBH;  // phase B active harmonic power
  signed short PmeanCH;  // phase C active harmonic power
};
```

ADC_REG_THD_ANGLE

```
typedef struct ADC_REG_THD_ANGLE  ADC_REG_THD_ANGLE;
struct ADC_REG_THD_ANGLE
{
  // THD+N, Frequency, Angle and Temperature Registers
  unsigned short THDNUA;    // phase A voltage THD+N
  unsigned short THDNUB;    // phase B voltage THD+N
  unsigned short THDNUC;    // phase C voltage THD+N
  unsigned short THDNIA;    // phase A current THD+N
  unsigned short THDNIB;    // phase B current THD+N
  unsigned short THDNIC;    // phase C current THD+N
  unsigned short Freq;      // Frequency
  signed short     PAngleA;   // phase A mean phase angle
  signed short     PAngleB;   // phase B mean phase angle
  signed short     PAngleC;   // phase C mean phase angle
  signed short     Temp;      // Measured temperature
  signed short     UangleA;   // phase A voltage phase angle
  signed short     UangleB;   // phase B voltage phase angle
  signed short     UangleC;   // phase C voltage phase angle
};
```

ADC_REG_ENERGY

```
typedef struct ADC_REG_ENERGY  ADC_REG_ENERGY;
struct ADC_REG_ENERGY
{
  unsigned long APenergyT;   // Total Forward Active Energy
  unsigned long APenergyA;   // Phase A Forward Active Energy
  unsigned long APenergyB;   // Phase B Forward Active Energy
  unsigned long APenergyC;   // Phase C Forward Active Energy
  unsigned long ANenergyT;   // Total Reverse Active Energy
  unsigned long ANenergyA;   // Phase A Reverse Active Energy
  unsigned long ANenergyB;   // Phase B Reverse Active Energy
  unsigned long ANenergyC;   // Phase C Reverse Active Energy
  unsigned long RPenergyT;   // Total Forward Reactive Energy
  unsigned long RPenergyA;   // Phase A Forward Reactive Energy
  unsigned long RPenergyB;   // Phase B Forward Reactive Energy
  unsigned long RPenergyC;   // Phase C Forward Reactive Energy
  unsigned long RNenergyT;   // Total Reverse Reactive Energy
  unsigned long RNenergyA;   // Phase A Reverse Reactive Energy
  unsigned long RNenergyB;   // Phase B Reverse Reactive Energy
  unsigned long RNenergyC;   // Phase C Reverse Reactive Energy
  unsigned long SAenergyT;   // (Arithmetic Sum) Total Apparent Energy
  unsigned long SenergyA;    // Phase A Apparent Energy
  unsigned long SenergyB;    // Phase B Apparent Energy
  unsigned long SenergyC;    // Phase C Apparent Energy
  unsigned long SVenergyT;   // (Vector Sum) Total Apparent Energy

  // Fundamental / Harmonic Energy Register
  unsigned long APenergyTF;  // Total Forward Active Fundamental Energy
  unsigned long APenergyAF;  // Phase A Forward Active Fundamental Energy
  unsigned long APenergyBF;  // Phase B Forward Active Fundamental Energy
  unsigned long APenergyCF;  // Phase C Forward Active Fundamental Energy
  unsigned long ANenergyTF;  // Total Reverse Active Fundamental Energy
  unsigned long ANenergyAF;  // Phase A Reverse Active Fundamental Energy
  unsigned long ANenergyBF;  // Phase B Reverse Active Fundamental Energy
  unsigned long ANenergyCF;  // Phase C Reverse Active Fundamental Energy
  unsigned long APenergyTH;  // Total Forward Active Harmonic Energy
  unsigned long APenergyAH;  // Phase A Forward Active Harmonic Energy
  unsigned long APenergyBH;  // Phase B Forward Active Harmonic Energy
  unsigned long APenergyCH;  // Phase C Forward Active Harmonic Energy
  unsigned long ANenergyTH;  // Total Reverse Active Harmonic Energy
  unsigned long ANenergyAH;  // Phase A Reverse Active Harmonic Energy
  unsigned long ANenergyBH;  // Phase B Reverse Active Harmonic Energy
  unsigned long ANenergyCH;  // Phase C Reverse Active Harmonic Energy

  signed long AEnergyT;   // Total Active Energy
  signed long REnergyT;   // Total Reactive Energy
};
```

ADC_REG_DFT

```
typedef struct ADC_REG_DFT  ADC_REG_DFT;
struct ADC_REG_DFT
{
  // Arithmetic ratio, 2 bits integer and 14 bits fractional;
  // That is: Harmonic Ratio (%) = Register Value / 163.84
  unsigned short DftAI[32];  // phase A, Current, Harmonic Ratio for 2nd to 32nd
                             // order componentand Total Harmonic Distortion Ratio
  unsigned short DftBI[32];  // phase B, Current, Harmonic Ratio for 2nd to 32nd
                             // order componentand Total Harmonic Distortion Ratio
  unsigned short DftCI[32];  // phase C, Current, Harmonic Ratio for 2nd to 32nd
                             // order componentand Total Harmonic Distortion Ratio
  unsigned short DftAV[32];  // phase A, Voltage, Harmonic Ratio for 2nd to 32nd
                             // order componentand Total Harmonic Distortion Ratio
  unsigned short DftBV[32];  // phase B, Voltage, Harmonic Ratio for 2nd to 32nd
                             // order componentand Total Harmonic Distortion Ratio
  unsigned short DftCV[32];  // phase C, Voltage, Harmonic Ratio for 2nd to 32nd
                             // order componentand Total Harmonic Distortion Ratio

  // Format: Need special scaling/conversion.
  //The register value * 147.62 = full-scale input signal RMS.
  // Current, Fundamental component value = Register Value * 209 * 65.535 / 8388608
  // Voltage, Fundamental component value = Register Value * 209 * 655.35 / 8388608

  unsigned short DftAI_Fund;
  unsigned short DftAV_Fund;
  unsigned short DftBI_Fund;
  unsigned short DftBV_Fund;
  unsigned short DftCI_Fund;
  unsigned short DftCV_Fund;
};

// Excerpt of configuration registers used by APROL, readable only by FS-IF
// and with register numbers of registers with the same names.

typedef struct ADC_REG_CFGACT ADC_REG_CFGACT;
struct ADC_REG_CFGACT
{
  unsigned short ChanControl;
  unsigned short IDispTh;
  unsigned short I_RatioA;
  unsigned short I_RatioB;
  unsigned short I_RatioC;
  unsigned short I_RatioN;
  unsigned short ZXConfig;
  unsigned short SagTh;
  unsigned short PhaseLoseTh;
  unsigned short INWarnTh0;
  unsigned short INWarnTh1;
  unsigned short THDNUTh;
  unsigned short THDNITh;
  unsigned short MeteringMode;
  unsigned short PLconstL;
  unsigned short PLconstH;
};

// Environment Variables

typedef struct ENV_STATUS ENV_STATUS;
struct ENV_STATUS
{
  unsigned long  ulUpTime;
  unsigned long  ulUpCnt;
  signed short   ssMinTemp;
  signed short   ssMaxTemp;
  unsigned long  ulRes[13];
};
```

4.3.22.11.6 Standard register

4.3.22.11.6.1 Total active power

Name:
PmeanT

The value in the register equals a fourth of the actual power. The calculation can be performed in either absolute or arithmetic mode (see register "MeteringMode" <Bit 3>). Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 4 W

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total active power = Register value * 4

4.3.22.11.6.2 Total reactive power

Name:
QmeanT

The value in the register equals a fourth of the actual power. The calculation can be performed in either absolute or arithmetic mode (see register "MeteringMode" <Bit 4>). Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 4 var

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total reactive power = Register value * 4

4.3.22.11.6.3 Total apparent power

Name:
SmeanT

The value in the register equals a fourth of the actual power. The power is calculated in arithmetic mode. Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	0 to 32767	Resolution 4 VA

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total apparent power = Register value * 4

4.3.22.11.6.4 Total active energy combined

Name:
AEnergyT

Total active energy in forward and backward direction.

Data type	Value	
DINT	-2,147,483,647 to 2,147,483,647	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Internal calculation formula for the total active energy:

AEnergyT = (DINT)(APenergyT - ANenergyT) ... Calculation overflows must be handled in the application

4.3.22.11.6.5 Total reactive energy combined

Name:
REnergyT

Total reactive energy in forward and backward direction.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Internal calculation formula for the total reactive energy:

REnergyT = (DINT)(RPenergyT - RNenergyT) ... Calculation overflows must be handled in the application

4.3.22.11.6.6 Status signals and responses

Name:
StatusInput

The signals are recorded in 200 µs intervals.

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	CF1 energy pulse 1, total active energy	0	Not yet calculated
		1	Calculated
1	CF2 energy pulse 2, total apparent energy, configurable Standard: Arithmetic sum of apparent energy, can be reconfigured via register <MeteringMode>	0	Not yet calculated
		1	Calculated
2	CF3 energy pulse 3, total active energy, fundamental wave	0	Not yet calculated
		1	Calculated
3	CF4 energy pulse 4, total active energy, harmonics	0	Not yet calculated
		1	Calculated
4	ZX1 zero cross signal – Phase A	0	Zero cross-over not detected
		1	Standard: Pulse at positive edge of the zero cross signal of the voltage input, can be reconfigured via register "ZXConfig"
5	ZX2 zero cross signal – Phase B	0	Zero cross-over not detected
		1	Standard: Pulse at positive edge of the zero cross signal of the voltage input, can be reconfigured via register "ZXConfig"
6	ZX3 zero cross signal – Phase C	0	Zero cross-over not detected
		1	Standard: Pulse at positive edge of the zero cross signal of the voltage input, can be reconfigured via register "ZXConfig"
7	Reserved	0	
8	DFT response sent	x	If the state in the register "ControlOutput" corresponds with the response, then the action is complete
9	Energy value update response sent	0	No update
		1	Update complete
10	Energy value response deleted	x	If the state in the register "ControlOutput" corresponds with the response, then the action is complete
11	Energy value response set	x	If the state in the register "ControlOutput" corresponds with the response, then the action is complete
12 - 15	Reserved	0	

4.3.22.11.6.7 Control signals

Name:
ControlOutput

Control signals are evaluated in a ~5 ms interval.

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	DFT analysis	0	Don't start
		1	Start[1)]
1	Automatically read energy values	0	Do not automatically read
		1	Automatically read
2	Clear energy values	0	Don't delete
		1	Delete[1)]
3	Set energy values	0	Don't start
		1	Start[1)]
4 - 15	Reserved	0	

1) If the state in the register "ControlOutput" corresponds with the response, then the action is complete.

4.3.22.11.7 Analog status registers

4.3.22.11.7.1 Read timestamp for I/O register (+0x0022 = 16 bit)

Name:
SampleTime01_32bit

Network timestamp for the readout of the status, RMS, power register.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	Network time

4.3.22.11.7.2 ADC system status 1

Name:
SysStatus1

The register is read by the converter in a ~5 ms interval.

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	SumStatusPhaseLoss, voltage of one or more phases < failure threshold in the register	0	Voltage within permitted range
		1	Voltage lower than the failure threshold
3	SumStatusPhaseWarning, voltage of one or more phases < warning threshold in the register	0	Voltage within permitted range
		1	Voltage lower than the warning threshold
4 - 5	Reserved	0	
6	ErrOrderPhasecurrent, error in the order of phase currents	0	No error
		1	Error
7	ErrOrderPhaseVoltage, error in the order of phase voltages	0	No error
		1	Error
8	CS3Err, checksum error in configuration block 3	0	No error
		1	Error
9	Reserved	0	
10	CS2Err, checksum error in configuration block 2	0	No error
		1	Error
11	Reserved	0	
12	CS1Err, checksum error in configuration block 1	0	No error
		1	Error
13	Reserved	0	
14	CS0Err, checksum error in configuration block 0	0	No error
		1	Error
15	Reserved	0	

4.3.22.11.7.3 ADC system status 2

Name:
SysStatus2

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	RevPchgC, the direction of the active energy for phase C has changed	0	No change of direction
		1	Direction has changed
1	RevPchgB, the direction of the active energy for phase B has changed	0	No change of direction
		1	Direction has changed
2	RevPchgA, the direction of the active energy for phase A has changed	0	No change of direction
		1	Direction has changed
3	RevPchgT, the direction of the active energy for the total has changed	0	No change of direction
		1	Direction has changed
4	RevQchgC, the direction of the reactive energy for phase C has changed	0	No change of direction
		1	Direction has changed
5	RevQchgB, the direction of the reactive energy for phase B has changed	0	No change of direction
		1	Direction has changed
6	RevQchgA, the direction of the reactive energy for phase A has changed	0	No change of direction
		1	Direction has changed
7	RevQchgT, the direction of the reactive energy for the total has changed	0	No change of direction
		1	Direction has changed
8	Reserved	0	
9	DFTDone, DFT analysis complete (temporary bit)	0	DFT analysis not complete
		1	DFT analysis complete
10	SumStatusWarningTHDCurrent, the THDIx value of one or more phases > warning threshold in the register	0	THDIx value within permitted range
		1	THDIx value higher than warning threshold
11	SumStatusWarningTHDVoltage, the THDUx value of one or more phases > warning threshold in the register	0	THDUx value within permitted range
		1	THDUx value higher than warning threshold
12 - 13	Reserved	0	
14	ErrIrmsNCalc, the calculated value of the neutral line > warning threshold in the Register	0	Calculated value within permitted range
		1	Calculated value higher than warning threshold
15	ErrIrmsNMeas, the measured value of the neutral line > warning threshold in the Register	0	Measured value within permitted range
		1	Measured value higher than warning threshold

4.3.22.11.7.4 ADC system status 3

Name:
SysStatus3

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	CF1RevFlag, direction of CF signal	0	Forward[1)]
		1	Back[2)]
1	CF2RevFlag, direction of CF signal	0	Forward[1)]
		1	Back[2)]
2	CF3RevFlag, direction of CF signal	0	Forward[1)]
		1	Back[2)]
3	CF4RevFlag, direction of CF signal	0	Forward[1)]
		1	Back[2)]
4 - 11	Reserved	0	
12	TVSNoload, vector-based total apparent power of all phases in "No load" state	0	Status with load
		1	Status without load
13	TASNoload, total apparent power of all phases in "No load" state	0	Status with load
		1	Status without load
14	TPNoload, total active power of all phases in "No load" state	0	Status with load
		1	Status without load
15	TQNoload, total reactive power of all phases in "No load" state	0	Status with load
		1	Status without load

1) Forward direction of CF pulse (positive sign of corresponding energy register)
2) Reverse direction of CF pulse (negative sign of corresponding energy register)

4.3.22.11.7.5 ADC system status 4

Name:
SysStatus4

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	LossPhaseC, voltage lower than value in the register "PhaseLoseTh"	0	Voltage is higher
		1	Voltage is lower
1	LossPhaseB, voltage lower than value in the register "PhaseLoseTh"	0	Voltage is higher
		1	Voltage is lower
2	LossPhaseA, voltage lower than value in the register "PhaseLoseTh"	0	Voltage is higher
		1	Voltage is lower
3	Reserved	0	
4	WarningPhaseC, voltage lower than value in the register "SagTh"	0	Voltage is higher
		1	Voltage is lower
5	WarningPhaseB, voltage lower than value in the register "SagTh"	0	Voltage is higher
		1	Voltage is lower
6	WarningPhaseA, voltage lower than value in the register "SagTh"	0	Voltage is higher
		1	Voltage is lower
7 - 15	Reserved	0	

4.3.22.11.7.6 ADC system status 1

Name:
SystemStatusSel01

The most important bits of the "SysStatus1" register are stored in this register.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	SumStatusPhaseLoss, voltage of one or more phases < failure threshold in the register	0	Voltage within permitted range
		1	Voltage lower than the failure threshold
3	SumStatusPhaseWarning, voltage of one or more phases < warning threshold in the register	0	Voltage within permitted range
		1	Voltage lower than the warning threshold
4 - 5	Reserved	0	
6	ErrOrderPhasecurrent, error in the order of phase currents	0	No error
		1	Error
7	ErrOrderPhaseVoltage, error in the order of phase voltages	0	No error
		1	Error

4.3.22.11.7.7 ADC system status 2

Name:
SystemStatusSel02

The most important bits of the "SysStatus2" register are stored in this register.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	SumStatusWarningTHDCurrent, the THDIx value of one or more phases > warning threshold in the register	0	THDIx value within permitted range
		1	THDIx value higher than warning threshold
3	SumStatusWarningTHDVoltage, the THDUx value of one or more phases > warning threshold in the register	0	THDUx value within permitted range
		1	THDUx value higher than warning threshold
4 - 5	Reserved	0	
6	ErrIrmsNCalc, the calculated value of the neutral line > warning threshold in the Register	0	Calculated value within permitted range
		1	Calculated value higher than warning threshold
7	ErrIrmsNMeas, the measured value of the neutral line > warning threshold in the Register	0	Measured value within permitted range
		1	Measured value higher than warning threshold

4.3.22.11.7.8 Phase status

Name:
PhaseStatus

This register corresponds to the SysStatus4 register. It contains the status of phases A, B und C.

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	LossPhaseC, voltage lower than value in the register "PhaseLoseTh"	0	Voltage is higher
		1	Voltage is lower
1	LossPhaseB, voltage lower than value in the register "PhaseLoseTh"	0	Voltage is higher
		1	Voltage is lower
2	LossPhaseA, voltage lower than value in the register "PhaseLoseTh"	0	Voltage is higher
		1	Voltage is lower
3	Reserved	0	
4	WarningPhaseC, voltage lower than value in the register "SagTh"	0	Voltage is higher
		1	Voltage is lower
5	WarningPhaseB, voltage lower than value in the register "SagTh"	0	Voltage is higher
		1	Voltage is lower
6	WarningPhaseA, voltage lower than value in the register "SagTh"	0	Voltage is higher
		1	Voltage is lower
7 - 15	Reserved	0	

4.3.22.11.8 Analog RMS registers

4.3.22.11.8.1 Current RMS neutral line measured

Name:
IrmsN

Measured value of the neutral current between the P and N connections on the current terminal, multiplied with the transfer factor of the transformer.

Data type	Value	Information
UINT	0 to 65,535	Measured value 0.001 Arms

4.3.22.11.8.2 Voltage RMS phase A/B/C

Name:
UrmsA
UrmsB
UrmsC

Measured value for N-terminal or virtual zero point.

Data type	Value	Information
UINT	0 to 65,535	Measured value 0.01 Vrms

4.3.22.11.8.3 Current RMS neutral line calculated

Name:
IrmsNcalc

Calculated value of neutral current derived from the other 3 phases.

Data type	Value	Information
UINT	0 to 65,535	Measured value 0.001 Arms

4.3.22.11.8.4 Current RMS phase A/B/C

Name:
IrmsA
IrmsB
IrmsC

Measured value of the phase current between the P and N connections on the current terminal, multiplied with the transfer factor of the transformer.

Data type	Value	Information
UINT	0 to 65,535	Measured value 0.001 Arms

4.3.22.11.9 Analog THD and angle registers

4.3.22.11.9.1 THD+N value voltage phase A/B/C

Name:
THDNUA
THDNUB
THDNUC

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01%

Harmonic content = (SQR(Rms_{total}^2 - $Rms_{fundamental}$^2))/$Rms_{fundamental}$

4.3.22.11.9.2 THD+N value current phase A/B/C

Name:
THDNIA
THDNIB
THDNIC

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01%

Harmonic content = (SQR(Rms_{total}^2 - $Rms_{fundamental}$^2))/$Rms_{fundamental}$

4.3.22.11.9.3 Fundamental frequency measured

Name:
Freq

Measured fundamental frequency of phases A, B and C.

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01 Hz

4.3.22.11.9.4 Phase angle of power on phase A/B/C

Name:
PAngleA
PAngleB
PAngleC

Middle phase angle (power angle) of the current to the voltage based on the zero-crossing detection.

Data type	Value	Information
INT	-1800 to 1800	Resolution 0.1°

4.3.22.11.9.5 Transformer temperature

Name:
Temperature

This register contains the internal temperature of the transformer component. The temperature is recorded in a 100 ms interval.

Data type	Value	Information
INT	-200 to 200	Resolution 1°C

4.3.22.11.9.6 Phase angle of voltage on phase A/B/C

Name:
UAngleA
UAngleB
UAngleC

The value for phase A is always 0. On the other phases, the angle corresponds with the offset to A. This is based on the zero-crossing detection.

Data type	Value	Information
INT	-1800 to 1800	Resolution 0.1°

4.3.22.11.10 Analog power register

4.3.22.11.10.1 Vector sum of the total apparent power LSW

Name:
SVmeanTLSB

The value in the register equals a fourth of the actual power.

Data type	Value	Information
INT	-32,767 to 32,767	Resolution of units/LSB equals 4/65536 VA

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual vector sum of the total apparent power LSW = register value * 4 (complex sum)

4.3.22.11.10.2 Vector sum of the total apparent power MSW

Name:
SVmeanT

The value in the register equals a fourth of the actual power. The calculation is made in accordance with IEEE 1459.

Data type	Value	Information
INT	0 to 32767	Resolution 4 VA

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual vector sum of the total apparent power MSW = register value * 4 (complex sum)

4.3.22.11.10.3 Total active power

Name:
PmeanT

The value in the register equals a fourth of the actual power. The calculation can be performed in either absolute or arithmetic mode (see register "MeteringMode" <Bit 3>). Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 4 W

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total active power = Register value * 4

4.3.22.11.10.4 Active power on phase A/B/C

Name:
PmeanA
PmeanB
PmeanC

Active power on the phase. Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 1 W

4.3.22.11.10.5 Total reactive power

Name:
QmeanT

The value in the register equals a fourth of the actual power. The calculation can be performed in either absolute or arithmetic mode (see register "MeteringMode" <Bit 4>). Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 4 var

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total reactive power = Register value * 4

4.3.22.11.10.6 Reactive power on phase A/B/C

Name:
QmeanA
QmeanB
QmeanC

Reactive power on the phase. Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 1 var

4.3.22.11.10.7 Total apparent power

Name:
SmeanT

The value in the register equals a fourth of the actual power. The power is calculated in arithmetic mode. Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	0 to 32767	Resolution 4 VA

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total apparent power = Register value * 4

4.3.22.11.10.8 Apparent power on phase A/B/C

Name:
SmeanA
SmeanB
SmeanC

Apparent power on the phase. Each phase can be separately enabled for the power calculation (see register "MeteringMode" <Bits 0, 1 and 2>).

Data type	Value	Information
INT	0 to 32767	Resolution 1 VA

4.3.22.11.10.9 Total power factor

Name:
PFmeanT

Data type	Value	Information
INT	-1000 to 1000	Resolution 0.001

4.3.22.11.10.10 Power factor on phase A/B/C

Name:
PFmeanA
PFmeanB
PFmeanC

Data type	Value	Information
INT	-1000 to 1000	Resolution 0.001

4.3.22.11.10.11 Total active power of fundamental wave

Name:
PmeanTF

The value in the register equals a fourth of the actual power.

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 4 W

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total active power of fundamental wave = Register value * 4

4.3.22.11.10.12 Fundamental wave active power on phase A/B/C

Name:
PmeanAF
PmeanBF
PmeanCF

Active power of fundamental wave on the phase.

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 1 W

4.3.22.11.10.13 Total active power of harmonics

Name:
PmeanTH

The value in the register equals a fourth of the actual power.

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 4 W

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total active power of harmonics = Register value * 4

4.3.22.11.10.14 Harmonics active power on phase A/B/C

Name:
PmeanAH
PmeanBH
PmeanCH

Active power of harmonics on the phase.

Data type	Value	Information
INT	-32,767 to 32,767	Resolution 1 W

4.3.22.11.11 Analog energy registers

4.3.22.11.11.1 Read timestamp for energy registers (+0x0022 = 16 bit)

Name:
SampleTime02_32bit

Network timestamp for the readout of the energy register.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	Network time

4.3.22.11.11.2 Forward total active energy

Name:
APenergyT

Total active energy in forward direction.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.3 Forward active energy on phase A/B/C

Name:
APenergyA
APenergyB
APenergyC

Active energy in forward direction of the phase.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.4 Reverse total active energy

Name:
ANenergyT

Total active energy in reverse direction.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.5 Reverse active energy on phase A/B/C

Name:
ANenergyA
ANenergyB
ANenergyC

Active energy in reverse direction of the phase.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.6 Forward total reactive energy

Name:
RPenergyT

Total reactive energy in forward direction.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.7 Forward reactive energy on phase A/B/C

Name:
RPenergyA
RPenergyB
RPenergyC

Reactive energy in forward direction of the phase.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.8 Reverse total reactive energy

Name:
RNenergyT

Total reactive energy in reverse direction.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.9 Reverse reactive energy on phase A/B/C

Name:
RNenergyA
RNenergyB
RNenergyC

Reactive energy in reverse direction of the phase.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.10 Arithmetic total apparent energy

Name:
SAenergyT

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.11 Apparent energy on phase A/B/C

Name:
SenergyA
SenergyB
SenergyC

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.12 Vectorized total apparent energy

Name:
SVenergyT

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.13 Forward fundamental wave total active energy

Name:
APenergyTF

Fundamental wave of total active energy in forward direction.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.14 Forward fundamental wave active energy on phase A/B/C

Name:
APenergyAF
APenergyBF
APenergyCF

Fundamental wave of active energy in forward direction of the phase.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.15 Reverse fundamental wave total active energy

Name:
ANenergyTF

Fundamental wave of total active energy in reverse direction.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.16 Reverse fundamental wave active energy on phase A/B/C

Name:
ANenergyAF
ANenergyBF
ANenergyCF

Fundamental wave of active energy in reverse direction of the phase.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.17 Forward harmonics total active energy

Name:
APenergyTH

Harmonics of total active energy in forward direction.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.18 Forward harmonics active energy on phase A/B/C

Name:
APenergyAH
APenergyBH
APenergyCH

Harmonics of active energy in forward direction of the phase.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.19 Reverse harmonics total active energy

Name:
ANenergyTH

Harmonics of total active energy in reverse direction.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.20 Reverse harmonics active energy on phase A/B/C

Name:
ANenergyAH
ANenergyBH
ANenergyCH

Harmonics of active energy in reverse direction of the phase.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.21 Total active energy combined

Name:
AEnergyT

Total active energy in forward and backward direction.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Internal calculation formula for the total active energy:

AEnergyT = (DINT)(APenergyT - ANenergyT) ... Calculation overflows must be handled in the application

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.11.22 Total reactive energy combined

Name:
REnergyT

Total reactive energy in forward and backward direction.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	Resolution 0.1 or 0.01 CF, depending on the Power Line factor (e.g. kWs)

Internal calculation formula for the total reactive energy:

REnergyT = (DINT)(RPenergyT - RNenergyT) ... Calculation overflows must be handled in the application

Comments:

- The unit CF is derived from the Power Line factor (default: 3600 Imp/kWh), see register "MeteringMode"
- The resolution can be switched between 0.1 and 0.01, see register "MeteringMode"
- The register is updated automatically after being enabled, see register "ControlOutput" <Bit 1>
- The register is cleared upon request, see register "ControlOutput"
- The register is set upon request, see register "ControlOutput" <Bit 3>

4.3.22.11.12 Analog DFT registers

4.3.22.11.12.1 Read timestamp for DFT register (+0x0022 = 16 bit)

Name:
SampleTime03_32bit

Network timestamp for the readout of the DFT register.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	Network time

4.3.22.11.12.2 HD register current I and voltage V for phases A/B/C

Name:
DftAI (0..30), DftAV (0..30)
DftBI (0..30), DftBV (0..30)
DftCI (0..30), DftCV (0..30)

Ratio of 2nd to 32nd order harmonics.

Data type	Value	Information
UINT	0 to 32767	Ratio of frequency component

Conversion from % = register value / 163.84

4.3.22.11.12.3 THD register current I and voltage V for phases A/B/C

Name:
DftAI (31), DftAV (31)
DftBI (31), DftBV (31)
DftCI (31), DftCV (31)

Ratio of total harmonic distortion.

Data type	Value	Information
UINT	0 to 32767	Total harmonic distortion on phase A current

Conversion from % = register value / 163.84

4.3.22.11.12.4 Fundamental wave current on phase A/B/C

Name:
DftAI_Fund
DftBI_Fund
DftCI_Fund

Data type	Value	Information
UINT	0 to 32767	Fundamental wave current

Conversion (%) of fundamental wave current = register value * 209 * 65.535 / 8388608

4.3.22.11.12.5 Fundamental wave voltage on phase A/B/C

Name:
DftAV_Fund
DftBV_Fund
DftCV_Fund

Data type	Value	Information
UINT	0 to 32767	Fundamental value voltage

Conversion (%) of fundamental wave voltage = register value * 418 * 655.35 / 8388608

4.3.22.11.13 Module configuration

4.3.22.11.13.1 Analog mode register

Name:
ChanControl

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	Channel status LED for phase A	0	Disabled
		1	Enabled[1)]
1	Channel status LED for phase B	0	Disabled
		1	Enabled[1)]
2	Channel status LED for phase C	0	Disabled
		1	Enabled[1)]
3	Reserved	0	
4	Neutral current monitor and status LED	0	Disabled
		1	Enabled[1)]
5	Neutral current status derived from the calculated or measured value	0	Derived from the calculated value[1)]
		1	Derived from the calculated value
6	Conversion of energy register to kWh (internal register / 4096)	0	Disabled
		1	Enabled
7	Display current values despite power failure[2)]	0	Disabled[3)], Current values = 0
		1	Enabled
8 - 15	Oversampling with prescaler	0	Disabled[1)], Current values = 0
		1 - 255	Enabled, Display current values despite power failure

1) Standard in the bus controller function model
2) When a power failure occurs, all current values are held at 0 by default.
3) According to the power failure status of the individual phases, the following values are held at 0 by default.

- Mains frequency, phase angle, power factor
- Effective voltage and current values
- Active, reactive and apparent power values

4.3.22.11.13.2 Analog minimum current for active current channel LED

Name:
IDispTh

Data type	Value	Information
UINT	100 to 65000	I RMS indicator threshold

The indicator threshold defines the RMS value of the current at which the status LED for the phase current is illuminated. The default values vary from module to module and should be adjusted to the maximum primary current. Suggestion: 1% of maximum value

Module	Indicator threshold
X20AP3111	200 mA
X20AP3121	500 mA
X20AP3131	500 mA
X20AP3161	500 mA

4.3.22.11.13.3 Current transformer rating phase A/B/C/N

Name:
I_RatioA
I_RatioB
I_RatioC
I_RatioN

Data type	Value	Information
UINT	10 to x	Current transformer rating

In the modules AP311, 21 and 31, the rated current is multiplied by the rated transformation ratio. In the module AP3161, the maximum primary current of the transformer is configured directly.

The permissible values differ from module to module (resolution 0.1):

Module	Rating
X20AP3111	Transformer ratio: 10 to 32,500 (default: 25000)
X20AP3121	Transformer ratio: 10 to 650 (default: 500)
X20AP3131	Transformer ratio: 10 to 130 (default: 100)
X20AP3161	Measurement range: 50 to 650 (default: 500)

Information:

The maximum resulting current must not exceed the value of 65000 mA.

4.3.22.11.13.4 Update request ADC Cfg register

Name:
CfgUpdate

The registers in the group CfgReg are only updated after the CfgUpdate register is changed. Setting 0xFFFF only causes this register to be reset without updating the CfgReg register.

Data type	Value	Information
UINT	0 to 65,535	Update request

4.3.22.11.13.5 Update request ADC Cs0, Cs1 and Cs3 register

Name:
Cs0Update
Cs1Update
Cs3Update

The registers in the group CsxReg are only updated after the CsxUpdate register is changed. Setting 0xFFFF only causes this register to be reset without updating the CsxReg register.

Data type	Value	Information
UINT	0 to 65,535	Update request

Name:
Cs1UpdateFB
Cs3UpdateFB

The ADC configuration registers are only transferred to the feedback buffer after transfer to the ADC is complete.

Data type	Value	Information
UINT	0 to 65,535	

4.3.22.11.14 ADC status configuration

4.3.22.11.14.1 ADC hardware signal allocation

Name:
ZXConfig

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	Zero cross signals	0	Enabled
		1	Disabled
1 - 2	ZX20Con: Trigger zero cross-over	00	Positive zero cross-over[1)]
		01	Negative zero cross-over
		10	Both zero cross-overs
		11	No zero cross-over
3 - 4	ZX1Con: Trigger zero cross-over	00	Positive zero cross-over[1)]
		01	Negative zero cross-over
		10	Both zero cross-overs
		11	No zero cross-over
5 - 6	ZX2Con: Trigger zero cross-over	00	Positive zero cross-over[1)]
		01	Negative zero cross-over
		10	Both zero cross-overs
		11	No zero cross-over
7 - 9	ZX0Src: Signal source for ZX0 hardware signal	000	A voltage[1)]
		001	B voltage
		010	C voltage
		011	Fix 0
		100	Current A
		101	Current B
		110	Current C
		111	Fix 0
10 - 12	ZX1Src: Signal source for ZX1 hardware signal	000	A voltage
		001	B voltage[1)]
		010	C voltage
		011	Fix 0
		100	Current A
		101	Current B
		110	Current C
		111	Fix 0
13 - 15	ZX2Src: Signal source for ZX2 hardware signal	000	A voltage
		001	B voltage
		010	C voltage[1)]
		011	Fix 0
		100	Current A
		101	Current B
		110	Current C
		111	Fix 0

1) Standard in the bus controller function model

4.3.22.11.14.2 Voltage warning threshold

Name:
SagTh

Data type	Value	Information
UINT	5000 to 50000	Resolution 0.01 V

This register defines an RMS voltage value for monitoring the voltage warning signal.

4.3.22.11.14.3 Power failure threshold

Name:
PhaseLoseTh

Data type	Value	Information
UINT	1000 to 6000	Resolution 0.01 V

This register defines an RMS voltage value for monitoring the power failure signal.

4.3.22.11.14.4 Warning threshold for the calculated neutral current

Name:
INWarnTh0

Current value for monitoring the calculated neutral line current.

Data type	Value	Information
UINT	0 to 65000	Resolution 0.001 A

4.3.22.11.14.5 Warning threshold for the measured neutral current.

Name:
INWarnTh1

Current value for monitoring the measured neutral line current.

Data type	Value	Information
UINT	0 to 65000	Resolution 0.001 A

4.3.22.11.14.6 Warning threshold for exceeding voltage THD

Name:
THDNUTh

Percentage value defining warning threshold for THD ratio.

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01%

4.3.22.11.14.7 Warning threshold for exceeding current THD

Name:
THDNITh

Percentage value defining warning threshold for THD ratio.

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01%

4.3.22.11.15 ADC measurement configuration checksum 0

4.3.22.11.15.1 High word for power line constants

Name:
PLconstH

Data type	Value
UINT	0 to 65,535

Basis value of power line constant = 0x4A817C80 = 1,250,000,000 corresponding to 360 CF pulses per kWh or 0.1 CF pulse per kWs. The result of setting the resolution in the energy registers to a decimal (see register "MeteringMode" <Bit 9>) is 1 kWs per digit. Power line constant / 10 results in a 10x resolution.

4.3.22.11.15.2 Low word for power line constants

Name:
PLconstL

Data type	Value
UINT	0 to 65,535

Basis value of power line constant = 0x4A817C80 = 1,250,000,000 corresponding to 360 CF pulses per kWh or 0.1 CF pulse per kWs. The result of setting the resolution in the energy registers to a decimal (see register "MeteringMode" <Bit 9>) is 1 kWs per digit. Power line constant / 10 results in a 10x resolution.

4.3.22.11.15.3 Analog ADC measurement setting 1

Name:
MeteringMode

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	Enables phase C for adding the power and energy values together	0	Not enabled
		1	Approved[1)]
1	Enables phase B for adding the power and energy values together	0	Not enabled
		1	Approved[1)]
2	Enables phase A for adding the power and energy values together	0	Not enabled
		1	Approved[1)]
3	Calculation method for adding active power and active energy	0	Arithmetic sum[1)]
		1	Absolute sum
4	Calculation method for adding reactive power and reactive energy	0	Arithmetic sum[1)]
		1	Absolute sum
5	Reserved	0	
6	Selects apparent energy for CF2 source	0	Arithmetic sum[1)]
		1	Vector sum
7	CF2 source	0	Apparent energy
		1	Reactive energy[1)]
8	Measuring configuration	0	3P4W[1)]
		1	3P3W
9	Resolution of energy register	0	0.1 CF[1)]
		1	0.01 CF
10	Integrator for didt current transformer	0	Disabled
		1	Enabled
11	High-pass filter	0	Enabled
		1	Disabled
12	Basis frequency	0	50 Hz[1)]
		1	60 Hz
13	Phase assignment	0	I1 to Phase A and I3 to Phase C[1)]
		1	I1 to Phase C and I3 to Phase A
14 - 15	Reserved	0	

1) Standard in the bus controller function model

Comments regarding measurement configurations:

Measuring configuration	Note
3P4W	Monitors the phasing of voltages and currents: Phase A before phase B before phase C
3P3W	Measuring configuration: Phase A and phase C, N connection bridges to phase B or open
	Measurement: e.g. the 2 phases A and C and the 2 corresponding currents are measured, phase B disabled
	Monitors the phasing of voltages and currents: Phase difference between A and C >180°

4.3.22.11.16 User calibration of current and voltage values

Use the following procedure to properly calculate gain and offset:

- Read out the predefined values:
  See section 4.3.22.11.17 "ADC RMS comparison – read"
- Calculate and set new values:
  See section 4.3.22.11.18 "ADC RMS comparison checksum 3"
- Update predefined values by setting the register "Cs3Update". The predefined values have been updated when the value in the register "Cs3UpdateFB" is equal to the value of <Cs3Update>.

4.3.22.11.17 ADC RMS comparison – read

4.3.22.11.17.1 General information

The values in the registers specified below must be read at the beginning of the calibration. This is the only way to ensure that the gain and offset will be calculated correctly.

The values contained in the registers correspond to the $value_{old}$ in the calculation formulas for gain and offset (see 4.3.22.11.18 "ADC RMS comparison checksum 3").

4.3.22.11.17.2 Voltage RMS gain phase A/B/C

Name:
UGainA_R
UGainB_R
UGainC_R

Data type	Value
UINT	0 to 65,535

4.3.22.11.17.3 Current RMS gain phase A/B/C/N

Name:
IGainA_R
IGainB_R
IGainC_R
IGainN_R

Data type	Value
UINT	0 to 65,535

4.3.22.11.17.4 Voltage RMS offset phase A/B/C

Name:
UoffsetA_R
UoffsetB_R
UoffsetC_R

Data type	Value
INT	-32,767 to 32,767

4.3.22.11.17.5 Current RMS offset phase A/B/C/N

Name:
IoffsetA_R
IoffsetB_R
IoffsetC_R
IoffsetN_R

Data type	Value
INT	-32,767 to 32,767

4.3.22.11.18 ADC RMS comparison checksum 3

4.3.22.11.18.1 Voltage RMS gain phase A/B/C

Name:
UGainA_W
UGainB_W
UGainC_W

Data type	Value	Information
UINT	0 to 65,535	Voltage RMS gain, phase-based

The resulting gain is calculated using the following formula:

$Value_{new} = Value_{old}$ * correction factor, determined when $U = U_n$

4.3.22.11.18.2 Current RMS gain phase A/B/C/N

Name:
IGainA_W
IGainB_W
IGainC_W
IGainN_W

Data type	Value	Information
UINT	0 to 65,535	Current RMS gain, phase-based

The resulting gain is calculated using the following formula:

$Value_{new} = Value_{old}$ * correction factor, determined when $I = I_n$

4.3.22.11.18.3 Voltage RMS offset phase A/B/C

Name:
UoffsetA_W
UoffsetB_W
UoffsetC_W

Corresponds to the negated value of the corresponding RMS register when U = 0.

Data type	Value	Information
INT	-32,767 to 32,767	RMS voltage offset, phase-based

4.3.22.11.18.4 Current RMS offset phase A/B/C/N

Name:
IoffsetA_W
IoffsetB_W
IoffsetC_W
IoffsetN_W

Corresponds to the negated value of the corresponding RMS register when I = 0.

Data type	Value	Information
INT	-32,767 to 32,767	RMS current offset, phase-based

4.3.22.11.19 User calibration of power values

Use the following procedure to properly calculate the power angle correction:

1 Calculate the values
2 Write the value 0xFFFF to register Cs1Update
3 Read register Cs1UpdateFB until 0xFFFF is returned
4 Write the calculated values to the registers PhiA_W, PhiB_W, PhiC_W
5 Write the value 0x0001 to register Cs1Update
6 Read register Cs1UpdateFB until 0x0001 is returned

Information:

These registers are NOT nonvolatile, and the process needs to be repeated after every PowerOn and every positive edge of the ModuleOK bit.

4.3.22.11.19.1 ADC power angle correction, Phase A/B/C

Name:
PhiA_R
PhiB_R
PhiC_R

These registers can be used to read out the configured values at runtime, but are not nonvolatile and have the value 0 after the system is started.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 9	Delay time for energy phase angle correction	x	The clock base is 2.048 MHz. Maximum 0.499 mSec.
10 - 14	Reserved	0	
15	Delay times	0	Effect on current channel
		1	Effect on voltage channel

4.3.22.11.19.2 ADC power calibration checksum 1

Name:
PhiA_W
PhiB_W
PhiC_W

These registers can be used to correct phase shifts at runtime. This can be necessary if the transformers used distort the phase shift.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 9	Delay time for energy phase angle correction	0 to 1023	See descriptions for Bits 0 to 9
10 - 14	Reserved	0	
15	Delay times	0 or 1	See description for Bit 15

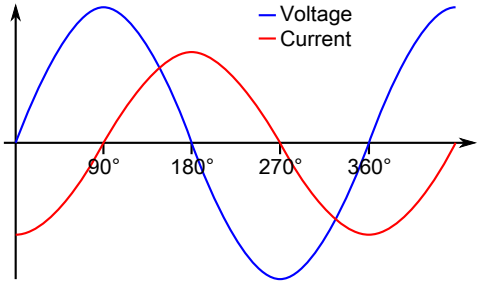
Description - Bits 0 to 9

The maximum correction 0x3FF = 1023 dec. corresponds to 0.49951 ms.

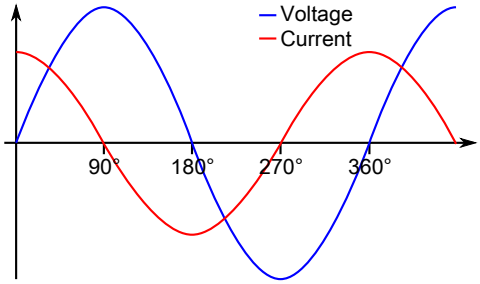
At 50 Hz mains this corresponds to a change of 8.99 degrees

At 60 Hz mains this corresponds to a change of 10.79 degrees

Schematic representation of inductive load: Voltage ahead of current



Schematic representation of capacitive load: Current ahead of voltage



Desription - Bit 15

0	Delay affects current channel	
	Effect with inductive load	Reduced angle between I and U, and therefore an increased power factor
	Effect with capacitive load	Increased angle between U and I, and therefore an reduced power factor
1	Delay affects voltage channel	
	Effect with inductive load	Reduced angle between U and I, and therefore an increased power factor
	Effect with capacitive load	Increased angle between I and U, and therefore an reduced power factor

4.3.22.11.20 FlatStream communication

4.3.22.11.20.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

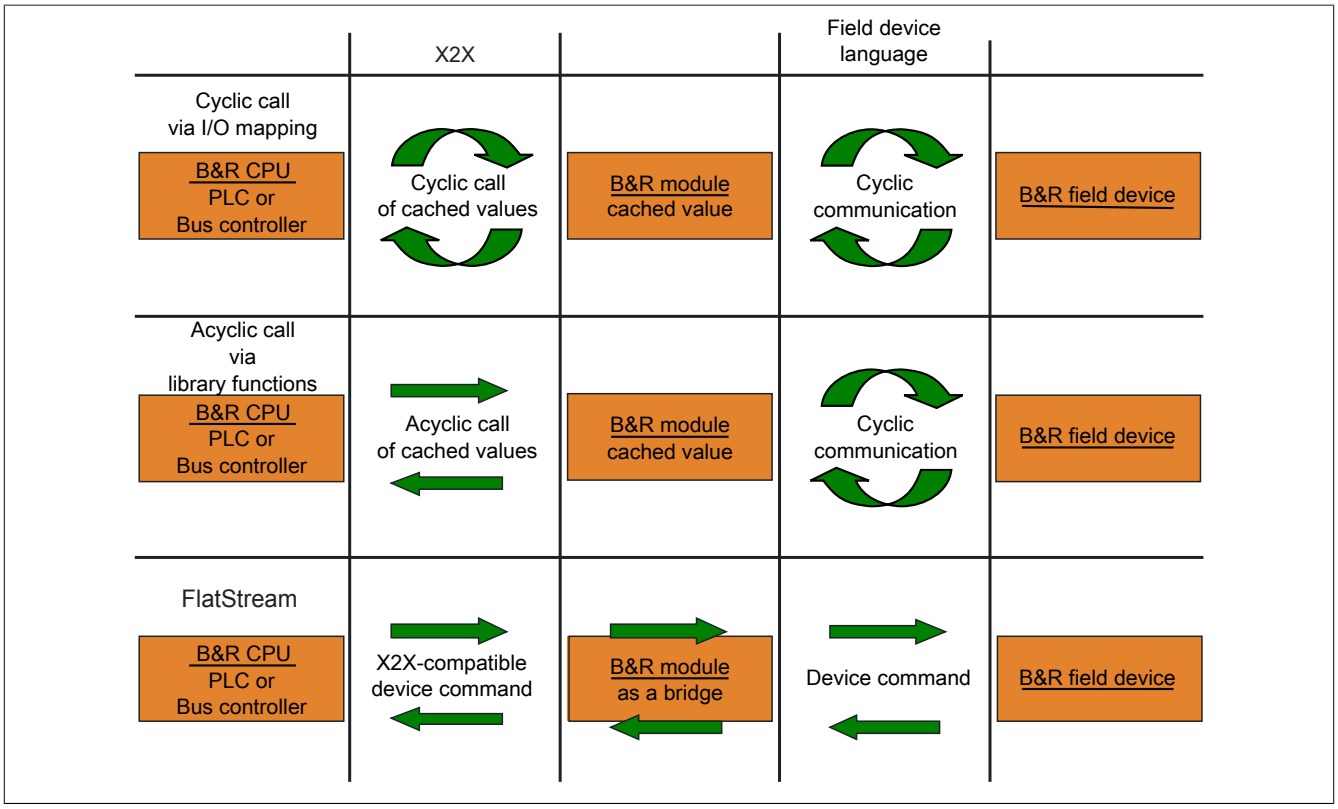


Figure 117: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.3.22.11.20.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.3.22.11.20.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

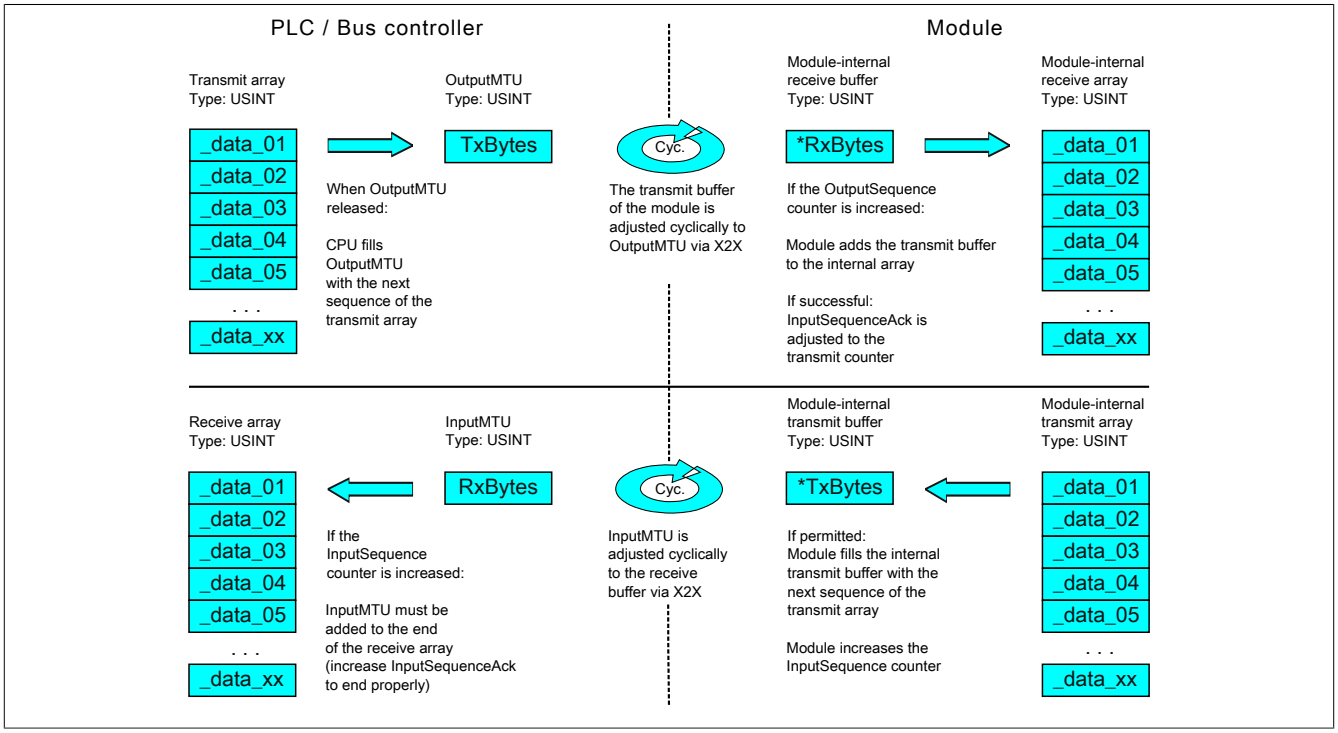


Figure 118: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.3.22.11.20.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

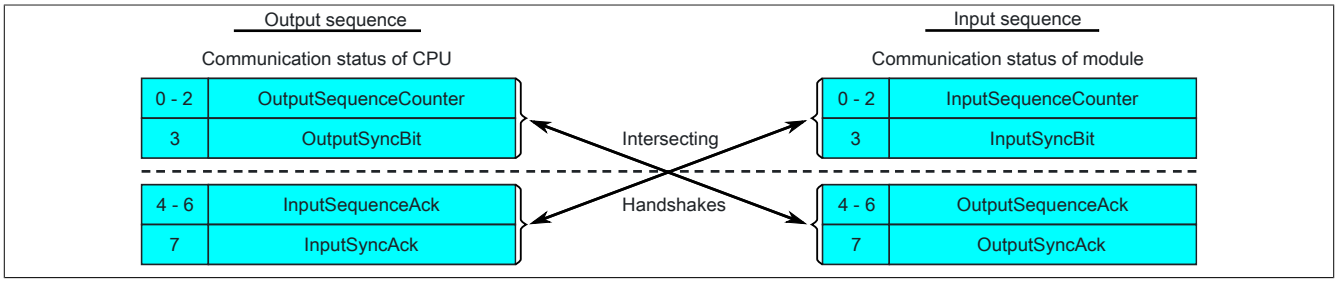


Figure 119: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

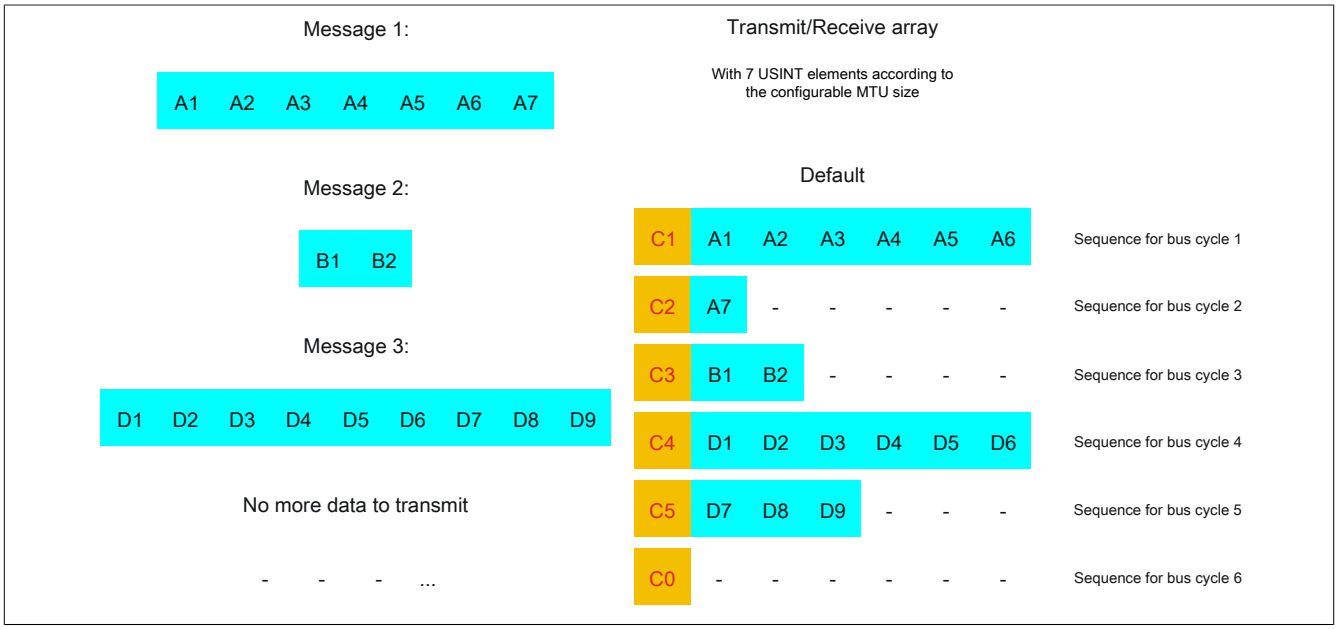


Figure 120: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 74: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 75: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

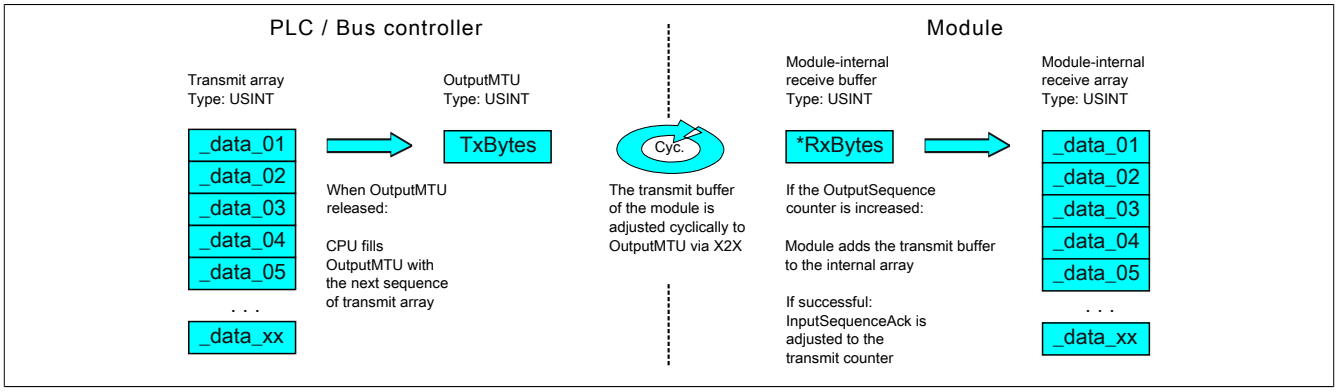


Figure 121: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

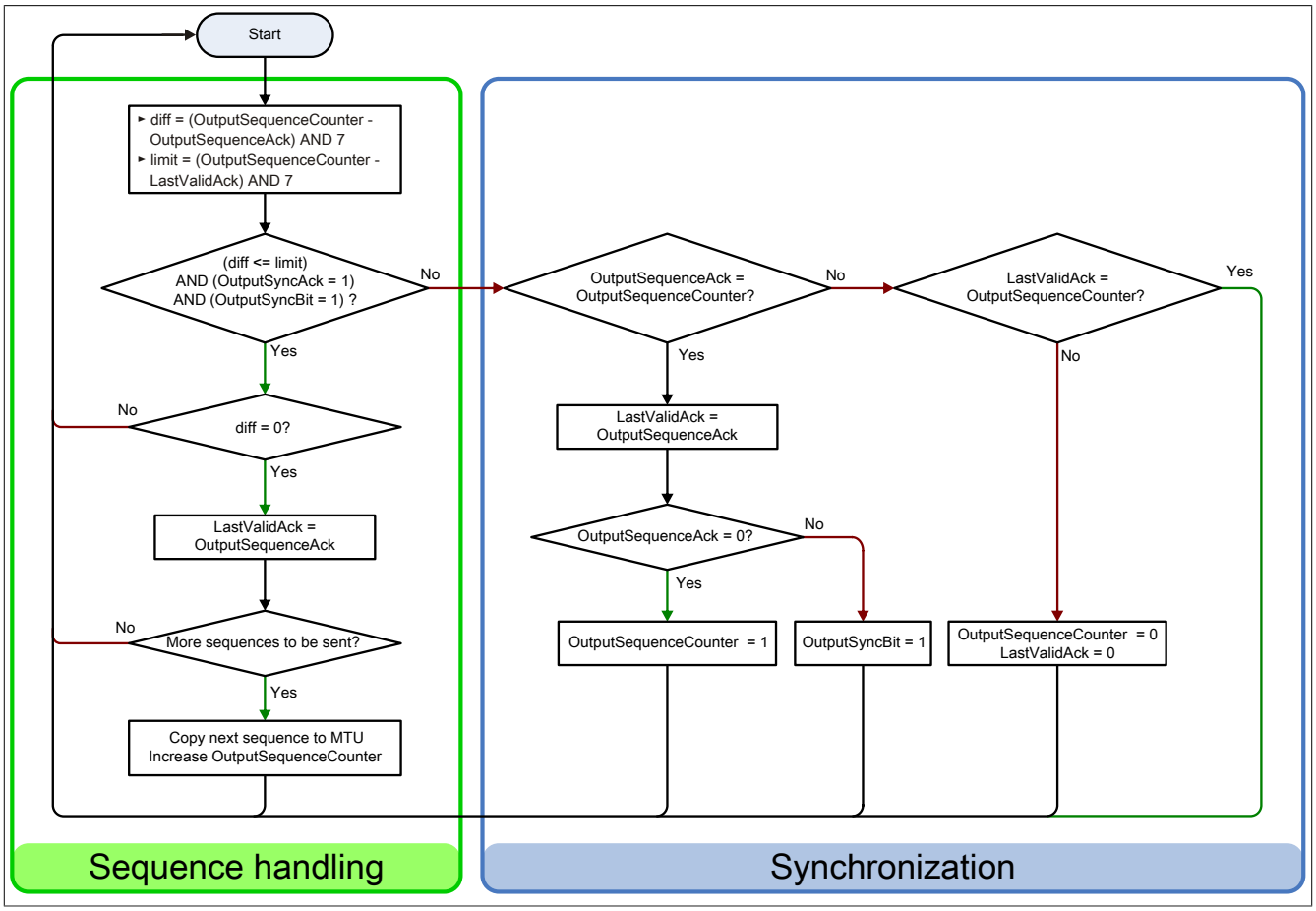


Figure 122: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

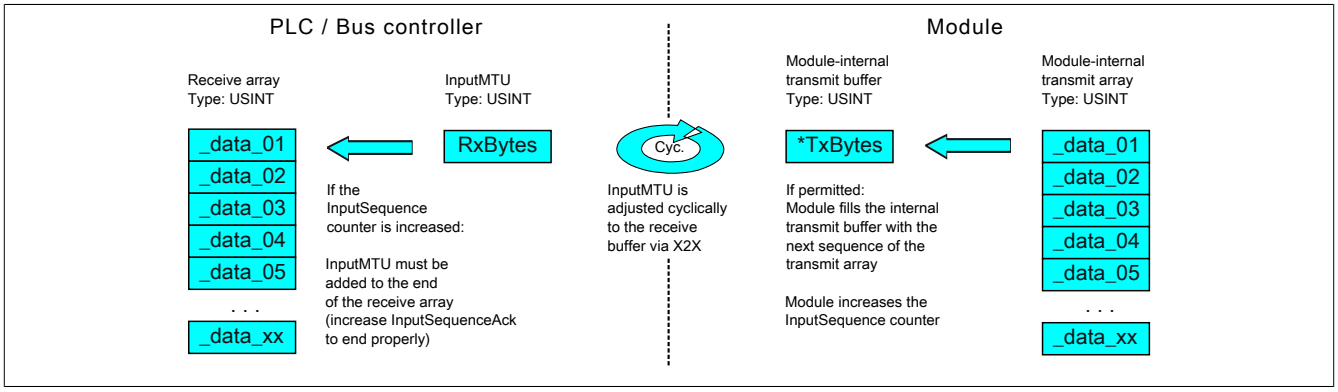


Figure 123: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

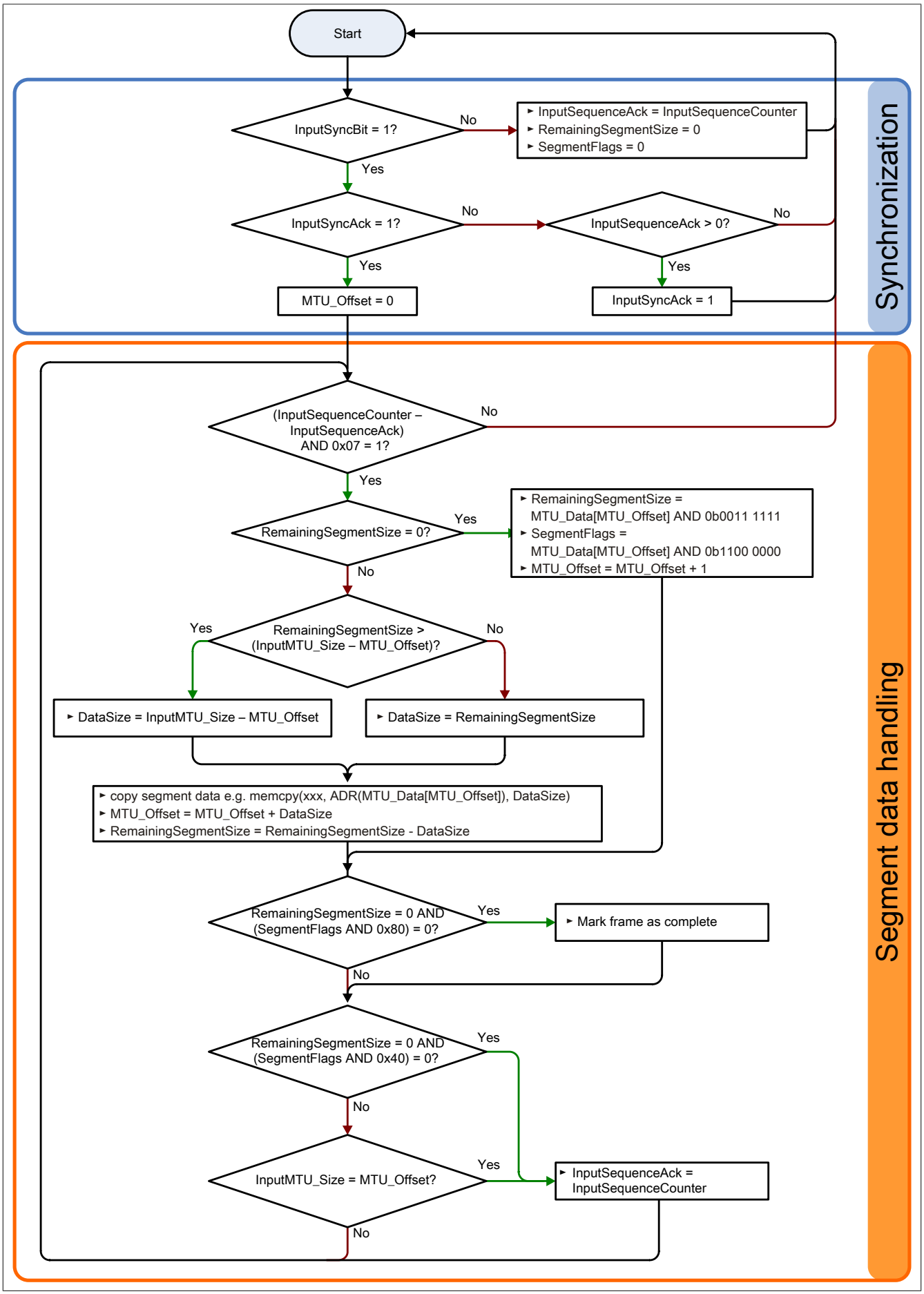


Figure 124: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

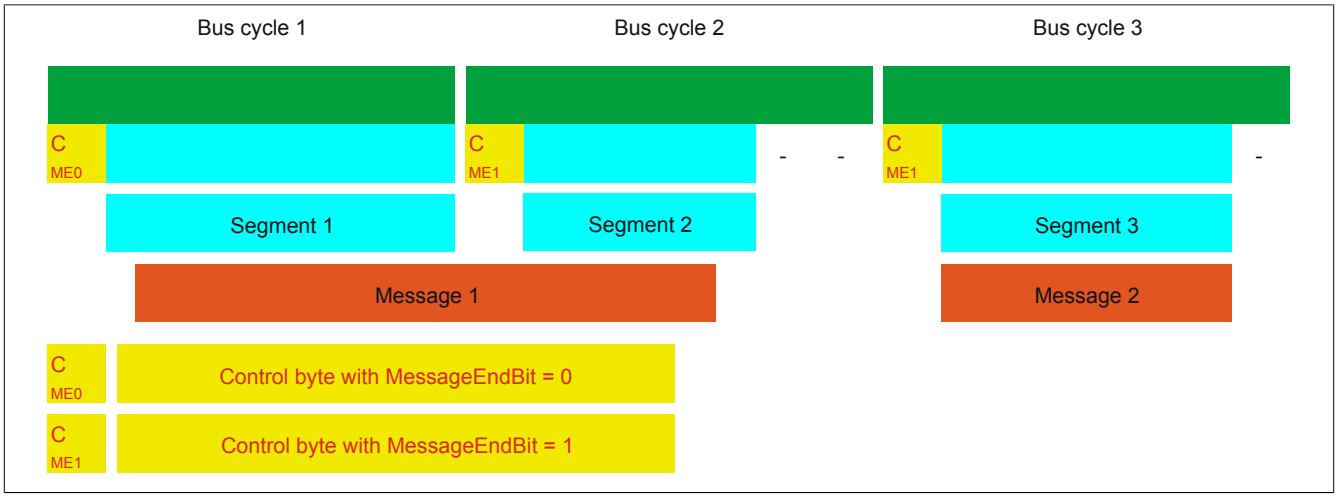


Figure 125: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

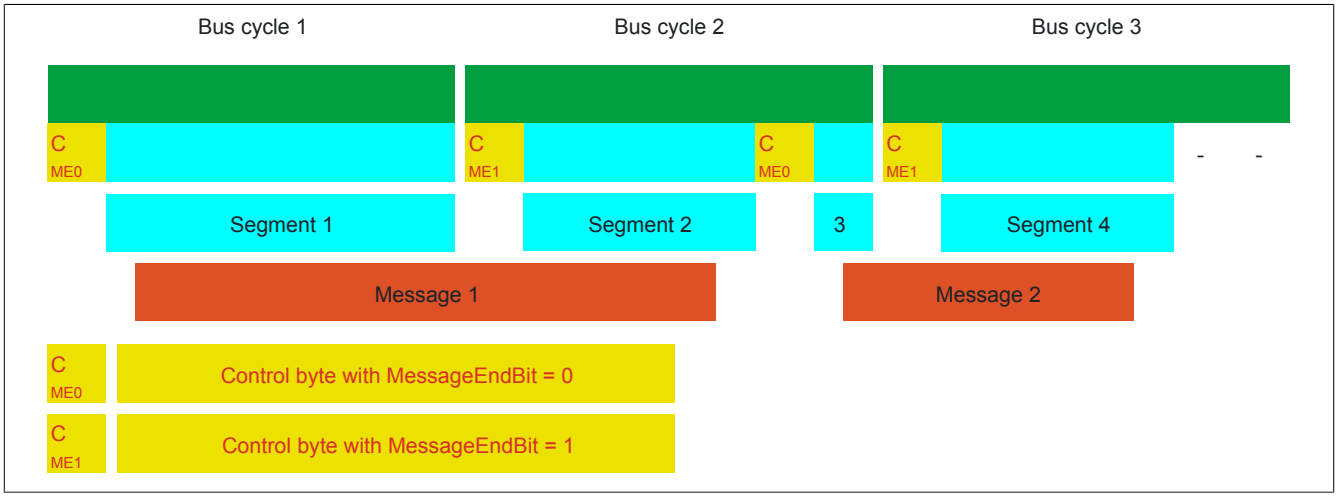


Figure 126: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

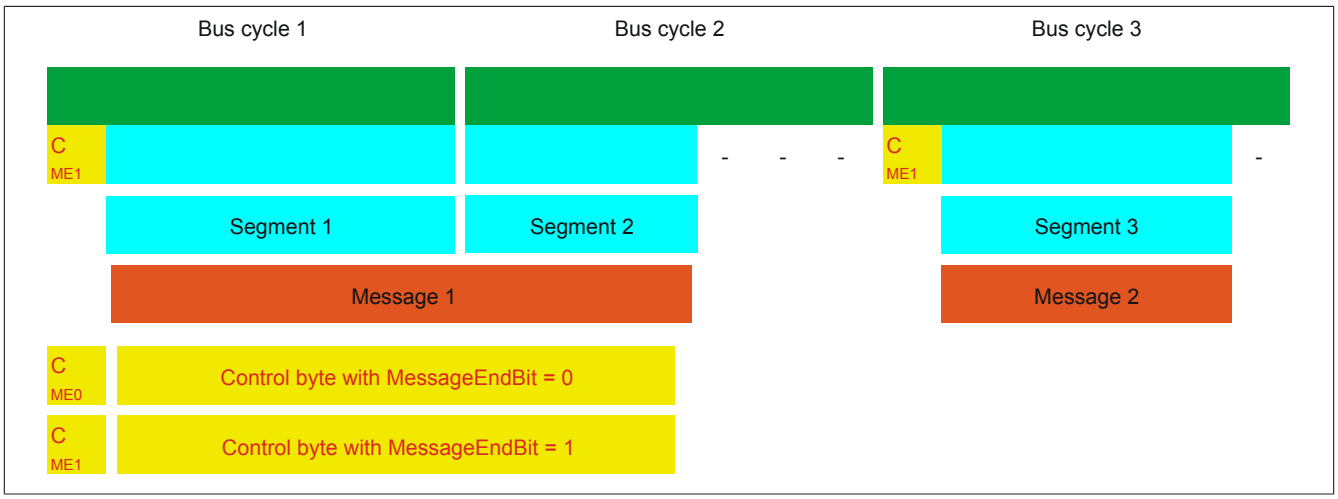


Figure 127: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

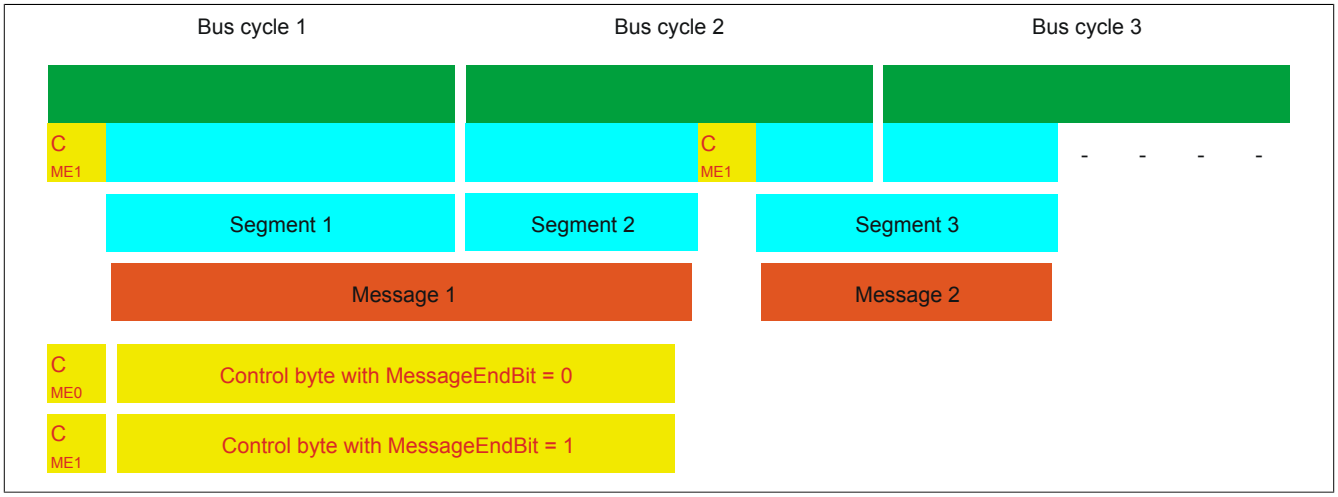


Figure 128: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

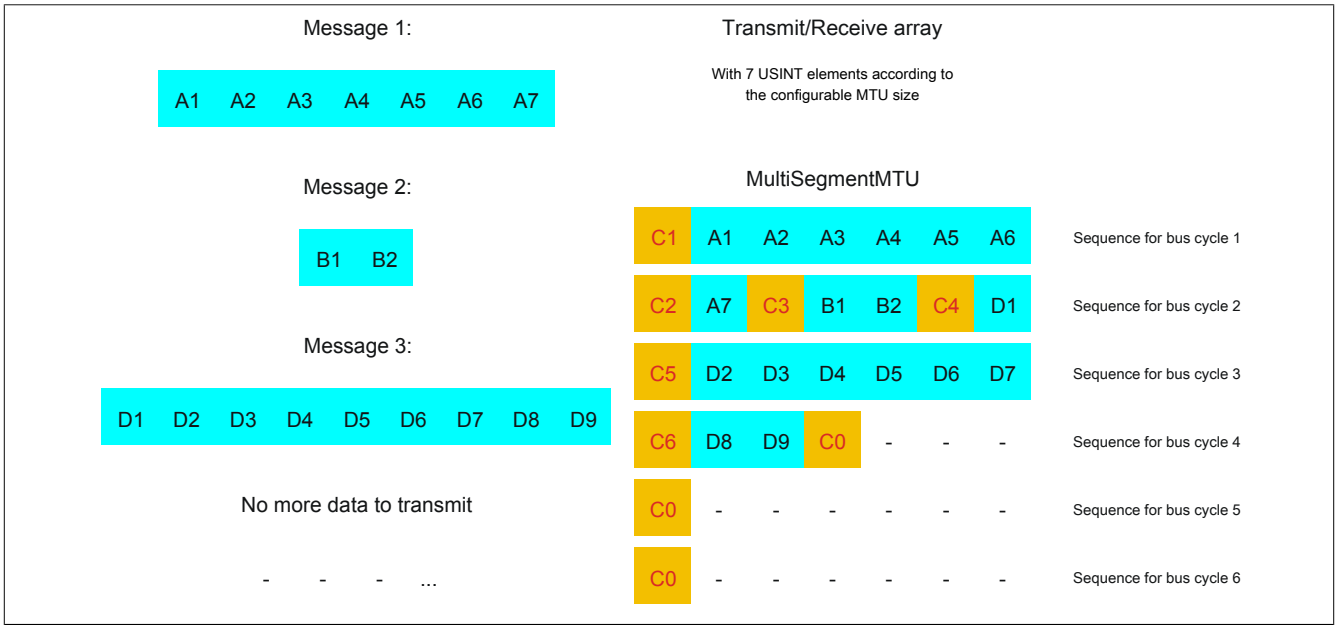


Figure 129: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 76: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 77: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

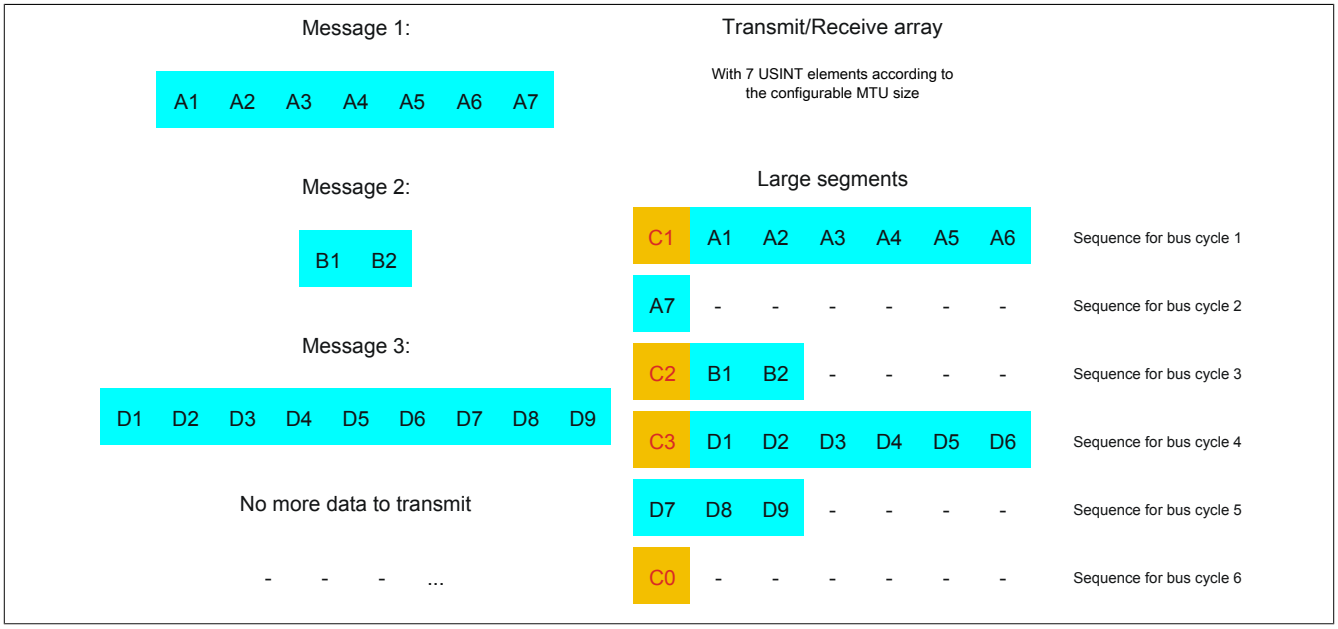


Figure 130: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 78: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

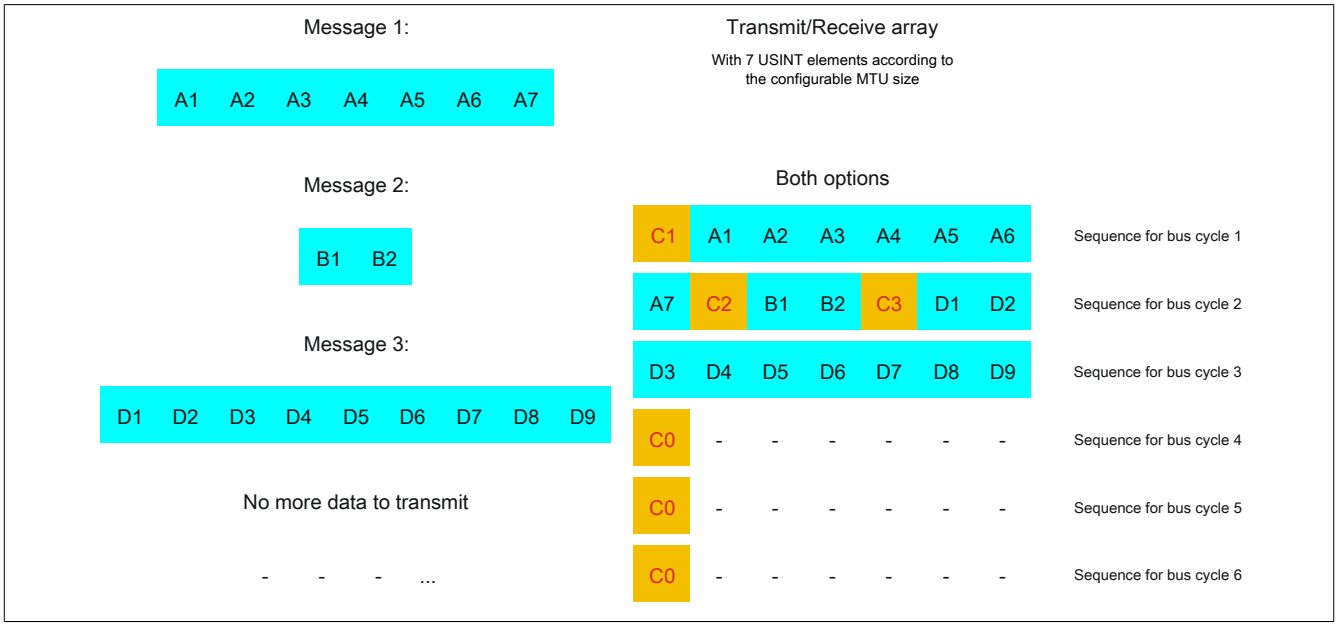


Figure 131: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 79: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.3.22.11.20.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

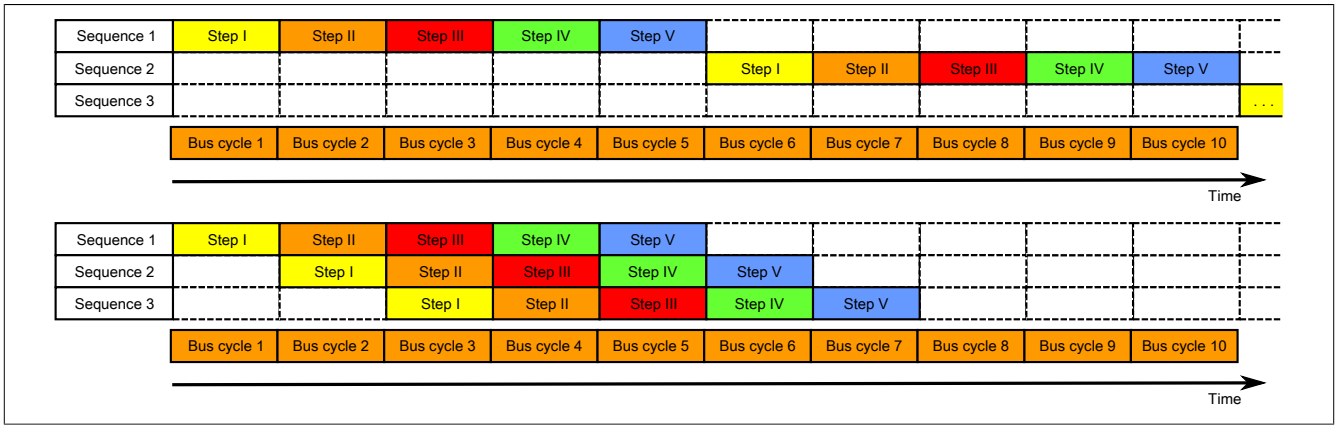


Figure 132: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

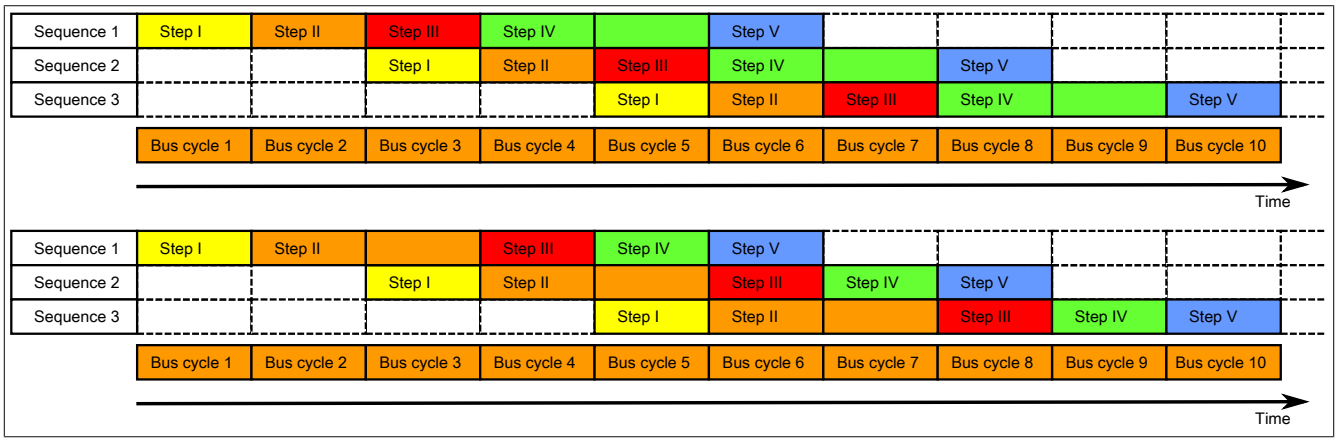


Figure 133: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

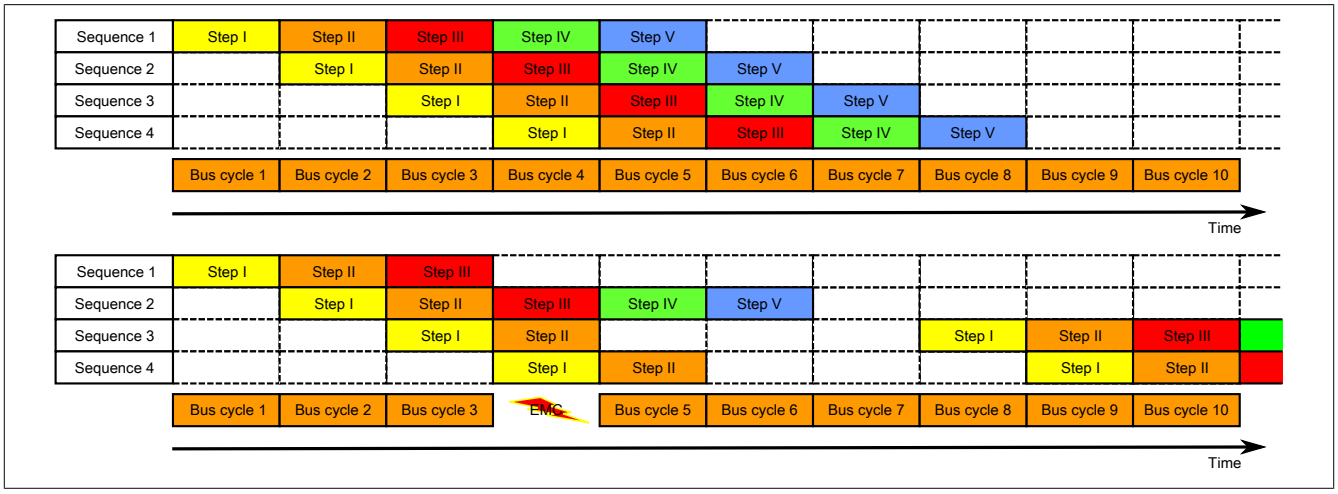


Figure 134: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.3.22.11.21 Force analog energy registers

Name:

The registers are described under 4.3.22.11.11 "Analog energy registers". Comparison:

Force registers	Read registers
Frc_APenergyT Frc_APenergyTF Frc_APenergyTH	"APenergyT"
Frc_APenergyA Frc_APenergyAF Frc_APenergyAH	"APenergyA"
Frc_APenergyB Frc_APenergyBF Frc_APenergyBH	"APenergyB"
Frc_APenergyC Frc_APenergyCF Frc_APenergyCH	"APenergyC"
Frc_ANenergyT Frc_ANenergyTF Frc_ANenergyTH	"ANenergyT"
Frc_ANenergyA Frc_ANenergyAF Frc_ANenergyAH	"ANenergyA"
Frc_ANenergyB Frc_ANenergyBF Frc_ANenergyBH	"ANenergyB"
Frc_ANenergyC Frc_ANenergyCF Frc_ANenergyCH	"ANenergyC"
Frc_RPenergyT	"RPenergyT"
Frc_RPenergyA	"RPenergyA"
Frc_RPenergyB	"RPenergyB"
Frc_RPenergyC	"RPenergyC"
Frc_RNenergyT	"RNenergyT"
Frc_RNenergyA	"RNenergyA"
Frc_RNenergyB	"RNenergyB"
Frc_RNenergyC	"RNenergyC"
Frc_SAenergyT	"SAenergyT"
Frc_SenergyA	"SenergyA"
Frc_SenergyB	"SenergyB"
Frc_SenergyC	"SenergyC"
Frc_SVenergyT	"SVenergyT"

These registers can be used to set the energy counter to a specific value after a module has been replaced.

Data type	Value
UDINT	0 to 4,294,967,295

4.3.22.11.21.1 Force forward total active energy

Name:
FrcAPenergyT

The registers are described under 4.3.22.11.11 "Analog energy registers".

These registers can be used to set the energy counter to a specific value after a module has been replaced. The register is updated to the current values when triggered by ControlOutput, Bit 3.

Data type	Value
UDINT	0 to 4,294,967,295

4.3.22.11.22 Oversampling buffer

4.3.22.11.22.1 General information

A Sample Line contains the present values for currents (4 channels) and voltages (3 channels), as well as a consecutive number and the network time when transferred from the transformer. These values are recorded in an interval of 125 µs * prescaler.

The user must then scale the values to respective physical values:

Voltage: Vrms = (INT32)Vs * 4 / Sqrt(2)
Current: Irms = (INT32)Is * 4 / Sqrt(2)

4.3.22.11.22.2 Sample - Neutral current

Name:
IactN_Sample1 to IactN_Sample16

Data type	Value	Information
INT	-32,767 to 32,767	Present value of the neutral current, resolution 0,001 A

This value must be converted by the application: See section 4.3.22.11.22.1 "General information"

4.3.22.11.22.3 Sample - Current on phase A

Name:
IactA_Sample1 to IactA_Sample16

Data type	Value	Information
INT	-32,767 to 32,767	Present current value on phase A, resolution 0.001 A

This value must be converted by the application: See section 4.3.22.11.22.1 "General information"

4.3.22.11.22.4 Sample - Voltage on phase A

Name:
UactA_Sample1 to UactA_Sample16

Data type	Value	Information
INT	-32,767 to 32,767	Present voltage value on phase A, resolution 0.01 V

This value must be converted by the application: See section 4.3.22.11.22.1 "General information"

4.3.22.11.22.5 Sample - Current on phase B

Name:
IactB_Sample1 to IactB_Sample16

Data type	Value	Information
INT	-32,767 to 32,767	Present current value on phase B, resolution 0.001 A

This value must be converted by the application: See section 4.3.22.11.22.1 "General information"

4.3.22.11.22.6 Sample - Voltage on phase B

Name:
UactB_Sample1 to UactB_Sample16

Data type	Value	Information
INT	-32,767 to 32,767	Present voltage value on phase B, resolution 0.01 V

This value must be converted by the application: See section 4.3.22.11.22.1 "General information"

4.3.22.11.22.7 Sample - Current on phase C

Name:
IactC_Sample1 to IactC_Sample16

Data type	Value	Information
INT	-32,767 to 32,767	Present current value on phase C, resolution 0.001 A

This value must be converted by the application: See section 4.3.22.11.22.1 "General information"

4.3.22.11.22.8 Sample - Voltage on phase C

Name:
UactC_Sample1 to UactC_Sample16

Data type	Value	Information
INT	-32,767 to 32,767	Present voltage value on phase C, resolution 0.01 V

This value must be converted by the application: See section 4.3.22.11.22.1 "General information"

4.3.22.11.22.9 Sample number

Name:
SampleCount1 to Samplecount16

Number of new Sample Lines since last readout.

Data type	Value	Information
SINT	-127 to 127	Sample Line number, ascending, cyclic
INT	-32,767 to 32,767	

4.3.22.11.22.10 Sample time

Name:
Timestamp

Older Sample Lines must each be back-calculated with 125 µs.

Data type	Value	Information
INT	-32,767 to 32,767	Network timestamp of Sample Line 1
DINT	-2,147,483,647 to 2,147,483,647	

4.3.22.11.23 Environment variables

4.3.22.11.23.1 Operating time in seconds

Name:
OnTime

The operating time since startup is saved in seconds in this register.

Data type	Value
UDINT	0 to 4,294,967,295

4.3.22.11.23.2 Startup counter

Name:
UpCounter

The number of restarts since startup is saved in this register.

Data type	Value
UDINT	0 to 4,294,967,295

4.3.22.11.23.3 Minimum operating temperature

Name:
MinTemp

The lowest transformer temperature [°C] since startup is saved in this register.

Data type	Value	Information
INT	-200 to 200	Resolution 1°C

4.3.22.11.23.4 Maximum operating temperature

Name:
MaxTemp

The highest transformer temperature [°C] since startup is saved in this register.

Data type	Value	Information
INT	-200 to 200	Resolution 1°C

4.3.22.11.24 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.3.22.11.25 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Voltage and current sampling rate for calculation of effective value, power and energy	1 MHz
Derived values: RMS, power, energy, power factor, phase angle, frequency (mean values over 16 full waves)	Approx. 3 Hz
FFT on request (SR: 8 kHz)	2 Hz

4.4 Analog output modules

Analog output modules convert PLC internal numerical values into voltages or currents. The numerical values which are to be converted must be in 16-bit 2s complement. The conversion takes place independently of the resolution of the output module used.

Every channel on an analog output module has a status LED.

4.4.1 Brief information

Product ID	Short description	on page
X20AO2437	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated	597
X20AO2438	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated, supports HART protocol	608
X20AO2622	X20 analog output module, 2 outputs, ±10 V / 0 to 20 mA / 4 to 20 mA, 13-bit resolution	661
X20AO2632	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution	668
X20AO2632-1	X20 analog output module, 2 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution	675
X20AO4622	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	682
X20AO4635	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, low temperature drift	708
X20cAO2437	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated	597
X20cAO2438	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated, supports HART protocol	608
X20cAO4622	X20 analog output module, coated, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	682

4.4.2 X20(c)AO2437

4.4.2.1 General information

The module is equipped with 2 current outputs with 16-bit digital converter resolution. The 2 channels are electrically isolated from each other. The user can select between the 3 output ranges 4 to 20 mA, 0 to 20 mA and 0 to 24 mA.

- 2 analog current outputs
- Electrically isolated analog channels
- 16-bit digital converter resolution

4.4.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.4.2.3 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO2437	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated	
X20cAO2437	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 80: X20AO2437, X20cAO2437 - Order data

4.4.2.4 Technical data

Product ID	X20AO2437	X20cAO2437
Short description		
I/O module	2 analog outputs 4 to 20 mA, 0 to 20 mA or 0 to 24 mA	
General information		
B&R ID code	0xB785	0xE1F2
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software	
Power consumption		
Bus	0.05 W	
Internal I/O	1.6 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Analog outputs		
Output	4 to 20 mA, 0 to 20 mA or 0 to 24 mA, configurable using software	
Digital converter resolution	16-bit	
Settling time for output changes over entire range	2 ms to 20 s, configurable using software	
Data output rate	1 ms without ramp	
Max. error at 25°C		
Gain		
4 to 20 mA	0.025% [2]	
0 to 20 mA	0.022% [2]	
0 to 24 mA	0.02% [2]	
Offset		
4 to 20 mA	0.025% [3]	
0 to 20 mA	0.022% [3]	
0 to 24 mA	0.02% [3]	
Output protection	Short circuit protection, overvoltage protection (up to 30 VDC)	
Open line detection	Yes, using hardware and software	
Data format	INT	
Output format		
4 to 20 mA	INT 0x0000 to 0x7FFF / 1 LSB = 0x0001 = 762.94 nA	
0 to 20 mA	INT 0x0000 to 0x7FFF / 1 LSB = 0x0001 = 610.352 nA UINT 0x0000 to 0xFFFF / 1 LSB = 0x0001 = 305.176 nA	
0 to 24 mA	INT 0x0000 to 0x5DC0 / 1 LSB = 0x0001 = 1000 nA	
Load per channel	Max. 600 Ω	
Short circuit protection	Yes, continuous	
Output filter	Active 2nd-order low pass / cutoff frequency 4 kHz Configurable slew rate	
Max. gain drift		
4 to 20 mA	0.0055 %/°C [2]	
0 to 20 mA	0.005 %/°C [2]	
0 to 24 mA	0.005 %/°C [2]	
Max. offset drift		
4 to 20 mA	0.0035 %/°C [3]	
0 to 20 mA	0.002 %/°C [3]	
0 to 24 mA	0.002 %/°C [3]	
Error caused by load change [4]		
4 to 20 mA	0.14%	
0 to 20 mA	0.1%	
0 to 24 mA	0.1%	
Nonlinearity	<0.003% [5]	
Test voltage between		
Channel and channel	1000 VAC	
Channel and bus	1000 VAC	
To ground	1000 VAC	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	

Table 81: X20AO2437, X20cAO2437 - Technical data

Product ID	X20AO2437	X20cAO2437
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 81: X20AO2437, X20cAO2437 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current output value.
3) Based on the respective output range
4) Load change from 1 Ω → 600 Ω, resistive
5) Based on the entire output range.

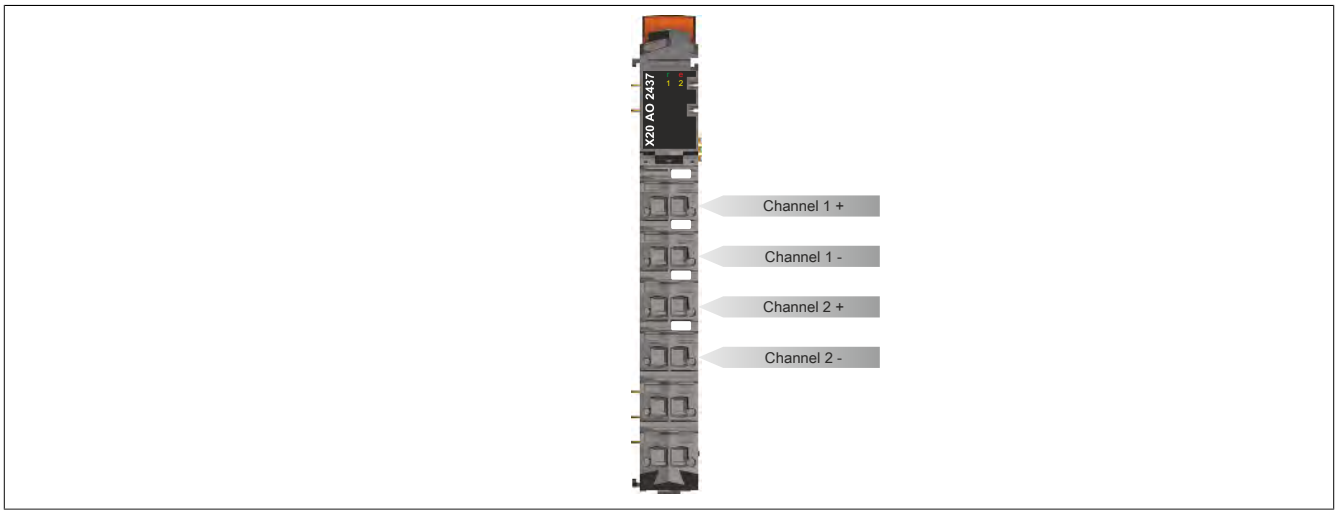
4.4.2.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

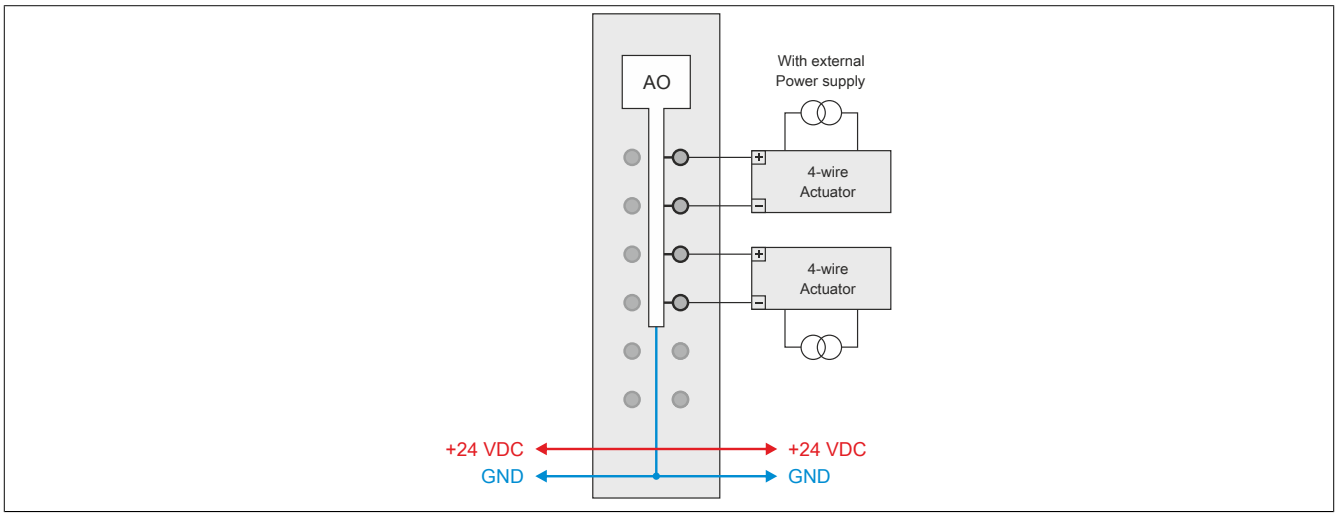
Figure	LED	Color	Status	Description
	**Operating status**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP mode
	Module status			
	e	Red	Off	No power to module or everything OK
			Single flash	A conversion error has occurred. When an error occurs, the LED of the faulty analog output channel begins to double flash and this status is output.
			On	Error or reset status
	Analog output			
	1 - 2	Orange	Off	Indicates one of the following cases: • No power to module • Channel disabled
			Single flash	Open line
			Double flash	A conversion error has occurred. A single flash is output on the red "e" module status LED.
			On	Digital/analog converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.2.6 Pinout



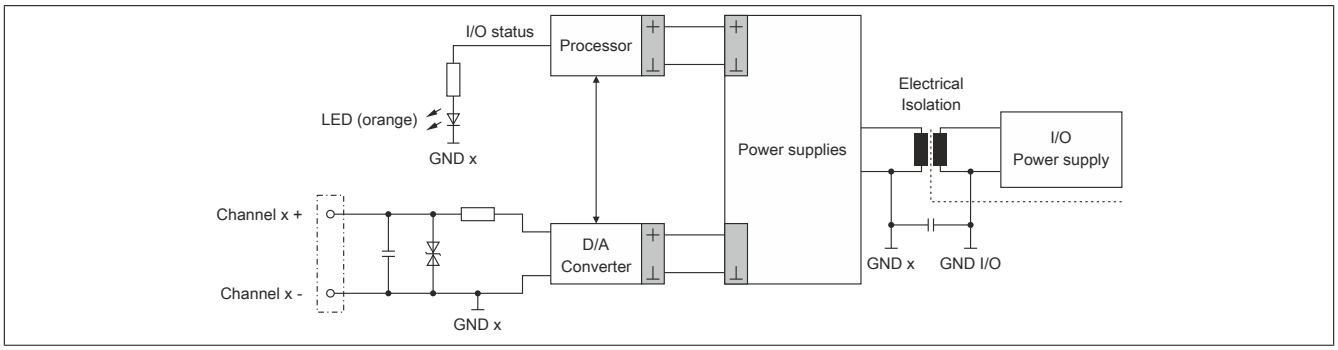
4.4.2.7 Connection example



4.4.2.8 OSP hardware requirements

In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.4.2.9 Output circuit diagram



4.4.2.10 Derating

To ensure proper operation, the derating values listed below must be adhered to:

Horizontal installation

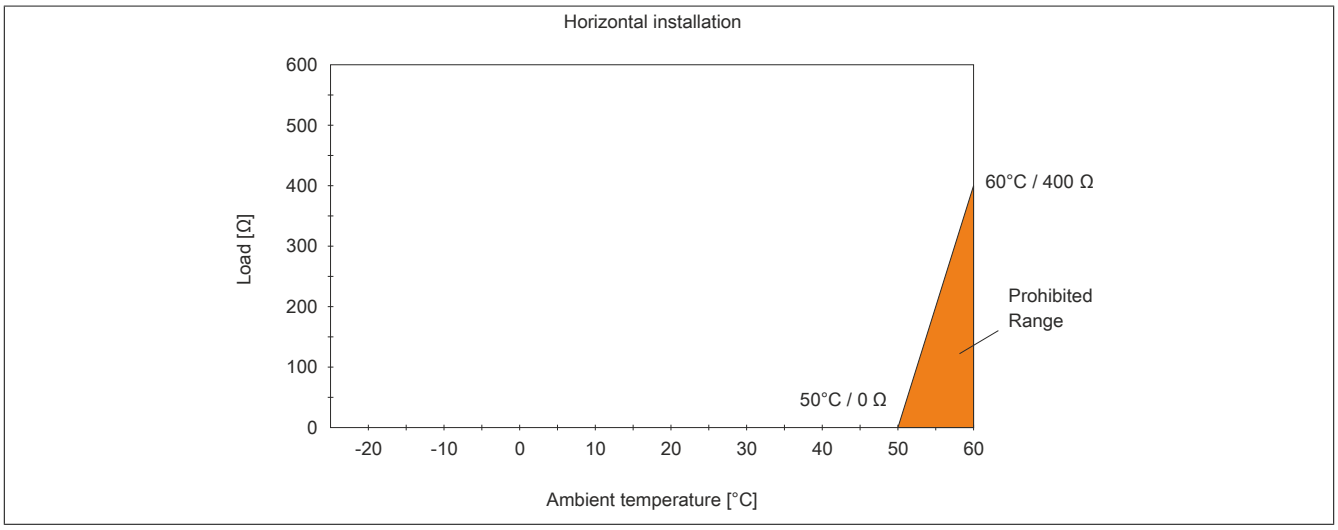


Figure 135: Derating the load with horizontal mounting

Vertical installation

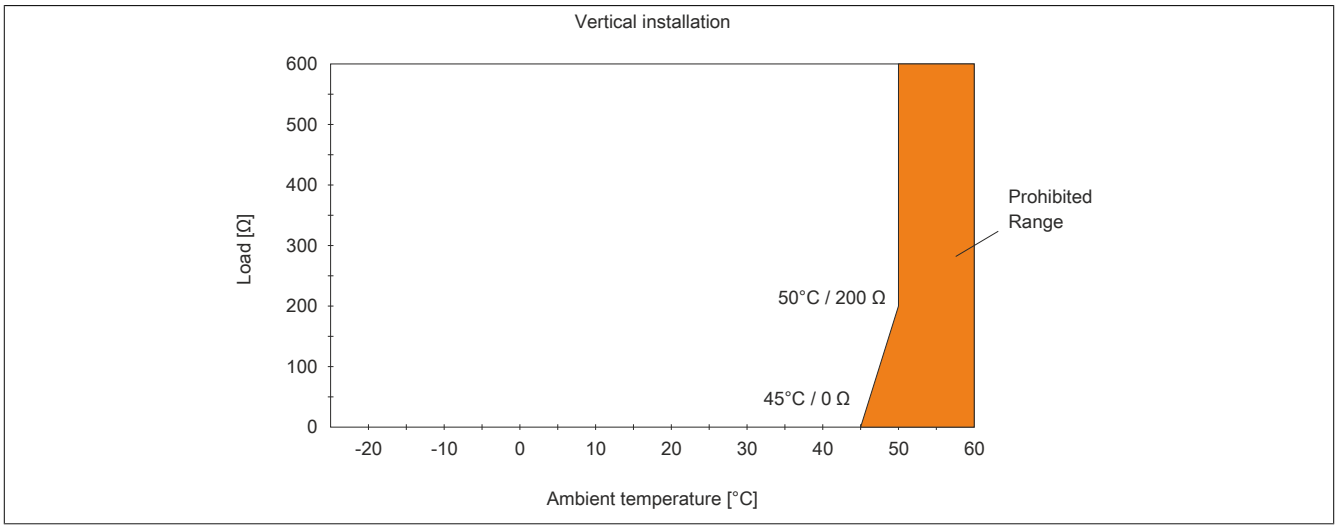


Figure 136: Derating the load with vertical mounting

4.4.2.11 Register description

4.4.2.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.2.11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
386 394	AnalogMode01 AnalogMode02	UINT				•
390 398	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication						
0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
	ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
	IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				

4.4.2.11.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
386 394	AnalogMode01 AnalogMode02	UINT				•
390 398	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication						
0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
	ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
	IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				
The OSP function model						
32	OSPComByte	USINT			•	
	OSPValid	Bit 0				
401 403	CfgOSPMode01 CfgOSPMode02	USINT				•
34 36	CfgOSPValue01 CfgOSPValue02	INT				•

4.4.2.11.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
386 394	-	AnalogMode01 AnalogMode02	UINT				•
390 398	-	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication							
0 2	0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	-	AnalogStatus01 AnalogStatus02	USINT		•		
		OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
		ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
		IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.4.2.11.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.4.2.11.5 Analog signal - Configuration

The module has 2 electrically isolated channels. All registers have a dual design. Channels can be configured and operated independently of one another.

Specific features

- Electrical isolation by channel
- Configurable output ramp DAC slew rate (Default: 210 ms full scale)

4.4.2.11.5.1 AnalogMode

Name:
AnalogMode01 to AnalogMode02

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be activated and configured separately.

Information:

When you select the operating mode "Scaling 0 to 20 mA (Resolution 0 to 65535)", then the corresponding "AnalogOutput" registers are interpreted internally as UINT instead of INT.
The entire program must be rebuilt for the data type change to take effect. The data type cannot be changed during runtime (e.g. using a library).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel	0	Disabled
		1	Enabled (bus controller default)
1	Check - DAC configuration/status	0	Enabled (bus controller default)
		1	Disabled
2 - 3	Reserved	-	
4	Scaling 0 to 20 mA (Resolution 0 to 32767)	0	Disabled
		1	Enabled
5	Scaling 4 to 20 mA (Resolution 0 to 32767)	0	Disabled
		1	Enabled (bus controller default)
6	Scaling 0 to 24 mA (Resolution 0 to 24000)	0	Disabled
		1	Enabled
7	Scaling 0 to 20 mA (Resolution 0 to 65535)	0	Disabled
		1	Enabled
8 - 15	Reserved	-	

4.4.2.11.5.2 DACSlewrate

Name:
DACSlewrate01 to DACSlewrate02

These registers limit the rate at which the analog signal is modified. This makes it possible to define a sort of upper limit frequency.

The following formula applies: f(Analog) = f(Output rate) * Permitted change / max. Δ(standardized output value)

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 2	Permitted change per rate	000	1-bit
		001	2-bit
		010	4 bit (bus controller default)
		011	8-bit
		100	16-bit
		101	32-bit
		110	64-bit
		111	128-bit
3 - 7	Reserved	-	
8 - 11	Output rate	0000	257730 Hz
		0001	198410 Hz
		0010	152440 Hz (bus controller default)
		0011	131580 Hz
		0100	115740 Hz
		0101	69440 Hz
		0110	37590 Hz
		0111	25770 Hz
		1000	20160 Hz
		1001	16030 Hz
		1010	10290 Hz
		1011	8280 Hz
		1100	6900 Hz
		1101	5530 Hz
		1110	4240 Hz
		1111	3300 Hz
12 - 14	Reserved	-	
15	Slewrate enable (ramp functionality)	0	Disabled (undefined jump behavior)
		1	Enabled (defined transitions)

4.4.2.11.6 Analog signal - Communication

In order to output the required current signal (default: 4 to 20 mA), the module must be provided with the standardized output value (default: 0 to 32767).

4.4.2.11.6.1 AnalogOutput

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Depending on the scaling selected (see AnalogMode register), the value range and the data type can be adapted to the requirements of the application. Once a permitted value is determined, the module outputs the respective current.

Information:

The value "0" disables the channel status LED.

Data type	Value	Information
INT	0 to 32767	Bus controller default: 0
Optional: UINT	0 to 65535	

4.4.2.11.6.2 AnalogStatus

Name:
AnalogStatus01 to AnalogStatus02

The status register gives the user feedback about whether the respective channel is functioning properly.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	-	
2	OpenLineAnalogOutput01, 02	0	Line OK
		1	Open line
3	ConversionErrorAnalogOutput01, 02	0	Conversion temperature OK
		1	Conversion temperature too high
4 - 6	Reserved	-	
7	IoSuppErrorAnalogOutput01, 02	0	Module supply OK
		1	Module supply error

4.4.2.11.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.4.2.11.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the relevant task in the master CPU. However, an output still occurs depending on the configuration of the OSP replacement value.

4.4.2.11.7.2 Setting the OSP mode

Name:
CfgOSPMode01 to CfgOSPMode02

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.4.2.11.7.3 Define the OSP analog output value

Name:
CfgOSPValue01 to CfgOSPValue02

This register contains the analog output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
Corresponds to AnalogOutput0x	Corresponds to AnalogOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.4.2.11.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.4.2.11.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.4.3 X20(c)AO2438

4.4.3.1 General information

The module is equipped with 2 current outputs with 16-bit digital converter resolution. It supports the HART communication standard for data transfer, parameter configuration and diagnostics.

The 2 channels are electrically isolated from each other. The user can select between the 3 output ranges 4 to 20 mA, 0 to 20 mA and 0 to 24 mA.

- 2 analog current outputs
- HART protocol integration
- Support for HART variables
- Electrically isolated analog channels
- 16-bit digital converter resolution

4.4.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.4.3.3 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO2438	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated, supports HART protocol	
X20cAO2438	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated, supports HART protocol	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 82: X20AO2438, X20cAO2438 - Order data

4.4.3.4 Technical data

Product ID	X20AO2438	X20cAO2438
Short description		
I/O module	2 analog outputs 4 to 20 mA, 0 to 20 mA or 0 to 24 mA	
General information		
B&R ID code	0xB3AA	0xE211
Status indicators	I/O function per channel, operating state, module status, HART	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software	
HART link	Yes, using status LED and software	
HART error	Yes, using status LED and software	
Power consumption		
Bus	0.05 W	
Internal I/O	1.65 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Analog outputs		
Output	4 to 20 mA, 0 to 20 mA or 0 to 24 mA, configurable using software	
Digital converter resolution	16-bit	
Settling time for output changes over entire range	2 ms to 20 s, configurable using software	
Data output rate		
With HART	210 ms (default)	
Analog	1 ms without ramp	
Max. error at 25°C		
Gain		
4 to 20 mA	0.025% [2]	
0 to 20 mA	0.022% [2]	
0 to 24 mA	0.02% [2]	
Offset		
4 to 20 mA	0.025% [3]	
0 to 20 mA	0.022% [3]	
0 to 24 mA	0.02% [3]	
Output protection	Short circuit protection, overvoltage protection (up to 30 VDC)	
Open line detection	Yes, using hardware and software	
Data format	INT	
Output format		
4 to 20 mA	INT 0x0000 to 0x7FFF / 1 LSB = 0x0001 = 762.94 nA	
0 to 20 mA	INT 0x0000 bis 0x7FFF / 1 LSB = 0x0001 = 610.352 nA UINT 0x0000 to 0xFFFF / 1 LSB = 0x0001 = 305.176 nA	
0 to 24 mA	INT 0x0000 to 0x5DC0 / 1 LSB = 0x0001 = 1000 nA	
Load per channel	Max. 600 Ω	
Short circuit protection	Yes, continuous	
Output filter	Active 2nd-order low pass / cutoff frequency 19 Hz Configurable slew rate	
Max. gain drift		
4 to 20 mA	0.0055 %/°C [2]	
0 to 20 mA	0.005 %/°C [2]	
0 to 24 mA	0.005 %/°C [2]	
Max. offset drift		
4 to 20 mA	0.0035 %/°C [3]	
0 to 20 mA	0.002 %/°C [3]	
0 to 24 mA	0.002 %/°C [3]	
Error caused by load change [4]		
4 to 20 mA	0.14%	
0 to 20 mA	0.1%	
0 to 24 mA	0.1%	
Nonlinearity	<0.003% [5]	
Test voltage between		
Channel and channel	1000 VAC	
Channel and bus	1000 VAC	
To ground	1000 VAC	
HART		
Transfer rate	1200 bit/s	

Table 83: X20AO2438, X20cAO2438 - Technical data

Product ID	X20AO2438	X20cAO2438
Operating frequencies	1200 Hz / 2200 Hz	
Burst operation possible	Yes	
Multi-drop operation		
Possible	Yes	
Participants	Up to 15	
Transmission amplitude		
Minimum	400 mV_{pp}	
Typical	500 mV_{pp}	
Maximum	600 mV_{pp}	
Receiving amplitude		
Minimum	120 mV_{pp}	
Maximum	1500 mV_{pp}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 83: X20AO2438, X20cAO2438 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current output value.
3) Based on the respective output range
4) Load change from 1 Ω → 600 Ω, resistive
5) Based on the entire output range.

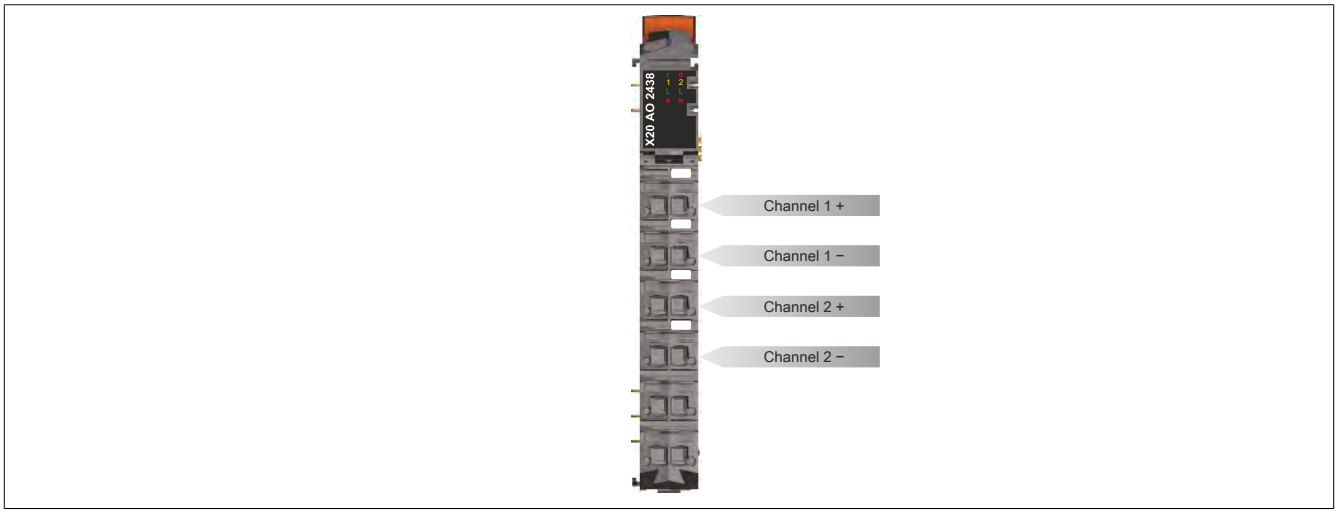
4.4.3.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

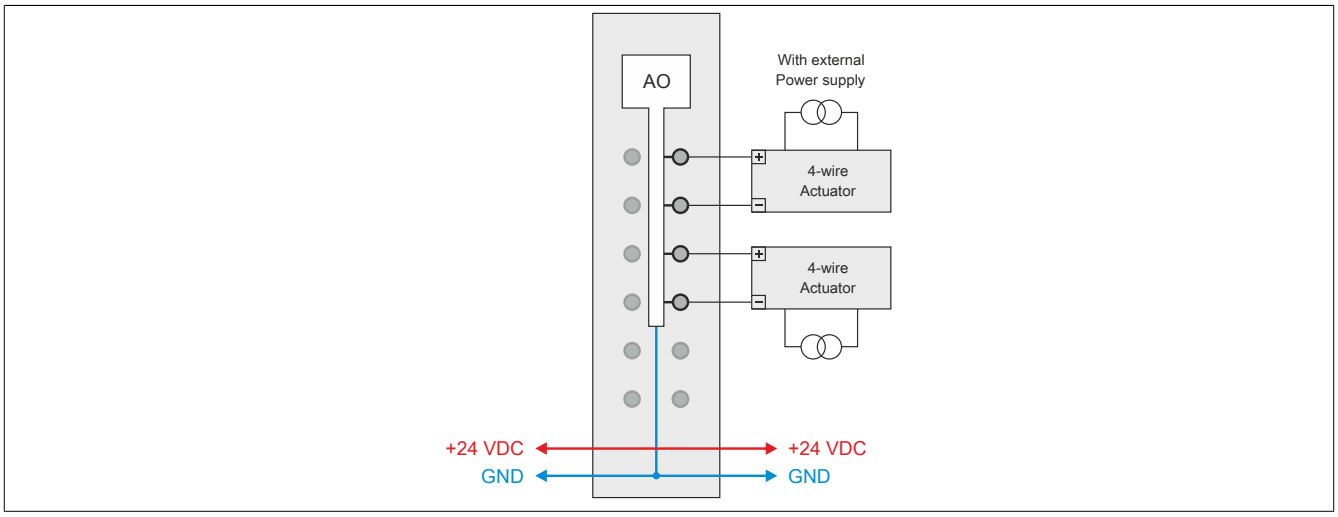
Figure	LED	Color	Status	Description
	**Operating status**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP mode
	Module status			
	e	Red	Off	No power to module or everything OK
			Single flash	A conversion error has occurred. When an error occurs, the LED of the faulty analog output channel begins to double flash and this status is output.
			On	Error or reset status
	Analog output			
	1 - 2	Orange	Off	Indicates one of the following cases: • No power to module • Channel disabled
			Single flash	Open line
			Double flash	A conversion error has occurred. A single flash is output on the red "e" module status LED.
			On	Digital/analog converter running, value OK
	HART link			
	L	Green	Off	Indicates one of the following cases: • No power to module • HART disabled for the respective channel
			Flickering	Carrier signal active (DCD or RTS)
	HART error			
	e	Red	Off	Indicates one of the following cases: • Communication taking place without errors • No power to module • HART disabled for the respective channel
			On	Communication error

1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.3.6 Pinout



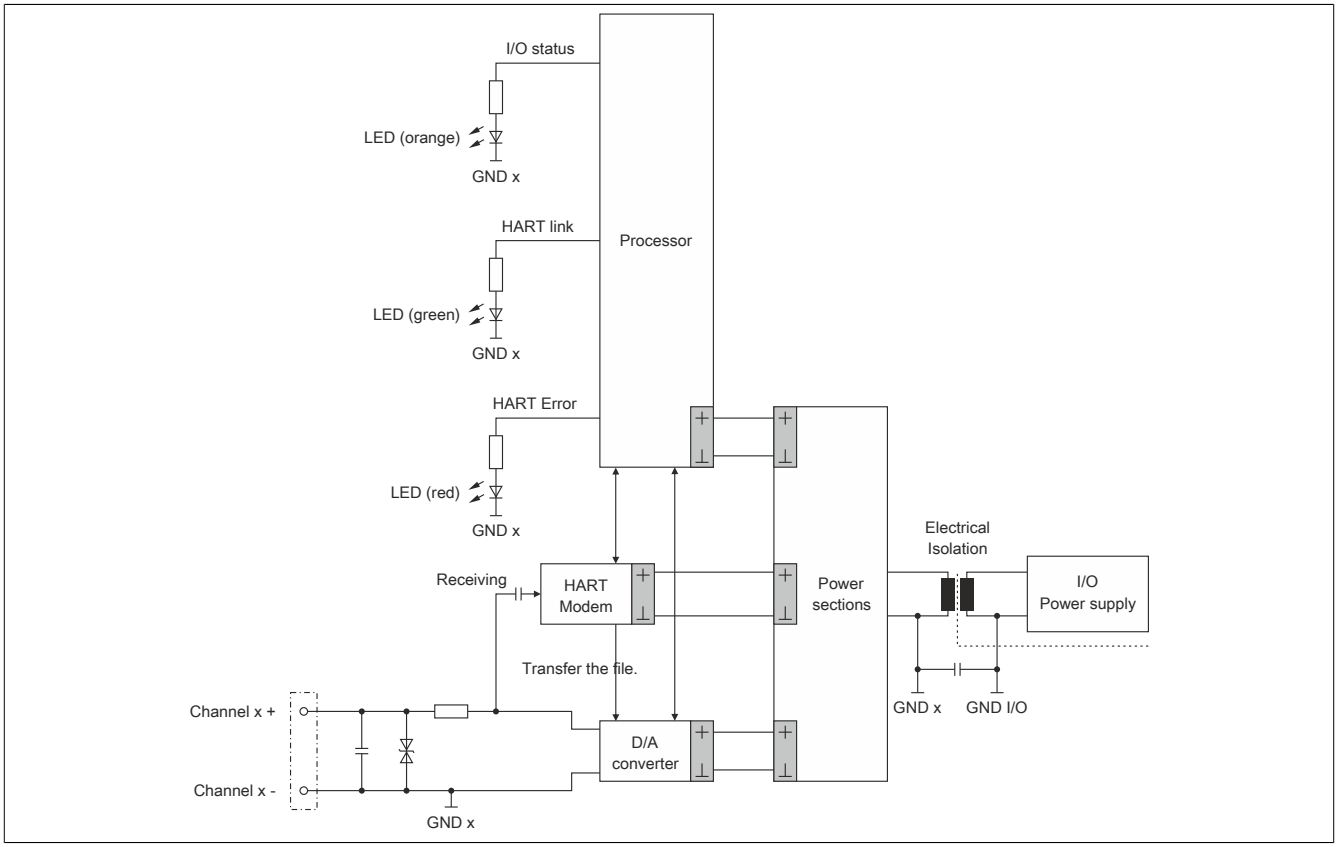
4.4.3.7 Connection example



4.4.3.8 OSP hardware requirements

In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.4.3.9 Output circuit diagram



4.4.3.10 Operation

4.4.3.10.1 Derating

To ensure proper operation, the derating values listed below must be adhered to:

Horizontal installation

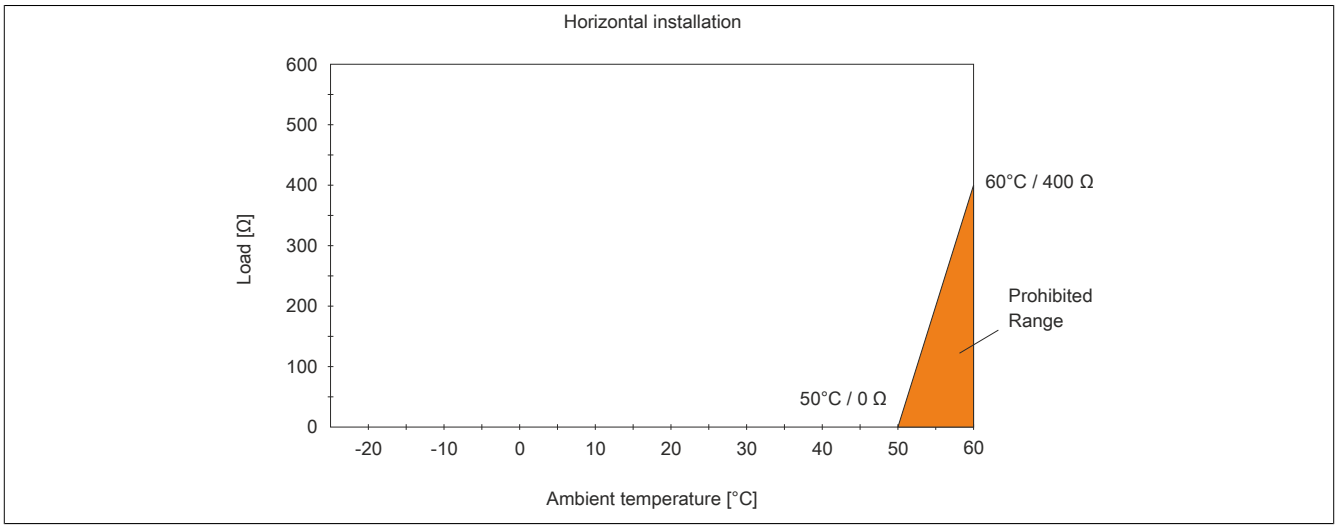


Figure 137: Derating the load with horizontal mounting

Vertical installation

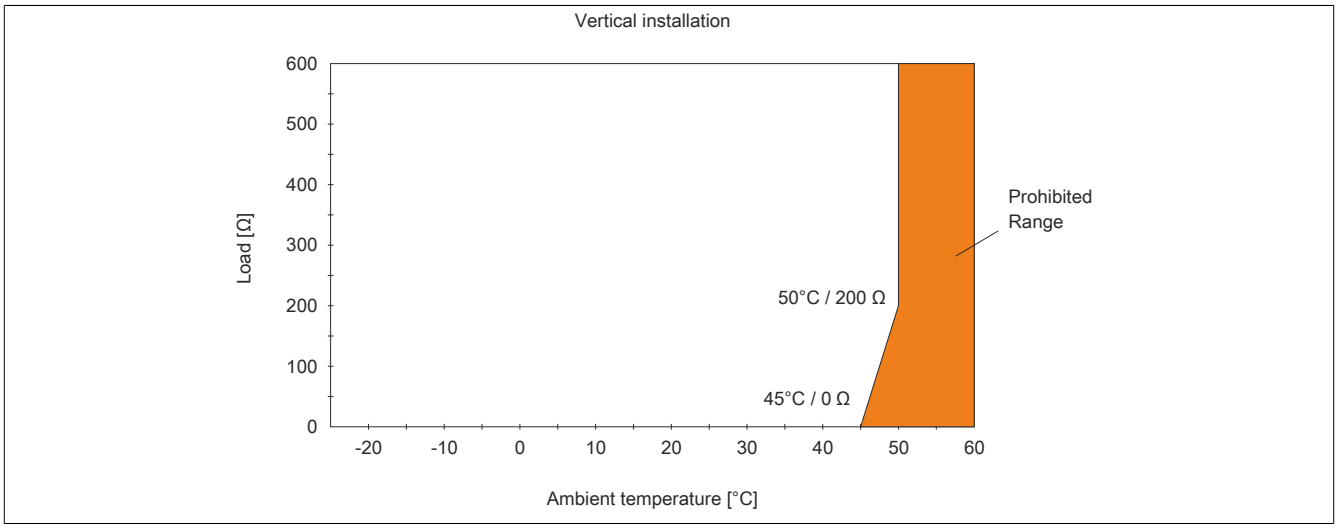


Figure 138: Derating the load with vertical mounting

4.4.3.10.2 HART communication standard

This module supports the HART communication standard for data transfer, parameter configuration and diagnostics. The HART standard is used for the current range 4 to 20 mA. Be aware that the load is not permitted to fall below 230 Ω .

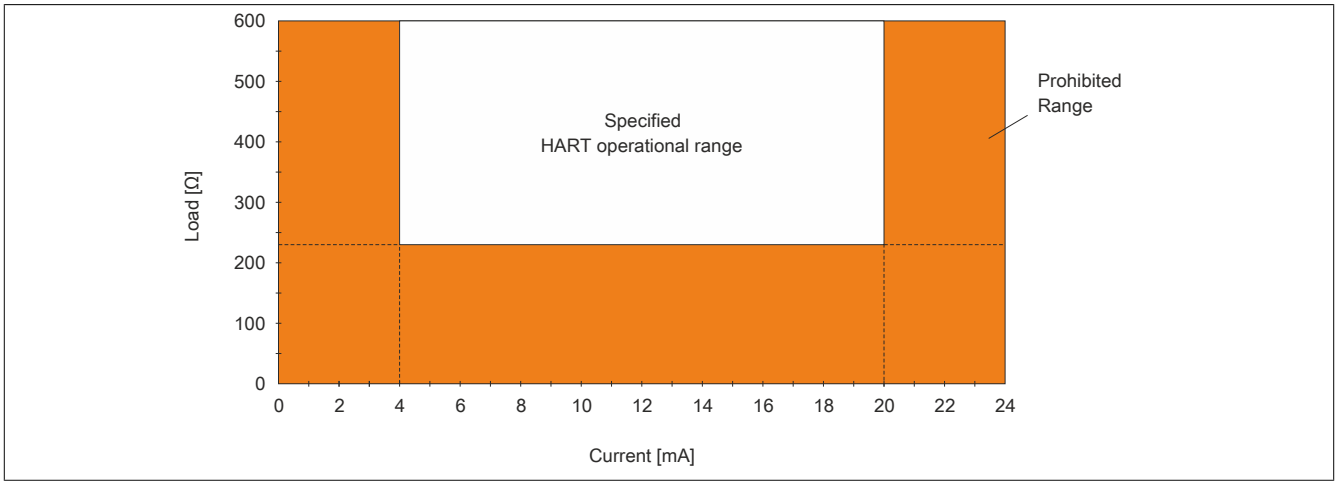


Figure 139: Specified HART operational range

Both current ranges 0 to 20 mA and 0 to 24 mA are supported by this module. HART communication can also be used in these ranges as well. It is important to make sure, however, that the output current lies within the specified HART operational range.

4.4.3.11 Register description

4.4.3.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.3.11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
386 394	AnalogMode01 AnalogMode02	UINT				•
390 398	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication						
0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
	ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
	IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				
HART - Configuration						
1537 1665	HartNodeCnt_1 HartNodeCnt_2	USINT				•
1539 1667	HartMode_1 HartMode_2	USINT				•
1541 1669	HartBurstNode_1 HartBurtNode_2	USINT				•
HART - Extended configuration						
1558 1668	HartNodeDisable_1 HartNodeDisable_2	UINT				•
1546 1674	HartProtTimeOut_1 HartProtTimeOut_2	UINT				•
1550 1678	HartProtRetry_1 HartProtRetry_2	UINT				•
1554 1682	HartPreamble_1 HartPreamble_2	UINT				•
HART - Communication (P2P)						
612 + Index*24 1124 + Index*24	PvInput01_N (Index N = 01 to 04) PvInput02_N (Index N = 01 to 04)	REAL	•	•[1)]		
617 + Index*24 1129 + Index*24	PvUnit01_N (Index N = 01 to 04) PvUnit02_N (Index N = 01 to 04)	USINT	•	•[1)]		
628 1140	PvSampleTime01 PvSampleTime02	DINT	•	•[1)]		
626 1138	PvSampleTime01 PvSampleTime02	INT	•			
566 1078	PvNodeComStatus01 PvNodeComStatus02	UINT		•		
HART - Communication (multidrop)						
612 + Index*24 1124 + Index*24	PvInput01_N (Index N = 01 to 15) PvInput02_N (Index N = 01 to 15)	REAL	•	•[1)]		
617 + Index*24 1129 + Index*24	PvUnit01_N (Index N = 01 to 15) PvUnit02_N (Index N = 01 to 15)	USINT	•	•[1)]		
604 + Index*24 1116 + Index*24	PvSampleTime01_N (Index N = 01 to 15) PvSampleTime02_N (Index N = 01 to 15)	DINT	•	•[1)]		
602 + Index*24 1114 + Index*24	PvSampleTime01_N (Index N = 01 to 15) PvSampleTime02_N (Index N = 01 to 15)	INT	•			
562 + Index*4 1116 + Index*24	PvNodeComStatus01_N (Index N = 01 to 15) PvNodeComStatus02_N (Index N = 01 to 15)	UINT		•		
HART - Extended communication						
522 1034	PvCountHartRequest01 PvCountHartRequest02	UINT	•			
530 1042	PvCountHartTimeout01 PvCountHartTimeout02	UINT	•			
538 1050	PvCountHartRxError01 PvCountHartRxError02	UINT	•			
546 1058	PvCountHartFrameError01 PvCountHartFrameError02	UINT	•			
554 1066	PvNodeFound01 PvNodeFound02	UINT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
558 1070	PvNodeError01 PvNodeError02	UINT	●			
FlatStream interface - Configuration						
1793	OutputMTU	USINT				●
1795	InputMTU	USINT				●
1797	FlatstreamMode	USINT				●
1799	Forward	USINT				●
1802	ForwardDelay	UINT				●
FlatStream interface - Communication						
1857	InputSequence	USINT	●			
1857 + Index*2	RxByteN (Index N = 1 to 15)	USINT	●			
1889	OutputSequence	USINT			●	
1889 + Index*2	TxByteN (Index N = 1 to 15)	USINT			●	

1) These HART registers are defined multiple times. Hence, they can be activated acyclically, if they are not registered during the cyclical phase of the X2X transmission.

4.4.3.11.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
386 394	AnalogMode01 AnalogMode02	UINT				●
390 398	DACSlewrate01 DACSlewrate02	UINT				●
Analog signal - Communication						
0 2	AnalogOutput01 AnalogOutput02	(U)INT			●	
30 31	AnalogStatus01 AnalogStatus02	USINT	●			
	OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
	ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
	IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				
HART - Configuration						
1537 1665	HartNodeCnt_1 HartNodeCnt_2	USINT				●
1539 1667	HartMode_1 HartMode_2	USINT				●
1541 1669	HartBurstNode_1 HartBurtNode_2	USINT				●
HART - Extended configuration						
1558 1668	HartNodeDisable_1 HartNodeDisable_2	UINT				●
1546 1674	HartProtTimeOut_1 HartProtTimeOut_2	UINT				●
1550 1678	HartProtRetry_1 HartProtRetry_2	UINT				●
1554 1682	HartPreamble_1 HartPreamble_2	UINT				●
HART - Communication (P2P)						
612 + Index*24 1124 + Index*24	PvInput01_N (Index N = 01 to 04) PvInput02_N (Index N = 01 to 04)	REAL	●	●[1)]		
617 + Index*24 1129 + Index*24	PvUnit01_N (Index N = 01 to 04) PvUnit02_N (Index N = 01 to 04)	USINT	●	●[1)]		
628 1140	PvSampleTime01 PvSampleTime02	DINT	●	●[1)]		
626 1138	PvSampleTime01 PvSampleTime02	INT	●			
566 1078	PvNodeComStatus01 PvNodeComStatus02	UINT		●		
HART - Communication (multidrop)						
612 + Index*24 1124 + Index*24	PvInput01_N (Index N = 01 to 15) PvInput02_N (Index N = 01 to 15)	REAL	●	●[1)]		
617 + Index*24 1129 + Index*24	PvUnit01_N (Index N = 01 to 15) PvUnit02_N (Index N = 01 to 15)	USINT	●	●[1)]		
604 + Index*24 1116 + Index*24	PvSampleTime01_N (Index N = 01 to 15) PvSampleTime02_N (Index N = 01 to 15)	DINT	●	●[1)]		
602 + Index*24 1114 + Index*24	PvSampleTime01_N (Index N = 01 to 15) PvSampleTime02_N (Index N = 01 to 15)	INT	●			
562 + Index*4 1116 + Index*24	PvNodeComStatus01_N (Index N = 01 to 15) PvNodeComStatus02_N (Index N = 01 to 15)	UINT		●		
HART - Extended communication						
522 1034	PvCountHartRequest01 PvCountHartRequest02	UINT	●			

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
530 1042	PvCountHartTimeout01 PvCountHartTimeout02	UINT	●			
538 1050	PvCountHartRxError01 PvCountHartRxError02	UINT	●			
546 1058	PvCountHartFrameError01 PvCountHartFrameError02	UINT	●			
554 1066	PvNodeFound01 PvNodeFound02	UINT	●			
558 1070	PvNodeError01 PvNodeError02	UINT	●			
FlatStream interface - Configuration						
1793	OutputMTU	USINT				●
1795	InputMTU	USINT				●
1797	FlatstreamMode	USINT				●
1799	Forward	USINT				●
1802	ForwardDelay	UINT				●
FlatStream interface - Communication						
1857	InputSequence	USINT	●			
1857 + Index*2	RxByteN (Index N = 1 to 15)	USINT	●			
1889	OutputSequence	USINT			●	
1889 + Index*2	TxByteN (Index N = 1 to 15)	USINT			●	
The OSP function model						
32	OSPComByte	USINT			●	
	OSPValid	Bit 0				
401 403	CfgOSPMode01 CfgOSPMode02	USINT				●
34 36	CfgOSPValue01 CfgOSPValue02	INT				●

1) These HART registers are defined multiple times. Hence, they can be activated acyclically, if they are not registered during the cyclical phase of the X2X transmission.

4.4.3.11.4 Function model 254 - Bus controller

Register	Offset[1]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
386 394	- -	AnalogMode01 AnalogMode02	UINT				•
390 398	- -	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication							
0 2	0 8	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	- -	AnalogStatus01 AnalogStatus02	USINT		•		
		OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
		ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
		IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				
HART - Configuration							
1537 1665	- -	HartNodeCnt_1 HartNodeCnt_2	USINT				•
1539 1667	- -	HartMode_1 HartMode_2	USINT				•
1541 1669	- -	HartBurstNode_1 HartBurtNode_2	USINT				•
HART - Extended configuration							
1558 1668	- -	HartNodeDisable_1 HartNodeDisable_2	UINT				•
1546 1674	- -	HartProtTimeOut_1 HartProtTimeOut_2	UINT				•
1550 1678	- -	HartProtRetry_1 HartProtRetry_2	UINT				•
1554 1682	- -	HartPreamble_1 HartPreamble_2	UINT				•
HART - Communication (P2P)							
636 1148	4 12	PvInput01_01 PvInput02_01	REAL	•			
612 + Index*24 1124 + Index*24	- -	PvInput01_N (Index N = 02 to 04) PvInput02_N (Index N = 02 to 04)	REAL		•		
641 1153	2 10	PvUnit01_01 PvUnit02_01	USINT	•			
617 + Index*24 1129 + Index*24	- -	PvUnit01_N (Index N = 02 to 04) PvUnit02_N (Index N = 02 to 04)	USINT		•		
566 1078	- -	PvNodeComStatus01 PvNodeComStatus02	UINT		•		
HART - Communication (multidrop)							
636 1148	4 12	PvInput01_01 PvInput02_01	REAL	•			
612 + Index*24 1124 + Index*24	- -	PvInput01_N (Index N = 02 to 15) PvInput02_N (Index N = 02 to 15)	REAL		•		
641 1153	2 10	PvUnit01_01 PvUnit02_01	USINT	•			
617 + Index*24 1129 + Index*24	- -	PvUnit01_N (Index N = 02 to 15) PvUnit02_N (Index N = 02 to 15)	USINT		•		
562 + Index*4 1116 + Index*24	- -	PvNodeComStatus01_N (Index N = 01 to 15) PvNodeComStatus02_N (Index N = 01 to 15)	UINT		•		
HART - Extended communication							
522 1034	- -	PvCountHartRequest01 PvCountHartRequest02	UINT		•		
530 1042	- -	PvCountHartTimeout01 PvCountHartTimeout02	UINT		•		
538 1050	- -	PvCountHartRxError01 PvCountHartRxError02	UINT		•		
546 1058	- -	PvCountHartFrameError01 PvCountHartFrameError02	UINT		•		
554 1066	- -	PvNodeFound01 PvNodeFound02	UINT		•		
558 1070	- -	PvNodeError01 PvNodeError02	UINT		•		

1) The offset specifies the position of the register within the CAN object.

4.4.3.11.4.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.4.3.11.5 Analog signal - Configuration

The module has 2 independent electrically isolated channels with integrated HART modems. Both channels can be used to output an analog signal and handle HART communication. Two registers need to be configured for one analog signal. The two channels operate independently, so two registers must be configured per channel to be used.

The current outputs (default: 4 to 20 mA) can be used as conventional analog signals. The integrated HART modems retrieve digital information from the memory on the HART slave using the same physical lines that modulate the HART signals.

Each channel can use one of the following connection variants:

- Point-to-point (connection of one HART node on the channel):
  → Evaluation of the analog signal
  and
  → Recording of up to 4 HART values
- Multidrop (connection of up to 15 HART nodes on the channel):
  → Recording of one HART value per connected node

Specific features

- Electrical isolation by channel
- Up to 4 or 15 HART input variables per channel
- Configurable output rate (DAC slew rate) to transfer HART and analog signal without interference (default: 210 ms full scale)
- Selectable error strategy (static replacement value or retention of the last permitted value)
- Cyclic "HART status" polling (HART command 0), the status information received is made available for channel diagnostics
- Compatible with an additional secondary master in the HART network (module acts as the primary master)
- "HART communication error bit" (shows loss of HART connection if a connection had already been established successfully)
- Optional: BURST mode for one node per channel
- Optional: Cyclic polling of "HART variables" (HART command 3 or 9)
- Optional: FlatStream functionality (module acts as bridge for HART packets)

4.4.3.11.5.1 AnalogMode

Name:
AnalogMode01 to AnalogMode02

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be activated and configured separately.

Information:

When you select the operating mode "Scaling 0 to 20 mA (Resolution 0 to 65535)", then the corresponding "AnalogOutput" registers are interpreted internally as UINT instead of INT.
The entire program must be rebuilt for the data type change to take effect. The data type cannot be changed during runtime (e.g. using a library).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel	0	Disabled
		1	Enabled (bus controller default)
1	Check - DAC configuration/status	0	Enabled (bus controller default)
		1	Disabled
2 - 3	Reserved	-	
4	Scaling 0 to 20 mA (Resolution 0 to 32767)	0	Disabled
		1	Enabled
5	Scaling 4 to 20 mA (Resolution 0 to 32767)	0	Disabled
		1	Enabled (bus controller default)
6	Scaling 0 to 24 mA (Resolution 0 to 24000)	0	Disabled
		1	Enabled
7	Scaling 0 to 20 mA (Resolution 0 to 65535)	0	Disabled
		1	Enabled
8 - 15	Reserved	-	

Information:

The "AnalogMode" registers provide the option of avoiding the cyclic check of the DAC configuration. To manage communication reliably, this option should only be used if no HART communication is taking place on the channel.

4.4.3.11.5.2 DACSlewrate

Name:
DACSlewrate01 to DACSlewrate02

These registers limit the rate at which the analog signal is modified. This makes it possible to define a sort of upper limit frequency.

The following formula applies: f(Analog) = f(Output rate) * Permitted change / max. ∆(standardized output value)

Data type	Value
UINT	See bit structure

To ensure communication takes place without errors, it's important that the frequency range of the digital HART signal is not influenced by the analog output. HART communication takes place in the frequency range 950 to 2500 Hz.

Example (default): f(Analog) = 152440 Hz * 4 / (32767 - 0)
Conclusion: f(Analog) = ~**20 Hz << 950 Hz** = f(HART)

Bit structure:

Bit	Name	Value	Information
0 - 2	Permitted change per rate	000	1-bit
		001	2-bit
		010	4 bit (bus controller default)
		011	8-bit
		100	16-bit
		101	32-bit
		110	64-bit
		111	128-bit
3 - 7	Reserved	-	
8 - 11	Output rate	0000	257730 Hz
		0001	198410 Hz
		0010	152440 Hz (bus controller default)
		0011	131580 Hz
		0100	115740 Hz
		0101	69440 Hz
		0110	37590 Hz
		0111	25770 Hz
		1000	20160 Hz
		1001	16030 Hz
		1010	10290 Hz
		1011	8280 Hz
		1100	6900 Hz
		1101	5530 Hz
		1110	4240 Hz
		1111	3300 Hz
12 - 14	Reserved	-	
15	Slewrate enable (ramp functionality)	0	Disabled (undefined jump behavior)
		1	Enabled (defined transitions)

4.4.3.11.6 Analog signal - Communication

In order to output the required current signal (default: 4 bis 20 mA), the module must be assigned the default output value (default: 0 to 32767). In this way, the X20AO2438 can be used as a conventional output module. The integrated HART modem uses the same physical line. Using signals with a higher frequency allows the module to communicate with and also retrieve information from the HART slave.

4.4.3.11.6.1 AnalogOutput

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Depending on the scaling selected (see AnalogMode register), the value range and the data type can be adapted to the requirements of the application. Once a permitted value is determined, the module outputs the respective current.

Information:

The value "0" disables the channel status LED.

Data type	Value	Information
INT	0 to 32767	Bus controller default: 0
Optional: UINT	0 to 65535	

4.4.3.11.6.2 AnalogStatus

Name:
AnalogStatus01 to AnalogStatus02

The status register gives the user feedback about whether the respective channel is functioning properly.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	-	
2	OpenLineAnalogOutput01, 02	0	Line OK
		1	Open line
3	ConversionErrorAnalogOutput01, 02	0	Conversion temperature OK
		1	Conversion temperature too high
4 - 6	Reserved	-	
7	IoSuppErrorAnalogOutput01, 02	0	Module supply OK
		1	Module supply error

4.4.3.11.7 HART

HART (Highway Addressable Remote Transducer) is a protocol for communicating with intelligent field devices. It was developed in order to more efficiently use the infrastructure for transferring analog signals. The digital HART notifications are modulated to the analog signal using Frequency Shift Keying (FSK). HART can thus use the same physical line as the analog signal without influencing the original function.
HART slaves are able to determine different process data independently and prepare HART concordantly. This protocol supports polling of the value of a process variable as well as its unit and status. Field devices usually supply their information after the master requests it. In newer revisions, it is also possible to transfer configuration data.

There are two different types of HART networks. In a *point-to-point* network, only one slave is connected to a HART master. Here, the analog signal and the HART signal can be transferred over the same line. Managing several slaves with HART requires what is known as a *multidrop* network. Here, each HART slave is assigned and identified by a unique address. Classic analog signals cannot be clearly traced in bus systems. As a result, the HART protocol does not support analog information transfers in multidrop networks up to and including HART Revision 5.

Information:

Split range operation with HART AO modules

Beginning with HART revision 6, bus stations that use an analog signal according to the split range method are written to separately. The HART protocol supports multidrop addressing as well as the use of analog signals for these applications.

The module was designed based on HART-Revision 5. Only single-channel FSK scheme is available for transmitting the signals.

Since all HART frames are generated and evaluated in the application when using the FlatStream interface, information that isn't specified until later revisions can also be read.

4.4.3.11.7.1 HART - Configuration

HART modules are analog modules equipped with a HART modem. For each channel, a separate HART network can be managed by the module, which acts as a primary master. Once configured successfully, the HART information is stored in the module where it can then be used by the PLC.

The number of HART slaves must be specified in the configuration.
If only one slave is connected to the HART channel, then it is part of a point-to-point network. The module can then prepare up to four process variables from the connected slave.
Multidrop mode allows up to 15 HART slaves to be connected. The primary process variable from each slave is then retrieved.

HartNodeCnt

Name:
HartCodeCnt_1 to HartCodeCnt_2

These registers tell the module how many HART slaves are connected to a channel.

Information:

If a slave is not connected to one of the HART channels, the value "0" should be defined in this register. This shortens the I/O update time and avoids superfluous error messages.

Data type	Value	Information	
USINT	0	HART communication disabled for this channel	
	1	Point-to-point	Standard HART communication (bus controller default)
	2 to 15	Multidrop	Number of HART slave nodes

HartBurstNode

Name:
HartBurstNode_1 to HartBurstNode_2

In addition to the type of network, the user can also choose from two different types of communication behavior. Conventional HART communication relies on polling. The module requests the data from the individual HART slaves and receives the corresponding information from each slave as a response. If a HART node should be queried in short time intervals, the user can configure burst mode for channels on one node. In this case, the slave transmits the node's information cyclically without constant prompting from the master.
The "HartBurstNode" registers are therefore used to enter the node numbers (short address) for the channels whose information should be retrieved using burst mode. Burst mode itself is enabled with the "HartMode" register.

Data type	Value	Information	
USINT	0 to 15	Point-to-point	0 (bus controller default)

HartMode

Name:
HartMode_1 to HartMode_2

The user can use these registers to configure the communication behavior of each of the HART channels. Generally, the HART nodes are polled individually. This register can still be used to start or stop burst mode when needed. In burst mode, a node transmits its information cyclically instead of continuously. As a result, the HART standard allows the simultaneous usage of both burst mode and polling.

Information:

To retrieve information with burst mode, theHartBurstNode register must be configured correctly.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Slave polling mode	0	Polling mode enabled (Bus Controller Default)
		1	Polling mode disabled
1	Start slave burst mode	0	No response to burst (bus controller default)
		1	Enables burst mode in the HartBurstNode node
2	Stop slave burst mode	0	No response to burst (bus controller default)
		1	Disables burst mode, if enabled
3 - 7	Reserved	-	

4.4.3.11.7.2 HART - Communication

Once the configuration has been completed, the information is retrieved automatically and transferred to the module's registers. A separate register in the module is implemented for each piece of information. HART modules are designed to retrieve up to 15 pieces of information per channel. The module reads in the data, stores it in temporary memory and prepares it for retrieval. When the X2X master accesses the module registers, it is irrelevant whether the HART data originates from a point-to-point network or a multidrop network.

Overview of internal module mapping

	Point-to-point network (1 HART slave)	*Multidrop network (2 to 15 HART slaves)*
(Pv)Input_01	Primary piece of information from HART node 1	Primary piece of information from HART node 1
(Pv)Input_02	Secondary piece of information from HART node 1	Primary piece of information from HART node 2
...	...	...
(Pv)Input_04	Quaternary piece of information from HART node 1	Primary piece of information from HART node 4
(Pv)Input_05	Reserved	Primary piece of information from HART node 5
...	...	...
(Pv)Input_15	Reserved	Primary piece of information from HART node 15

The HART specifications stipulates that information from a HART node be split into various pieces. The value of a process variable is stored to the respective "PvInput" register and has a size of 4 bytes (REAL) in accordance with the HART specification. Due to the length limitation of 30 bytes on the X2X link, there are restrictions to the number of possible cyclic variables. It is recommended to only transfer a maximum of 2 "PvInput" registers cyclically to the X2X master. All other information should be transferred in a different way. To access HART information, the user can choose from among the following methods:

- Data points that are configured to be transferred cyclically are read once per bus cycle. This method allows information to be exchanged between the module and the X2X master in real time. Nevertheless, the length limitation may prevent all data from being retrieved within one cycle.
- If the AsIOAcc library is used, information is retrieved acyclically only when it is needed, i.e. communication can be adapted to the application running on the X2X master. In this way, all of the necessary module registers on the X2X link can be polled despite the length limitation.
  This method of information exchange is not real-time capable.
- HART modules are equipped with a FlatStream interface. When using FlatStream communication, the module acts a bridge between the X2X master and the HART slave, i.e. the X2X master communicates directly with the HART slave (see section "FlatStream communication""FlatStream communication").
  FlatStream communication is also not real-time capable. It allows unrestricted access to the HART slave. The user must have sufficient knowledge of the HART protocol command set as well as the capabilities of the HART slave device.

PvInput

Name:
PvInput_01 to PvInput_15
PvInput_01_01 to PvInput_01_15
PvInput_02_01 to PvInput_02_15

These registers return the current value of the process variable that has been read.

Information:

These registers are of data type REAL, which means that the available bytes on the X2X Link are filled more quickly when operated cyclically. If information from several slave nodes is needed, it must be retrieved acyclically or using Flatstream .

Data type	Value	Information
REAL	IEEE745 SPF	32-bit data type with valid value
	0x7FA00000	Not a number (NaN) with invalid value

PvUnit

Name:
PvUnit_01 to PvUnit_15
PvUnit_01_01 to PvUnit_01_15
PvUnit_02_01 to PvUnit_02_15

These registers return a HART-specific code that specifies the unit for the measured value. The coding for this is established in the HART specification.

Data type	Value
USINT	See description of the HART slave See HART specification

PvSampleTime

Name:
PvSampleTime01 to PvSampleTime02
PvSampleTime01_01 to PvSampleTime01_15
PvSampleTime02_01 to PvSampleTime02_15

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	Information
INT	-32,768 to 32767	Nettime timestamp of the current input value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current input value

This refers to the point in time when the HART master receives the slave's response. This is a way to check whether new HART information has been read since the last X2X cycle.

Information:

The cycle times of a HART network are relatively long so that it is not possible to reliably determine when the measured value is retrieved with just this information.

PvNodeComStatus

Name:
PvNodeComStatus01 to PvNodeComStatus02
PvNodeComStatus01_01 to PvNodeComStatus01_15
PvNodeComStatus02_01 to PvNodeComStatus02_15

These registers return information about whether a value that has been read is valid. According to the HART specification, this type of status register consists of two parts. The high byte stores the "response code" and the low byte the "field device status". This makes it possible to check the current status of a read process variable.

These registers can be checked before further processing information in temporary storage. If the current value is 0x0000, an error was not detected during the HART transfer and the information from the checked node can be used. If a different value is present, the situation in the HART network should be checked. This can be done using an extension register, for example.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Quality - Node information 2 to n	0	Digital measured value okay
		1	Measured value outside the permitted range
1	Quality - Node information 1	0	Digital measured value okay
		1	Measured value outside the permitted range
2	Limit violation	0	Parameter okay
		1	Invalid measured value(s) or encoder supply value
3	Static analog signal	0	Normal value change/fluctuation
		1	Constant analog value of Node 1 slave
4	Additional status information (only supported by a few slaves)	0	Not available
		1	Available (only using Flatstream command #48)
5	Restart	0	Normal operation
		1	Field device restarts
6	Device ID	0	Unchanged
		1	Changed
7	Device error	0	Measured value okay
		1	Questionable measured value information
8 - 14	Response code, if relevant	x	See **HART-specific response code**
15	Error - Communication	0	Error-free communication (response code irrelevant)
		1	Faulty communication (response code relevant)

HART-specific response code (excerpt):

0x82 … Receive buffer overflow 0x88 … Checksum incorrect 0x90 … Faulty protocol structure 0xA0 … Overrun 0xC0 … Parity not allowed 0xFF … Timeout	If a HART communication error occurs, the response code is written. Bit 15 is always set.

Retrieving information that has been read

After the node data has been transferred to the module registers, the information can be retrieved from the module. A separate register in the module is implemented for each piece of information.

PvCountHartRequest

Name:
PvCountHartRequest01 to PvCountHartRequest02

These registers are increased once the module is ready to transmit a message to the corresponding channel.

Data type	Value
UDINT	0 to 4,294,967,295

PvCountHartTimeout

Name:
PvCountHartTimeout01 to PvCountHartTimeout02

These registers are increased if the slave exceeds the maximum permitted time before responding to the module's request.

Data type	Value
UDINT	0 to 4,294,967,295

PvCountHartRxError

Name:
PvCountHartRxError01 to PvCountHartRxError02

These registers are increased if communication errors occur on Layer 1 of the OSI model (e.g. transmission error as per parity bit).

Data type	Value
UDINT	0 to 4,294,967,295

PvCountHartFrameError

Name:
PvCountHartFrameError01 to PvCountHartFrameError02

These registers are increased if communication errors occur on Layer 2 of the OSI model (e.g. faulty telegram structure).

Data type	Value
UDINT	0 to 4,294,967,295

PvNodeFound

Name:
PvNodeFound01 to PvNodeFound02

These registers provide information about which nodes were detected on which channel (slave identified successfully).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
1	Node 2 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
...		...	
13	Node 14 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
14	Node 15 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
15	Reserved	-	

PvNodeError

Name:
PvNodeError01 to PvNodeError02

These registers contain the HART communications error bits. These bits are set if the connection to a node was established successfully but the node at some point no longer responds as it should (e.g. the HART slave exceeds the configured timeout / number of retries).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
1	Node 2 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
...		...	
13	Node 14 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
14	Node 15 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
15	Reserved	-	

4.4.3.11.7.3 Extended configuration

The additional configuration registers are specified values when the module is started. In most systems, the user does not need to make any adjustments here. Register values should only be changed if HART network communication is not taking place satisfactorily.

HartNodeDisable

Name:
HartNodeDisable_1 to HartNodeDisable_2

These registers are intended for things like maintenance. They make it possible to cut off configured HART nodes to suppress error messages for a certain period of time. During normal operation, the configured nodes must be switched active to guarantee that the procedure runs smoothly.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Enabled (bus controller default setting)
		1	Disabled
1	Node 2 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default)
...		...	
13	Node 14 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default)
14	Node 15 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default)
15	Reserved	-	

HartProtTimeOut

Name:
HartProtTimeOut_1 to HartProtTimeOut_2

These registers specify the time span within which the slave must respond for the response to be valid.

Data type	Values [ms]	Information
UINT	0 to 65535	Bus controller default: 256 [ms]

HartProtRetry

Name:
HartProtRetry_1 to HartProtRetry_2

These registers determine how many times the master retries a request if it receives an invalid response or no response at all.

Data type	Value	Information
UINT	0 to 65535	Bus controller default: 3 attempts

HartPreamble

Name:
HartPreamble_1 to HartPreamble_2

The length of the preamble can be set in these registers. The preamble is used to synchronize the receiver to the transmitter. The longer the declared preamble, the less chance that a communication error will occur. Nevertheless, a useful signal is not transmitted during synchronization so the preamble should be kept as short as possible.

Data type	Value	Information
UINT	5 to 20	Bus controller default: 20

4.4.3.11.8 FlatStream communication

4.4.3.11.8.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

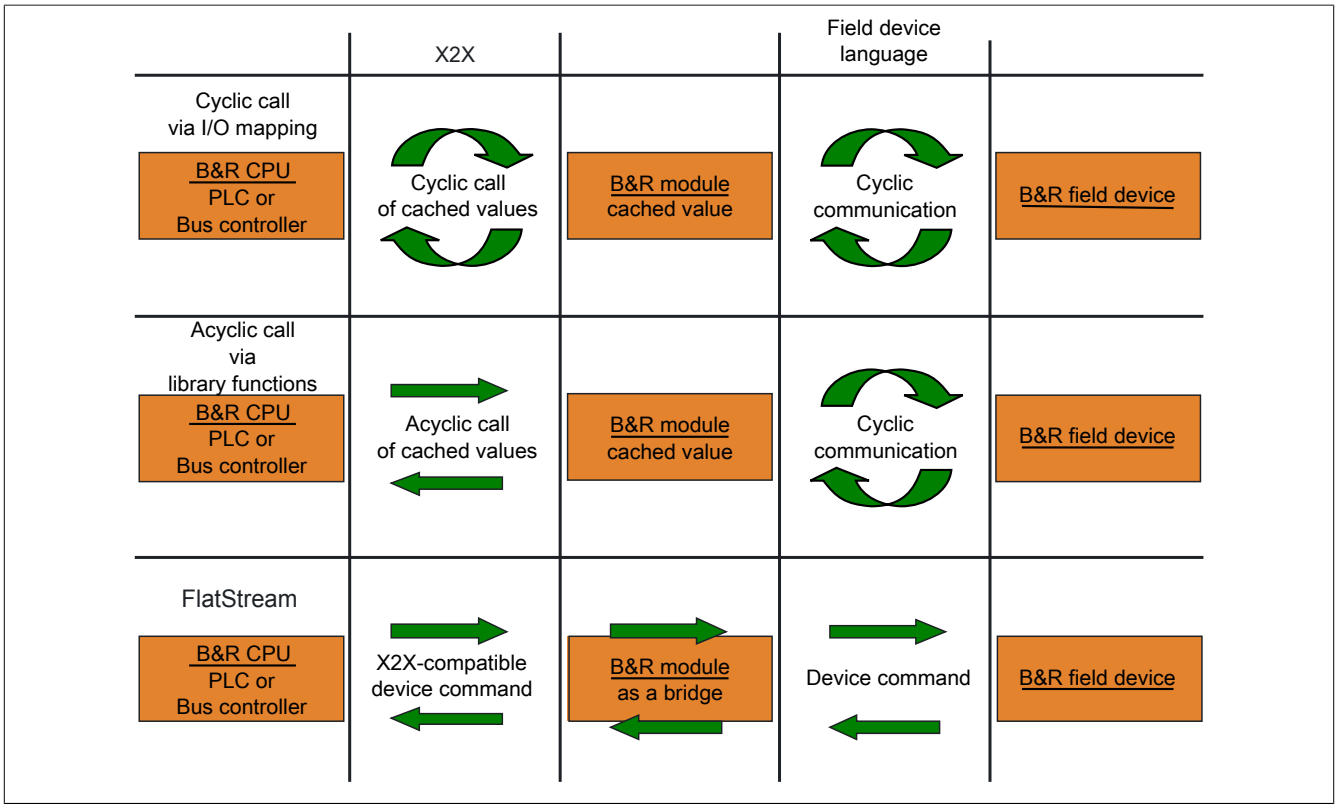


Figure 140: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.4.3.11.8.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.4.3.11.8.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

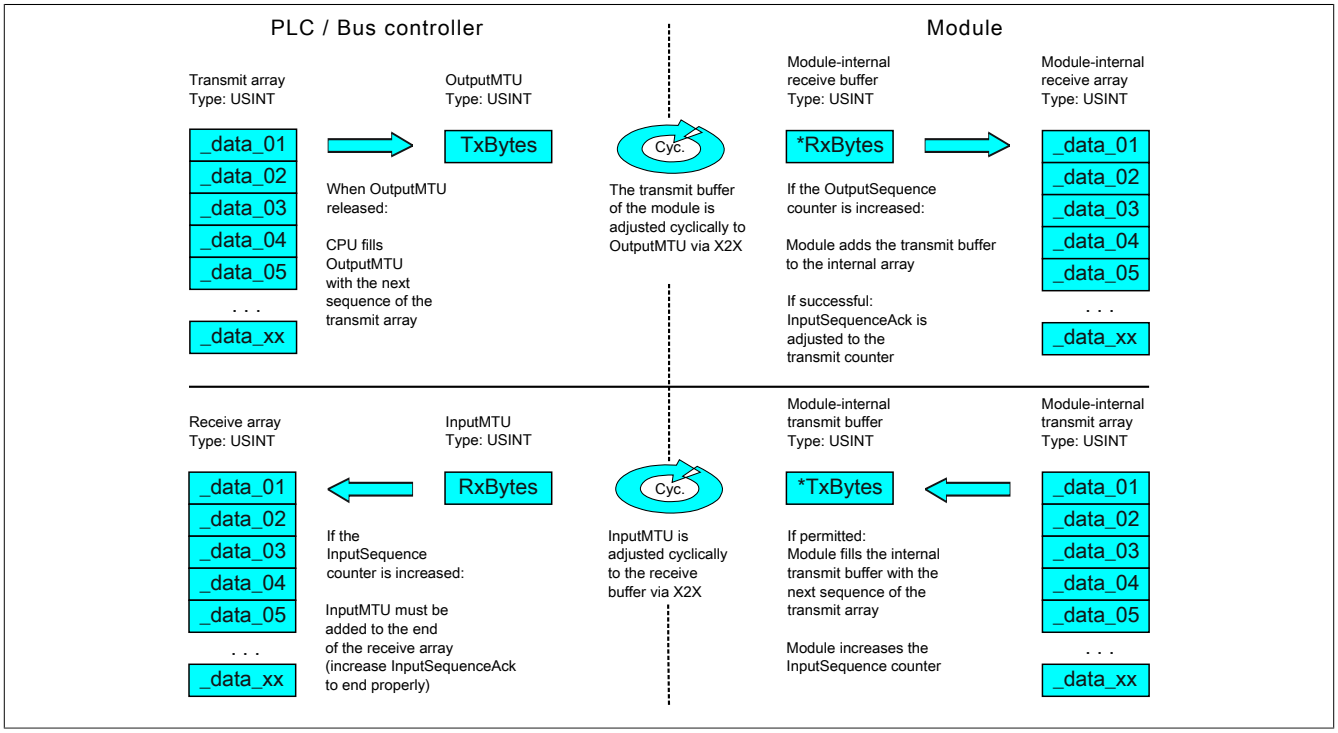


Figure 141: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.4.3.11.8.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

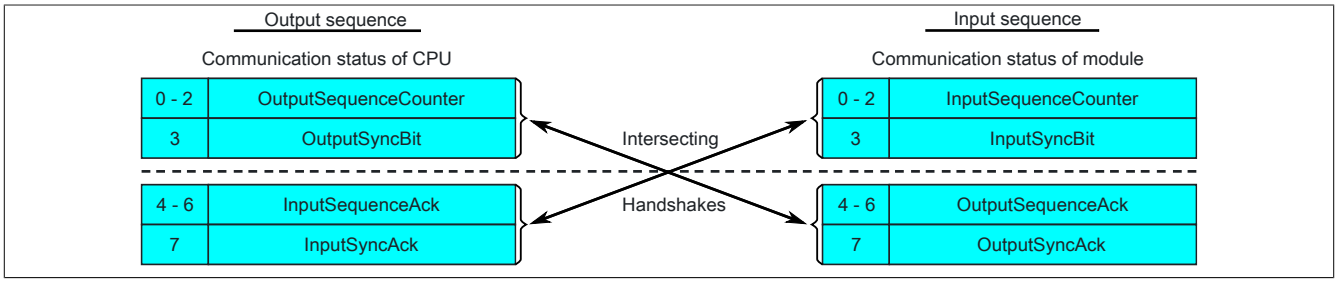


Figure 142: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

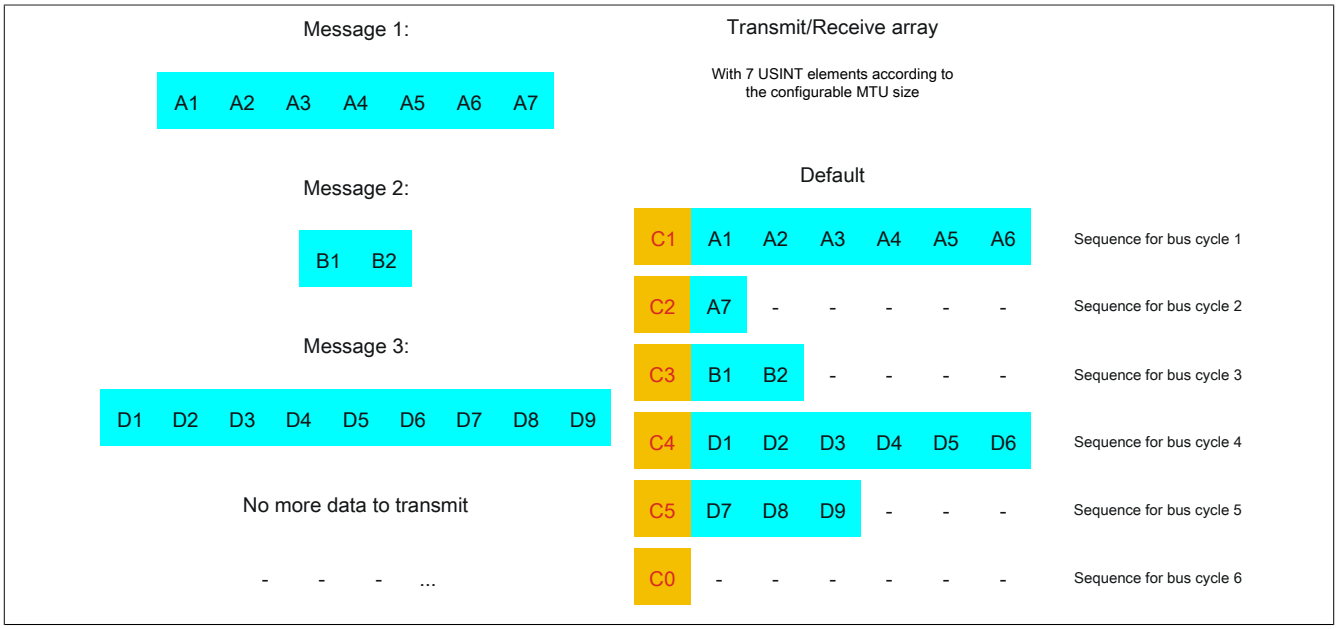


Figure 143: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 84: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 85: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

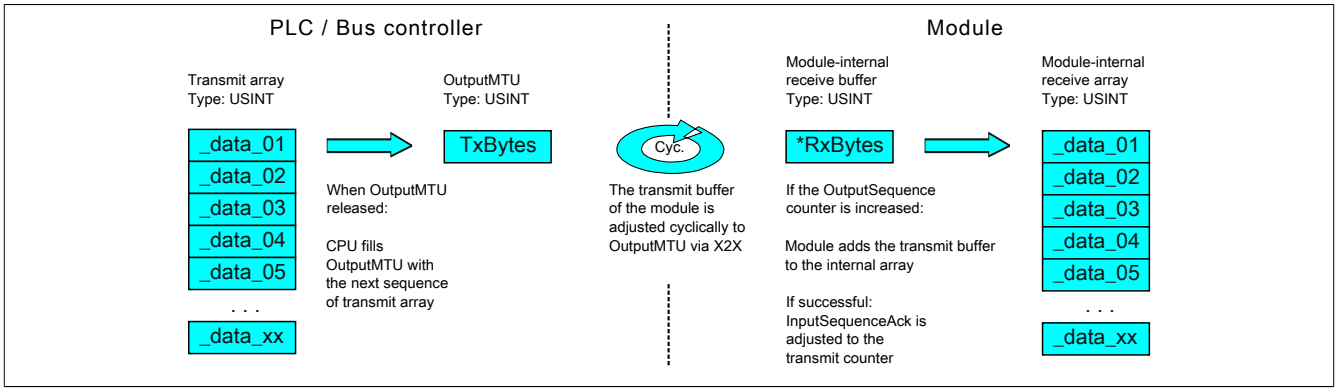


Figure 144: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

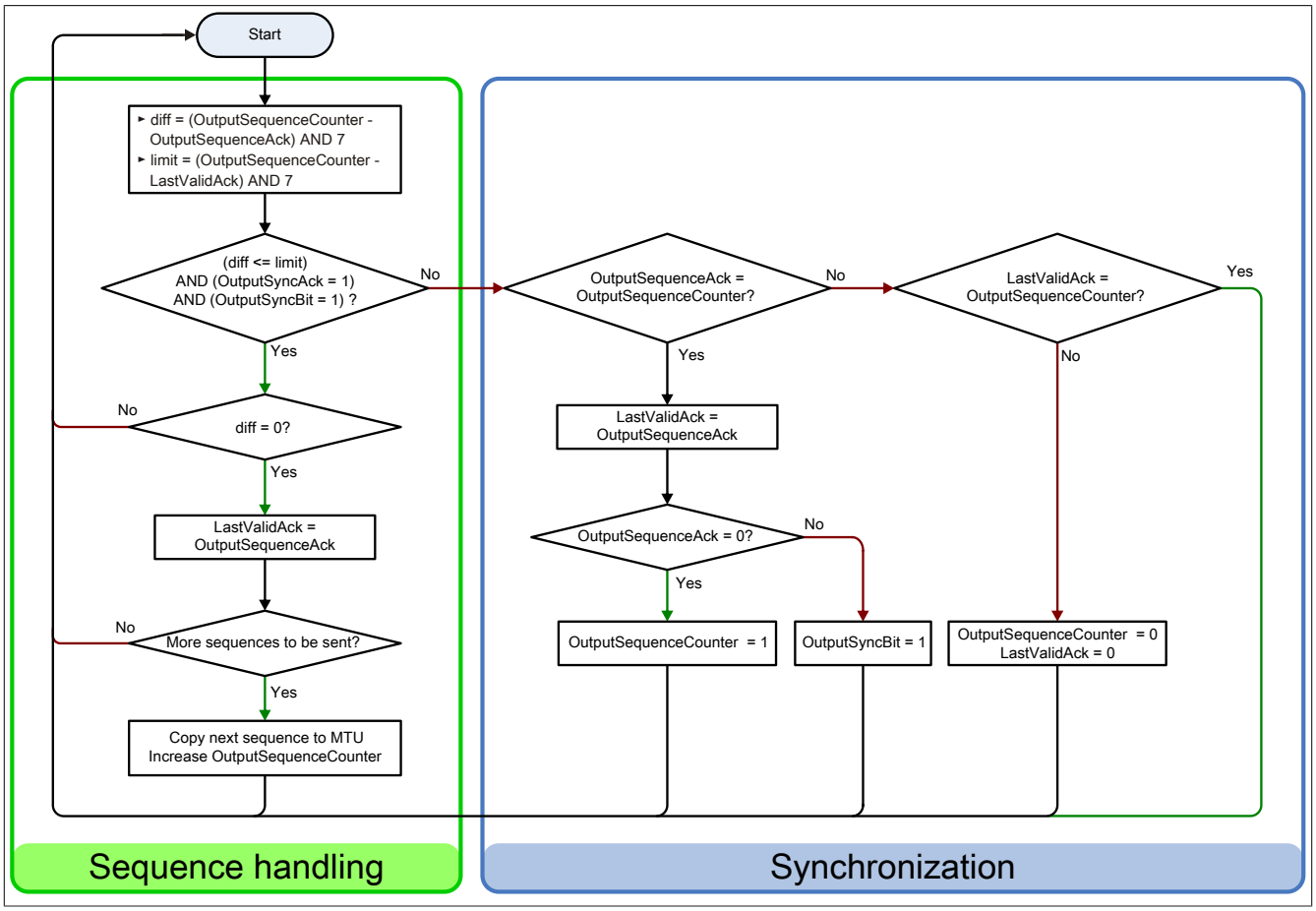


Figure 145: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

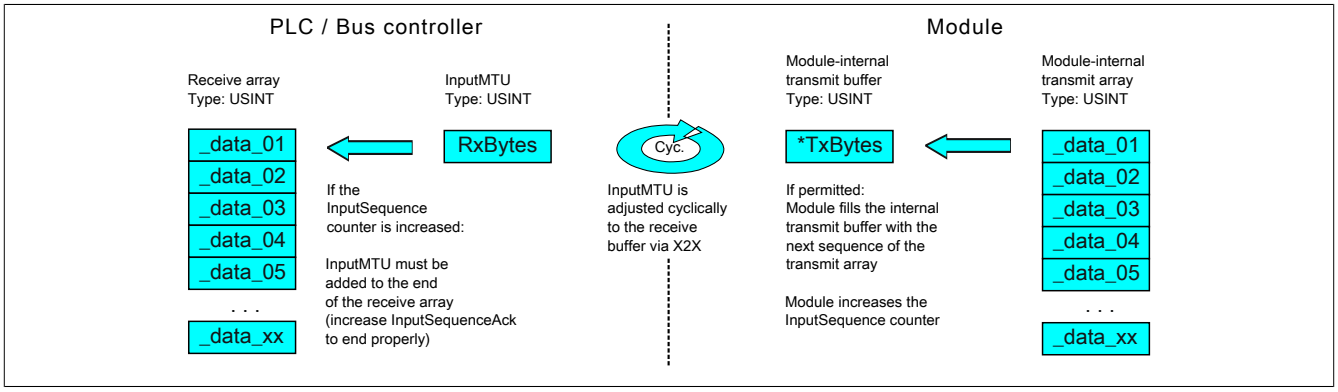


Figure 146: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

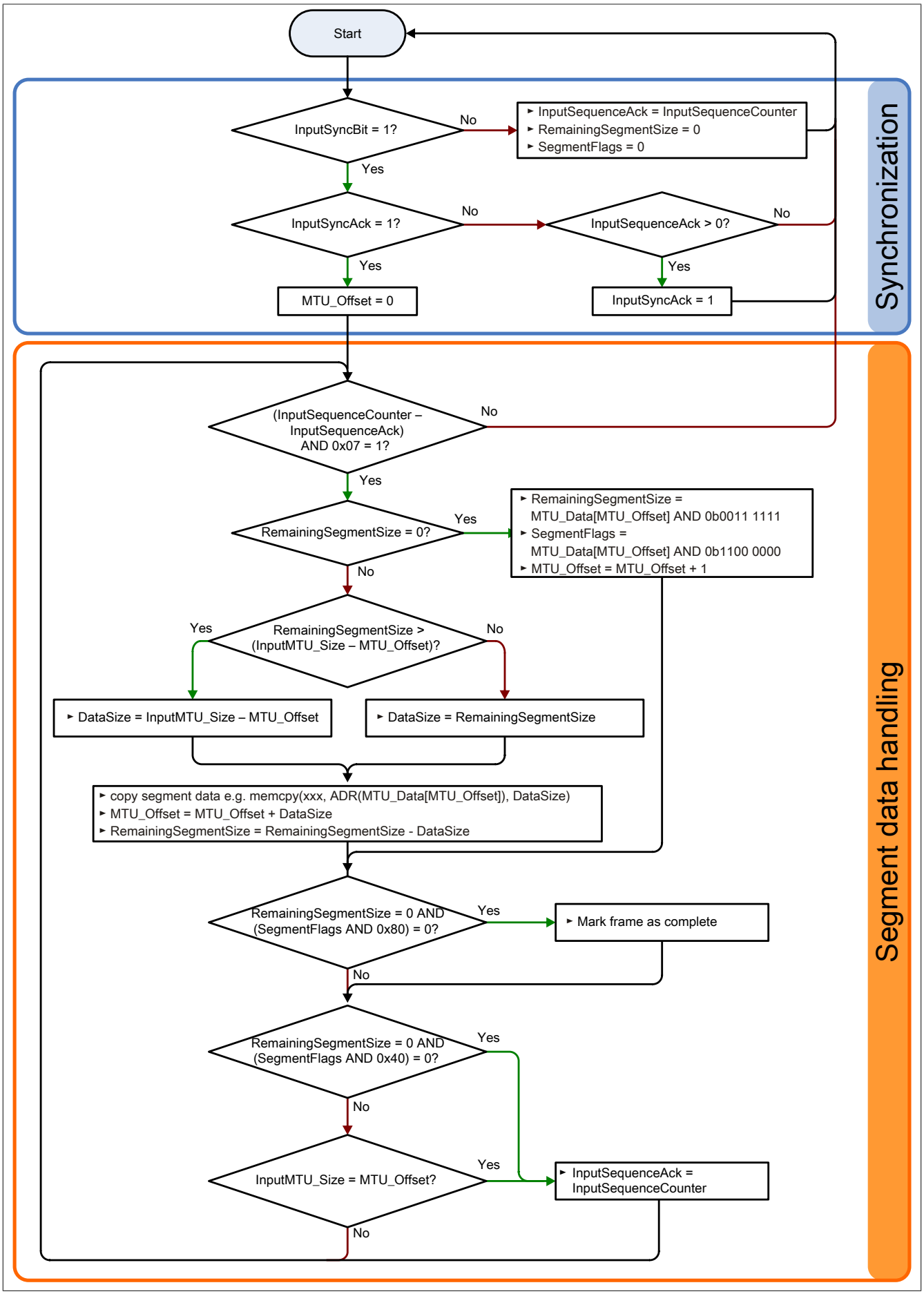


Figure 147: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

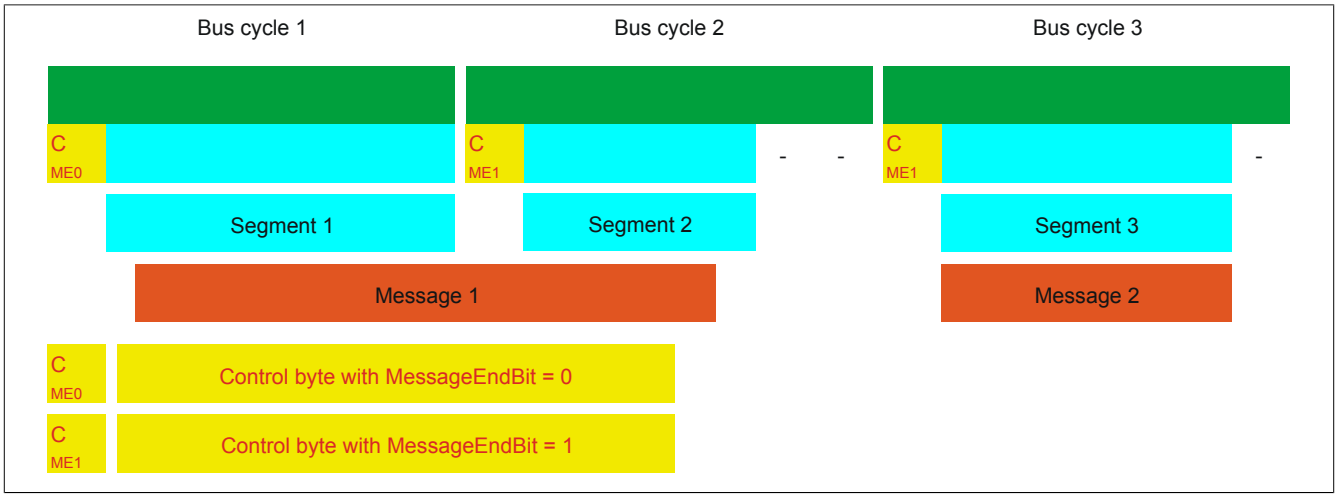


Figure 148: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

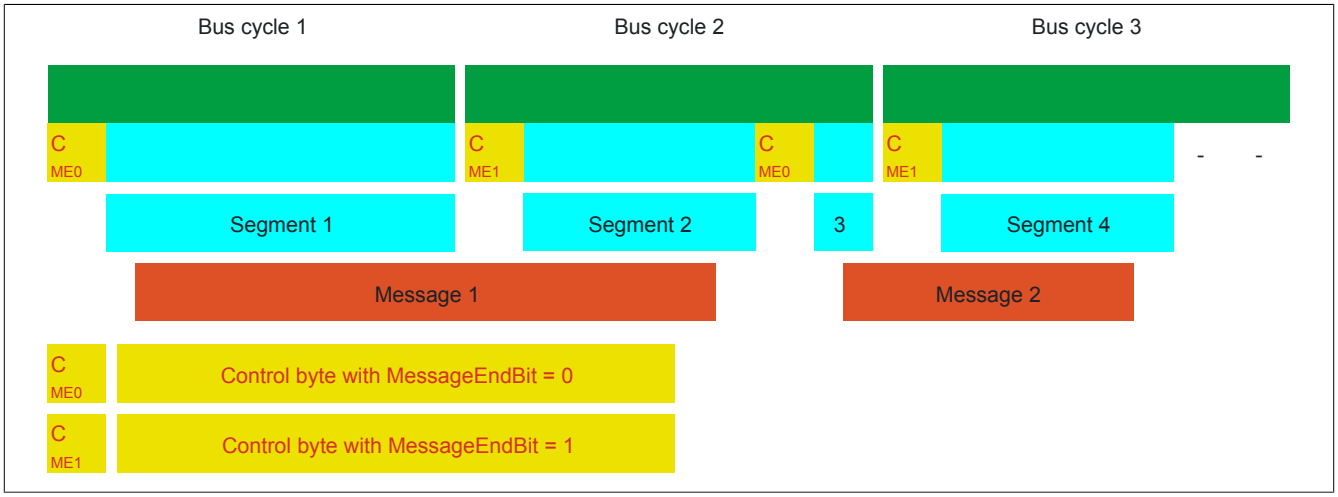


Figure 149: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

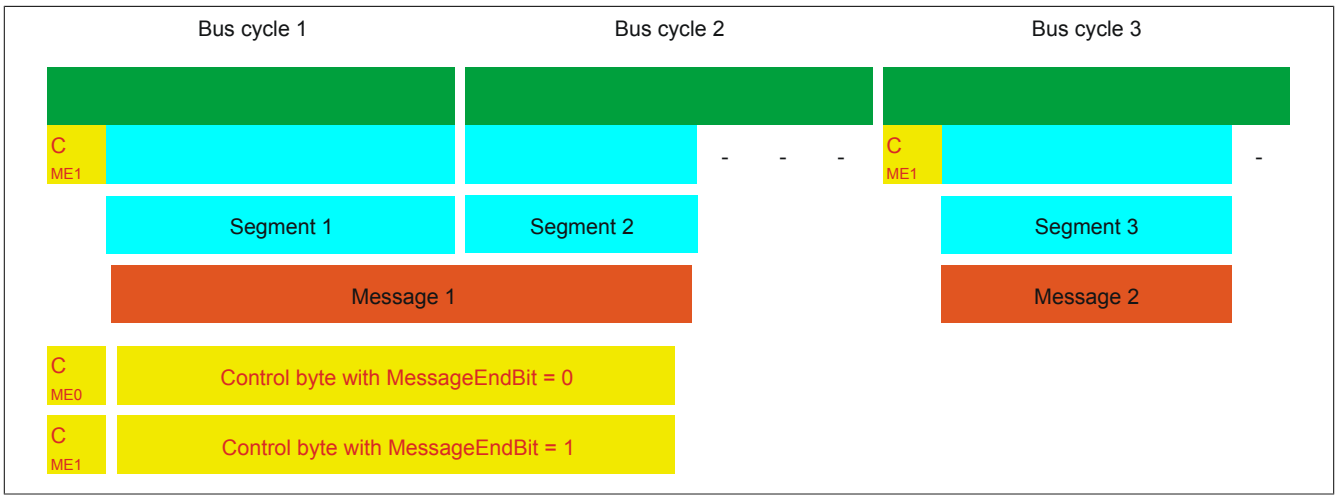


Figure 150: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

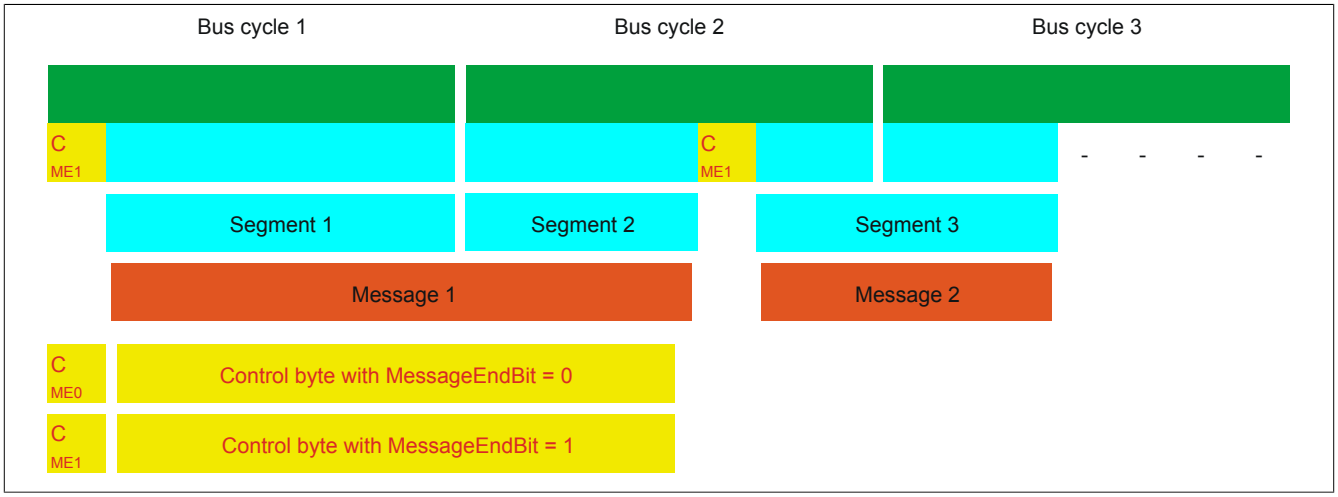


Figure 151: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

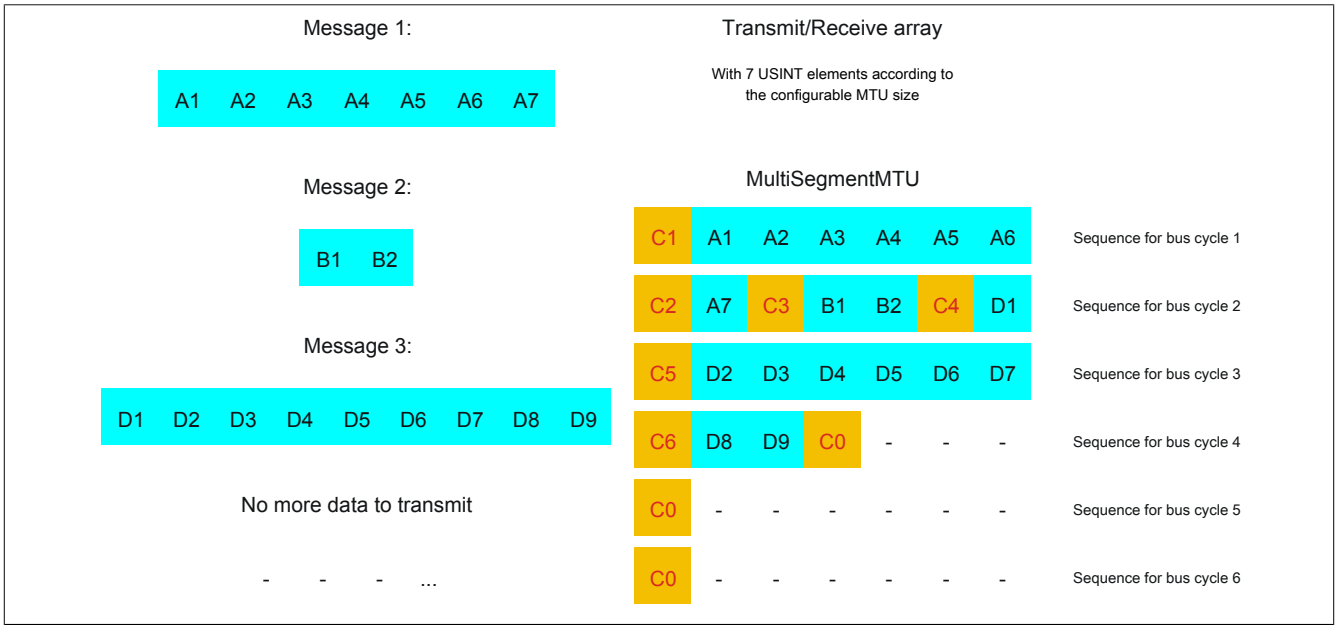


Figure 152: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 86: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 87: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

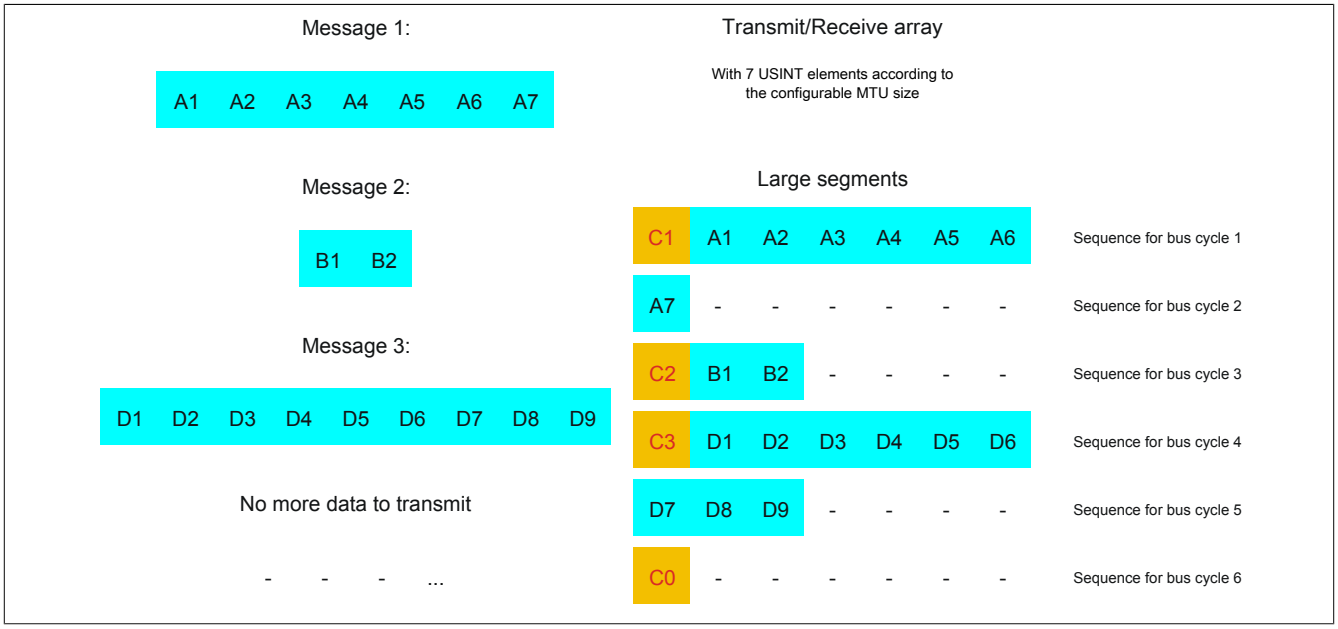


Figure 153: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 88: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

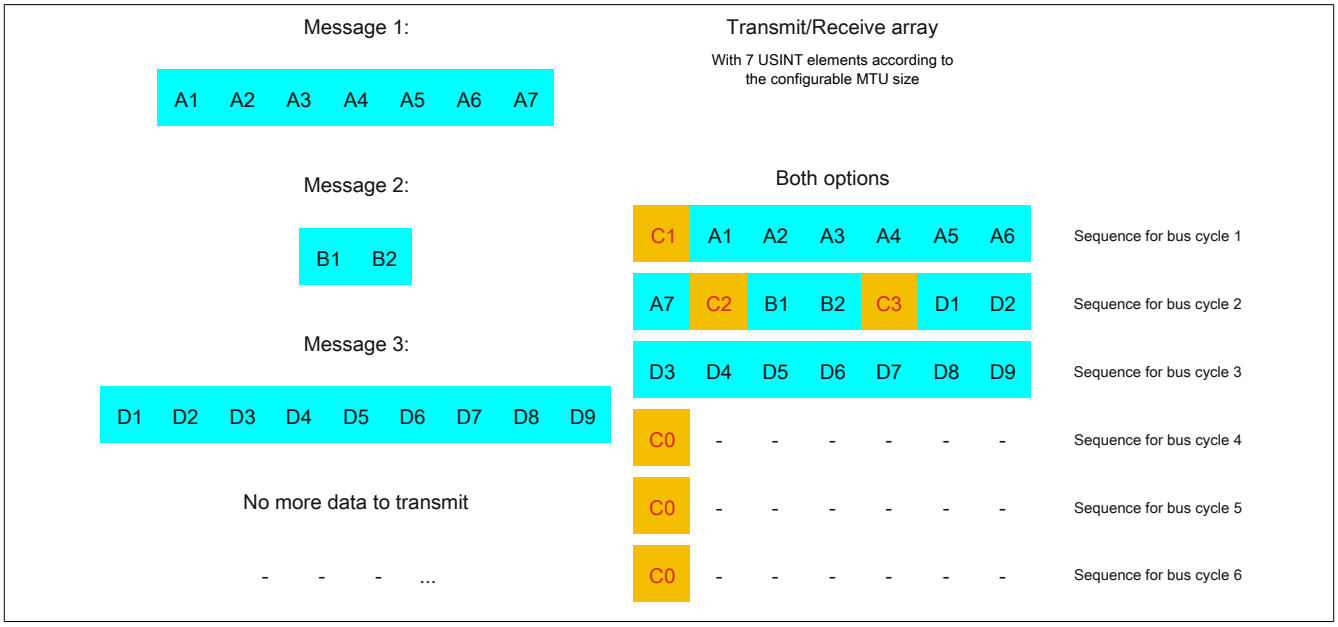


Figure 154: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 89: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.4.3.11.8.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

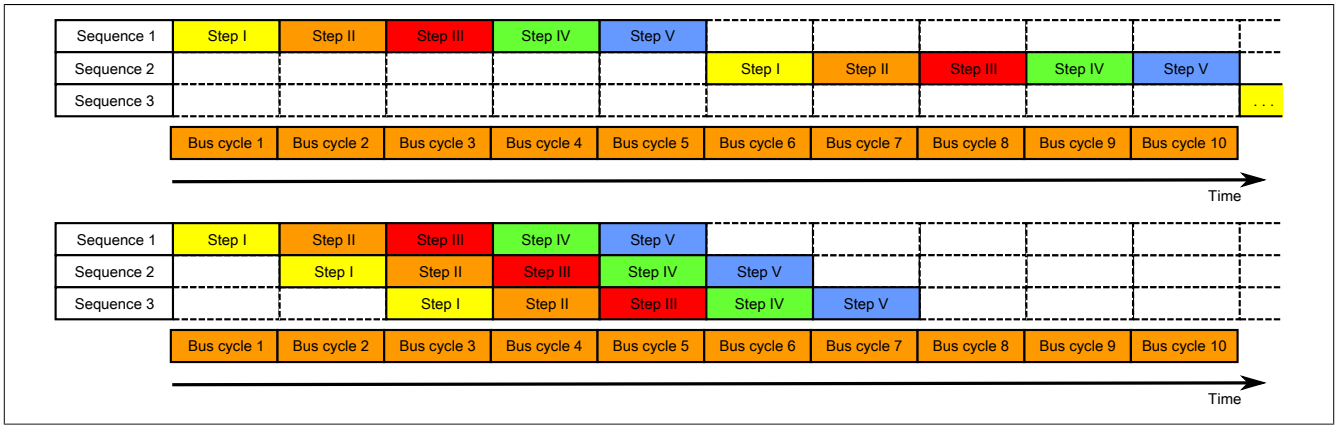


Figure 155: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

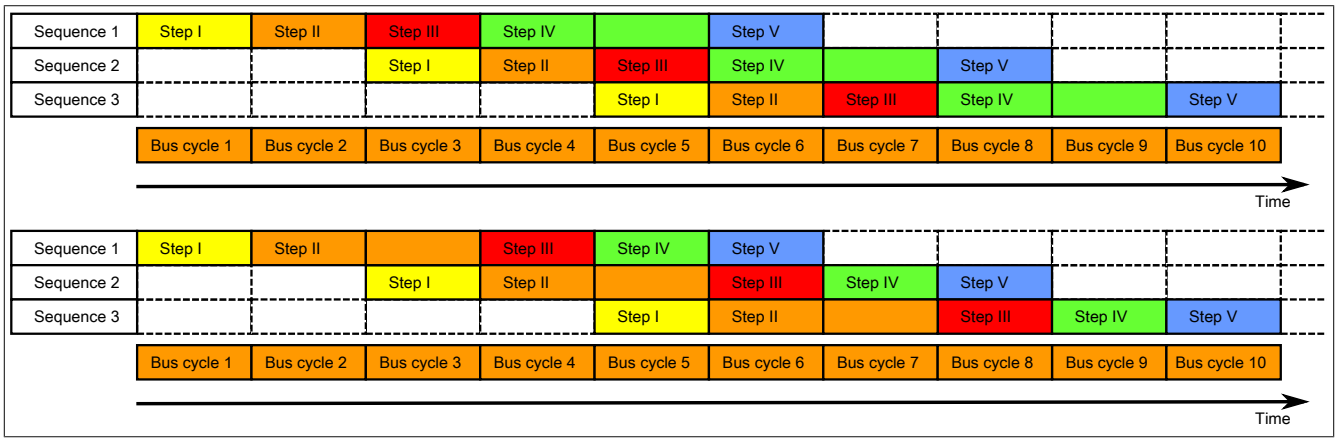


Figure 156: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

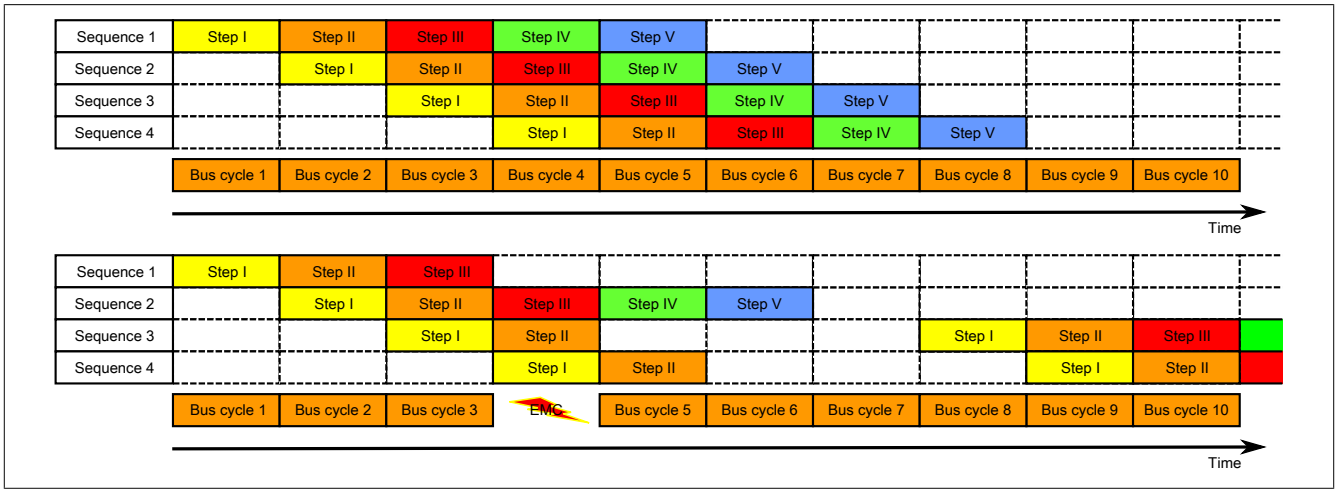


Figure 157: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.4.3.11.9 HART with Flatstream

When using Flatstream communication, the module acts as a bridge between the X2X master and an intelligent field device connected to the module. Flatstream mode can be used for either point-to-point connections as well as for multidrop systems. Specific algorithms such as timeout and checksum monitoring are usually managed automatically. During normal operation, the user does not have access to these details.

HART is considered a master-slave network where half-duplex communication takes place asynchronously. Various features have been included to ensure that signals are transmitted without errors.
For example, the user can increase the length of the preamble, thus making the transmission more secure. However, this also has an effect on the percentage of payload data and overhead.

Additional information about HART can be found at www.HARTcomm.org.

How it works

The module has two independent channels. When using Flatstream , the channel number must therefore be specified. The general structure of a Flatstream frame is extended as follows.

Input/Output sequence	Tx/Rx bytes		
(unchanged)	Control byte (unchanged)	Channel number	HART frame (without preamble and checksum)

HART frame with Flatstream					
Startup	ADDR	CMD	BCNT	(STS)	(DATA)

Startup	Start identification
ADDR	Address within the HART network
CMD	HART command
BCNT	Byte counters (number of remaining bytes)
*STS	Status of the last command received. Information about the working mode of the HART Slave and communication errors (if supported, return data from the HART Slave)
*DATA	Data (if necessary for the command)

Examples of HART commands

Command	Function
0x00	Read slave ID
0x03	Read current value and up to four variables
0x09	Read up to four variables including status
0x21	Read variables

4.4.3.11.10 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.4.3.11.10.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the relevant task in the master CPU. However, an output still occurs depending on the configuration of the OSP replacement value.

4.4.3.11.10.2 Setting the OSP mode

Name:
CfgOSPMode01 to CfgOSPMode02

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.4.3.11.10.3 Define the OSP analog output value

Name:
CfgOSPValue01 to CfgOSPValue02

This register contains the analog output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
Corresponds to AnalogOutput0x	Corresponds to AnalogOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.4.3.11.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.4.3.11.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Analog outputs	1 ms

Minimum I/O update time Hart Communication	
Point-to-point	500 ms
Multidrop	Number of stations * 1000 ms

4.4.4 X20AO2622

4.4.4.1 General information

The module is equipped with two outputs with 13-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog outputs
- Either current or voltage signal possible
- 13-bit digital converter resolution

4.4.4.2 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO2622	X20 analog output module, 2 outputs, ±10 V / 0 to 20 mA / 4 to 20 mA, 13-bit resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 90: X20AO2622 - Order data

4.4.4.3 Technical data

Product ID	X20AO2622
Short description	
I/O module	2 analog outputs ±10 V or 0 to 20 mA / 4 to 20 mA [1]
General information	
B&R ID code	0x1BA2
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Analog outputs	
Output	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections [1]
Max. output current	10 mA at voltages >5 V 15 mA at voltages <5 V
Digital converter resolution	
Voltage	±12-bit
Current	12 Bit
Conversion time	200 µs for all outputs
Settling time for output changes over entire range	1 ms
Power on/off behavior	Internal enable relay for booting
Max. error at 25°C	
Voltage	
Gain	0.150% [2]
Offset	0.050% [3]
Current	
Gain	0.150% [2]
Offset	0.050% [3]
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0010 = 4.882 mV
Current	INT 0x8001 - 0x7FFF / 1 LSB = 0x0010 = 9.766 µA
Load per channel	
Voltage	Max. ±10 mA, load ≥1 kΩ
Current	Load max. 600 Ω (Rev. ≥ J0); 500 Ω (Rev. < J0)
Short circuit protection	Current limiting ±40 mA
Output filter	1st-order low pass / cutoff frequency 10 kHz
Max. gain drift	
Voltage	0.020 %/°C [2]
Current	0.020 %/°C [2]
Max. offset drift	
Voltage	0.032 %/°C [3]
Current	0.032 %/°C [3]
Error caused by load change	
Voltage	Max. 0.11%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.50%, from 1 Ω → 600 Ω, resistive
Non-linearity	<0.007% [4]
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20

Table 91: X20AO2622 - Technical data

Product ID	X20AO2622
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 91: X20AO2622 - Technical data

1) 4 to 20 mA: From upgrade version 1.0.2.0 or hardware revision "I0"
2) Based on the current output value.
3) Based on the entire output range.
4) Based on the output range.

4.4.4.4 LED status indicators

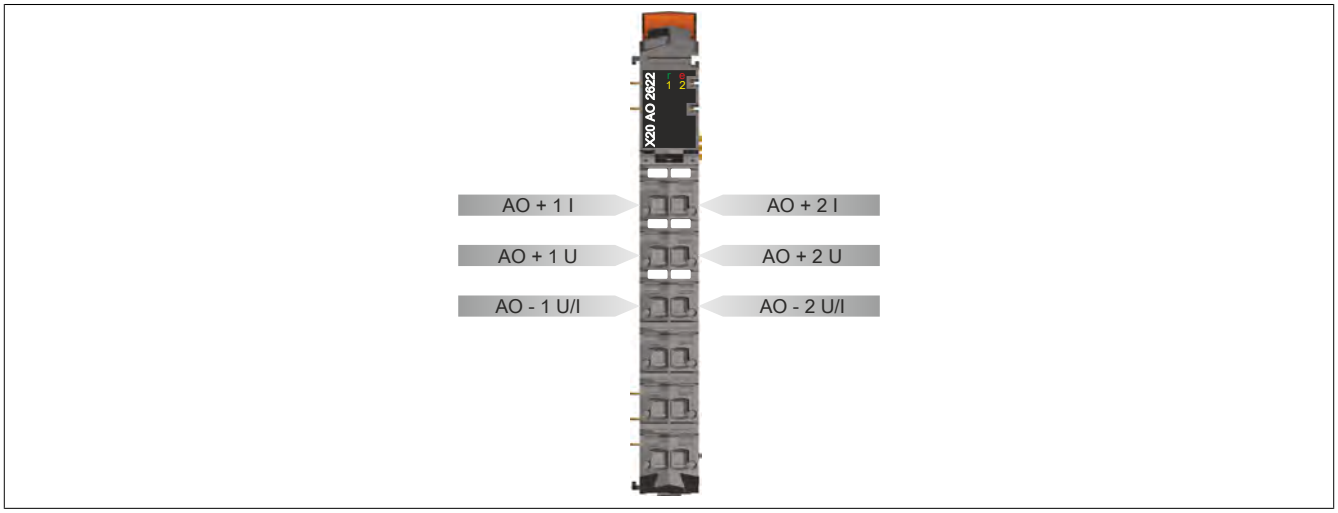
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Orange	Off	Value = 0
			On	Value ≠ 0

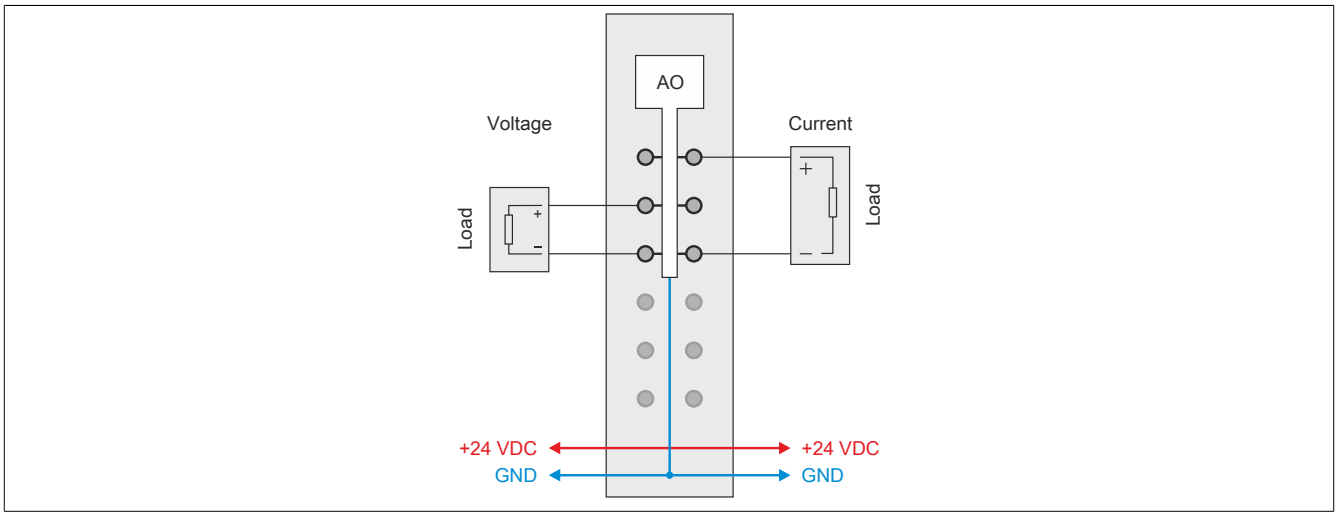
1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.4.5 Pinout

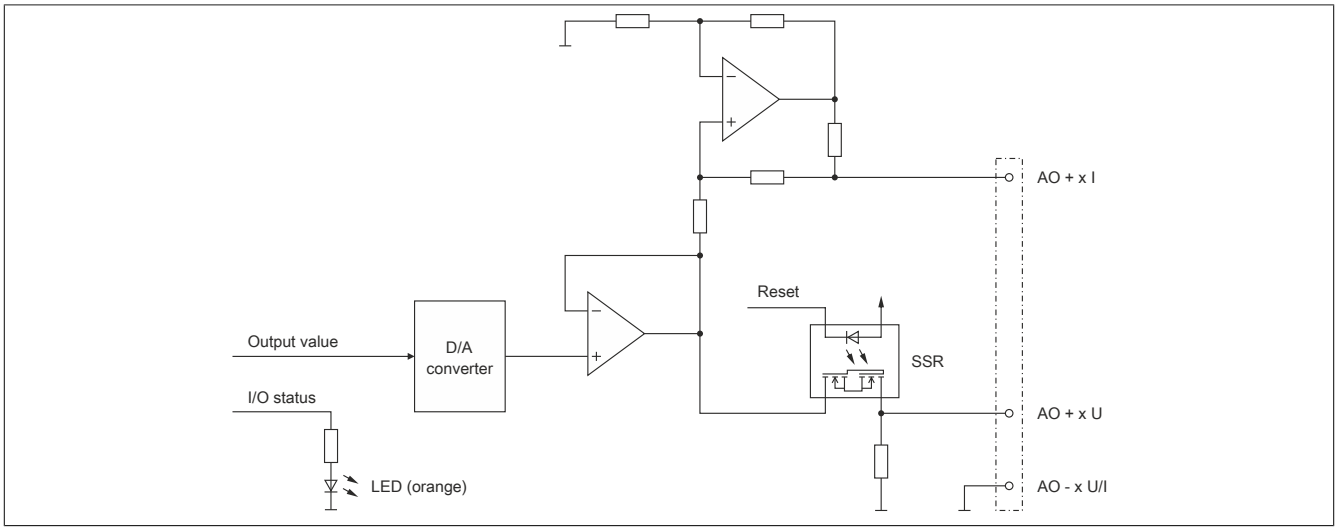
Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.



4.4.4.6 Connection example



4.4.4.7 Output circuit diagram



4.4.4.8 Register description

4.4.4.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.4.8.2 Function model 0 - Standard and function model 1 - I/O with fast reaction

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
18	ConfigOutput01	USINT				•
Communication						
0	AnalogOutput01	INT			•	
2	AnalogOutput02	INT			•	

4.4.4.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration							
18	-	ConfigOutput01	USINT				•
Communication							
0	0	AnalogOutput01	INT			•	
2	2	AnalogOutput02	INT			•	

1) The offset specifies the position of the register within the CAN object.

4.4.4.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.4.4.8.4 Function model comparison

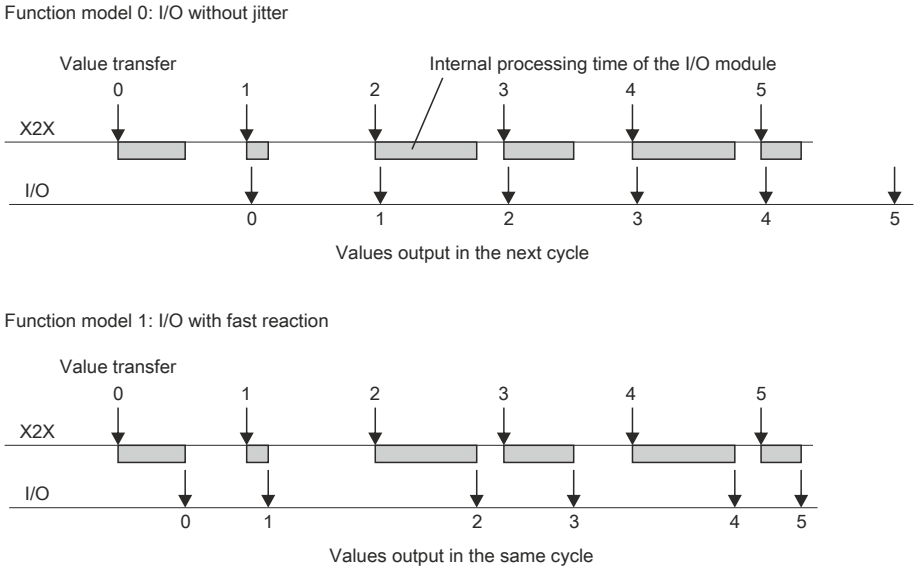
Function model 0: I/O without jitter (standard)

Corrected values are output in the next cycle if the minimum cycle is ≥300 µs in order to reduce jitter to a minimum.

Function model 1: I/O with fast reaction

Corrected values are output in the same cycle if the minimum cycle is ≥300 µs (optimized reactions).

Comparison of the two function models



4.4.4.8.5 Analog outputs

Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.

4.4.4.8.5.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Once a permitted value is received the module outputs the respective current or voltage.

Data type	Value	Information
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA
	0 to 32767	Current signal 4 to 20 mA[1)]

1) From upgrade version 1.0.2.0 or hardware revision "I0"

4.4.4.8.5.2 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel 1	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 4
1	Channel 2	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 5
2 - 3	Reserved	0	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
6 - 7	Reserved	0	

4.4.4.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

4.4.4.8.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
300 µs

4.4.5 X20AO2632

4.4.5.1 General information

The module is equipped with two outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog outputs
- Either current or voltage signal possible
- 16-bit digital converter resolution

4.4.5.2 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO2632	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 92: X20AO2632 - Order data

4.4.5.3 Technical data

Product ID	X20AO2632
Short description	
I/O module	2 analog outputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0x1BA4
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog outputs	
Output	±10 V or 0 to 20 mA, via different terminal connections
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all outputs
Settling time for output changes over entire range	500 µs (Rev. <H0: 1 ms)
Power on/off behavior	Internal enable relay for booting

Table 93: X20AO2632 - Technical data

Product ID	X20AO2632
Max. error at 25°C	
Voltage	
Gain	0.045% 2)
Offset	0.025% 3)
Current	
Gain	0.09% 2)
Offset	0.045% 3)
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Load per channel	
Voltage	Max. ±10 mA, load ≥1 kΩ
Current	Load max. 600 Ω (Rev. ≥ J0); 500 Ω (Rev. < J0)
Short circuit protection	Current limiting ±40 mA
Output filter	1st-order low pass / cutoff frequency 10 kHz
Max. gain drift	
Voltage	0.015 %/°C 2)
Current	0.02 %/°C 2)
Max. offset drift	
Voltage	0.013 %/°C 3)
Current	0.013 %/°C 3)
Error caused by load change	
Voltage	Max. 0.11%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive
Nonlinearity	<0.007% 4)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 93: X20AO2632 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Based on the current output value.
3) Based on the entire output range.
4) Based on the output range.

4.4.5.4 LED status indicators

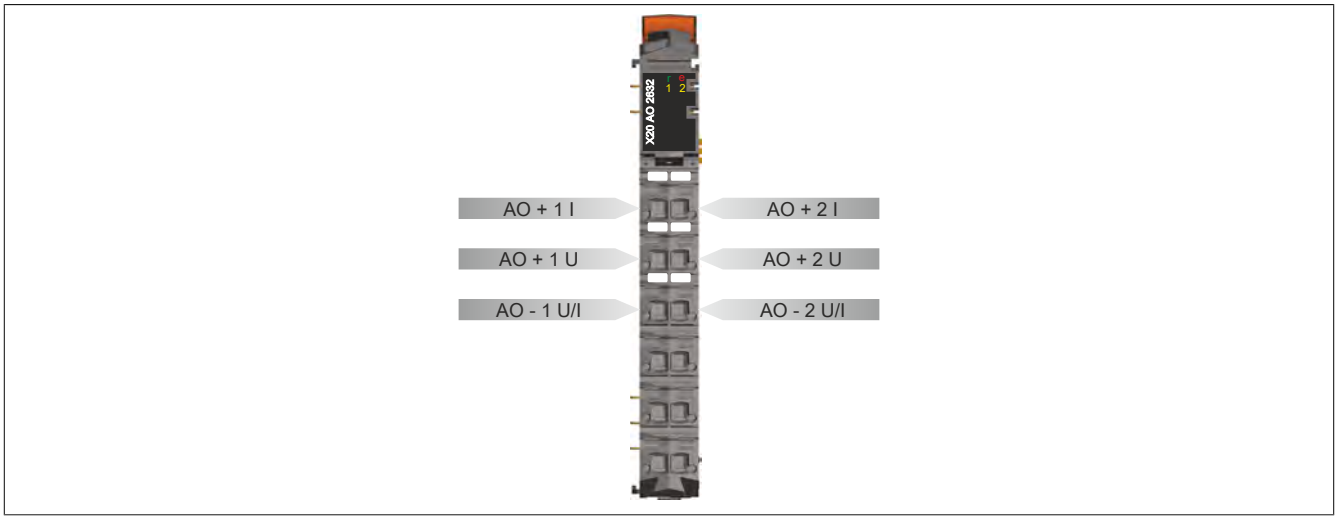
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 2	Orange	Off	Value = 0
			On	Value ≠ 0

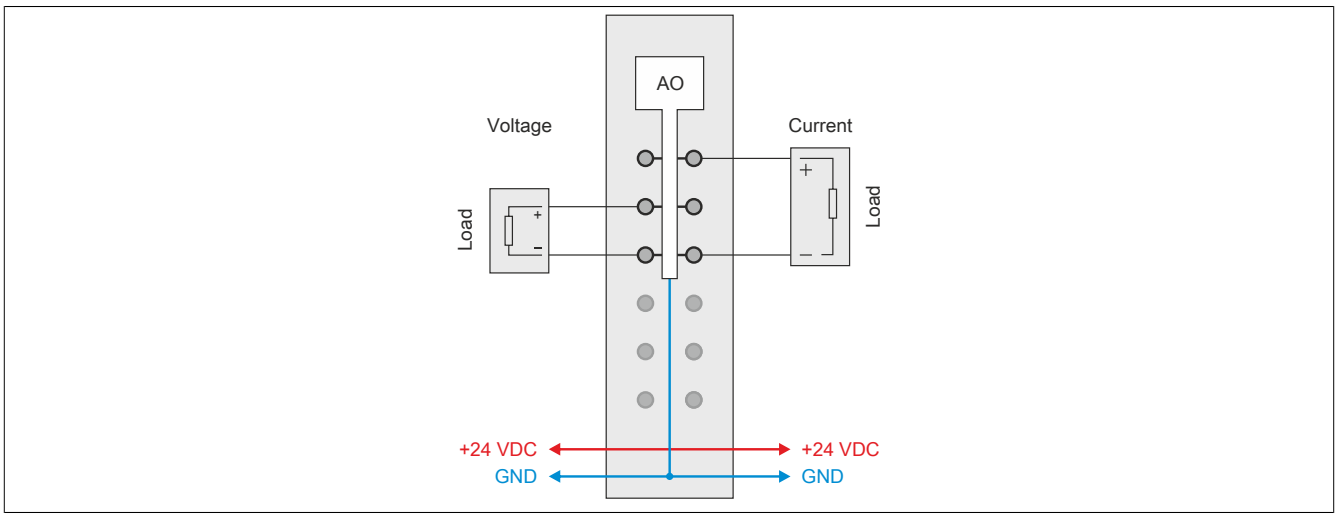
1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.5.5 Pinout

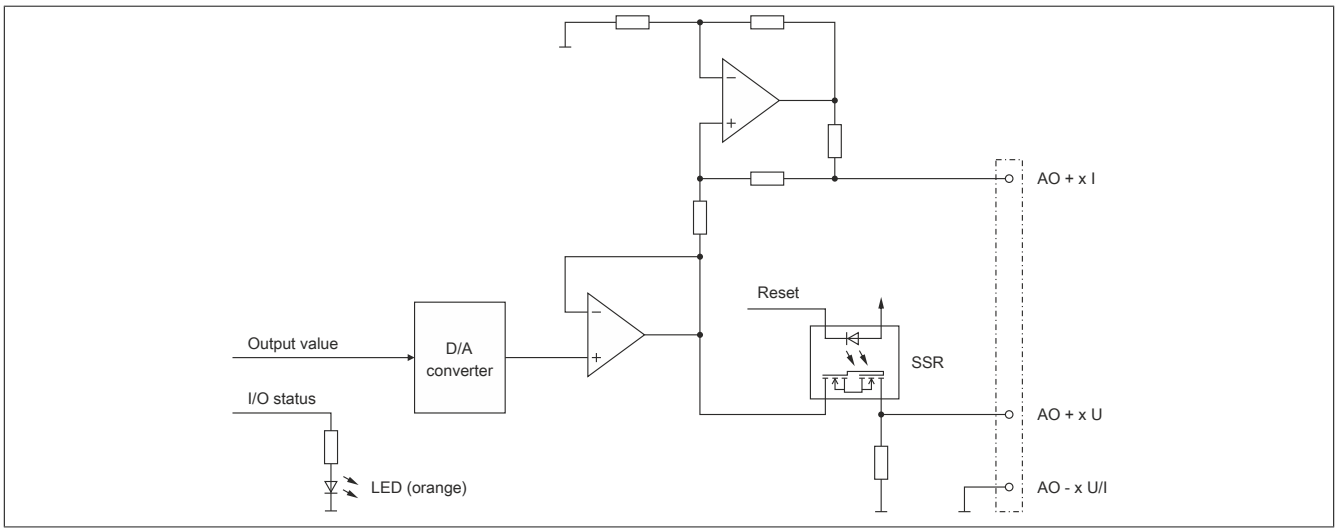
Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.



4.4.5.6 Connection example



4.4.5.7 Output circuit diagram



4.4.5.8 Register description

4.4.5.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.5.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration						
0	ConfigOutput01	UINT				•
594 598	Cfo_Channel01TimeMode Cfo_Channel02TimeMode	UINT				•
Analog output - Communication						
2 4	AnalogOutput01 AnalogOutput02	INT			•	
457	SDCLifeCount	SINT	•			
802 810	ValidationTimer01 ValidationTimer02	INT			•	
804 812	ValidationTimer01 ValidationTimer02	DINT			•	
833	Enabling/disabling the output channels	USINT	•		•	
	AnalogOutput01Enable, ~Readback	Bit 0				
	AnalogOutput02Enable, ~Readback	Bit 1				
835	Checking the output values	USINT	•			
	AnalogOutput01OK	Bit 0				
	AnalogOutput02OK	Bit 1				

4.4.5.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration							
0	-	ConfigOutput01	UINT				•
Analog output - Communication							
2 4	0 2	AnalogOutput01 AnalogOutput02	INT			•	

1) The offset specifies the position of the register within the CAN object.

4.4.5.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.4.5.8.4 General information

The module provides two analog outputs. Each channel can output a voltage range of ±10 V or a current range of 0 to 20 mA.

The module also has a time-based watchdog monitor. The user can activate this feature channel-by-channel as needed.

4.4.5.8.5 Analog output - Configuration

Each channel is configured independently. The user can also define an optional time-based monitor. To make this possible, two watchdog timers were implemented, which can be assigned to the outputs.

4.4.5.8.5.1 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal
		1	Current signal
9	Channel 2	0	Voltage signal
		1	Current signal
10 - 15	Reserved	0	

4.4.5.8.5.2 Configuring the time-based watchdog monitor

Name:
Cfo_Channel01TimeMode to Cfo_Channel02TimeMode

This register is used to activate or configure the time-based watchdog monitor for the analog output channels.

Possibilities per channel:

- Validation timer data type: General choice 16 or 32 bit
- Validation window: The maximum value can be further limited within the data type.
- Timer allocation: A separate timer is available for each channel. However, all channels can be configured with the same validation timer, whereby the same settings must be made for the data type and window in the TimeMode registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 4	Max. validation time	00000	Disabled
		00001	2 µs
		00010	4 µs
		00011	8 µs
		...	...
		11111	2,147,483,648 µs (~35 min)
5 - 7	Reserved	0	
8	Timer allocation	0	ValidationTimer01 (default for channel 1)
		1	ValidationTimer02 (default for channel 2)
9 - 14	Reserved	0	
15	Time format	0	16-bit
		1	32-bit

4.4.5.8.6 Analog output - Communication

In standard mode, the module's outputs are enabled. Based on the configuration and AnalogOutput value, they output the corresponding current or voltage.

If the application requires time-based monitoring of the outputs, then a validation timer can be assigned to each channel. The validation timer register assigns a validity duration to the current output value. When validation is enabled, the module compares the validation time with the Nettime of the X2X Link. If the transferred validity duration is exceeded, the module disables the channel and resets the output. The "safety shutdown" state will not be reset until a new and valid validation time has been transferred. If enabled, the module reports which state it is currently in via the channel's error status bit.

If the value of the validation timer is incremented in each task cycle, the valid validation time will be calculated as follows:

Nettime of the X2X Link master (which the module is connected to)	
+	Timespan for transferring data from the X2X Link master to the CPU (higher-level system)
+	Cycle time of task class (including tolerance)
+	Timespan for transferring the data from the CPU to the module
+	Timespan allowed by the application (e.g. for tolerating failure of an X2X Link cycle)
=	Valid validation time

The AnalogOutputEnableByte is enabled during time-based monitoring. If the timer expires prematurely, the corresponding bit in the AnalogOutputOkayByte is reset and the output drops out. This provides an easy way to achieve a defined state.

4.4.5.8.6.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage; Bus controller default setting: 0
	0 to 32767	Current

4.4.5.8.6.2 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.4.5.8.6.3 Transfer of the timestamp

Name:
ValidationTimer01 to ValidationTimer02

When an output is being monitored, these registers must provide the timestamp which, when reached, will cause the output to shut down automatically. The values must be provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	
INT	-32768 to 32767	Nettime timestamp of the current output value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current output value

4.4.5.8.6.4 Enabling/disabling the output channels

Name:
AnalogOutput01Enable to AnalogOutput02Enable
AnalogOutput01EnableReadback to AnalogOutput02EnableReadback

The "OutputEnable" byte is only needed for the channels with activated time-based monitoring. The individual bits are used to enable/disable the respective channels. To receive reliable feedback about the current state of the module, the byte was also implemented so that it can be read cyclically.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01Enable AnalogOutput01EnableReadback	0	Output deactivated
		1	Output activated
1	AnalogOutput02Enable AnalogOutput02EnableReadback	0	Output deactivated
		1	Output activated
2 - 7	Reserved	0	

4.4.5.8.6.5 Checking the output values

Name:
AnalogOutput01OK to AnalogOutput02OK

These registers are only needed for channels with activated time-based monitoring. The individual bits report whether the respective channel is actually generating the required voltage or current.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01OK	0	Electrical signal deactivated
		1	Electrical signal activated
1	AnalogOutput02OK	0	Electrical signal deactivated
		1	Electrical signal activated
2 - 7	Reserved	0	

4.4.5.8.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.4.5.8.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.4.6 X20AO2632-1

4.4.6.1 General information

The module is equipped with two outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog outputs
- Either current or voltage signal possible
- Extended signal range
- 16-bit digital converter resolution

4.4.6.2 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO2632-1	X20 analog output module, 2 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 94: X20AO2632-1 - Order data

4.4.6.3 Technical data

Product ID	X20AO2632-1
Short description	
I/O module	2 analog outputs ±11 V or 0 to 22 mA
General information	
B&R ID code	0xC36E
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.25 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog outputs	
Output	±11 V or 0 to 22 mA, via different terminal connections
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all outputs
Settling time for output changes over entire range	500 µs
Power on/off behavior	Internal enable relay for booting

Table 95: X20AO2632-1 - Technical data

Product ID	X20AO2632-1
Max. error at 25°C	
Voltage	
Gain	0.05% 2)
Offset	0.015% 3)
Current	
Gain	0.08% 2)
Offset	0.05% 3)
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.386 nA
Load per channel	
Voltage	Max. ±11 mA, load ≥1 kΩ
Current	Max. load is 600 Ω
Short circuit protection	Current limiting ±40 mA
Output filter	1st-order low pass / cutoff frequency 10 kHz
Max. gain drift	
Voltage	0.008 %/°C 2)
Current	0.011 %/°C 2)
Max. offset drift	
Voltage	0.003 %/°C 3)
Current	0.008 %/°C 3)
Error caused by load change	
Voltage	Max. 0.1%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive
Nonlinearity	<0.007% 4)
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 95: X20AO2632-1 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current output value.
3) Based on the entire output range.
4) Based on the output range.

4.4.6.4 LED status indicators

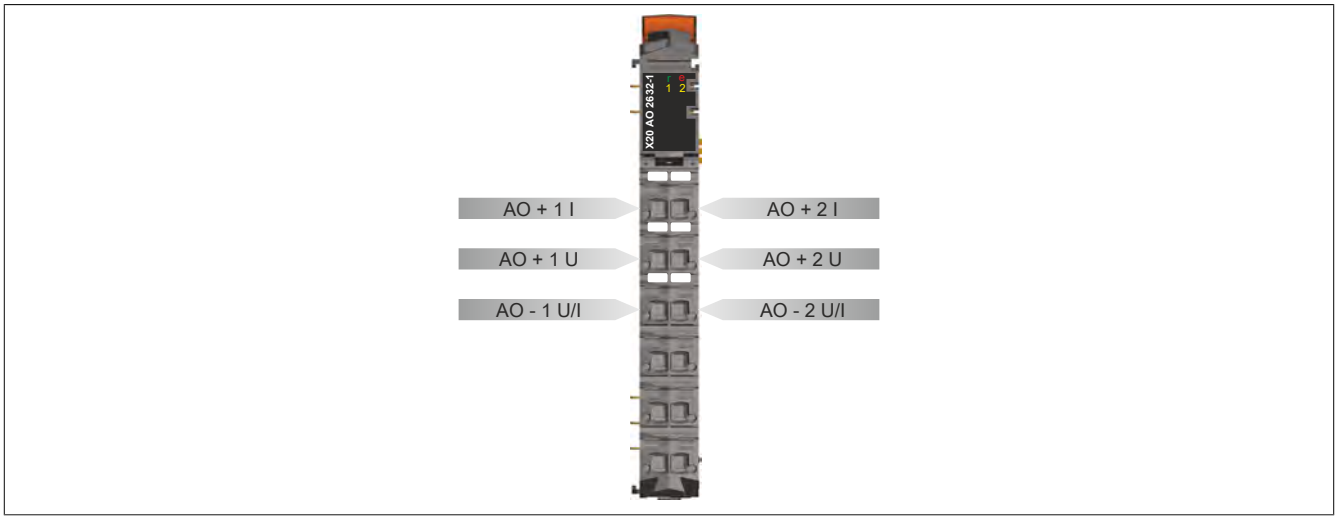
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 2	Orange	Off	Value = 0
			On	Value ≠ 0

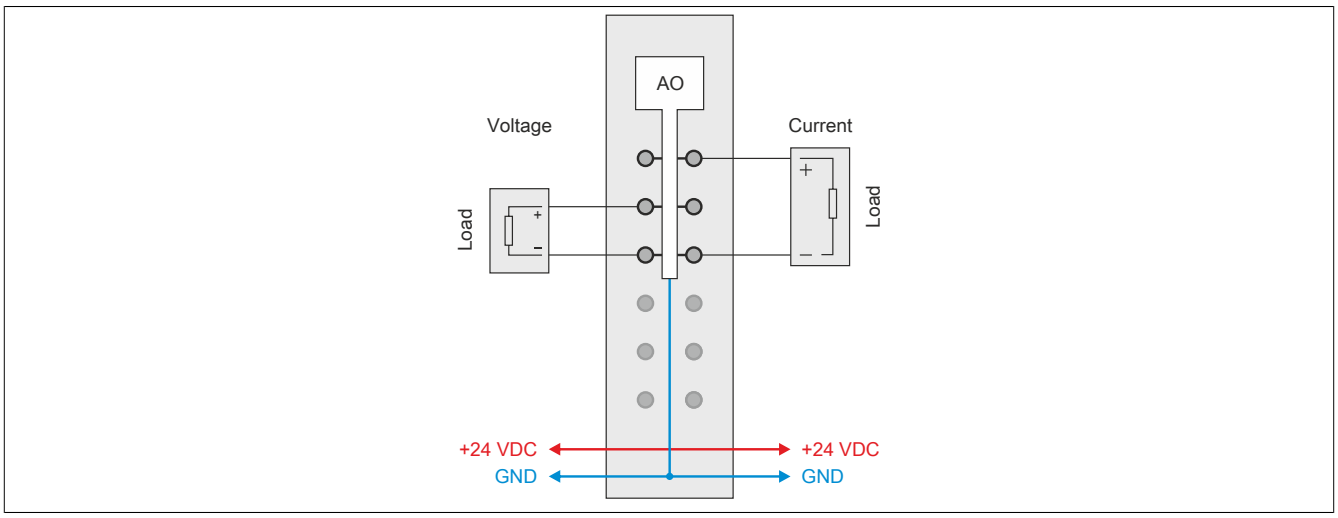
1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.6.5 Pinout

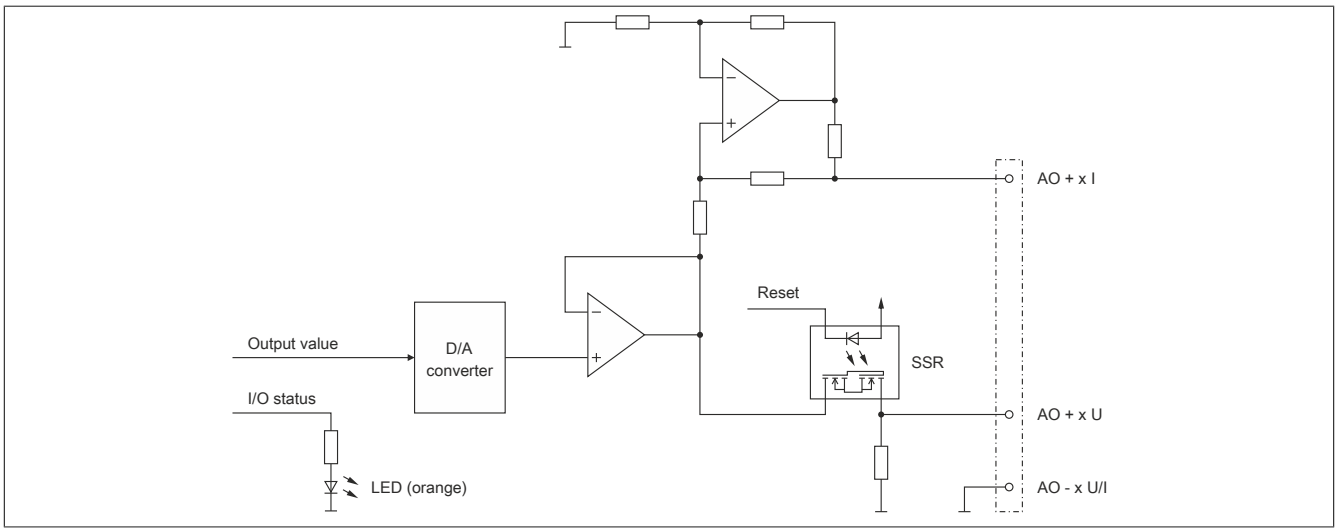
Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.



4.4.6.6 Connection example



4.4.6.7 Output circuit diagram



4.4.6.8 Register description

4.4.6.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.6.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration						
0	ConfigOutput01	UINT				•
594 598	Cfo_Channel01TimeMode Cfo_Channel02TimeMode	UINT				•
Analog output - Communication						
2 4	AnalogOutput01 AnalogOutput02	INT			•	
457	SDCLifeCount	SINT	•			
802 810	ValidationTimer01 ValidationTimer02	INT			•	
804 812	ValidationTimer01 ValidationTimer02	DINT			•	
833	Enabling/disabling the output channels	USINT	•		•	
	AnalogOutput01Enable, ~Readback	Bit 0				
	AnalogOutput02Enable, ~Readback	Bit 1				
835	Checking the output values	USINT	•			
	AnalogOutput01OK	Bit 0				
	AnalogOutput02OK	Bit 1				

4.4.6.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration							
0	-	ConfigOutput01	UINT				•
Analog output - Communication							
2 4	0 2	AnalogOutput01 AnalogOutput02	INT			•	

1) The offset specifies the position of the register within the CAN object.

4.4.6.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.4.6.8.4 General information

The module provides two analog outputs. Each channel can output a voltage range of ±11 V or a current range of 0 to 22 mA.

The module also has a time-based watchdog monitor. The user can activate this feature channel-by-channel as needed.

4.4.6.8.5 Analog output - Configuration

Each channel is configured independently. The user can also define an optional time-based monitor. To make this possible, two watchdog timers were implemented, which can be assigned to the outputs.

4.4.6.8.5.1 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±11 V voltage signal (default)
- 0 to 22 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal
		1	Current signal
9	Channel 2	0	Voltage signal
		1	Current signal
10 - 15	Reserved	0	

4.4.6.8.5.2 Configuring the time-based watchdog monitor

Name:
Cfo_Channel01TimeMode to Cfo_Channel02TimeMode

This register is used to activate or configure the time-based watchdog monitor for the analog output channels.

Possibilities per channel:

- Validation timer data type: General choice 16 or 32 bit
- Validation window: The maximum value can be further limited within the data type.
- Timer allocation: A separate timer is available for each channel. However, all channels can be configured with the same validation timer, whereby the same settings must be made for the data type and window in the TimeMode registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 4	Max. validation time	00000	Disabled
		00001	2 µs
		00010	4 µs
		00011	8 µs
		...	...
		11111	2,147,483,648 µs (~35 min)
5 - 7	Reserved	0	
8	Timer allocation	0	ValidationTimer01 (default for channel 1)
		1	ValidationTimer02 (default for channel 2)
9 - 14	Reserved	0	
15	Time format	0	16-bit
		1	32-bit

4.4.6.8.6 Analog output - Communication

In standard mode, the module's outputs are enabled. Based on the configuration and AnalogOutput value, they output the corresponding current or voltage.

If the application requires time-based monitoring of the outputs, then a validation timer can be assigned to each channel. The validation timer register assigns a validity duration to the current output value. When validation is enabled, the module compares the validation time with the Nettime of the X2X Link. If the transferred validity duration is exceeded, the module disables the channel and resets the output. The "safety shutdown" state will not be reset until a new and valid validation time has been transferred. If enabled, the module reports which state it is currently in via the channel's error status bit.

If the value of the validation timer is incremented in each task cycle, the valid validation time will be calculated as follows:

Nettime of the X2X Link master (which the module is connected to)	
+	Timespan for transferring data from the X2X Link master to the CPU (higher-level system)
+	Cycle time of task class (including tolerance)
+	Timespan for transferring the data from the CPU to the module
+	Timespan allowed by the application (e.g. for tolerating failure of an X2X Link cycle)
=	Valid validation time

The AnalogOutputEnableByte is enabled during time-based monitoring. If the timer expires prematurely, the corresponding bit in the AnalogOutputOkayByte is reset and the output drops out. This provides an easy way to achieve a defined state.

4.4.6.8.6.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage; Bus controller default setting: 0
	0 to 32767	Current

4.4.6.8.6.2 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.4.6.8.6.3 Transfer of the timestamp

Name:
ValidationTimer01 to ValidationTimer02

When an output is being monitored, these registers must provide the timestamp which, when reached, will cause the output to shut down automatically. The values must be provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	
INT	-32768 to 32767	Nettime timestamp of the current output value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current output value

4.4.6.8.6.4 Enabling/disabling the output channels

Name:
AnalogOutput01Enable to AnalogOutput02Enable
AnalogOutput01EnableReadback to AnalogOutput02EnableReadback

The "OutputEnable" byte is only needed for the channels with activated time-based monitoring. The individual bits are used to enable/disable the respective channels. To receive reliable feedback about the current state of the module, the byte was also implemented so that it can be read cyclically.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01Enable AnalogOutput01EnableReadback	0	Output deactivated
		1	Output activated
1	AnalogOutput02Enable AnalogOutput02EnableReadback	0	Output deactivated
		1	Output activated
2 - 7	Reserved	0	

4.4.6.8.6.5 Checking the output values

Name:
AnalogOutput01OK to AnalogOutput02OK

These registers are only needed for channels with activated time-based monitoring. The individual bits report whether the respective channel is actually generating the required voltage or current.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01OK	0	Electrical signal deactivated
		1	Electrical signal activated
1	AnalogOutput02OK	0	Electrical signal deactivated
		1	Electrical signal activated
2 - 7	Reserved	0	

4.4.6.8.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.4.6.8.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.4.7 X20(c)AO4622

4.4.7.1 General information

The module is equipped with four outputs with 13-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

- 4 analog outputs
- Either current or voltage signal possible
- 13-bit digital converter resolution

4.4.7.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.4.7.3 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO4622	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	
X20cAO4622	X20 analog output module, coated, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 96: X20AO4622, X20cAO4622 - Order data

4.4.7.4 Technical data

Product ID	X20AO4622	X20cAO4622
Short description		
I/O module	4 analog outputs ±10 V or 0 to 20 mA / 4 to 20 mA [1]	4 analog outputs ±10 V or 0 to 20 mA / 4 to 20 mA
General information		
B&R ID code	0x1BA3	0xE212
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.8 W (Rev. ≥ J0); 2.2 W (Rev. < J0)	1.8 W
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Analog outputs		
Output	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections [1]	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections
Max. output current	10 mA at voltages >5 V 15 mA at voltages <5 V	
Digital converter resolution		
Voltage	±12-bit	
Current	12 Bit	
Conversion time	300 µs for all outputs	
Settling time for output changes over entire range	500 µs	
Power on/off behavior	Internal enable relay for booting	
Max. error at 25°C		
Voltage		
Gain	0.08% [3]	
Offset	0.05% [4]	
Current		
Gain	0.09% [3]	
Offset	0.05% [4]	
Output protection	Short circuit protection	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0010 = 4.882 mV	
Current	INT 0x8001 - 0x7FFF / 1 LSB = 0x0010 = 9.766 µA	
Load per channel		
Voltage	Max. ±10 mA, load ≥1 kΩ	
Current	Load max. 600 Ω (Rev. ≥ J0); 500 Ω (Rev. < J0)	Max. load is 600 Ω
Short circuit protection	Current limiting ±40 mA	
Output filter	1st-order low pass / cutoff frequency 10 kHz	
Max. gain drift		
Voltage	0.015 %/°C [3]	
Current	0.02 %/°C [3]	
Max. offset drift		
Voltage	0.032 %/°C [4]	
Current	0.032 %/°C [4]	
Error caused by load change		
Voltage	Max. 0.11%, from 10 MΩ → 1 kΩ, resistive	
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive	
Nonlinearity	<0.005% [5]	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	

Table 97: X20AO4622, X20cAO4622 - Technical data

Product ID	X20AO4622	X20cAO4622
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C (Rev. ≥ J0); 0 to 55°C (Rev. < J0)	-25 to 60°C
Vertical installation	-25 to 50°C (Rev. ≥ J0); 0 to 50°C (Rev. < J0)	-25 to 50°C
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 97: X20AO4622, X20cAO4622 - Technical data

1) 4 to 20 mA: From upgrade version 1.0.2.0 or hardware revision "I0"
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Based on the current output value.
4) Based on the entire output range.
5) Based on the output range.

4.4.7.5 LED status indicators

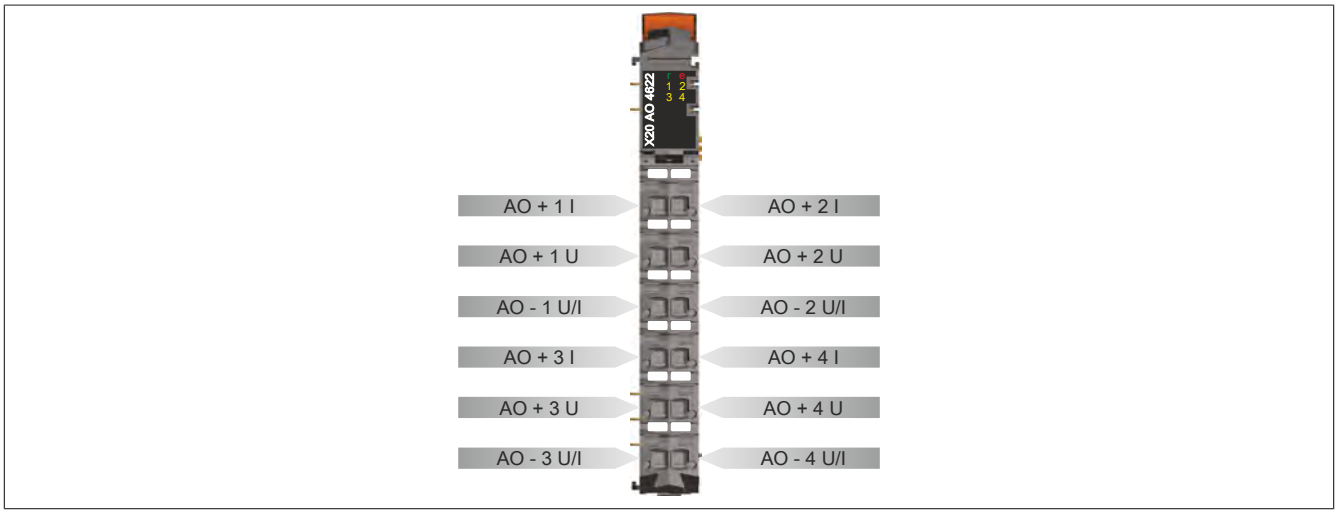
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange	Off	Value = 0
			On	Value ≠ 0

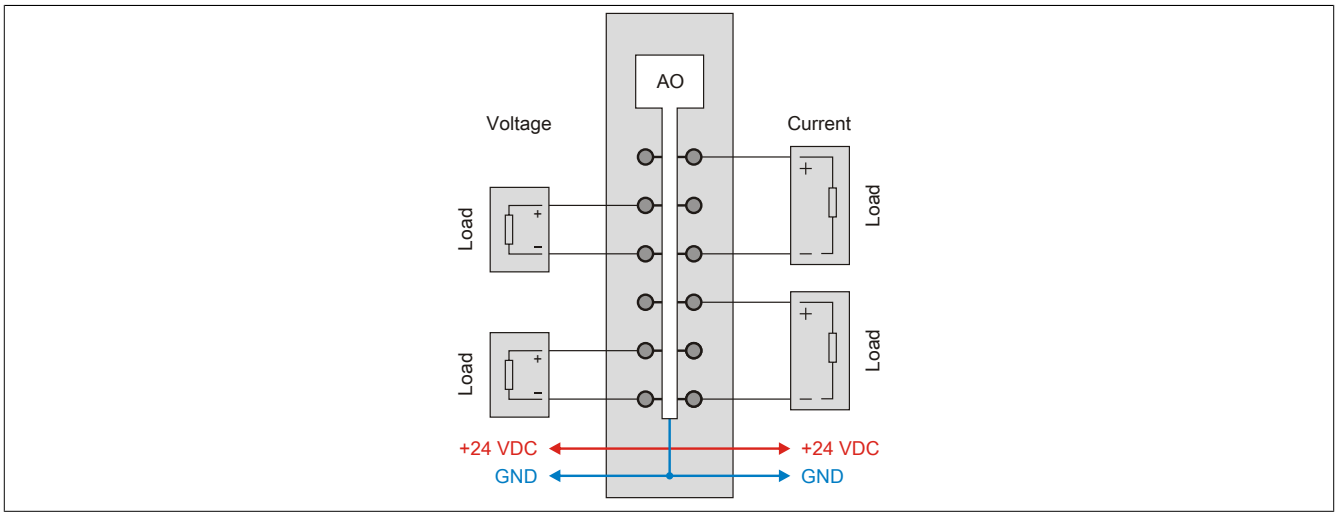
1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.7.6 Pinout

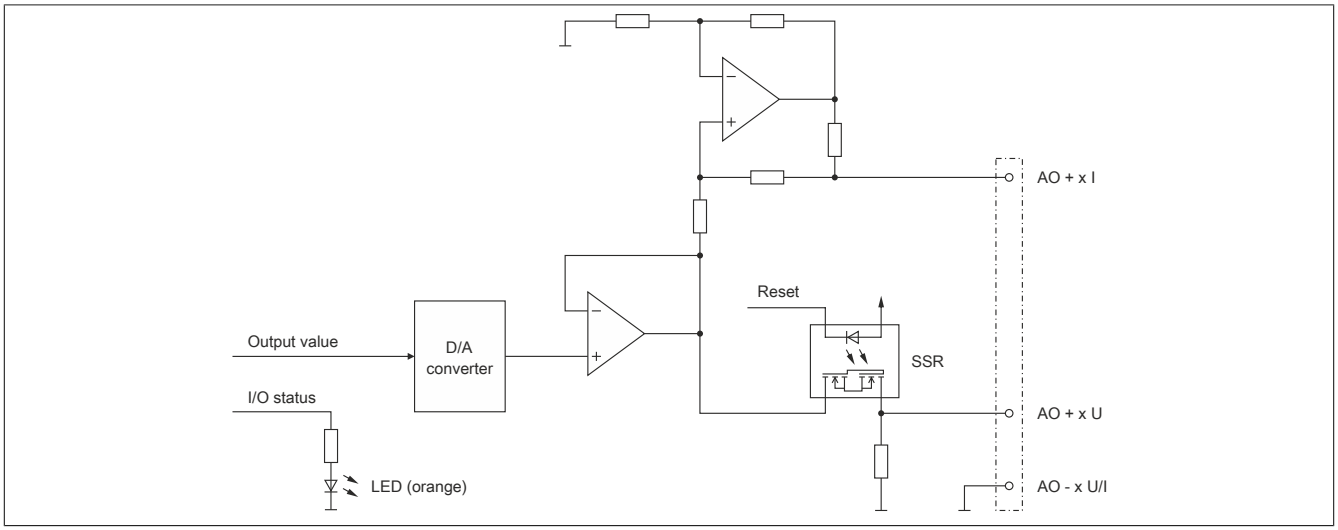
Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.



4.4.7.7 Connection example



4.4.7.8 Output circuit diagram



4.4.7.9 Derating

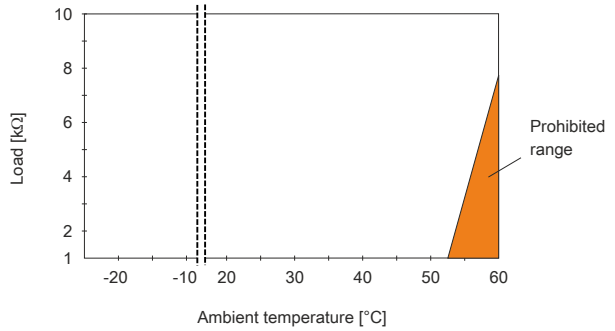
To ensure proper operation, the following items must be taken into consideration:

- The following derating listings must be taken into consideration
- For mixed operation with one current output, the average of both derating curves should be used
- For mixed operation with two or three current outputs, the derating for the current outputs should be used

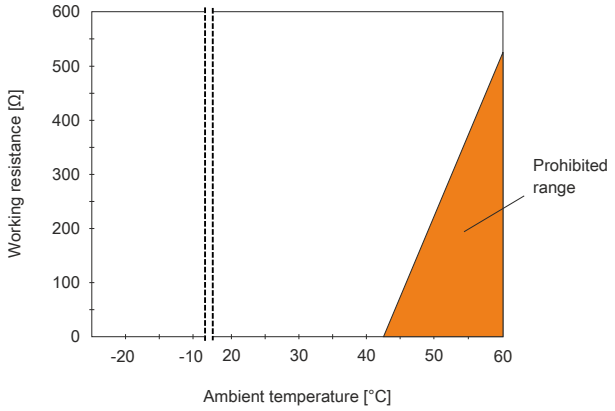
Horizontal installation

From revision J0

Voltage output

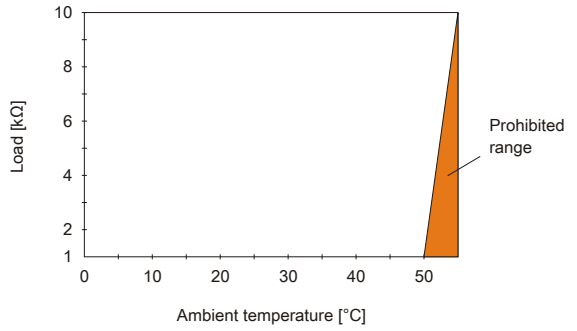


Current output

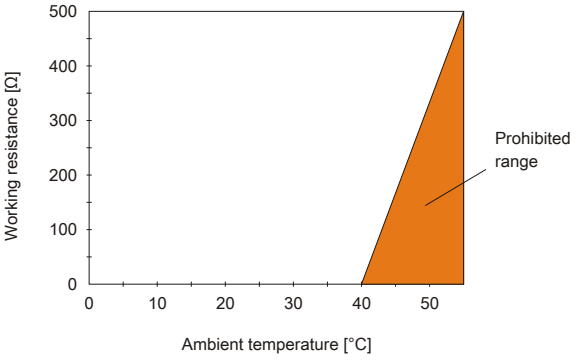


Before revision J0

Voltage output



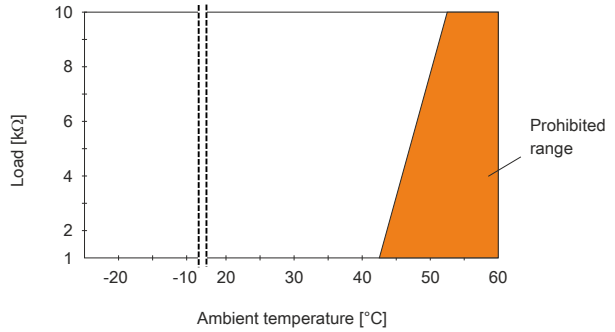
Current output



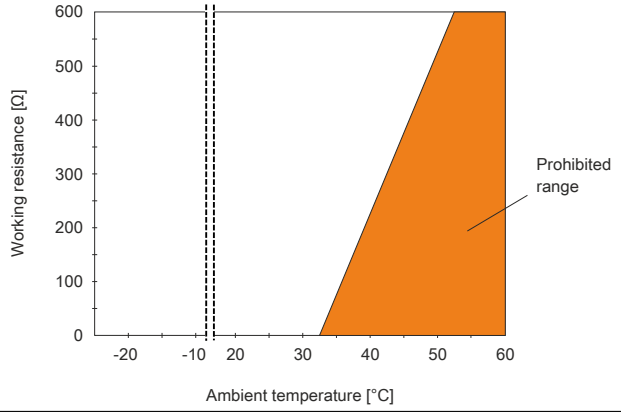
Vertical installation

From revision J0

Voltage output

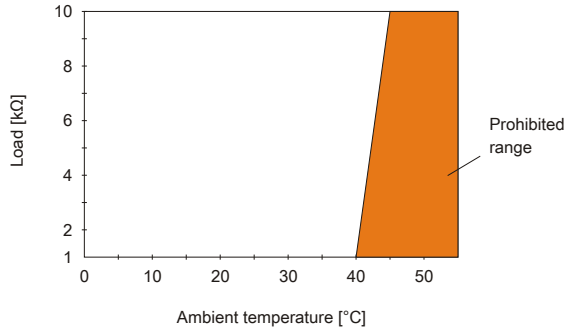


Current output

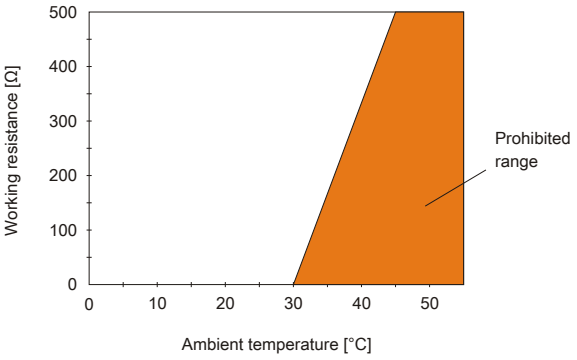


Before revision J0

Voltage output



Current output



4.4.7.10 Register description

4.4.7.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.7.10.2 Function model 0 - Standard and function model 1 - I/O with fast reaction

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
18	ConfigOutput01	USINT				•
Analog signal - Communication						
0	AnalogOutput01	INT			•	
2	AnalogOutput02	INT			•	
4	AnalogOutput03	INT			•	
6	AnalogOutput04	INT			•	

4.4.7.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
18	-	ConfigOutput01	USINT				•
Analog signal - Communication							
0	0	AnalogOutput01	INT			•	
2	2	AnalogOutput02	INT			•	
4	4	AnalogOutput03	INT			•	
6	6	AnalogOutput04	INT			•	

1) The offset specifies the position of the register within the CAN object.

4.4.7.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.4.7.10.4 Function model comparison

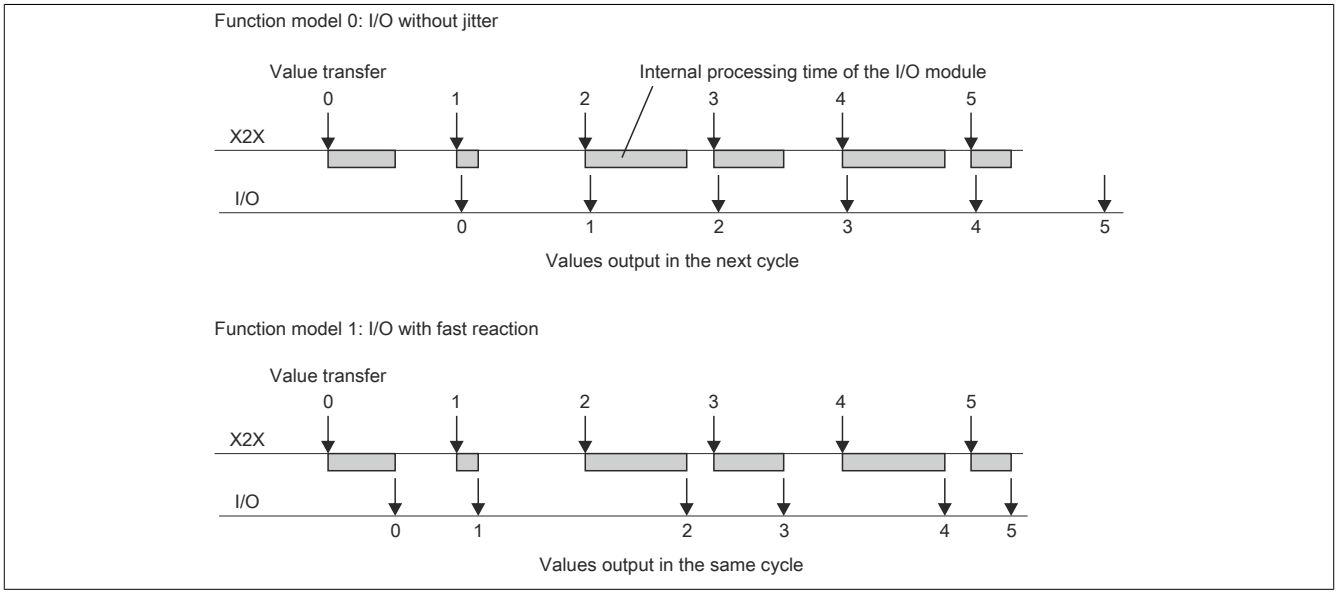
Function model 0: I/O without jitter (standard)

Corrected values are output in the next cycle if the minimum cycle is ≥400 µs in order to reduce jitter to a minimum.

Function model 1: I/O with fast reaction

Corrected values are output in the same cycle if the minimum cycle is ≥400 µs (optimized reactions).

Comparison of the two function models



4.4.7.10.5 Analog outputs

Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.

4.4.7.10.5.1 Output values of the analog output

Name:
AnalogOutput01 to AnalogOutput04

These registers provide the standardized output values. Once a permitted value is received the module outputs the respective current or voltage.

Data type	Value	Information
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA
	0 to 32767	Current signal 4 to 20 mA[1)]

1) From upgrade version 1.0.2.0 or hardware revision "I0"

4.4.7.10.5.2 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 4
...		...	
3	Channel 4	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 7
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
...		...	
7	Channel 4: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal

4.4.7.10.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

4.4.7.10.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
400 µs

4.4.8 X20(c)AO4632

4.4.8.1 General information

The module is equipped with four outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

- 4 analog outputs
- Either current or voltage signal possible
- 16-bit digital converter resolution

4.4.8.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.4.8.3 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO4632	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution	
X20cAO4632	X20 analog output module, coated, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 98: X20AO4632, X20cAO4632 - Order data

4.4.8.4 Technical data

Product ID	X20AO4632	X20cAO4632
Short description		
I/O module	4 analog outputs, ±10 V or 0 to 20 mA	
General information		
B&R ID code	0x1BA5	0xD575
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.8 W (Rev. ≥ J0); 2.2 W (Rev. < J0)	1.8 W
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Analog outputs		
Output	±10 V or 0 to 20 mA, via different connection terminal points	
Digital converter resolution		
Voltage	±15-bit	
Current	15-bit	
Conversion time	50 µs for all outputs	
Settling time for output changes over entire range	500 µs	
Power on/off behavior	Internal enable relay for booting	
Max. error at 25°C		
Voltage		
Gain	0.040% [2]	
Offset	0.022% [3]	
Current		
Gain	0.090% [2]	
Offset	0.045% [3]	
Output protection	Short circuit protection	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA	
Load per channel		
Voltage	Max. ±10 mA, load ≥1 kΩ	
Current	Load max. 600 Ω (Rev. ≥ J0); 500 Ω (Rev. < J0)	Max. load is 600 Ω
Short circuit protection	Current limiting ±40 mA	
Output filter	1st-order low pass / cutoff frequency 10 kHz	
Max. gain drift		
Voltage	0.010 %/°C [2]	
Current	0.020 %/°C [2]	
Max. offset drift		
Voltage	0.012 %/°C [3]	
Current	0.012 %/°C [3]	
Error caused by load change		
Voltage	Max. 0.11%, from 10 MΩ → 1 kΩ, resistive	
Current	Max. 0.50%, from 1 Ω → 600 Ω, resistive	
Nonlinearity	<0.005% [4]	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	

Table 99: X20AO4632, X20cAO4632 - Technical data

Product ID	X20AO4632	X20cAO4632
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C (Rev. ≥ J0); 0 to 55°C (Rev. < J0)	-25 to 60°C
Vertical installation	-25 to 50°C (Rev. ≥ J0); 0 to 50°C (Rev. < J0)	-25 to 50°C
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 99: X20AO4632, X20cAO4632 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Based on the current output value.
3) Based on the entire output range.
4) Based on the output range.

4.4.8.5 LED status indicators

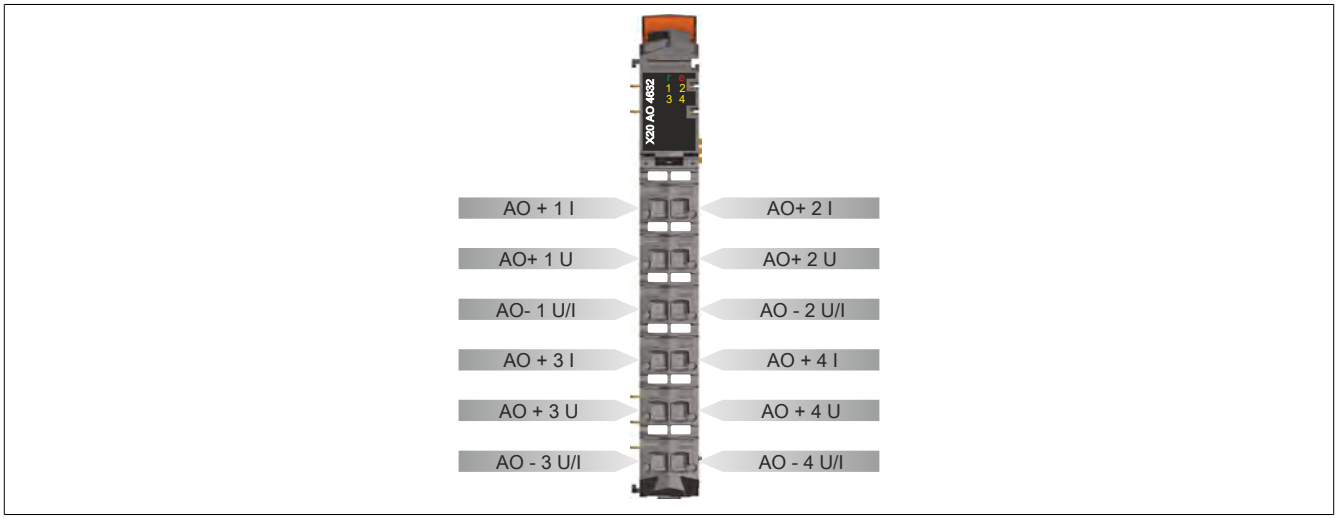
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 4	Orange	Off	Value = 0
			On	Value ≠ 0

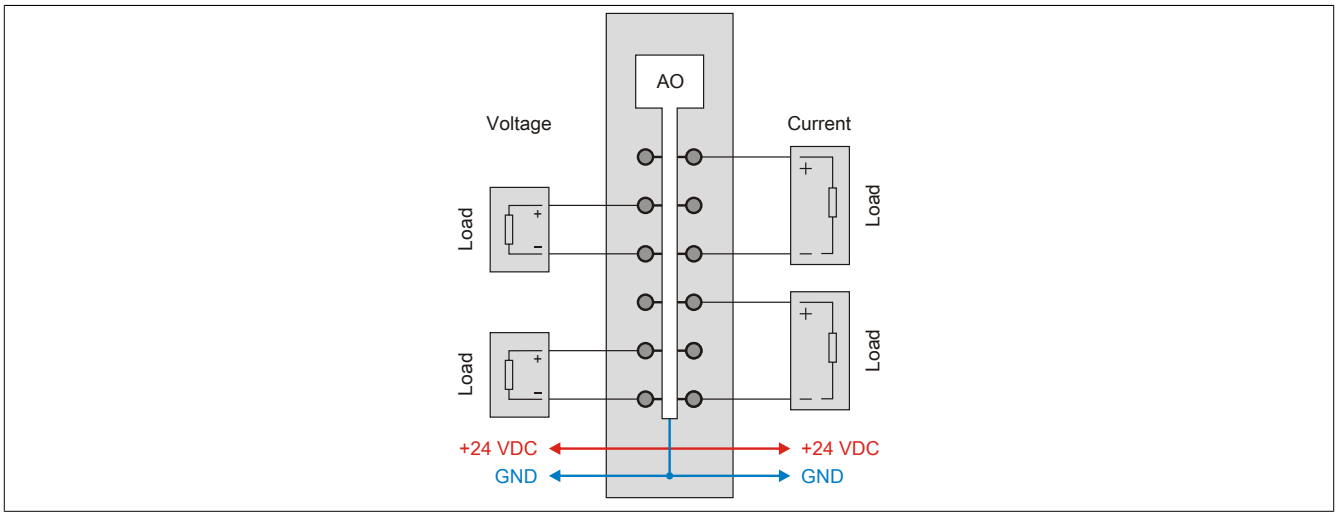
1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.8.6 Pinout

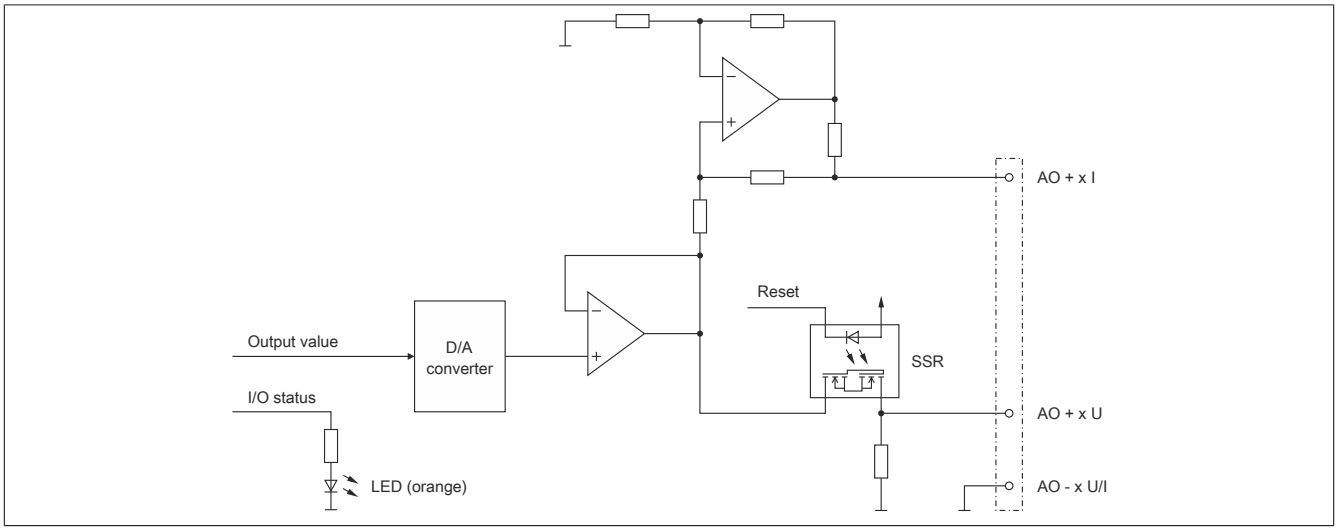
Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.



4.4.8.7 Connection example



4.4.8.8 Output circuit diagram



4.4.8.9 Derating

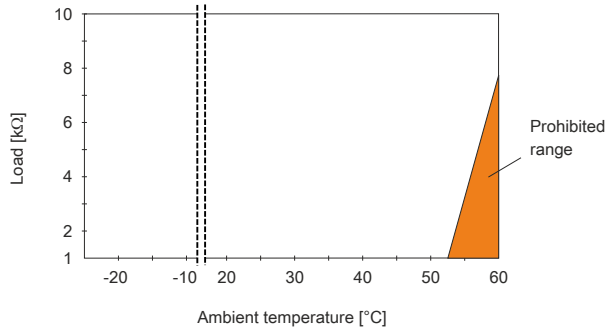
To ensure proper operation, the following items must be taken into consideration:

- The following derating listings must be taken into consideration
- For mixed operation with one current output, the average of both derating curves should be used
- For mixed operation with two or three current outputs, the derating for the current outputs should be used

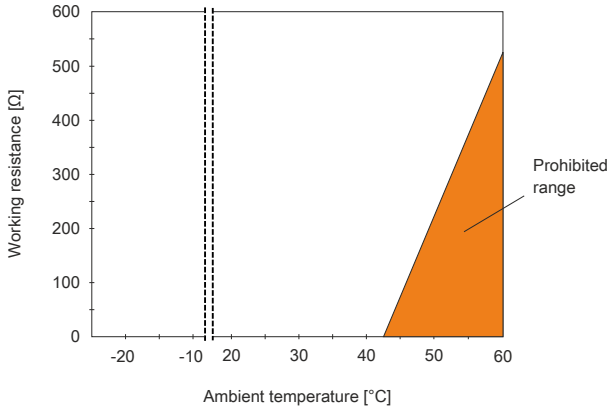
Horizontal installation

From revision J0

Voltage output

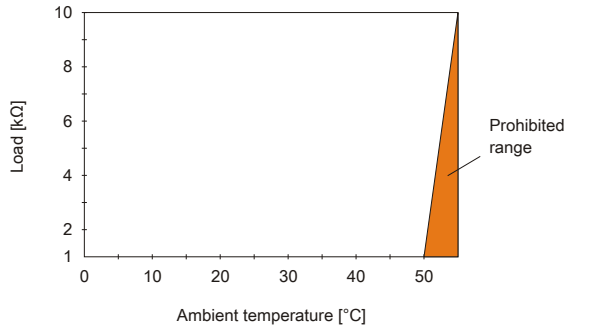


Current output

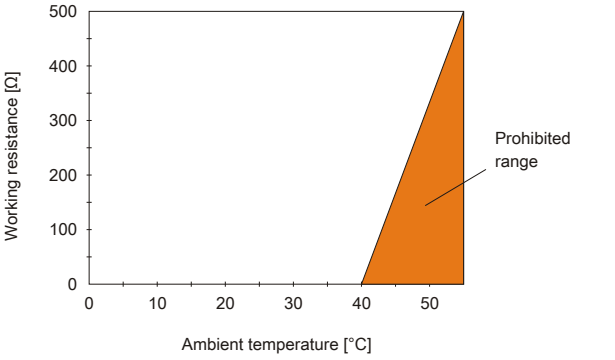


Before revision J0

Voltage output



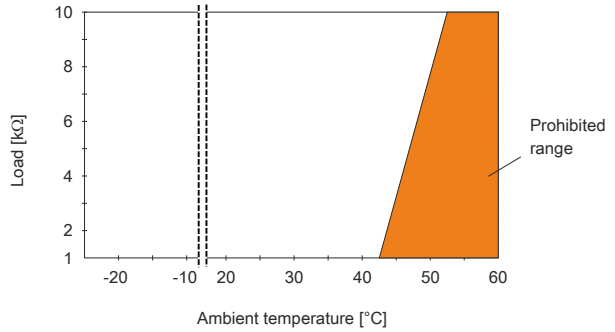
Current output



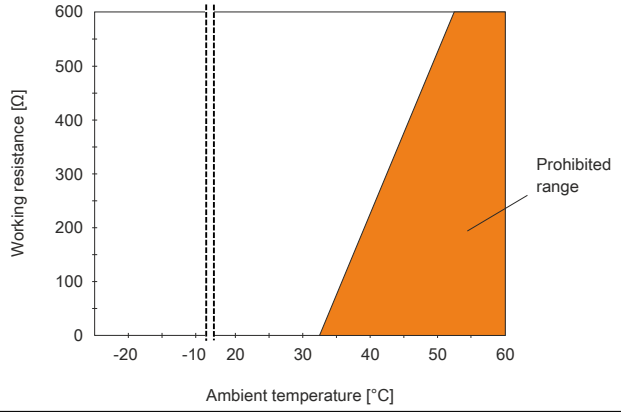
Vertical installation

From revision J0

Voltage output

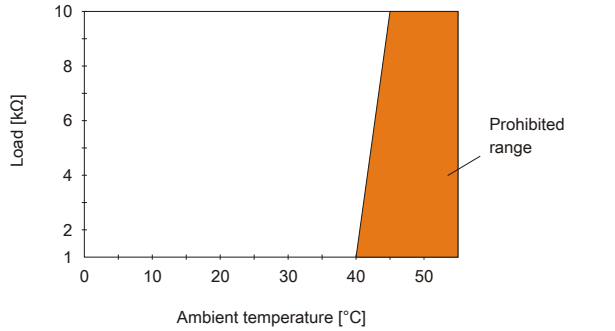


Current output

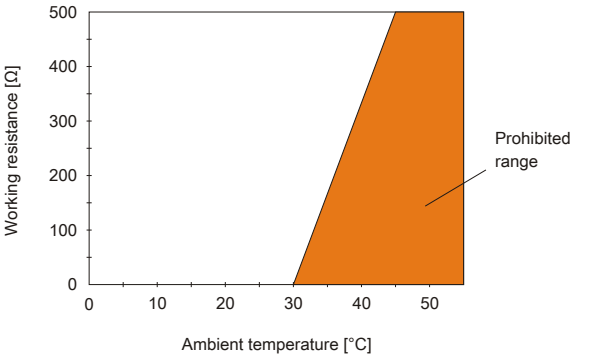


Before revision J0

Voltage output



Current output



4.4.8.10 Register description

4.4.8.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.8.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
0	ConfigOutput01	UINT				•
Analog signal - Communication						
Index * 2	AnalogOutput0N (Index N = 1 to 4)	INT			•	
10 + Index * 4	AnalogOutputDelayed0N (Index N = 0 to 3)	INT			•	
12	OutputDelayConfig00	UINT			•	
18	OutputDelayConfig01	UINT			•	
14	AnalogOutputLatchTime00	UINT	•			
22	AnalogOutputLatchTime01	UINT	•			
20	Error	UINT	•			

4.4.8.10.3 Function model 254 - Bus controller

Register	Offset[1]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
0	-	ConfigOutput01	UINT				•
Analog signal - Communication							
10 + Index * 4	Index * 2 - 2	AnalogOutput0N (Index N = 1 to 4)	INT			•	

1) The offset specifies the position of the register within the CAN object.

4.4.8.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.4.8.10.4 Analog output - Configuration

4.4.8.10.4.1 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal
		1	Current signal
...		...	
11	Channel 4	0	Voltage signal
		1	Current signal
12 - 15	Reserved	0	

4.4.8.10.5 Analog output - Configuration

4.4.8.10.5.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput04

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage; Bus controller default setting: 0
	0 to 32767	Current

4.4.8.10.5.2 Value for delayed output

Name:
AnalogOutputDelayed00 to AnalogOutputDelayed03

These registers contain the values with which the analog outputs are overwritten after the delay configured with OutputDelayConfig0x has expired.

Data type	Value	Output Signal
INT	-32768 to 32767	Voltage signal -10 VDC to 10 VDC
	0 to 32767	Current signal 0 mA to 20 mA

4.4.8.10.5.3 Configuration of the output delay

Name:
OutputDelayConfig00 to OutputDelayConfig01

Two configurations independent from each other can be created using these registers.

The delay time after which AnalogOutputDelay0x should overwrite the channel can be configured using bits 0 to 13. Using bits 14 and 15, the channel is determined for which the configuration is valid.

Each channel can only be overwritten once. No additional channel can be overwritten while the respective time is running.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 13	Delay time for the selected channel	x	Time in µs
14 - 15	Channel	00	Analog output 01
		01	Analog output 02
		10	Analog output 03
		11	Analog output 04

4.4.8.10.5.4 Delay time for the output value

Name:
AnalogOutputLatchTime00 to AnalogOutputLatchTime01

These registers can be used to read when the respective overwrite value was actually written on the output.

Data type	Value
UINT	Actual delay time

4.4.8.10.5.5 Error register for counter

Name:
Error

There are some limitations because two timers are used. This register is available to the user for reporting these potential errors.
The error bits are deleted as soon as a valid state is reset.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Analog output 01	0	OK
		1	Has already been overwritten
...		...	
3	Analog output 04	0	OK
		1	Has already been overwritten
4	Timer 01	0	OK
		1	Already in use
5	Timer 02	0	OK
		1	Already in use
6	Timer 01 and 02	0	OK
		1	Both timers refer to the same channel number
7 - 15	Reserved		

4.4.8.10.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.4.8.10.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.4.9 X20(c)AO4632-1

4.4.9.1 General information

The module is equipped with four outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

- 4 analog outputs
- Either current or voltage signal possible
- Extended signal range
- 16-bit digital converter resolution

4.4.9.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.4.9.3 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO4632-1	X20 analog output module, 4 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution	
X20cAO4632-1	X20 analog output module, coated, 4 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 100: X20AO4632-1, X20cAO4632-1 - Order data

4.4.9.4 Technical data

Product ID	X20AO4632-1	X20cAO4632-1
Short description		
I/O module	4 analog outputs, ±11 V or 0 to 22 mA	
General information		
B&R ID code	0xC36F	0xE213
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	2.15 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Analog outputs		
Output	±11 V or 0 to 22 mA, via different connection terminal points	
Digital converter resolution		
Voltage	±15-bit	
Current	15-bit	
Conversion time	50 µs for all outputs	
Settling time for output changes over entire range	500 µs	
Power on/off behavior	Internal enable relay for booting	
Max. error at 25°C		
Voltage		
Gain	0.05% [2]	
Offset	0.015% [3]	
Current		
Gain	0.08% [2]	
Offset	0.05% [3]	
Output protection	Short circuit protection	
Output format		
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.386 nA	
Load per channel		
Voltage	Max. ±11 mA, load ≥1 kΩ	
Current	Max. load is 600 Ω	
Short circuit protection	Current limiting ±40 mA	
Output filter	1st-order low pass / cut-off frequency 10 kHz	
Max. gain drift		
Voltage	0.008%/°C [2]	
Current	0.011%/°C [2]	
Max. offset drift		
Voltage	0.003%/°C [3]	
Current	0.008%/°C [3]	
Error caused by load change		
Voltage	Max. 0.1%, from 10 MΩ → 1 kΩ, resistive	
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive	
Nonlinearity	<0.007% [4]	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	

Table 101: X20AO4632-1, X20cAO4632-1 - Technical data

Product ID	X20AO4632-1	X20cAO4632-1
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 101: X20AO4632-1, X20cAO4632-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Based on the current output value.
3) Based on the entire output range.
4) Based on the output range.

4.4.9.5 LED status indicators

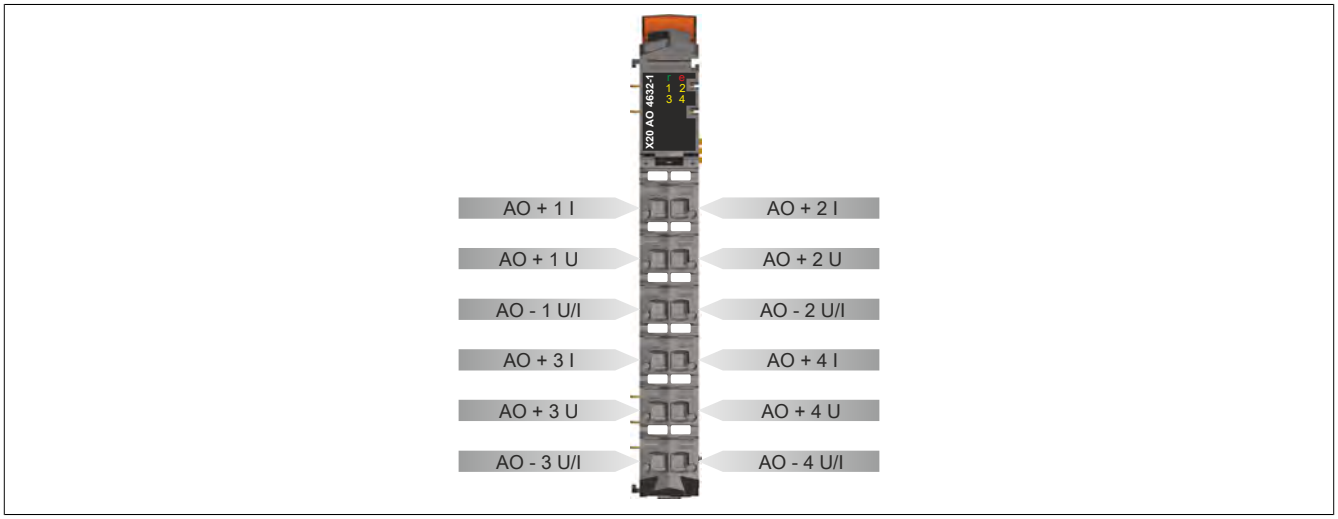
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 4	Orange	Off	Value = 0
			On	Value ≠ 0

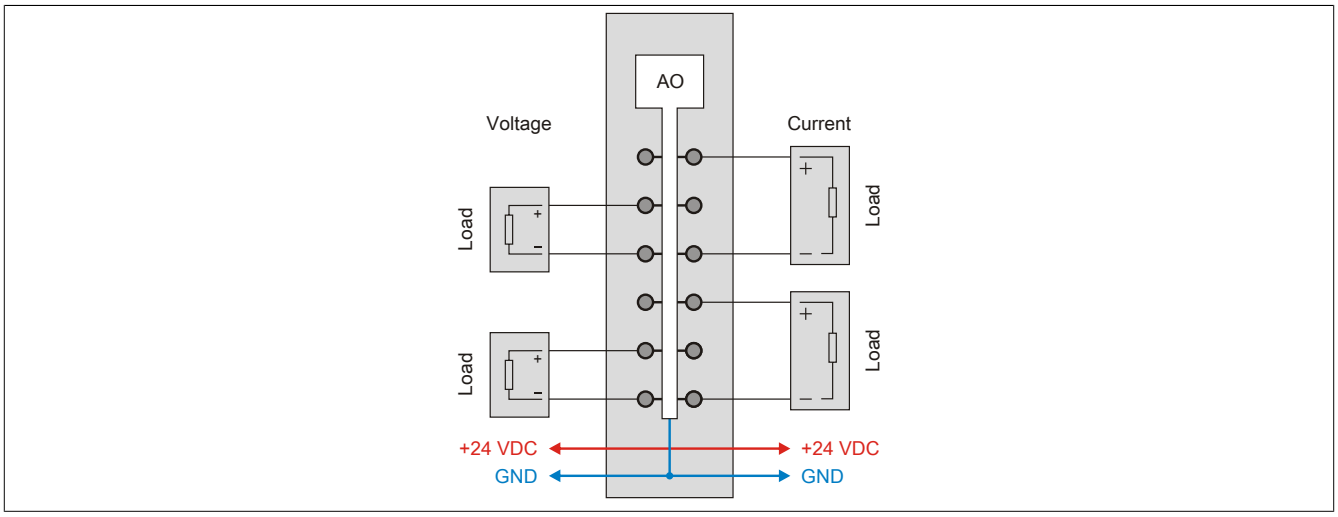
1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.9.6 Pinout

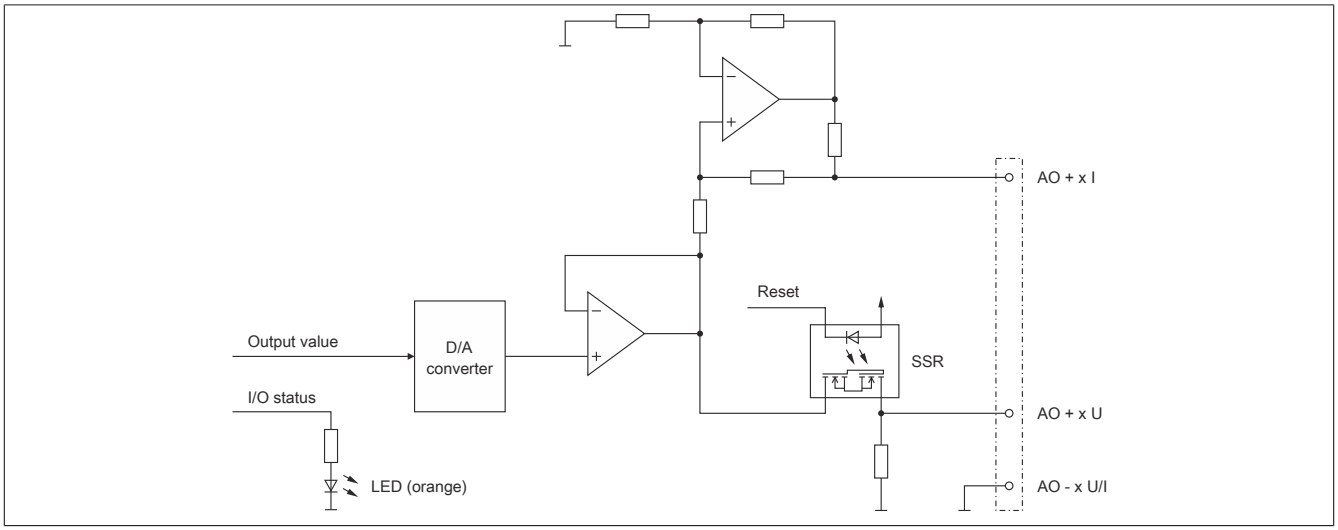
Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.



4.4.9.7 Connection example



4.4.9.8 Output circuit diagram



4.4.9.9 Derating

To ensure proper operation, the following items must be taken into consideration:

- The following derating listings must be taken into consideration
- For mixed operation with one current output, the average of both derating curves should be used
- For mixed operation with two or three current outputs, the derating for the current outputs should be used

Horizontal installation

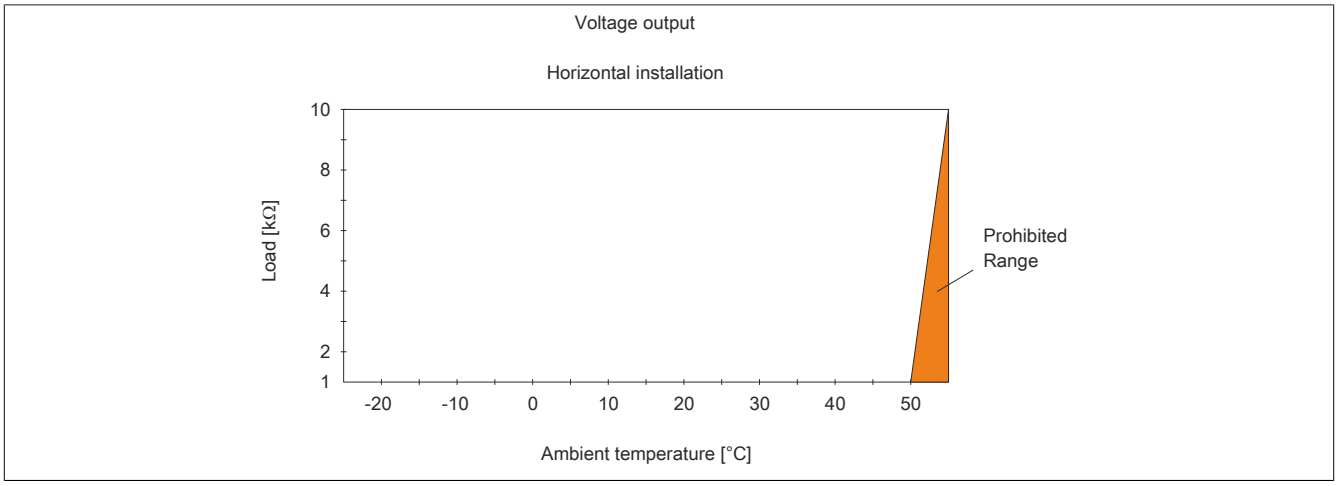


Figure 158: Derating the load with a voltage output and horizontal mounting

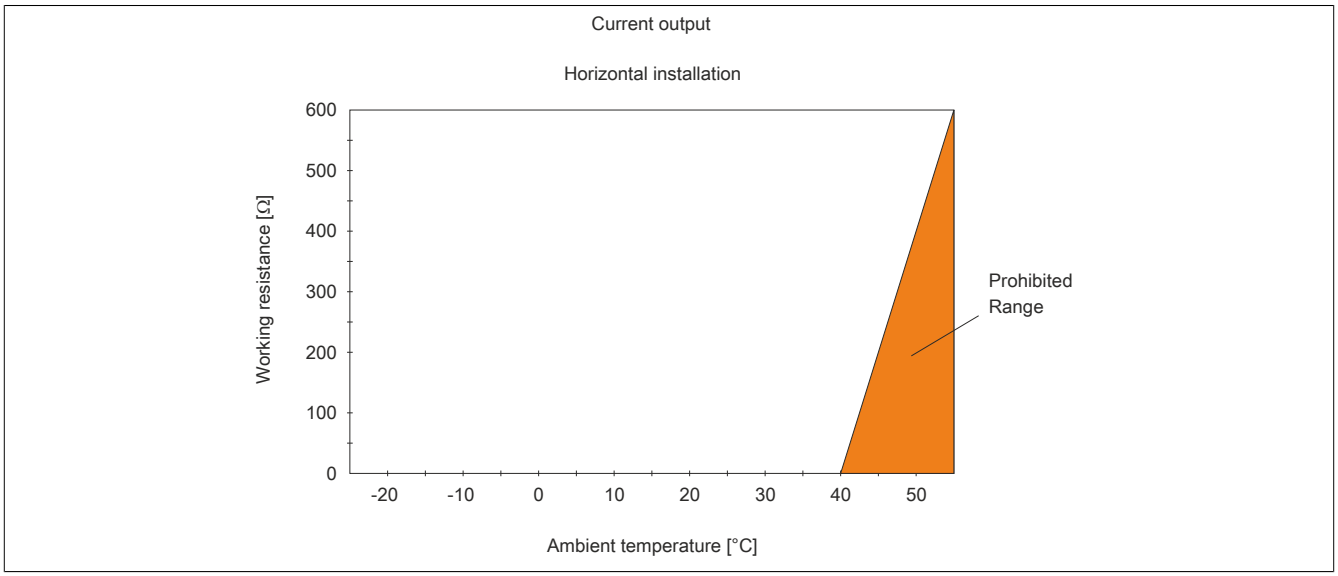


Figure 159: Derating the load with a current output and horizontal mounting

Vertical installation

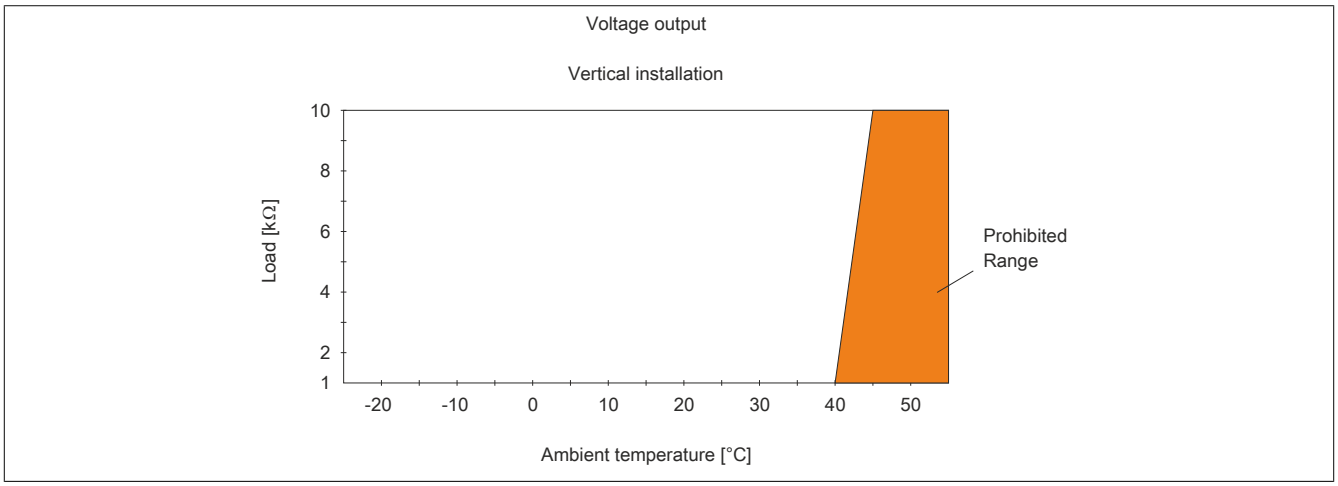


Figure 160: Derating the load with a voltage output and vertical mounting

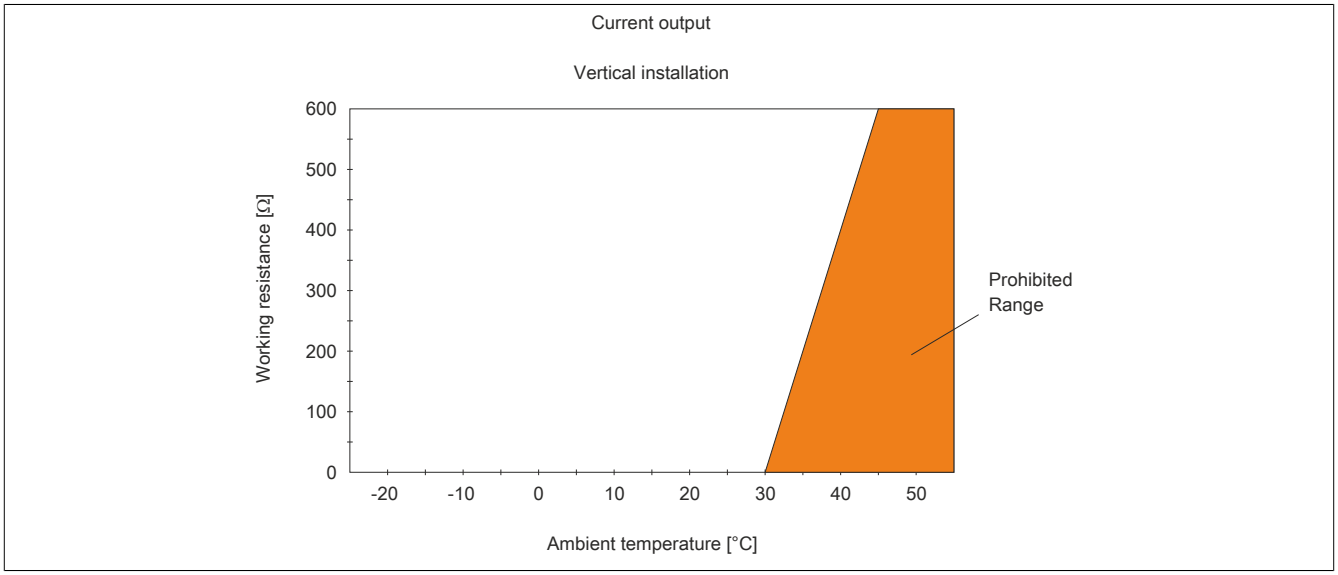


Figure 161: Derating the load with a current output and vertical mounting

4.4.9.10 Register description

4.4.9.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.9.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration						
0	ConfigOutput01	UINT				•
590 + Index*4	Cfo_Channel0NTimeMode (Index N = 1 to 4)	UINT				•
Analog output - Communication						
Index * 2	AnalogOutput0N (Index N = 1 to 4)	INT			•	
457	SDCLifeCount	SINT	•			
794 + Index*8	ValidationTimer0N (Index N = 1 to 4)	INT			•	
796 + Index*8	ValidationTimer0N (Index N = 1 to 4)	DINT			•	
833	Enabling/disabling the output channels	USINT	•		•	
	AnalogOutput01Enable, ~Readback	Bit 0				
	...	...				
	AnalogOutput04Enable, ~Readback	Bit 3				
835	Checking the output values	USINT	•			
	AnalogOutput01OK	Bit 0				
	...	...				
	AnalogOutput04OK	Bit 3				

4.4.9.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration							
0	-	ConfigOutput01	UINT				•
Analog output - Communication							
10 + Index * 4	Index * 2 - 2	AnalogOutput0N (Index N = 1 to 4)	INT			•	

1) The offset specifies the position of the register within the CAN object.

4.4.9.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.4.9.10.4 General information

The module provides four analog outputs. Each channel can output a voltage range of ±11 V or a current range of 0 to 22 mA.

The module also has a time-based watchdog monitor. The user can activate this feature on a channel-by-channel basis as needed.

4.4.9.10.5 Analog output - Configuration

Each channel is configured independently. The user can also define an optional time-based monitor. To make this possible, four watchdog timers were implemented, which can be assigned to the outputs.

4.4.9.10.5.1 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±11 V voltage signal (default)
- 0 to 22 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal
		1	Current signal
...		...	
11	Channel 4	0	Voltage signal
		1	Current signal
12 - 15	Reserved	0	

4.4.9.10.5.2 Configuring the time-based watchdog monitor

Name:
Cfo_Channel01TimeMode to Cfo_Channel04TimeMode

This register is used to activate or configure the time-based watchdog monitor for the analog output channels.

Possibilities per channel:

- Validation timer data type: General choice 16 or 32 bit
- Validation window: The maximum value can be further limited within the data type.
- Timer allocation: A separate timer is available for each channel. However, all channels can be configured with the same validation timer, whereby the same settings must be made for the data type and window in the TimeMode registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 4	Max. validation time	00000	Disabled
		00001	2 µs
		00010	4 µs
		00011	8 µs
		...	...
		11111	2,147,483,648 µs (~35 min)
5 - 7	Reserved	0	
8 - 9	Timer allocation	00	ValidationTimer01 (default for channel 1)
		01	ValidationTimer02 (default for channel 2)
		10	ValidationTimer03 (default for channel 3)
		11	ValidationTimer04 (default for channel 4)
10 - 14	Reserved	0	
15	Time format	0	16-bit
		1	32-bit

4.4.9.10.6 Analog output - Communication

In standard mode, the module's outputs are enabled. Based on the configuration and AnalogOutput value, they output the corresponding current or voltage.

If the application requires time-based monitoring of the outputs, then a validation timer can be assigned to each channel. The validation timer register assigns a validity duration to the current output value. When validation is enabled, the module compares the validation time with the Nettime of the X2X Link. If the transferred validity duration is exceeded, the module disables the channel and resets the output. The "safety shutdown" state will not be reset until a new and valid validation time has been transferred. If enabled, the module reports which state it is currently in via the channel's error status bit.

If the value of the validation timer is incremented in each task cycle, the valid validation time will be calculated as follows:

Nettime of the X2X Link master (which the module is connected to)	
+	Timespan for transferring data from the X2X Link master to the CPU (higher-level system)
+	Cycle time of task class (including tolerance)
+	Timespan for transferring the data from the CPU to the module
+	Timespan allowed by the application (e.g. for tolerating failure of an X2X Link cycle)
=	Valid validation time

The AnalogOutputEnableByte is enabled during time-based monitoring. If the timer expires prematurely, the corresponding bit in the AnalogOutputOkayByte is reset and the output drops out. This provides an easy way to achieve a defined state.

4.4.9.10.6.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput04

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage; Bus controller default setting: 0
	0 to 32767	Current

4.4.9.10.6.2 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.4.9.10.6.3 Transfer of the timestamp

Name:
ValidationTimer01 to ValidationTimer04

When an output is being monitored, these registers must provide the timestamp which, when reached, will cause the output to shut down automatically. The values must be provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	
INT	-32768 to 32767	Nettime timestamp of the current output value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current output value

4.4.9.10.6.4 Enabling/disabling the output channels

Name:
AnalogOutput01Enable to AnalogOutput04Enable
AnalogOutput01EnableReadback to AnalogOutput04EnableReadback

The "OutputEnable" byte is only needed for the channels with activated time-based monitoring. The individual bits are used to enable/disable the respective channels. To receive reliable feedback about the current state of the module, the byte was also implemented so that it can be read cyclically.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01Enable AnalogOutput01EnableReadback	0	Output deactivated
		1	Output activated
...		...	
3	AnalogOutput04Enable AnalogOutput04EnableReadback	0	Output deactivated
		1	Output activated
4 - 7	Reserved	0	

4.4.9.10.6.5 Checking the output values

Name:
AnalogOutput01OK to AnalogOutput04OK

These registers are only needed for channels with activated time-based monitoring. The individual bits report whether the respective channel is actually generating the required voltage or current.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01OK	0	Electrical signal deactivated
		1	Electrical signal activated
...		...	
3	AnalogOutput04OK	0	Electrical signal deactivated
		1	Electrical signal activated
4 - 7	Reserved	0	

4.4.9.10.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.4.9.10.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.4.10 X20AO4635

4.4.10.1 General information

The module is equipped with four outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different connection terminal points.

- 4 analog outputs
- Either current or voltage signal possible
- 16-bit digital converter resolution
- Low temperature drift

4.4.10.2 Order data

Model number	Short description	Figure
	Analog outputs	
X20AO4635	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, low temperature drift	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 102: X20AO4635 - Order data

4.4.10.3 Technical data

Product ID	X20AO4635
Short description	
I/O module	4 analog outputs, ±10 V or 0 to 20 mA, low temperature drift
General information	
B&R ID code	0xA7FE
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Analog outputs	
Output	±10 V or 0 to 20 mA, via different terminal connections
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all outputs
Settling time for output changes over entire range	500 µs
Power on/off behavior	Internal enable relay for booting

Table 103: X20AO4635 - Technical data

Product ID	X20AO4635
Max. error at 25°C	
Gain	0.04% 2)
Offset	0.022% 3)
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Load per channel	
Voltage	Max. ±10 mA, load ≥ 1 kΩ
Current	Max. load is 500 Ω
Short circuit protection	Current limiting ±40 mA
Output filter	1st-order low pass / cutoff frequency 10 kHz
Error caused by load change	
Voltage	Max. 0.02%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 500 Ω, resistive
Nonlinearity	<0.005%
Isolation voltage between channel and bus	500 V_{eff}
Signal	
0 to 20 mA	
Max. gain drift	0.01 %/°C 2)
Max. offset drift	0.012 %/°C 3)
±10 V	
Max. gain drift	0.0025 %/°C 2)
Max. offset drift	0.001 %/°C 3)
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 55°C
Vertical installation	-25 to 50°C
Derating	See section "Module operation"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 103: X20AO4635 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Based on the current output value.
3) Based on the entire output range.

4.4.10.4 LED status indicators

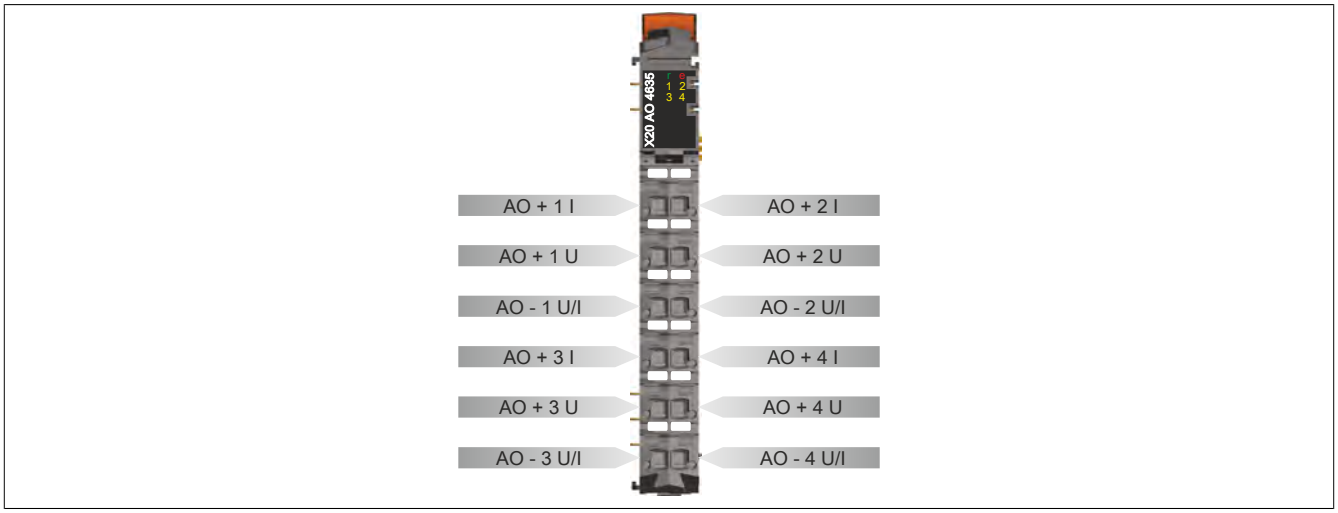
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 4	Orange	Off	Value = 0
			On	Value ≠ 0

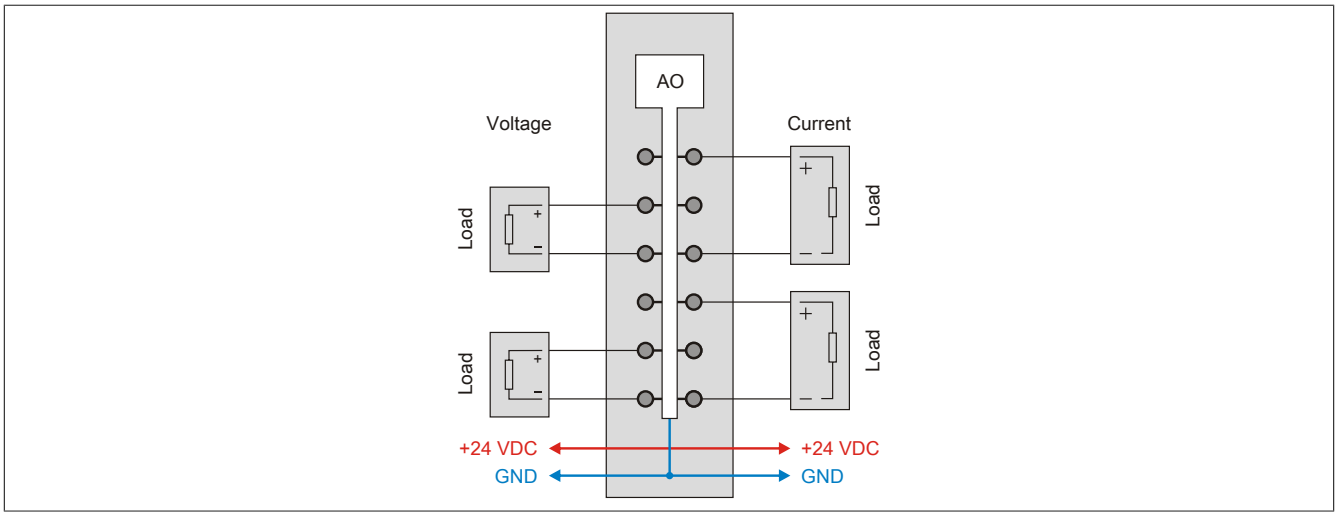
1) Depending on the configuration, a firmware update can take up to several minutes.

4.4.10.5 Pinout

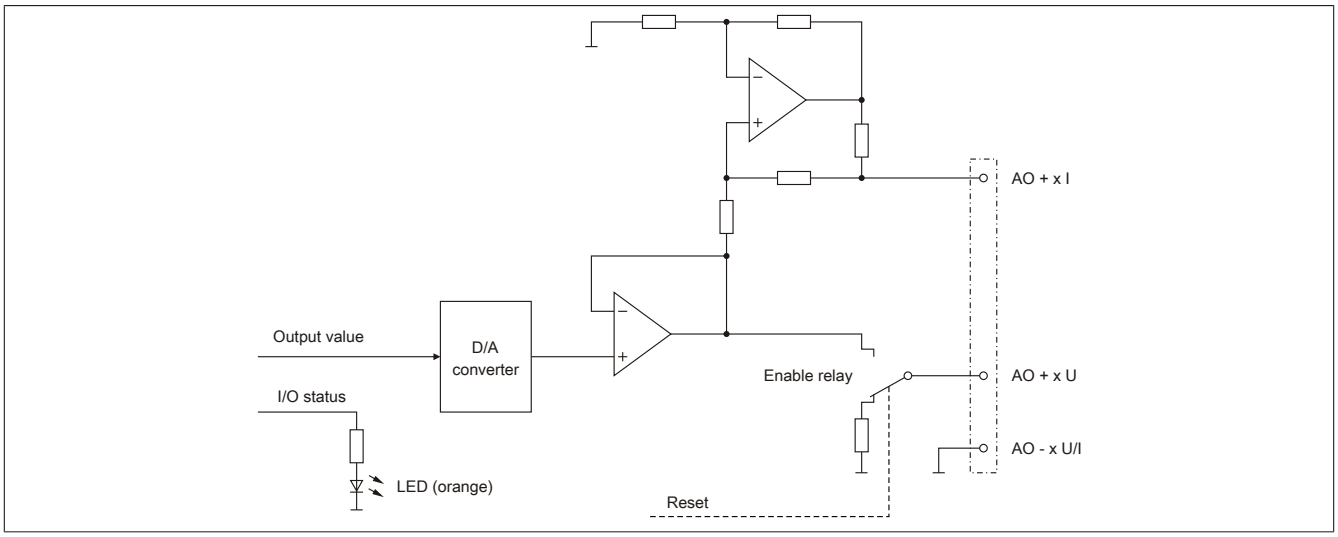
Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.



4.4.10.6 Connection example



4.4.10.7 Output circuit diagram



4.4.10.8 Module operation

To ensure proper operation, the following items must be taken into consideration:

- The following derating listings must be taken into consideration
- For mixed operation with one current output, the average of both derating curves should be used
- For mixed operation with two or three current outputs, the derating for the current outputs should be used

Horizontal installation

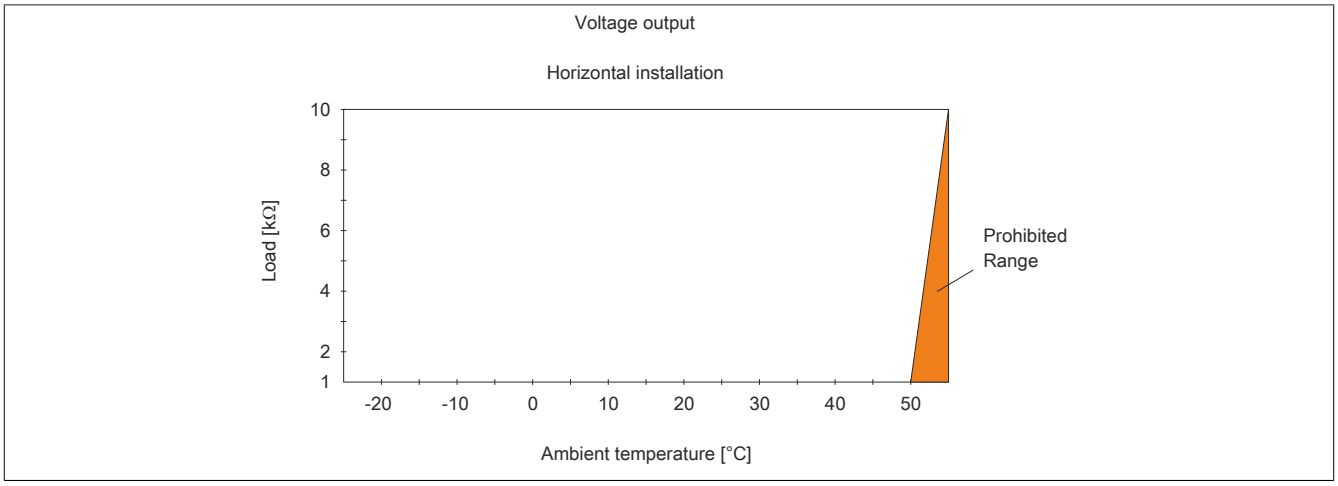
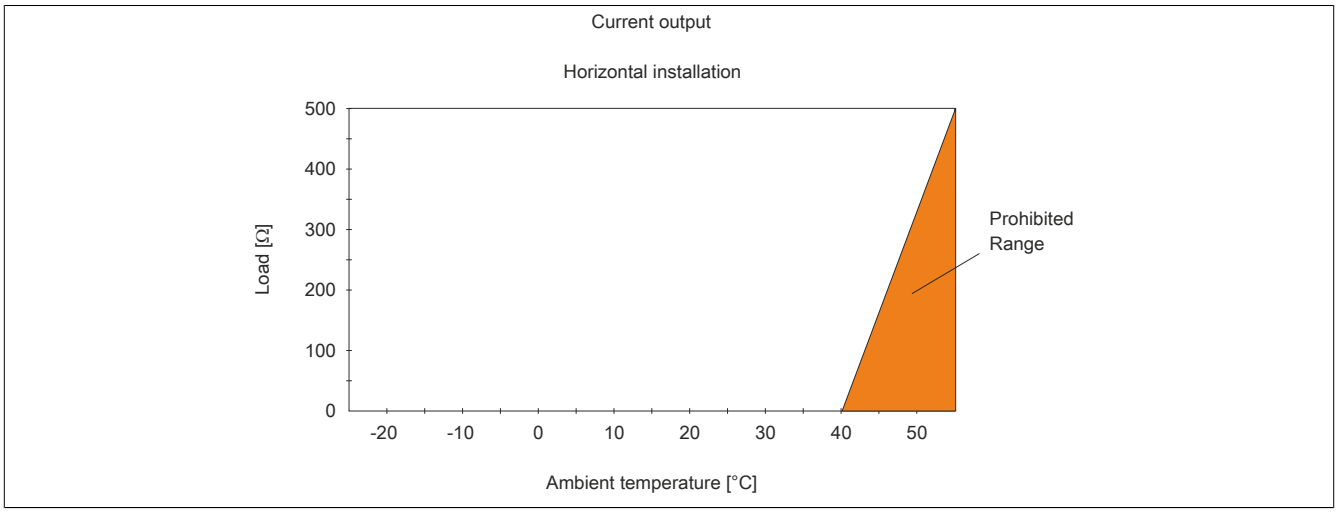


Figure 162: Derating the load with a voltage output and horizontal mounting



Vertical installation

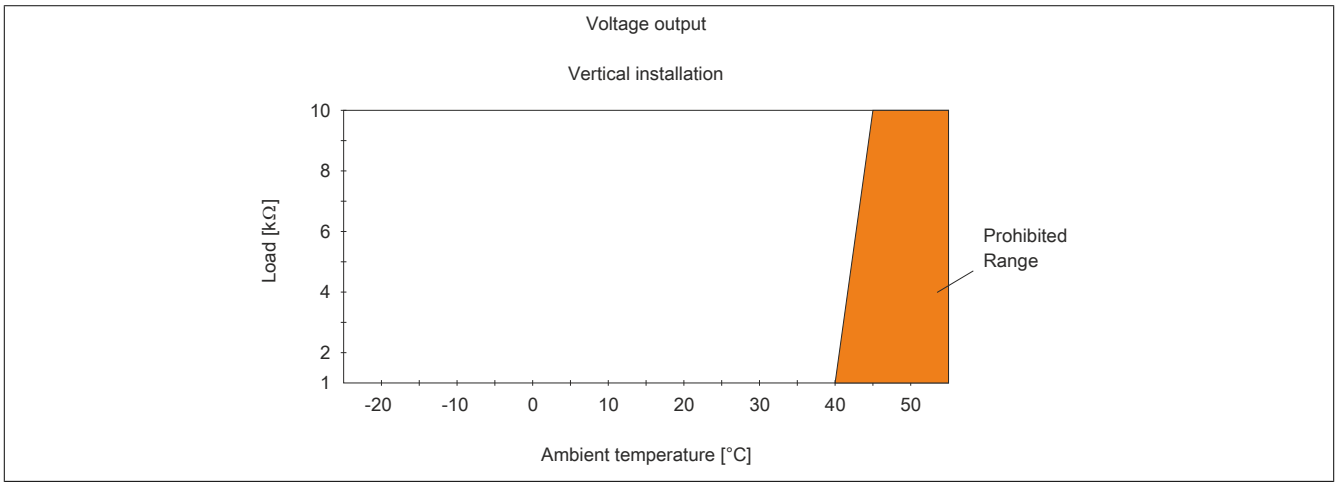
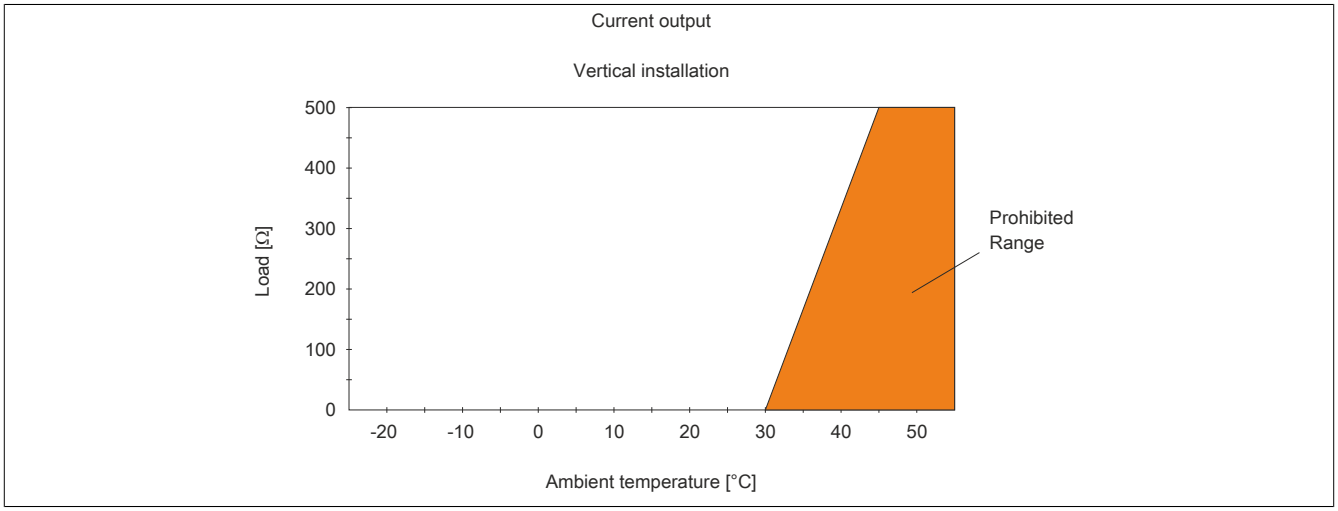


Figure 163: Derating the load with a voltage output and vertical mounting



4.4.10.9 Register description

4.4.10.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.4.10.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
0	ConfigOutput01	UINT				●
Communication						
2	AnalogOutput01	INT			●	
4	AnalogOutput02	INT			●	
6	AnalogOutput03	INT			●	
8	AnalogOutput04	INT			●	

4.4.10.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration							
0	-	ConfigOutput01	UINT				●
Communication							
2	0	AnalogOutput01	INT			●	
4	2	AnalogOutput02	INT			●	
6	4	AnalogOutput03	INT			●	
8	6	AnalogOutput04	INT			●	

1) The offset specifies the position of the register within the CAN object.

4.4.10.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.4.10.9.4 Analog outputs

Each channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.

4.4.10.9.4.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput04

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage; Bus controller default setting: 0
	0 to 32767	Current

4.4.10.9.4.2 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal
		1	Current signal
...		...	
11	Channel 4	0	Voltage signal
		1	Current signal
12 - 15	Reserved	0	

4.4.10.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.4.10.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.5 Bus controllers

The bus controllers adhere to the completely modular strategy used for the I/O modules. Made up of a base module, a supply module to supply the voltage for the entire system, and a fieldbus interface, the bus controller is an extremely flexible fieldbus connection.

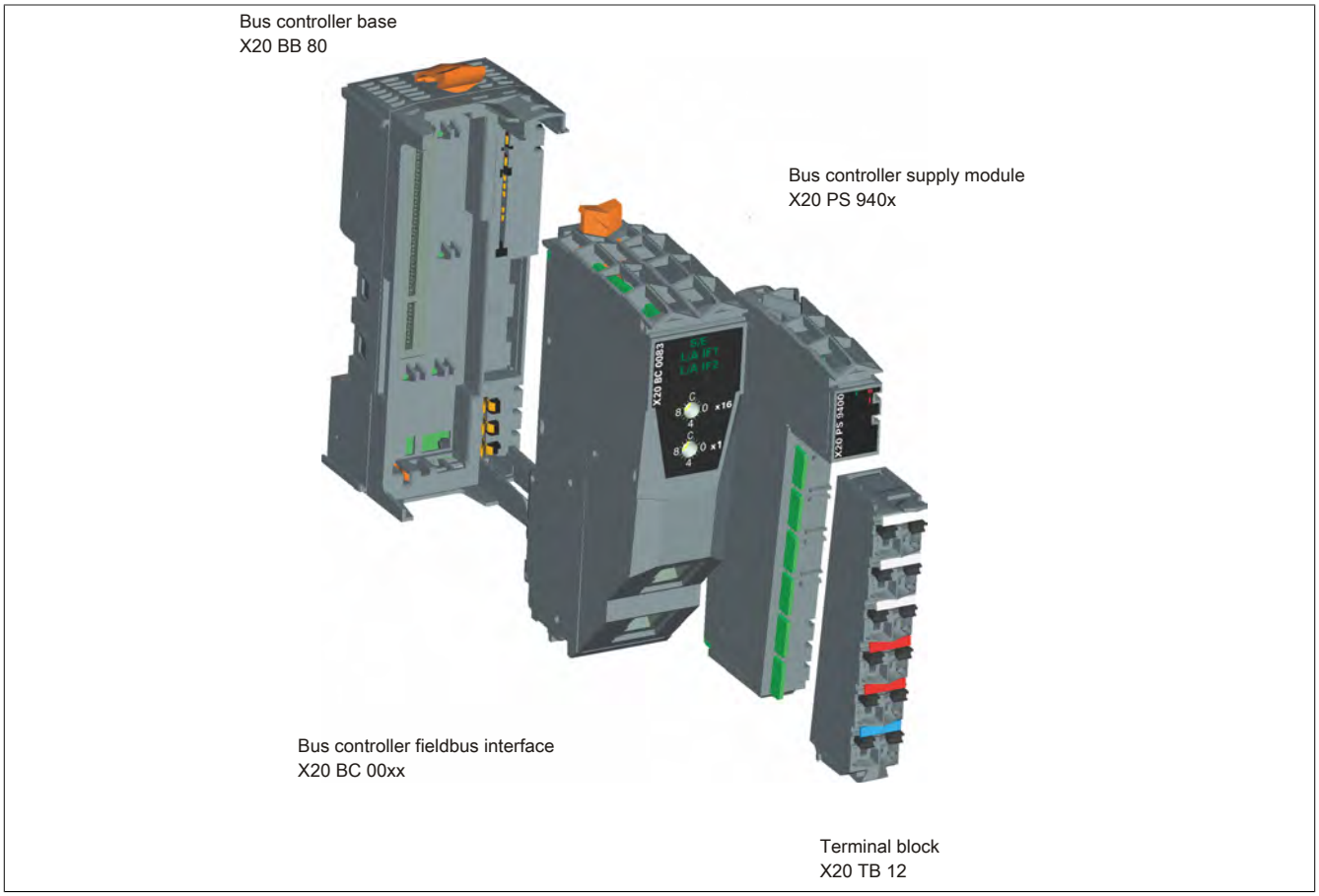


Figure 164: The four parts of a bus controller - fieldbus interface, base module, supply module, terminal block

The entire backplane can be preinstalled. With the removable terminals, the entire system can be wired separately from the electronics module. The individual modules are put in place during commissioning. This is where the I/O system is adapted to the fieldbus being used.

Unlike the Compact CPU with integrated fieldbus connection, the bus controller does not need to be programmed in order to transfer or receive the I/O data on the fieldbus. It can be configured on the fieldbus master.

4.5.1 Brief information

Product ID	Short description	on page
X20BC0043	X20 bus controller, 1 CANopen interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately	717
X20BC0043-10	X20 bus controller, 1 CANopen interface, FieldbusDESIGNER supported, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately	724
X20BC0053	X20 bus controller, 1 DeviceNet interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately	731
X20BC0063	X20 bus controller, 1 PROFIBUS DP interface, 9-pin DSUB connection, order bus base, power supply module and terminal block separately	737
X20BC0073	X20 bus controller, 1 CAN I/O interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately	741
X20BC0083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, 2x RJ45, order bus base, power supply module and terminal block separately.	747
X20BC0087	X20 bus controller, 1 Modbus TCP or Modbus UDP interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately.	753
X20BC0088	X20 bus controller, 1 EtherNet/IP interface, integrated switch, web interface, 2x RJ45, order bus base, power supply module and terminal block separately	759
X20BC00E3	X20 bus controller, 1 PROFINET RT interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately.	764
X20BC00G3	X20 bus controller, 1 EtherCAT interface, 2x RJ45, order bus base, power supply module and terminal block separately	770
X20BC0143-10	X20 bus controller, 1 CANopen interface, 9-pin DSUB, FieldbusDESIGNER supported, order 1x 7AC911.9 terminal block separately Order bus base, power supply module and terminal separately	774
X20cBC0083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, 2x RJ45, order bus base, power supply module and terminal block separately	747
X20cBC0087	X20 bus controller, coated, Modbus/TCP or Modbus/UDP interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately	753
X20cBC0088	X20 bus controller, coated, 1 EtherNet/IP interface, integrated switch, web interface, 2x RJ45, order bus base, power supply module and terminal block separately	759
X20cBC00E3	X20 bus controller, coated, 1 PROFINET RT interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately	764

4.5.2 X20BC0043

4.5.2.1 General information

CAN (Controller Area Network) systems are widespread in the field of automation technology. CAN topology is based on a line structure and uses twisted wire pairs for data transfer. CANopen is a higher-layer protocol based on CAN. As a standardized protocol, it provides a high degree of flexibility for implementing a wide range of configurations.

The X20BC0043-10 bus controller makes it possible to connect up to 253 X2X Link I/O nodes to CANopen. A transition between IP20 and IP67 protection outside of the control cabinet is possible by aligning X20, X67 or XV modules one after the other as needed at distances up to 100m. All CANopen transmission types such as synchronous, event and polling modes are supported together with PDO linking, life/node guarding, emergency objects, and much more.

- Fieldbus: CANopen
- I/O configuration via the fieldbus
- 20 receiver PDOs and 20 sender PDOs
- Select between entry of a fixed transfer rate or automatic transfer rate detection.
- Integrated terminating resistor

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

The B&R FieldbusDESIGNER can be used to create configuration files (e.g. DCF files) in six easy steps. All other function models are also supported by transferring configuration data to the bus controller (e.g. from the master environment with an SDO download or via the serial interface).

The B&R FieldbusDESIGNER is available free of charge in the download section of the B&R website www.br-automation.com.

4.5.2.2 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0043	X20 bus controller, 1 CANopen interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 104: X20BC0043 - Order data

4.5.2.3 Technical data

Product ID	X20BC0043
Short description	
Bus controller	CANopen slave
General information	
B&R ID code	0x1F1A
Status indicators	Module status, bus function, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	
Bus	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Fieldbus - X2X Link	No
Fieldbus - I/O	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
Fieldbus	CANopen slave
Design	5-pin male multipoint connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Default transfer rate	Automatic transfer rate detection or fixed rate setting
Min. cycle time 2)	
Fieldbus	No limitations
X2X Link	400 µs
Synchronization between bus systems possible	No
Terminating resistor	Integrated in the module
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB2105 terminal block separately Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately
Spacing 3)	37.5 $^{+0.2}$ mm

Table 105: X20BC0043 - Technical data

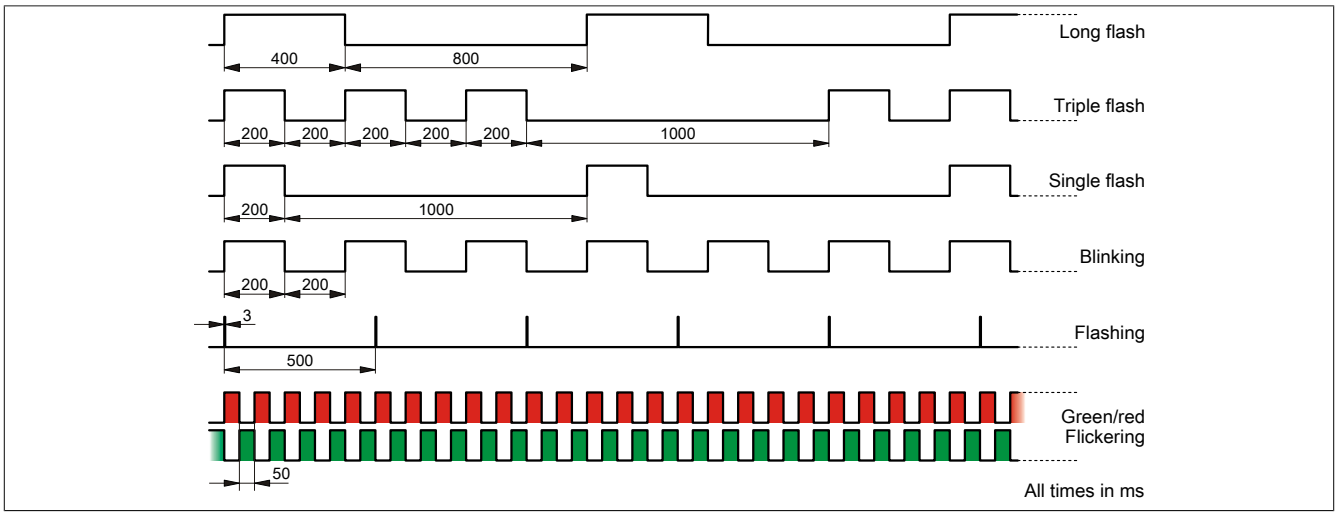
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.2.4 LED status indicators

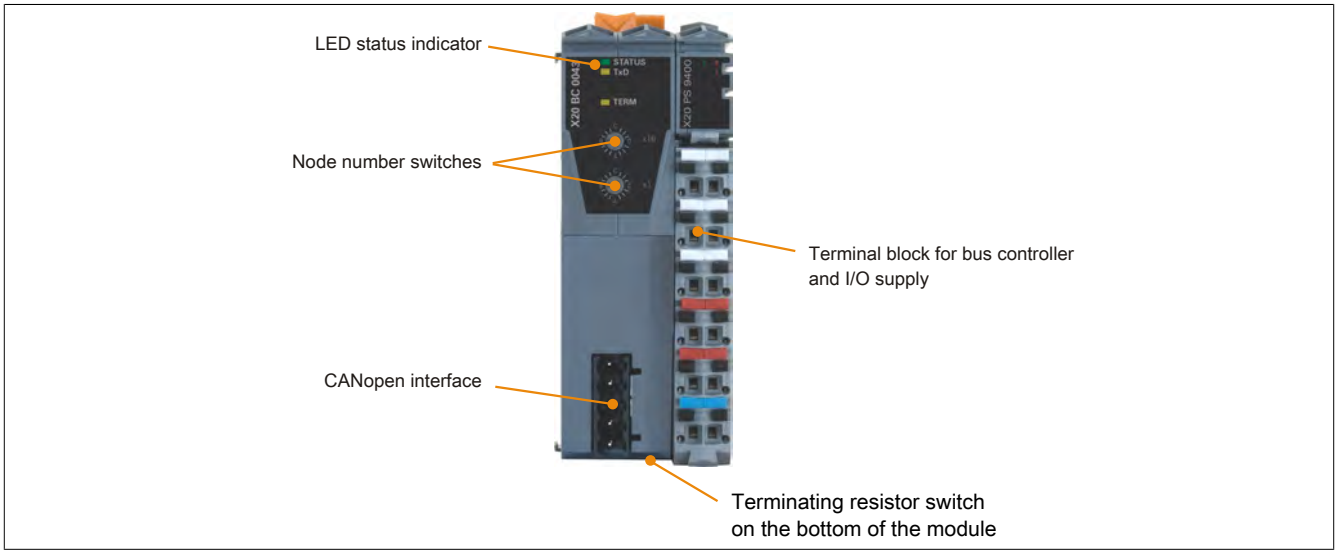
Figure	LED	Color	Status	Description
	STATUS[1]	Green	Off	No power supply
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Single flash	STOP mode
			Flashing	Flash delete in progress
		Red	Off	No power supply or everything is OK
			Single flash	Bus errors
			On	Bus errors: Bus is off
			Triple flash	Transfer rate selection
			Long flash	Invalid node switch position
		Green/red	Flickering	Transfer rate detection in progress
	TxD	Yellow	Off	The bus controller is not transmitting any data via the CANopen fieldbus
			On	The bus controller is transmitting data via the CANopen fieldbus
	TERM	Yellow	Off	The terminating resistor integrated in the bus controller is turned off
			On	The terminating resistor integrated in the bus controller is turned on

1) The "STATUS" LED is a green/red dual LED.

Status LED - Blinking patterns

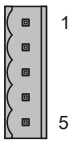


4.5.2.5 Operating and connection elements

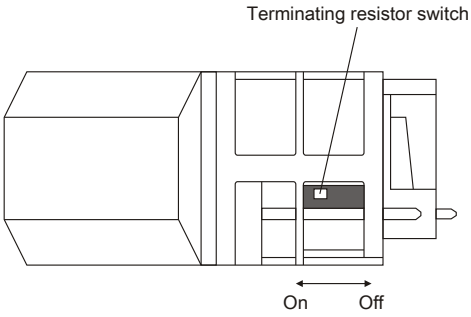


4.5.2.6 CAN bus interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	**Terminal**	**Function**	
	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	

4.5.2.7 Terminating resistor



A terminating resistor is already integrated on the bus controller. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.5.2.8 Node number and transfer rate

Node numbers and transfer rates are configured using the two bus controller number switches.

The transfer rate can be specified in two ways:

- Automatic detection by bus controller (see 4.5.2.9 "Automatic transfer rate detection")
- Fixed definition by user (see 4.5.2.10 "Setting the transfer rate")

Switch position	Node number	Transfer rate
0x00	Not allowed	-
0x01 - 0x7F	1 - 127	Automatically set by the bus controller (default) or fixed setting by the user
0x80 - 0x88	-	Sets a fixed transfer rate
0x89	-	Sets automatic transfer rate detection
0x8A - 0x8F	Not allowed	-
0x90	Clearing the parameters See section 4.5.2.11 "Clearing parameters"	-
0x91 - 0xFF	Not allowed	-

4.5.2.9 Automatic transfer rate detection

After booting, the bus controller goes into "Listen only" mode. This means the bus controller behaves passively on the bus and only listens.

The bus controller attempts to receive valid objects. If receive errors occur, the controller switches to the next transfer rate in the lookup table.

If no objects are received, all transfer rates are tested cyclically. This procedure is repeated until valid objects are received.

Lookup table

The controller tests the transfer rate according to this table. Beginning with the starting transfer rate (1000 kbit/s), the controller switches to the next lower transfer rate. At the end of the table, the bus controller restarts the search from the beginning.

Transfer rate
1000 kbit/s
800 kbit/s
500 kbit/s
250 kbit/s
125 kbit/s
100 kbit/s
50 kbit/s
20 kbit/s
10 kbit/s

4.5.2.10 Setting the transfer rate

The bus controller will detect the transfer rate automatically by default. Switch positions 0x80 - 0x88 can be used to set a fixed transfer rate, or 0x89 can be used to enable automatic transfer rate detection.

Switch position	Transfer rate
0x80	1000 kbit/s
0x81	800 kbit/s
0x82	500 kbit/s
0x83	250 kbit/s
0x84	125 kbit/s
0x85	100 kbit/s
0x86	50 kbit/s
0x87	20 kbit/s
0x88	10 kbit/s
0x89	Automatic transfer rate detection

Table 106: Possible transfer rates

Programming the transfer rate

1. Turn off the power supply to the bus controller.
2. Define the transfer rate to be programmed by setting the node numbers (0x80 - 0x89)
3. Turn on the power supply to the bus controller.
4. Wait until the "MS" LED blinks with a red triple-flash (transfer rate is now programmed).
5. Turn off the power supply to the bus controller.
6. Set the desired node number (0x01 - 0x7F).
7. Turn on the power supply to the bus controller.
8. The bus controller now boots with the set node number and the programmed transfer rate.

4.5.2.11 Clearing parameters

Various parameters can be stored in the bus controller's flash memory:

- Communication parameters
- Vendor-specific parameters
- Application parameters (device profile)
- Programmed transfer rate

Clearing the parameters using switch position 0x90 returns the bus controller to its factory settings.

Clearing the parameters listed above

1. Turn off the power supply to the bus controller.
2. Set the node number to 0x90.
3. Turn on the power supply to the bus controller.
4. Wait until the "MS" LED flashes green. The node number switch must be set to 0x00 and then back to 0x090 within this time window of 5 seconds (rotate the top switch).
5. Wait until the "MS" LED blinks with a red double-flash (parameters have been cleared).
6. Turn off the power supply to the bus controller.
7. Set the desired node number (0x01 - 0x7F).
8. Turn on the power supply to the bus controller.
9. The bus controller boots with the set node number and automatic transfer rate detection.

4.5.2.12 Additional documentation and import files (EDS)

Additional documentation about bus controller functions as well as the necessary import files for the master engineering tool are available in the Downloads section of the B&R website (www.br-automation.com).

4.5.3 X20BC0043-10

4.5.3.1 General information

CAN (Controller Area Network) systems are widespread in the field of automation technology. CAN topology is based on a line structure and uses twisted wire pairs for data transfer. CANopen is a higher-layer protocol based on CAN. As a standardized protocol, it provides a high degree of flexibility for implementing a wide range of configurations.

The X20BC0043-10 bus controller makes it possible to connect up to 253 X2X Link I/O nodes to CANopen. A transition between IP20 and IP67 protection outside of the control cabinet is possible by aligning X20, X67 or XV modules one after the other as needed at distances up to 100m. All CANopen transmission types such as synchronous, event and polling modes are supported together with PDO linking, life/node guarding, emergency objects, and much more.

- Fieldbus: CANopen
- Auto-configuration of I/O modules
- I/O configuration via the fieldbus (also supported by the B&R FieldbusDESIGNER)
- Constant response times even with large amounts of data (max. 32 Rx and 32 Tx PDOs)
- Configurable I/O cycle (0.5 to 4 ms)
- Possible to configure the transfer rate or have it detected automatically
- Heartbeat consumer and producer
- Emergency producer
- 2x SDO server, NMT slave
- Simple bootup (autostart)
- Terminal access via the serial interface on the X20PS9400
- Integrated terminating resistor

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

The B&R FieldbusDESIGNER can be used to create configuration files (e.g. DCF files) in six easy steps. All other function models are also supported by transferring configuration data to the bus controller (e.g. from the master environment with an SDO download or via the serial interface).

The B&R FieldbusDESIGNER is available free of charge in the download section of the B&R website www.br-automation.com.

4.5.3.2 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0043-10	X20 bus controller, 1 CANopen interface, FieldbusDESIGNER supported, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 107: X20BC0043-10 - Order data

4.5.3.3 Technical data

Product ID	X20BC0043-10
Short description	
Bus controller	CANopen slave
General information	
B&R ID code	0xA8B8
Status indicators	Module status, bus function, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED and software
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	
Bus	2 W
Electrical isolation	
Fieldbus - X2X Link	No
Fieldbus - I/O	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
Fieldbus	CANopen slave
Design	5-pin male multipoint connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Default transfer rate	Automatic transfer rate detection or fixed rate setting
Min. cycle time [2)]	
Fieldbus	No limitations
X2X Link	500 µs
Synchronization between bus systems possible	No
Terminating resistor	Integrated in the module
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20

Table 108: X20BC0043-10 - Technical data

Product ID	X20BC0043-10
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB2105 terminal block separately Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately
Spacing 3)	37.5 +0.2 mm

Table 108: X20BC0043-10 - Technical data

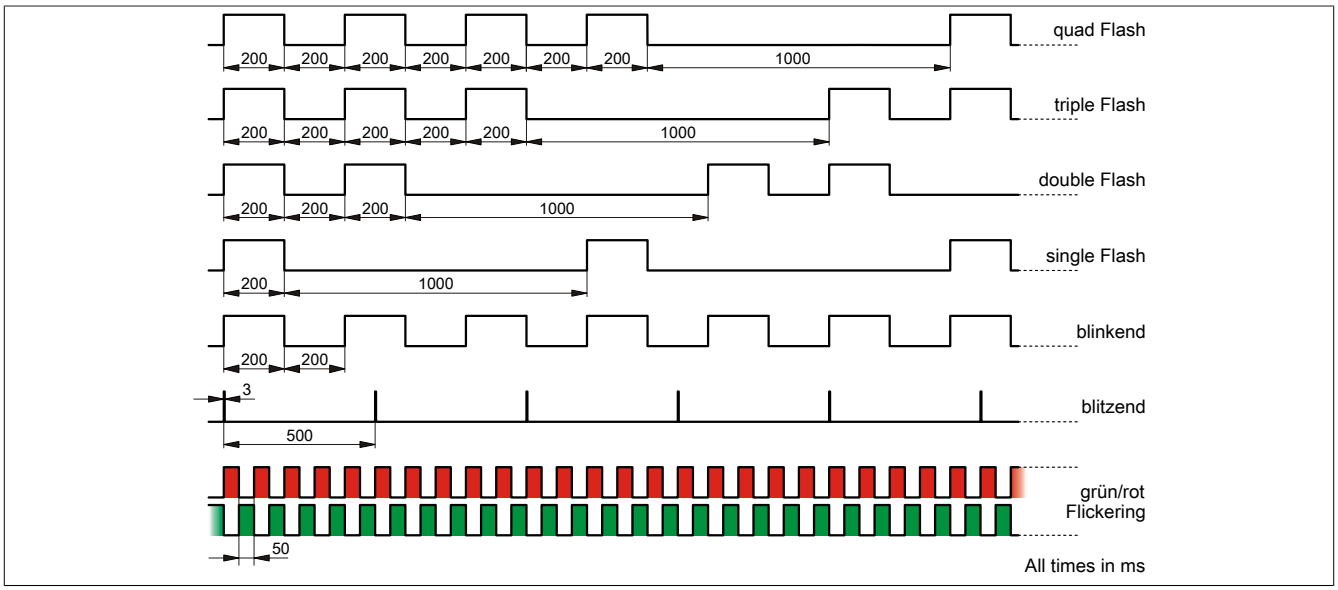
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.3.4 LED status indicators

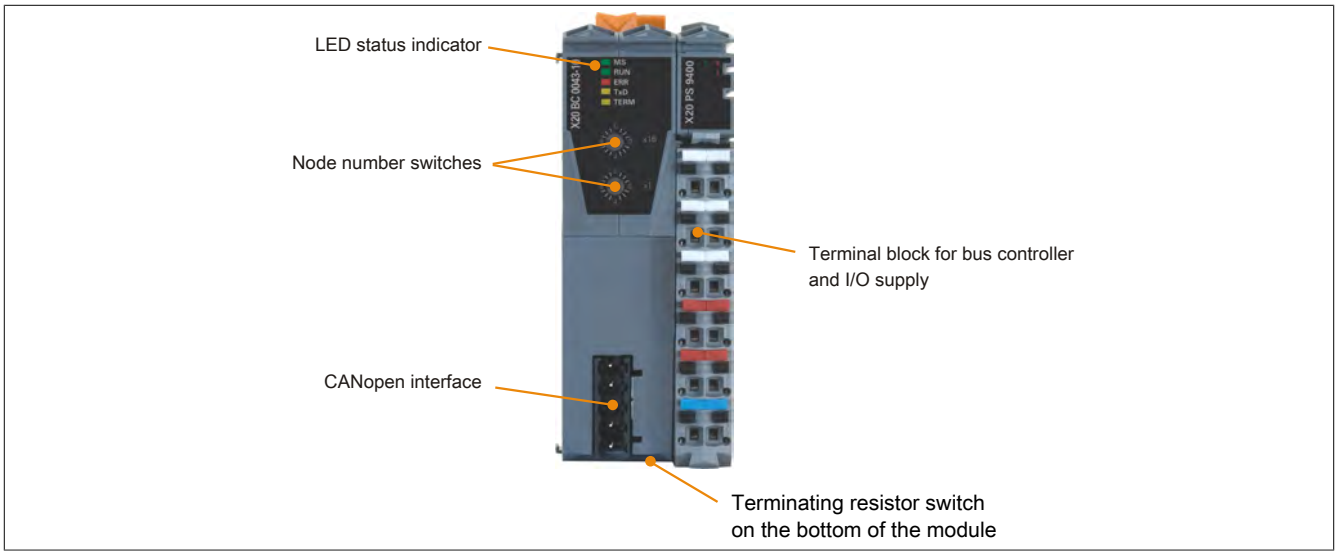
Figure	LED	Color	Status	Description
	MS1)	Green	Off	No power supply
			Flashing	5 second window for deleting all configuration settings
			On	Boot procedure OK, I/O modules OK
		Red	Double flash	Successfully erased flash memory
			Triple flash	Successfully saved transfer rate
			Quad flash	Successfully saved configuration
			On	I/O modules: Error message or incorrect configuration
	RUN	Green	Off	No power supply
			Single flash	STOP mode
			Triple flash	Firmware download in progress
			Blinking	PREOPERATIONAL mode
			On	OPERATIONAL mode
	ERR	Red	Off	No power supply or everything is OK
			Single flash	CAN warning limit reached
			Double flash	Node guarding / heartbeat error
			Blinking	Invalid node number or configuration
			On	Bus errors: Bus off
	RUN/ERR	Green/red	Flickering	Transfer rate detection in progress
	TxD	Yellow	Off	The bus controller is not transmitting any data via the CANopen fieldbus
			On	The bus controller is transmitting data via the CANopen fieldbus
	TERM	Yellow	Off	The terminating resistor integrated in the bus controller is turned off
			On	The terminating resistor integrated in the bus controller is turned on

1) The "MS" LED is a green/red dual LED. The LED blinks red several times immediately after startup. This is a boot message, however, and not an error.

Status LEDs - Blinking patterns



4.5.3.5 Operating and connection elements

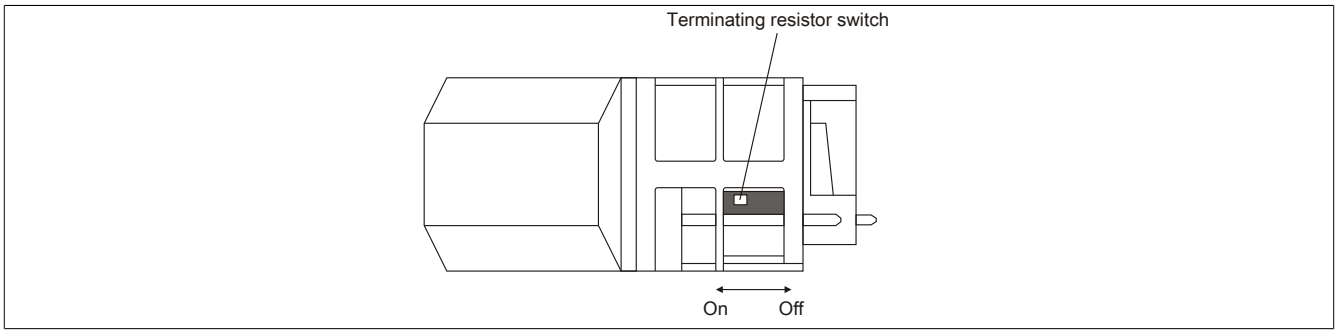


4.5.3.6 CAN bus interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
	Terminal	Function	
 1 5	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	
5-pin male multipoint connector			

4.5.3.7 Terminating resistor



A terminating resistor is already integrated on the bus controller. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.5.3.8 Node number and transfer rate

Node numbers and transfer rates are configured using the two bus controller number switches.

The transfer rate can be specified in two ways:

- Automatic detection by bus controller (see 4.5.2.9 "Automatic transfer rate detection")
- Fixed definition by user (see 4.5.2.10 "Setting the transfer rate")

Switch position	Node number	Transfer rate
0x00	Not allowed	-
0x01 - 0x7F	1 - 127	Automatically set by the bus controller (default) or fixed setting by the user
0x80 - 0x88	-	Sets a fixed transfer rate
0x89	-	Sets automatic transfer rate detection
0x8A - 0x8F	Not allowed	-
0x90	Clearing the parameters See section 4.5.2.11 "Clearing parameters"	-
0x91	Not allowed	-
0x92	Save configuration[1)] See section 4.5.3.11 "Save automatic configuration"	-
0x93 - 0xFF	Not allowed	-

1) This function is available starting with Hardware version E0 or Firmware version V0001.0107.

4.5.3.9 Automatic transfer rate detection

After booting, the bus controller goes into "Listen only" mode. This means the bus controller behaves passively on the bus and only listens.

The bus controller attempts to receive valid objects. If receive errors occur, the controller switches to the next transfer rate in the lookup table.

If no objects are received, all transfer rates are tested cyclically. This procedure is repeated until valid objects are received.

Lookup table

The controller tests the transfer rate according to this table. Beginning with the starting transfer rate (1000 kbit/s), the controller switches to the next lower transfer rate. At the end of the table, the bus controller restarts the search from the beginning.

Transfer rate
1000 kbit/s
800 kbit/s
500 kbit/s
250 kbit/s
125 kbit/s
100 kbit/s
50 kbit/s
20 kbit/s
10 kbit/s

4.5.3.10 Setting the transfer rate

The bus controller will detect the transfer rate automatically by default. Switch positions 0x80 - 0x88 can be used to set a fixed transfer rate, or 0x89 can be used to enable automatic transfer rate detection.

Switch position	Transfer rate
0x80	1000 kbit/s
0x81	800 kbit/s
0x82	500 kbit/s
0x83	250 kbit/s
0x84	125 kbit/s
0x85	100 kbit/s
0x86	50 kbit/s
0x87	20 kbit/s
0x88	10 kbit/s
0x89	Automatic transfer rate detection

Table 109: Possible transfer rates

Programming the transfer rate

1. Turn off the power supply to the bus controller.
2. Define the transfer rate to be programmed by setting the node numbers (0x80 - 0x89)
3. Turn on the power supply to the bus controller.
4. Wait until the "MS" LED blinks with a red triple-flash (transfer rate is now programmed).
5. Turn off the power supply to the bus controller.
6. Set the desired node number (0x01 - 0x7F).
7. Turn on the power supply to the bus controller.
8. The bus controller now boots with the set node number and the programmed transfer rate.

4.5.3.11 Save automatic configuration

The node number position 0x92 can be used to save automatically generated configurations. This makes it possible to work with a standardized configuration without having to adapt the application to changes associated with service work or different development stages for example.

1. Turn off the power supply to the bus controller.
2. Set the node number to 0x90.
3. Turn on the power supply to the bus controller.
4. Wait until the "MS" LED flashes green.
5. The node number switch must be set to 0x00 and then back to 0x90 within this time window of 5 seconds (rotate the top switch).
6. Wait until the "MS" LED blinks with a red double-flash (parameters have been cleared).
7. Turn off the power supply to the bus controller.
8. Set the node number to 0x92.
9. Turn on the power supply to the bus controller.
10. Wait until the "MS" LED flashes green.
11. The node number switch must be set to 0x02 and then back to 0x092 within this time window of 5 seconds (rotate the top switch).
12. Wait until the "MS" LED blinks with a red quad-flash (parameters have been saved).
13. Turn off the power supply to the bus controller.
14. Set the desired node number (0x01 - 0x7F).
15. Turn on the power supply to the bus controller.
16. The bus controller boots with the set node number and automatic transfer rate detection.

Information:

A mapping tool for decoding the saved PDO mapping is available in the Download section of the B&R website (www.br-automation.com).

Information:

This function is available starting with Hardware version E0 or Firmware version V0001.0107.

4.5.3.12 Clearing parameters

Various parameters can be stored in the bus controller's flash memory:

- Communication parameters
- Vendor-specific parameters
- Application parameters (device profile)
- Programmed transfer rate

Clearing the parameters using switch position 0x90 returns the bus controller to its factory settings.

Clearing the parameters listed above

1. Turn off the power supply to the bus controller.
2. Set the node number to 0x90.
3. Turn on the power supply to the bus controller.
4. Wait until the "MS" LED flashes green. The node number switch must be set to 0x00 and then back to 0x090 within this time window of 5 seconds (rotate the top switch).
5. Wait until the "MS" LED blinks with a red double-flash (parameters have been cleared).
6. Turn off the power supply to the bus controller.
7. Set the desired node number (0x01 - 0x7F).
8. Turn on the power supply to the bus controller.
9. The bus controller boots with the set node number and automatic transfer rate detection.

4.5.3.13 Additional documentation and import files (EDS)

Additional documentation about bus controller functions as well as the necessary import files for the master engineering tool are available in the Downloads section of the B&R website (www.br-automation.com).

4.5.4 X20BC0053

4.5.4.1 General information

DeviceNet was developed by Allen Bradley as a CAN bus based automation network. It is based on a producer/consumer protocol. From the user's point of view, all data is handled separately from CAN bus transfer possibilities (e.g. longer data packets are automatically fragmented by DeviceNet). Access occurs using I/O messages with defined properties.

The bus controller makes it possible to connect X2X Link I/O nodes to DeviceNet. It has automatic transfer rate detection, auto scan, automatic mapping and automatic configuration of the I/O modules. Explicit messaging, change of state, cyclic, polled and bit strobe are supported as transfer modes. In addition to the standard communication objects, there are also manufacturer-specific objects used to represent the modular X20 System in the best manner possible.

X20 and other modules that are based on X2X Link can be connected to the bus controller. The entire configuration of this type of modular system is supported by the DeviceNet standard. Allen Bradley developed the modular I/O configuration to simplify the necessary configuration steps. The DeviceNet bus controllers from B&R also support this type of configuration.

- Fieldbus: DeviceNet
- I/O configuration via the fieldbus
- Support of both linear and modular (Allen Bradley) configuration systems
- Auto scan, automatic I/O mapping of the I/Os
- Automatic I/O configuration (starting with Rev. D0, firmware version 1.23)
- Integrated terminating resistor

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

4.5.4.2 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0053	X20 bus controller, 1 DeviceNet interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 110: X20BC0053 - Order data

4.5.4.3 Technical data

Product ID	X20BC0053
Short description	
Bus controller	DeviceNet adapter (slave)
General information	
B&R ID code	0x1F1B
Status indicators	Module status, bus function, 24V DeviceNet voltage, data transfer, terminating resistor.

Table 111: X20BC0053 - Technical data

Product ID	X20BC0053
Diagnostics	
24 V DeviceNet voltage	Yes, with LED status indicators (MOD and NET)
Module status	Yes, using status LED and software
Bus function	Yes, using status LED
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	
Bus	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Fieldbus - X2X Link	No
Fieldbus - I/O	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
Fieldbus	DeviceNet adapter (slave)
Design	5-pin male multipoint connector
Max. distance	500 m
Transfer rate	Max. 500 kbit/s
Default transfer rate	Automatic transfer rate detection
Min. cycle time 2)	
Fieldbus	No limitations
X2X Link	400 µs
Synchronization between bus systems possible	No
Terminating resistor	Integrated in the module
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB2105 terminal block separately Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately
Spacing 3)	37.5 $^{+0.2}$ mm

Table 111: X20BC0053 - Technical data

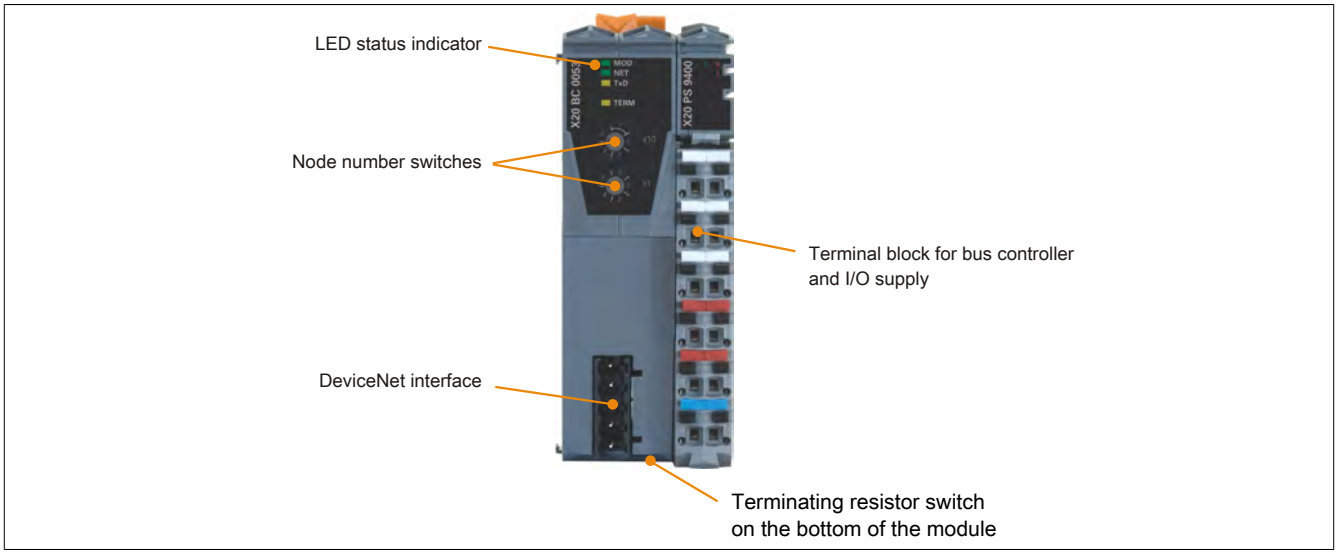
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.4.4 LED status indicators

Figure	LED	Color	Status	Description
	MOD[1]	Green	Off	Bus sense error: If the "NET" LED is also "off", there is no 24 V DeviceNet voltage. No transfer rate: If the PS9400's "RUN" LED is active (PREOPERATIONAL or RUN mode), the automatic transfer rate detection is still running or no transfer rate could be detected.
			On	RUN mode: The 24 V DeviceNet voltage is OK and the module is operating under normal conditions.
			Blinking	Standby mode: Configuration is missing, incomplete, or incorrect.
		Red	Blinking	Recoverable Fault mode:
		Green/red	Blinking	Module is performing a self test.
	NET[1]	Green	Off	No power, offline: • Bus sense error: If the "MOD" LED is also off, there is no 24 V DeviceNet voltage. • No transfer rate: If the PS9400's "RUN" LED is active (PREOPERATIONAL or RUN mode), the automatic transfer rate detection is still running or no transfer rate could be detected. • Module has not yet completed a duplicate MAC-ID test.
			Blinking	Online, not connected: • The module has carried out the duplicate MAC-ID test and is online. • There is no established connection to a master/scanner.
			On	Everything is OK: A connection to the master/scanner (explicit or I/O) is set up.
		Red	Blinking	Connection timeout: The time for an I/O connection has expired.
			On	Critical connection error - fieldbus communication no longer possible: • Duplicate MAC ID error • Bus off • Receive/transmit overrun
	TxD	Yellow	Off	The bus controller is not transmitting any data via the DeviceNet fieldbus
			On	The bus controller is transmitting data via the DeviceNet fieldbus
	TERM	Yellow	Off	The terminating resistor integrated in the bus controller is turned off
			On	The terminating resistor integrated in the bus controller is turned on

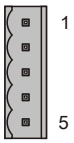
1) The "MOD" and "NET" LEDs are green/red dual LEDs.

4.5.4.5 Operating and connection elements



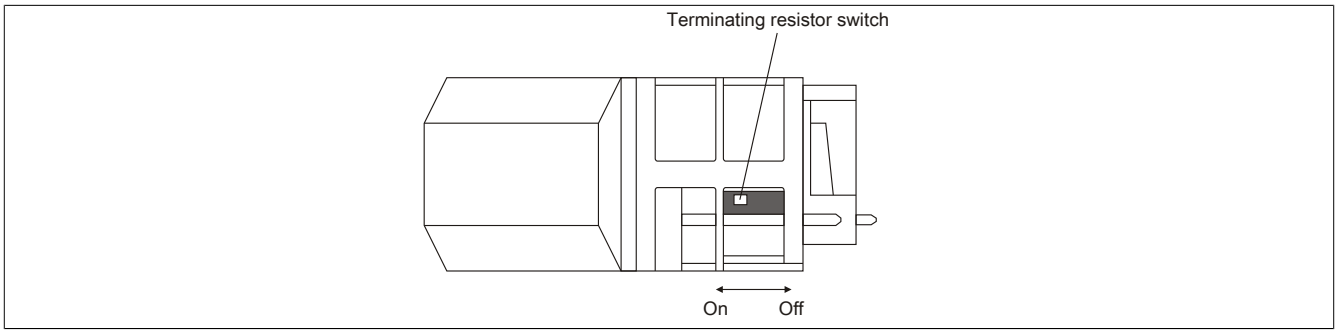
4.5.4.6 DeviceNet interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	**Terminal**	**DeviceNet**	
	1	CAN⊥ (V-)	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	V+	Supply voltage[1)]

1) The 24 VDC in the DeviceNet network must be fed in externally in order to guarantee correct operation and data exchange. 24 VDC is not made available by the device.

4.5.4.7 Terminating resistor

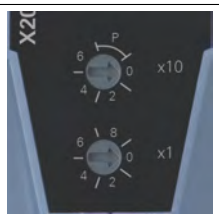


A terminating resistor is already integrated on the bus controller. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.5.4.8 Node number

The MAC ID is configured using the two address switches on the bus controller.

The configurable range lies between 0 and 63. This value range is required in the DeviceNet specifications for a DeviceNet device.



Switch position	MAC ID
00 - 63	0 - 63
64	The MAC ID can be configured by setting the address switch using the master/scanner software.
65 - 89	Not permitted
90	"Clearing parameters"
91 - 94	Not permitted
95	"Automatic configuration"
96 - 99	Not permitted

4.5.4.9 Automatic transfer rate detection

After booting, the bus controller goes into "Listen only" mode. This means the bus controller behaves passively on the bus and only listens.

The bus controller attempts to receive valid objects. If receive errors occur, the controller switches to the next transfer rate in the lookup table.

If no objects are received, all transfer rates are tested cyclically. This procedure is repeated until valid objects are received, indicating that the correct transfer rate has been determined. Only transfer rates permitted by the DeviceNet specification are tested.

Lookup table

The controller tests the transfer rate according to this table. Beginning with the starting transfer rate (500 kbit/s), the controller switches to the next lower transfer rate. At the end of the table, the bus controller restarts the search from the beginning.

Transfer rate
500 kbit/s
250 kbit/s
125 kbit/s

Table 112: Transfer rate lookup table

Information:

While automatic transfer rate recognition is running, both DeviceNet LEDs are switched off (because there is no LED status definition in the DeviceNet specifications for this status).

To ensure that the module has been supplied and booted, this manufacturer specific status definition requires the X20PS9400 RUN LED to be active.

4.5.4.10 Clearing parameters

Various parameters can be stored in the bus controller's flash memory. Deleting these parameters using switch position 90 returns the bus controller to its factory settings.

Deleting the parameters

1. Turn off the power supply to the bus controller.
2. Set the node number to 90
3. Turn on the power supply to the bus controller.
4. Wait until the "MOD" LED flashes green for 5 s (3 ms on / 500 ms off). The node number switch "x10" must be set to 0 and then back to 9 within this time window.
5. Wait until the "MOD" LED blinks with a red double-flash (parameters have been cleared).
6. Turn off the power supply to the bus controller.
7. Set the desired node number (00 - 63).
8. Turn on the power supply to the bus controller.
9. The bus controller boots with the set node number and automatic transfer rate detection.

4.5.4.11 Automatic configuration of the I/O modules

The automatic configuration of the connected I/O modules by the bus controller is supported starting with Rev.D0 (firmware ≥V 1.23) of the bus controller.

To prevent the configuration data from being accidentally overwritten on the bus controller, the procedure described below must be followed when creating the configuration data. When doing this, it is important that all required I/O modules are also started when booting the bus controller (i.e. supplied with power). This is especially important when using potential groups (E-stop switches).

The automatic configuration sets the following attributes of class 0x65 on the individual I/O modules:

- Module type (0x01)
- Input length (0x03)
- Output length (0x05)

Additional parameters are not set. That means that the connected modules are configured with their standard settings and standard I/O lengths. This can be changed by editing the parameters in the respective master engineering tool.

Automatic configuration

1. Turn off the power supply to the bus controller.
2. Set node number switch to 95 (this is done by turning "x10" switch right to the position "P" and the "x1" switch to 5).
3. Turn on the power supply to the bus controller.
4. Wait until the "MOD" LED starts blinking green (3 ms on / 500 ms off). This phase of green blinking lasts 5 s. The node number "x10" switch must be set to 0 within this time frame and then set back to 9.
5. Wait until the "MOD" LED blinks (4 red flashes). The old configuration data is now deleted completely and overwritten with the new values from the connected I/O modules.
6. Turn off the power supply to the bus controller.
7. Set the desired node number (00 to 63).
8. Turn on the power supply to the bus controller.
9. The bus controller boots using the set node number, automatic transfer rate recognition and standard settings from the connected I/O modules.

4.5.4.12 Additional documentation and import files (EDS)

Additional documentation about bus controller functions as well as the necessary import files for the master engineering tool are available in the Downloads section of the B&R website (www.br-automation.com).

4.5.5 X20BC0063

4.5.5.1 General information

PROFIBUS DP is based on the physics of the RS485 interface. Data transfer is controlled using a hybrid bus access procedure. Active stations receive communication rights via a token passing procedure and can then access all stations on the network according to the master-slave principle. The maximum time of circulation for a token can be configured, which results in a defined cycle time.

Access represents various services for the user for both cyclic and for non-cyclic data transfer.

The bus controller makes it possible to connect X2X Link I/O nodes to PROFIBUS DP. It supports PROFIBUS DP with all of its options and other additional properties. In addition to the device, module, and channel diagnostics provided in the PROFIBUS standard, it is also possible, for example, to switch to the slot diagnostics option in S7 format. X20 or other modules that are based on X2X Link can be connected to the bus controller. Modular system configurations are optimally supported by PROFIBUS DP.

- Fieldbus: PROFIBUS DP
- I/O configuration via the fieldbus
- Extensive device, module, and channel diagnosis according to PROFIBUS DP standard
- Communication with X2X Link I/O nodes even works when some nodes are missing or without power

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

4.5.5.2 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0063	X20 bus controller, 1 PROFIBUS DP interface, 9-pin DSUB connection, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	Infrastructure components	
0G1000.00-090	Bus connector, RS485, for PROFIBUS networks	

Table 113: X20BC0063 - Order data

4.5.5.3 Technical data

Product ID	X20BC0063
Short description	
Bus controller	PROFIBUS DP V0 slave
General information	
B&R ID code	0x1F1C
Status indicators	Module status, bus function, data transfer
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED
Data transfer	Yes, using status LED
Power consumption	
Bus	2.3 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Fieldbus - X2X Link	No
Fieldbus - I/O	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Fieldbus	PROFIBUS DP V0 slave
Design	9-pin female DSUB connector
Max. distance	1200 m
Transfer rate	Max. 12 Mbit/s
Default transfer rate	Automatic transfer rate detection
Min. cycle time 2)	
Fieldbus	No limitations
X2X Link	400 µs
Synchronization between bus systems possible	No
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately
Spacing 3)	37.5 $^{+0.2}$ mm

Table 114: X20BC0063 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.5.4 LED status indicators

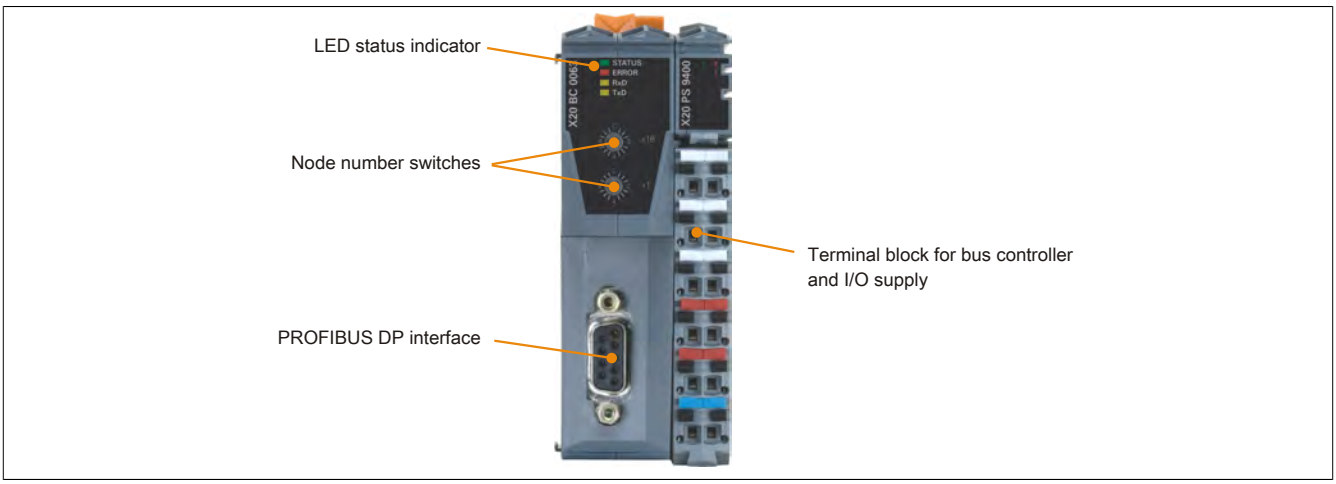
<table>
<tr><th>Figure</th><th>LED</th><th colspan="3">Description</th></tr>
<tr><td rowspan="12"> 
</td><td rowspan="10">STATUS and ERROR</td><td colspan="3">Status indicator for PROFIBUS DP bus controller.</td></tr>
<tr><td>STATUS (green)</td><td>ERROR (red)</td><td>Description</td></tr>
<tr><td>Off</td><td>Off</td><td>HARDWARE FAULT / POWER FAIL</td></tr>
<tr><td>On</td><td>On</td><td>BUS OFF</td></tr>
<tr><td>On</td><td>Blinking</td><td>WAIT FOR CONFIG</td></tr>
<tr><td>Blinking</td><td>Off</td><td>DATA EXCHANGE - DIAGNOSTICS</td></tr>
<tr><td>On</td><td>Off</td><td>DATA EXCHANGE - NO ERROR</td></tr>
<tr><td>Blinking</td><td>Blinking</td><td>CONFIG ERROR</td></tr>
<tr><td>Off</td><td>Blinking</td><td>SERVICE MODE - BOOT</td></tr>
<tr><td>Single flash</td><td>Single flash</td><td>HARDWARE FAULT</td></tr>
<tr><td colspan="3">For a more detailed description see the section 4.5.5.5 "State diagnostics via the Status/Error LEDs".</td></tr>
<tr><td>RxD</td><td colspan="3">This yellow LED lights up when the bus controller is receiving data from the PROFIBUS DP fieldbus.</td></tr>
<tr><td>TxD</td><td colspan="3">This yellow LED lights up when the bus controller is sending data via the PROFIBUS DP fieldbus.</td></tr>
</table>

4.5.5.5 State diagnostics via the Status/Error LEDs

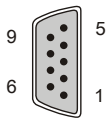
The condition of the PROFIBUS DP bus controller is diagnosed using the LED status indicators "STATUS" and "ERROR".

STATUS (Green)	ERROR (Red)	Function	Solution
Off	Off	HARDWARE FAULT / POWER FAIL	• Check wiring of supply voltage.
On	On	BUS OFF • Baud rate not detected • No connection to the DP master • DP master not active	• Check the PROFIBUS network • Check the PROFIBUS master
On	Blinking	WAIT FOR CONFIG • Transfer rate has been detected, but the PROFIBUS master has not yet configured the bus controller	• Check the node number switch • Check the slave address in the master configuration
Blinking	Off	DATA EXCHANGE - DIAGNOSTICS • The bus controller is still initializing the I/O modules • The I/O modules configured by the master cannot be found • An error has occurred on one or more I/O modules (short circuit, etc.)	• Initialization can take a few seconds depending on the number of I/O modules connected • Check the wiring and power supply for the I/O modules • Read diagnostic messages in the respective PROFIBUS master's engineering tool
On	Off	DATA EXCHANGE • Cyclic data exchange with the PROFIBUS DP master	
Blinking	Blinking	CONFIG ERROR • One or more I/O modules found do not match with the configuration of the PROFIBUS DP master • The configuration received from the PROFIBUS master is invalid	• Check the wiring of the X2X Link and the order of I/O modules • Check configuration of the PROFIBUS master • Read diagnostic messages in the respective PROFIBUS master's engineering tool • Check the configuration being used - it is possible that the number of configured I/O modules is too high
Off	Blinking	SERVICE MODE - BOOT • The bus controller's node number has been set to 255 (0xFF) - after 2 s the bus controller starts in service mode	• Set a valid node number
Single flash	Single flash	HARDWARE FAULT	

4.5.5.6 Operating and connection elements



4.5.5.7 PROFIBUS DP interface

Interface	Pinout		
	Pin	RS485	
 9-pin female DSUB connector	1	Reserved	
	2	Reserved	
	3	RxD/TxD-P	Data[1]
	4	CNTR-P	Transmit enable
	5	DGND	Electrically isolated supply
	6	CP	Electrically isolated supply
	7	Reserved	
	8	RxD/TxD-N	Data\[2]
	9	CNTR-N	Transmit enable\
	CNTR ... Directional switch for external repeater		

1) Cable color: Red
2) Cable color: Green

4.5.5.8 PROFIBUS DP node number switches

The PROFIBUS DP node number is configured using both number switches of the bus controller.

Switch position	Node number
0x00	Not allowed
0x01 - 0x7D	1 to 125
0x7E - 0xFF	Not allowed

4.5.5.9 Automatic transfer rate detection

After booting or after a communication timeout, the bus controller goes into the status "Baud Search". This means the bus controller behaves passively on the bus.

The bus controller always begins the search for the configured transfer rate with the highest transfer rate. If a complete error-free telegram is not received during monitoring time, then the search is continued using the next lowest transfer rate.

Transfer rate
12 Mbit/s
6 Mbit/s
3 Mbit/s
1.5 Mbit/s
500 kbit/s
187.5 kbit/s
93.75 kbit/s
45.45 kbit/s
19.2 kbit/s
9.6 kbit/s

Table 115: Transfer rates supported by the bus controller

4.5.5.10 Additional documentation and import files (EDS)

Additional documentation about bus controller functions as well as the necessary import files for the master engineering tool are available in the Downloads section of the B&R website (www.br-automation.com).

4.5.6 X20BC0073

4.5.6.1 General information

The bus controller makes it possible to connect X2X Link I/O nodes to CAN I/O. CAN I/O is a transfer protocol based on standard CAN bus fully integrated in the B&R system. From the user's point of view, it doesn't matter if I/O points are operated locally or remotely via CAN I/O.

Up to 43 logic I/O modules can be connected to the bus controller. Up to 16 of them can be analog modules.

- Fieldbus: CAN bus
- Automatic firmware update via the fieldbus
- Integrated I/O access in B&R Automation Studio
- Integrated terminating resistor

Information:

The bus controller is unable to detect modules after a gap in the X2X Link station numbers. This can be caused by:

- **X20 modules not being connected**
- **Modules with integrated node number switch, such as the X20BM05**

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

4.5.6.2 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0073	X20 bus controller, 1 CAN I/O interface, order 1x TB2105 terminal block separately Order bus base, power supply module and terminal separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 116: X20BC0073 - Order data

4.5.6.3 Technical data

Product ID	X20BC0073
Short description	
Bus controller	CAN I/O slave
General information	
B&R ID code	0x1F1D
Status indicators	Module status, bus function, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	
Bus	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Fieldbus - X2X Link	No
Fieldbus - I/O	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Fieldbus	CAN I/O slave
Design	5-pin male multipoint connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Default transfer rate	Automatic transfer rate detection or fixed rate setting
Min. cycle time 2)	
Fieldbus	1 ms
X2X Link	1 ms
Synchronization between bus systems possible	No
Terminating resistor	Integrated in the module
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB2105 terminal block separately Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately
Spacing 3)	37.5 $^{+0.2}$ mm

Table 117: X20BC0073 - Technical data

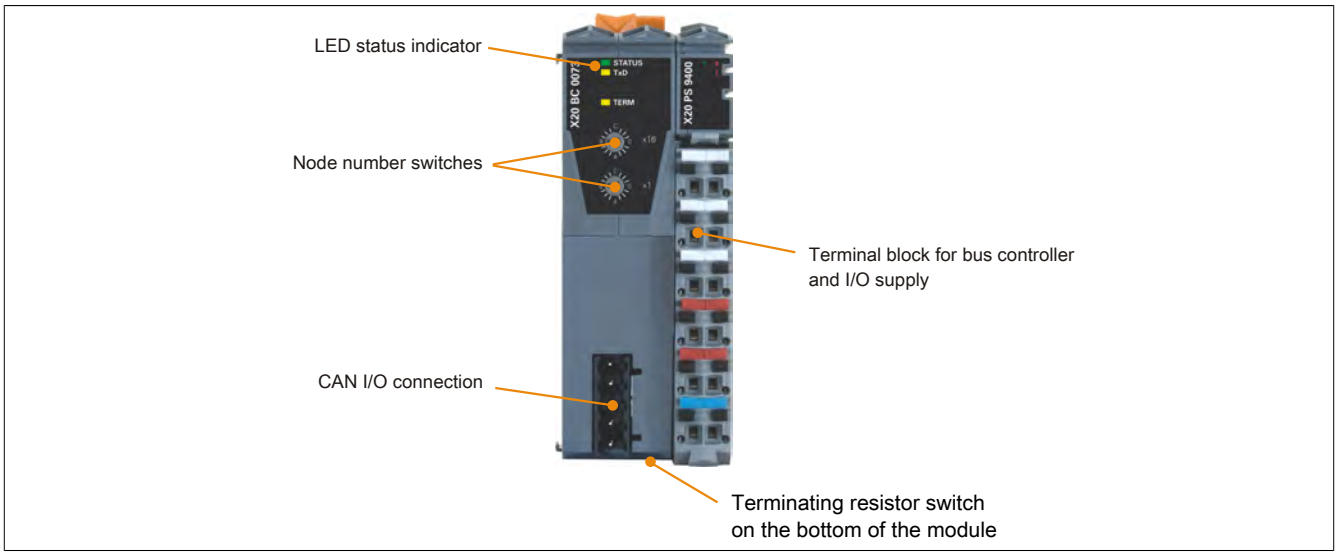
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.6.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS[1)]	Green	Off	No power supply
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	On	CAN connection reports BusOff status
		Green/red	Flickering	Transfer rate detection in progress
		Green blinking / red single flash		PREOPERATIONAL mode; CAN connection reports: Warning limit reached
		Steady green / single red flash		RUN mode; CAN connection reports: Warning limit reached
	TxD	Yellow	Off	The bus controller is not transmitting any data via the CAN I/O fieldbus
			On	The bus controller is transmitting data via the CAN I/O fieldbus
	TERM	Yellow	Off	The terminating resistor integrated in the bus controller is turned off
			On	The terminating resistor integrated in the bus controller is turned on

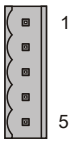
1) The "STATUS" LED is a green/red dual LED.

4.5.6.5 Operating and connection elements

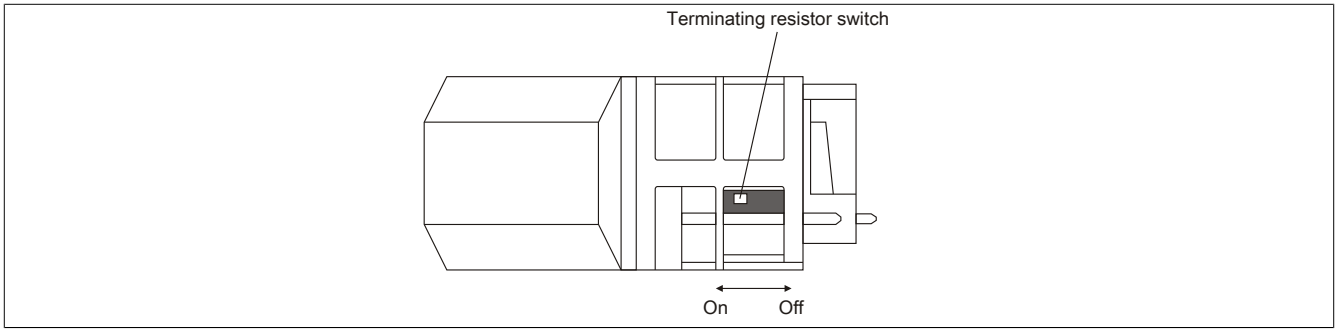


4.5.6.6 CAN bus interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
	Terminal	Function	
 5-pin male multipoint connector	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	

4.5.6.7 Terminating resistor



A terminating resistor is already integrated on the bus controller. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.5.6.8 Node number and transfer rate

Node numbers and transfer rates are configured using the two bus controller number switches. The switch positions 0x00 to 0x40 and 0x60 enable automatic transfer rate detection (see section 4.5.6.9 "Automatic transfer rate detection" on page 744). The rest of the switch positions have a fixed transfer rate (see table).

Switch position	Node number	Transfer rate
0x00[1)]	From EEPROM	From EEPROM
0x01 - 0x3F	1 - 63	Automatic
0x40[1)]	From EEPROM	From EEPROM
0x41 - 0x5F	1 - 31	1000 kbit/s
0x60[1)]	From EEPROM	From EEPROM
0x61 - 0x7F	1 - 31	800 kbit/s
0x80	Reserved	-
0x81 - 0x9F	1 - 31	500 kbit/s
0xA0	Reserved	-
0xA1 - 0xBF	1 - 31	250 kbit/s
0xC0	Reserved	-
0xC1 - 0xDF	1 - 31	125 kbit/s
0xE0	Reserved	-
0xE1 - 0xFE	1 - 31	20 kbit/s
0xFF	Reserved	-

1) When one of these numbers is configured, the bus controller uses the operating parameters from the internal EEPROM. The EEPROM is programmed using the CANIO library.

4.5.6.9 Automatic transfer rate detection

After booting, the bus controller goes into "Listen only" mode. This means the bus controller behaves passively on the bus and only listens.

The bus controller attempts to receive valid objects. If receive errors occur, the controller switches to the next transfer rate in the lookup table.

If no objects are received, all transfer rates are tested cyclically. This procedure is repeated until valid objects are received.

Starting transfer rate

The bus controller begins the search with this transfer rate. The starting transfer rate can be defined in two different ways:

- Read from EEPROM
- Using the last detected transfer rate after a software reset (command code 20)

Lookup table

The controller tests the transfer rate according to this table. Beginning with the starting transfer rate, the controller switches to the next lower transfer rate. At the end of the table, the bus controller restarts the search from the beginning.

Transfer rate
1000 kbit/s
500 kbit/s
250 kbit/s
125 kbit/s
50 kbit/s
20 kbit/s
10 kbit/s

4.5.6.10 SG4

This module comes with preinstalled firmware. The firmware is also part of the Automation Runtime operating system for the PLC. If the two versions are different, the Automation Runtime firmware is loaded to the module.

The latest firmware is made available automatically when updating Automation Runtime.

4.5.6.11 Logical I/O modules

Up to 43 I/O modules can be connected to the bus controller (up to 16 can be analog modules). This value refers not to the physical but the logical I/O module slots.

Information:

Physical I/O modules can take up more than one digital or analog slot.

The following table lists all X67 modules capable of using CAN bus and how many logical digital and analog slots are needed.

Module	Digital module slots	Analog module slots
X20AI1744, X20AI1744-3	0	1
X20AI2222	0	1
X20AI2237	0	1
X20AI2322	0	1
X20AI2437	0	1
X20AI2438	0	**2**
X20AI2622	0	1
X20AI2632, X20AI2632-1	0	1
X20AI2636	0	1
X20AI4222	0	1
X20AI4322	0	1
X20AI4622	0	1
X20AI4632, X20AI4632-1	0	1
X20AI4636	0	1
X20AI8221	0	**2**
X20AI8321	0	**2**
X20AIA744	0	**4**
X20AIB744	0	**4**
X20AO2437	0	1
X20AO2438	0	**2**
X20AO2622	0	1
X20AO2632, X20AO2632-1	0	1
X20AO4622	0	1
X20AO4632, X20AO4632-1	0	1
X20AO4635	0	1
X20AP31x1	0	**3**
X20AT2222	0	1
X20AT2311	0	1
X20AT2402	0	1
X20AT4222	0	1
X20AT6402	0	**2**
X20ATA312	0	1
X20ATA492	0	1
X20ATB312	0	1
X20ATC402	0	**2**
X20BR9300	0	1
X20BT9100	0	1
X20BT9400	0	1
X20CM0985	0	**8**
X20CM1201	0	1
X20CM1941	0	1
X20CM4810	0	**2**
X20CM8281	0	1
X20CM8323	0	1
X20CS1011	0	**2**
X20CS1012	0	**3**
X20CS1013	0	1
X20CS1020	0	1
X20CS1030	0	1
X20CS1070	0	1
X20CS2770	0	**2**
X20DC1073	0	1
X20DC1176	0	1
X20DC1178	0	1
X20DC1196	0	1
X20DC1198	0	1
X20DC11A6	0	1
X20DC1376	0	1
X20DC137A	0	1
X20DC1396	0	1
X20DC1398	0	1
X20DC1976	0	1

Module	Digital module slots	Analog module slots
X20DC2190	0	**4**
X20DC2395	0	1
X20DC2396	0	1
X20DC2398	0	**2**
X20DC4395	0	**2**
X20DI2371	1	0
X20DI2372	1	0
X20DI2377	0	1
X20DI2653	1	0
X20DI4371	1	0
X20DI4372	1	0
X20DI4375	1	0
X20DI4653	1	0
X20DI4760	1	0
X20DI6371	1	0
X20DI6372	1	0
X20DI6373	1	0
X20DI6553	1	0
X20DI8371	1	0
X20DI9371	**2**	0
X20DI9372	**2**	0
X20DID371	1	0
X20DIF371	**2**	0
X20DM9324	1	0
X20DO2321	1	0
X20DO2322	1	0
X20DO2623	0	1
X20DO2633	0	1
X20DO2649	1	0
X20DO4321	1	0
X20DO4322	1	0
X20DO4331	1	0
X20DO4332	1	0
X20DO4529	1	0
X20DO4613	0	1
X20DO4623	0	1
X20DO4633	0	1
X20DO4649	1	0
X20DO6321	1	0
X20DO6322	1	0
X20DO6325	1	0
X20DO6529	1	0
X20DO8232	1	0
X20DO8322	1	0
X20DO8331	1	0
X20DO8332	1	0
X20DO9321	**2**	0
X20DO9322	**2**	0
X20DOD322	1	0
X20DOF322	**2**	0
X20DS1119	0	1
X20DS1319	0	1
X20DS1828	0	**2**
X20DS1928	0	**2**
X20DS4387	0	**2**
X20DS4389	0	1
X20DS438A	0	**2**
X20MM2436	0	1
X20MM3332	0	1
X20MM4331	0	**2**
X20MM4456	0	**4**
X20PD0011	1	0
X20PD0012	1	0
X20PD0016	1	0
X20PD2113	1	0
X20PS2100	0	1
X20PS2110	0	1
X20PS3300	0	1
X20PS3310	0	1
X20PS4951	1	0
X20PS9400	0	1
X20PS9402	0	1
X20SM1426	0	1
X20SM1436	0	1

4.5.7 X20(c)BC0083

4.5.7.1 General information

The bus controller makes it possible to connect X2X Link I/O nodes to POWERLINK. It is also possible to operate the X2X Link cycle synchronously 1:1 or synchronous to POWERLINK using a prescaler.

POWERLINK is a standard protocol for Fast Ethernet with hard real-time properties. The Ethernet POWERLINK Standardization Group (EPSG) ensures that the standard remains open and is continually developed: www.ethernet-powerlink.org

- POWERLINK
- I/O configuration and Firmware update via the fieldbus
- Integrated hub for efficient cabling

4.5.7.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.5.7.3 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, 2x RJ45, order bus base, power supply module and terminal block separately.	
X20cBC0083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, 2x RJ45, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 118: X20BC0083, X20cBC0083 - Order data

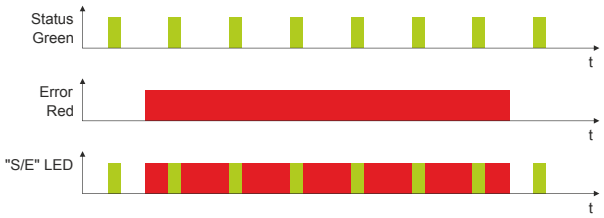
4.5.7.4 Technical data

Product ID	X20BC0083	X20cBC0083
Short description		
Bus controller	POWERLINK (V1/V2) controlled node	
General information		
B&R ID code	0x1F1E	0xE216
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Power consumption		
Bus	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - X2X Link	Yes	
Fieldbus - I/O	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Fieldbus	POWERLINK (V1/V2) controlled node	
Design	2x shielded RJ45 (hub)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Min. cycle time [2]		
Fieldbus	200 µs	
X2X Link	200 µs	
Synchronization between bus systems possible	Yes	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS9400 power supply module separately Order 1x X20cBB80 bus base separately
Spacing [3]	37.5 $^{+0.2}$ mm	

Table 119: X20BC0083, X20cBC0083 - Technical data

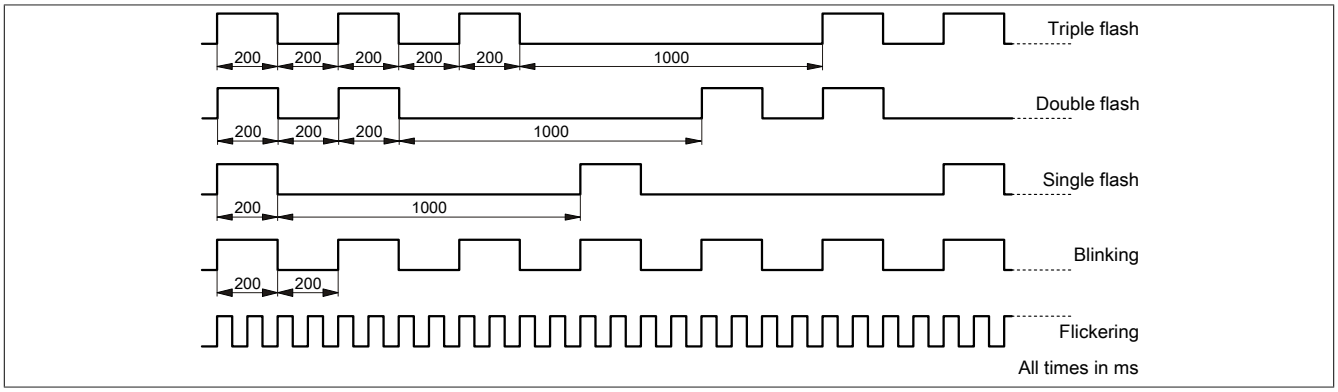
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.7.5 LED status indicators

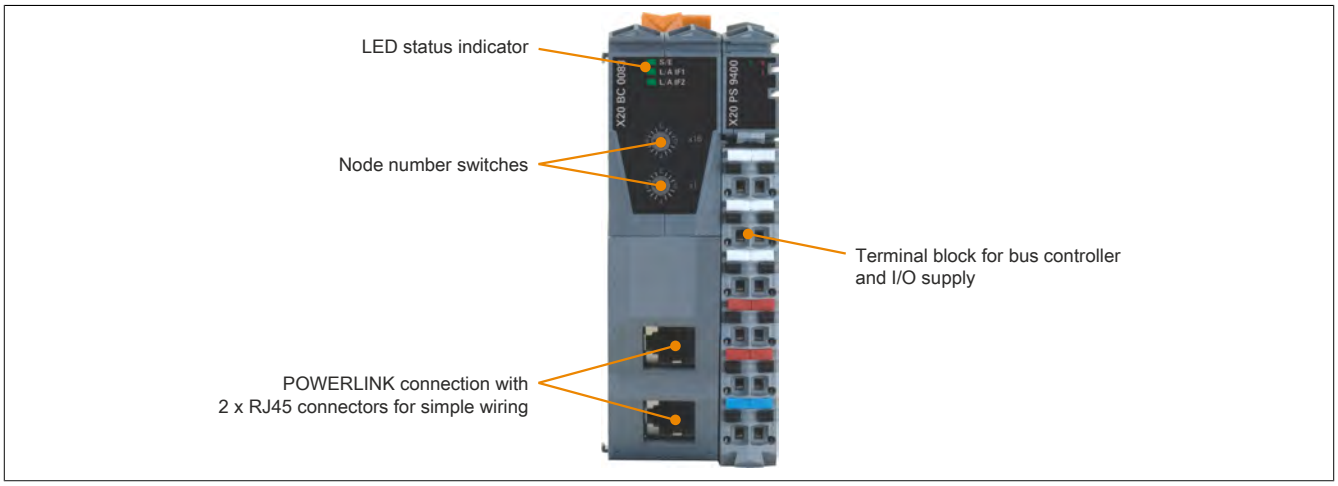
Figure	LED	Color	Status	Description
	S/E[1]	Green	Off	No power supply or mode is NOT_ACTIVE. The controlled node (CN) is either not getting power, or it is in the NOT_ACTIVE state. The CN waits in this state for about 5 seconds after a restart. Communication is not possible with the module. If no POWERLINK communication is detected during these 5 seconds, the CN goes into the BASIC_ETHERNET state (flickering). If POWERLINK communication is detected before this time passes, however, the CN goes directly into the PRE_OPERATIONAL_1 state.
			Flickering	BASIC_ETHERNET mode. The CN has not detected any POWERLINK communication. It is possible to communicate directly with the CN in this state (e.g. with UDP, IP, etc.). If POWERLINK communication is detected while in this state, the CN goes into the PRE_OPERATIONAL_1 state.
			Single flash	PRE_OPERATIONAL_1 mode. When operated on a POWERLINK V1 manager, the CN goes directly into the PRE_OPERATIONAL_2 state. When operated on a POWERLINK V2 manager, the CN waits until an SoC frame is received and then goes into the PRE_OPERATIONAL_2 state.
			Double flash	PRE_OPERATIONAL_2 mode. The CN is normally configured by the manager in this state. Issuing a command (POWERLINK V2) or setting the data valid flag in the output data (POWERLINK V1) then switches to the READY_TO_OPERATE state.
			Triple flash	READY_TO_OPERATE mode. In a POWERLINK V1 network, the CN automatically switches to the OPERATIONAL state as soon as input data is present. In a POWERLINK V2 network, the manager switches to the OPERATIONAL state by issuing a command.
			On	OPERATIONAL mode. PDO mapping is active and cyclic data is being evaluated.
			Blinking	STOPPED mode. No output data is produced or input data supplied. It is only possible to enter or leave this state after the manager has given the appropriate command.
		Red	On	The controlled node (CN) is in an error state (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: • The LED blinks red several times immediately after startup. This is not an error. • The LED is lit red for CNs with configured physical node number 0 but that have not yet been assigned a node number via Dynamic Node Allocation (DNA).
	L/A IFx	Green	On	Link established to the remote station
			Blinking	A link to the remote station has been established and there is activity on bus.

1) The Status/Error LED "S/E" is a green/red dual LED.

Status LEDs - Blinking patterns



4.5.7.6 Operating and connection elements



4.5.7.7 POWERLINK node number

The node number for the POWERLINK node is set using the two number switches. Node numbers between 0x01 and 0xEF are permitted.

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node Operation as a controlled node.
0xF0 - 0xFF	Reserved, switch position not permitted

4.5.7.8 Dynamic Node Allocation (DNA)

The node numbers of all POWERLINK bus controllers can be assigned dynamically. This has the following advantages:

- No need to set the node number switch
- Easier installation
- Reduced error sources

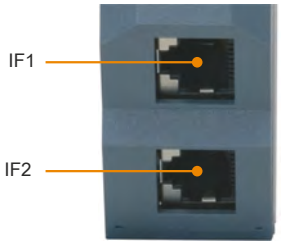
For information about configuration as well as an example, see the AS help system (Communication → POWERLINK → General information → Dynamic Node Allocation (DNA)).

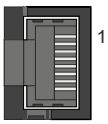
Information:

The IF1 interface must always be used as the input from the preceding node.

4.5.7.9 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.5.7.10 SG3

This module is not supported on SG3 targets.

4.5.7.11 SG4

This module comes with preinstalled firmware. The firmware is also part of the Automation Runtime operating system for the PLC. If the two versions are different, the Automation Runtime firmware is loaded to the module.

The latest firmware is made available automatically when updating Automation Runtime.

4.5.8 X20(c)BC0087

4.5.8.1 General information

Established in 1979, the Modbus protocol has approved the use of Ethernet with both Modbus TCP and Modbus UDP. Today, Modbus TCP is an open Internet draft standard introduced by Schneider Automation to the Internet Engineering Task Force (IETF), the organization responsible for Internet standardization. The Modbus services and object model have been preserved since the original version and left unchanged for use with the TCP/IP transmission medium.

Modbus/UDP differs from Modbus TCP in that it uses connectionless communication via UDP/IP. The advantages of faster and easier communication with UDP/IP also brings with it the disadvantage of requiring error detection and correction in the application layer.

This bus controller makes it possible to connect X2X Link I/O nodes to Modbus via Ethernet. The bus controller can be operated on B&R controllers through the use of Automation Studio or on third-party systems with Modbus TCP or UDP master functionality.

- Fieldbus: Modbus/TCP, Modbus/UDP
- I/O configuration via the fieldbus
- DHCP-capable
- Bootp-capable
- Integrated double switch for efficient cabling
- Configurable I/O cycle (0.5 to 4 ms)
- Response time: <1 - 8 ms (depending on the load on the integrated switch)
- Validity check for command sequences before execution

> **Information:**
>
> **Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.**
>
> **All other function models are supported when configured accordingly. The B&R FieldbusDESIGNER is available at no cost in the Downloads section of the B&R website www.br-automation.com.**

4.5.8.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

> **For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.**

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.5.8.3 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0087	X20 bus controller, 1 Modbus TCP or Modbus UDP interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately.	
X20cBC0087	X20 bus controller, coated, Modbus/TCP or Modbus/UDP interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 120: X20BC0087, X20cBC0087 - Order data

4.5.8.4 Technical data

Product ID	X20BC0087	X20cBC0087
Short description		
Bus controller	Modbus TCP/UDP slave	
General information		
B&R ID code	0x227C	0xD577
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Power consumption		
Bus	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - X2X Link	Yes	
Fieldbus - I/O	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Fieldbus	Modbus TCP/UDP slave	
Design	2x shielded RJ45 (switch)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	10/100 Mbit/s	
Transmission		
Physical layer	10 BASE-T/100 BASE-TX	
Half-duplex	Yes	
Full-duplex	Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Min. cycle time [2]		
Fieldbus	1 ms	
X2X Link	500 µs	
Synchronization between bus systems possible	No	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	

Table 121: X20BC0087, X20cBC0087 - Technical data

Product ID	X20BC0087	X20cBC0087
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS9400 power supply module separately Order 1x X20cBB80 bus base separately
Spacing [3]	37.5 $^{+0.2}$ mm	

Table 121: X20BC0087, X20cBC0087 - Technical data

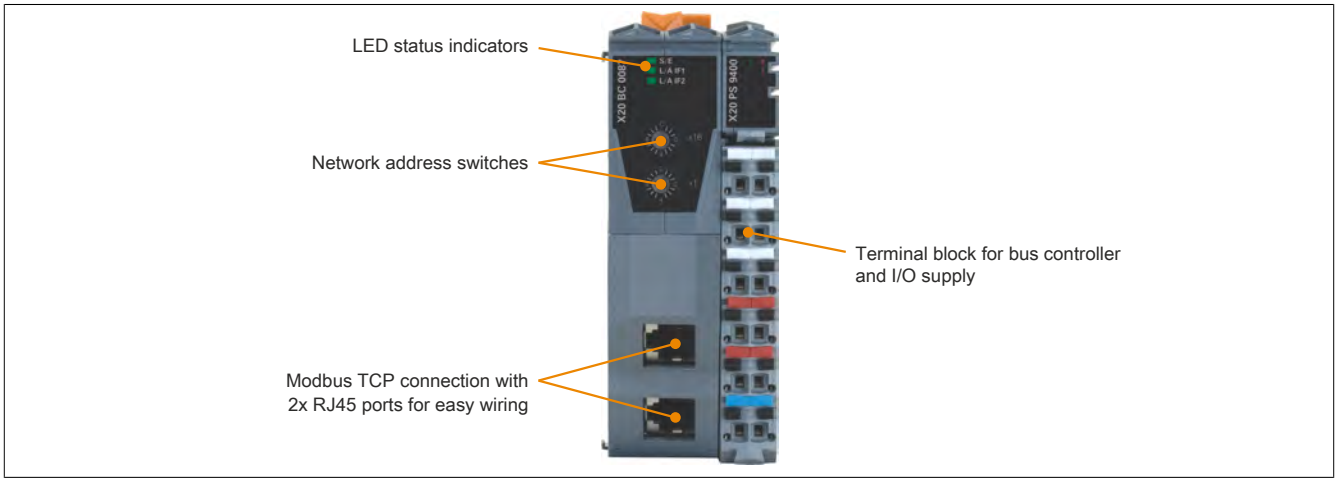
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.8.5 LED status indicators

Figure	LED	Color	Status	Description
	S/E[1]	Green	On	Indicates that there is at least one client connection
			2 pulses	Indicates that there are no client connections
			4 pulses	Indicates that the controller is waiting for an address from the DHCP server
			Blinking	Initialization of connected I/O modules
		Red	2 pulses	Watchdog timeout
			3 pulses	Faulty I/O module configuration data
			4 pulses	Indicates that the controller has detected an IP address being used twice
			5 pulses	Indicates a missing, defective or incorrect I/O module
			6 pulses	Error reading flash memory. Last write operation was incomplete or contained errors.[2]
			On	Indicates a major unrecoverable fault
	L/A IFx	Green	Blinking	Ethernet activity taking place on the RJ45 port (IF1, IF2) indicated by the respective LED
			On	Indicates an established connection (link), but no communication is taking place
			Off	Indicates that no physical Ethernet connection exists

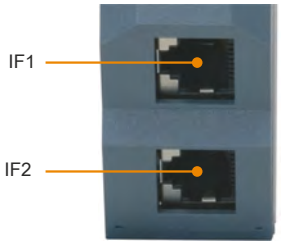
1) The Status/Error LED "S/E" is a green/red dual LED. The LED blinks red several times immediately after startup. This is a boot message, however, and not an error.
2) Possible cause: The bus controller received a command to save, but was switched off before saving was complete. In this case, the bus controller continues to use the old configuration and indicates the failed write operation with a blink code.

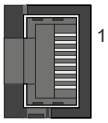
4.5.8.6 Operating and connection elements



4.5.8.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
Shielded RJ45	8	Termination	

4.5.8.8 Modbus/TCP network address switch

Switch position	Description
0x00	This switch position is the factory default setting. In this position, the address switches have no effect on system parameters. The bus controller parameters in flash memory are used (IP address and port number). The bus controller is started with factory default values if valid flash data is not present.
0x01 - 0x7F	The last position of the IP address saved in flash memory is changed to the address switch value. The IP address saved in flash memory is not changed. The port number is read from flash memory.
0x80 - 0xEF	When set within this range, the bus controller runs in DHCP mode. The current hostname is then passed on to the DNS server. A hostname is generated according to how the address switches are set. **Example** The generated hostname is made up of three elements: "br" + "mb" + address switch value (three decimal places). This means, for example, that the following hostname is generated for address switch setting 0xD7 (dec. 215): "brmb215"
0xF0	Auto Store mode: The IP settings are taken from the DHCP or BooTP server. If the IP settings differ from the values stored in the flash memory, then the current IP parameters are saved. This function is only available with Firmware version >= 1.39.
0xF1 - 0xFD	Reserved (same function as position 0xFF)
0xFE	Initializes all bus controller parameters with default values during booting. No values are read from flash memory. The communication parameters correspond to the values assigned with switch setting 0xFF.
0xFF	Initializes all communication parameters with default values. All other bus controller parameters are read from flash memory. Default parameters: • IP address: 192.168.100.1 • Subnet mask: 255.255.255.0 • Gateway: 192.168.100.254 • Primary NetBIOS name: "br" + MAC address • Secondary NetBIOS name: "br" + "mb" + address switch value (decimal) • Port number: 502 • X2X Link configuration: 4 ms cycle time • X2X Link cable length: 0 m

4.5.8.9 Setting the IP address (default value)

Changes to the network address switches are only applied after a restart. If the bus controller is restarted with the address switch value 0xFF, it is initialized with the IP address 192.168.100.1. This address is also the factory default setting. The port number is set to 502 (reserved for Modbus).
This IP address can be used to establish a connection to the bus controller. The internationally unique MAC address is listed on the housing side of the bus controller. The combination of "br" and the MAC address results in a unique name (primary NetBIOS name) that also makes it possible to access the bus controller.

Example of the primary NetBIOS name:

MAC address:	00-60-65-00-49-02
Resulting NetBIOS name:	br006065004902

This means that, without additional parameter changes, either the default IP address 192.168.100.1 or the NetBIOS name "br+MAC" can be used to communicate with the controller.

Since NetBIOS is being used, the bus controller can only be accessed via this name if there are no intermediary routers or gateways in the way.

4.5.8.10 Automatic IP assignment by a DHCP server

If a network address switch setting between 0x80 and 0xEF is configured, the bus controller will attempt to request an IP address from the DHCP server. The assigned IP address can be queried with a "ping" command together with the hostname. The bus controller registers this hostname on the DHCP server, which should forward it to a DNS server.

Example The hostname (DNS name) is made up of three elements:
"br" + "mb" + Address switch value (3 decimal places)
This means, for example, that the following hostname is generated for address switch setting 0xD7 (dec. 215): "brmb215".

If DNS service is not available on the network, the bus controller's two NetBIOS names can also be used for access. The secondary NetBIOS name is identical to the hostname. If the address switches are set to 0x00, it is identical to the primary NetBIOS name. The bus controller can only be reached via its NetBIOS name if no other routers or gateways are in the way.

4.5.8.11 Changing the IP address with the network address switches

The address switches can be used to change the last byte in the IP address configured on the bus controller. The IP address saved in flash memory is not changed. If the address switches are set to 0x00, the bus controller applies the IP address last saved to flash memory. Switch positions between 0x01 and 0x7F cause the last position of the IP address (the lowest byte) to be overwritten by the value of the address switch. This provides the user a quick and easy way to address a large number of bus controllers. In short, an IP address between 192.168.100.1 and 192.168.100.127 can be selected for a bus controller using the address switches without requiring any additional software configuration.

4.5.8.12 Information about NetBIOS names

In addition to the hostname used to register on the register on the DHCP server, the bus controller also has so-called NetBIOS names. These are used to access the bus controller from a PC using its name (as opposed to its IP address). This is only possible if no routers or gateways are in the way, however.

The primary NetBIOS name is always composed of the prefix "br" and the MAC address from the bus controller (see 4.5.8.10 "Automatic IP assignment by a DHCP server").

The secondary NetBIOS name corresponds to the primary NetBIOS name at address switch position 0x00. This is necessary because there may be several bus controllers with the address switch 0x00 in a network segment. In this case, the IP address from flash memory is used.

For all other address switch positions, the secondary NetBIOS name is generated from the network address switch value (as in DHCP mode): "br" + "mb" + Address switch value (3 decimal places).
A hostname defined explicitly by the user will be used for the secondary NetBIOS name regardless of the address switch value.

This makes it possible to access the bus controller with the NetBIOS name configured using the address switches. This is also possible if the controller was not configured for use with a DHCP server (address switch setting between 0x01 and 0x7F).

4.5.8.13 Saving an IP address to flash memory

The IP parameters in flash memory can be changed via the Modbus protocol, the ModbusTCP Toolbox or the Telnet interface. The ModbusTCP Toolbox can be downloaded from the B&R website.
The IP address, subnet and gateway are all defined in the address range 0x1003 to 0x100E. Each has a length of 4 words. The data is applied by writing the constant 0xC1 to the address 0x1140 ("Write Single Register" fc6, addr. 0x1140, data 0xC1). The new settings are applied after the bus controller is restarted.

4.5.9 X20(c)BC0088

4.5.9.1 General information

EtherNet/IP is a fieldbus based on EtherNet/IP that was developed by Allen-Bradley (Rockwell Automation) and later handed off to the Open DeviceNet Vendor Association (ODVA) as an open standard. In 1998, a working group at ControlNet International developed a procedure for setting the published Common Industrial Protocol to Ethernet. EtherNet/IP was published in March 2000 as an open industrial automation standard based on this procedure.

The bus controller makes it possible to connect X2X Link I/O nodes to EtherNet/IP. The bus controller can be operated via the X20IF10D1-1 interface module or by 3rd-party systems with EtherNet/IP scanner functionality.

- Fieldbus: EtherNet/IP
- Integrated 3-port switch for efficient cabling
- Auto-configuration of I/O modules
- Can be configured by the scanner (master) using configuration assembly
- Web interface
- DHCP-capable
- Configurable I/O cycle (0.5 to 4 ms)
- Minimum fieldbus cycle time (also requested packet interval or RPI): 1 ms

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

FieldbusDESIGNER can be used to create configuration files (e.g. EDS files, binary files) in six easy steps. All other function models are also supported by transferring configuration data to the bus controller (e.g. using its web interface or the scanner via a "Configuration Assembly").

FieldbusDESIGNER is available at no cost in the Downloads section of the B&R website www.br-automation.com.

4.5.9.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.5.9.3 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0088	X20 bus controller, 1 EtherNet/IP interface, integrated switch, web interface, 2x RJ45, order bus base, power supply module and terminal block separately	
X20cBC0088	X20 bus controller, coated, 1 EtherNet/IP interface, integrated switch, web interface, 2x RJ45, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 122: X20BC0088, X20cBC0088 - Order data

4.5.9.4 Technical data

Product ID	X20BC0088	X20cBC0088
Short description		
Bus controller	EtherNet/IP adapter (slave)	
General information		
B&R ID code	0x26D8	0xE67F
Status indicators	Module status, network status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Network status	Yes, using status LED and software	
Power consumption		
Bus	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - X2X Link	Yes	
Fieldbus - I/O	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Fieldbus	EtherNet/IP adapter (slave)	
Design	2x shielded RJ45 (switch)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	10/100 Mbit/s	
Transmission		
Physical layer	10 BASE-T/100 BASE-TX	
Half-duplex	Yes	
Full-duplex	Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Min. cycle time [2]		
Fieldbus	1 ms	
X2X Link	500 µs	
Synchronization between bus systems possible	No	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	

Table 123: X20BC0088, X20cBC0088 - Technical data

Product ID	X20BC0088	X20cBC0088
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS9400 or X20cPS9402 power supply module separately Order 1x X20cBB80 bus base separately
Spacing [3]	37.5 +0.2 mm	

Table 123: X20BC0088, X20cBC0088 - Technical data

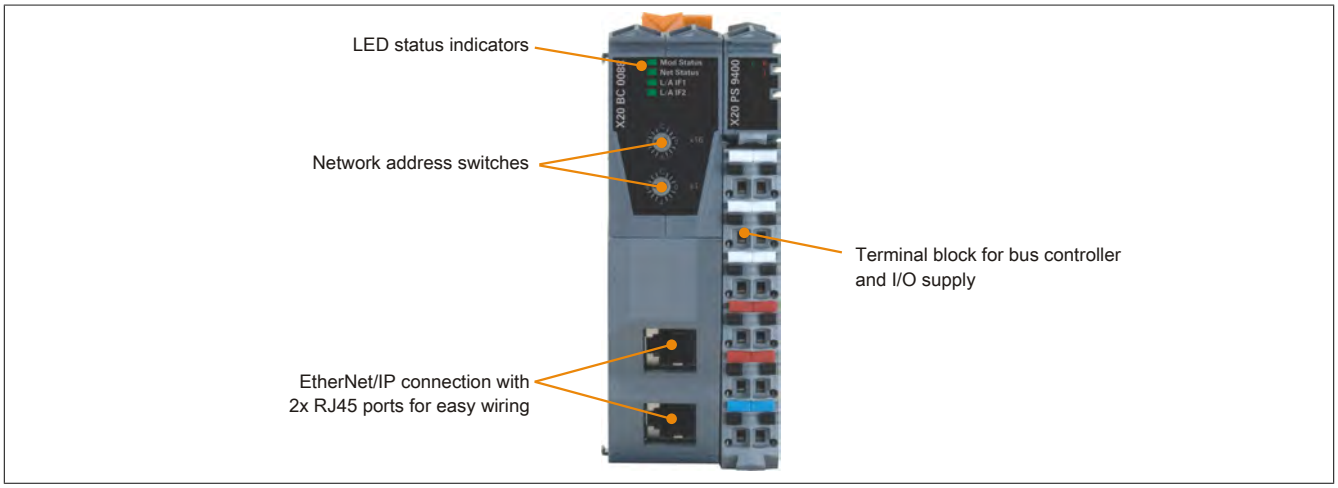
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.9.5 LED status indicators

Figure	LED	Color	Status	Description
	Mod status[1]	Green	On	Indicates that there is at least one client connection
			Blinking	Bus controller not yet configured
			Flickering	HTTP file upload (firmware or configuration file)
		Red	On	Major unrecoverable fault.
			Blinking	Major recoverable fault.
		Green/Red	Blinking	Initialization / Self-test
	Net status[1]	Green	On	Indicates at least one established active scanner (master) connection
			Blinking	Indicates no established active scanner (master) connection
		Red	Off	Indicates no IP address has been assigned
			On	Indicates an IP address has been used more than once
			Blinking	Indicates a timeout on at least one connection
		Green/Red	Blinking	Initialization / Self-test
	L/A IFx	Green	Blinking	Ethernet activity taking place on the RJ45 port (IF1, IF2) indicated by the respective LED
			On	Indicates an established connection (link), but no communication is taking place
			Off	Indicates that no physical Ethernet connection exists

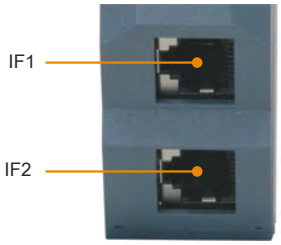
1) The "Mod status" and "Net status" LEDs are green/red dual LEDs.

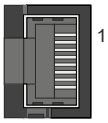
4.5.9.6 Operating and connection elements



4.5.9.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
Shielded RJ45	8	Termination	

4.5.9.8 EtherNet/IP address switching positions

Switch position	Description
0x00	The IP address saved in flash memory is used. The adapter is started via DHCP if attribute 3 (configuration control) of the TCP/IP interface object was set to DHCP.
0x01 to 0x7F	The last position of the IP address saved in flash memory is changed to the address switch value. The IP address saved in the flash memory is not changed. All other adapter parameters are read from the flash memory and are used without being changed.
0x80 to 0xEF	The bus controller runs in this range in DHCP mode. The DNS server is informed of the current host name. A host name is generated according to the setting of the network address switch. Example: The generated host name is made up of three elements: "br" + "eip" + address switch number (three decimal places) This means that a address switch number of e.g. 0xD7 (dec. 215) would result in the following host name: "breip215"
0xF0 to 0xFD	Reserved (same function as position 0xFF).
0xFE	All bus controller parameters are initialized with default values during the boot procedure. No values are read from the flash. The communication parameters are equal to the values as with the switch setting 0xFF.
0xFF	All communication parameters are initialized with default values. All other bus controller parameters are read from the flash. The default parameters: • IP address: 192,168,100.1 • Network mask: 255,255,255.0 • Gateway: 192,168,100,254 • Primary NetBIOS name: "br" + MAC address • Secondary NetBIOS name: "br" + "eip" + address switch number (decimal) • X2X Link configuration: 1 ms cycle time • X2X Link cable length: 0 m

4.5.9.9 Setting the IP address (default value)

Changes to the network address switch are only applied after a restart (power cycle). If the bus controller is restarted with the address switch number 0xFF, it is initialized with the IP address 192.168.100.1. This address is also the default address upon delivery.
This IP can be used to establish a connection to the bus controller. The internationally unique MAC address is listed on the housing side of the bus controller. The combination of "br" and the MAC address results in a unique name (primary NetBIOS name) that also makes it possible to access the bus controller.

Example for the primary NetBIOS names:

MAC address:	00-60-65-00-49-02
Resulting NetBIOS name:	br006065004902

This means that, without additional parameter changes, either the default IP address 192.168.100.1 or the NetBIOS name "br+MAC" can be used to communicate with the controller.

The bus controller can only be accessed via this name if there are no intermediary routers or gateways because the NetBIOS method is used.

4.5.9.10 Automatic IP assignment by DHCP server

At an address switch position between 0x80 and 0xEF, the bus controller attempts to request an IP address from the DHCP server. To query this IP address, simply run a "ping" command with the host name. The bus controller registers this host name on the DHCP server, which should forward it to a DNS server.

Example: The host name (DNS name) is made up of three elements:
"br" + "eip" + address switch value (three decimal places)
This means that a address switch value of e.g. 0xD7 (dec. 215) would result in the following host name: "breip215"

If DNS service is not available on the network, the bus controller's two NetBIOS names can also be used for access. The secondary NetBIOS name is identical to the host name; at address switch value 0x00, it is identical with the primary NetBIOS name. The bus controller can only be reached via its NetBIOS name if no other routers or gateways are in the way.

4.5.9.11 Changing the IP address with the network address switches

The address switches can be used to change the last byte in the IP address configured on the bus controller. The IP address saved in flash memory is not changed. If the address switches are set to 0x00, the bus controller applies the IP address last saved to flash memory. Switch positions between 0x01 and 0x7F cause the last position of the IP address (the lowest byte) to be overwritten by the value of the address switch. This provides the user a quick and easy way to address a large number of bus controllers. In short, an IP address between 192.168.100.1 and 192.168.100.127 can be selected for a bus controller using the address switches without requiring any additional software configuration.

4.5.9.12 Saving an IP address in flash memory

The IP parameters in the flash memory can be changed via the EtherNet/IP protocol or using the Telnet interface (see EtherNet/IP in User's Manual). If the IP address should be set via the TCP/IP object (class 0xF5), then the new address is only saved in the flash if the instance attribute 3 (Configuration Control) of the TCP/IP object is set at 0 (see CIP specification).

4.5.10 X20(c)BC00E3

4.5.10.1 General information

PROFINET (Process Field Network) is an Industrial Ethernet protocol. It uses TCP/IP and is real-time capable.

PROFINET IO was developed for real-time (RT) and synchronous communication (IRT = Isochronous Real Time). The designations RT and IRT merely describe the real-time properties for communication taking place within PROFINET IO. PROFINET IO defines how all data is exchanged between controllers (masters) and devices (slaves) and how parameter settings and diagnostics are handled. The bus system is designed to exchange data between Ethernet-based field devices using the producer/consumer model.

X20 modules or other modules that are based on X2X Link can be connected to the bus controller. Modular system configurations are optimally supported by PROFINET. Using the device description file (GSDML format), it is very easy to handle project configuration in the respective engineering tool from the manufacturer of the master device.

- Fieldbus: PROFINET RT
- I/O configuration via the fieldbus
- Conformance Class B
- Minimum cycle time 1 ms
- Integrated switch for cabling multiple slaves
- 100 Mbit/s full duplex mode
- Up to 1440 bytes of input data and up to 1440 bytes of output data are possible
- Implemented web interface
- PROFINET diagnostics and module diagnostics during runtime from within the master environment
- Module and switch diagnostics during runtime using the Web interface or SNMP

4.5.10.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.5.10.3 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC00E3	X20 bus controller, 1 PROFINET RT interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately.	
X20cBC00E3	X20 bus controller, coated, 1 PROFINET RT interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 124: X20BC00E3, X20cBC00E3 - Order data

4.5.10.4 Technical data

Product ID	X20BC00E3	X20cBC00E3
Short description		
Bus controller	PROFINET RT slave	
General information		
B&R ID code	0xBB7D	0xE4E0
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Power consumption		
Bus	2.5 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - X2X Link	Yes	
Fieldbus - I/O	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 1)	Yes	
GOST-R	Yes	
Interfaces		
Fieldbus	PROFINET RT slave	
Design	2x shielded RJ45 (switch)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Min. cycle time 2)		
Fieldbus	1 ms	
X2X Link	250 µs	
Synchronization between bus systems possible	Yes	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS9400 power supply module separately Order 1x X20cBB80 bus base separately
Spacing 3)	37.5 $^{+0.2}$ mm	

Table 125: X20BC00E3, X20cBC00E3 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

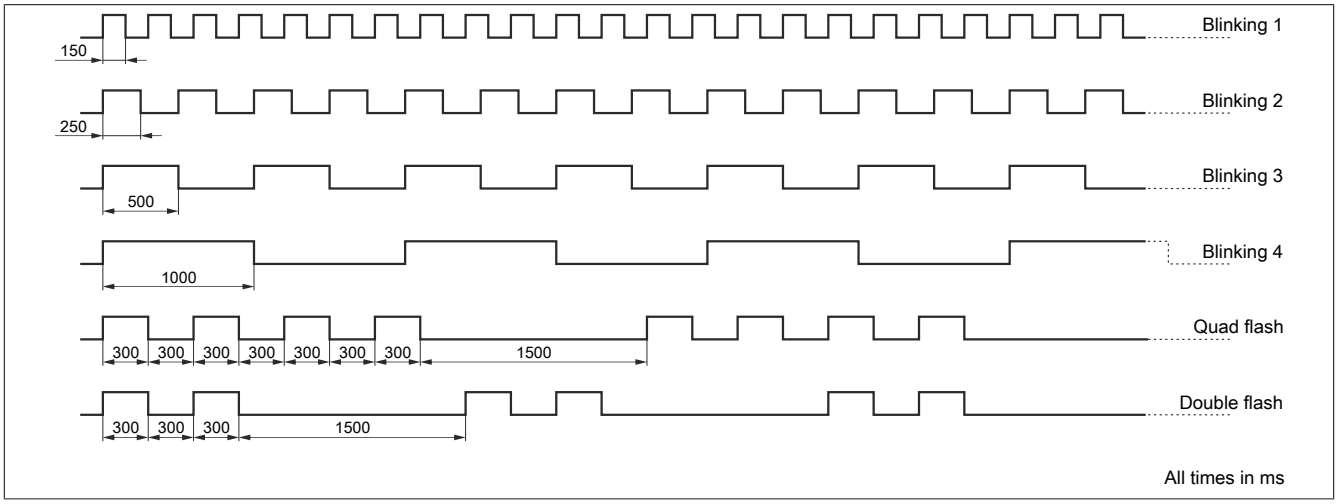
4.5.10.5 LED status indicators

The following table lists the status LEDs available on the bus controller. Exact blink times are specified in the timing diagram in the next section.

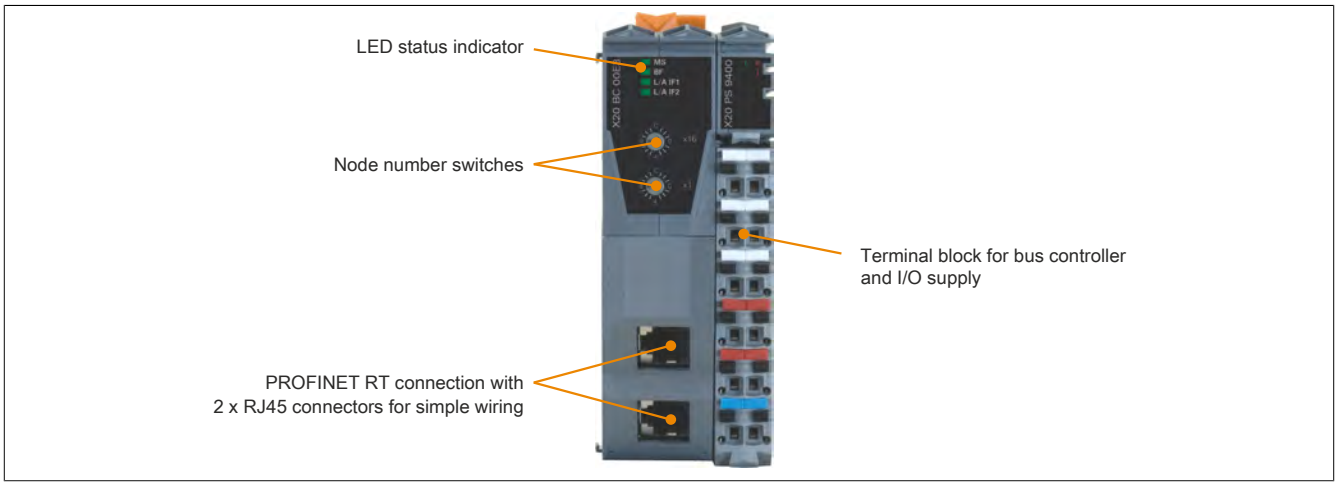
Figure	LED	Color	Status	Description
	MS[1]	Green	Off	The PROFINET master is in "Stop" mode.
			Quad flash	The bus controller does not have a valid IP address (0.0.0.0). It will wait in this state until it is assigned an IP address from the PROFINET master or from an external source. This state can also occur if the bus controller is being operated in DHCP mode.
			Double flash	An unacknowledged alarm is pending on the bus controller.
			Blinking 1	The bus controller is in the initialization phase. This boot phase is where all connected I/O modules are initialized.
			Blinking 3	The bus controller is configuring the connected I/O modules. The configuration is transferred to the bus controller via the PROFINET master.
			On	A connection to a PROFINET master has been established. The master and slave are both in OPERATIONAL mode and data is being exchanged between them. This mode also indicates that the master itself is in RUN mode.
		Red	Blinking 4	The bus controller has detected an error. However, it can still be corrected in the master environment during runtime.
			Blinking 1	The bus controller has detected an error. This error cannot be corrected during runtime; a restart is required.
	BF[1]	Green	Blinking 2	Device identification ("blink" function in step 7 when searching for existing Ethernet stations).
			On	A connection to a PROFINET master has been established.
		Red	On	Not connected to a PROFINET Master
	L/A IFx	Green	Off	No physical Ethernet connection exists.
			Blinking	The respective LED blinks when Ethernet activity is detected on the corresponding RJ45 port (IF1, IF2).
			On	Connection (link) established, but no communication is taking place.

1) The "MS" and "BF" LEDs are green/red dual LEDs.

Status LEDs - Blinking patterns

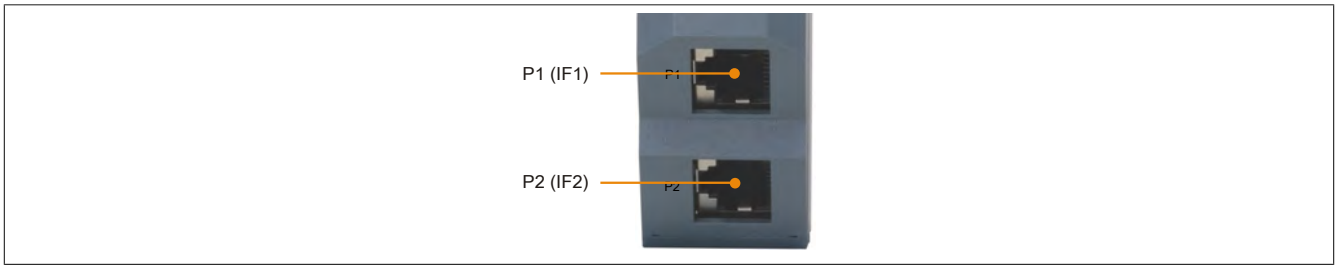


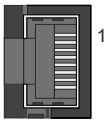
4.5.10.6 Operating and connection elements



4.5.10.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.5.10.8 Node number switches

The bus controller has 2 node number switches. The bus controller can be set to different operating modes using certain, pre-defined switch positions. They can also be used to configure various additional parameters (PROFINET device name, DHCP mode, etc.).

Switch position	Description
0x00	All parameters are loaded from flash memory: Default PROFINET initialization via the DCP protocol (factory state)
0x01 - 0xEF	These switch positions generate a valid PROFINET device name. This name is composed as follows: "brpnXXX". XXX refers to the decimal value of the node number switch position. The system automatically adds any necessary leading zeros.
0xF0	Clears flash (see 4.5.10.9 "Erasing flash memory" on page 768)
0xF1 - 0xFD	Reserved, switch position not permitted
0xFE	IP address via DHCP server
0xFF	All parameters set to default: PME mode

Default PROFINET factory state - Node number switch position 0x00

Parameter	Value
IP address	0.0.0.0
Subnet mask	0.0.0.0
Gateway	0.0.0.0
PROFINET device name	"" ... no factory default name

Default parameters - Node number switch position 0xFF

Parameters cannot be changed by the master in node switch position 0xFF.

Parameter	Value
IP address	192,168,100.1
Subnet mask	255,255,255.0
Gateway	192,168,100,254
PROFINET device name	x20bc00e3

4.5.10.9 Erasing flash memory

Erasing flash memory using switch position 0xF0 returns the bus controller to its factory state.

Procedure

1. Turn off the power supply to the bus controller.
2. Set the node number to 0xF0.
3. Turn the power supply to the bus controller back on.
4. Wait until the "MS" LED flashes green for 5 s. The node number switch must be set to 0x00 and then back to 0xF0 within this time window of 5 seconds (rotate the top switch).
5. Wait until the "MS" LED blinks with a red double-flash (flash has been cleared).
6. Turn off the power supply to the bus controller.
7. Set the desired node number (0x00 - 0xEF)
8. Turn the power supply to the bus controller back on.
9. The bus controller boots with the configured node number.

4.5.10.10 Web interface

The integrated Web interface gives the user an overview of the bus controller's network parameters, the configured I/O modules and the switch configuration. The starting page includes information regarding specific bus controller settings such as IP address, host name and the PROFINET device name. In addition, the web page provides information about the current firmware version. Information concerning module diagnostics is incorporated into a tree structure. Expanding and collapsing the individual module nodes provides an overview of the configured I/O modules. In addition, various package counters are read from the integrated switch. This makes diagnosing errors on the network quick and easy.

Network parameters concerning the bus controller itself can be read, but they cannot be modified. The bus controller's IP configuration is handled during booting or by the PROFINET master when a connection is established.

Each page of the Web interface contains help information that describes the functions and parameters displayed on that page. The link to this information can be found in the upper right corner of the page in the form of a question mark.

A connection to the web interface is established by entering the **current IP address** or the unique **host name** in a Web browser. Some functions require authentication.

The host name is composed of a predefined text and a unique MAC address. For example, if the bus controller has the MAC address 00:60:65:11:22:33, this will result in the following host name: **br006065112233.**

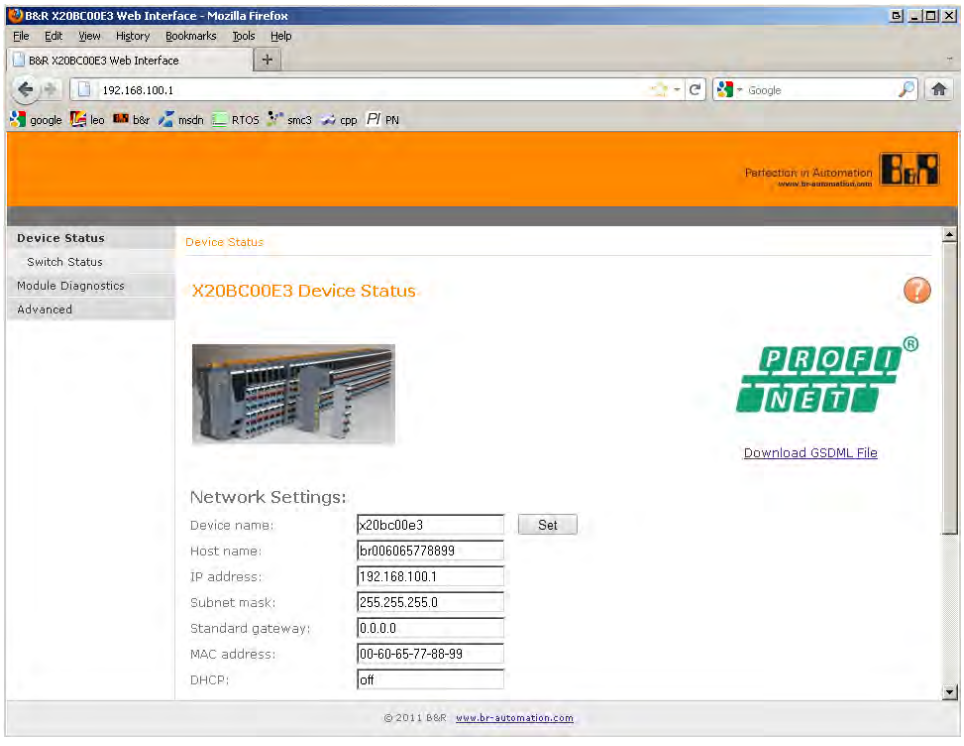
Default parameters for the web interface

IP address:	192.168.100.1
Username:	admin
Password:	B&R

Information:

Take note of the node number switch position.

Please note that authentication parameters are case-sensitive.



4.5.11 X20BC00G3

4.5.11.1 General information

EtherCAT is an Ethernet-based fieldbus developed by Beckhoff. The protocol is suitable for hard and soft real-time requirements in automation technology. In addition to a ring structure, which becomes logically necessary because of the summation frame telegram used, the EtherCAT technology also physically supports topologies such as line, tree, star (limited) and combinations of these topologies. B&R's X20BC80G3 (expandable bus controller module) and X20HB88G0 (stand alone junction base module) are available for implementing these topologies.

EtherCAT slave devices take the data designated for them from a telegram as it is passing through the device. Input data is also inserted in the telegram as it is passing through. The X20BC00G3 bus controller allows X2X Link I/O modules to be coupled to EtherCAT and can be operated on any EtherCAT master system. A transition between IP20 and IP67 protection outside of the control cabinet is possible by aligning X20, X67 or XV modules one after the other as needed at distances up to 100 m.

Master systems without FoE (File Access over EtherCAT) support require an appropriate configuration tool to transfer the configuration (optional).

- Fieldbus: EtherCAT
- Auto-configuration of I/O modules
- I/O configuration and firmware update via the fieldbus (FoE)
- Full support of the modular slice concept via CoE (CANopen over EtherCAT)
- Configurable I/O cycle (0.2 to 4 ms)
- Synchronization between the fieldbus and X2X Link
- X20BC80G3 module type with two additional output ports (X20HB28G0)

Information:

Only the default function model is supported (see respective module description) when the bus controller automatically configures multi-function modules.

All other function models are supported when configured accordingly (see EtherCAT user's manual). The easy-to-use B&R FieldbusDESIGNER can help in this regard and is available for free download from www.br-automation.com/designer.

4.5.11.2 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC00G3	X20 bus controller, 1 EtherCAT interface, 2x RJ45, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 126: X20BC00G3 - Order data

4.5.11.3 Technical data

Product ID	X20BC00G3
Short description	
Bus controller	EtherCAT slave
General information	
B&R ID code	0xAC23
Status indicators	Module status, bus function
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED and software
Power consumption	
Bus	1.68 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Fieldbus - X2X Link	Yes
Fieldbus - I/O	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Fieldbus	EtherCAT slave
Design	2x shielded RJ45
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100BASE-TX
Half-duplex	Yes
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Hub runtime	750 ns
Min. cycle time 2)	
Fieldbus	200 µs
X2X Link	200 µs
Synchronization between bus systems possible	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately
Spacing 3)	37.5 $^{+0.2}$ mm

Table 127: X20BC00G3 - Technical data

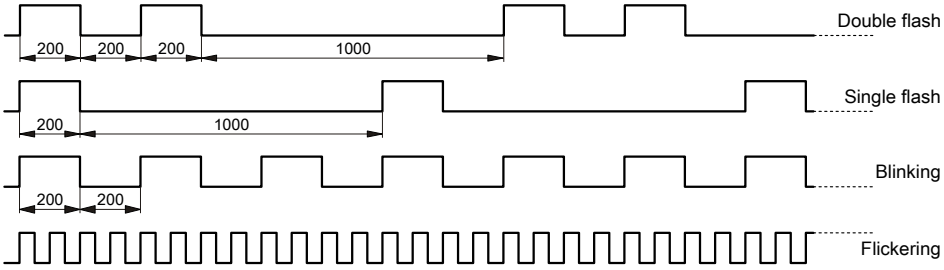
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.11.4 LED status indicators

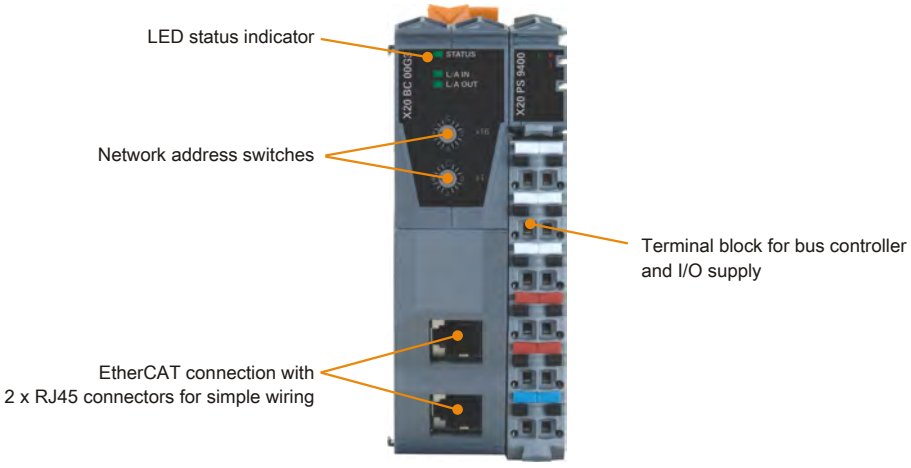
Figure	LED	Color	Status	Description
	STATUS[1]	Green	On	The bus controller is OPERATIONAL.
			Blinking	PREOPERATIONAL status
			Single flash	SAFE-OPERATIONAL status
			Flickering	The bus controller has started and is not yet in INIT status or it is in BOOTSTRAP status (e.g.while downloading firmware).
			Off	INIT status
		Red	On	A critical communication or application error has occurred.
			Blinking	Invalid configuration data
			Single flash	The bus controller has an internal error and changed the EtherCAT status on its own
			Double flash	Watchdog timeout (process data watchdog or EtherCAT watchdog)
			Flickering	Error in the start procedure (INIT status has been achieved, but the error indicator bit in the AL status register is set)
			Off	No error
	L/A IN L/A OUT	Green	Blinking	The respective LED blinks when Ethernet activity is present (PORT OPEN) on the corresponding RJ45 port (IN, OUT).
			On	Connection (link) established, however no communication (PORT OPEN).
			Off	No physical Ethernet connection exists (PORT CLOSED).

1) The "STATUS" LED is a green/red dual LED and is used to indicate EtherCAT states ERROR and RUN.

Status LEDs - Blinking patterns

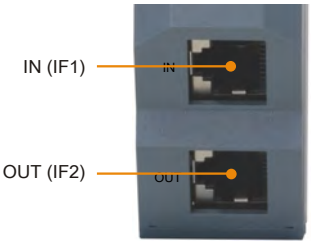


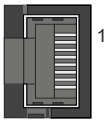
4.5.11.5 Operating and connection elements



4.5.11.6 RJ45 ports

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.5.11.7 EtherCAT network address switch

A slave alias address can be set using the two network address switches on the bus controller. During the initialization phase (during start-up), the bus controller writes the value of the address switch to the ESC register 0x12 or 0x13. However, the value is only accepted in the register if the value of the switch value is between 0x00 and 0xFA (decimal 250).

Switch position	Description
0x00 to 0xFA	Writes the address switch value to the "Station Alias" register.
0xFB to 0xFE	Address switch value not used. ESC Alias registers not changed.
0xFF	Address switch value not used. ESC Alias registers not changed. The bus controller boots with the default values if the address switch is set to the value "0xFF" before a restart. All set parameters remain unchanged in flash memory.

The master determines whether the alias address is used for the slave addressing by setting the corresponding bit in the ESC DL control register (bit 24).

4.5.12 X20BC0143-10

4.5.12.1 General information

CAN (Controller Area Network) systems are widespread in the field of automation technology. CAN topology is based on a line structure and uses twisted wire pairs for data transfer. CANopen is a higher-layer protocol based on CAN. As a standardized protocol, it provides a high degree of flexibility for implementing a wide range of configurations.

The X20BC0043-10 bus controller makes it possible to connect up to 253 X2X Link I/O nodes to CANopen. A transition between IP20 and IP67 protection outside of the control cabinet is possible by aligning X20, X67 or XV modules one after the other as needed at distances up to 100m. All CANopen transmission types such as synchronous, event and polling modes are supported together with PDO linking, life/node guarding, emergency objects, and much more.

- Fieldbus: CANopen
- Auto-configuration of I/O modules
- I/O configuration via the fieldbus (also supported by the B&R FieldbusDESIGNER)
- Constant response times even with large amounts of data (max. 32 Rx and 32 Tx PDOs)
- Configurable I/O cycle (0.5 - 4 ms)
- Possible to configure the transfer rate or have it detected automatically
- Heartbeat consumer and producer
- Emergency producer
- 2x SDO server, NMT slave
- Simple bootup (autostart)
- Terminal access via the serial interface on the X20PS9400

Information:

Only the standard function model (see the respective module description) is supported when the bus controller is used together with multi-function modules it has automatically configured itself.

The B&R FieldbusDESIGNER can be used to create configuration files (e.g. DCF files) in six easy steps. All other function models are also supported by transferring configuration data to the bus controller (e.g. from the master environment with an SDO download or via the serial interface).

The B&R FieldbusDESIGNER is available free of charge in the download section of the B&R website www.br-automation.com.

4.5.12.2 Order data

Model number	Short description	Figure
	Bus controllers	
X20BC0143-10	X20 bus controller, 1 CANopen interface, 9-pin DSUB, FieldbusDESIGNER supported, order 1x 7AC911.9 terminal block separately Order bus base, power supply module and terminal separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	Infrastructure components	
0AC912.9	Bus adapter, CAN, 1 CAN interface	
0AC913.92	Bus adapter, CAN, 2 CAN interfaces, including 30 cm attachment cable (DSUB)	
7AC911.9	Bus connector, CAN	

Table 128: X20BC0143-10 - Order data

4.5.12.3 Technical data

Product ID	X20BC0143-10
Short description	
Bus controller	CANopen slave
General information	
B&R ID code	0xAD3E
Status indicators	Module status, bus function, data transfer
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED and software
Data transfer	Yes, using status LED
Power consumption	
Bus	2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Fieldbus - X2X Link	No
Fieldbus - I/O	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
Fieldbus	CANopen slave
Design	9-pin male DSUB connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Default transfer rate	Automatic transfer rate detection or fixed rate setting
Min. cycle time 2)	
Fieldbus	No limitations
X2X Link	500 µs
Synchronization between bus systems possible	No
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 bus base separately
Spacing 3)	37.5 $^{+0.2}$ mm

Table 129: X20BC0143-10 - Technical data

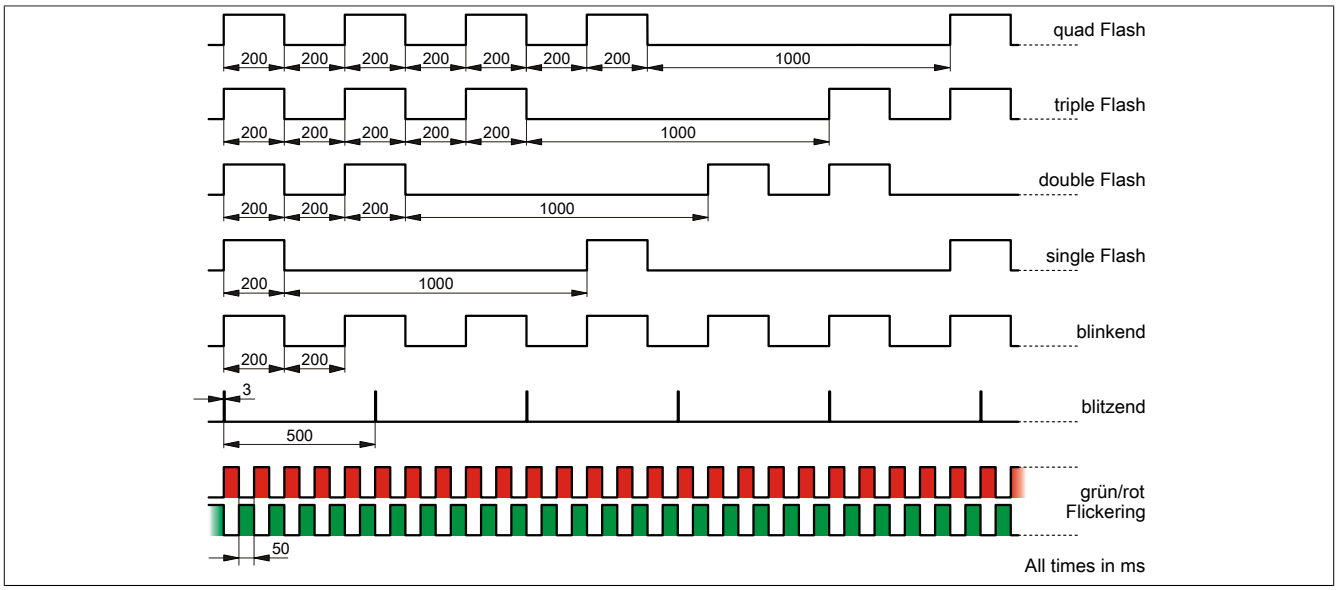
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller.

4.5.12.4 LED status indicators

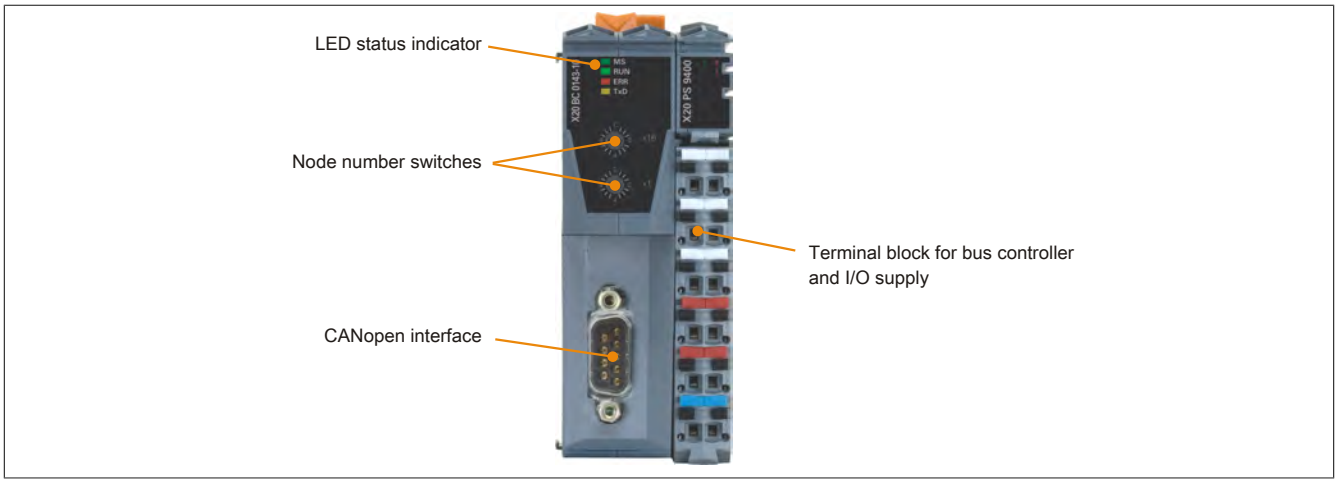
Figure	LED	Color	Status	Description
	MS [1]	Green	Off	No power supply
			Flashing	5 s window for deleting all configuration settings
			On	Boot procedure OK, I/O modules OK
		Red	Double flash	Successfully erased flash memory
			Triple flash	Successfully saved transfer rate
			Quad flash	Successfully saved configuration
			On	I/O modules: Error message or incorrect configuration
	RUN	Green	Off	No power supply
			Single flash	STOP mode
			Triple flash	Firmware download in progress
			Blinking	PREOPERATIONAL mode
			On	OPERATIONAL mode
	ERR	Red	Off	No power supply or everything is OK
			Single flash	CAN warning limit reached
			Double flash	Node guarding / heartbeat error
			Blinking	Invalid node number or configuration
			On	Bus errors: Bus off
	RUN/ERR	Green/red	Flickering	Transfer rate detection in progress
	TxD	Yellow	Off	The bus controller is not transmitting any data via the CANopen fieldbus
			On	The bus controller is transmitting data via the CANopen fieldbus

1) The "MS" LED is a green/red dual LED. The LED blinks red several times immediately after startup. This is a boot message, however, and not an error.

Status LEDs - Blinking patterns

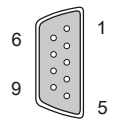


4.5.12.5 Operating and connection elements



4.5.12.6 CAN bus interface

The CAN bus interface is a 9-pin DSUB plug.

Interface	Pin	CAN	
	1	Reserved	
	2	CAN_L	CAN low
	3	CAN_GND	CAN ground
	4	Reserved	
	5	Reserved	
	6	Reserved	
	7	CAN_H	CAN high
	8	Reserved	
	9	Reserved	

4.5.12.7 Node number and transfer rate

Node numbers and transfer rates are configured using the two bus controller number switches.

The transfer rate can be specified in two ways:

- Automatic detection by bus controller (see 4.5.2.9 "Automatic transfer rate detection")
- Fixed definition by user (see 4.5.2.10 "Setting the transfer rate")

Switch position	Node number	Transfer rate
0x00	Not allowed	-
0x01 - 0x7F	1 - 127	Automatically set by the bus controller (default) or fixed setting by the user
0x80 - 0x88	-	Sets a fixed transfer rate
0x89	-	Sets automatic transfer rate detection
0x8A - 0x8F	Not allowed	-
0x90	Clearing the parameters See section 4.5.2.11 "Clearing parameters"	-
0x91	Not allowed	-
0x92	Save configuration[1)] See section 4.5.3.11 "Save automatic configuration"	-
0x93 - 0xFF	Not allowed	-

1) This function is available starting with Hardware version E0 or Firmware version V0001.0107.

4.5.12.8 Automatic transfer rate detection

After booting, the bus controller goes into "Listen only" mode. This means the bus controller behaves passively on the bus and only listens.

The bus controller attempts to receive valid objects. If receive errors occur, the controller switches to the next transfer rate in the lookup table.

If no objects are received, all transfer rates are tested cyclically. This procedure is repeated until valid objects are received.

Lookup table

The controller tests the transfer rate according to this table. Beginning with the starting transfer rate (1000 kbit/s), the controller switches to the next lower transfer rate. At the end of the table, the bus controller restarts the search from the beginning.

Transfer rate
1000 kbit/s
800 kbit/s
500 kbit/s
250 kbit/s
125 kbit/s
100 kbit/s
50 kbit/s
20 kbit/s
10 kbit/s

4.5.12.9 Setting the transfer rate

The bus controller will detect the transfer rate automatically by default. Switch positions 0x80 - 0x88 can be used to set a fixed transfer rate, or 0x89 can be used to enable automatic transfer rate detection.

Switch position	Transfer rate
0x80	1000 kbit/s
0x81	800 kbit/s
0x82	500 kbit/s
0x83	250 kbit/s
0x84	125 kbit/s
0x85	100 kbit/s
0x86	50 kbit/s
0x87	20 kbit/s
0x88	10 kbit/s
0x89	Automatic transfer rate detection

Table 130: Possible transfer rates

Programming the transfer rate

1. Turn off the power supply to the bus controller.
2. Define the transfer rate to be programmed by setting the node numbers (0x80 - 0x89)
3. Turn on the power supply to the bus controller.
4. Wait until the "MS" LED blinks with a red triple-flash (transfer rate is now programmed).
5. Turn off the power supply to the bus controller.
6. Set the desired node number (0x01 - 0x7F).
7. Turn on the power supply to the bus controller.
8. The bus controller now boots with the set node number and the programmed transfer rate.

4.5.12.10 Save automatic configuration

The node number position 0x92 can be used to save automatically generated configurations. This makes it possible to work with a standardized configuration without having to adapt the application to changes associated with service work or different development stages for example.

1. Turn off the power supply to the bus controller.
2. Set the node number to 0x90.
3. Turn on the power supply to the bus controller.
4. Wait until the "MS" LED flashes green.
5. The node number switch must be set to 0x00 and then back to 0x90 within this time window of 5 seconds (rotate the top switch).
6. Wait until the "MS" LED blinks with a red double-flash (parameters have been cleared).
7. Turn off the power supply to the bus controller.
8. Set the node number to 0x92.
9. Turn on the power supply to the bus controller.
10. Wait until the "MS" LED flashes green.
11. The node number switch must be set to 0x02 and then back to 0x092 within this time window of 5 seconds (rotate the top switch).
12. Wait until the "MS" LED blinks with a red quad-flash (parameters have been saved).
13. Turn off the power supply to the bus controller.
14. Set the desired node number (0x01 - 0x7F).
15. Turn on the power supply to the bus controller.
16. The bus controller boots with the set node number and automatic transfer rate detection.

Information:

A mapping tool for decoding the saved PDO mapping is available in the Download section of the B&R website (www.br-automation.com).

Information:

This function is available starting with Hardware version E0 or Firmware version V0001.0107.

4.5.12.11 Clearing parameters

Various parameters can be stored in the bus controller's flash memory:

- Communication parameters
- Vendor-specific parameters
- Application parameters (device profile)
- Programmed transfer rate

Clearing the parameters using switch position 0x90 returns the bus controller to its factory settings.

Clearing the parameters listed above

1. Turn off the power supply to the bus controller.
2. Set the node number to 0x90.
3. Turn on the power supply to the bus controller.
4. Wait until the "MS" LED flashes green. The node number switch must be set to 0x00 and then back to 0x090 within this time window of 5 seconds (rotate the top switch).
5. Wait until the "MS" LED blinks with a red double-flash (parameters have been cleared).
6. Turn off the power supply to the bus controller.
7. Set the desired node number (0x01 - 0x7F).
8. Turn on the power supply to the bus controller.
9. The bus controller boots with the set node number and automatic transfer rate detection.

4.5.12.12 Additional documentation and import files (EDS)

Additional documentation about bus controller functions as well as the necessary import files for the master engineering tool are available in the Downloads section of the B&R website (www.br-automation.com).

4.6 Bus controllers system modules

The X20 system bus controllers are made up of a bus controller fieldbus interface, a bus controller system module and an X20TB12 terminal block.

Bus controller system modules include the base module and the supply modules.

4.6.1 Brief information

Product ID	Short description	on page
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	782
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	784
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	791
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	782
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	784

4.6.2 X20(c)BB80

4.6.2.1 General information

The following modules are used on the bus module:

- Base module (BC, HB, etc.)
- Supply module

The left and right end plates are included in the delivery.

- Bus base

4.6.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.6.2.3 Order data

Model number	Short description	Figure
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	

Table 131: X20BB80, X20cBB80 - Order data

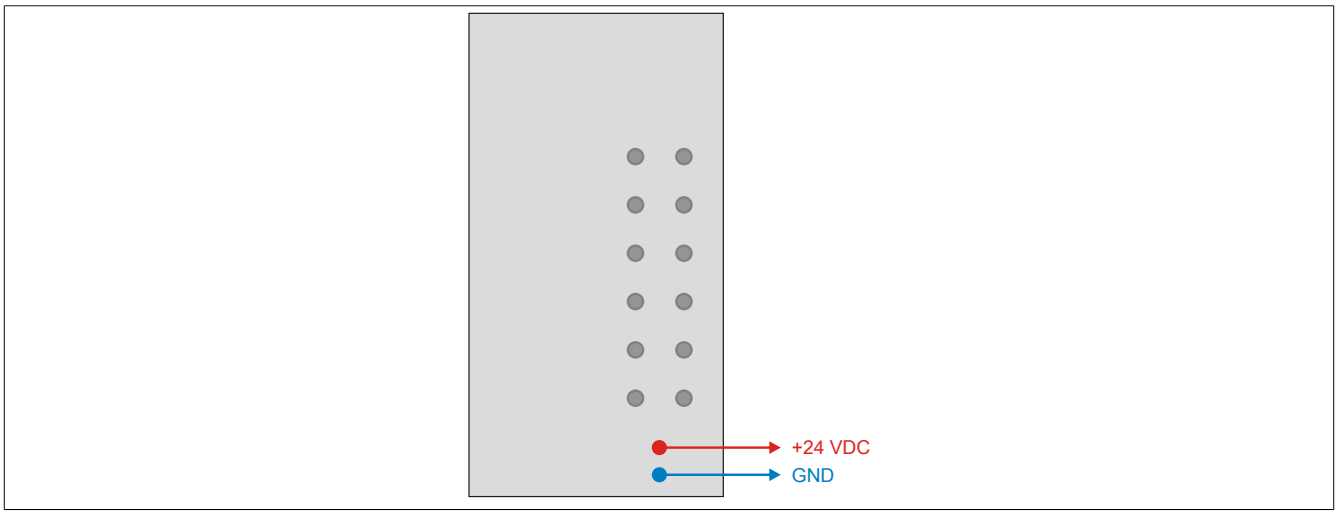
4.6.2.4 Technical data

Product ID	X20BB80	X20cBB80
Short description		
Bus module	Bus base - Backplane for bus controller fieldbus interface and bus controller power supply module	
General information		
Power consumption		
Bus	0.35 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
I/O supply		
Nominal voltage	24 VDC	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Left and right X20 locking plates included in delivery	
Spacing	37.5 $^{+0.2}$ mm	

Table 132: X20BB80, X20cBB80 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.6.2.5 Voltage routing



4.6.3 X20(c)PS9400

4.6.3.1 General information

The supply module is used together with an X20 bus controller. It is equipped with a feed for the bus controller, the X2X Link and the internal I/O supply.

- Supply for the bus controller, X2X Link and internal I/O supply
- Feed and bus controller / X2X Link supply electrically isolated
- Redundancy of bus controller / X2X Link supply possible by operating multiple supply modules simultaneously
- Service interface (RS232)

4.6.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.6.3.3 Order data

Model number	Short description	Figure
	System modules for bus controllers	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 133: X20PS9400, X20cPS9400 - Order data

4.6.3.4 Technical data

Product ID	X20PS9400	X20cPS9400
Short description		
Power supply module	24 VDC power supply module for bus controller, X2X Link supply and I/O	
Interfaces	1x RS232 service interface	
General information		
B&R ID code	0x1F8C	0xD579
Status indicators	Overload, operating status, module status, RS232	
Diagnostics		
Module run/error	Yes, using status LED and software	
RS232 data transfer	Yes, using status LED	
Overload	Yes, using status LED and software	
Power consumption [1]		
Bus	1.42 W	
Internal I/O	0.6 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Bus - RS232	No	
I/O feed - I/O supply	No	
BC/X2X Link feed - BC/X2X Link supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Bus controller / X2X Link supply input		
Input voltage	24 VDC -15 % / +20 %	
Input current	Max. 0.7 A	
Fuse	Integrated, cannot be replaced	
Reverse polarity protection	Yes	
Bus controller / X2X Link supply output		
Nominal output power	7 W	
Parallel operation	Yes [3]	
Redundant operation	Yes	
Overload behavior	Short circuit protection, temporary overload	
Input I/O supply		
Input voltage	24 VDC -15% / +20%	
Fuse	Required line fuse: Max. 10 A, slow-blow	
Reverse polarity protection	No	
Output I/O supply		
Rated output voltage	24 VDC	
Behavior if a short circuit occurs	Required line fuse	
Permitted contact load	10 A	
Interfaces		
Service interface		
Signal	RS232	
Design	Connection made using 12-pin X20TB12 terminal block	
Max. transfer rate	115.2 kbit/s	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section"Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 134: X20PS9400, X20cPS9400 - Technical data

Product ID	X20PS9400	X20cPS9400
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BB8x bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cBB8x bus base separately
Spacing	12.5$^{+0.2}$ mm	

Table 134: X20PS9400, X20cPS9400 - Technical data

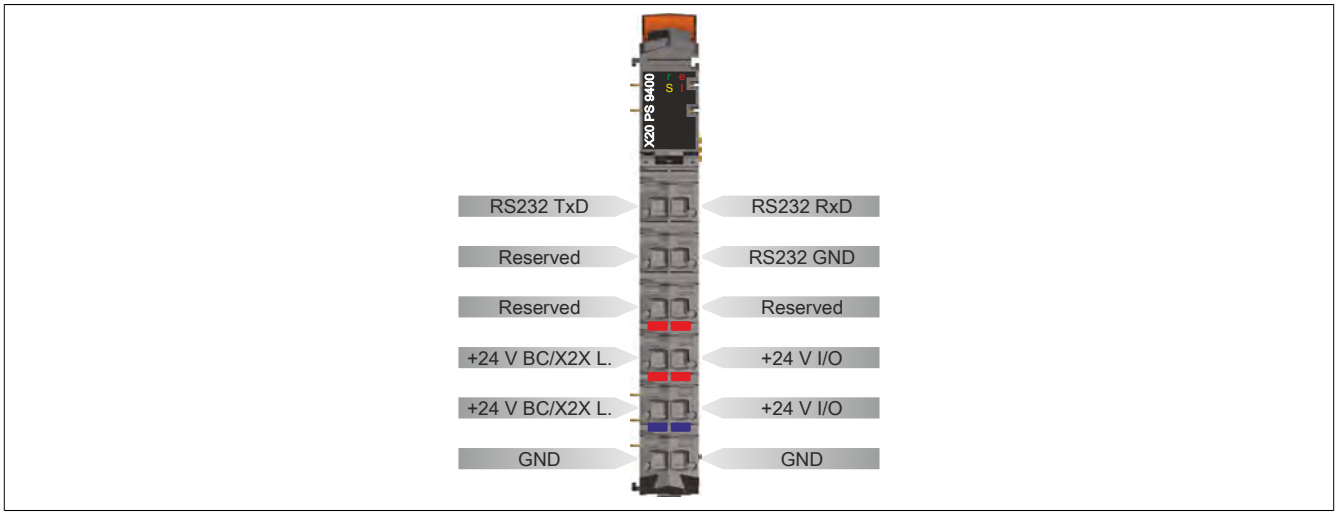
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) In parallel operation, only 75% of the rated power can be assumed. It is important to make sure that all power supplies operated in parallel are switched on and off at the same time.

4.6.3.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

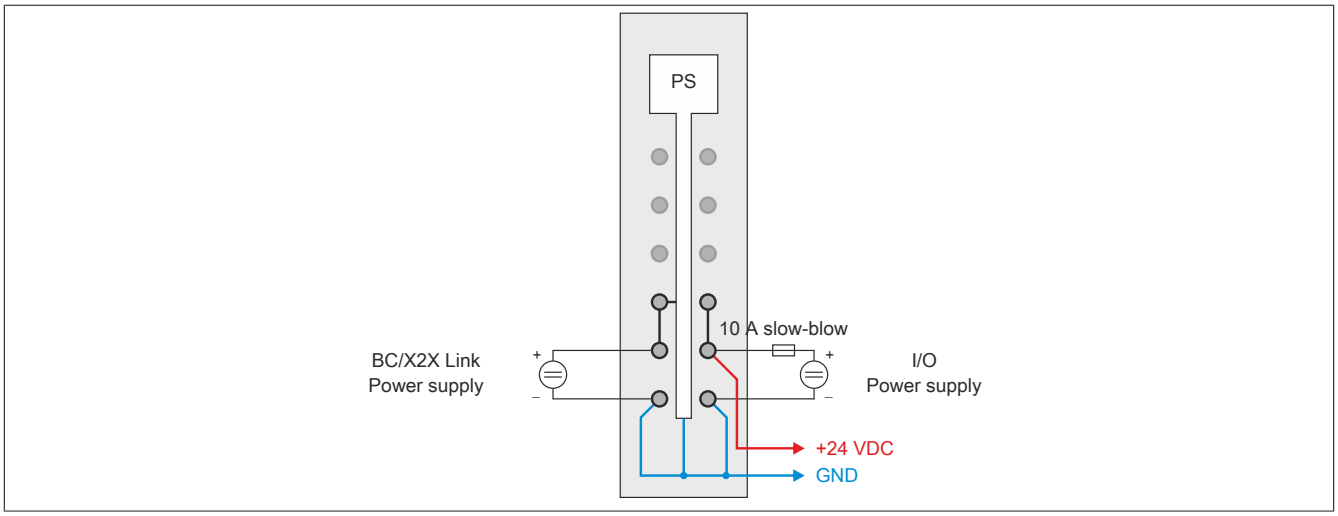
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • The bus controller / X2X Link supply for the power supply is overloaded • I/O supply too low • Input voltage for bus controller / X2X Link supply too low
	e + r	Red on / Green single flash		Invalid firmware
	I	Red	Off	The bus controller / X2X Link supply is within the valid limits
			On	The bus controller / X2X Link supply for the power supply is overloaded
	S	Yellow	Off	No data traffic via service interface
			On	Data is being transmitted via the service interface

4.6.3.6 Pinout

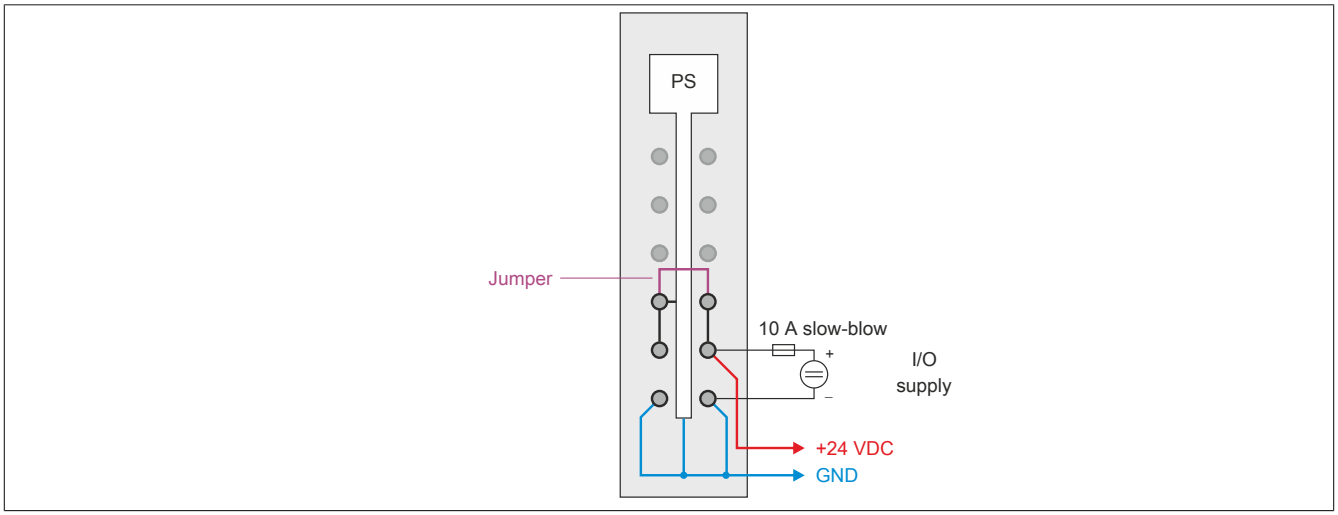


4.6.3.7 Connection examples

With 2 separate supplies

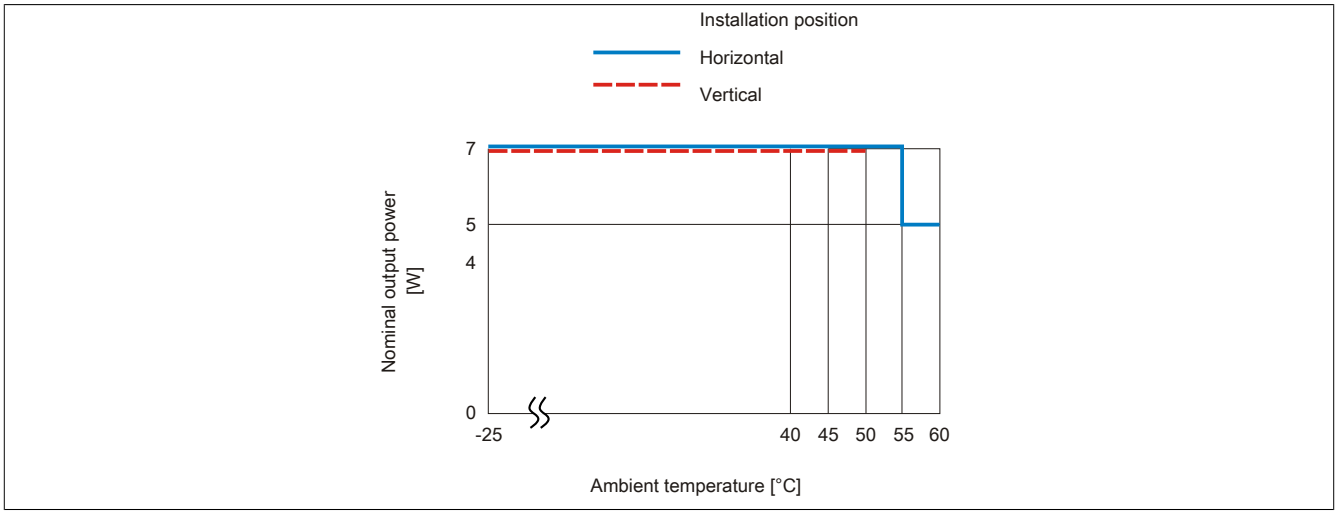


With a supply and jumper



4.6.3.8 Derating

The rated output current for the supply is 7 W. Derating must be taken into consideration based on mounting orientation.



4.6.3.9 Using the service interface

The RS232 service interface is not for use in a machine or system application. It is only intended to be used to update the firmware on various bus controllers and X2X modules as well as to save settings.

4.6.3.10 Register description

4.6.3.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.6.3.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
2	SupplyCurrent	USINT	•			
4	SupplyVoltage	USINT	•			

4.6.3.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 2				
2	2	SupplyCurrent	UINT	•			
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.6.3.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.6.3.10.4 Module status

Name:
Module status

The following voltage and current states of the module are monitored in this register:

Bus supply current:	A bus supply current of >2.3A is displayed as a warning.
Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Warning - overcurrent (>2.3 A) or undervoltage (<4.7 V)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.6.3.10.5 Bus supply current

Name:
SupplyCurrent

This register displays the bus supply current measured at a resolution of 0.1 A.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.6.3.10.6 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.6.3.10.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.6.3.10.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.6.4 X20PS9402

4.6.4.1 General information

The supply module is used together with an X20 bus controller. It is equipped with a feed for the bus controller, the X2X Link and the internal I/O supply.

The module is designed to supply power for smaller X20 systems. Potential groups are able to be formed. An expansion or redundancy of the X2X Link with the X20PS3300 or X20PS3310 supply module is not possible. Expansion of the X20 system with a bus transmitter is not permitted either.

- Supply for the bus controller, X2X Link and internal I/O supply
- Low-cost supply module for small X20 system
- Feed and bus controller / X2X Link supply not electrically isolated
- Expansion or redundancy of bus controller / X2X Link supply not possible by operating multiple supply modules simultaneously

4.6.4.2 Order data

Model number	Short description	Figure
	System modules for bus controllers	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 135: X20PS9402 - Order data

4.6.4.3 Technical data

Product ID	X20PS9402
Short description	
Power supply module	24 VDC supply module for bus controller, X2X Link supply and I/O
General information	
B&R ID code	0xA389
Status indicators	Operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Overload	Yes, using status LED and software
Power consumption [1]	
Bus	1.44 W
Internal I/O	0.6 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
I/O feed - I/O supply	No
BC/X2X Link feed - BC/X2X Link supply	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GOST-R	Yes
Bus controller / X2X Link supply input	
Input voltage	24 VDC -15 % / +20 %
Input current	Max. 0.7 A
Fuse	Integrated, cannot be replaced

Table 136: X20PS9402 - Technical data

Product ID	X20PS9402
Reverse polarity protection	Yes
Bus controller / X2X Link supply output	
Nominal output power	
Horizontal installation	7 W at 45°C and 5 W at 55°C
Vertical installation	7 W at 40°C and 5 W at 50°C
Parallel operation	No
Redundant operation	No
Overload behavior	Short circuit / temporary overload protection
Input I/O supply	
Input voltage	24 VDC -15 % / +20 %
Fuse	Required line fuse: Max. 10 A, slow-blow
Reverse polarity protection	No
Output I/O supply	
Rated output voltage	24 VDC
Behavior if a short circuit occurs	Required line fuse
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BB8x bus base separately
Spacing	$12.5^{+0.2}$ mm

Table 136: X20PS9402 - Technical data

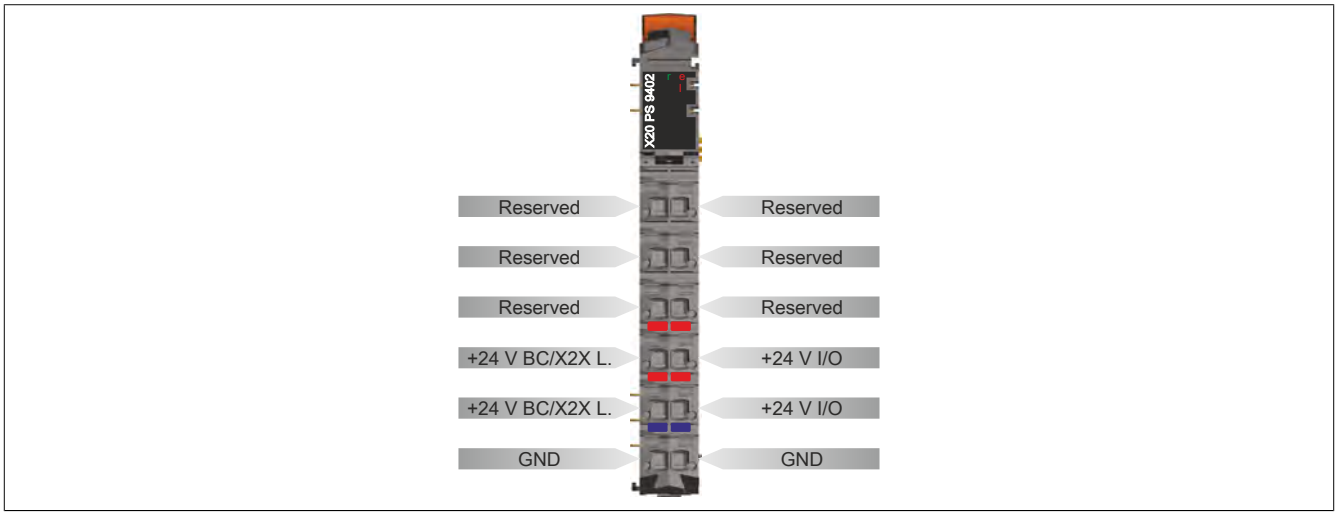
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.6.4.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

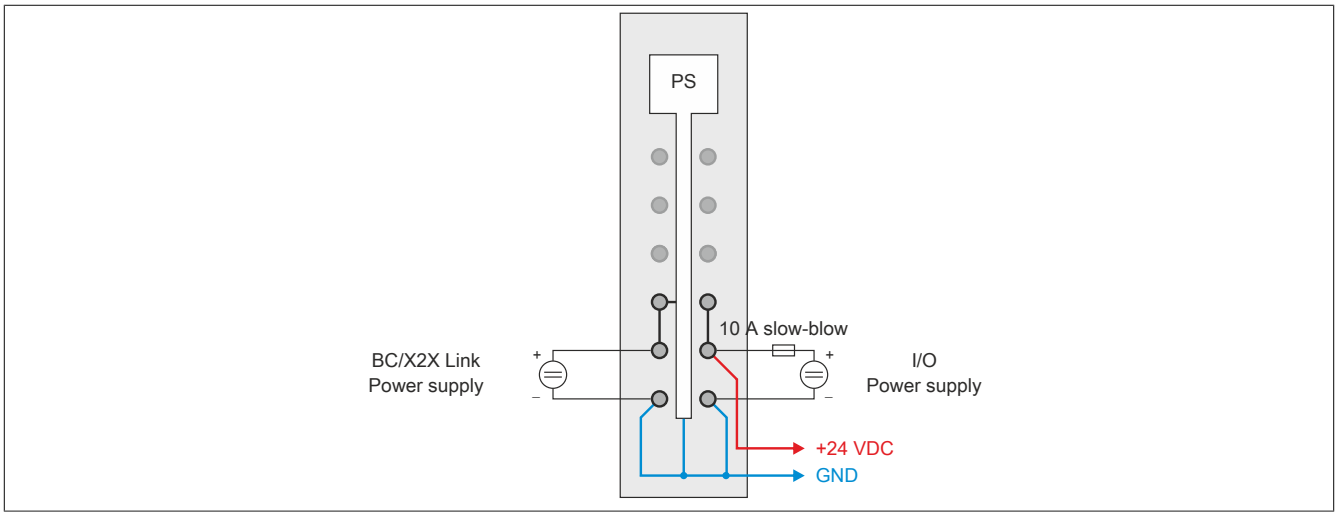
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • The bus controller / X2X Link supply for the power supply is overloaded • I/O supply too low • Input voltage for bus controller / X2X Link supply too low
	e + r	Red on / Green single flash		Invalid firmware

4.6.4.5 Pinout

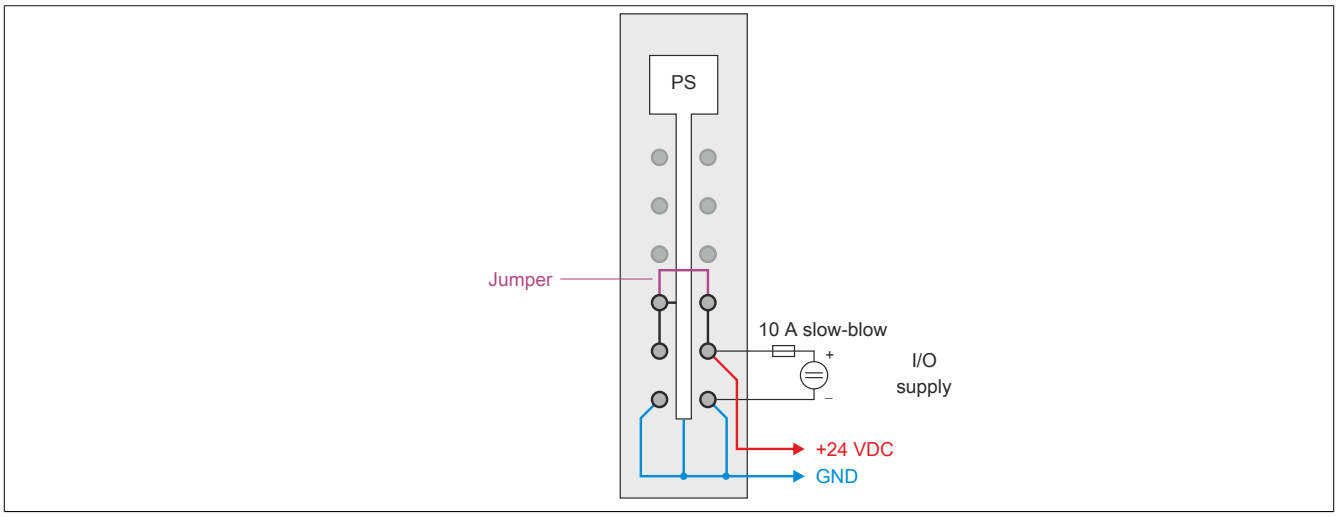


4.6.4.6 Connection examples

With 2 separate supplies

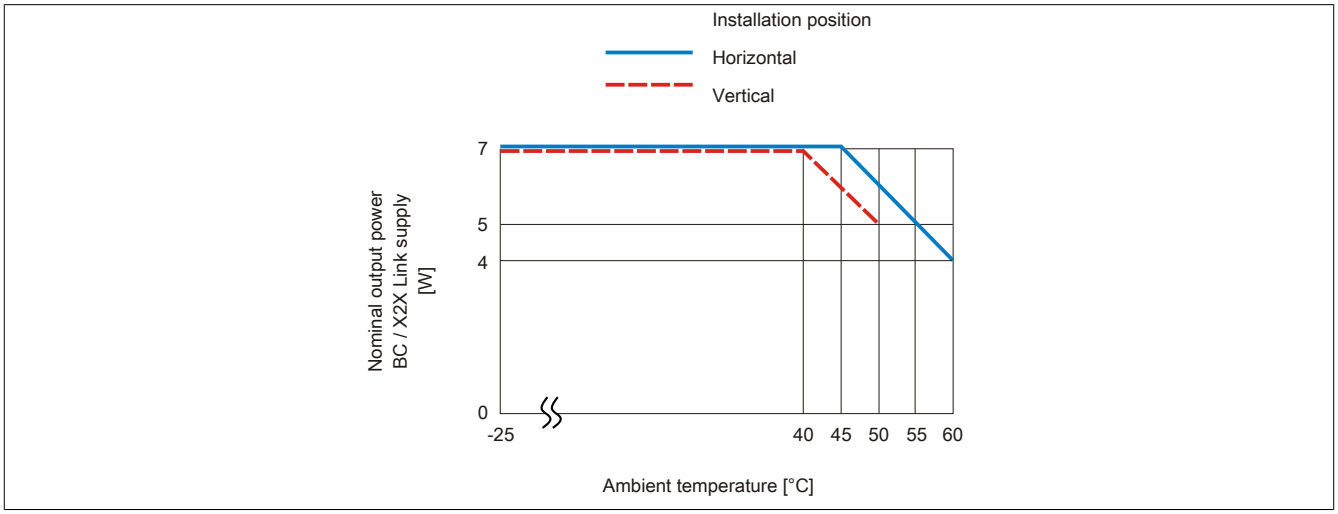


With a supply and jumper



4.6.4.7 Derating for bus controller / X2X Link supply

The rated output current for the bus controller / X2X Link supply is 7.0 W. Derating must be taken into consideration based on mounting orientation.



4.6.4.8 Register description

4.6.4.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.6.4.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
4	SupplyVoltage	USINT	•			

4.6.4.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 2				
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.6.4.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.6.4.8.4 Module status

Name:
Module status

The following module supply voltages are monitored in this register:

Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Bus supply warning - Undervoltage (<4.7V)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.6.4.8.5 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.6.4.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.6.4.8.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.7 Bus modules

In the X20 system, a bus module takes the place of a rack.

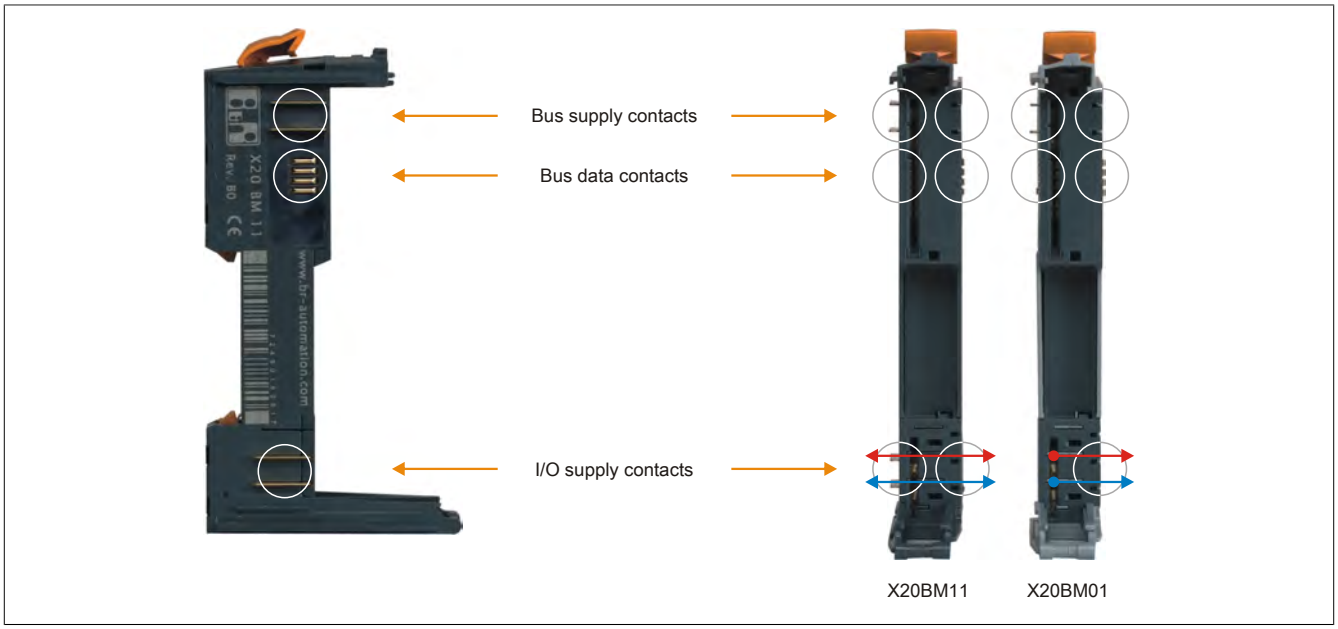


Figure 165: The bus module replaces the rack in the X20 system

The bus module is the backbone of the X20 system regarding the bus supply and bus data as well as the I/O supply for the electronics modules. Each bus module is an active bus station, even without an electronics module. There are two variations of the bus module:

- Interconnected I/O supply
- I/O supply isolated to the left (for power supply modules)

4.7.1 Brief information

Product ID	Short description	on page
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	798
X20BM05	X20 power supply bus module, with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left	800
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	802
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	804
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	806
X20BM21	X20 power supply bus module, for double-width modules, 24 VDC keyed, internal I/O supply interrupted to the left	808
X20BM31	X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous	810
X20BM32	X20 bus module for double-width modules, 240 VAC keyed, internal I/O supply continuous	812
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	798
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	802
X20cBM12	X20 bus module, coated, 240 VAC keyed, internal I/O supply continuous	804
X20cBM31	X20 bus module, coated, for double-width modules, 24 VDC keyed, internal I/O supply continuous	810
X20cBM32	X20 bus module, coated, for double-width modules, 240 VAC keyed, internal I/O supply continuous	812

4.7.2 X20(c)BM01

4.7.2.1 General information

The bus module is the base for all supply modules.

- Basis for all power supply modules
- For creating voltage groups
- The internal I/O supply is isolated to the left

4.7.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.7.2.3 Order data

Model number	Short description	Figure
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	

Table 137: X20BM01, X20cBM01 - Order data

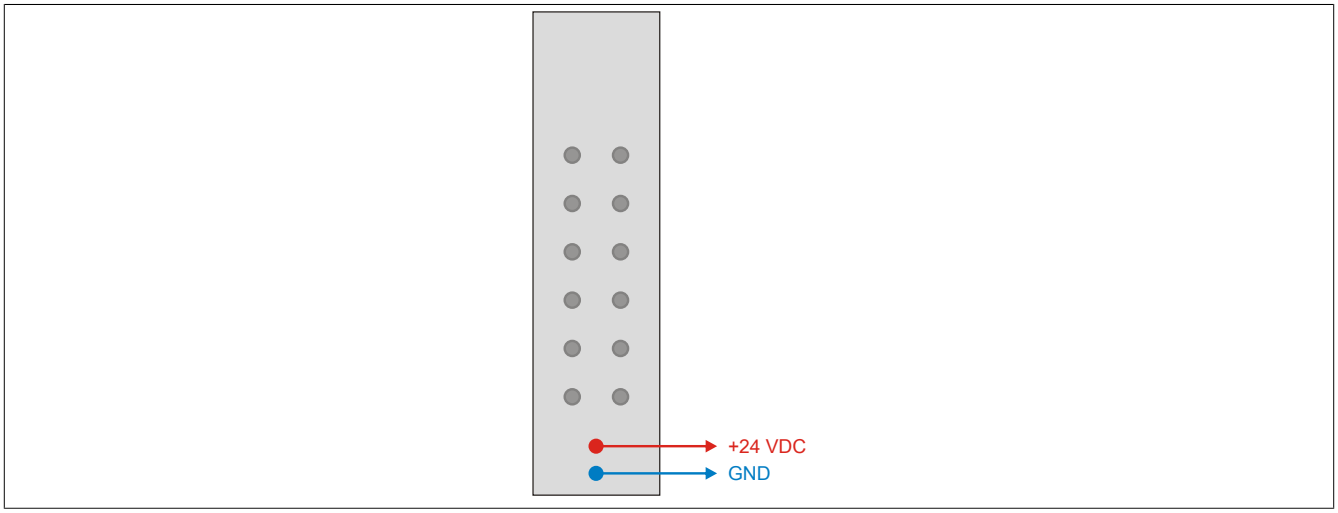
4.7.2.4 Technical data

Product ID	X20BM01	X20cBM01
Short description		
Bus module	Power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
General information		
Power consumption		
Bus	0.13 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
I/O supply		
Nominal voltage	24 VDC	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Spacing	12.5$^{+0.2}$ mm	

Table 138: X20BM01, X20cBM01 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.7.2.5 Voltage routing



4.7.3 X20BM05

4.7.3.1 General information

The bus modules have node number switches that can be used to set permanent addresses. Placing one of these modules at the beginning of an X20 block ensures a unique address. The addresses of subsequent modules are automatically set in ascending order starting at this address. This simple feature greatly increases the flexibility of applications.

Another advantage: Addresses can be set independently of which specific I/O modules are used. All that is required are the respective bus modules. This provides logistical advantages with respect to cost and the variety of parts.

- The bus module is the base for all X20 supply modules
- For creating voltage groups
- The internal I/O supply is isolated to the left
- Manual node number assignment
- Independent of electronics module
- Manual and automatic addressing can be combined as desired

4.7.3.2 Order data

Model number	Short description	Figure
	Bus modules	
X20BM05	X20 power supply bus module, with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left	

Table 139: X20BM05 - Order data

4.7.3.3 Technical data

Product ID	X20BM05
Short description	
Bus module	Power supply bus module with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left
General information	
Power consumption	
Bus	0.13 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes

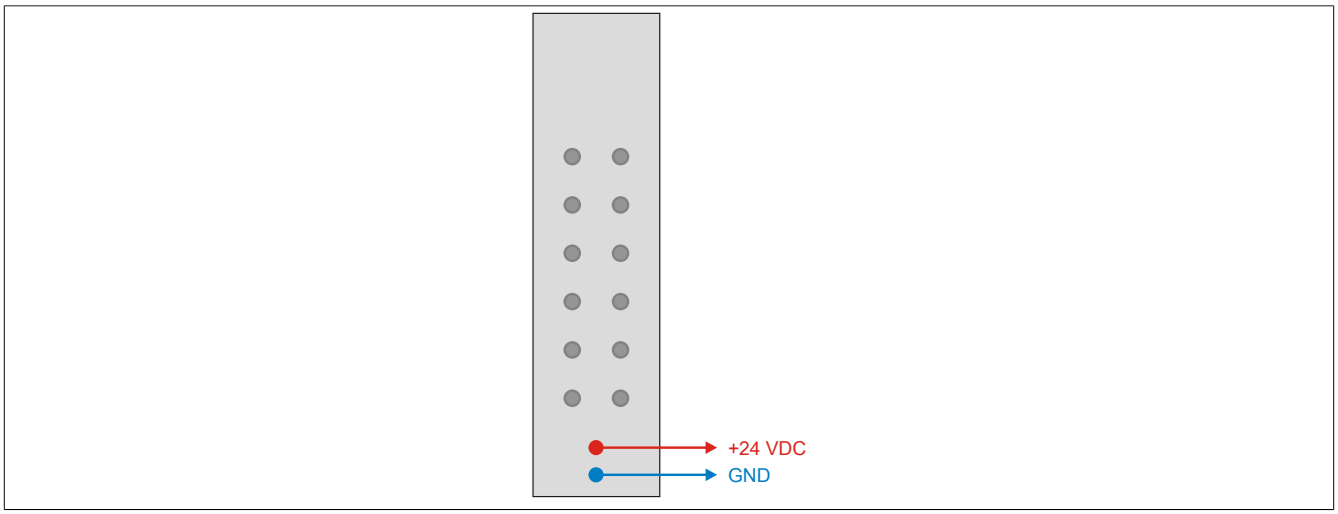
Table 140: X20BM05 - Technical data

Product ID	X20BM05
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Spacing	12.5 $^{+0.2}$ mm

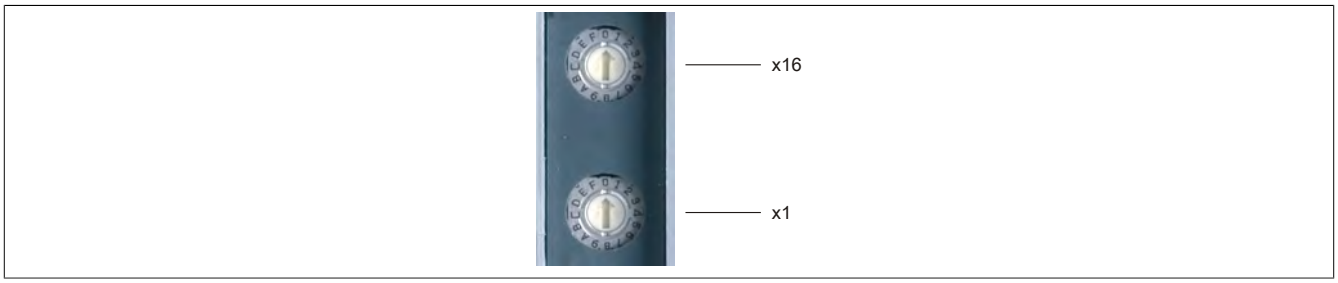
Table 140: X20BM05 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.7.3.4 Voltage routing



4.7.3.5 Node number switches



The X2X Link address of the module is set using the node number switches (0x01 to 0xFD).

Setting node number 0x00 causes the X2X Link address to be assigned automatically.

4.7.4 X20(c)BM11

4.7.4.1 General information

The bus module serves as the base for all 24 VDC X20 I/O modules. The internal I/O supply is interconnected.

- Bus module for 24 VDC I/O modules
- The internal I/O supply is interconnected

4.7.4.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.7.4.3 Order data

Model number	Short description	Figure
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	

Table 141: X20BM11, X20cBM11 - Order data

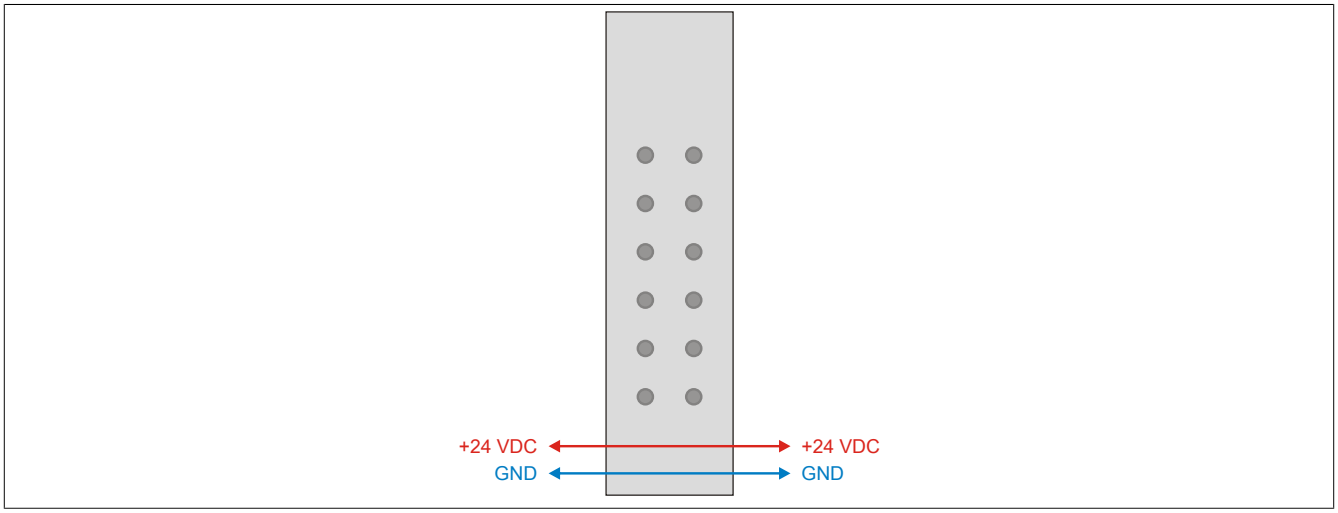
4.7.4.4 Technical data

Product ID	X20BM11	X20cBM11
Short description		
Bus module	Bus module, 24 VDC keyed, internal I/O supply continuous	
General information		
Power consumption		
Bus	0.13 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
I/O supply		
Nominal voltage	24 VDC	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Spacing	12.5$^{+0.2}$ mm	

Table 142: X20BM11, X20cBM11 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.7.4.5 Voltage routing



4.7.5 X20(c)BM12

4.7.5.1 General information

The bus module serves as the base for all 240 VAC X20 I/O modules. The internal I/O supply is interconnected.

- Bus module for 240 VAC I/O modules
- The internal I/O supply is interconnected
- 240 V coding for bus module, electronic module and terminal block

4.7.5.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.7.5.3 Order data

Model number	Short description	Figure
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
X20cBM12	X20 bus module, coated, 240 VAC keyed, internal I/O supply continuous	

Table 143: X20BM12, X20cBM12 - Order data

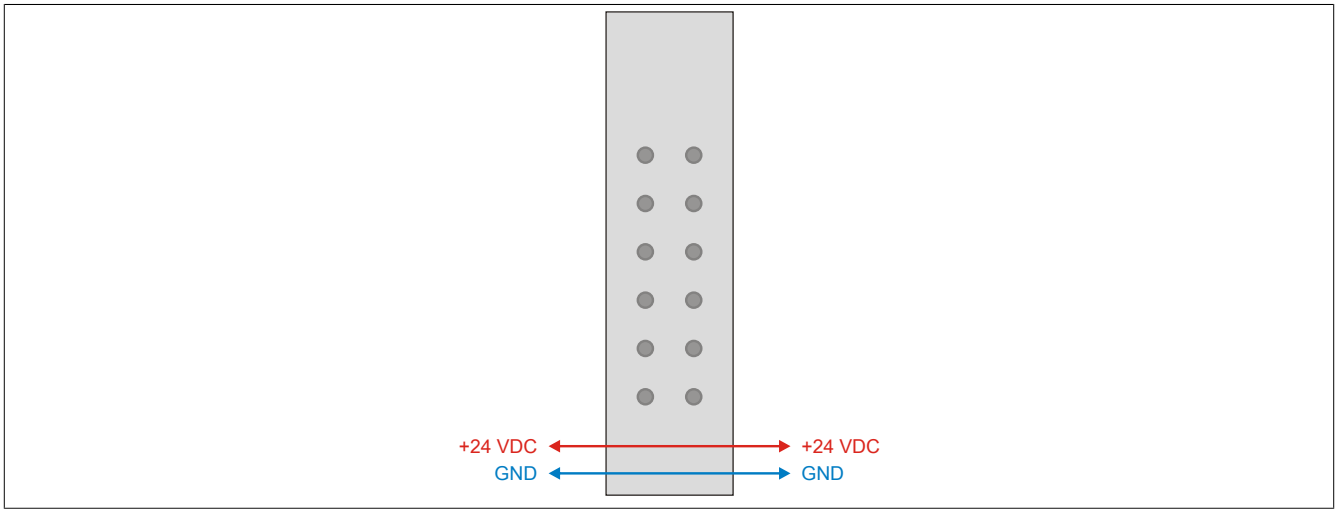
4.7.5.4 Technical data

Product ID	X20BM12	X20cBM12
Short description		
Bus module	Bus module, 240 VAC keyed, internal I/O supply continuous	
General information		
Power consumption		
Bus	0.13 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
I/O supply		
Nominal voltage	24 VDC	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Spacing	12.5$^{+0.2}$ mm	

Table 144: X20BM12, X20cBM12 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.7.5.5 Voltage routing



4.7.6 X20BM15

4.7.6.1 General information

The bus modules have node number switches that can be used to set permanent addresses. Placing one of these modules at the beginning of an X20 block ensures a unique address. The addresses of subsequent modules are automatically set in ascending order starting at this address. This simple feature greatly increases the flexibility of applications.

Another advantage: Addresses can be set independently of which specific I/O modules are used. All that is required are the respective bus modules. This provides logistical advantages with respect to cost and the variety of parts.

- The bus module is the base for all X20 24 VDC I/O modules
- The internal I/O supply is interconnected
- Manual node number assignment
- Independent of electronics module
- Manual and automatic addressing can be combined as desired

4.7.6.2 Order data

Model number	Short description	Figure
	Bus modules	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	

Table 145: X20BM15 - Order data

4.7.6.3 Technical data

Product ID	X20BM15
Short description	
Bus module	Bus module with node number switch, 24 VDC keyed, internal I/O supply continuous
General information	
Power consumption	
Bus	0.13 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20

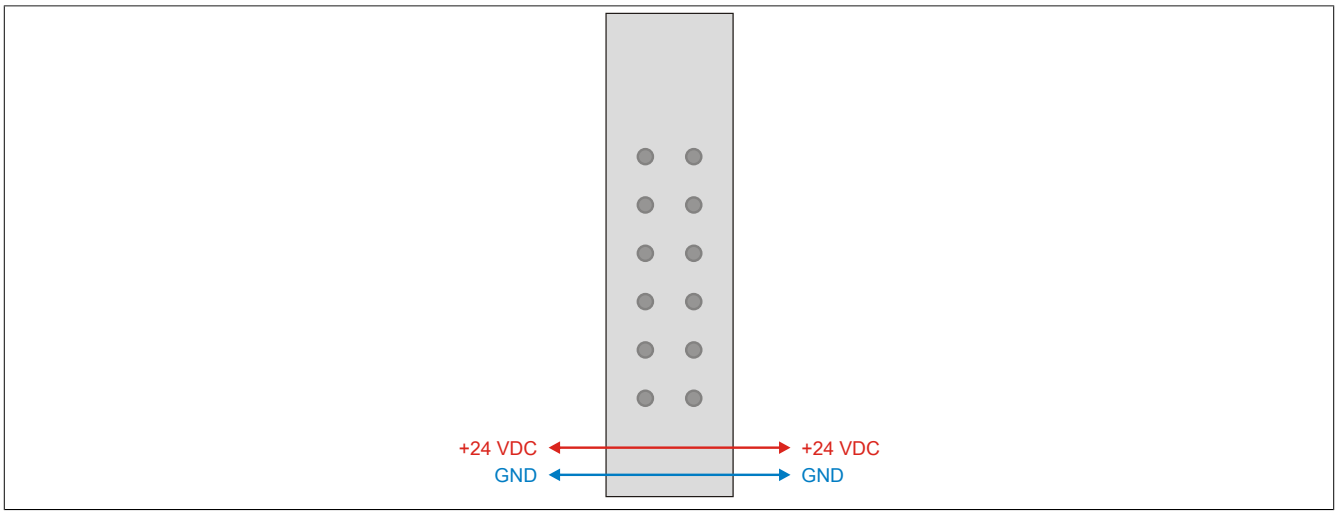
Table 146: X20BM15 - Technical data

Product ID	X20BM15
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Spacing	12.5 $^{+0.2}$ mm

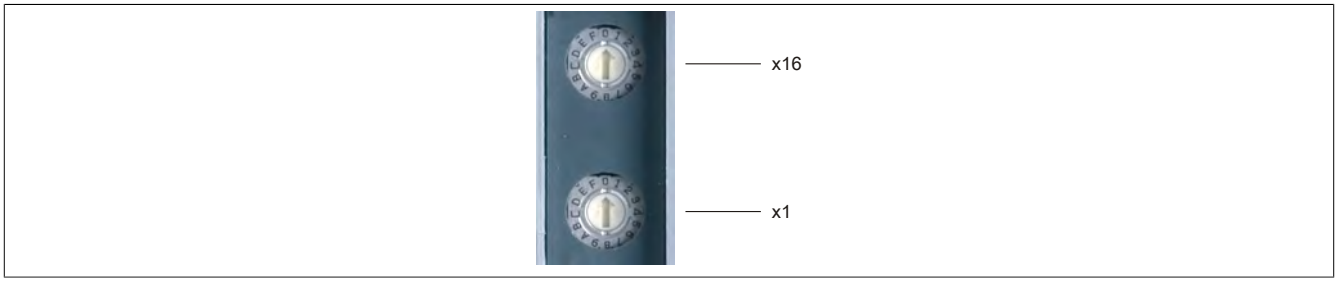
Table 146: X20BM15 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.7.6.4 Voltage routing



4.7.6.5 Node number switches



The X2X Link address of the module is set using the node number switches (0x01 to 0xFD).

Setting node number 0x00 causes the X2X Link address to be assigned automatically.

4.7.7 X20BM21

4.7.7.1 General information

The bus module serves as a basis for all double-width X20 I/O modules. The internal I/O supply is isolated to the left. This allows the bus module to be used to set up a separate voltage group if the X20BT9100 bus transmitter is used for the supply.

- For creating voltage groups
- The internal I/O supply is isolated to the left

4.7.7.2 Order data

Model number	Short description	Figure
	Bus modules	
X20BM21	X20 power supply bus module, for double-width modules, 24 VDC keyed, internal I/O supply interrupted to the left	

Table 147: X20BM21 - Order data

4.7.7.3 Technical data

Product ID	X20BM21
Short description	
Bus module	Power supply bus module for double-width modules, 24 VDC keyed, internal I/O supply interrupted to the left
General information	
Power consumption	
Bus	0.13 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C

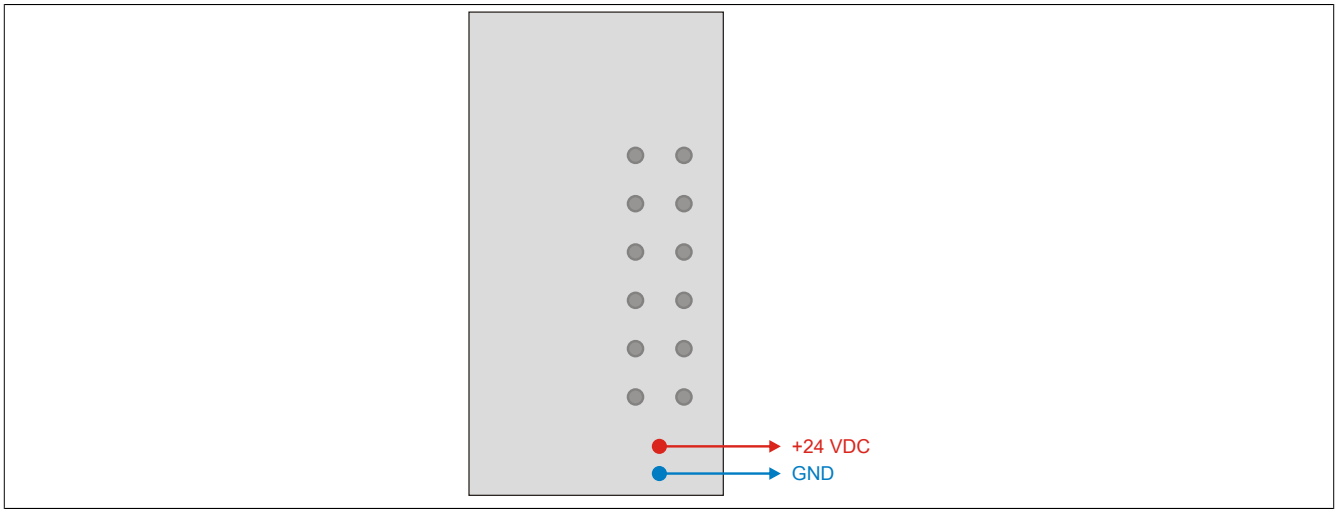
Table 148: X20BM21 - Technical data

Product ID	X20BM21
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Spacing	$25^{+0.2}$ mm

Table 148: X20BM21 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.7.7.4 Voltage routing



4.7.8 X20(c)BM31

4.7.8.1 General information

The bus module serves as a basis for all double-width X20 I/O modules. The internal I/O supply is interconnected.

- Bus module for double-width I/O modules
- The internal I/O supply is interconnected

4.7.8.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.7.8.3 Order data

Model number	Short description	Figure
	Bus modules	
X20BM31	X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous	
X20cBM31	X20 bus module, coated, for double-width modules, 24 VDC keyed, internal I/O supply continuous	

Table 149: X20BM31, X20cBM31 - Order data

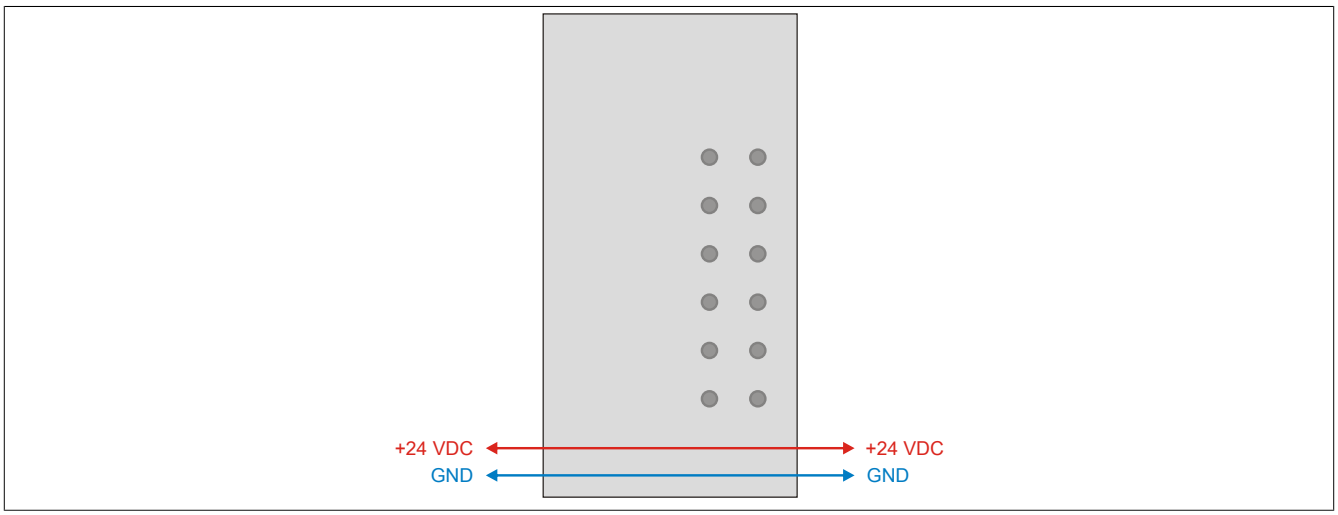
4.7.8.4 Technical data

Product ID	X20BM31	X20cBM31
Short description		
Bus module	Bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous	
General information		
Power consumption		
Bus	0.13 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
I/O supply		
Nominal voltage	24 VDC	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Spacing	$25^{+0.2}$ mm	

Table 150: X20BM31, X20cBM31 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.7.8.5 Voltage routing



4.7.9 X20(c)BM32

4.7.9.1 General information

The bus module serves as the base for all double-width 240 VAC X20 I/O modules. The internal I/O supply is interconnected.

- Bus module for double-width 240 VAC I/O modules
- The internal I/O supply is interconnected
- 240 V coding for bus module, electronic module and terminal block

4.7.9.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.7.9.3 Order data

Model number	Short description	Figure
	Bus modules	
X20BM32	X20 bus module for double-width modules, 240 VAC keyed, internal I/O supply continuous	
X20cBM32	X20 bus module, coated, for double-width modules, 240 VAC keyed, internal I/O supply continuous	

Table 151: X20BM32, X20cBM32 - Order data

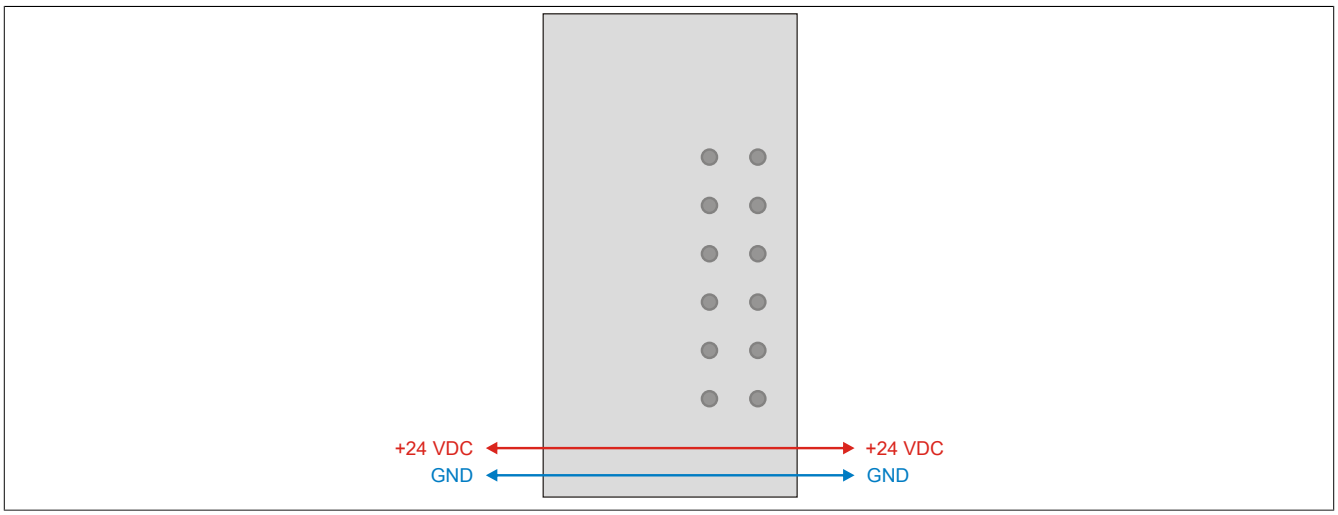
4.7.9.4 Technical data

Product ID	X20BM32	X20cBM32
Short description		
Bus module	Bus module for double-width modules, 240 VAC keyed, internal I/O supply continuous	
General information		
Power consumption		
Bus	0.13 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
I/O supply		
Nominal voltage	24 VDC	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Spacing	25 $^{+0.2}$ mm	

Table 152: X20BM32, X20cBM32 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.7.9.5 Voltage routing



4.8 Bus receivers and Bus transmitters

The bus receiver X20BR9300is used to connect the X20 system directly to the remote X2X Link backplane. The bus transmitter X20BT9100 is used to connect to the next station.

4.8.1 Brief information

Product ID	Short description	on page
X20BR9300	X20 bus receiver, X2X Link, supply for X2X Link and internal I/O supply, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	815
X20BT9100	X20 bus transmitter, X2X Link, supply for internal I/O supply	821
X20BT9400	X20 bus transmitter X2X Link, feed for internal I/O supply, X2X Link supply for X67 modules, reverse polarity protection, short circuit protection, overload protection, parallel connection possible, redundancy operation possible	828
X20cBR9300	X20 bus receiver, coated, X2X Link, supply for X2X Link and internal I/O supply, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	815
X20cBT9100	X20 bus transmitter, coated, X2X Link, supply for internal I/O supply	821

4.8.2 X20(c)BR9300

4.8.2.1 General information

The bus receiver is used to connect the X20 System to the X2X Link. The module is equipped with a feed for the X2X Link as well as the internal I/O supply.

The left and right end plates are included in the delivery.

- X2X Link bus receiver
- Feed for X2X Link and internal I/O supply
- Electrical isolation of feed and X2X Link supply
- Redundancy of X2X Link supply possible by operating multiple supply modules simultaneously
- Operation only on the slot to the far left

4.8.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.8.2.3 Order data

Model number	Short description	Figure
	Bus receivers and transmitters	
X20BR9300	X20 bus receiver, X2X Link, supply for X2X Link and internal I/O supply, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20cBR9300	X20 bus receiver, coated, X2X Link, supply for X2X Link and internal I/O supply, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	X2X Link cable	
X67CA0X99.1000	Cable for custom assembly, 100 m	
X67CA0X99.5000	Cable for custom assembly, 500 m	

Table 153: X20BR9300, X20cBR9300 - Order data

Information:

This module is NOT PERMITTED to be used together with continuous power supply modules (e.g. X20BM11 or X20BM15) since this can result in problems with X2X Link!

4.8.2.4 Technical data

Product ID	X20BR9300	X20cBR9300
Short description		
Bus receiver	X2X Link bus receiver with supply for I/O and bus	
General information		
B&R ID code	0x1BC1	0xDD48
Status indicators	X2X bus function, overload, operating status, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Overload	Yes, using status LED and software	
X2X bus function	Yes, using status LED	
Power consumption [1]		
Bus	1.62 W	
Internal I/O	0.6 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
I/O feed - I/O supply	No	
X2X Link feed - X2X Link supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
X2X Link input supply		
Input voltage	24 VDC -15 % / +20 %	
Input current	Max. 0.7 A	
Fuse	Integrated, cannot be replaced	
Reverse polarity protection	Yes	
X2X Link supply output		
Nominal output power	7 W	
Parallel operation	Yes [3]	
Redundant operation	Yes	
Overload behavior	Short circuit / temporary overload protection	
Input I/O supply		
Input voltage	24 VDC -15 % / +20 %	
Fuse	Required line fuse: Max. 10 A, slow-blow	
Reverse polarity protection	No	
Output I/O supply		
Rated output voltage	24 VDC	
Behavior if a short circuit occurs	Required line fuse	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 154: X20BR9300, X20cBR9300 - Technical data

Product ID	X20BR9300	X20cBR9300
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM01 supply bus module separately Left and right X20 locking plates included in delivery	Order 1x X20TB12 terminal block separately Order 1x X20cBM01 supply bus module separately Left and right X20 locking plates included in delivery
Spacing	12.5$^{+0.2}$ mm	

Table 154: X20BR9300, X20cBR9300 - Technical data

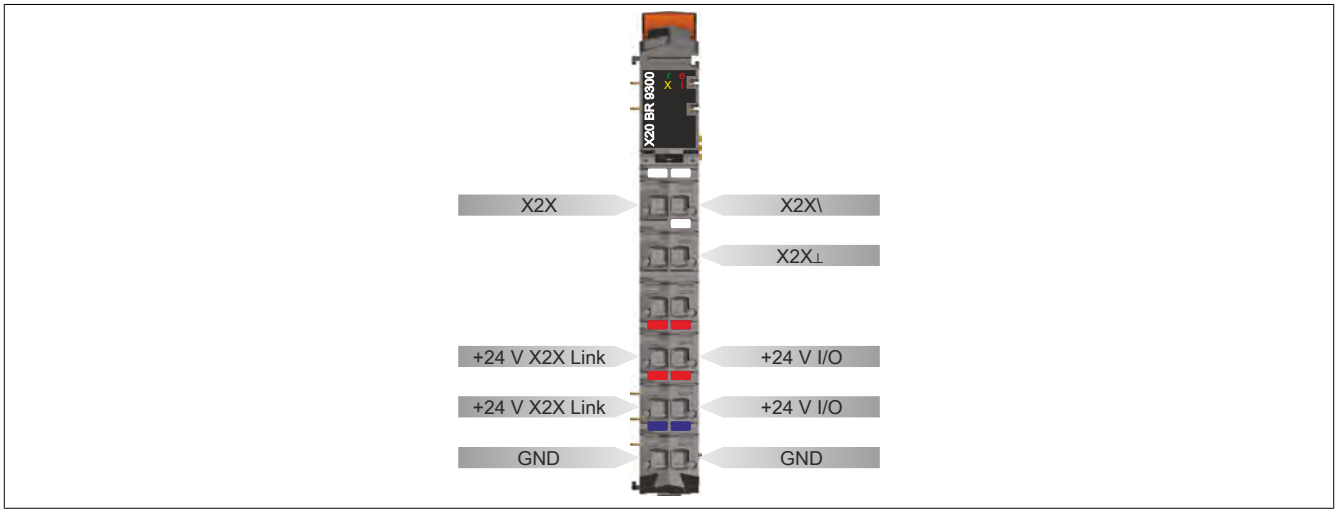
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) In parallel operation, only 75% of the rated power can be assumed. It is important to make sure that all power supplies operated in parallel are switched on and off at the same time.

4.8.2.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

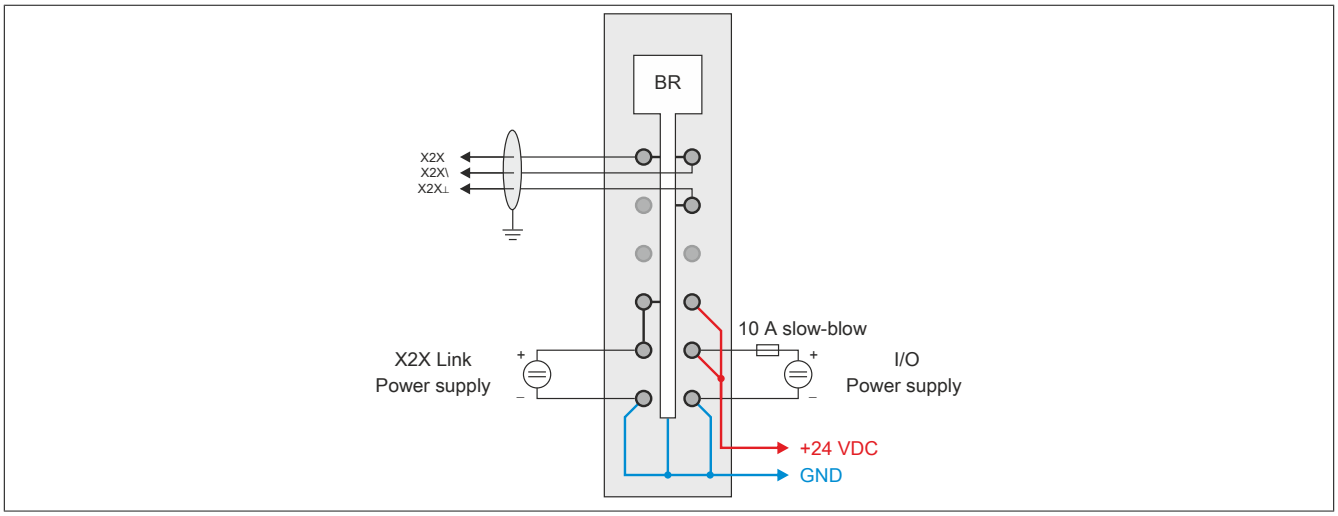
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • X2X Link power supply is overloaded • I/O supply too low • Input voltage for X2X Link supply too low
	e + r	Red on / Green single flash		Invalid firmware
	X	Orange	Off	No communication at the X2X Link
			On	X2X Link communication in progress
	l	Red	Off	X2X Link supply in the acceptable range
			On	X2X Link power supply is overloaded Solution: Use an additional feed module X20PS3300

4.8.2.6 Pinout

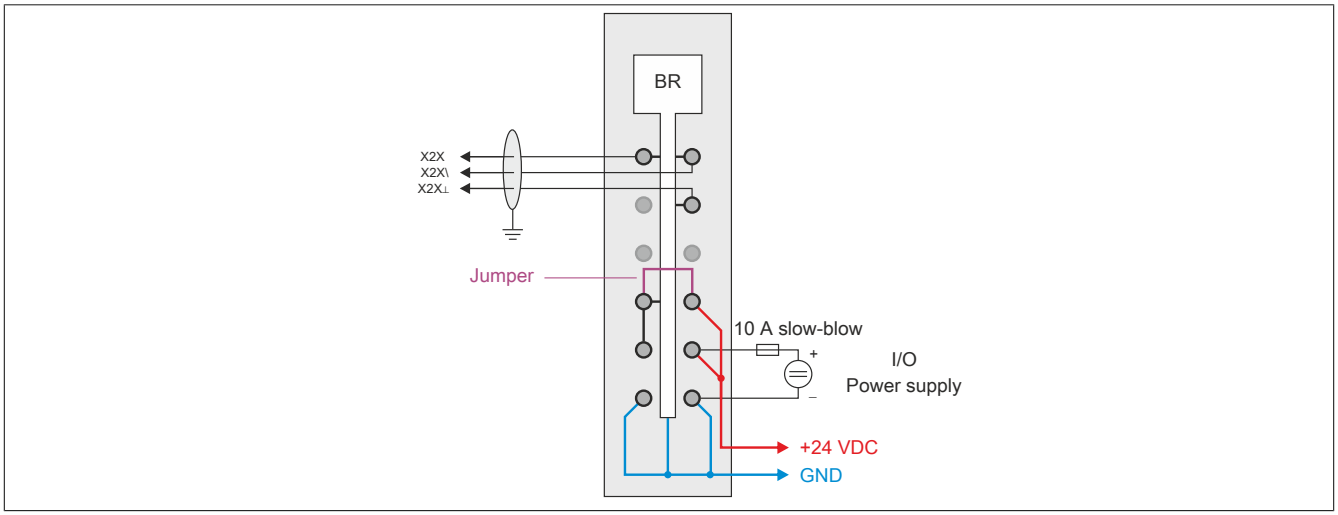


4.8.2.7 Connection examples

With two separate supplies

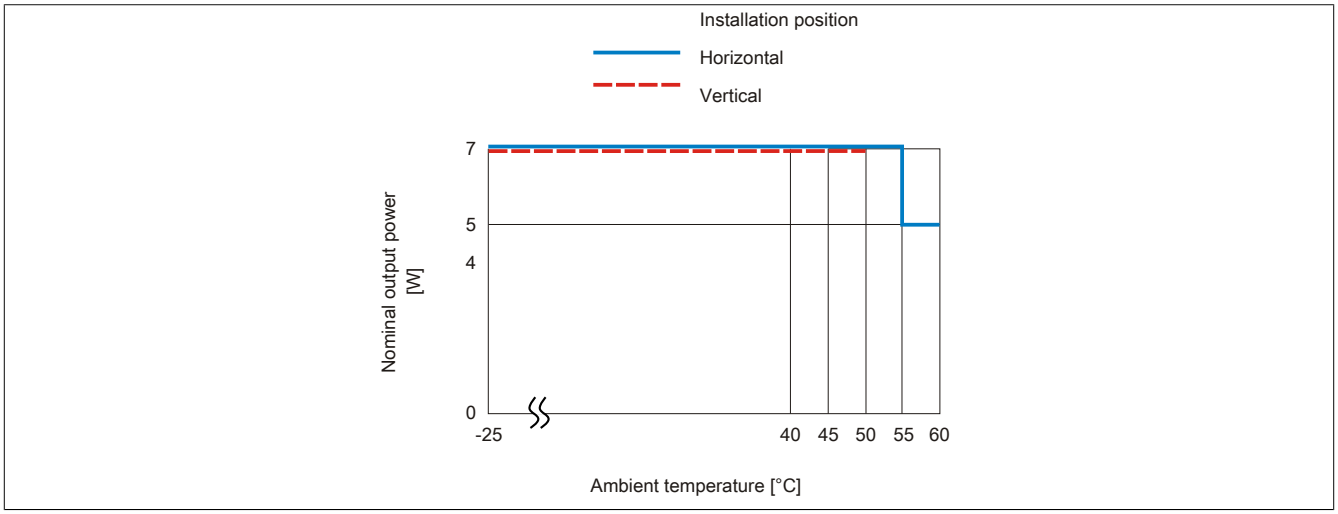


With a supply and jumper



4.8.2.8 Derating

The rated output current for the supply is 7 W. Derating must be taken into consideration based on mounting orientation.



4.8.2.9 Register description

4.8.2.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.8.2.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
2	SupplyCurrent	USINT	•			
4	SupplyVoltage	USINT	•			

4.8.2.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 2				
2	2	SupplyCurrent	UINT	•			
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.8.2.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.8.2.9.4 Module status

Name:
Module status

The following voltage and current states of the module are monitored in this register:

Bus supply current:	A bus supply current of >2.3A is displayed as a warning.
Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Warning - overcurrent (>2.3 A) or undervoltage (<4.7 V)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.8.2.9.5 Bus supply current

Name:
SupplyCurrent

This register displays the bus supply current measured at a resolution of 0.1 A.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.8.2.9.6 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.8.2.9.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.8.2.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.8.3 X20(c)BT9100

4.8.3.1 General information

The bus transmitter provides for the seamless expansion of the X20 System. The stations can be up to 100 m away from each other.

- X2X Link bus transmitter
- For seamless expansion of the system
- Up to 100 m segment lengths
- Feed for internal I/O supply
- Operation only on the slot to the far right

Information:

The bus transmitter modules may only be operated with a bus module where the internal I/O supply is connected through (e.g. X20BM11).

If the incoming voltage is used for internal I/O supply, then this potential group must not be supplied by any other module. An I/O module with bus module X20BM01 should be used to separate the potential group.

4.8.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.8.3.3 Order data

Model number	Short description	Figure
	Bus receivers and transmitters	
X20BT9100	X20 bus transmitter, X2X Link, supply for internal I/O supply	
X20cBT9100	X20 bus transmitter, coated, X2X Link, supply for internal I/O supply	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	X2X Link cable	
X67CA0X99.1000	Cable for custom assembly, 100 m	
X67CA0X99.5000	Cable for custom assembly, 500 m	

Table 155: X20BT9100, X20cBT9100 - Order data

4.8.3.4 Technical data

Product ID	X20BT9100	X20cBT9100
Short description		
Bus transmitter	X2X Link bus transmitter with supply for I/O	
General information		
B&R ID code	0x1BC2	0xE219
Status indicators	X2X bus function, operating status, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
X2X bus function	Yes, using status LED	
Power consumption [1]		
Bus	0.5 W	
Internal I/O		
As bus transmitter	0.1 W	
Additionally as supply module	0.6 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
Input I/O supply		
Input voltage	24 VDC -15 % / +20 %	
Fuse	Required line fuse: Max. 10 A, slow-blow	
Reverse polarity protection	No	
Output I/O supply		
Rated output voltage	24 VDC	
Behavior if a short circuit occurs	Required line fuse	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20BM11 or X20B-M15 bus module separately	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 156: X20BT9100, X20cBT9100 - Technical data

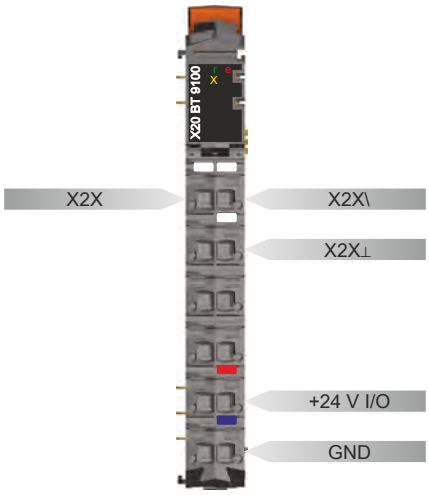
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.8.3.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

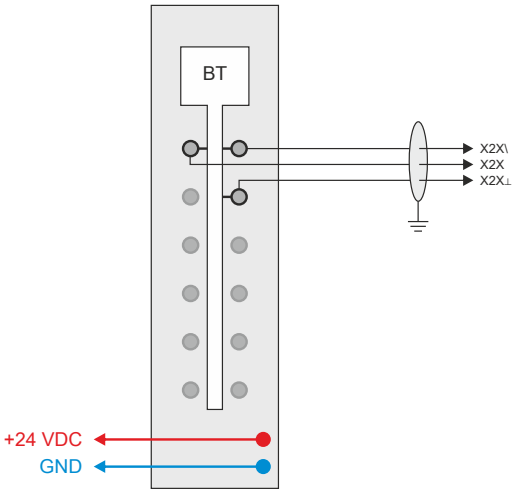
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • I/O supply too low • X2X bus supply too low
	e + r	Red on / Green single flash		Invalid firmware
	X	Orange	Off	No communication at the X2X Link
			On	X2X Link communication in progress

4.8.3.6 Pinout



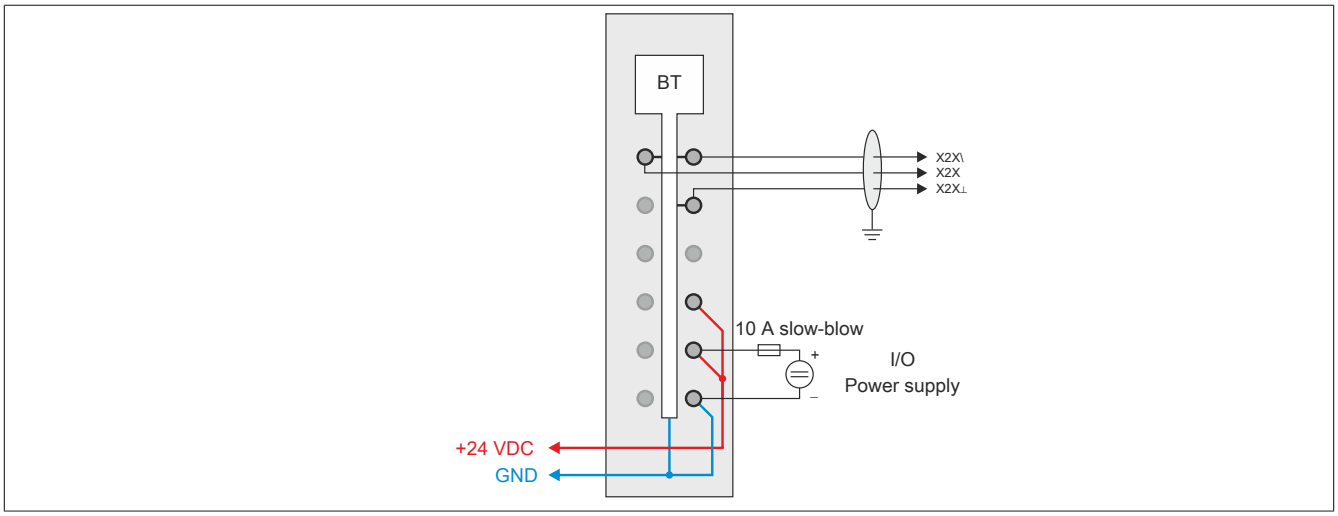
4.8.3.7 Connection examples

No feed for internal I/O supply



With feed for internal I/O supply

See also 3.19.2 "Supply via bus transmitter".



4.8.3.8 Supply via bus transmitter

The bus transmitter has an integrated internal I/O supply feed. This saves a power supply module for the last potential group.

Keep in mind: this potential group is separated from the rest of the potential groups by an I/O module with the bus module.

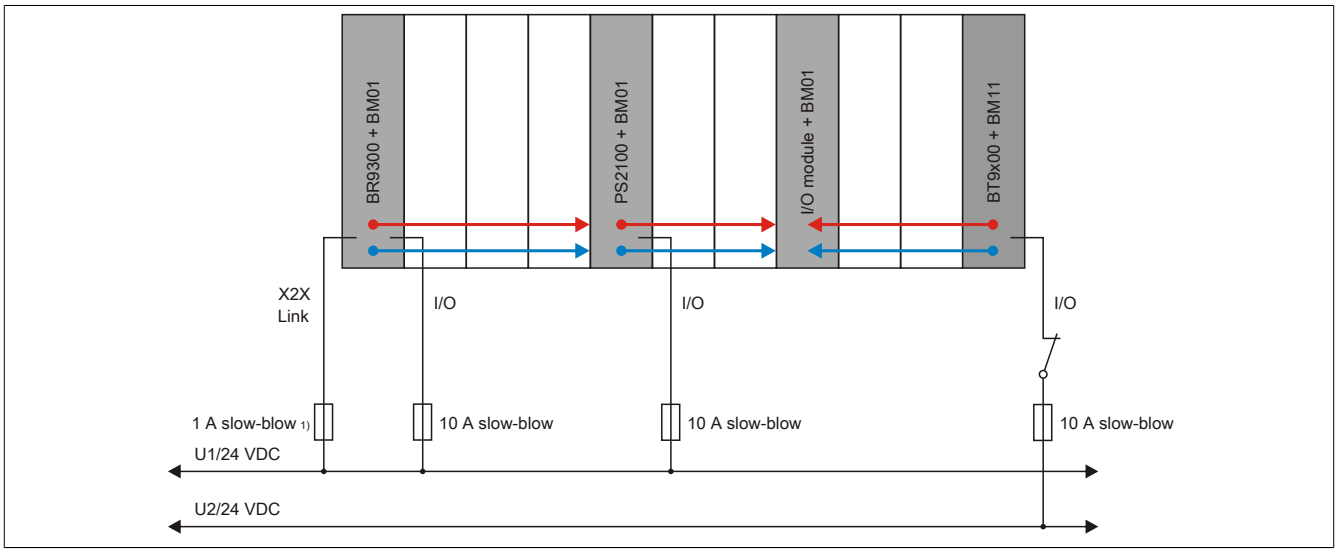


Figure 166: Protection when supplied via bus transmitter

1) Recommended for line protection.

4.8.3.9 Connection to next X2X Link I/O node

The bus transmitter establishes the connection to the next X2X Link based I/O node. It is important to be sure that only the data lines are connected on. X2X Link supply is system dependant.

System	X2X Link supply
X67 system	System supply X67PS1300
Remote I/O with X2X Link (XX modules)	24 VDC external supply
Remote valve terminal connection (XV modules)	24 VDC external supply

Table 157: X20BT9100 - System-dependent X2X Link supply

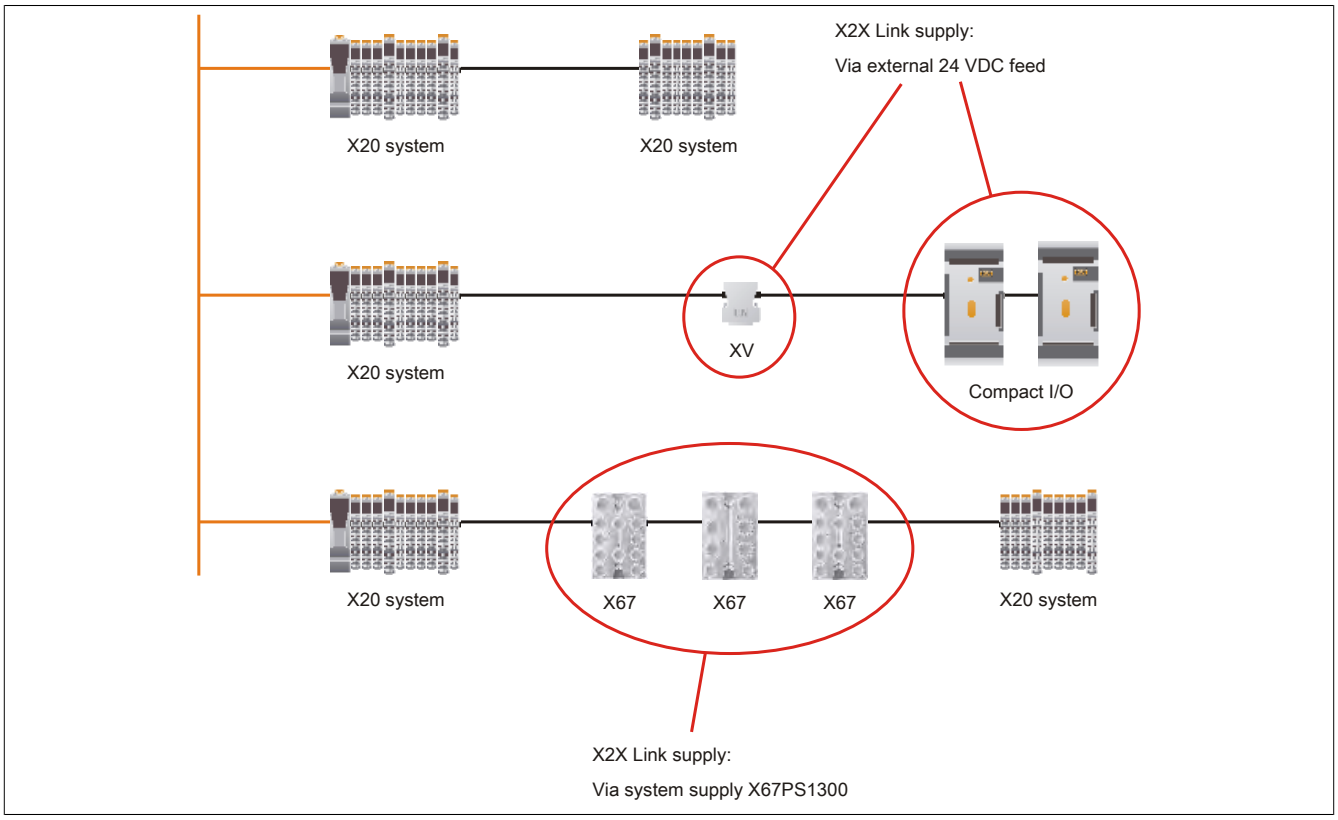


Figure 167: X2X Link supply depending on the system

4.8.3.10 Register description

4.8.3.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.8.3.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
4	SupplyVoltage	USINT	•			

4.8.3.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 2				
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.8.3.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.8.3.10.4 Module status

Name:
Module status

The following module supply voltages are monitored in this register:

Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Bus supply warning - Undervoltage (<4.7V)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.8.3.10.5 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.8.3.10.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.8.3.10.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.8.4 X20BT9400

4.8.4.1 General information

To connect an X20 system to an X67 system, a bus transmitter is simple added to the end of the X20 block, so that the X2X Link cable can be connected. The bus transmitter also provides the X2X supply voltage for the X67 system. There is no longer a need for an X67 system supply module.

- X2X Link bus transmitter
- For seamless expansion of the system
- Up to 100 m segment lengths
- Feed for internal I/O supply
- Integrated X2X Link supply for the X67 system
- Operation only on the slot to the far right

Information:

The bus transmitter modules may only be operated with a bus module where the internal I/O supply is connected through (e.g. X20BM11).

If the incoming voltage is used for internal I/O supply, then this potential group must not be supplied by any other module. An I/O module with bus module X20BM01 should be used to separate the potential group.

4.8.4.2 Order data

Model number	Short description	Figure
	Bus receivers and transmitters	
X20BT9400	X20 bus transmitter X2X Link, feed for internal I/O supply, X2X Link supply for X67 modules, reverse polarity protection, short circuit protection, overload protection, parallel connection possible, redundancy operation possible	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	X2X Link cable	
X67CA0X99.1000	Cable for custom assembly, 100 m	
X67CA0X99.5000	Cable for custom assembly, 500 m	

Table 158: X20BT9400 - Order data

4.8.4.3 Technical data

Product ID	X20BT9400
Short description	
Bus transmitter	X2X Link bus transmitter with supply for I/O and integrated supply for the X67 system
General information	
B&R ID code	0xA238
Status indicators	X2X bus function, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
X2X bus function	Yes, using status LED
Power consumption [1]	
Bus	0.5 W
Internal X67 X2X Link	1.38 W
Internal I/O	
As bus transmitter	0.1 W
Additionally as supply module	0.6 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GOST-R	Yes
X67 X2X Link supply input	
Input voltage	24 VDC -15% / +20%
Input current	Max. 0.5 A
Fuse	Integrated, cannot be replaced
Reverse polarity protection	Yes
X67 X2X Link supply output	
Parallel connection with X67PS1300	Yes [3]
Overload behavior	Temporarily protected against short circuit, overload Be aware of corresponding status message (LED "I") or evaluate software status
X67 modules supplied by BT9400	
Horizontal installation	Max. 8 (Nominal output power: 6 W)
Vertical installation	Max. 6 (Nominal output power: 4.5 W)
Input I/O supply	
Input voltage	24 VDC -15% / +20%
Fuse	Required line fuse: Max. 10 A, slow-blow
Reverse polarity protection	No
Output I/O supply	
Rated output voltage	24 VDC
Behavior if a short circuit occurs	Required line fuse
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 or 1x X20BM15 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 159: X20BT9400 - Technical data

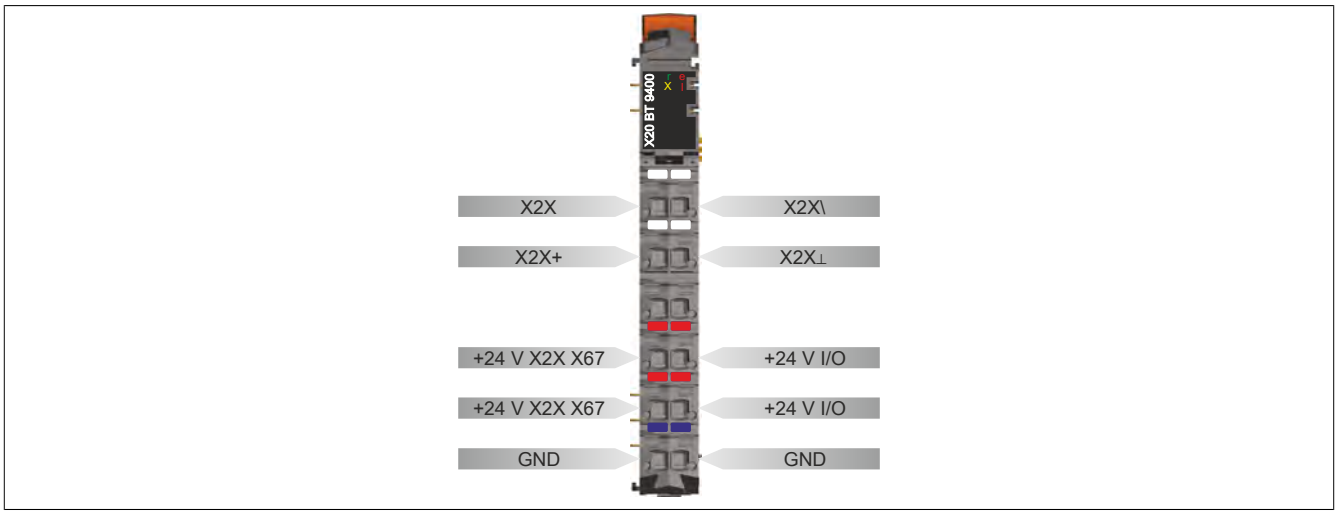
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions
3) Only the PS1300 can be used for calculating the total number of X67 modules.

4.8.4.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

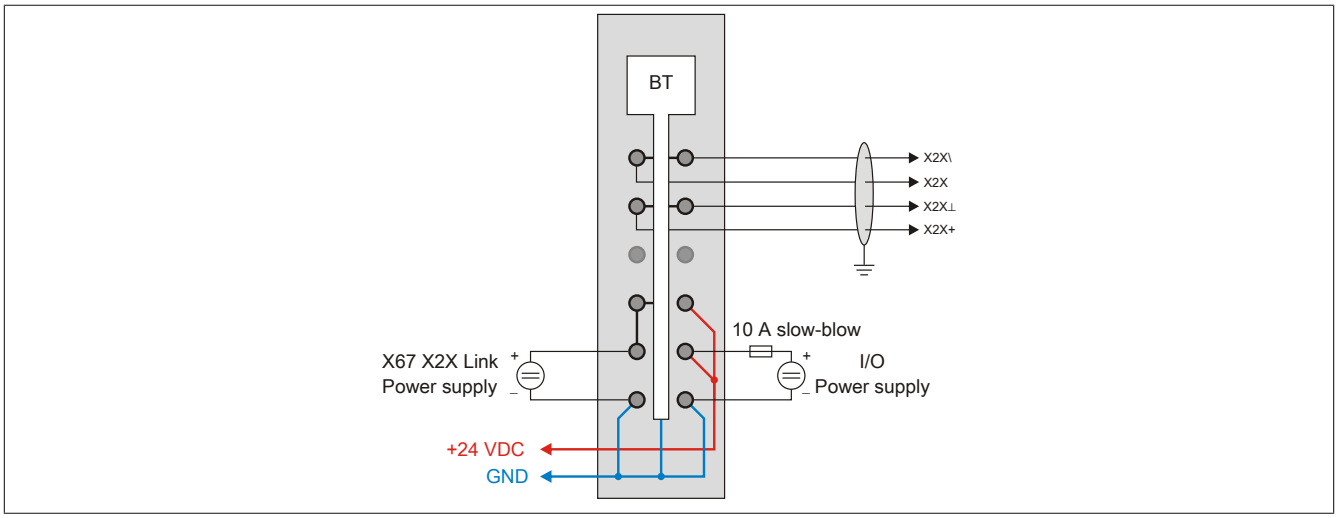
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • I/O supply too low • X2X Link voltage too low
	e + r	Red on / Green single flash		Invalid firmware
	X	Orange	Off	No X2X Link communication
			On	X2X Link communication active
	l	Red	Off	The X67 / X2X Link supply is within the valid limits
			On	The X67 / X2X Link supply for the power supply is overloaded **Remedy:** Use additional X67PS1300 supply modules

4.8.4.5 Pinout

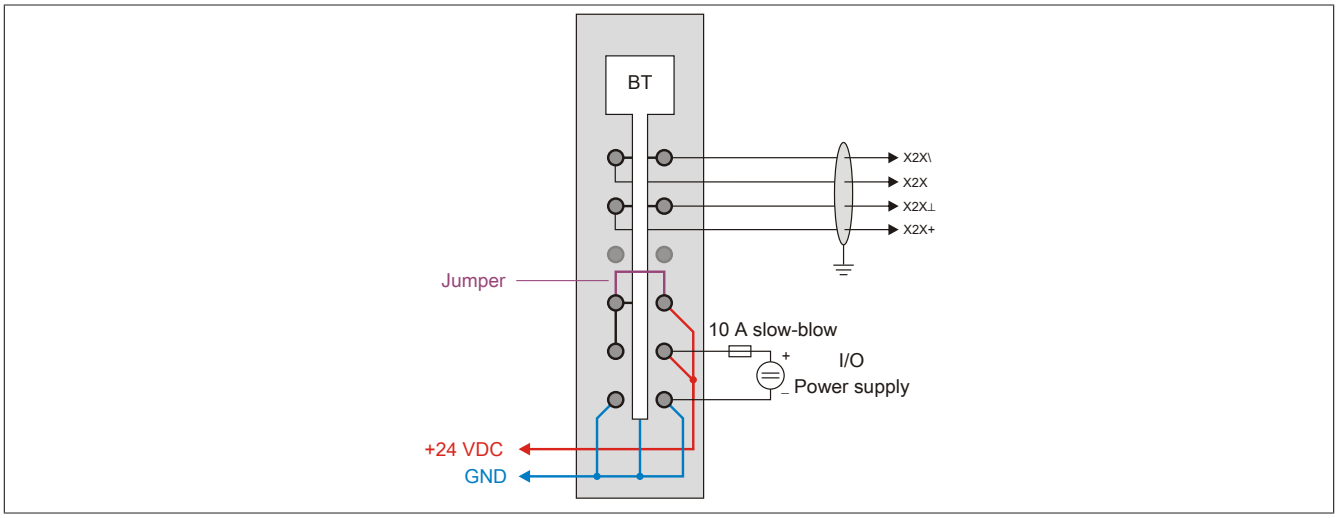


4.8.4.6 Connection examples

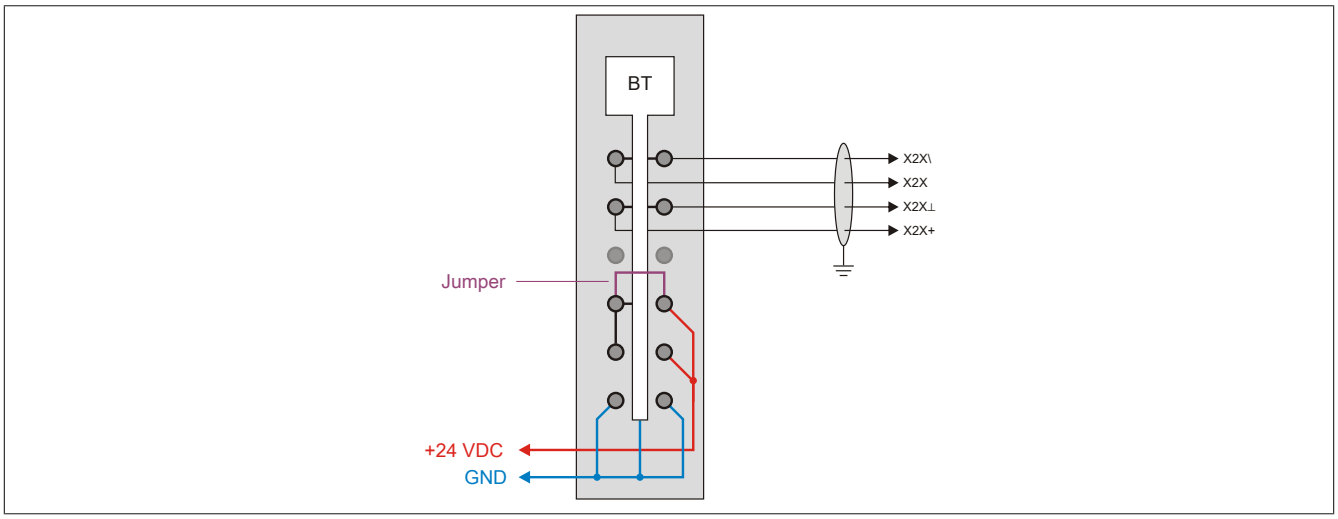
With 2 separate supplies



With a supply and jumper



No feed for internal I/O supply



4.8.4.7 Supply via bus transmitter

The bus transmitter has an integrated internal I/O supply feed. This saves a power supply module for the last potential group.

Keep in mind: this potential group is separated from the rest of the potential groups by an I/O module with the bus module.

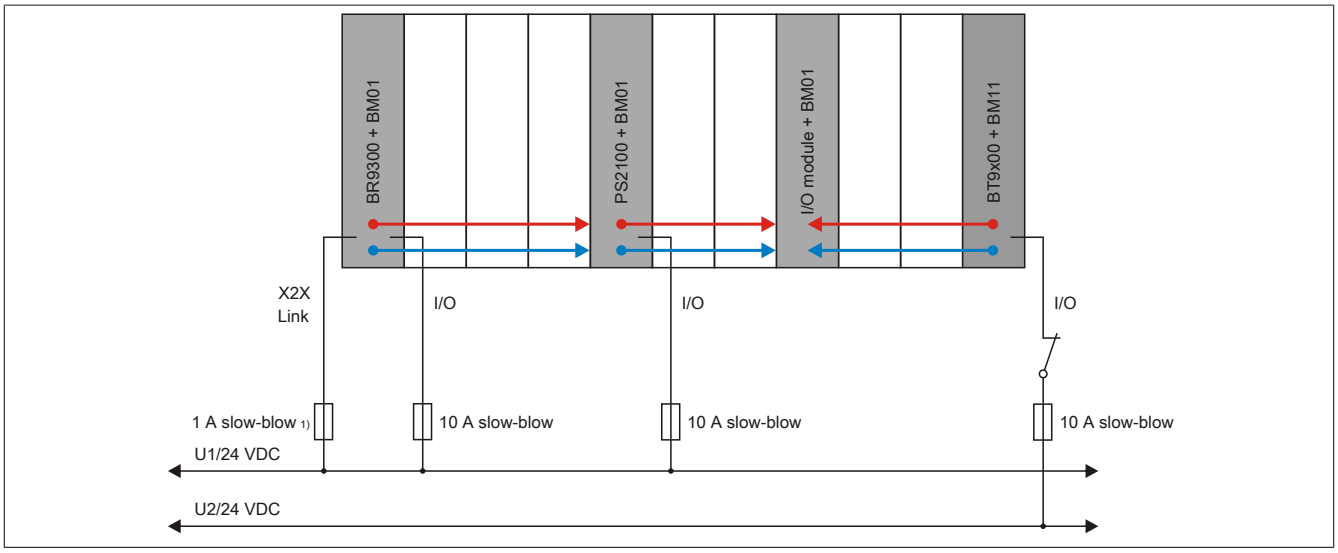


Figure 168: Protection when supplied via bus transmitter

1) Recommended for line protection.

4.8.4.8 Connection between X20 and X67 system

The bus transmitter establishes the link between the X20 system and the X67 system. In addition to the data lines, the X2X Link supply is also fed through. The module can supply up to 8 X67 modules. An additional X67 supply module is only needed if operating more than 8 X67 modules.

Information:

Only the X67PS1300 system supply module can be used for calculating the total number of X67 modules.

4.8.4.9 Register description

4.8.4.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.8.4.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
2	SupplyCurrent	USINT	•			
4	SupplyVoltage	USINT	•			

4.8.4.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 2				
2	2	SupplyCurrent	UINT	•			
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.8.4.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.8.4.9.4 Module status

Name:
Module status

The following module supply voltages are monitored in this register:

X67 bus supply current:	An X67 bus supply current of >0.4 A is displayed as a warning.
X67 bus supply voltage:	A bus supply voltage of <18 V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	X67 bus supply warning for undervoltage (18 V) or when over-current (0.4 A)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.8.4.9.5 X67 bus supply current

Name:
SupplyCurrent

This register shows the X67 bus supply current with a resolution of 0.01 A.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.8.4.9.6 X67 bus supply voltage

Name:
SupplyVoltage

This register shows the X67 bus supply voltage with a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.8.4.9.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.8.4.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.9 Compact CPUs

The modular structure of the Compact CPUs allows the user to assemble a CPU that meets their unique power supply and interface requirements.

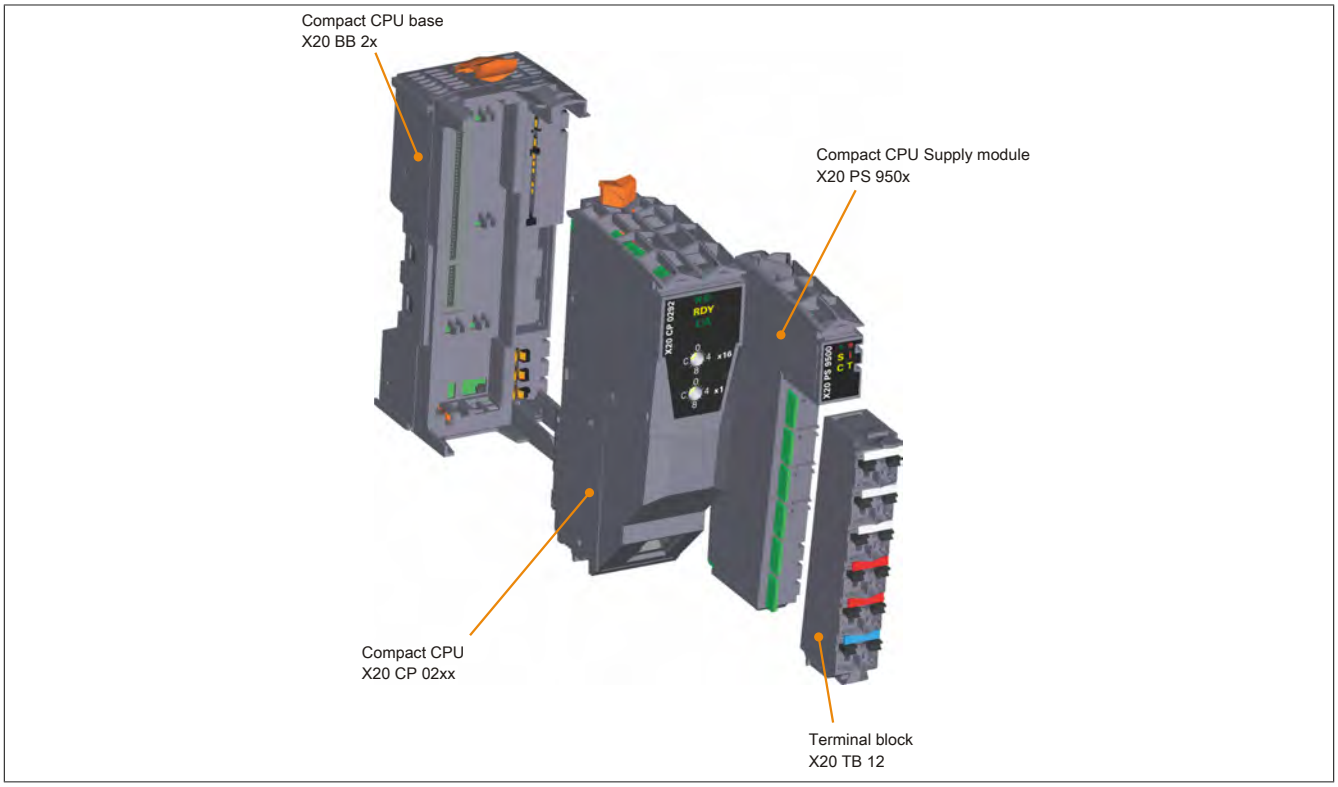


Figure 169: The four parts of the Compact CPU - Compact CPU, bus module, supply module, terminal block

Adaptable to individual requirements

- Embedded µP 25 with Ethernet on-board
- Embedded µP 16 with or without Ethernet on-board

- Bus module with RS232 connection
- Bus module with RS232 and CAN bus connections

- Supply module for Compact CPU, X2X Link bus supply and I/O
- RS232 interface connection
- CAN bus connection
- Without or without electrical isolation of the CPU/X2X Link supply

- 12-pin terminal block

The battery-free CPU

To meet the high demands of the market, the Compact CPU was designed to run without a battery. This makes it completely maintenance-free. The following features make operation without a buffer battery possible.

The real-time clock is buffered for approx. 1000 hours by a gold foil capacitor.

This FRAM stores its contents ferroelectrically. Unlike normal SRAM, this does not require a battery.

Compact design

Despite the sleek profile of only 37.5 mm, the CPU supply, the X2X Link bus supply, and the I/O module supply are integrated in the CPU. No additional power modules are necessary.

4.9.1 Brief information

Product ID	Short description	on page
X20CP0201	X20 compact CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, order bus base, power supply module and terminal block separately	837
X20CP0291	X20 compact CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, 1 Ethernet interface 100 Base-T, order bus base, power supply module and terminal block separately	837
X20CP0292	X20 compact CPU, µP 25, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, 3 Ethernet interface 750 Base-T, order bus base, power supply module and terminal block separately	837

4.9.2 X20CP0201, X20CP0291, X20CP0292

4.9.2.1 General information

Compact CPUs are ideal for situations where cycle times in the millisecond range are sufficient and a cost-benefit analysis plays a decisive role. A range of models with CAN and Ethernet can adapt optimally to all demands. The result: extremely sleek automation solutions.

- Embedded µP 16 / µP 25 with additional I/O processor
- 100/750 kB User SRAM
- 1 MB / 3 MB User FlashPROM
- X20CP0291 and X20CP0292: Onboard Ethernet
- Only 37.5 mm wide
- No battery

4.9.2.2 Order data

CP0201

CP0291, CP0292

Model number	Short description
	Compact CPUs
X20CP0201	X20 compact CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, order bus base, power supply module and terminal block separately
X20CP0291	X20 compact CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, 1 Ethernet interface 100 Base-T, order bus base, power supply module and terminal block separately
X20CP0292	X20 compact CPU, µP 25, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus according to compact CPU base, 3 Ethernet interface 750 Base-T, order bus base, power supply module and terminal block separately
	Required accessories
	System modules for compact CPUs
X20BB22	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB27	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20PS9500	X20 supply module for compact and fieldbus CPUs and internal I/O supply, X2X Link supply
X20PS9502	X20 supply module, for compact and fieldbus CPUs and internal I/O supply, X2X Link supply, supply not electrically isolated
	Terminal blocks
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed

Table 160: X20CP0201, X20CP0291, X20CP0292 - Order data

Model number	Included in delivery
X20AC0SL1	X20 locking plate, left
X20AC0SR1	X20 locking plate, right

4.9.2.3 Technical data

Product ID	X20CP0201	X20CP0291	X20CP0292
Short description			
Interfaces	-	1x Ethernet onboard	
System module	CPU		
General information			
B&R ID code	0x22A2	0x22A4	0x22A6
Status indicators	CPU function	CPU function, Ethernet	
Diagnostics			
CPU function	Yes, using status LED		
Ethernet	-	Yes, using status LED	
Overtemperature	-		Yes, using software
Power consumption	2.2 W	2.7 W	3 W
Temperature sensor	No		Yes
ACOPOS capability	Limited (User PROM)		Yes
Visual Components support	Limited (User PROM)		Yes
Additional power dissipation caused by the actuators (resistive) [W]	-		
Electrical isolation			
PLC - IF2	-	Yes	
Certification			
CE	Yes		
cULus	Yes		
cCSAus HazLoc Class 1 Division 2	Yes		
ATEX Zone 2 [1]	Yes		
KC	Yes		
GL	Yes		
GOST-R	Yes		
Controller			
Real-time clock [2]	Yes, 1 s resolution, -18 to 28 ppm accuracy at 25°C		
Processor			
Type	Embedded µP 16		Embedded µP 25
Integrated I/O processor	Processes I/O data points in the background		
Backup battery	No		
Shortest task class cycle time	4 ms		2 ms
Typical instruction cycle time	0.8 µs		0.5 µs
Permanent variables			
Buffer duration	>10 years		
Memory	2.75 kB FRAM [3]		
Standard memory			
User PROM	1 MB FlashPROM		3 MB FlashPROM
User RAM	100 kB SRAM [4]		750 kB SRAM [4]
Interfaces			
IF2 interface			
Signal	-	Ethernet	
Design	-	1x RJ45 shielded	
Cable length	-	Max. 100 m between 2 stations (segment length)	
Transfer rate	-	100 Mbit/s	
Transmission			
Physical layer	-	100BASE-TX	
Half-duplex	-	Yes	
Full-duplex	-	No	
Autonegotiation	-	No	
Auto-MDI / MDIX	-	Yes	
On base module			
X20BB22 [5]	Compact CPU base module with integrated RS232 interface		
X20BB27 [6]	Compact CPU base module with integrated RS232 and CAN interfaces		
Operating conditions			
Mounting orientation			
Horizontal	Yes		
Vertical	Yes		
Installation at elevations above sea level			
0 to 2000 m	No limitations		
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m		
EN 60529 protection	IP20		
Environmental conditions			
Temperature			
Operation			
Horizontal installation	-25 to 60°C		
Vertical installation	-25 to 50°C		
Derating	-		
Storage	-40 to 85°C		
Transport	-40 to 85°C		

Table 161: X20CP0201, X20CP0291, X20CP0292 - Technical data

Product ID	X20CP0201	X20CP0291	X20CP0292
Relative humidity			
Operation	5 to 95%, non-condensing		
Storage	5 to 95%, non-condensing		
Transport	5 to 95%, non-condensing		
Mechanical characteristics			
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9500 or X20PS9502 power supply module separately Order 1x X20BB22 or X20BB27 compact CPU base separately		
Spacing 7)	$37.5^{+0.2}$ mm		

Table 161: X20CP0201, X20CP0291, X20CP0292 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The real-time clock is buffered for approx. 1000 hours by a gold foil capacitor. The gold foil capacitor is completely charged after 18 continuous hours of operation.
3) This FRAM stores its contents ferroelectrically. Therefore, no backup battery is needed.
4) Not buffered.
5) For technical data, see the data sheet for the X20PS9500 power supply module.
6) For technical data, see the data sheet for the X20PS9502 power supply module.
7) Spacing is based on the width of the compact CPU base X20BB22 or X20BB27. An X20PS9500 or X20PS9502 supply module is also always required for the CPU.

4.9.2.4 LED status indicators

X20CP0201

Figure	LED	Color	Status	Description
	R/E	Green	On	Application running
		Red	On	SERVICE mode
			Off	1)
	RDY	Yellow	On	SERVICE mode
			Off	1)

1) BOOT mode: R/E and RDY LEDs are off and the power supply LED is blinking

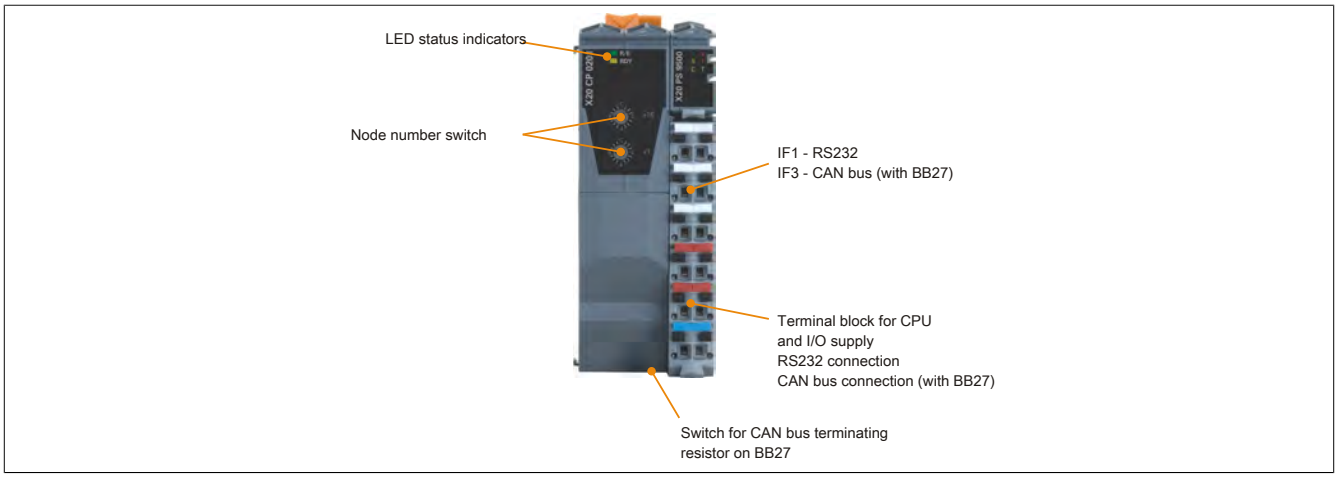
X20CP029x

Figure	LED	Color	Status	Description
	R/E	Green	On	Application running
		Red	On	SERVICE mode
			Off	1)
	RDY	Yellow	On	SERVICE mode
			Off	1)
	L/A	Green	On	A link to the peer station has been established.
			Blinking	A link to the peer station has been established. Indicates Ethernet activity is taking place on the bus.

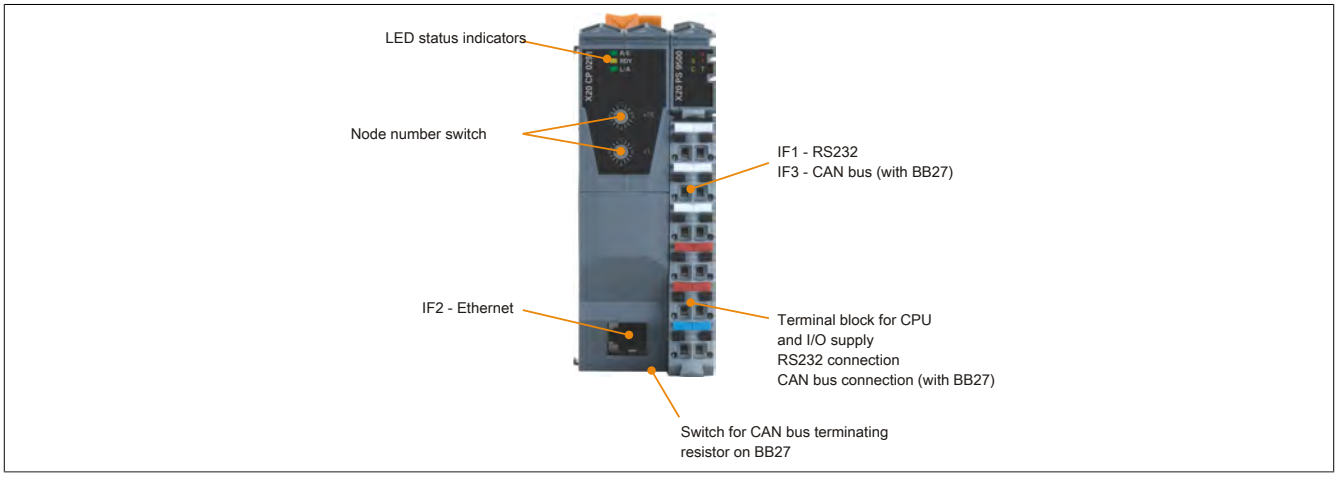
1) BOOT mode: R/E and RDY LEDs are off and the power supply LED is blinking

4.9.2.5 Operating and connection elements

X20CP0201



X20CP0291 and X20CP0292



4.9.2.6 Node number switches

The node number is set using the two hex switches. The switch setting can be evaluated by the application program at any time. The operating system only evaluates the switch position when the device is switched on.

Switch position	Operating mode	Description
0x00	BOOT	In this switch position, the operating system can be installed via the RS232 interface configured as the online interface. User Flash is deleted only after the update begins.
0x01 - 0xFE	RUN	RUN mode, the application is running.
0xFF	Diagnostics	Boots the CPU in Diagnostics mode. Program sections in User RAM and User FlashPROM are not initialized. Following diagnostics mode, the CPU always boots with a **cold restart**.

X20CP0201

When used with the X20BB27 bus module, the X20CP0201 has access to a CAN bus interface. The INA2000 station number for CAN is set using the node number switches.

X20CP0291 and X20CP0292

Both of these CPUs are equipped with an onboard Ethernet interface. When used with the X20BB27 bus module, they also have access to a CAN bus interface.

The number set using the two hex switches defines the INA2000 station number of both the CAN and the Ethernet interface.

4.9.2.7 Ethernet interface (IF2)

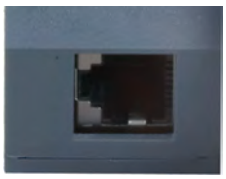
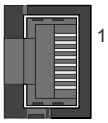


Figure 170: X20 compact CPUs - Ethernet interface for X20CP0291 and X20CP0292

The X20CP0291 and X20CP0292 are equipped with an Ethernet interface. The connection is made using a 100 BASE-T twisted pair RJ45 socket.

Pinout

Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).

Information:

The Ethernet interface (IF2) is not suited for POWERLINK.

Starting with operating system version 1.07, CPUs have a default IP address.

IP address: 192.168.0.1
Subnet mask: 255.255.0.0

4.9.2.8 Programming the system flash memory

General information

CPUs are delivered with a runtime system. When delivered, the node number switch is set to switch position 0x00 (bootstrap loader mode).

A suitable switch position must be set (0x01 to 0xFE) in order to boot the PLC in RUN mode. Updating the runtime system is only possible in RUN mode.

Runtime system update

The runtime system can be updated via the programming environment. When updating the runtime system via an online connection, the following procedure must be carried out:

1. An online runtime system update is only possible if the processor is in RUN mode. For this to be true, the node number must be set to a value in the range 0x01 to 0xFE.
2. Switch on the power.
3. The runtime system update is performed via the existing online connection. The online connection can be established via the onboard serial RS232 interface, for example. If a CPU has an Ethernet interface, then it too can be used to perform the update.
4. Start B&R Automation Studio.
5. Start the update procedure by selecting **Online** from the **Project** menu. Select **Transfer Automation Runtime** from the pop-up menu. Now follow the instructions given by B&R Automation Studio.
6. A window opens up for setting the runtime system version. The runtime system version is already pre-selected by the project settings made by the user. The drop-down menu can be used to select one of the runtime system versions stored in the project. Clicking on the **Browse** button allows a runtime system version to be loaded from the hard drive or CD.

   Clicking on **Next** opens a pop-up window that allows the user to select whether modules with target memory SYSTEM ROM should be transferred during the subsequent runtime system update. If not, these modules can also be transferred later during an application download.

   Clicking on **Next** opens a dialog box where the user can set the CAN transfer rate, CAN ID and CAN node number (the CAN node number set here is only relevant if an interface module does not have a CAN node number switch). The CAN node number must be between decimal 01 and 99. Assigning a unique node number is especially important with online communication over a CAN network (INA2000 protocol).
7. The update procedure is started by clicking on **Next**. Update progress is shown in a message box.

   > **Information:**
   >
   > **User flash memory is deleted.**
8. When the update procedure is complete, the online connection is reestablished automatically.
9. The PLC is now ready for use.

Updating the runtime system is possible not only via an online connection, but also via a CAN network, serial network (INA2000 protocol) or Ethernet network, depending on the system configuration.

4.10 Compact CPUs system modules

The X20 system Compact CPUs consist of the Compact CPU, Compact CPU system modules and the X20TB12 terminal block.

The Compact CPU system modules also include the X20BB22 and X20BB27 base modules as well as the X20PS9500 supply module for supplying the entire system with voltage.

4.10.1 Brief information

Product ID	Short description	on page
X20BB22	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	844
X20BB27	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	846
X20PS9500	X20 supply module for compact and fieldbus CPUs and internal I/O supply, X2X Link supply	848
X20PS9502	X20 supply module, for compact and fieldbus CPUs and internal I/O supply, X2X Link supply, supply not electrically isolated	854

4.10.2 X20BB22

4.10.2.1 General information

The bus module is the base for all X20 Compact CPUs.

The left and right end plates are included in the delivery.

- Base for all X20 Compact CPUs
- RS232 connection

4.10.2.2 Order data

Model number	Short description	Figure
	System modules for compact CPUs	
X20BB22	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included	

Table 162: X20BB22 - Order data

4.10.2.3 Technical data

Product ID	X20BB22
Short description	
Bus module	X20 compact CPU base - backplane for compact CPU and compact CPU supply module
Interfaces	1x RS232 connection
General information	
Power consumption	
Bus	0.32 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - RS232	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20

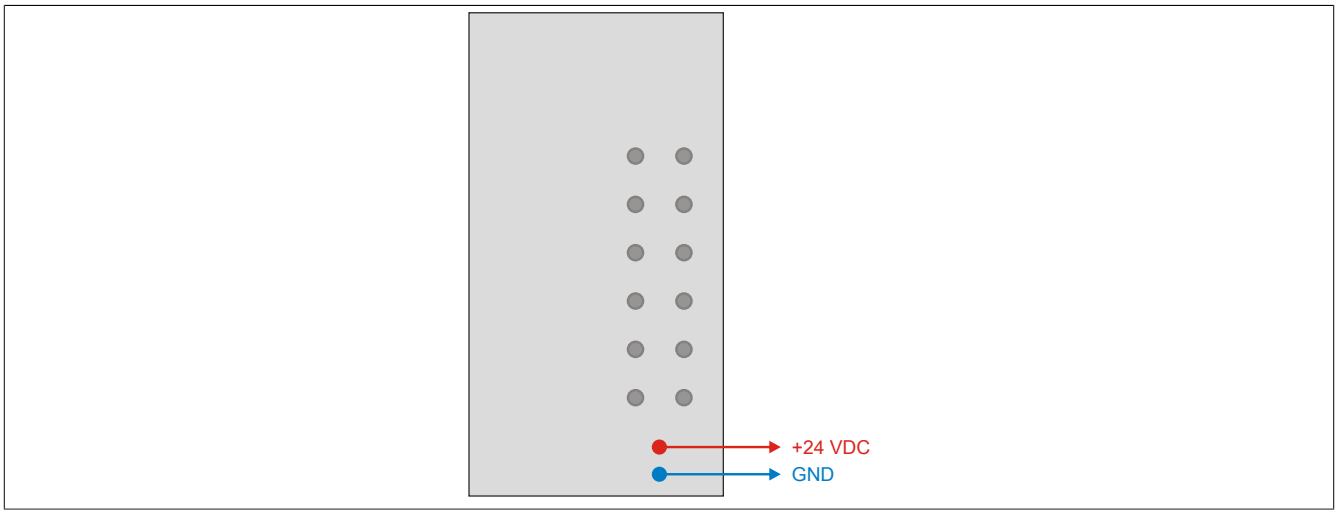
Table 163: X20BB22 - Technical data

Product ID	X20BB22
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Left and right X20 locking plates included in delivery
Spacing	37.5 $^{+0.2}$ mm

Table 163: X20BB22 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.10.2.4 Voltage routing



4.10.3 X20BB27

4.10.3.1 General information

The bus module is the base for all X20 Compact CPUs.

The left and right end plates are included in the delivery.

- Base for all X20 Compact CPUs
- RS232 connection
- CAN bus connection
- Integrated terminating resistor for CAN bus

4.10.3.2 Order data

Model number	Short description	Figure
	System modules for compact CPUs	
X20BB27	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	

Table 164: X20BB27 - Order data

4.10.3.3 Technical data

Product ID	X20BB27
Short description	
Bus module	X20 compact CPU base - backplane for compact CPU and compact CPU supply module
Interfaces	1x RS232 connection, 1x CAN bus connection
General information	
Power consumption	
Bus	0.53 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - CAN bus	No
Bus - RS232	No
RS232 - CAN bus	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20

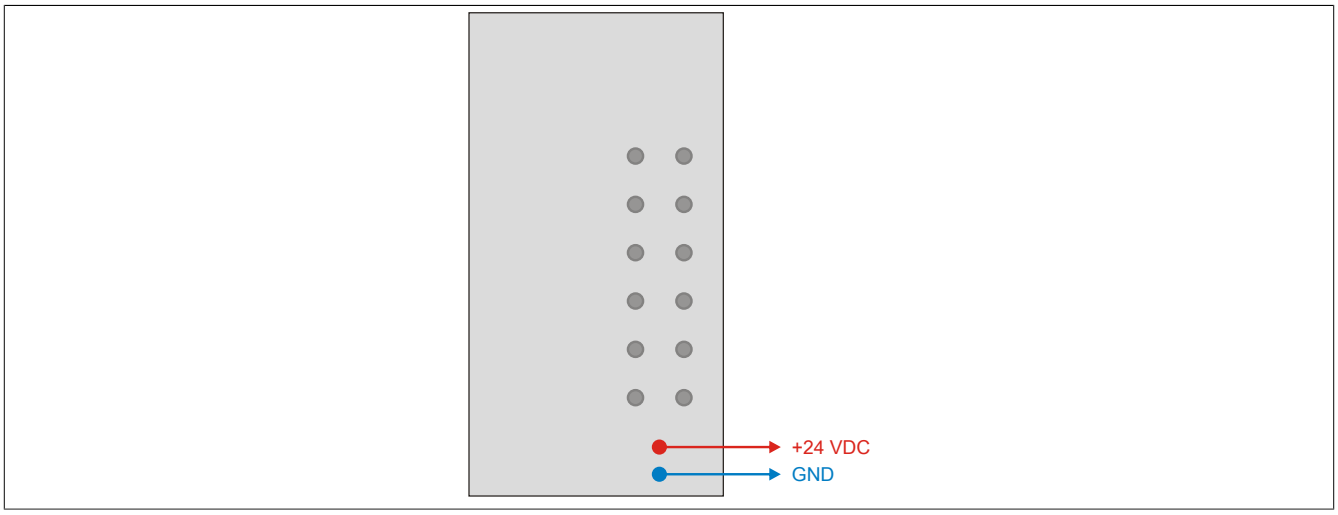
Table 165: X20BB27 - Technical data

Product ID	X20BB27
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Left and right X20 locking plates included in delivery
Spacing	37.5 $^{+0.2}$ mm

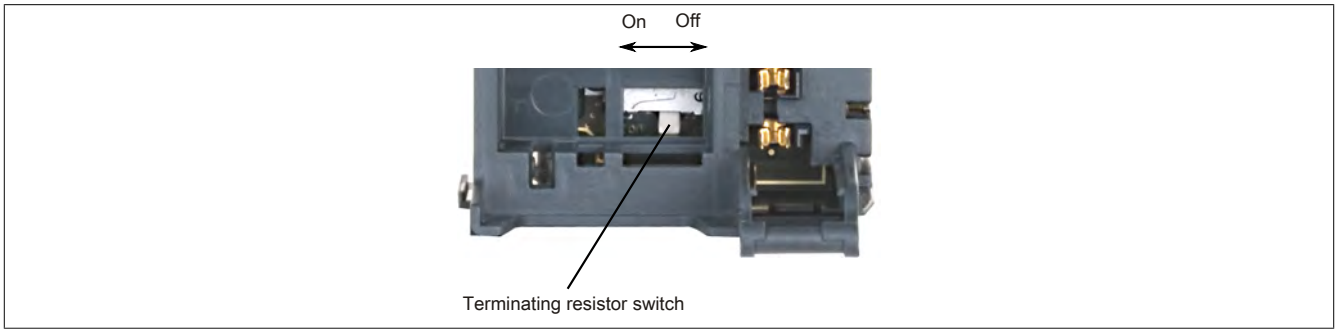
Table 165: X20BB27 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.10.3.4 Voltage routing



4.10.3.5 Terminating resistor for CAN bus



The bus module has an integrated CAN bus terminating resistor. The terminating resistor is turned on and off with a switch. An active terminating resistor is indicated on the supply module by the "T" LED.

4.10.4 X20PS9500

4.10.4.1 General information

The supply module is used together with an X20 compact or fieldbus CPU. It has a feed for the compact or fieldbus CPU, the X2X Link and the internal I/O supply.

- Supply for the compact or fieldbus CPU, X2X Link, and internal I/O supply
- Electrical isolation of feed and CPU / X2X Link supply
- Redundancy of CPU / X2X Link supply possible by operating multiple supply modules simultaneously
- RS232 interface configurable as online interface
- CAN bus

4.10.4.2 Order data

Model number	Short description	Figure
	System modules for compact CPUs	
X20PS9500	X20 supply module for compact and fieldbus CPUs and internal I/O supply, X2X Link supply	
	Required accessories	
	System modules for compact CPUs	
X20BB22	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20BB27	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for fieldbus CPUs	
X20BB32	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB37	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB42	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB47	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 166: X20PS9500 - Order data

4.10.4.3 Technical data

Product ID	X20PS9500
Short description	
Power supply module	24 VDC supply module for compact or fieldbus CPU, X2X Link supply and I/O
Interfaces	1x RS232, 1x CAN bus [1]
General information	
B&R ID code	0x2018
Status indicators	Overload, operating state, module status, RS232, CAN bus [1]
Diagnostics	
Module run/error	Yes, using status LED and software
CAN bus data transfer [1]	Yes, using status LED
RS232 data transfer	Yes, using status LED
Overload	Yes, using status LED and software
Power consumption [2]	
Bus	1.42 W
Internal I/O	0.6 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
CPU/X2X Link feed - CPU/X2X Link supply	Yes
I/O feed - I/O supply	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [3]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
CPU / X2X Link supply input	
Input voltage	24 VDC -15 % / +20 %
Input current	Max. 0.7 A
Fuse	Integrated, cannot be replaced
Reverse polarity protection	Yes
CPU / X2X Link supply output	
Nominal output power	7 W
Parallel operation	Yes [4]
Redundant operation	Yes
Overload behavior	Short circuit / temporary overload protection
Input I/O supply	
Input voltage	24 VDC -15 % / +20 %
Fuse	Required line fuse: Max. 10 A, slow-blow
Reverse polarity protection	No
Output I/O supply	
Rated output voltage	24 VDC
Behavior if a short circuit occurs	Required line fuse
Permitted contact load	10 A
Interfaces	
IF1 interface	
Signal	RS232
Design	Connection made using 12-pin X20TB12 terminal block
Transfer rate	Max. 115.2 kbit/s
IF3 interface [1]	
Signal	CAN bus
Design	Connection made using 12-pin X20TB12 terminal block
Transfer rate	Max. 1 Mbit/s
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C

Table 167: X20PS9500 - Technical data

Product ID	X20PS9500
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BB22 or X20BB27 compact CPU base separately Order 1x X20BB3x/4x fieldbus CPU base separately
Spacing	12.5$^{+0.2}$ mm

Table 167: X20PS9500 - Technical data

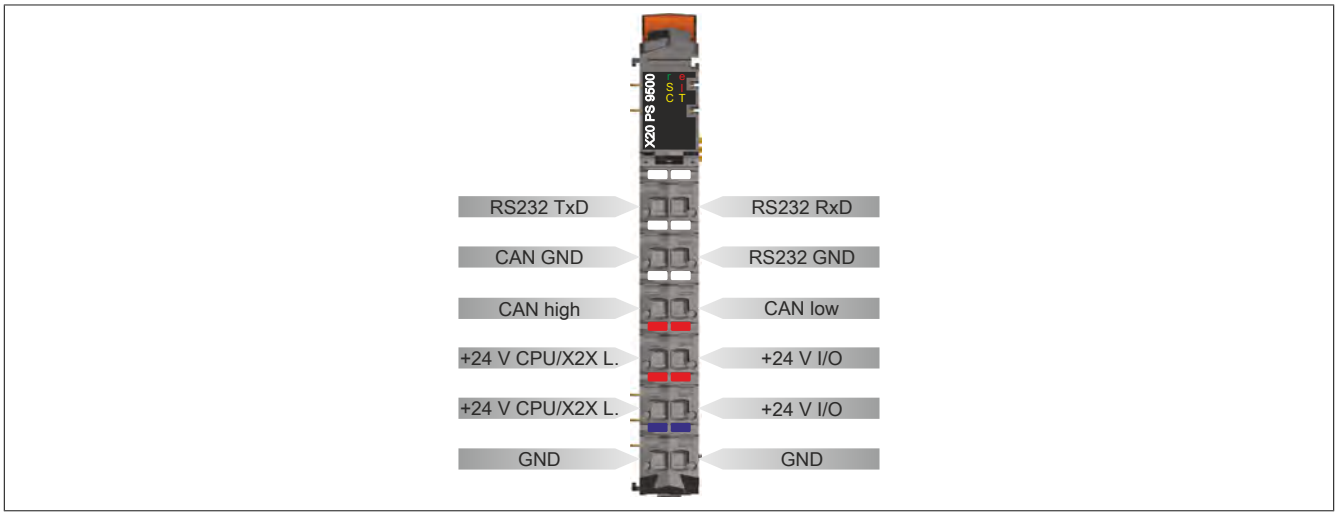
1) CAN bus only when used with the X20BB27, X20BB37 or X20BB47 bus module.
2) The specified values are maximum values. The calculation is also available for download as a data sheet with the other module documentation on the B&R website.
3) Ta min.: 0°C
   Ta max.: See environmental conditions
4) In parallel operation, only 75% of the rated power can be assumed. It is important to make sure that all power supplies operated in parallel are switched on and off at the same time.

4.10.4.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

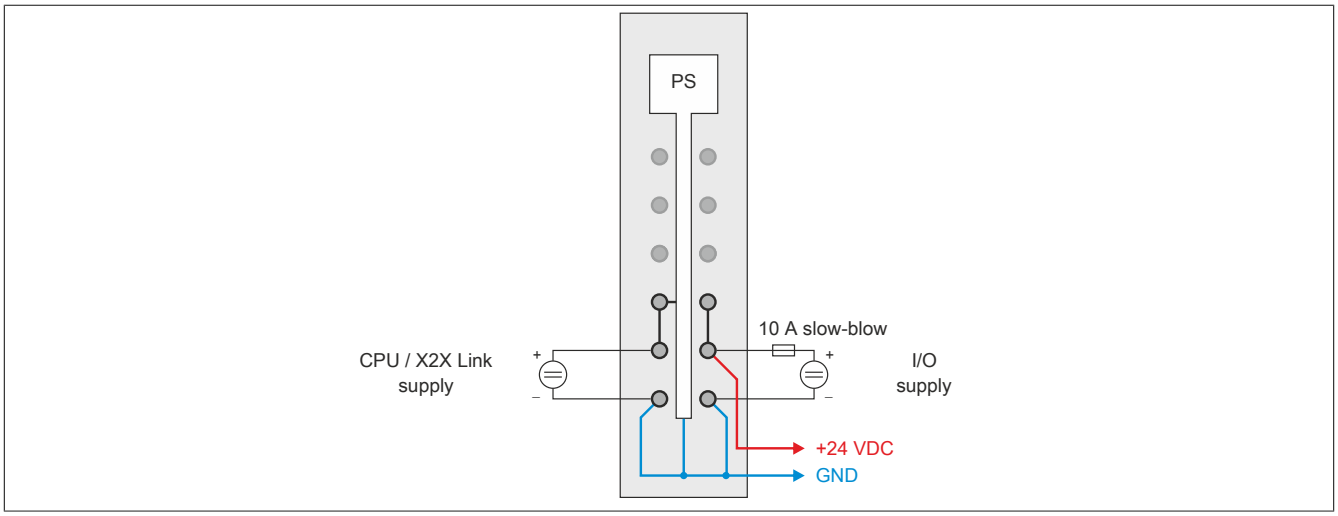
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • The CPU / X2X Link supply for the power supply is overloaded • I/O supply too low • Input voltage for CPU / X2X Link supply too low
	e + r	Red on / Green single flash		Invalid firmware
	I	Red	Off	The CPU / X2X Link supply is within the valid limits
			On	The CPU / X2X Link supply for the power supply is overloaded
	S	Yellow	Off	The CPU does not send data via the RS232 interface.
			On	The CPU sends data via the RS232 interface.
	C	Yellow	Off	The CPU is not sending data via the CAN bus interface.
			On	The CPU is sending data via the CAN bus interface.
	T	Yellow	Off	The terminating resistor integrated in the BB27 or BB37 bus module is turned off.
			On	The terminating resistor integrated in the BB27 or BB37 bus module is turned on.

4.10.4.5 Pinout

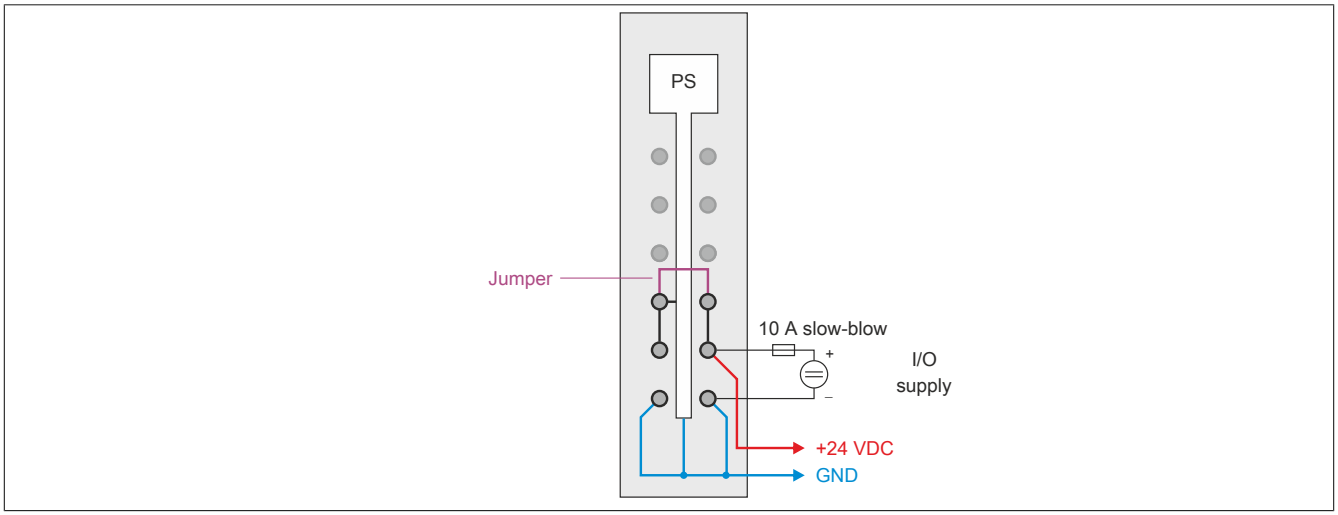


4.10.4.6 Connection examples

With 2 separate supplies

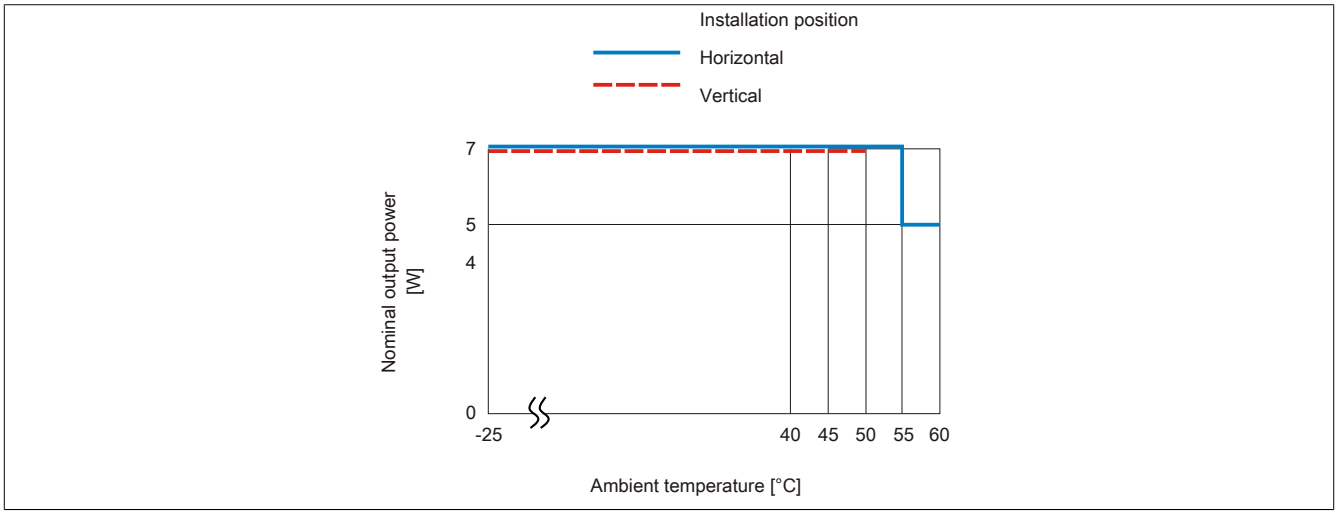


With a supply and jumper



4.10.4.7 Derating

The rated output current for the supply is 7 W. Derating must be taken into consideration based on mounting orientation.



4.10.4.8 Register description

4.10.4.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.10.4.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
2	SupplyCurrent	USINT	•			
4	SupplyVoltage	USINT	•			

4.10.4.8.3 Module status

Name:
Module status

The following module supply voltages are monitored in this register:

Bus supply current:	A bus supply current of >2.3A is displayed as a warning.
Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Warning - overcurrent (>2.3 A) or undervoltage (<4.7 V)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.10.4.8.4 Bus supply current

Name:
SupplyCurrent

This register displays the bus supply current measured at a resolution of 0.1 A.

Function model	Data type
0 - Standard	USINT

4.10.4.8.5 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT

4.10.4.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.10.4.8.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.10.5 X20PS9502

4.10.5.1 General information

The supply module is used together with an X20 Compact or Fieldbus CPU. It is equipped with a feed for the Compact or Fieldbus CPU, the X2X Link and the internal I/O supply.

The module is intended as a low-cost supply module for small X20 Systems. Voltage groups are able to be formed. An expansion or redundancy of the X2X Link with the X20PS3300 or X20PS3310 supply module is not possible. Expansion of the X20 System with a bus transmitter is not permitted either.

- Supply for the Compact or Fieldbus CPU, X2X Link, and internal I/O supply
- Low-cost supply module for small X20 Systems
- No electrical isolation of feed and CPU / X2X Link supply
- Expansion or redundancy of CPU / X2X Link supply not possible by operating multiple supply modules simultaneously
- RS232 can be configured as an online interface
- CAN bus

4.10.5.2 Order data

Model number	Short description	Figure
	System modules for compact CPUs	
X20PS9502	X20 supply module, for compact and fieldbus CPUs and internal I/O supply, X2X Link supply, supply not electrically isolated	
	Required accessories	
	System modules for compact CPUs	
X20BB22	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20BB27	X20 compact CPU base, for compact CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for fieldbus CPUs	
X20BB32	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB37	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB42	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB47	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 168: X20PS9502 - Order data

4.10.5.3 Technical data

Product ID	X20PS9502
Short description	
Power supply module	24 VDC supply module for compact or fieldbus CPU, X2X Link bus supply and I/O
Interfaces	1x RS232, 1x CAN bus [1]
General information	
B&R ID code	0xA38A
Status indicators	Operating state, module status, RS232, CAN bus [1]
Diagnostics	
Module run/error	Yes, using status LED and software
CAN bus data transfer [1]	Yes, using status LED
RS232 data transfer	Yes, using status LED
Overload	Yes, using status LED and software
Power consumption [2]	
Bus	1.44 W
Internal I/O	0.6 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
CPU/X2X Link feed - CPU/X2X Link supply	No
I/O feed - I/O supply	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [3]	Yes
KC	Yes
GOST-R	Yes
CPU / X2X Link supply input	
Input voltage	24 VDC -15 % / +20 %
Input current	Max. 0.7 A
Fuse	Integrated, cannot be replaced
Reverse polarity protection	Yes
CPU / X2X Link supply output	
Nominal output power	
Horizontal installation	7 W at 45°C and 5 W at 55°C
Vertical installation	7 W at 40°C and 5 W at 50°C
Parallel operation	No
Redundant operation	No
Overload behavior	Short circuit / temporary overload protection
Input I/O supply	
Input voltage	24 VDC -15 % / +20 %
Fuse	Required line fuse: Max. 10 A, slow-blow
Reverse polarity protection	No
Output I/O supply	
Rated output voltage	24 VDC
Behavior if a short circuit occurs	Required line fuse
Permitted contact load	10 A
Interfaces	
IF1 interface	
Signal	RS232
Design	Connection made using 12-pin X20TB12 terminal block
Transfer rate	Max. 115.2 kbit/s
IF3 interface [1]	
Signal	CAN bus
Design	Connection made using 12-pin X20TB12 terminal block
Transfer rate	Max. 1 Mbit/s
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C

Table 169: X20PS9502 - Technical data

Product ID	X20PS9502
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BB22 or X20BB27 compact CPU base separately Order 1x X20BB32 or X20BB37 fieldbus CPU base separately
Spacing	12.5$^{+0.2}$ mm

Table 169: X20PS9502 - Technical data

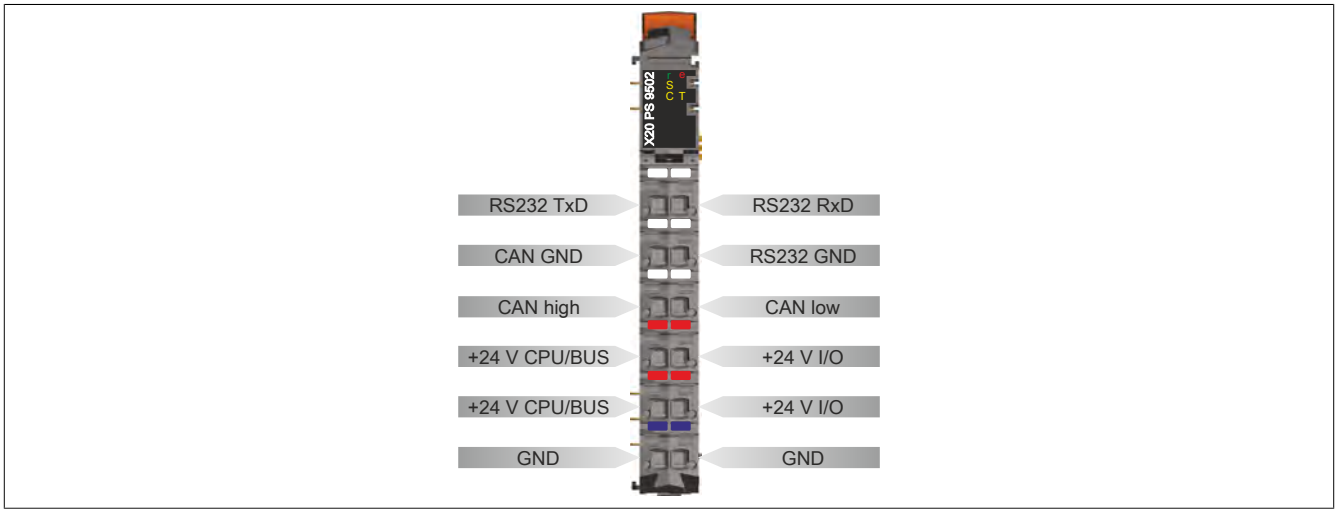
1) CAN bus only when used with the X20BB27 or X20BB37 bus module.
2) The specified values are maximum values. The calculation is also available for download as a data sheet with the other module documentation on the B&R website.
3) Ta min.: 0°C
   Ta max.: See environmental conditions

4.10.5.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

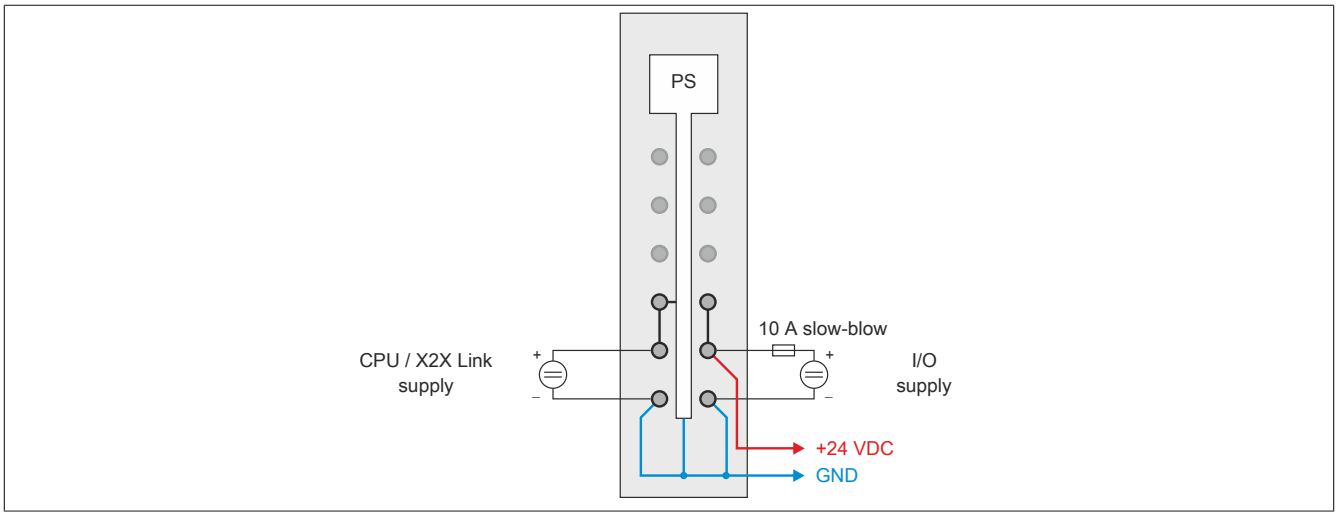
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • The CPU / X2X Link power supply is overloaded • I/O supply too low • Input voltage for CPU / X2X Link too low
	e + r	Red on / Green single flash		Invalid firmware
	S	Yellow	Off	The CPU does not send data via the RS232 interface.
			On	The CPU sends data via the RS232 interface.
	C	Yellow	Off	The CPU does not send data via the CAN bus interface.
			On	The CPU sends data via the CAN bus interface.
	T	Yellow	Off	The terminating resistor integrated in the X20BB27 or X20BB37 bus module is turned off.
			On	The terminating resistor integrated in the X20BB27 or X20BB37 bus module is turned on.

4.10.5.5 Pinout

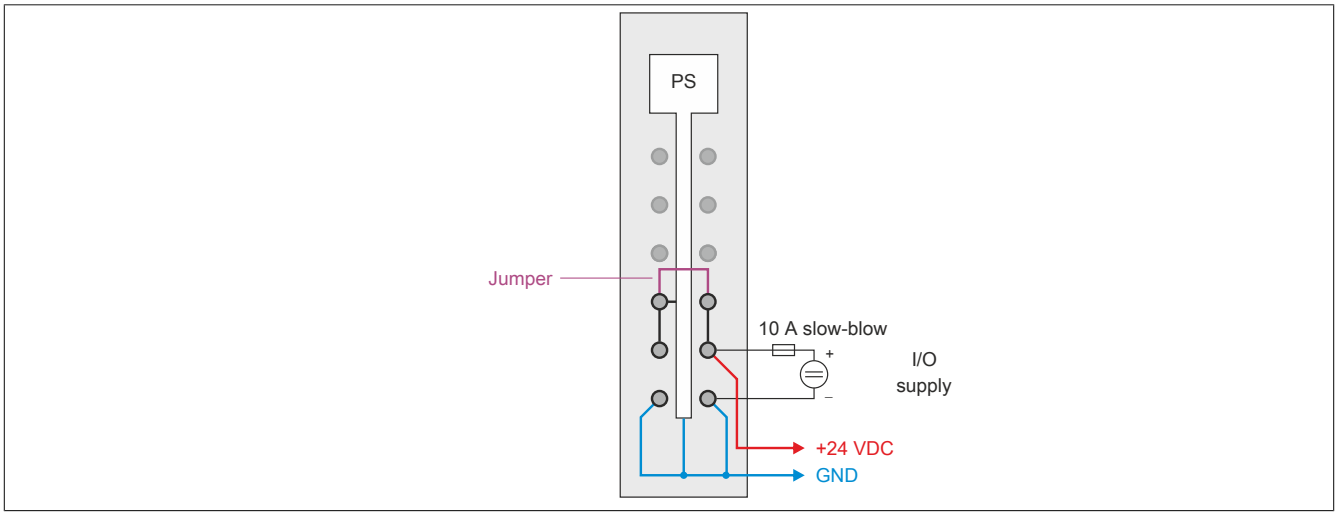


4.10.5.6 Connection examples

With 2 separate supplies

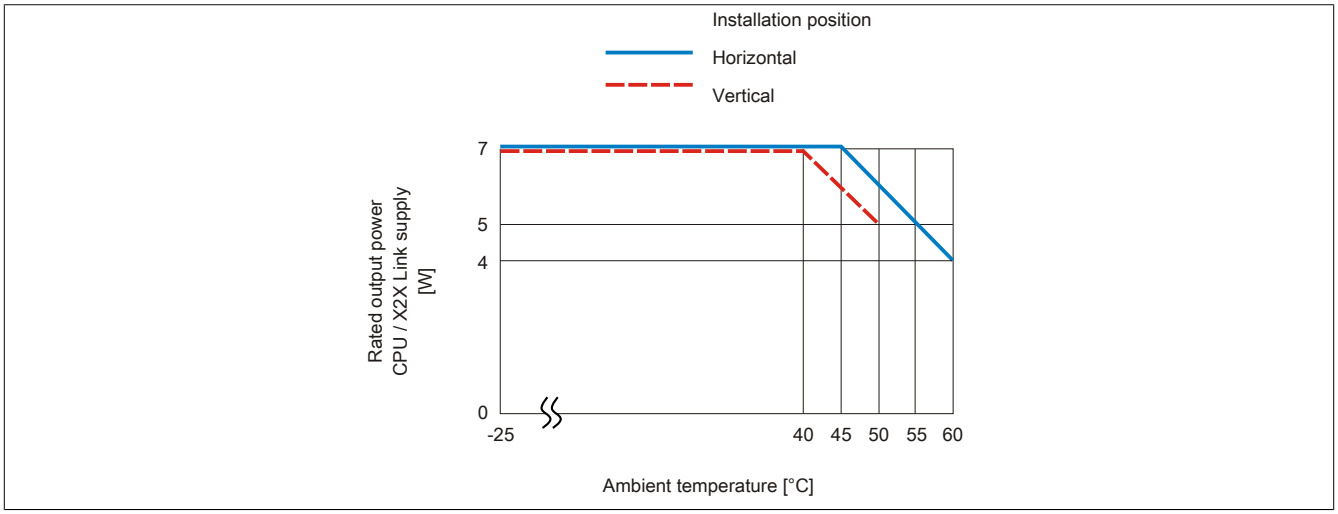


With a supply and jumper



4.10.5.7 Derating for CPU / X2X Link supply

The rated output power for the CPU / X2X Link supply is 7.0W. Derating may be necessary depending on the mounting orientation.



4.10.5.8 Register description

4.10.5.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.10.5.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
4	SupplyVoltage	USINT	•			

4.10.5.8.3 Module status

Name:
Module status

The following module supply voltages are monitored in this register:

Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	A supply voltage of <20.4V is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Bus supply warning - Undervoltage (<4.7V)
1		0	Reserved
2	StatusInput02	0	I/O supply above the warning level of 20.4V
		1	I/O supply below the warning level of 20.4V
3 - x		0	Reserved

4.10.5.8.4 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.10.5.8.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.10.5.8.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.11 Counter modules

Counter modules are used for position detection. Each signal on a counter module is assigned to a status LED.

4.11.1 Brief information

Product ID	Short description	on page
X20CM1941	X20 resolver module, 14-bit resolver input, converter up to 12-bit ABR output	860
X20DC1176	X20 digital counter module, 1 ABR incremental encoder, 5 V 600 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module	867
X20DC1178	X20 digital counter module, 1 SSI absolute encoders, 5 V, 1 Mbit/s, 32-bit, encoder monitoring, NetTime module	883
X20DC1196	X20 digital counter module, 1 ABR incremental encoders, 5 V, 600 kHz input frequency, 4x evaluation	898
X20DC1198	X20 digital counter module, 1 SSI absolute encoder, 5 V, 1 Mbit/s, 32-bit	908
X20DC11A6	X20 digital counter module, 1 ABR incremental encoder, 5 V 5 MHz input frequency, 4x evaluation, encoder monitoring, NetTime module	915
X20DC1376	X20 digital counter module, 1 ABR incremental encoder, 24 V 100 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module	931
X20DC137A	X20 digital counter module, 1x ABR incremental encoder, 24 V (differential), 300 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module	946
X20DC1396	X20 digital counter module, 1 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation	961
X20DC1398	X20 digital counter module, 1 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit	971
X20DC1976	X20 digital counter module, 1x ABR incremental encoder, 5 V (single ended), 250 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module	978
X20DC2190	X20 digital counter module, ultrasonic transducer module, interfaces: EP start/stop, DPI/IP, 2 transducer rods, 4 path evaluation	994
X20DC2395	X20 digital counter module, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function	1008
X20DC2396	X20 digital counter module, 2 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation	1048
X20DC2398	X20 digital counter module, 2 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit	1059
X20DC4395	X20 digital counter module, 2 SSI absolute encoder, 24 V, 2 ABR incremental encoder, 24 V, 4 AB incremental encoders, 24 V, 8 event counters or 4 PWM, local time measurement function	1066
X20cDC1198	X20 digital counter module, coated, 1 SSI absolute encoders, 5 V, 1 Mbit/s, 32-bit	908
X20cDC1396	X20 digital counter module, coated, 1 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation	961
X20cDC2395	X20 digital counter module, coated, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function	1008

4.11.2 X20CM1941

4.11.2.1 General information

The module is equipped with a resolver input and a configurable ABR output.

- Resolver input (differential), with angular position and cyclic counter
- 14-bit resolution for the angular position
- ABR output (configurable)

4.11.2.2 Order data

Model number	Short description	Figure
	Counter functions	
X20CM1941	X20 resolver module, 14-bit resolver input, converter up to 12-bit ABR output	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 170: X20CM1941 - Order data

4.11.2.3 Technical data

Product ID	X20CM1941
Short description	
I/O module	1 resolver input, 1 ABR output
General information	
B&R ID code	0x1E85
Status indicators	Input, output, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Resolver input (OK, open line)	Yes, using status LED and software
Resolver input (counter direction)	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Input/Output - Bus	Yes
Input/Output - I/O supply	No
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Resolver inputs	
Resolver transformation ratio	0.5 (±10%)
Reference output	
Output voltage	3.4 V_{eff}
Output current	Max. 50 mA_{eff}
Frequency	10 kHz
Type	Differential
Angular position resolution	14-bit
Short circuit protection (reference output)	Yes
Input impedance	10.4 kΩ - j 11.1 kΩ
Resolver type	BRX BRT with limitations

Table 171: X20CM1941 - Technical data

Product ID	X20CM1941
ABR output	
Encoder signal	RS422
Type	ABR differential
ABR output (starting with firmware version 5)	
8-bit to 12-bit	3500 rpm
ABR output (up to firmware version 4) 2)	
8-bit	Max. 2343 rpm
9-bit	Max. 1171 rpm
10-bit	Max. 585 rpm
Short circuit protection	Yes (reference output)
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 171: X20CM1941 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Configurable

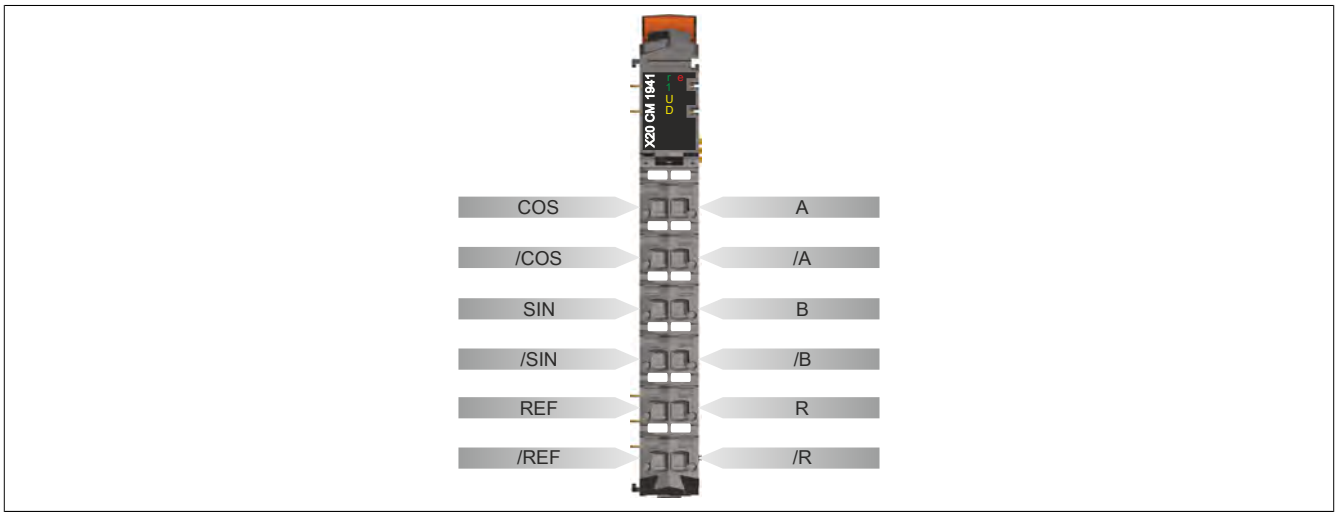
4.11.2.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

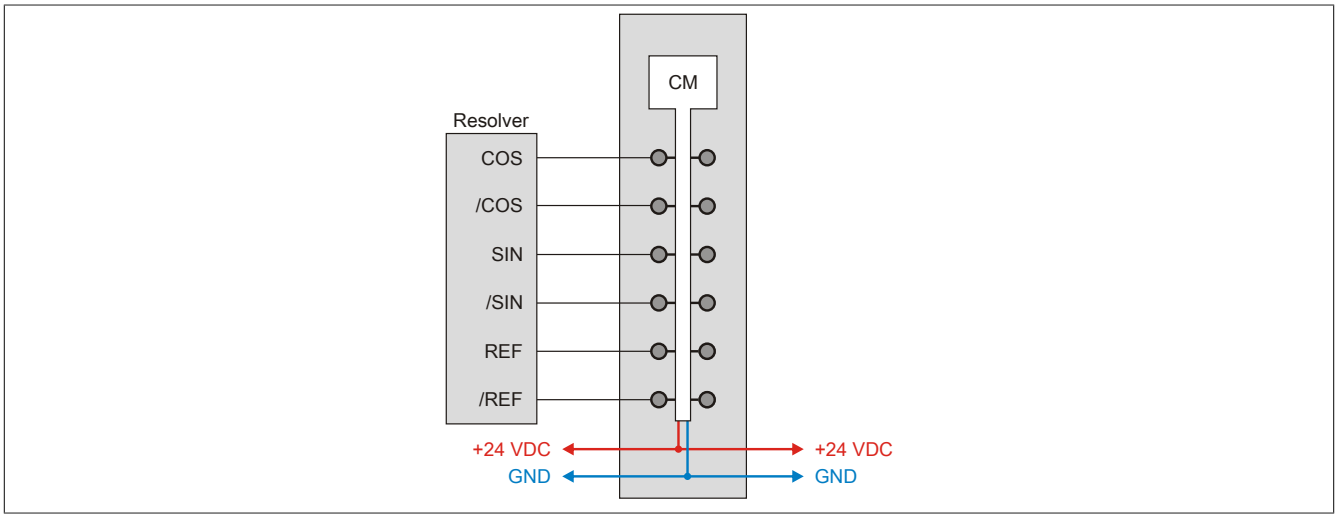
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1	Green	On	Resolver connected and OK
			Off	Open line or no resolver connected
	U	Orange		UP: Counts up
	D	Orange		DOWN: Counts down

1) Depending on the configuration, a firmware update can take up to several minutes.

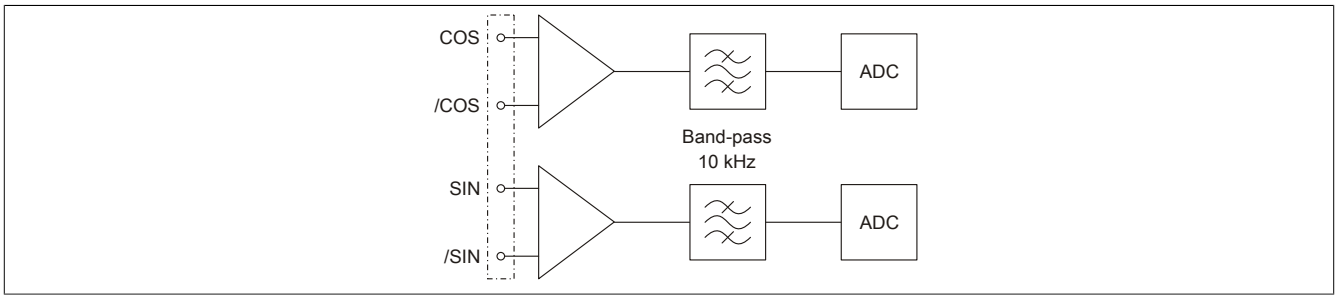
4.11.2.5 Pinout



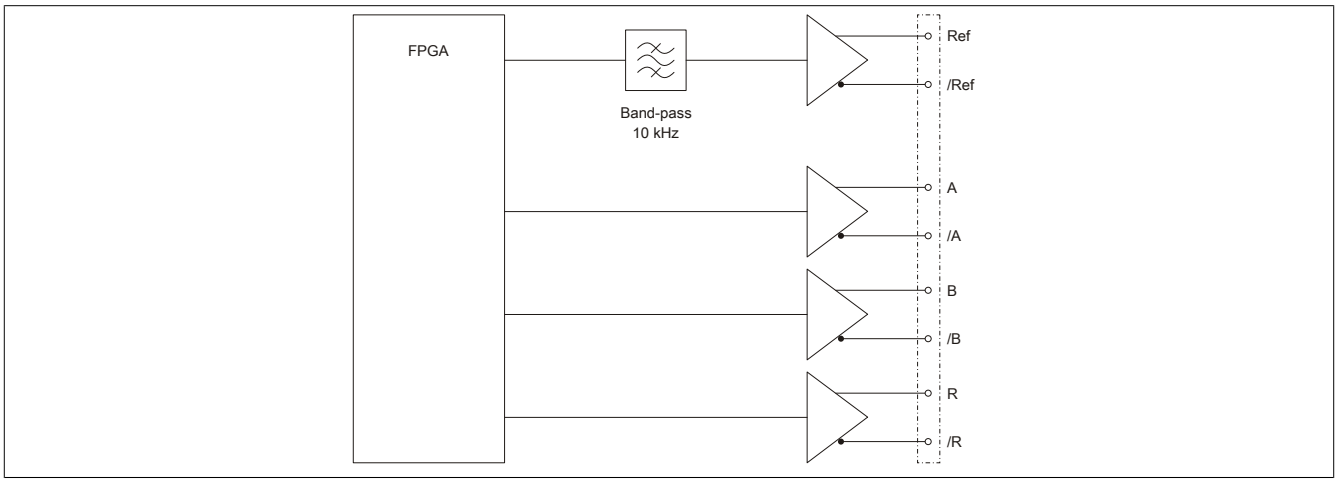
4.11.2.6 Connection example



4.11.2.7 Input circuit diagram



4.11.2.8 Output circuit diagram



4.11.2.9 ABR encoder

Up to firmware version 4

The module measures the resolver's current angular position every 100 µs. The value for A, B or R is generated immediately from the highest value bits (depending on configuration bit 8 to 10).

Firmware version 5 or higher

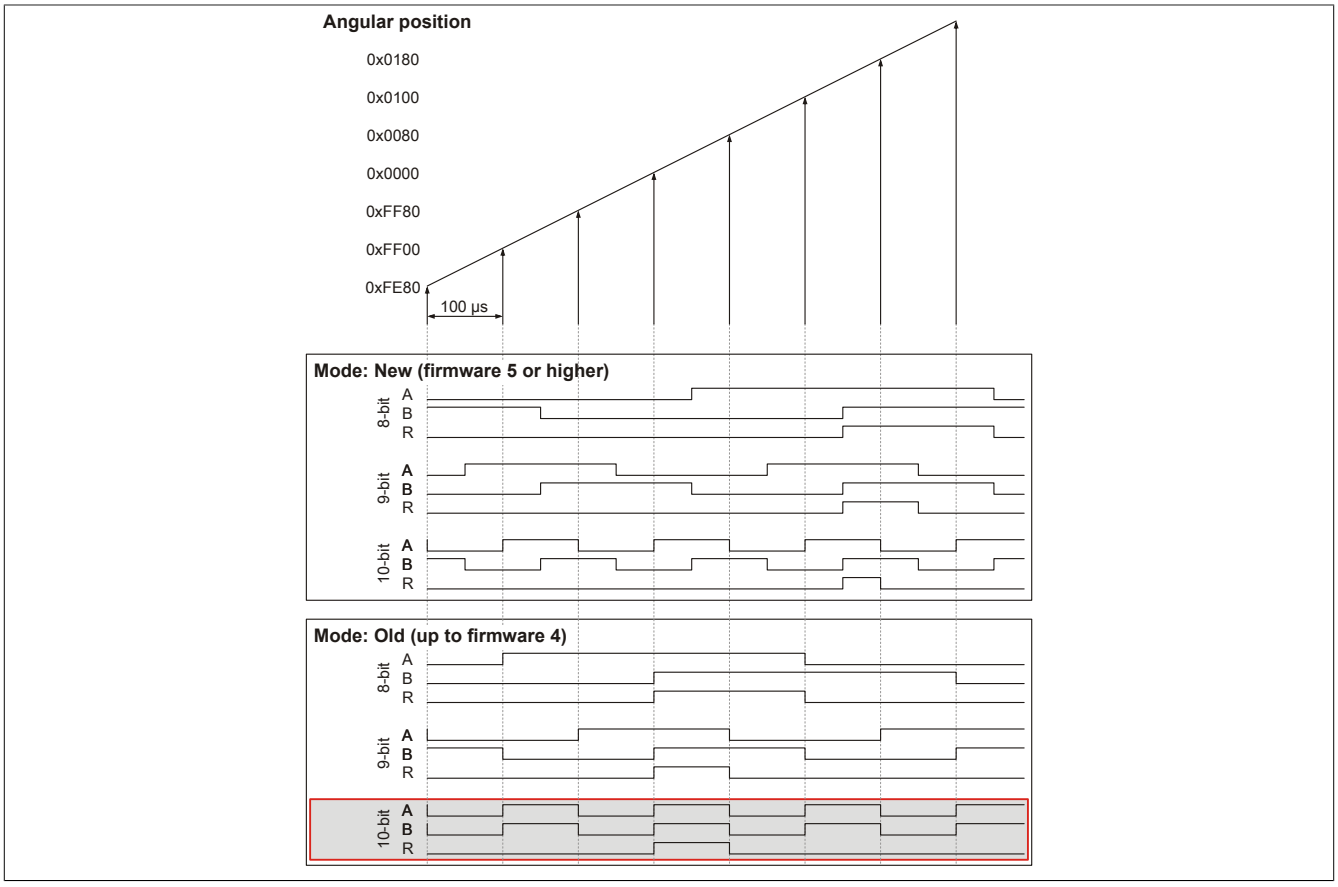
The procedure shown above reaches its limits as soon as more than one LSB difference occurs from one position measurement to the next since only one edge of A or B is possible every 100 µs.

To achieve higher clock rates on the ABR encoder (and therefore higher rotational speeds) while simultaneously improving temporal jitter, the ABR signal is no longer derived directly from the most recent measurement value, but rather generated through interpolation between consecutive position measurements determined every 100 µs.

Information:

In comparison to firmware versions ≤4, the ABR outputs have a constant time offset of 250 µs. See also "Comparison of the timing of the ABR outputs between Firmware version 4 and 5".

Comparison of the timing of the ABR outputs between Firmware version 4 and 5



4.11.2.10 Register description

4.11.2.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.2.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
20	ConfigOutput01	UINT				•
22	ConfigOutput02	USINT				•
Communication						
0	Position	DINT	•			
10	StatusInput	USINT	•			

4.11.2.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
20	-	ConfigOutput01	UINT				•
22	-	ConfigOutput02	USINT				•
Communication							
0	0	Position	DINT	•			
10	4	StatusInput	USINT	•			

1) The offset specifies the position of the register within the CAN object.

4.11.2.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.2.10.4 Set the zero position

Name:
ConfigOutput01

This register can be used to set or move the zero position for the resolver. The zero position/offset specification refers to the current resolver position.

Data type	Value
UINT	0 to 65535

4.11.2.10.5 Encoder emulation configuration

Name:
ConfigOutput02

This register can be used to configure the resolution of the ABR emulation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Number of bits	0	8-bit = 256 increments/rotation
		1	9-bit = 512 increments/rotation
		2	10-bit = 1024 increments/rotation
		3	11-bit = 2048 increments/rotation
		4	12-bit = 4096 increments/rotation
		5 - 7	Not permitted
3 - 7	Reserved	-	

4.11.2.10.6 Current encoder position

Name:
Position

The current angle position of the resolver is shown in this register. The value consists of:

- The two upper bytes, which correspond to the number of rotations counted from -32768 (0x8000xxxx) to +32767 (0x7FFFxxxx)
- The two lower bytes, which correspond to the angle position within the current rotation 1 LSB = 360° / 65536

The position value can, however, be interpreted exactly as an individual 32-bit long angle with resolution 1 / 65536 * 360°.

Data type	Value	Information
DINT	0x0000xxxx to 0xFFFFxxxx	Number of rotations (cyclic)
	0xxxxx0000 to 0xxxxxFFFF	Angle position within the current rotation

Example

0x7FFF0080 corresponds to 32767 rotations, and 128 / 65536 * 360 = 0.703°.

4.11.2.10.7 Connection status

Name:
StatusInput

This register shows a potential open line between the module and the encoder.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Open line	0	No open line
		1	Open line
1- 7	Reserved	-	

4.11.2.10.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.11.2.10.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.11.3 X20DC1176

4.11.3.1 General information

The module is equipped with 1 input for an ABR incremental encoder with 5 V encoder signal. The encoder inputs are monitored (A, B, R, A\, B\, R\).

- 1 ABR incremental encoder 5 V
- Encoder input monitoring
- 2 additional inputs, e.g. for latch input
- 5 VDC, 24 VDC and GND for encoder supply

4.11.3.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1176	X20 digital counter module, 1 ABR incremental encoder, 5 V 600 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 172: X20DC1176 - Order data

4.11.3.3 Technical data

Product ID	X20DC1176
Short description	
I/O module	1 ABR incremental encoder 5 V
General information	
B&R ID code	0xA706
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input voltage	24 VDC (-15 % / +20 %)
Input current at 24 VDC	Approx. 3.3 mA
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input circuit	Sink
Additional functions	Latch input

Table 173: X20DC1176 - Technical data

Product ID	X20DC1176
Input resistance	7.03 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Encoder inputs	5 V, symmetrical
Counter size	16/32-bit
Input frequency	Max. 600 kHz
Evaluation	4x
Encoder supply	
5 VDC	±5%, module-internal, max. 300 mA
24 VDC	Module-internal, max. 300 mA
Input filter	
Hardware	≤400 ns
Software	-
Common-mode range	-10 V ≤ V_{CM} ≤ +13.2 V
Overload behavior of the encoder supply	Short circuit protection, overload protection
Isolation voltage between encoder and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 173: X20DC1176 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.3.4 LED status indicators

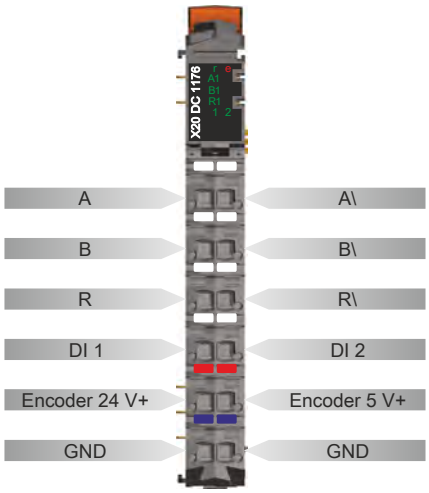
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	The encoder monitor has detected a line fault on the encoder inputs. The status bits must be evaluated in order to provide a more detailed definition of this error. The following error states are detected: • Open line • Short-circuit or voltage level too low
			On	Error or reset status
	A1	Green		Input state of counter input A
	B1	Green		Input state of counter input B
	R1	Green		Input state of reference pulse R
	1 - 2	Green		Input state of the corresponding digital input

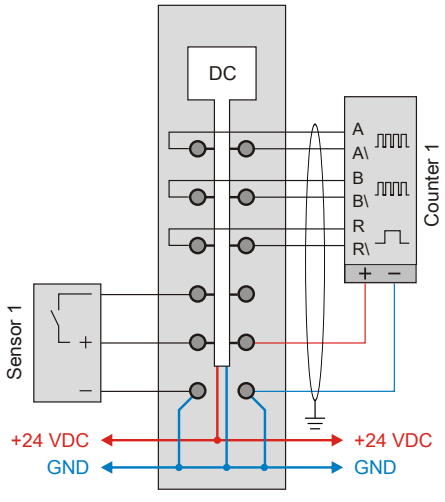
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.3.5 Pinout

Shielded cables must be used for all signal lines.

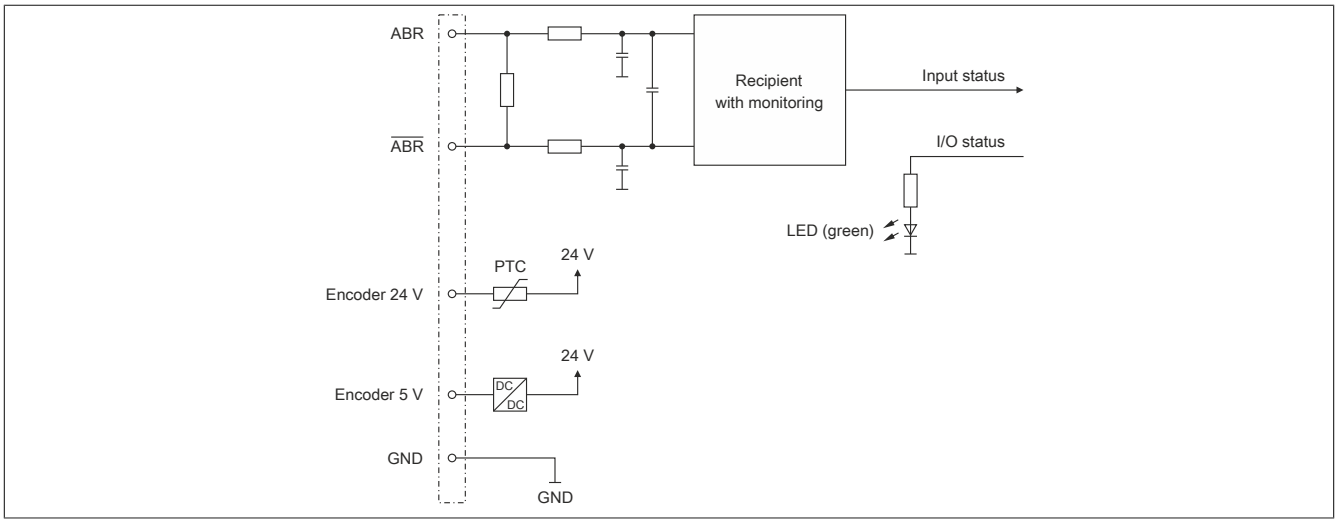


4.11.3.6 Connection example

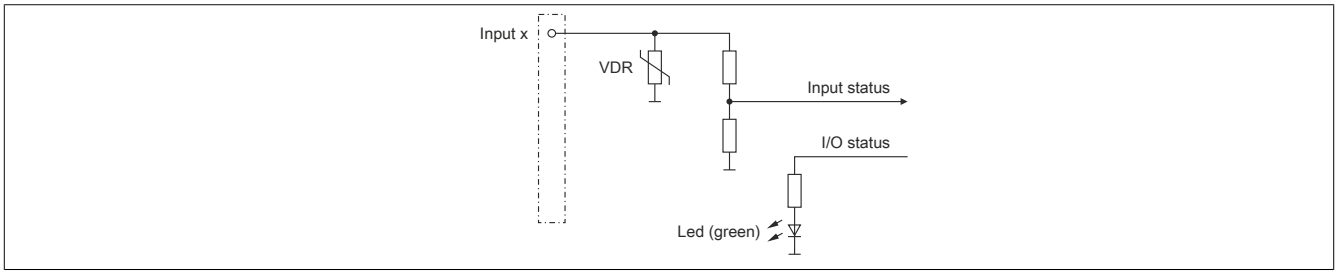


4.11.3.7 Input circuit diagram

Counter inputs



Standard inputs



4.11.3.8 Register description

4.11.3.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.3.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication						
683	SDCLifeCount	SINT	•			
6342	Encoder01	INT	•			
6340		DINT				
6310	Encoder01TimeValid	INT	•			
6308		DINT				
6358	Encoder01Latch	INT	•			
6356		DINT				
6153	Encoder commands	USINT			•	
	Encoder01Reset	Bit 0				
	Encoder01LatchEnable	Bit 1				
927	Input status of signal lines	USINT	•			
	Encoder01_A	Bit 0				
	Encoder01_B	Bit 1				
	Encoder01_R	Bit 2				
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
847	Status of signal lines	USINT	•			
	BW_Channel_A	Bit 0				
	BW_Channel_B	Bit 1				
	BW_Channel_R	Bit 2				
811	Acknowledging error status of signal lines	USINT			•	
	BW_QuitChannel_A	Bit 0				
	BW_QuitChannel_B	Bit 1				
	BW_QuitChannel_R	Bit 2				
6326	Encoder01TimeChanged	INT	•			
6324		DINT				
6303	Encoder01LatchCount	SINT	•			
843	Status of encoder supplies	USINT	•			
	PowerSupply01	Bit 0				
	PowerSupply02	Bit 1				
Encoder - Configuration						
513	CfO_SIframeGenID	USINT				•
642	CfO_SystemCycleTime	UINT				•
769	CfO_PhyIOConfigCh01	USINT				•
771	CfO_PhyIOConfigCh02	USINT				•
773	CfO_PhyIOConfigCh03	USINT				•
777	CfO_PhyIOConfigCh04	USINT				•
779	CfO_PhyIOConfigCh05	USINT				•
815	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	CfO_BWQuitTime_0	UDINT				•
6145	CfO_CounterCycleSelect	USINT				•
6147	CfO_CounterMode	USINT				•
6149	CfO_LatchMode	USINT				•
6151	CfO_LatchComparator	USINT				•
6159	CfO_BWCNTEnableMaskChannel7_0	USINT				•

4.11.3.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication							
6342	0	Encoder01	INT	•			
6310	2	Encoder01TimeValid	INT	•			
6358	4	Encoder01Latch	INT	•			
6153	1	Encoder commands	USINT			•	
		Encoder01Reset	Bit 0				
		Encoder01LatchEnable	Bit 1				
927	7	Input status of signal lines	USINT	•			
		Encoder01_A	Bit 0				
		Encoder01_B	Bit 1				
		Encoder01_R	Bit 2				
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
847	6	Status of signal lines	USINT	•			
		BW_Channel_A	Bit 0				
		BW_Channel_B	Bit 1				
		BW_Channel_R	Bit 2				
811	0	Acknowledging error status of signal lines	USINT			•	
		BW_QuitChannel_A	Bit 0				
		BW_QuitChannel_B	Bit 1				
		BW_QuitChannel_R	Bit 2				
6326	-	Encoder01TimeChanged	INT		•		
6303	-	Encoder01LatchCount	SINT		•		
843	-	Status of encoder supplies	USINT		•		
		PowerSupply01	Bit 0				
		PowerSupply02	Bit 1				
Encoder - Configuration							
513	-	CfO_SIframeGenID	USINT				•
642	-	CfO_SystemCycleTime	UINT				•
769	-	CfO_PhyIOConfigCh01	USINT				•
771	-	CfO_PhyIOConfigCh02	USINT				•
773	-	CfO_PhyIOConfigCh03	USINT				•
777	-	CfO_PhyIOConfigCh04	USINT				•
779	-	CfO_PhyIOConfigCh05	USINT				•
815	-	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	-	CfO_BWQuitTime_0	UDINT				•
6145	-	CfO_CounterCycleSelect	USINT				•
6147	-	CfO_CounterMode	USINT				•
6149	-	CfO_LatchMode	USINT				•
6151	-	CfO_LatchComparator	USINT				•
6159	-	CfO_BWCNTEnableMaskChannel7_0	USINT				•

1) The offset specifies the position of the register within the CAN object.

4.11.3.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.3.8.4 Encoder - Configuration

The following registers are used for setting functions and configuring the module.

4.11.3.8.4.1 Enabling error monitoring for the signal lines

Name:
CfO_BWCNTEnableMaskChannel7_0

This register requires individually enabling error monitoring for each of the signal channels. "Open line", "short circuit" and "voltage level too low" are reported as error states. Any errors that occur are reported in the error status registers BW_Channel_x.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Enable error monitoring for signal A lines	0	Error monitoring - Encoder Signal A disabled
		1	Error monitoring - Encoder Signal A enabled - Only default in bus controller function model
1	Enable error monitoring for signal B lines	0	Error monitoring - Encoder Signal B disabled
		1	Error monitoring - Encoder Signal B enabled - Only default in bus controller function model
2	Enable error monitoring for signal R lines	0	Error monitoring - Encoder Signal R disabled
		1	Error monitoring - Encoder Signal R enabled - Only default in bus controller function model
3 - 7	Reserved	0	

4.11.3.8.4.2 Timing for automatic error acknowledgment

Name:
CfO_BWQuitTime_0

This register can be used to enable an additional automatic acknowledgment of the error status through timing. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Data type	Value	Information
UDINT	0	No automatic acknowledgment - Only default in bus controller function model
	1 to 2.147.483.647	Time for automatic acknowledgment [µs]

4.11.3.8.4.3 Setting the latch mode

Name:
CfO_LatchMode

This register is used to set the latch mode:

- Single shot latch mode:
  The latch function must be enabled/set. After a successful latch procedure, the activation must be reset in order for a new latch procedure to be activated.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired.

A changed counter state on Encoder01LatchCount indicates that the latch procedure has been performed. The counter value is stored in the latch register Encoder01Latch.

Data type	Value	Information
USINT	0	Single shot latch procedure
	1	Continuous latch procedure

4.11.3.8.4.4 Signal channels for triggering latch procedure

Name:
CfO_LatchComparator

This register defines the signal channels and their level for triggering the latch procedure.

- This mainly configures which channels are linked to generate the latch event. All three signals from the encoder and digital input 1 can be used for the "AND" operation.
- The "active voltage level" needed for the latch procedure can now be used according to the physical signals.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Defines signal level for encoder signal A	0	Low
		1	High
1	Defines signal level for encoder signal B	0	Low
		1	High
2	Defines signal level for encoder signal R	0	Low
		1	High
3	Defines signal level for digital input 1	0	Low
		1	High
4	Use encoder signal A to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal A
5	Use encoder signal B to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal B
6	Use encoder signal R to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal R
7	Use digital input 1 to trigger latch procedure	0	Disabled
		1	Latch function linked to digital input 1

4.11.3.8.4.5 Physical configuration

The following registers must be set to the specified constant value for correct physical configuration:

Constant register "CfO_SIframeGenID"

Name:
CfO_SIframeGenID

Data type	Value	Information
USINT	9	Only default in the bus controller module

Constant register "CfO_SystemCycleTime"

Name:
CfO_SystemCycleTime

Cycle time of encoder acquisition in 1/8 µs steps. 1 encoder value is acquired as the counter value per cycle.

Data type	Value	Information
UINT	800	800 = 100 µs; only default in the bus controller module

Constant register "CfO_PhyIOConfigCh01"

Name:
CfO_PhyIOConfigCh01

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh02"

Name:
CfO_PhyIOConfigCh02

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh03"

Name:
CfO_PhyIOConfigCh03

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh04"

Name:
CfO_PhyIOConfigCh04

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh05"

Name:
CfO_PhyIOConfigCh05

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_BWQuitTimeSelChannel7_0"

Name:
CfO_BWQuitTimeSelChannel7_0

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_CounterCycleSelect"

Name:
CfO_CounterCycleSelect

Data type	Value	Information
USINT	2	Only default in the bus controller module

Constant register "CfO_CounterMode"

Name:
CfO_CounterMode

Data type	Value	Information
USINT	3	Only default in the bus controller module

4.11.3.8.5 Encoder - Communication

4.11.3.8.5.1 Counter for verifying the data frame

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.11.3.8.5.2 Display of the counter state

Name:
Encoder01

The counter state of the incremental encoder is displayed as a 16 or 32-bit counter value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.3.8.5.3 Net time of the last valid counter value

Name:
Encoder01TimeValid

The net time of the last valid counter value is the time of the last valid counter value (see "Cfo_SystemCycleTime" register) recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The net time of the last valid counter value that was read is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in milliseconds.
DINT[1)]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

4.11.3.8.5.4 Net time of the last counter value change

Name:
Encoder01TimeChanged

For slow X2X Link cycles, the net time of the last counter value change can be used to more accurately determine the speed.

The net time of the last counter value change is displayed as 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µsec.
DINT[1)]	-2.147.483.648 bis 2.147.483.647	

1) Can only be configured in the standard function model

4.11.3.8.5.5 Counter value at the time of the last latch

Name:
Encoder01Latch

The counter value at the time of the last latch is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.3.8.5.6 Counter value of latch event

Name:
Encoder01LatchCount

The latch events are counted and stored in a cyclic 8-bit counter. This counter is incremented with each latch event, thereby indicating a new occurrence. The new latched counter value is stored in the respective latch register.

Data type	Value
SINT	-128 to 127

4.11.3.8.5.7 Encoder commands

Name:
Encoder01Command

This register can be used to

1 reset the counter value. The counter is kept at zero until this command is reset.
2 enable the latch procedure. If the latch configuration is valid and matches the hardware signals, then this activation causes the counter value to be saved in the latch register.

The two different latch configurations that are possible (see section 4.11.3.8.4.3 "Setting the latch mode") must be handled as follows:

- Single shot latch mode:
  After successful latching, indicated by the latch event counter, activation must be reset before any more latching is possible. The activation must be set again if additional latching is needed.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired. The latch event counter is incremented with each event.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01Reset	0	Do not reset
		1	Set encoder value to 0
1	Encoder01LatchEnable	0	Do not activate latch
		1	Latching
2 - 7	Reserved	0	

4.11.3.8.5.8 Input status of signal lines

Name:
Encoder01_A
Encoder01_B
Encoder01_R
DigitalInput01 to DigitalInput02

This register displays the input status of the signal lines from the encoder and the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01_A	0/1	Input state of encoder signal A
1	Encoder01_B	0/1	Input state of encoder signal B
2	Encoder01_R	0/1	Input state of encoder signal R
3	Reserved	0	
4	DigitalInput01	0/1	Input state - Digital input 1
5	DigitalInput02	0/1	Input state - Digital input 2
6 - 7	Reserved	0	

4.11.3.8.5.9 Error status of signal lines

The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Status of signal lines

Name:
BW_Channel_A
BW_Channel_B
BW_Channel_R

This register displays the error states of the signal lines from the encoder. The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_Channel_A	0	No error in encoder signal A
		1	Open line, short circuit or voltage level too low
1	BW_Channel_B	0	No error in encoder signal B
		1	Open line, short circuit or voltage level too low
2	BW_Channel_R	0	No error in encoder signal R
		1	Open line, short circuit or voltage level too low
3 - 7	Reserved	0	

Acknowledging error status of signal lines

Name:
BW_QuitChannel_A
BW_QuitChannel_B
BW_QuitChannel_R

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_QuitChannel_A	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal A
1	BW_QuitChannel_B	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal B
2	BW_QuitChannel_R	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal R
3 - 7	Reserved	0	

Manual acknowledgment of latched error states

The latched error states of the signal lines from the encoder can be acknowledged manually. However, if there are still pending errors remaining, then the error status remains active. After successfully acknowledging the errors (latched error status = 0), the acknowledge bits must still be reset by the user or else a re-occurrence of an error could be overlooked by the user.

Example 1: **Cause of error corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user after the cause of error has been corrected. The latched error status changes to zero.

The manual acknowledge must now be reset so that any new errors will be recognized by the user.

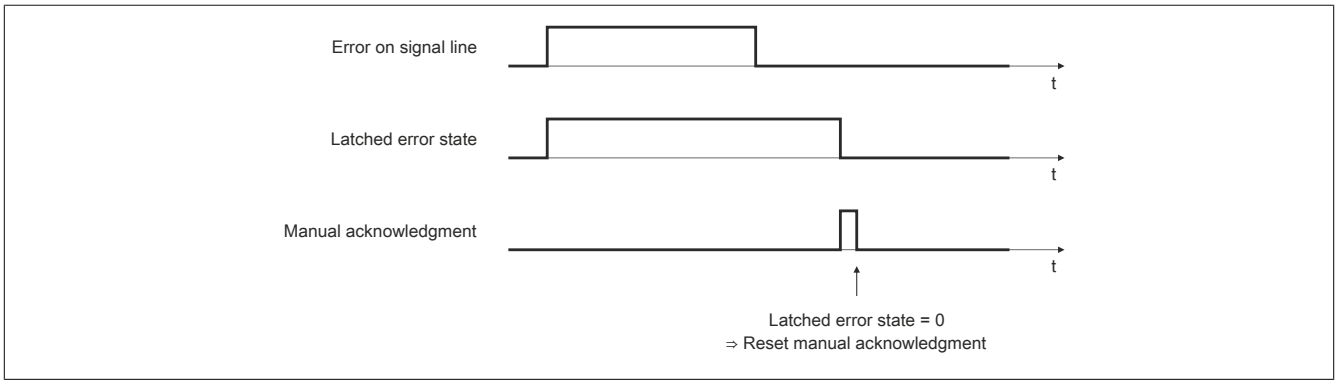


Figure 171: Cause of error corrected before being acknowledged

Example 2: **Cause of error not yet corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user before the cause of error has been corrected. The latched error status remains set because the error is still remaining.

Acknowledgment is only successful after the cause of error has been corrected. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

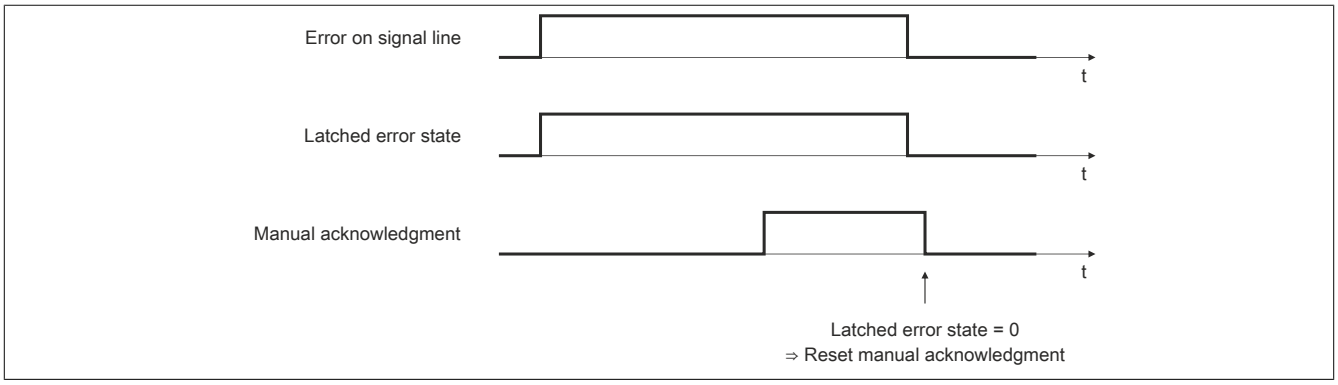


Figure 172: Cause of error not yet corrected before being acknowledged

Automatic acknowledgment of latched error states

In addition to manual acknowledgment, automatic acknowledgment of the latched error states after a specified amount of time can also be enabled. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages and for the validity of the counter value to be determined using its age.

If the time specification = 0, then only manual acknowledgment is possible.

Example 1: An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged as soon as the time expires. The latched error status changes to zero.

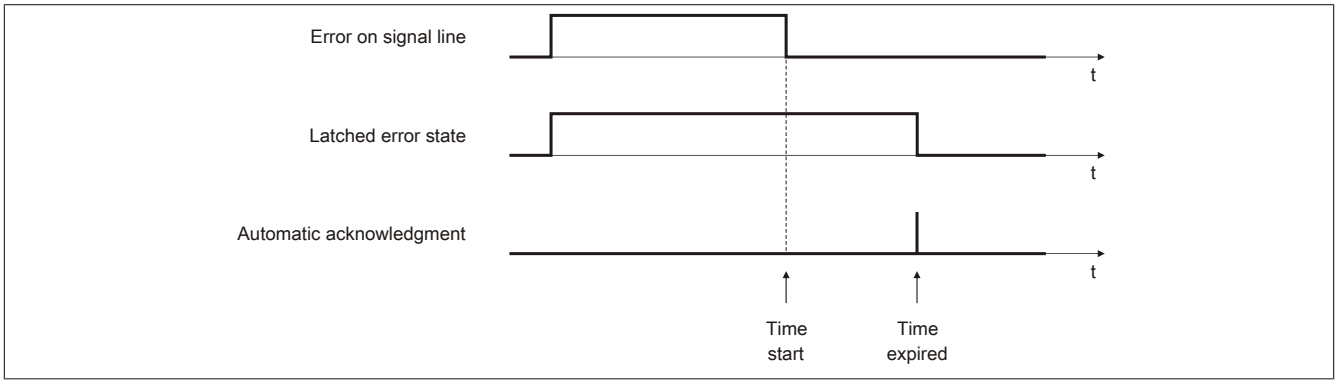


Figure 173: Latched error state acknowledged automatically

Example 2: Automatic and manual acknowledge used

An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged manually by the user before the time expires. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

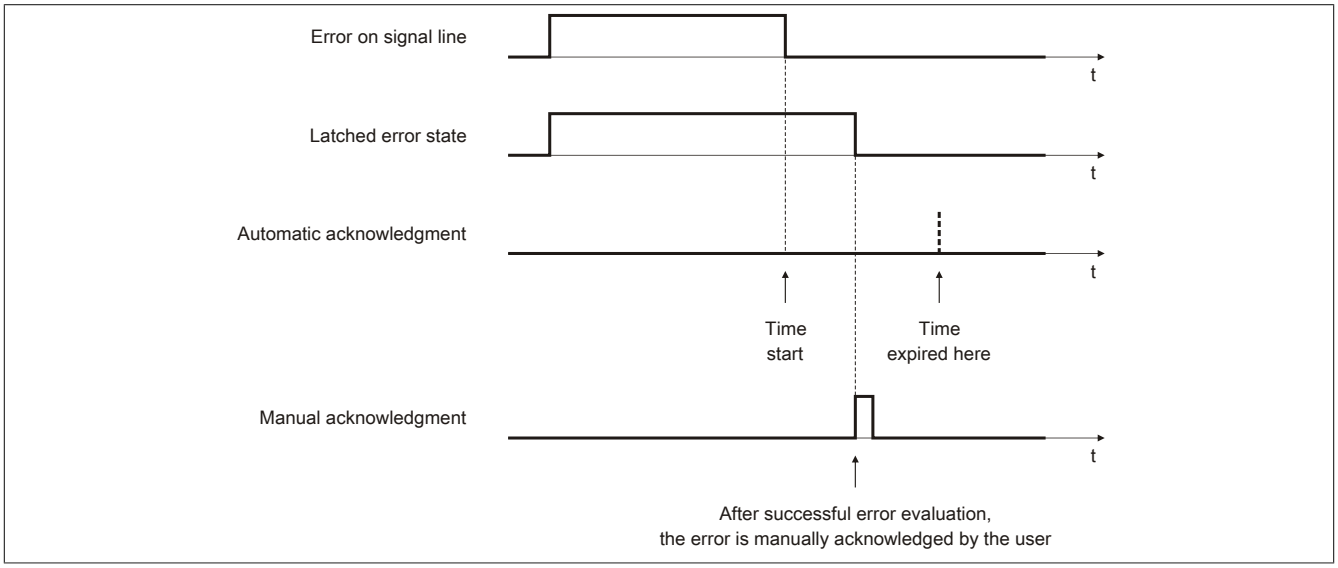


Figure 174: Automatic and manual acknowledge used

4.11.3.8.5.10 Status of encoder supplies

Name:
PowerSupply01 to PowerSupply02

This register shows the status of the integrated encoder supplies. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1	PowerSupply02	0	5 VDC encoder power supply OK
		1	5 VDC encoder power supply faulty
2 - 7	Reserved	-	

4.11.3.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.11.3.8.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
150 µs

4.11.4 X20DC1178

4.11.4.1 General information

This module is equipped with one input for SSI absolute encoders with 5 V encoder signal. The data signal is monitored (Data, Data\).

- 1 SSI absolute encoder 5 V
- Monitoring the data signal
- 2 additional inputs
- 5 VDC, 24 VDC and GND for encoder supply

4.11.4.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1178	X20 digital counter module, 1 SSI absolute encoders, 5 V, 1 Mbit/s, 32-bit, encoder monitoring, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 174: X20DC1178 - Order data

4.11.4.3 Technical data

Product ID	X20DC1178
Short description	
I/O module	1 SSI absolute encoder 5 V
General information	
B&R ID code	0xA708
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input voltage	24 VDC (-15% / +20%)
Input current at 24 VDC	Approx. 3.3 mA
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input circuit	Sink
Input resistance	7.03 kΩ

Table 175: X20DC1178 - Technical data

Product ID	X20DC1178
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
SSI absolute encoder	
Counter size	Encoder-dependent up to 32-bit
Max. transfer rate	1 Mbit/s
Keying	Gray/Binary
Encoder signal	5 V, symmetrical
Isolation voltage between encoder and bus	500 V_{eff}
Overload behavior of the encoder supply	Short circuit protection, overload protection
Transfer rate	125 kbit/s / 250 kbit/s / 500 kbit/s / 1 Mbit/s
Encoder supply	
5 VDC	±5%, module-internal, max. 300 mA
24 VDC	Module-internal, max. 300 mA
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 175: X20DC1178 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.4.4 LED status indicators

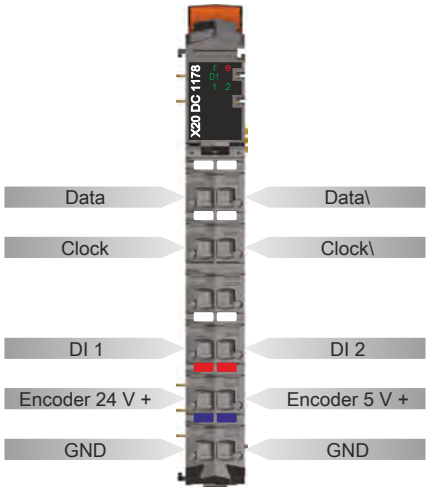
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Either the encoder monitor has detected a line fault on the encoder inputs or a transfer error has occurred. The status bits must be evaluated in order to provide a more detailed definition of this error. The following error states are detected: • Open line • Short-circuit or voltage level too low • SSI cycle time violation • Parity error
			On	Error or reset status
	D1	Green		Input status - Data signal
	1 - 2	Green		Input state of the corresponding digital input

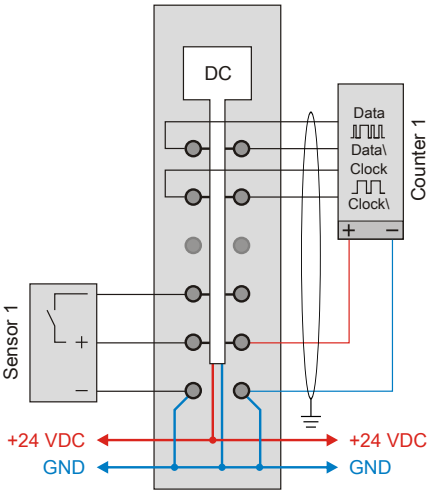
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.4.5 Pinout

Shielded cables must be used for all signal lines.

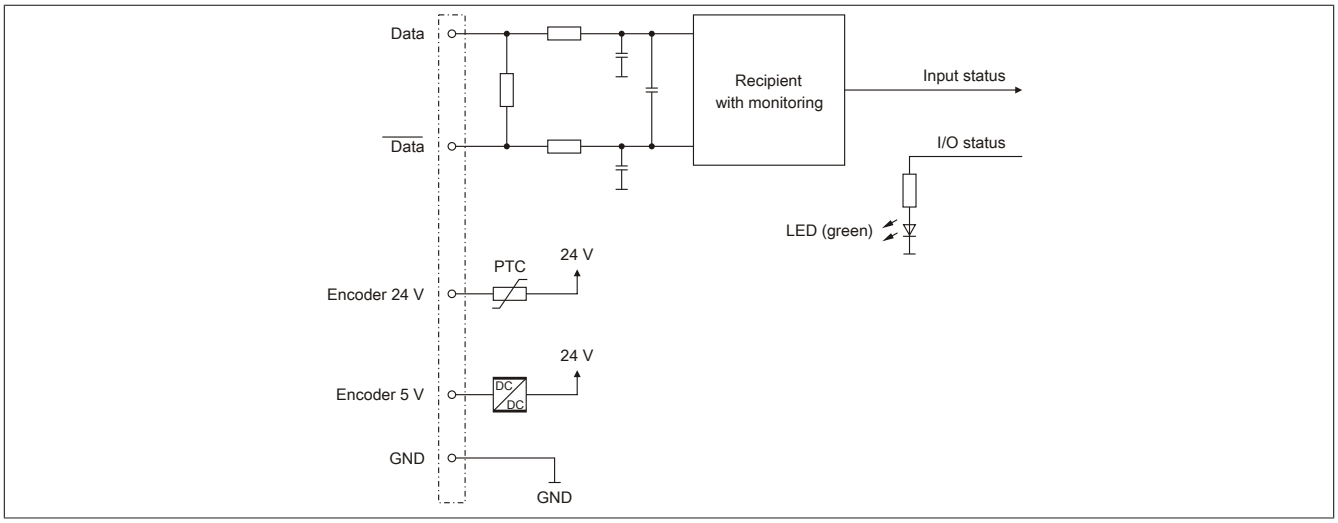


4.11.4.6 Connection example

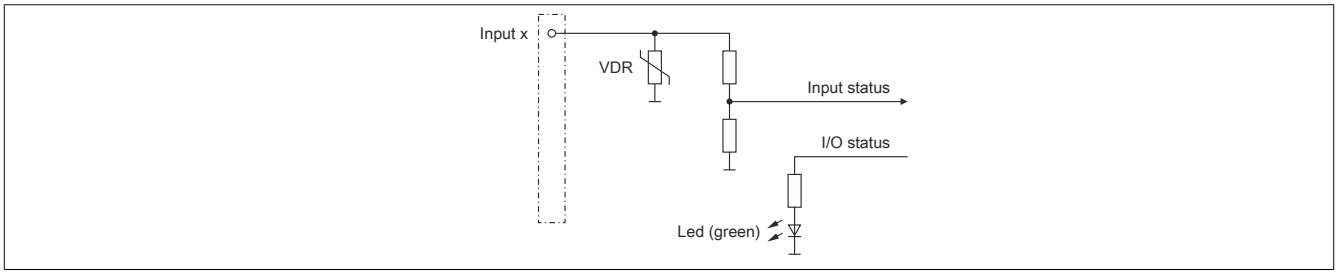


4.11.4.7 Input circuit diagram

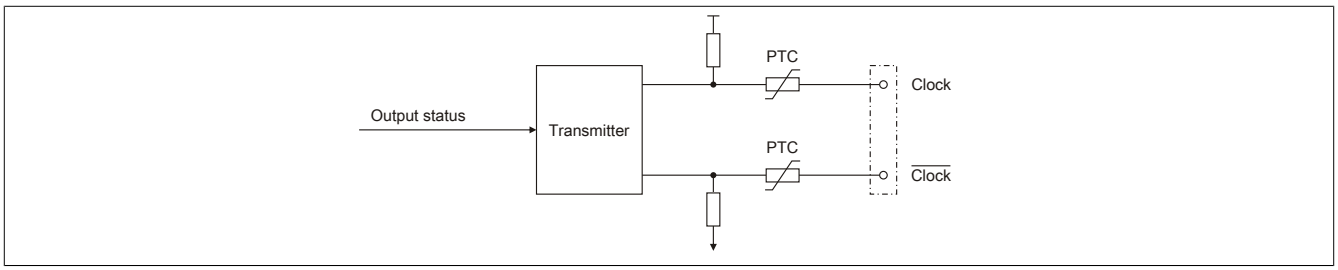
Counter input



Standard inputs



4.11.4.8 Output circuit diagram



4.11.4.9 Register description

4.11.4.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.4.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
650	CfO_SystemCyclePrescaler	UINT				•
2049	CfO_CycleSelect	USINT				•
2951	CfO_PhysicalMode	USINT				•
2053	CfO_DataBits	USINT				•
2055	CfO_NullBits	USINT				•
820	CfO_BWQuitTime_0	UDINT				•
815	CfO_BWQuitTimeSelChannel7_0	USINT				•
2059	CfO_BWSSIEnableMaskChannel7_0	USINT				•
Communication						
683	SDCLifeCount	SINT	•			
927	Input status of signal lines	USINT	•			
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
2100	Encoder01	(U)DINT	•			
2102	Encoder01	UINT	•			
2086	Encoder01TimeValid	INT	•			
2084	Encoder01TimeValid	DINT	•			
2094	Encoder01TimeChanged	INT	•			
2092	Encoder01TimeChanged	DINT	•			
259	State of the encoder	USINT	•			
	EncoderCycleTimeViolation	Bit 0				
	EncoderDataError	Bit 1				
323	Acknowledging error status of the encoder	USINT			•	
	EncoderQuitCycleTimeViolation	Bit 0				
	EncoderQuitDataError	Bit 1				
847	Status of signal lines	USINT	•			
	BW_Channel_D	Bit 0				
811	Acknowledging error status of the signal line	USINT			•	
	BW_QuitChannel_D	Bit 0				
843	Status of encoder supplies	USINT	•			
	PowerSupply01	Bit 0				
	PowerSupply02	Bit 1				

4.11.4.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
650	-	CfO_SystemCyclePrescaler	UINT				●
2049	-	CfO_CycleSelect	USINT				●
2951	-	CfO_PhysicalMode	USINT				●
2053	-	CfO_DataBits	USINT				●
2055	-	CfO_NullBits	USINT				●
820	-	CfO_BWQuitTime_0	UDINT				●
815	-	CfO_BWQuitTimeSelChannel7_0	USINT				●
2059	-	CfO_BWSSIEnableMaskChannel7_0	USINT				●
Communication							
683		SDCLifeCount	SINT	●			
927	7	Input status of signal lines	USINT	●			
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
2100	-	Encoder01	(U)DINT	●			
2086	4	Encoder01TimeValid	INT	●			
2094	-	Encoder01TimeChanged	INT	●			
259	-	State of the encoder	USINT	●			
		EncoderCycleTimeViolation	Bit 0				
		EncoderDataError	Bit 1				
323	-	Acknowledging error status of the encoder	USINT			●	
		EncoderQuitCycleTimeViolation	Bit 0				
		EncoderQuitDataError	Bit 1				
847	6	Status of signal lines	USINT	●			
		BW_Channel_D	Bit 0				
811	0	Acknowledging error status of the signal line	USINT			●	
		BW_QuitChannel_D	Bit 0				
843	-	Status of encoder supplies	USINT	●			
		PowerSupply01	Bit 0				
		PowerSupply02	Bit 1				

1) The offset specifies the position of the register within the CAN object.

4.11.4.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.4.9.4 Encoder - Configuration

The following registers are used for setting functions and configuring the module.

4.11.4.9.4.1 Setting the SSI sampling cycle time

The following two registers define the cycle time for SSI sampling.

Setting the interrupt

Name:

CfO_CycleSelect

This register assigns the principle interrupt setting:

- **Timer configuration (time setting with CfO_SystemCyclePrescaler register):** The SSI transfer can be started independently of the X2X cycle. The timer is synchronized with X2X Link.
- **AOAI:** Configuration with X2X interrupt, one-time start of the SSI transfer in the X2X cycle. The SSI transfer may require an entire X2X cycle.
- **SOSI:** Configuration with X2X interrupt, one-time start of the SSI transfer in the X2X cycle. The reaction time can be optimized with this setting if the SSI transfer doesn't exceed half of an X2X cycle.

Data type	Value	Filter
USINT	3	Timer [µsec] ... Time setting with register CfO_SystemCyclePrescaler
	10	AOAI
	14	SOSI

Setting the cycle time

Name:

CfO_SystemCyclePrescaler

The desired cycle time must be configured additionally for the timer setting using this register.

Data type	Value	Filter
USINT	1	50 µs
	2	100 µs
	4	200 µs
	8	400 µs
	16	800 µs
	0	All other settings in the CfO_CycleSelect register

4.11.4.9.4.2 Setting operating parameters

Name:
CfO_PhysicalMode

This register defines the operating parameters for the SSI encoder to correctly evaluate the data from the encoder.

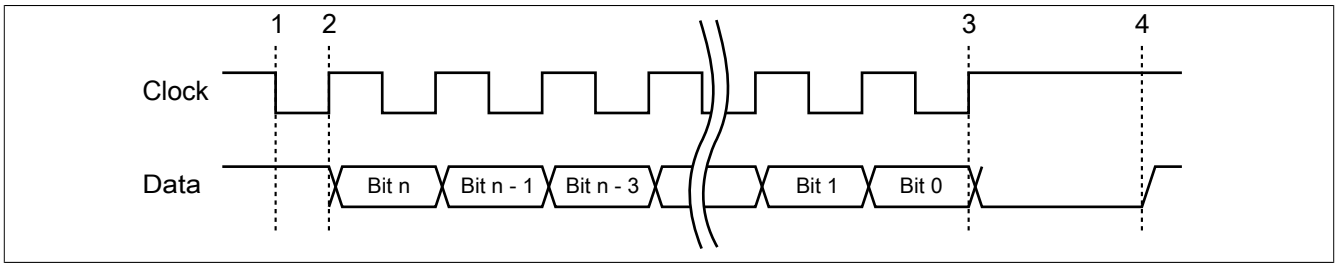
- **Parity:** Data with or without parity; an error is reported if there is an even or uneven parity mismatch.
- **Monoflop check:** The encoder uses the monoflop to signal the readiness to accept a new clock cycle.
- **Data coding:** Binary or gray coding of the data bits
- **Clock rate:** Speed of data transfer

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Parity bit	00	No parity bit (no clock bit output)
		01	Even parity bit
		10	Uneven parity bit
		11	Ignore parity bit (clock bit is output, but the result is ignored)
2 - 3	Monostable multivibrator testing	00	No monostable multivibrator check (no clock bit output)
		01	Check - Low level
		10	Check - High level
		11	Check - Ignore level (clock bit is output, but the result is ignored)
4	Data coding	0	Binary coding
		1	Gray coding
5	Reserved	0	
6 - 7	Clock rate	00	1 MHz
		01	500 kHz
		10	250 kHz
		11	125 kHz

Transfer to synchronous serial interface



Measurement value processing

1 Starting bit ... Stores the measurement value
2 Output of first data bit
3 All data bits are transferred, monostable multivibrator time starts counting down.
4 Monostable multivibrator returns to its initial state. A new transfer can be started.

4.11.4.9.4.3 Number of data bits

Name:

Cfo_DataBits

This register can be used to define the number of SSI encoder data bits.

Data type	Value	Filter
USINT	1 to 32	Number of SSI data bits

4.11.4.9.4.4 Leading zeros of the encoder

Name:

Cfo_NullBits

This register can be used to define the number of SSI encoder leading zeros.

Data type	Value	Filter
USINT	1 to 32	Number of leading zeros

4.11.4.9.4.5 Timing for automatic error acknowledgment

Name:
CfO_BWQuitTime_0

This register can be used to enable an additional automatic acknowledgment of the error status through timing. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Data type	Value	Information
UDINT	0	No automatic acknowledgment - Only default in bus controller function model
	1 to 2.147.483.647	Time for automatic acknowledgment [µs]

Automatic acknowledgment of latched error states

In addition to manual acknowledgment, automatic acknowledgment of the latched error states after a specified amount of time can also be enabled. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages and for the validity of the counter value to be determined using its age.

If the time specification = 0, then only manual acknowledgment is possible.

Example 1: An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged as soon as the time expires. The latched error status changes to zero.

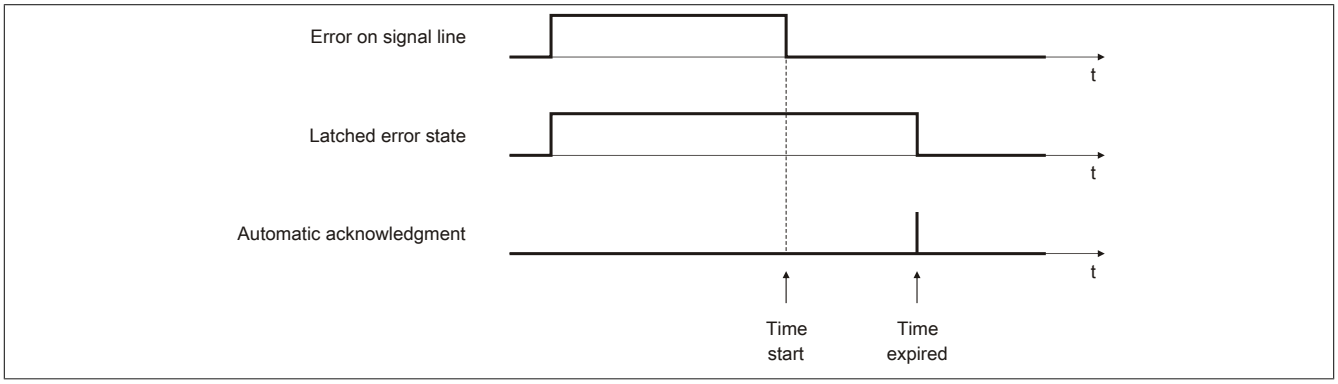


Figure 175: Latched error state acknowledged automatically

Example 2: Automatic and manual acknowledge used

An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged manually by the user before the time expires. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

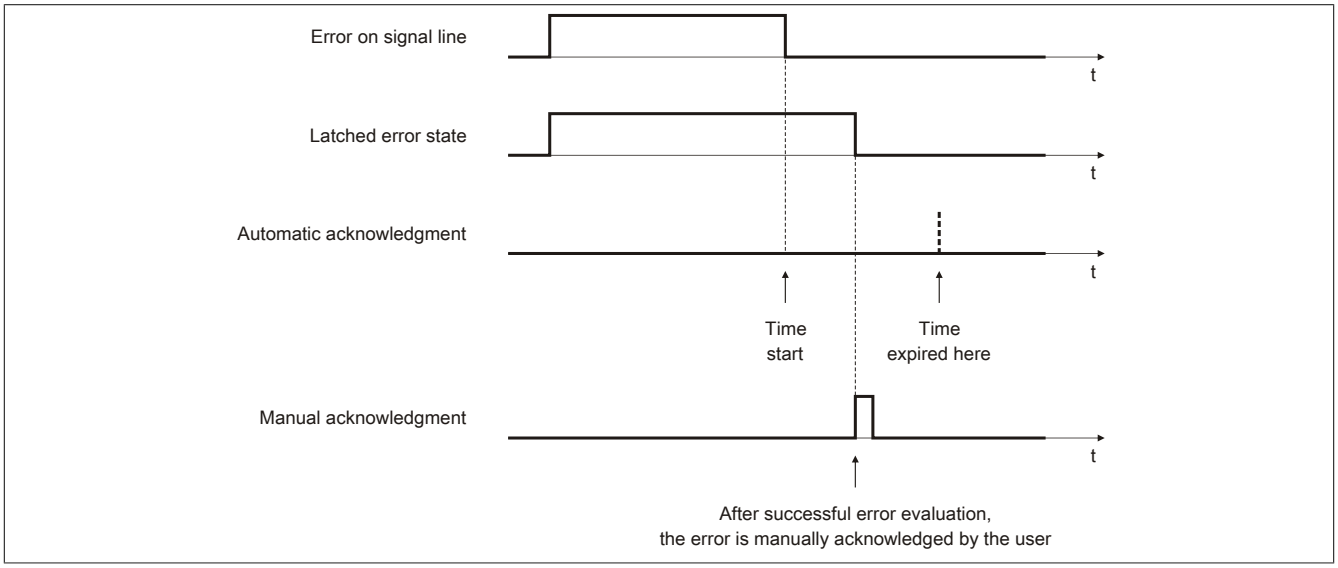


Figure 176: Automatic and manual acknowledge used

Manual acknowledgment of latched error states

The latched error states of the signal lines from the encoder can be acknowledged manually. However, if there are still pending errors remaining, then the error status remains active. After successfully acknowledging the errors (latched error status = 0), the acknowledge bits must still be reset by the user or else a re-occurrence of an error could be overlooked by the user.

Example 1: **Cause of error corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user after the cause of error has been corrected. The latched error status changes to zero.

The manual acknowledge must now be reset so that any new errors will be recognized by the user.

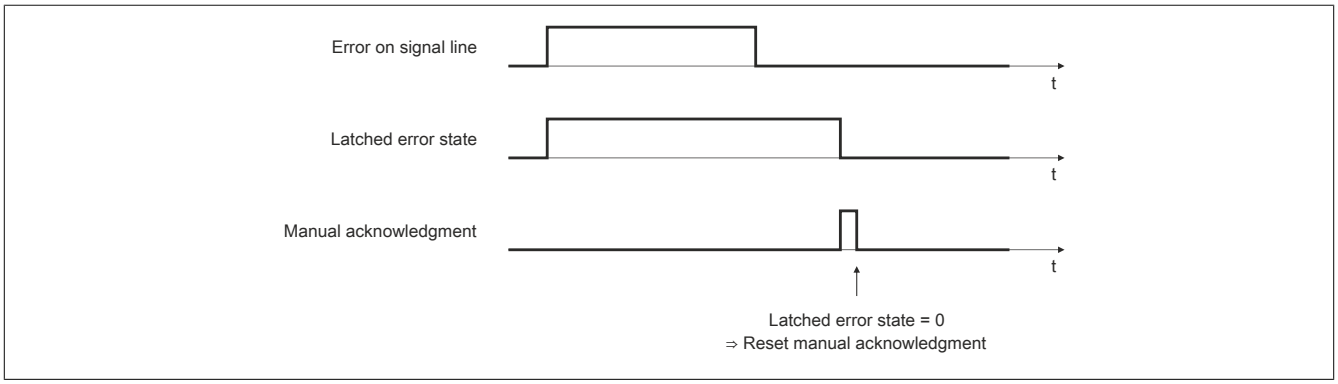


Figure 177: Cause of error corrected before being acknowledged

Example 2: **Cause of error not yet corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user before the cause of error has been corrected. The latched error status remains set because the error is still remaining.

Acknowledgment is only successful after the cause of error has been corrected. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

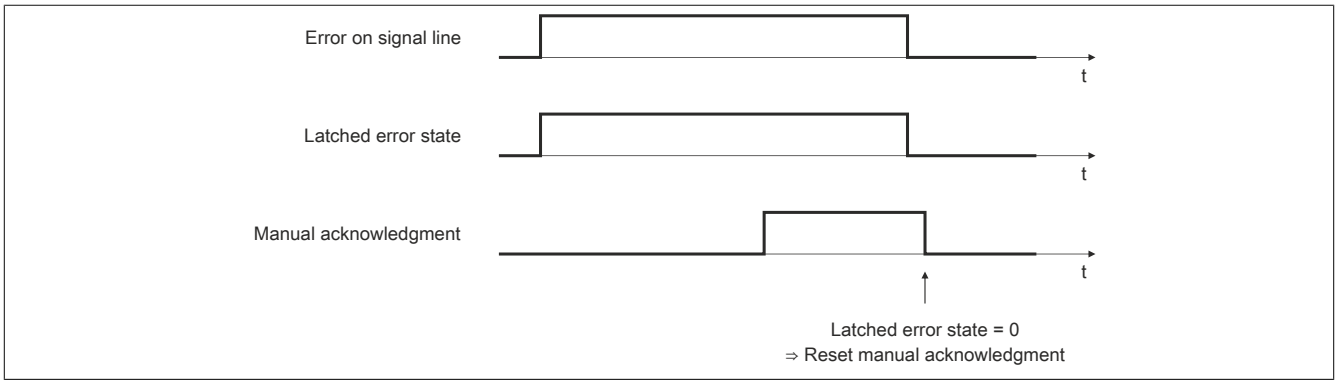


Figure 178: Cause of error not yet corrected before being acknowledged

4.11.4.9.4.6 Enable/disable error monitoring for the signal channels

Name:
CfO_BWSSIEnableMaskChannel7_0

This register allows error monitoring for each of the signal channels to be enabled individually. "Open line", "short circuit" and "voltage level too low" are reported as error states. Any errors that occur are reported in the error status registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder signal D	0	Error monitoring switched off
		1	Error monitoring enabled
1 - 7	Reserved	0	

4.11.4.9.4.7 Physical configuration

The following registers must be set to the specified constant value for correct physical configuration:

Constant register "CfO_BWQuitTimeSelChannel7_0"

Name:
CfO_BWQuitTimeSelChannel7_0

Data type	Value	Information
USINT	0	Only default in the bus controller module

4.11.4.9.5 Encoder - Communication

4.11.4.9.5.1 Counter for verifying the data frame

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.11.4.9.5.2 Input status of signal lines

Name:
DigitalInput0 to DigitalInput02

This register displays the input states for the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Reserved	0	
4	DigitalInput01	0 or 1	Input state - Digital input 1
5	DigitalInput02	0 or 1	Input state - Digital input 2
6 - 7	Reserved	0	

4.11.4.9.5.3 Display of the counter state

Name:
Encoder01

The counter state of the incremental encoder is displayed as a 16 or 32-bit counter value.

Data type	Value
UDINT	0 to 4.294.967.295
DINT	-2.147.483.648 to 2.147.483.647
UINT[1)]	0 to 65535

1) Only available in function model 0

4.11.4.9.5.4 Net time of the last valid counter value

Name:
Encoder01TimeValid

The net time of the last valid counter value is the time of the last valid counter value (see "Cfo_SystemCycleTime" register) recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The net time of the last valid counter value that was read is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in milliseconds.
DINT[1)]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

4.11.4.9.5.5 Net time of the last counter value change

Name:
Encoder01TimeChanged

For slow X2X Link cycles, the net time of the last counter value change can be used to more accurately determine the speed.

The net time of the last counter value change is displayed as 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µsec.
DINT[1)]	-2.147.483.648 bis 2.147.483.647	

1) Can only be configured in the standard function model

4.11.4.9.5.6 State of the encoder

Name:
EncoderCycleTimeViolation
EncoderDataError

This register displays the error states that occurred while determining the position. The error states are latched when they occur and are maintained until acknowledged.

A cycle time error is triggered if:

- Transfer is still active: This means that the defined cycle time is shorter than the time resulting from the sum of the data bits and stop bits and the clock rate.
- The monoflop level does not match the defined start level
- There is an error pending on the signal line (open line, short circuit).

A data error is triggered if:

- The parity bit does not match.
- An error occurs on the signal line (open line, short circuit) during transfer.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EncoderCycleTimeViolation	0	No error
		1	Error status - Cycle time violation
1	EncoderDataError	0	No error
		1	Error status - Data error
2 - 7	Reserved	0	

4.11.4.9.5.7 Acknowledging error status of the encoder

Name:
EncoderQuitCycleTimeViolation
EncoderQuitDataError

This register can be used to acknowledge the latched data error states from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EncoderQuitCycleTimeViolation	0	No acknowledgment
		1	Confirmation of error status - Cycle time violation
1	EncoderQuitDataError	0	No acknowledgment
		1	Confirmation of error status - Data error
2 - 7	Reserved	0	

4.11.4.9.5.8 Status of signal lines

Name:
BW_Channel_D

This register displays the error state of the signal line from the encoder. The error state is latched when it occurs and is maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_Channel_D	0	No error - Encoder signal D
		1	Error status - Open line or short circuit (voltage level too low)
1 - 7	Reserved	0	

4.11.4.9.5.9 Acknowledging error status of the signal line

Name:
BW_QuitChannel_D

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bit must also be reset or else any repetition of the error will be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_QuitChannel_D	0	No acknowledgment
		1	Acknowledgment of error status
1 - 7	Reserved	0	

4.11.4.9.5.10 Status of encoder supplies

Name:
PowerSupply01 to PowerSupply02

This register shows the status of the integrated encoder supplies. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1	PowerSupply02	0	5 VDC encoder power supply OK
		1	5 VDC encoder power supply faulty
2 - 7	Reserved	-	

4.11.4.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.11.4.9.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
150 µs

4.11.5 X20DC1196

4.11.5.1 General information

The module is equipped with 1 input for an ABR incremental encoder with 5 V encoder signal.

- 1 ABR incremental encoder 5 V
- 2 additional inputs e.g. for home enable switch
- 5 VDC, 24 VDC and GND for encoder supply

4.11.5.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1196	X20 digital counter module, 1 ABR incremental encoders, 5 V, 600 kHz input frequency, 4x evaluation	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 176: X20DC1196 - Order data

4.11.5.3 Technical data

Product ID	X20DC1196
Short description	
I/O module	1 ABR incremental encoder 5 V
General information	
B&R ID code	0x1BAF
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Encoder - Bus	Yes
Channel - Bus	Yes
Channel - Encoder	No
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines.
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Approx. 3.3 mA
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input circuit	Sink

Table 177: X20DC1196 - Technical data

Product ID	X20DC1196
Additional functions	Home enable switch
Input resistance	7.19 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Encoder inputs	5 V, symmetrical
Counter size	16/32-bit
Input frequency	Max. 600 kHz
Evaluation	4x
Encoder supply	
5 VDC	±5%, module-internal, max. 300 mA
24 VDC	Module-internal, max. 300 mA
Input filter	
Hardware	≤200 ns
Software	-
Common-mode range	-7 V ≤ V_{CM} ≤ +12 V
Overload behavior of the encoder supply	Short circuit protection, overload protection
Isolation voltage between encoder and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 177: X20DC1196 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.5.4 LED status indicators

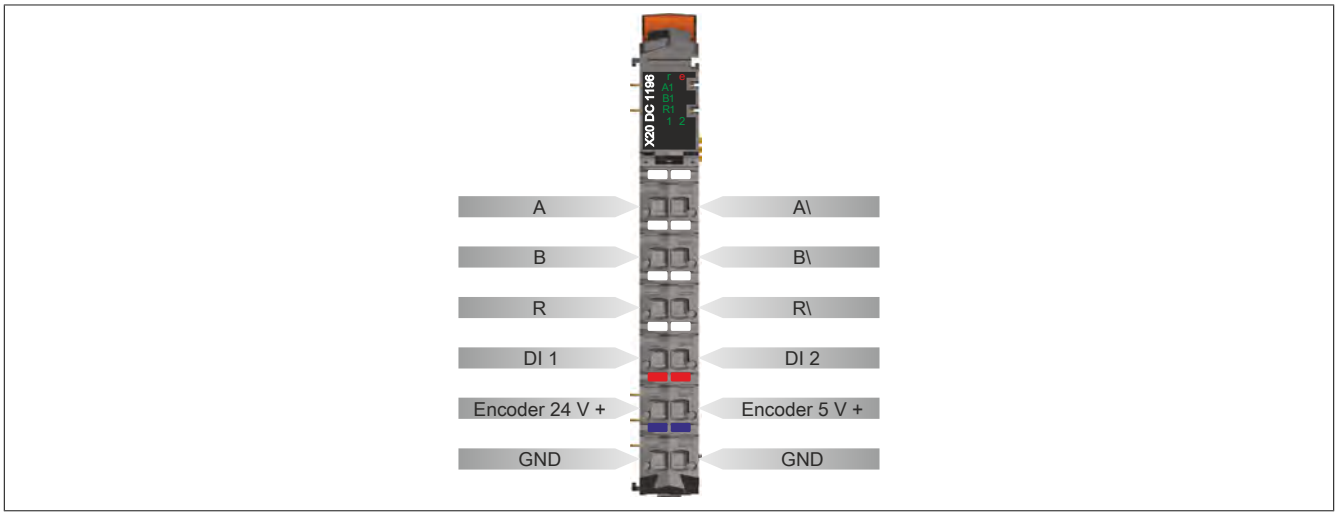
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	A1	Green		Input state of counter input A
	B1	Green		Input state of counter input B
	R1	Green		Input state of reference pulse R
	1 - 2	Green		Input state of the corresponding digital input

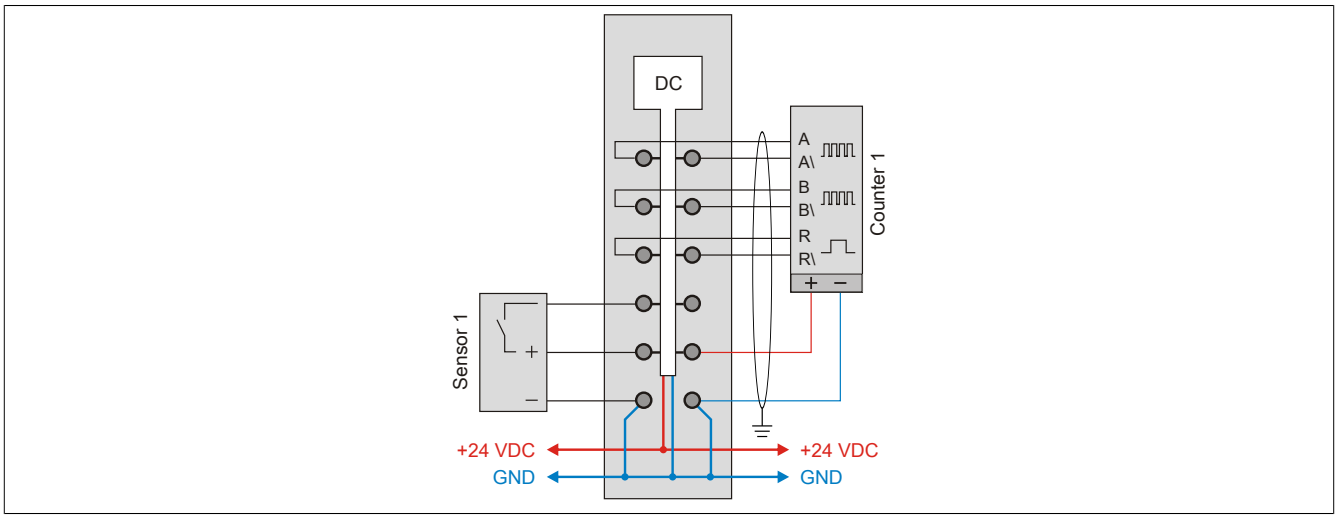
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.5.5 Pinout

Shielded cables must be used for all signal lines.

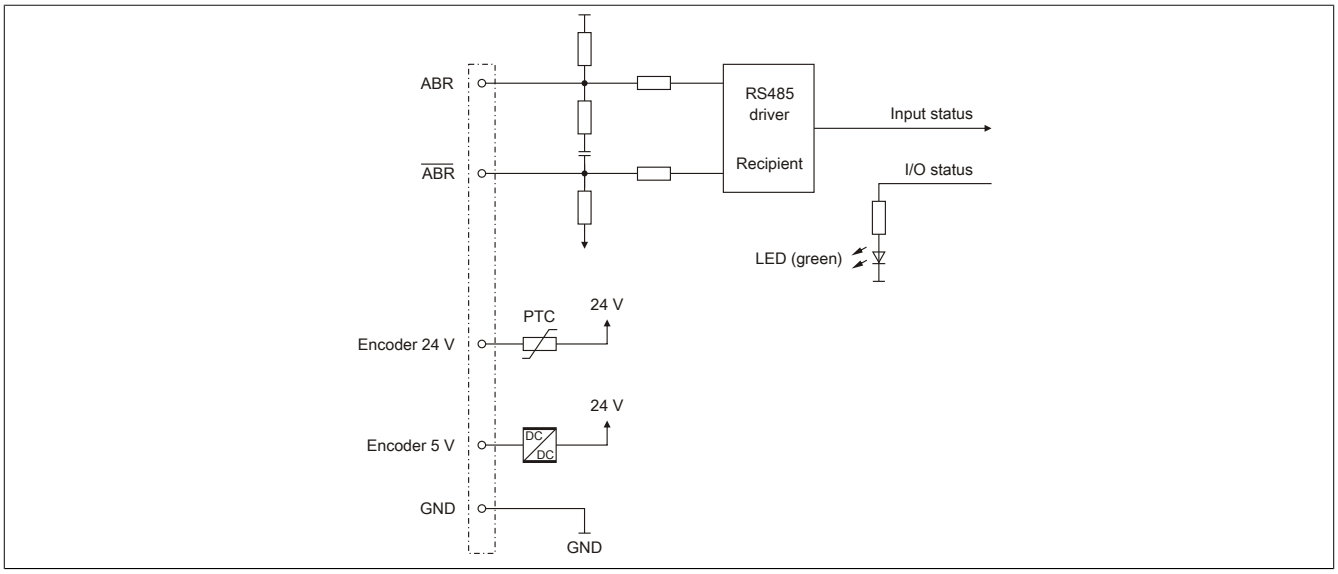


4.11.5.6 Connection example

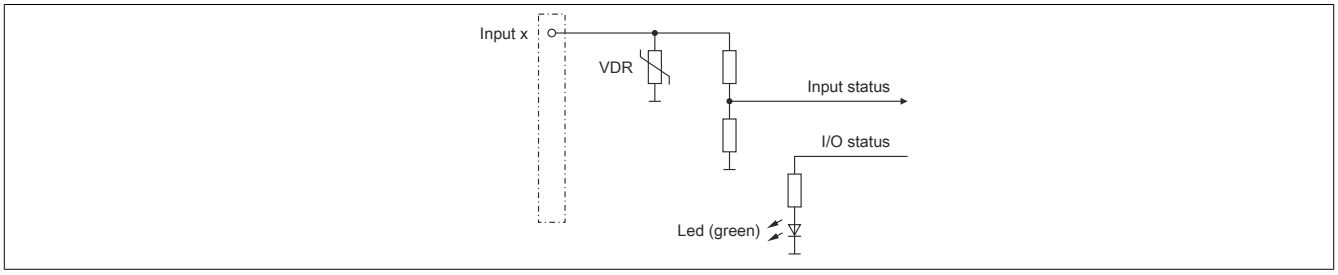


4.11.5.7 Input circuit diagram

Counter inputs



Standard inputs



4.11.5.8 Register description

4.11.5.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.5.8.2 Function model 0 - Standard and Function model 1 - Standard with 32-bit encoder counter value

The difference between function model 0 and function model 1 is the size of the data type for some registers.

- Function model 0 uses data type INT
- Function model 1 uses data type DINT (specified in parentheses)

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
4104	CfO_EdgeDetectFalling	USINT				•
4106	CfO_EdgeDetectRising	USINT				•
2064	CfO_PresetABR01_1(_32Bit)	(D)INT				•
2068	CfO_PresetABR01_2(_32Bit)	(D)INT				•
512	ConfigOutput24	UINT				•
522	ConfigOutput26	USINT				•
520	ConfigOutput27	USINT				•
Communication						
2116	ReferenceModeEncoder01	USINT			•	
2080	Encoder01	(D)INT	•			
264	Input state of digital inputs 1 to 2	USINT	•			
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
2118	StatusInput01	USINT	•			
40	Status of encoder supplies	USINT	•			
	PowerSupply01	Bit 0				
	PowerSupply02	Bit 1				

4.11.5.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
4104	-	CfO_EdgeDetectFalling	USINT				•
4106	-	CfO_EdgeDetectRising	USINT				•
2064	-	CfO_PresetABR01_1	INT				•
2068	-	CfO_PresetABR01_2	INT				•
512	-	ConfigOutput24	UINT				•
522	-	ConfigOutput26	USINT				•
520	-	ConfigOutput27	USINT				•
Communication							
2116	0	ReferenceModeEncoder01	USINT			•	
2080	0	Encoder01	INT	•			
264	2	Input state of digital inputs 1 to 2	USINT	•			
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
2118	4	StatusInput01	USINT	•			
40	3	Status of encoder supplies	USINT	•			
		PowerSupply01	Bit 0				
		PowerSupply02	Bit 1				

1) The offset specifies the position of the register within the CAN object.

4.11.5.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.5.8.4 ABR encoder - Configuration registers

4.11.5.8.4.1 Reference pulse

The following registers must be configured by a single acyclic write with the listed values so that the homing procedure is completed on the edge of the reference pulse.

The homing procedure can take place on:

- Rising edge
- Falling edge (default configuration)

Constant register "CfO_EdgeDetectFalling"

Name:

CfO_EdgeDetectFalling

Data type	Value	Filter
USINT	0x00	Configuration value for rising edge
	0x04	Configuration value for falling edge

Constant register "CfO_EdgeDetectRising"

Name:

CfO_EdgeDetectRising

Data type	Value	Filter
USINT	0x04	Configuration value for rising edge
	0x00	Configuration value for falling edge

Constant register "ConfigOutput24"

Name:

ConfigOutput24

This register contains the value for ABR encoder 1.

Data type	Value	Filter
UINT	0x1012	Configuration value for rising edge
	0x1002	Configuration value for falling edge

4.11.5.8.4.2 Setting the home position

Name:
Cfo_PresetABR01_1 to Cfo_PresetABR01_2

CfO_PresetABR01_1_32Bit to CfO_PresetABR01_2_32Bit (only in function model 1)

It is possible to specify two home positions with these registers through a one-off acyclic write, for example (default = 0). The configured values are applied to the counter values after a completed homing procedure.

Data type	Value
INT	-32,768 to 32,767
DINT[1)]	-2,147,483,648 to 2,147,483,647

1) Only in function model 1

4.11.5.8.4.3 Homing with reference enable input

Regardless of the referencing mode, it is possible using this register to prevent the home position from being applied when the corresponding reference input voltage level occurs (see 4.11.5.8.5.2 "Input state of digital inputs 1 to 2": bit 4). The desired setting can be configured by a one-off acyclic write.

Voltage level for reference enable activation

Name:

ConfigOutput26

The voltage level of the digital inputs to activate reference enable is configured with this register.

Data type	Value	Filter
USINT	0x00	Reference enable is active at 0 VDC
	0x10	Reference enable for digital input 1 is active at 24 VDC
	0x20	Reference enable for digital input 2 is active at 24 VDC
	0x30	Reference enable for both digital inputs is active at 24 VDC

Reference enable of the input

Name:

ConfigOutput27

This register can be used to define whether the reference enable is activated.

Data type	Value	Filter
USINT	0x00	Reference enable input OFF (default)
	0x10	Reference enable input 1 enabled
	0x20	Reference enable input 2 enabled
	0x30	Reference enable input 1 and 2 enabled

4.11.5.8.5 ABR encoder - Configuration registers

4.11.5.8.5.1 Counter state of the encoder

Name:
Encoder01

The encoder values are represented as 16-bit or 32-bit counter values in this register.

Data type	Value
INT	-32,768 to 32,767
DINT[1)]	-2,147,483,648 to 2,147,483,647

1) Only in function model 1

4.11.5.8.5.2 Input state of digital inputs 1 to 2

Name:
DigitalInput01 to DigitalInput02.

This register displays the input status of the encoders and the digital inputs.

Data type	Value
USINT	See bit structure.

Bit	Name	Value	Information
0	Encoder A	0 or 1	Input state
1	Encoder B	0 or 1	Input state
2	Encoder A + B	0 or 1	Input state of reference pulse
4	DigitalInput01	0 or 1	Input state - Digital input 1
5	DigitalInput02	0 or 1	Input state - Digital input 2

4.11.5.8.5.3 Reading the referencing mode

Name:
ReferenceModeEncoder01

This register determines the referencing mode.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1		00	Referencing OFF
		01	Single shot referencing
		11	Continuous referencing
2 - 5		0	Bits permanently set = 0
6 - 7		00	Referencing OFF
		11	Bits permanently set = 1

This results in the following values:

Binary	Hex	Function
00000000	0x00	Referencing OFF
11000001	0xC1	Single shot referencing For a new start after the completed homing procedure: • Write value 0x00 • Wait until bit 0 to bit 3 of the StatusInput01 register takes on the value 0. Counter bits 4 to 7 are not erased • Switch homing procedure on again
11000011	0xC3	Continuous referencing Referencing occurs at every reference pulse.

It is important to know how the optional reference enable is configured. See section 4.11.5.8.4.3 "Homing with reference enable input"

4.11.5.8.5.4 Status of the homing procedure

Name:
StatusInput01

This register contains information regarding whether the referencing process is off, active or complete.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Reference pulse without homing[1)]	0	No reference impulse without homing has occurred yet
		1	At least a reference impulse without homing has occurred
1	State change	0 or 1	Changes with each reference pulse without homing
2	Reference pulse with homing[1)]	0	No homing has occurred yet
		1	At least one homing procedure has occurred
3	State change	0 or 1	Changes with each homing procedure that has taken place
4	Reference pulse	0	The last reference pulse didn't bring about a homing procedure
		1	The last reference pulse brought about a homing procedure
5 - 7	Counter	x	Free-running counter, increased with each reference pulse

1) Always 1 after the first reference pulse that has occurred

Examples of possible values:

Binary	Hex	Function
0x00000000	0x00	Referencing OFF or homing procedure already active
0x00111100	0x3CE	First homing procedure complete Reference value applied in the Encoder01 register
0xxxx11100	0xxB	Bits 5 to 7 are changed with each reference pulse
0xxxx1x100	0xxx	Continuously changing the bits with the "Continuous referencing" setting. The reference value is applied to the Encoder01 register on each reference pulse.

It is important to know how the optional reference enable (see section 4.11.5.8.4.3 "Homing with reference enable input" on page 904) is configured.

4.11.5.8.5.5 Status of encoder supplies

Name:
PowerSupply01 to PowerSupply02

This register shows the status of the integrated encoder supplies. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1	PowerSupply02	0	5 VDC encoder power supply OK
		1	5 VDC encoder power supply faulty
2 - 7	Reserved	-	

4.11.5.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

4.11.5.8.7 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

4.11.5.8.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
128 µs

4.11.6 X20(c)DC1198

4.11.6.1 General information

This module is equipped with one input for SSI absolute encoders with 5 V encoder signal.

- 1 SSI absolute encoder 5 V
- 2 additional inputs
- 5 VDC, 24 VDC and GND for encoder supply

4.11.6.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.11.6.3 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1198	X20 digital counter module, 1 SSI absolute encoder, 5 V, 1 Mbit/s, 32-bit	
X20cDC1198	X20 digital counter module, coated, 1 SSI absolute encoders, 5 V, 1 Mbit/s, 32-bit	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 178: X20DC1198, X20cDC1198 - Order data

4.11.6.4 Technical data

Product ID	X20DC1198	X20cDC1198
Short description		
I/O module	1 SSI absolute encoder 5 V	
General information		
B&R ID code	0x1BB0	0xE501
Status indicators	I/O function per channel, operating state, module status	
Diagnostics Module run/error	 Yes, using status LED and software	
Power consumption Bus Internal I/O	 0.01 W 1.5 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation Encoder - Bus Channel - Bus Channel - Encoder Channel - Channel	 Yes Yes No No	
Type of signal lines	Shielded cables must be used for all signal lines.	

Table 179: X20DC1198, X20cDC1198 - Technical data

Product ID	X20DC1198	X20cDC1198
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Digital inputs		
Quantity	2	
Nominal voltage	24 VDC	
Input voltage	24 VDC -15 % / +20 %	
Input current at 24 VDC	Approx. 3.3 mA	
Input filter		
Hardware	≤2 µs	
Software	-	
Connection type	3-wire connections	
Input circuit	Sink	
Input resistance	7.19 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
SSI absolute encoder		
Encoder inputs	5 V, symmetrical	
Counter size	32-bit	
Max. transfer rate	1 Mbit/s	
Keying	Gray/Binary	
Isolation voltage between encoder and bus	500 V_{eff}	
Overload behavior of the encoder supply	Short circuit protection, overload protection	
Transfer rate	125 kbit/s / 250 kbit/s / 500 kbit/s / 1 Mbit/s	
Encoder supply		
5 VDC	±5%, module-internal, max. 300 mA	
24 VDC	Module-internal, max. 300 mA	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 179: X20DC1198, X20cDC1198 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.6.5 LED status indicators

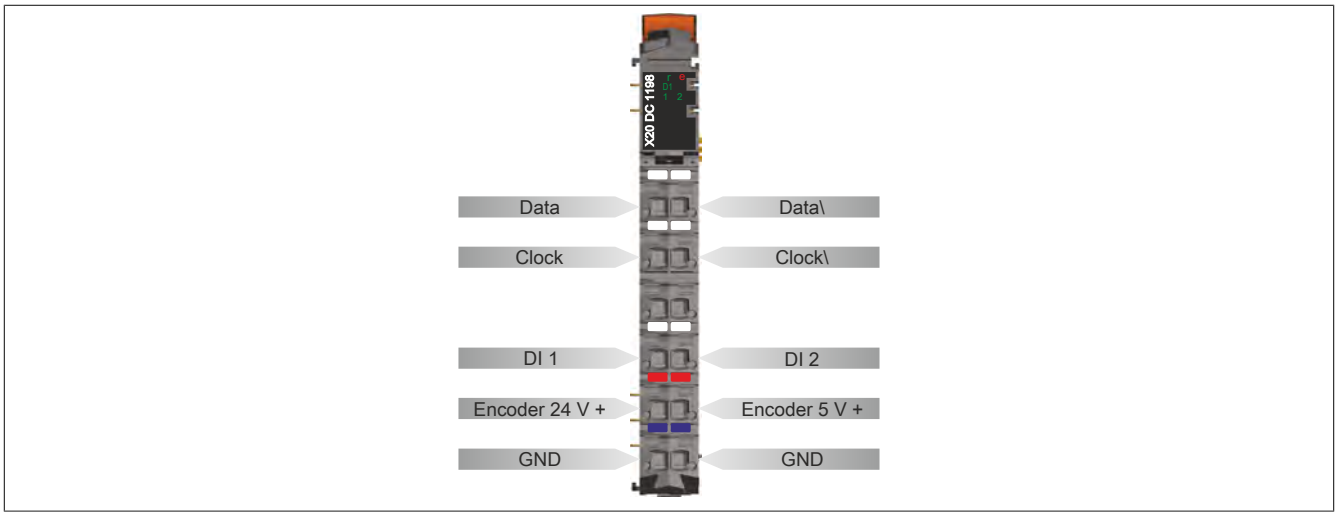
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	D1	Green		Input status - Data signal
	1 - 2	Green		Input state of the corresponding digital input

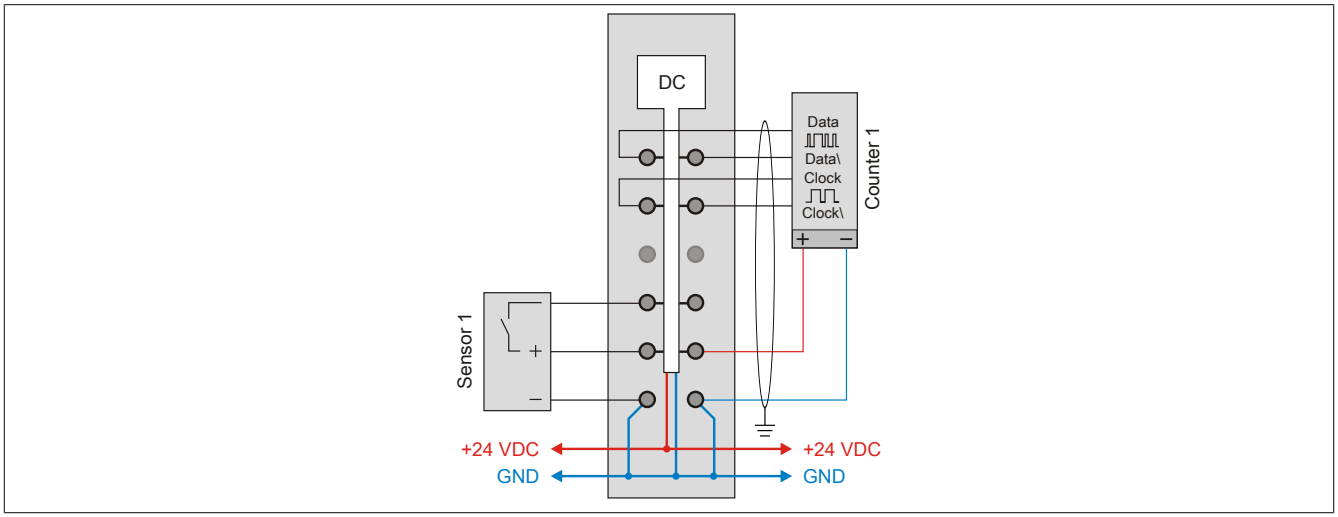
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.6.6 Pinout

Shielded cables must be used for all signal lines.

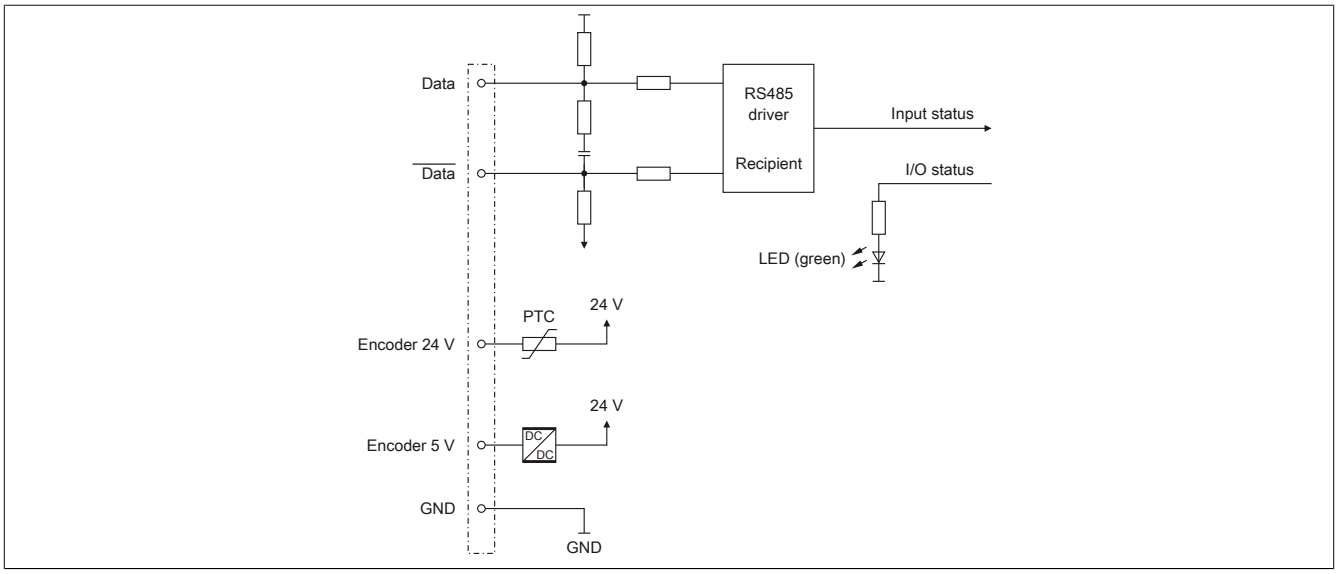


4.11.6.7 Connection example

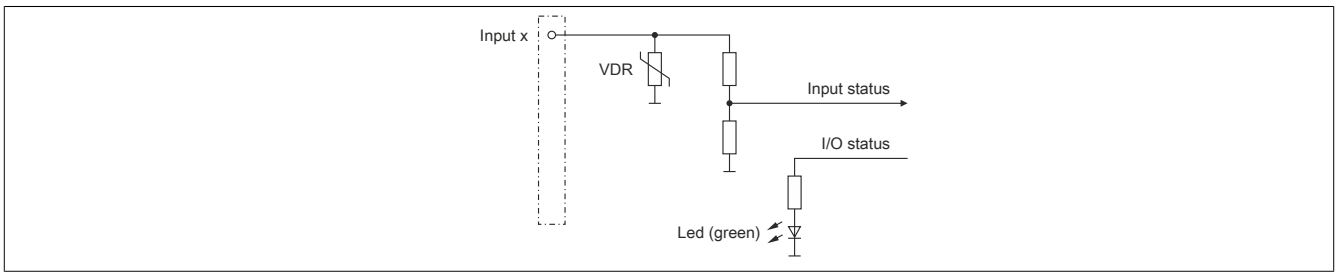


4.11.6.8 Input circuit diagram

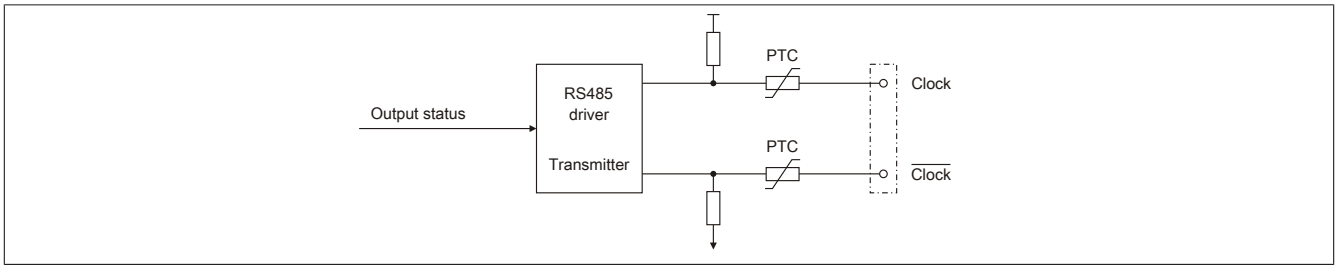
Counter input



Standard inputs



4.11.6.9 Output circuit diagram



4.11.6.10 Register description

4.11.6.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.6.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
7176	ConfigOutput14	UINT				•
7172	ConfigAdvanced	UDINT				•
Communication						
7184	Encoder01	UDINT	•			
264	Input state of digital inputs 1 to 2	USINT	•			
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
40	Status of encoder supplies	USINT	•			
	PowerSupply01	Bit 0				
	PowerSupply02	Bit 1				

4.11.6.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
7176	-	ConfigOutput14	UINT				•
7172	-	ConfigAdvanced	UDINT				•
Communication							
7184	0	Encoder01	UDINT	•			
264	4	Input state of digital inputs 1 to 2	USINT	•			
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
40	5	Status of encoder supplies	USINT	•			
		PowerSupply01	Bit 0				
		PowerSupply02	Bit 1				

1) The offset specifies the position of the register within the CAN object.

4.11.6.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.6.10.4 SSI encoder configuration register

4.11.6.10.4.1 Standard configuration

Name:
ConfigOutput14

This configuration register is used to set the coding, the clock rate and the number of bits. Default = 0. This must be set once using an acyclic write command.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	00	1 MHz
		01	500 kHz
		10	250 kHz
		11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding

4.11.6.10.4.2 Extended configuration

Name:
ConfigAdvanced

This configuration register is used to set the coding, the clock rate, the number of bits and the monostable multivibrator settings. Default = 0. This must be set once using an acyclic write command.

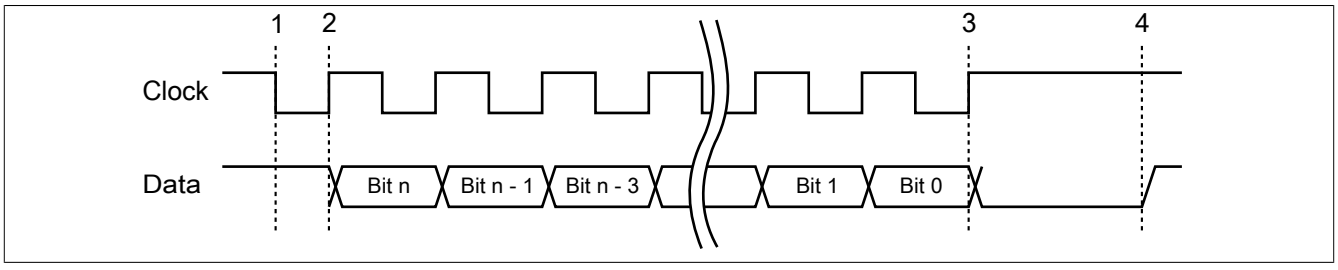
It only differs from ConfigOutput14 by data length and additional monostable multivibrator testing.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	00	1 MHz
		01	500 kHz
		10	250 kHz
		11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding
16 - 17	Monostable multivibrator testing	00	Check OFF, no additional clock bit
		01	Check set to High level
		10	Check set to Low level
		11	Level is clocked but ignored
18 - 31	Reserved	0	Reserved

Transfer to synchronous serial interface



Measurement value processing

1 Starting bit ... Stores the measurement value
2 Output of first data bit
3 All data bits are transferred, monostable multivibrator time starts counting down.
4 Monostable multivibrator returns to its initial state. A new transfer can be started.

4.11.6.10.5 SSI encoder - Configuration registers

4.11.6.10.5.1 SSI position values

Name:
Encoder01

The SSI encoder value is displayed as a 32-bit position value. The SSI position value is generated synchronously with the X2X cycle.

Data type	Value	Filter
UDINT	0 to 4,294,967,295	SSI position

4.11.6.10.5.2 Input state of digital inputs 1 to 2

Name:
DigitalInput01 to DigitalInput02

This register is used to indicate the input state of digital inputs 1 to 2.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
4	DigitalInput01	0 or 1	Input state - Digital input 1
5	DigitalInput02	0 or 1	Input state - Digital input 2

4.11.6.10.5.3 Status of encoder supplies

Name:
PowerSupply01 to PowerSupply02

This register shows the status of the integrated encoder supplies. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1	PowerSupply02	0	5 VDC encoder power supply OK
		1	5 VDC encoder power supply faulty
2 - 7	Reserved	-	

4.11.6.10.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

4.11.6.10.7 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

4.11.6.10.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
128 µs

4.11.7 X20DC11A6

4.11.7.1 General information

The module is equipped with 1 input for an ABR incremental encoder with 5 V encoder signal. The encoder inputs are monitored (A, B, R, A\, B\, R\).

- 1 ABR incremental encoder 5 V
- Encoder input monitoring (up to 250 kHz input frequency)
- 2 additional inputs, e.g. for latch input
- 5 VDC, 24 VDC and GND for encoder supply

4.11.7.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC11A6	X20 digital counter module, 1 ABR incremental encoder, 5 V 5 MHz input frequency, 4x evaluation, encoder monitoring, Net-Time module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 180: X20DC11A6 - Order data

4.11.7.3 Technical data

Product ID	X20DC11A6
Short description	
I/O module	1 ABR incremental encoder 5 V
General information	
B&R ID code	0xB76B
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Approx. 3.3 mA
Input filter	
Hardware	≤30 ns
Software	-
Connection type	3-wire connections
Input circuit	Sink
Additional functions	Latch input

Table 181: X20DC11A6 - Technical data

Product ID	X20DC11A6
Input resistance	7.03 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Encoder inputs	5 V, symmetrical
Counter size	16/32-bit
Input frequency	Max. 5 MHz
Evaluation	4x
Encoder supply	
5 VDC	±5%, module-internal, max. 300 mA
24 VDC	Module-internal, max. 300 mA
Input filter	
Hardware	≤30 ns
Software	-
Common-mode range	-10 V ≤ V_{CM} ≤ +13.2 V
Overload behavior of the encoder supply	Short circuit protection, overload protection
Isolation voltage between encoder and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 181: X20DC11A6 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.7.4 LED status indicators

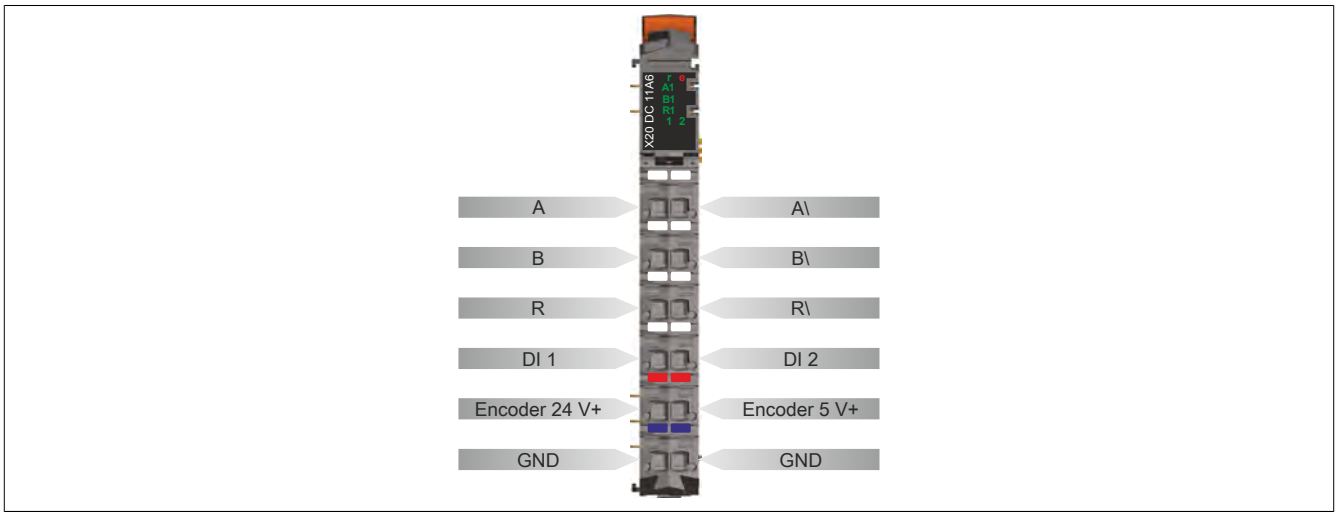
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	The encoder monitor has detected a line fault on the encoder inputs. The status bits must be evaluated in order to provide a more detailed definition of this error. The following error states are detected: • Broken connection (up to 250 kHz input frequency) • Short-circuit or voltage level too low
			On	Error or reset status
	A1	Green		Input state of counter input A
	B1	Green		Input state of counter input B
	R1	Green		Input state of reference pulse R
	1 - 2	Green		Input state of the corresponding digital input

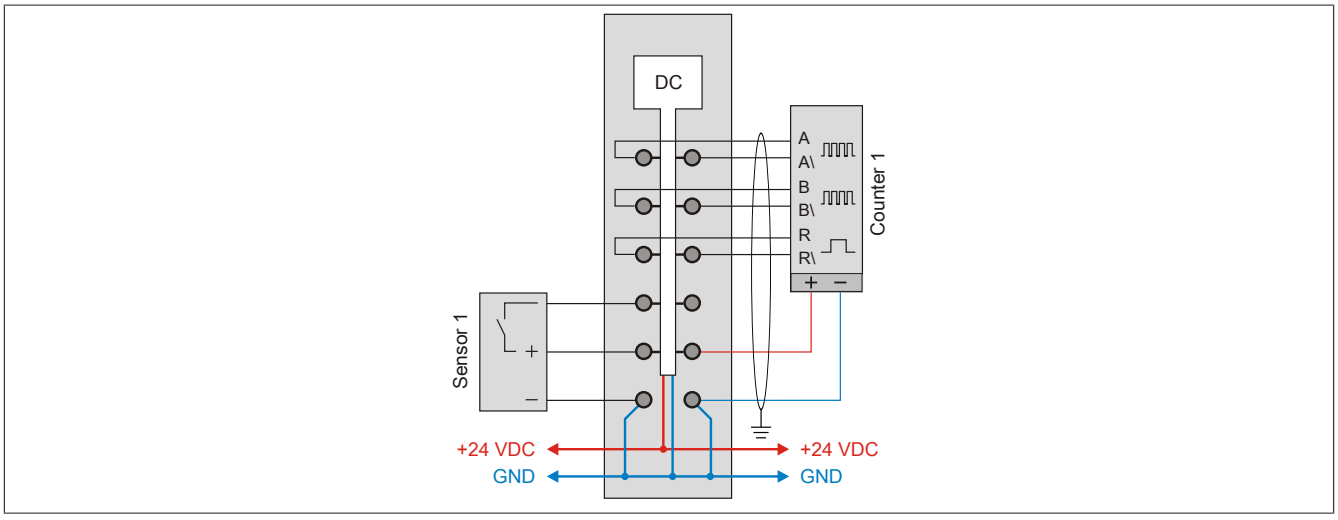
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.7.5 Pinout

Shielded cables must be used for all signal lines.

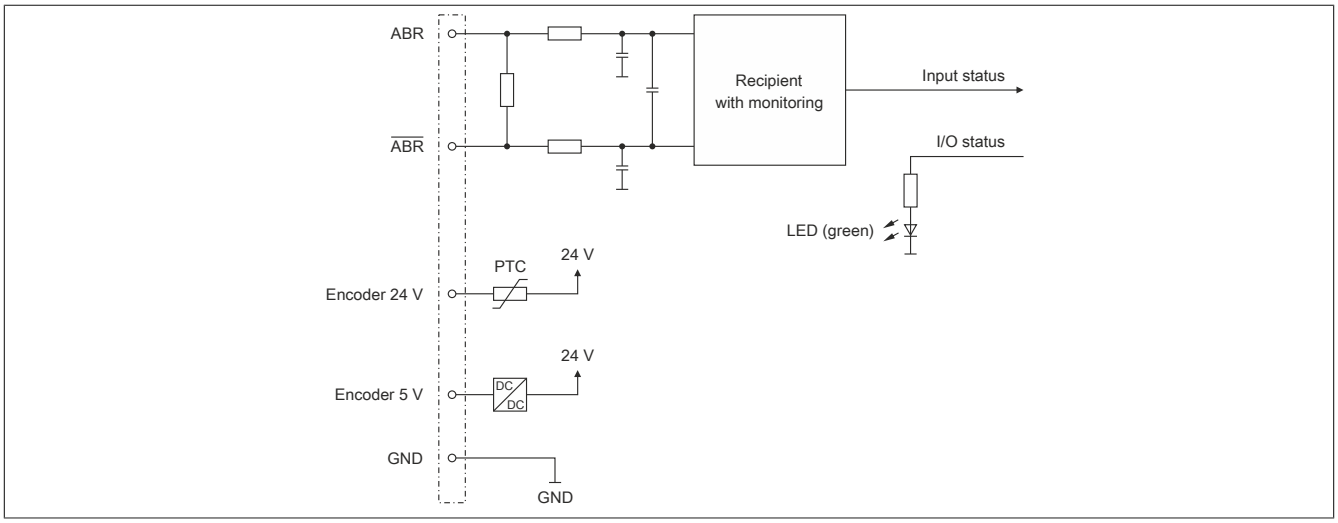


4.11.7.6 Connection example

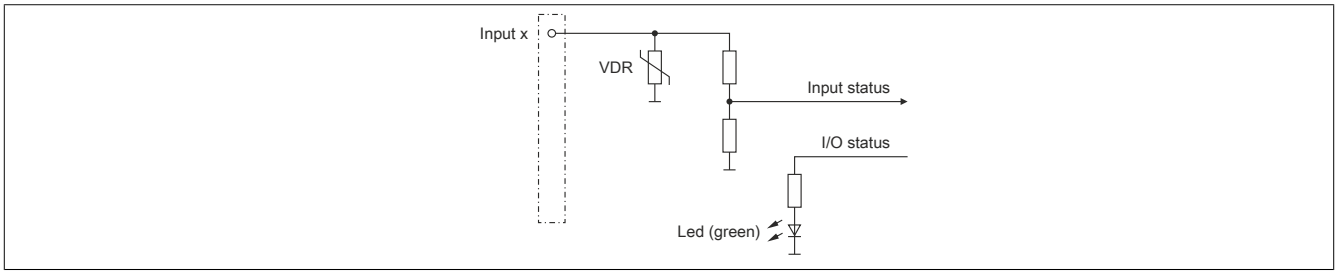


4.11.7.7 Input circuit diagram

Counter inputs



Standard inputs



4.11.7.8 Register description

4.11.7.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.7.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication						
683	SDCLifeCount	SINT	•			
6342	Encoder01	INT	•			
6340		DINT				
6310	Encoder01TimeValid	INT	•			
6308		DINT				
6358	Encoder01Latch	INT	•			
6356		DINT				
6153	Encoder commands	USINT			•	
	Encoder01Reset	Bit 0				
	Encoder01LatchEnable	Bit 1				
927	Input status of signal lines	USINT	•			
	Encoder01_A	Bit 0				
	Encoder01_B	Bit 1				
	Encoder01_R	Bit 2				
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
847	Status of signal lines	USINT	•			
	BW_Channel_A	Bit 0				
	BW_Channel_B	Bit 1				
	BW_Channel_R	Bit 2				
811	Acknowledging error status of signal lines	USINT			•	
	BW_QuitChannel_A	Bit 0				
	BW_QuitChannel_B	Bit 1				
	BW_QuitChannel_R	Bit 2				
6326	Encoder01TimeChanged	INT	•			
6324		DINT				
6303	Encoder01LatchCount	SINT	•			
843	Status of encoder supplies	USINT	•			
	PowerSupply01	Bit 0				
	PowerSupply02	Bit 1				
Encoder - Configuration						
513	CfO_SIframeGenID	USINT				•
642	CfO_SystemCycleTime	UINT				•
769	CfO_PhyIOConfigCh01	USINT				•
771	CfO_PhyIOConfigCh02	USINT				•
773	CfO_PhyIOConfigCh03	USINT				•
777	CfO_PhyIOConfigCh04	USINT				•
779	CfO_PhyIOConfigCh05	USINT				•
815	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	CfO_BWQuitTime_0	UDINT				•
6145	CfO_CounterCycleSelect	USINT				•
6147	CfO_CounterMode	USINT				•
6149	CfO_LatchMode	USINT				•
6151	CfO_LatchComparator	USINT				•
6159	CfO_BWCNTEnableMaskChannel7_0	USINT				•

4.11.7.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication							
6342	0	Encoder01	INT	•			
6310	2	Encoder01TimeValid	INT	•			
6358	4	Encoder01Latch	INT	•			
6153	1	Encoder commands	USINT			•	
		Encoder01Reset	Bit 0				
		Encoder01LatchEnable	Bit 1				
927	7	Input status of signal lines	USINT	•			
		Encoder01_A	Bit 0				
		Encoder01_B	Bit 1				
		Encoder01_R	Bit 2				
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
847	6	Status of signal lines	USINT	•			
		BW_Channel_A	Bit 0				
		BW_Channel_B	Bit 1				
		BW_Channel_R	Bit 2				
811	0	Acknowledging error status of signal lines	USINT			•	
		BW_QuitChannel_A	Bit 0				
		BW_QuitChannel_B	Bit 1				
		BW_QuitChannel_R	Bit 2				
6326	-	Encoder01TimeChanged	INT		•		
6303	-	Encoder01LatchCount	SINT		•		
843	-	Status of encoder supplies	USINT		•		
		PowerSupply01	Bit 0				
		PowerSupply02	Bit 1				
Encoder - Configuration							
513	-	CfO_SIframeGenID	USINT				•
642	-	CfO_SystemCycleTime	UINT				•
769	-	CfO_PhyIOConfigCh01	USINT				•
771	-	CfO_PhyIOConfigCh02	USINT				•
773	-	CfO_PhyIOConfigCh03	USINT				•
777	-	CfO_PhyIOConfigCh04	USINT				•
779	-	CfO_PhyIOConfigCh05	USINT				•
815	-	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	-	CfO_BWQuitTime_0	UDINT				•
6145	-	CfO_CounterCycleSelect	USINT				•
6147	-	CfO_CounterMode	USINT				•
6149	-	CfO_LatchMode	USINT				•
6151	-	CfO_LatchComparator	USINT				•
6159	-	CfO_BWCNTEnableMaskChannel7_0	USINT				•

1) The offset specifies the position of the register within the CAN object.

4.11.7.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.7.8.4 Encoder - Configuration

The following registers are used for setting functions and configuring the module.

4.11.7.8.4.1 Enabling error monitoring for the signal lines

Name:
CfO_BWCNTEnableMaskChannel7_0

This register requires individually enabling error monitoring for each of the signal channels. "Open line", "short circuit" and "voltage level too low" are reported as error states. Any errors that occur are reported in the error status registers BW_Channel_x.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Enable error monitoring for signal A lines	0	Error monitoring - Encoder Signal A disabled
		1	Error monitoring - Encoder Signal A enabled - Only default in bus controller function model
1	Enable error monitoring for signal B lines	0	Error monitoring - Encoder Signal B disabled
		1	Error monitoring - Encoder Signal B enabled - Only default in bus controller function model
2	Enable error monitoring for signal R lines	0	Error monitoring - Encoder Signal R disabled
		1	Error monitoring - Encoder Signal R enabled - Only default in bus controller function model
3 - 7	Reserved	0	

4.11.7.8.4.2 Timing for automatic error acknowledgment

Name:
CfO_BWQuitTime_0

This register can be used to enable an additional automatic acknowledgment of the error status through timing. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Data type	Value	Information
UDINT	0	No automatic acknowledgment - Only default in bus controller function model
	1 to 2.147.483.647	Time for automatic acknowledgment [µs]

4.11.7.8.4.3 Setting the latch mode

Name:
CfO_LatchMode

This register is used to set the latch mode:

- Single shot latch mode:
  The latch function must be enabled/set. After a successful latch procedure, the activation must be reset in order for a new latch procedure to be activated.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired.

A changed counter state on Encoder01LatchCount indicates that the latch procedure has been performed. The counter value is stored in the latch register Encoder01Latch.

Data type	Value	Information
USINT	0	Single shot latch procedure
	1	Continuous latch procedure

4.11.7.8.4.4 Signal channels for triggering latch procedure

Name:
CfO_LatchComparator

This register defines the signal channels and their level for triggering the latch procedure.

- This mainly configures which channels are linked to generate the latch event. All three signals from the encoder and digital input 1 can be used for the "AND" operation.
- The "active voltage level" needed for the latch procedure can now be used according to the physical signals.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Defines signal level for encoder signal A	0	Low
		1	High
1	Defines signal level for encoder signal B	0	Low
		1	High
2	Defines signal level for encoder signal R	0	Low
		1	High
3	Defines signal level for digital input 1	0	Low
		1	High
4	Use encoder signal A to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal A
5	Use encoder signal B to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal B
6	Use encoder signal R to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal R
7	Use digital input 1 to trigger latch procedure	0	Disabled
		1	Latch function linked to digital input 1

4.11.7.8.4.5 Physical configuration

The following registers must be set to the specified constant value for correct physical configuration:

Constant register "CfO_SIframeGenID"

Name:
CfO_SIframeGenID

Data type	Value	Information
USINT	9	Only default in the bus controller module

Constant register "CfO_SystemCycleTime"

Name:
CfO_SystemCycleTime

Cycle time of encoder acquisition in 1/8 µs steps. 1 encoder value is acquired as the counter value per cycle.

Data type	Value	Information
UINT	800	800 = 100 µs; only default in the bus controller module

Constant register "CfO_PhyIOConfigCh01"

Name:
CfO_PhyIOConfigCh01

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh02"

Name:
CfO_PhyIOConfigCh02

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh03"

Name:
CfO_PhyIOConfigCh03

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh04"

Name:
CfO_PhyIOConfigCh04

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh05"

Name:
CfO_PhyIOConfigCh05

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_BWQuitTimeSelChannel7_0"

Name:
CfO_BWQuitTimeSelChannel7_0

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_CounterCycleSelect"

Name:
CfO_CounterCycleSelect

Data type	Value	Information
USINT	2	Only default in the bus controller module

Constant register "CfO_CounterMode"

Name:
CfO_CounterMode

Data type	Value	Information
USINT	3	Only default in the bus controller module

4.11.7.8.5 Encoder - Communication

4.11.7.8.5.1 Counter for verifying the data frame

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.11.7.8.5.2 Display of the counter state

Name:
Encoder01

The counter state of the incremental encoder is displayed as a 16 or 32-bit counter value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.7.8.5.3 Net time of the last valid counter value

Name:
Encoder01TimeValid

The net time of the last valid counter value is the time of the last valid counter value (see "Cfo_SystemCycleTime" register) recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The net time of the last valid counter value that was read is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in milliseconds.
DINT[1)]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

4.11.7.8.5.4 Net time of the last counter value change

Name:
Encoder01TimeChanged

For slow X2X Link cycles, the net time of the last counter value change can be used to more accurately determine the speed.

The net time of the last counter value change is displayed as 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µsec.
DINT[1)]	-2.147.483.648 bis 2.147.483.647	

1) Can only be configured in the standard function model

4.11.7.8.5.5 Counter value at the time of the last latch

Name:
Encoder01Latch

The counter value at the time of the last latch is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.7.8.5.6 Counter value of latch event

Name:
Encoder01LatchCount

The latch events are counted and stored in a cyclic 8-bit counter. This counter is incremented with each latch event, thereby indicating a new occurrence. The new latched counter value is stored in the respective latch register.

Data type	Value
SINT	-128 to 127

4.11.7.8.5.7 Encoder commands

Name:
Encoder01Command

This register can be used to

1 reset the counter value. The counter is kept at zero until this command is reset.
2 enable the latch procedure. If the latch configuration is valid and matches the hardware signals, then this activation causes the counter value to be saved in the latch register.

The two different latch configurations that are possible (see section 4.11.3.8.4.3 "Setting the latch mode") must be handled as follows:

- Single shot latch mode:
  After successful latching, indicated by the latch event counter, activation must be reset before any more latching is possible. The activation must be set again if additional latching is needed.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired. The latch event counter is incremented with each event.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01Reset	0	Do not reset
		1	Set encoder value to 0
1	Encoder01LatchEnable	0	Do not activate latch
		1	Latching
2 - 7	Reserved	0	

4.11.7.8.5.8 Input status of signal lines

Name:
Encoder01_A
Encoder01_B
Encoder01_R
DigitalInput01 to DigitalInput02

This register displays the input status of the signal lines from the encoder and the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01_A	0/1	Input state of encoder signal A
1	Encoder01_B	0/1	Input state of encoder signal B
2	Encoder01_R	0/1	Input state of encoder signal R
3	Reserved	0	
4	DigitalInput01	0/1	Input state - Digital input 1
5	DigitalInput02	0/1	Input state - Digital input 2
6 - 7	Reserved	0	

4.11.7.8.5.9 Error status of signal lines

The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Status of signal lines

Name:
BW_Channel_A
BW_Channel_B
BW_Channel_R

This register displays the error states of the signal lines from the encoder. The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_Channel_A	0	No error in encoder signal A
		1	Open line, short circuit or voltage level too low
1	BW_Channel_B	0	No error in encoder signal B
		1	Open line, short circuit or voltage level too low
2	BW_Channel_R	0	No error in encoder signal R
		1	Open line, short circuit or voltage level too low
3 - 7	Reserved	0	

Acknowledging error status of signal lines

Name:
BW_QuitChannel_A
BW_QuitChannel_B
BW_QuitChannel_R

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_QuitChannel_A	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal A
1	BW_QuitChannel_B	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal B
2	BW_QuitChannel_R	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal R
3 - 7	Reserved	0	

Manual acknowledgment of latched error states

The latched error states of the signal lines from the encoder can be acknowledged manually. However, if there are still pending errors remaining, then the error status remains active. After successfully acknowledging the errors (latched error status = 0), the acknowledge bits must still be reset by the user or else a re-occurrence of an error could be overlooked by the user.

Example 1: **Cause of error corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user after the cause of error has been corrected. The latched error status changes to zero.

The manual acknowledge must now be reset so that any new errors will be recognized by the user.

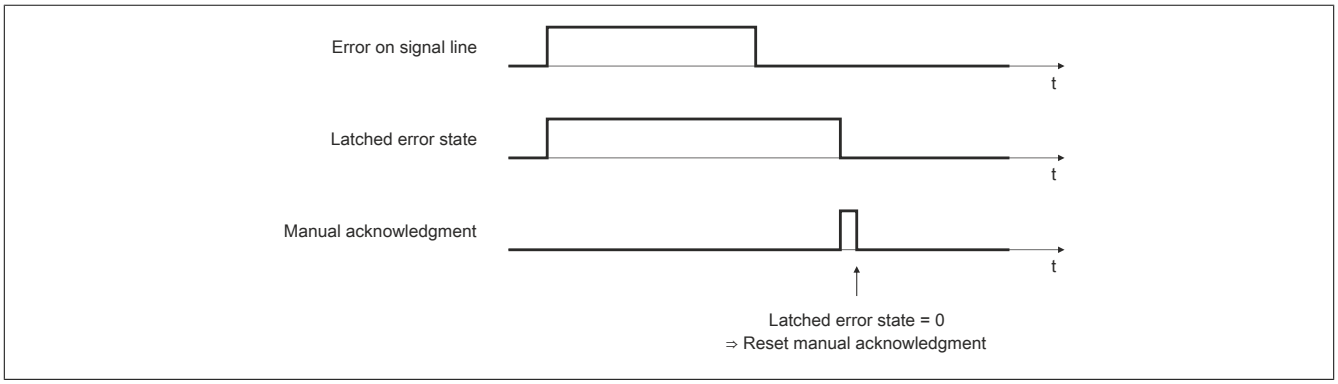


Figure 179: Cause of error corrected before being acknowledged

Example 2: **Cause of error not yet corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user before the cause of error has been corrected. The latched error status remains set because the error is still remaining.

Acknowledgment is only successful after the cause of error has been corrected. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

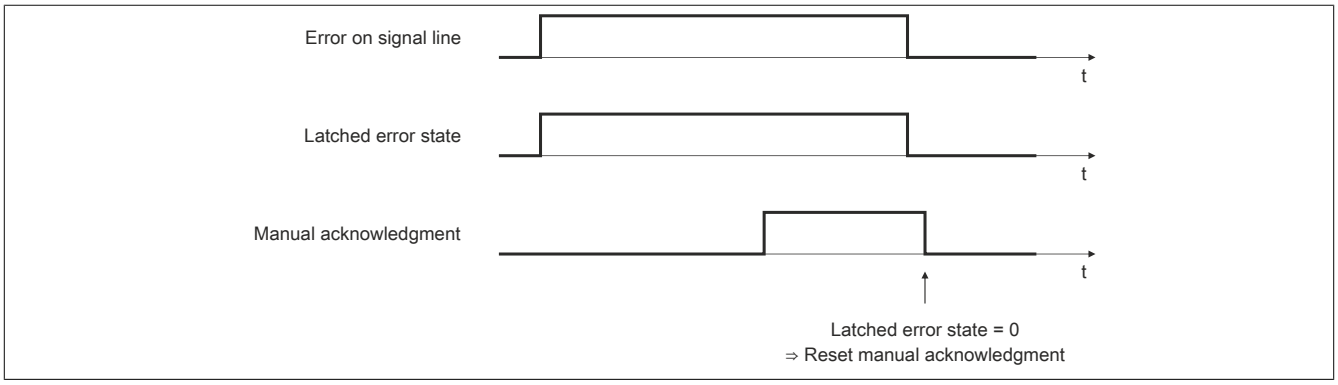


Figure 180: Cause of error not yet corrected before being acknowledged

Automatic acknowledgment of latched error states

In addition to manual acknowledgment, automatic acknowledgment of the latched error states after a specified amount of time can also be enabled. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages and for the validity of the counter value to be determined using its age.

If the time specification = 0, then only manual acknowledgment is possible.

Example 1: An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged as soon as the time expires. The latched error status changes to zero.

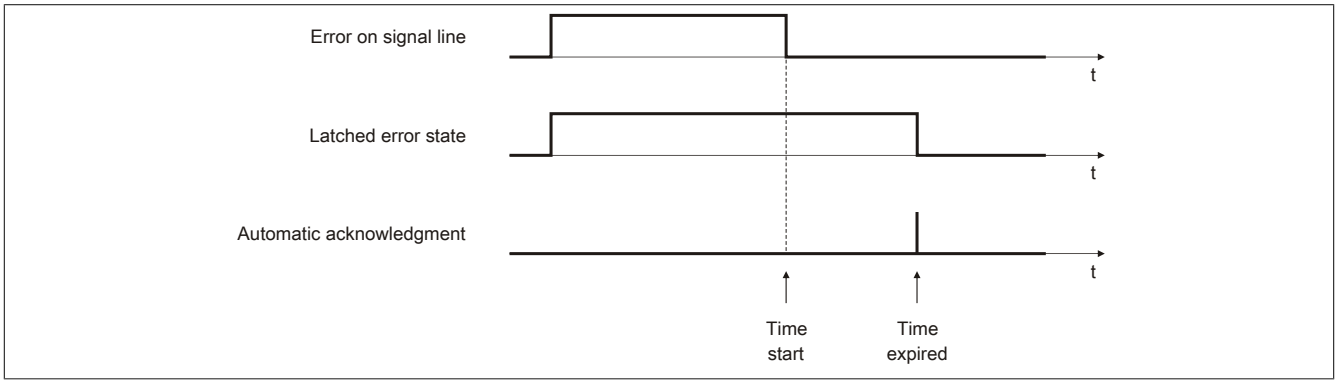


Figure 181: Latched error state acknowledged automatically

Example 2: Automatic and manual acknowledge used

An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged manually by the user before the time expires. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

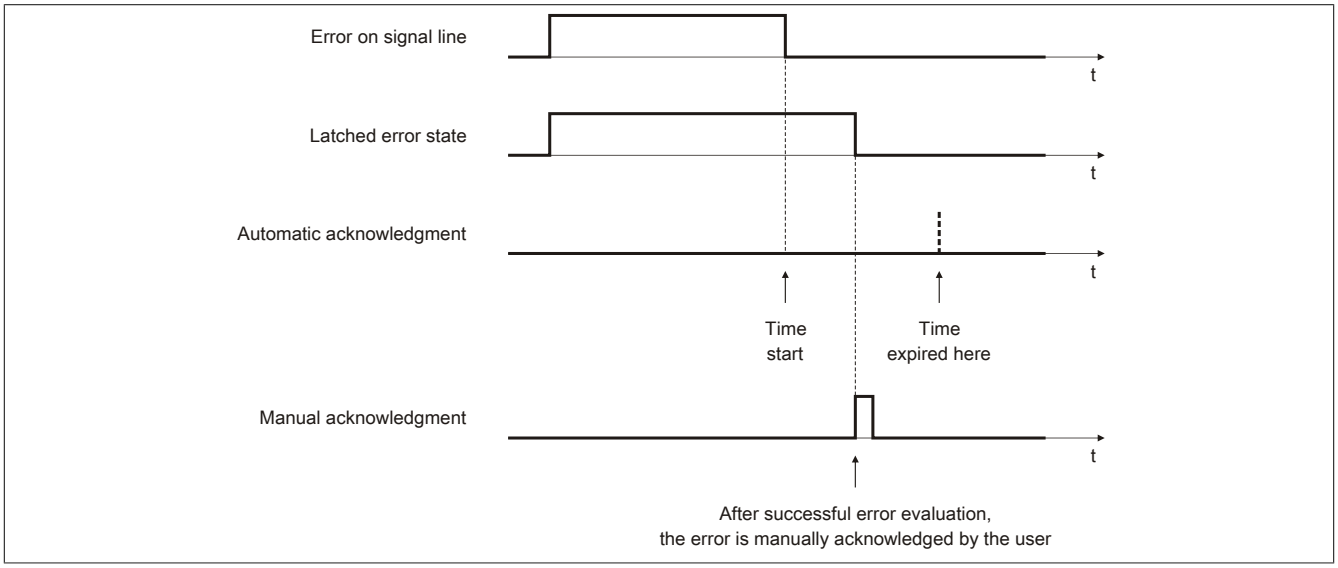


Figure 182: Automatic and manual acknowledge used

4.11.7.8.5.10 Status of encoder supplies

Name:
PowerSupply01 to PowerSupply02

This register shows the status of the integrated encoder supplies. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1	PowerSupply02	0	5 VDC encoder power supply OK
		1	5 VDC encoder power supply faulty
2 - 7	Reserved	-	

4.11.7.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.11.7.8.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
150 µs

4.11.8 X20DC1376

4.11.8.1 General information

The module is equipped with 1 input for an ABR incremental encoder with 24 V encoder signal. The encoder inputs are monitored (A, B, R).

- 1 ABR incremental encoder 24 V, asymmetric
- Encoder input monitoring
- 2 additional inputs, e.g. for latch input
- 24 VDC and GND for encoder supply

4.11.8.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1376	X20 digital counter module, 1 ABR incremental encoder, 24 V 100 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 182: X20DC1376 - Order data

4.11.8.3 Technical data

Product ID	X20DC1376
Short description	
I/O module	1 ABR incremental encoder 24 V
General information	
Input voltage	24 VDC (-15% / +20%)
B&R ID code	0xA705
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.3 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input voltage	24 VDC (-15% / +20%)
Input current at 24 VDC	Approx. 3.3 mA
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input circuit	Sink

Table 183: X20DC1376 - Technical data

Product ID	X20DC1376
Additional functions	Latch input
Input resistance	7.03 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Encoder inputs	24 V, asymmetrical (single-ended)
Counter size	16/32-bit
Input frequency	Max. 100 kHz
Evaluation	4x
Encoder supply	Module-internal, max. 600 mA
Input filter	
Hardware	≤1 µs
Software	-
Isolation voltage between encoder and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 183: X20DC1376 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.8.4 LED status indicators

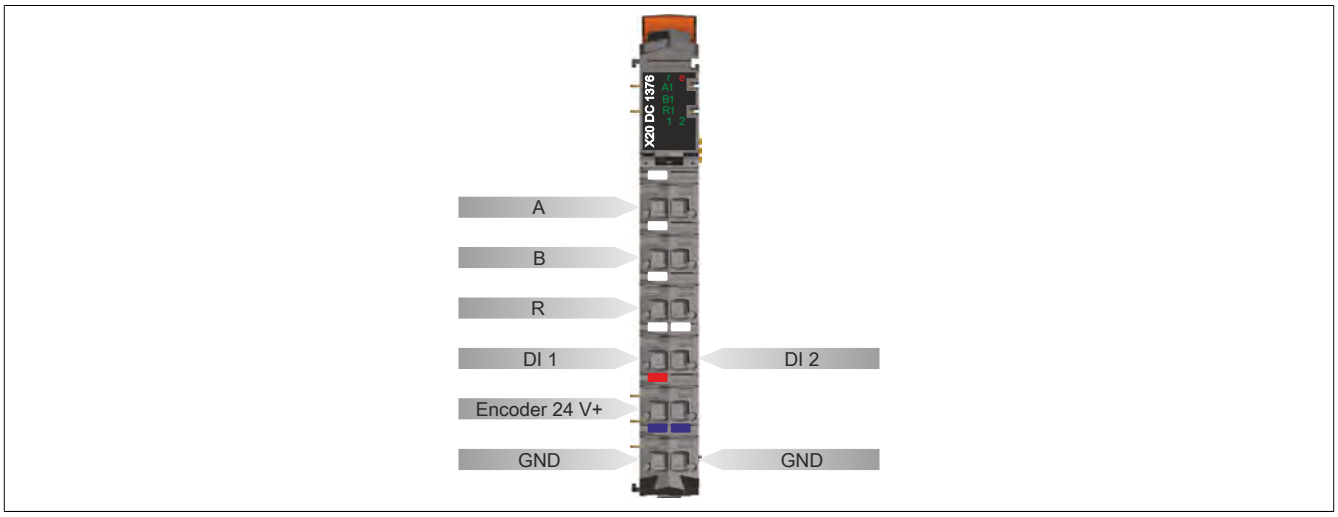
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	The encoder monitor has detected a line fault on the encoder inputs. The status bits must be evaluated in order to provide a more detailed definition of this error. The following error states are detected: • Open line • Short-circuit or voltage level too low
			On	Error or reset status
	A1	Green		Input state of counter input A
	B1	Green		Input state of counter input B
	R1	Green		Input state of reference pulse R
	1 - 2	Green		Input status - digital input

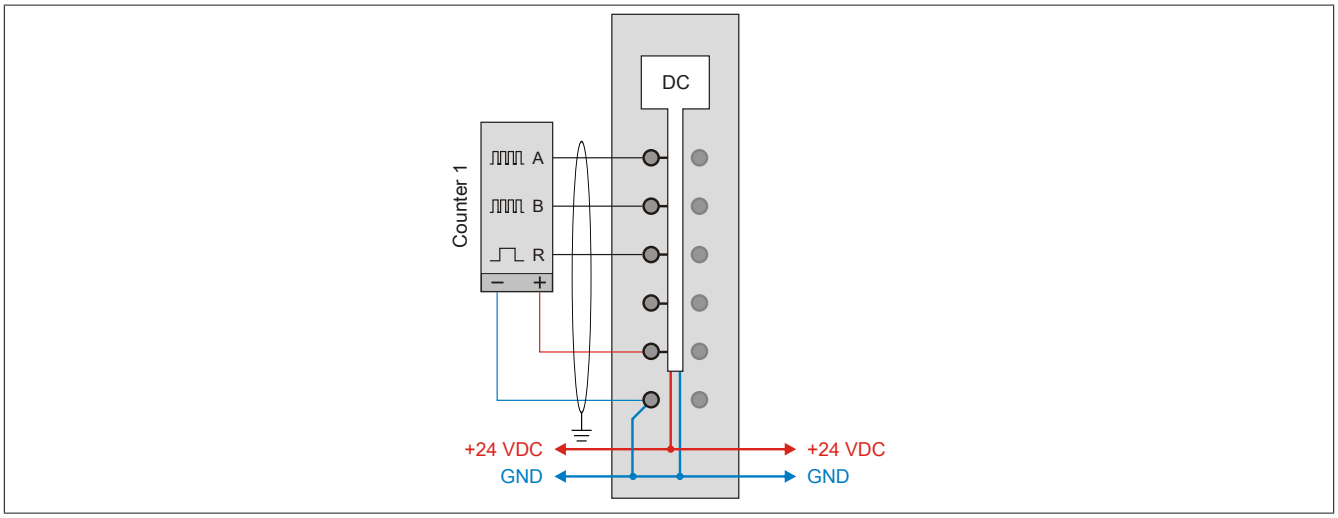
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.8.5 Pinout

Shielded cables must be used for all signal lines.

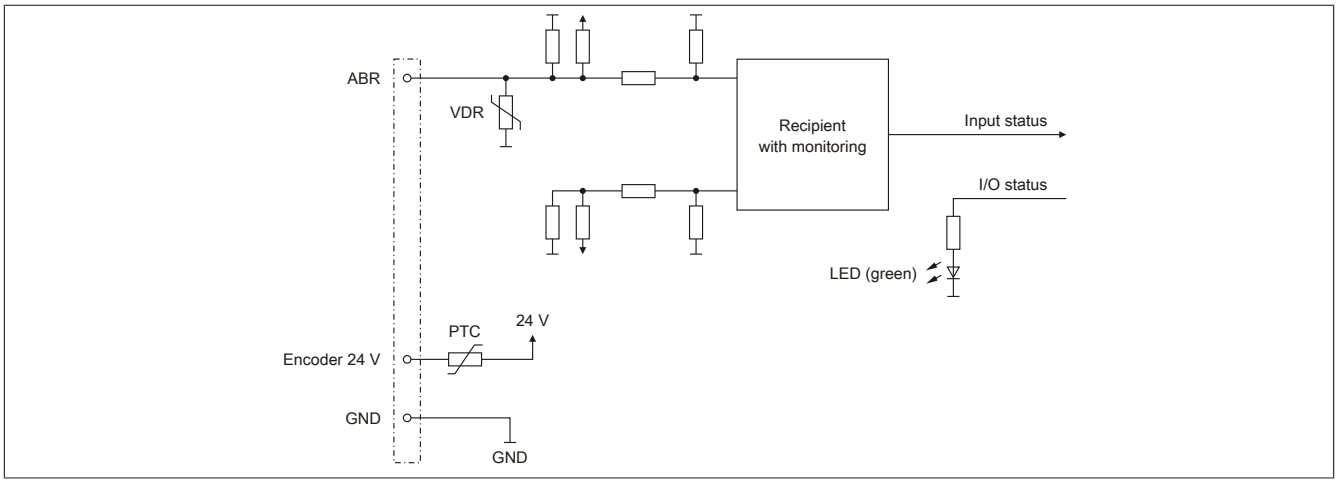


4.11.8.6 Connection example

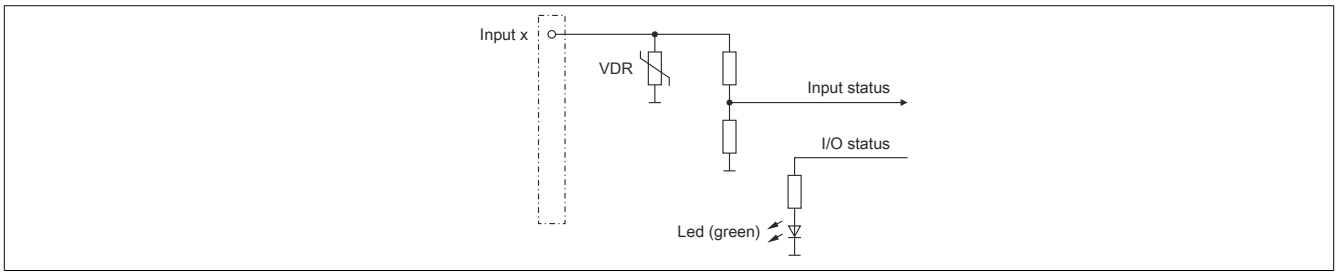


4.11.8.7 Input circuit diagram

Counter inputs



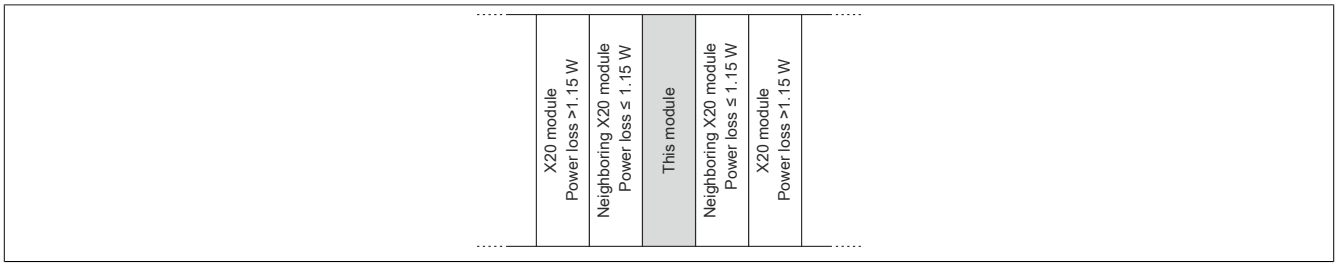
Standard inputs



4.11.8.8 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.11.8.9 Register description

4.11.8.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.8.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication						
683	SDCLifeCount	SINT	•			
6342	Encoder01	INT	•			
6340		DINT				
6310	Encoder01TimeValid	INT	•			
6308		DINT				
6358	Encoder01Latch	INT	•			
6356		DINT				
6153	Encoder commands	USINT			•	
	Encoder01Reset	Bit 0				
	Encoder01LatchEnable	Bit 1				
927	Input status of signal lines	USINT	•			
	Encoder01_A	Bit 0				
	Encoder01_B	Bit 1				
	Encoder01_R	Bit 2				
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
847	Status of signal lines	USINT	•			
	BW_Channel_A	Bit 0				
	BW_Channel_B	Bit 1				
	BW_Channel_R	Bit 2				
811	Acknowledging error status of signal lines	USINT			•	
	BW_QuitChannel_A	Bit 0				
	BW_QuitChannel_B	Bit 1				
	BW_QuitChannel_R	Bit 2				
6326	Encoder01TimeChanged	INT	•			
6324		DINT				
6303	Encoder01LatchCount	SINT	•			
843	Status of encoder supply	USINT	•			
	PowerSupply01	Bit 0				
Encoder - Configuration						
513	CfO_SIframeGenID	USINT				•
642	CfO_SystemCycleTime	UINT				•
769	CfO_PhyIOConfigCh01	USINT				•
771	CfO_PhyIOConfigCh02	USINT				•
773	CfO_PhyIOConfigCh03	USINT				•
777	CfO_PhyIOConfigCh04	USINT				•
779	CfO_PhyIOConfigCh05	USINT				•
815	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	CfO_BWQuitTime_0	UDINT				•
6145	CfO_CounterCycleSelect	USINT				•
6147	CfO_CounterMode	USINT				•
6149	CfO_LatchMode	USINT				•
6151	CfO_LatchComparator	USINT				•
6159	CfO_BWCNTEnableMaskChannel7_0	USINT				•

4.11.8.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication							
6342	0	Encoder01	INT	•			
6310	2	Encoder01TimeValid	INT	•			
6358	4	Encoder01Latch	INT	•			
6153	1	Encoder commands	USINT			•	
		Encoder01Reset	Bit 0				
		Encoder01LatchEnable	Bit 1				
927	7	Input status of signal lines	USINT	•			
		Encoder01_A	Bit 0				
		Encoder01_B	Bit 1				
		Encoder01_R	Bit 2				
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
847	6	Status of signal lines	USINT	•			
		BW_Channel_A	Bit 0				
		BW_Channel_B	Bit 1				
		BW_Channel_R	Bit 2				
811	0	Acknowledging error status of signal lines	USINT			•	
		BW_QuitChannel_A	Bit 0				
		BW_QuitChannel_B	Bit 1				
		BW_QuitChannel_R	Bit 2				
6326	-	Encoder01TimeChanged	INT		•		
6303	-	Encoder01LatchCount	SINT		•		
843	-	Status of encoder supply	USINT		•		
		PowerSupply01	Bit 0				
Encoder - Configuration							
513	-	CfO_SIframeGenID	USINT				•
642	-	CfO_SystemCycleTime	UINT				•
769	-	CfO_PhyIOConfigCh01	USINT				•
771	-	CfO_PhyIOConfigCh02	USINT				•
773	-	CfO_PhyIOConfigCh03	USINT				•
777	-	CfO_PhyIOConfigCh04	USINT				•
779	-	CfO_PhyIOConfigCh05	USINT				•
815	-	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	-	CfO_BWQuitTime_0	UDINT				•
6145	-	CfO_CounterCycleSelect	USINT				•
6147	-	CfO_CounterMode	USINT				•
6149	-	CfO_LatchMode	USINT				•
6151	-	CfO_LatchComparator	USINT				•
6159	-	CfO_BWCNTEnableMaskChannel7_0	USINT				•

1) The offset specifies the position of the register within the CAN object.

4.11.8.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.8.9.4 Encoder - Configuration

The following registers are used for setting functions and configuring the module.

4.11.8.9.4.1 Enabling error monitoring for the signal lines

Name:
CfO_BWCNTEnableMaskChannel7_0

This register requires individually enabling error monitoring for each of the signal channels. "Open line", "short circuit" and "voltage level too low" are reported as error states. Any errors that occur are reported in the error status registers BW_Channel_x.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Enable error monitoring for signal A lines	0	Error monitoring - Encoder Signal A disabled
		1	Error monitoring - Encoder Signal A enabled - Only default in bus controller function model
1	Enable error monitoring for signal B lines	0	Error monitoring - Encoder Signal B disabled
		1	Error monitoring - Encoder Signal B enabled - Only default in bus controller function model
2	Enable error monitoring for signal R lines	0	Error monitoring - Encoder Signal R disabled
		1	Error monitoring - Encoder Signal R enabled - Only default in bus controller function model
3 - 7	Reserved	0	

4.11.8.9.4.2 Timing for automatic error acknowledgment

Name:
CfO_BWQuitTime_0

This register can be used to enable an additional automatic acknowledgment of the error status through timing. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Data type	Value	Information
UDINT	0	No automatic acknowledgment - Only default in bus controller function model
	1 to 2.147.483.647	Time for automatic acknowledgment [µs]

4.11.8.9.4.3 Setting the latch mode

Name:
CfO_LatchMode

This register is used to set the latch mode:

- Single shot latch mode:
  The latch function must be enabled/set. After a successful latch procedure, the activation must be reset in order for a new latch procedure to be activated.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired.

A changed counter state on Encoder01LatchCount indicates that the latch procedure has been performed. The counter value is stored in the latch register Encoder01Latch.

Data type	Value	Information
USINT	0	Single shot latch procedure
	1	Continuous latch procedure

4.11.8.9.4.4 Signal channels for triggering latch procedure

Name:
CfO_LatchComparator

This register defines the signal channels and their level for triggering the latch procedure.

- This mainly configures which channels are linked to generate the latch event. All three signals from the encoder and digital input 1 can be used for the "AND" operation.
- The "active voltage level" needed for the latch procedure can now be used according to the physical signals.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Defines signal level for encoder signal A	0	Low
		1	High
1	Defines signal level for encoder signal B	0	Low
		1	High
2	Defines signal level for encoder signal R	0	Low
		1	High
3	Defines signal level for digital input 1	0	Low
		1	High
4	Use encoder signal A to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal A
5	Use encoder signal B to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal B
6	Use encoder signal R to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal R
7	Use digital input 1 to trigger latch procedure	0	Disabled
		1	Latch function linked to digital input 1

4.11.8.9.4.5 Physical configuration

The following registers must be set to the specified constant value for correct physical configuration:

Constant register "CfO_SIframeGenID"

Name:
CfO_SIframeGenID

Data type	Value	Information
USINT	9	Only default in the bus controller module

Constant register "CfO_SystemCycleTime"

Name:
CfO_SystemCycleTime

Cycle time of encoder acquisition in 1/8 µs steps. 1 encoder value is acquired as the counter value per cycle.

Data type	Value	Information
UINT	800	800 = 100 µs; only default in the bus controller module

Constant register "CfO_PhyIOConfigCh01"

Name:
CfO_PhyIOConfigCh01

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh02"

Name:
CfO_PhyIOConfigCh02

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh03"

Name:
CfO_PhyIOConfigCh03

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh04"

Name:
CfO_PhyIOConfigCh04

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh05"

Name:
CfO_PhyIOConfigCh05

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_BWQuitTimeSelChannel7_0"

Name:
CfO_BWQuitTimeSelChannel7_0

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_CounterCycleSelect"

Name:
CfO_CounterCycleSelect

Data type	Value	Information
USINT	2	Only default in the bus controller module

Constant register "CfO_CounterMode"

Name:
CfO_CounterMode

Data type	Value	Information
USINT	3	Only default in the bus controller module

4.11.8.9.5 Encoder - Communication

4.11.8.9.5.1 Counter for verifying the data frame

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.11.8.9.5.2 Display of the counter state

Name:
Encoder01

The counter state of the incremental encoder is displayed as a 16 or 32-bit counter value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.8.9.5.3 Net time of the last valid counter value

Name:
Encoder01TimeValid

The net time of the last valid counter value is the time of the last valid counter value (see "Cfo_SystemCycleTime" register) recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The net time of the last valid counter value that was read is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in milliseconds.
DINT[1)]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

4.11.8.9.5.4 Net time of the last counter value change

Name:
Encoder01TimeChanged

For slow X2X Link cycles, the net time of the last counter value change can be used to more accurately determine the speed.

The net time of the last counter value change is displayed as 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µsec.
DINT[1)]	-2.147.483.648 bis 2.147.483.647	

1) Can only be configured in the standard function model

4.11.8.9.5.5 Counter value at the time of the last latch

Name:
Encoder01Latch

The counter value at the time of the last latch is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.8.9.5.6 Counter value of latch event

Name:
Encoder01LatchCount

The latch events are counted and stored in a cyclic 8-bit counter. This counter is incremented with each latch event, thereby indicating a new occurrence. The new latched counter value is stored in the respective latch register.

Data type	Value
SINT	-128 to 127

4.11.8.9.5.7 Encoder commands

Name:
Encoder01Command

This register can be used to

1 reset the counter value. The counter is kept at zero until this command is reset.
2 enable the latch procedure. If the latch configuration is valid and matches the hardware signals, then this activation causes the counter value to be saved in the latch register.

The two different latch configurations that are possible (see section 4.11.3.8.4.3 "Setting the latch mode") must be handled as follows:

- Single shot latch mode:
  After successful latching, indicated by the latch event counter, activation must be reset before any more latching is possible. The activation must be set again if additional latching is needed.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired. The latch event counter is incremented with each event.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01Reset	0	Do not reset
		1	Set encoder value to 0
1	Encoder01LatchEnable	0	Do not activate latch
		1	Latching
2 - 7	Reserved	0	

4.11.8.9.5.8 Input status of signal lines

Name:
Encoder01_A
Encoder01_B
Encoder01_R
DigitalInput01 to DigitalInput02

This register displays the input status of the signal lines from the encoder and the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01_A	0/1	Input state of encoder signal A
1	Encoder01_B	0/1	Input state of encoder signal B
2	Encoder01_R	0/1	Input state of encoder signal R
3	Reserved	0	
4	DigitalInput01	0/1	Input state - Digital input 1
5	DigitalInput02	0/1	Input state - Digital input 2
6 - 7	Reserved	0	

4.11.8.9.5.9 Error status of signal lines

The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Status of signal lines

Name:
BW_Channel_A
BW_Channel_B
BW_Channel_R

This register displays the error states of the signal lines from the encoder. The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_Channel_A	0	No error in encoder signal A
		1	Open line, short circuit or voltage level too low
1	BW_Channel_B	0	No error in encoder signal B
		1	Open line, short circuit or voltage level too low
2	BW_Channel_R	0	No error in encoder signal R
		1	Open line, short circuit or voltage level too low
3 - 7	Reserved	0	

Acknowledging error status of signal lines

Name:
BW_QuitChannel_A
BW_QuitChannel_B
BW_QuitChannel_R

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_QuitChannel_A	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal A
1	BW_QuitChannel_B	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal B
2	BW_QuitChannel_R	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal R
3 - 7	Reserved	0	

Manual acknowledgment of latched error states

The latched error states of the signal lines from the encoder can be acknowledged manually. However, if there are still pending errors remaining, then the error status remains active. After successfully acknowledging the errors (latched error status = 0), the acknowledge bits must still be reset by the user or else a re-occurrence of an error could be overlooked by the user.

Example 1: **Cause of error corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user after the cause of error has been corrected. The latched error status changes to zero.

The manual acknowledge must now be reset so that any new errors will be recognized by the user.

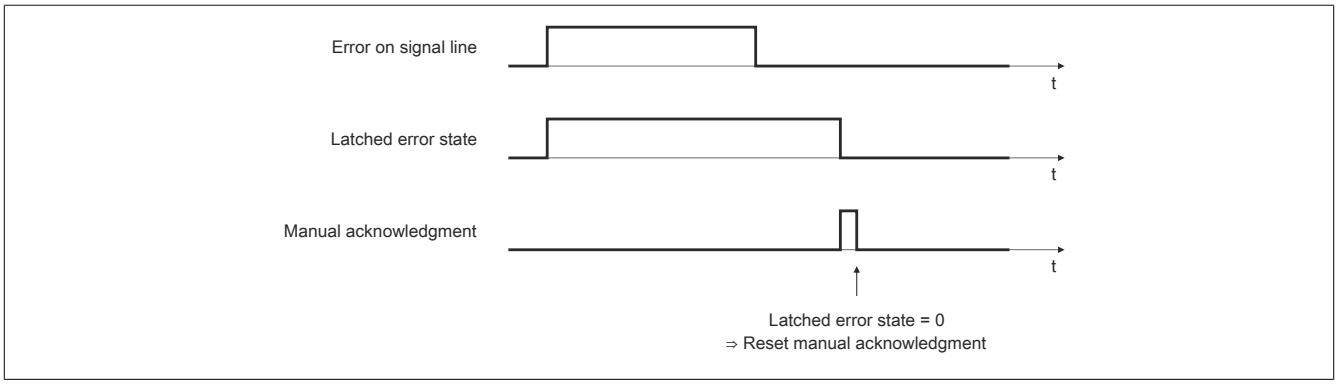


Figure 183: Cause of error corrected before being acknowledged

Example 2: **Cause of error not yet corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user before the cause of error has been corrected. The latched error status remains set because the error is still remaining.

Acknowledgment is only successful after the cause of error has been corrected. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

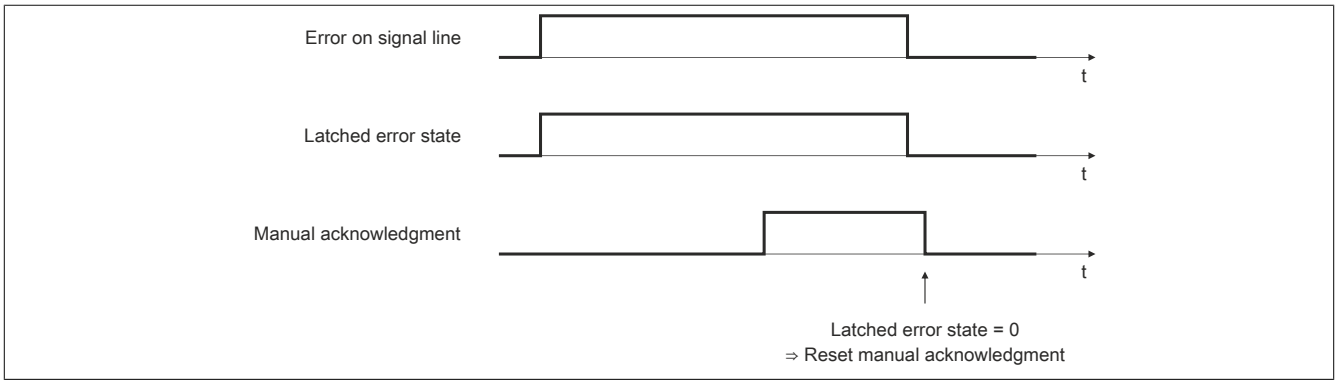


Figure 184: Cause of error not yet corrected before being acknowledged

Automatic acknowledgment of latched error states

In addition to manual acknowledgment, automatic acknowledgment of the latched error states after a specified amount of time can also be enabled. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages and for the validity of the counter value to be determined using its age.

If the time specification = 0, then only manual acknowledgment is possible.

Example 1: An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged as soon as the time expires. The latched error status changes to zero.

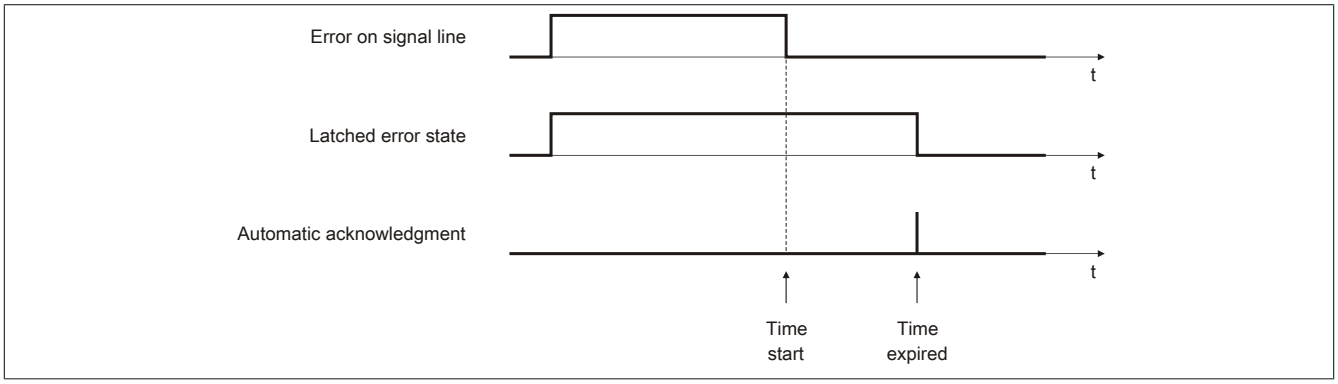


Figure 185: Latched error state acknowledged automatically

Example 2: Automatic and manual acknowledge used

An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged manually by the user before the time expires. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

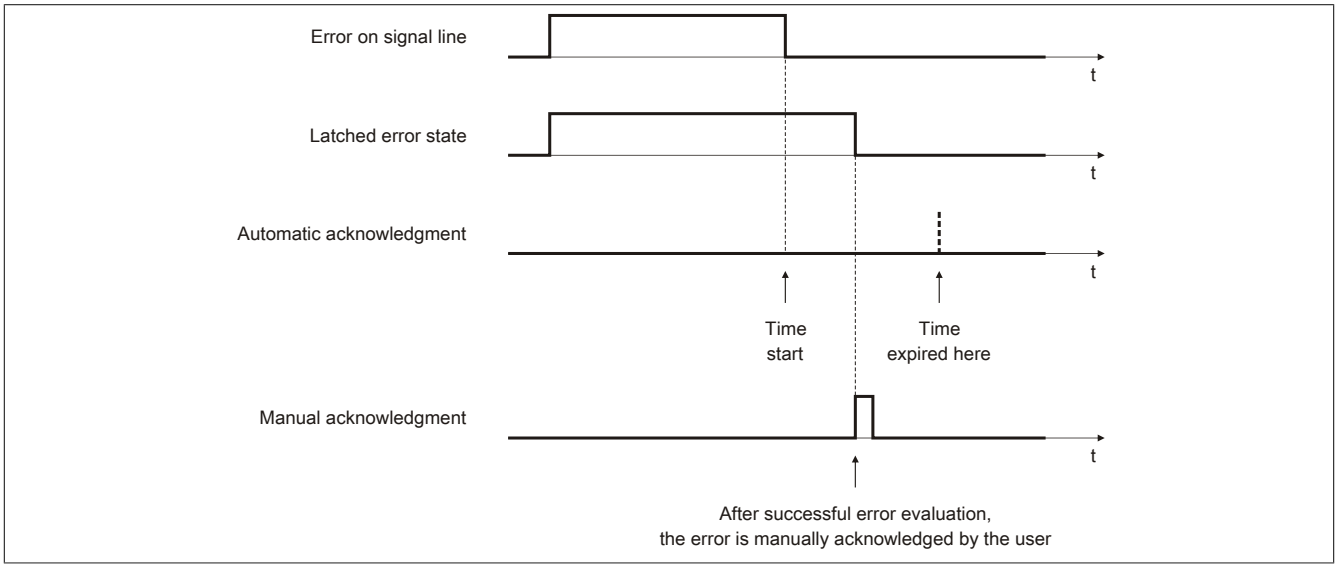


Figure 186: Automatic and manual acknowledge used

4.11.8.9.5.10 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.11.8.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.11.8.9.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
150 µs

4.11.9 X20DC137A

4.11.9.1 General information

The module is equipped with 1 input for an ABR incremental encoder with 24 V differential signals. The encoder inputs are monitored (A, B, R, A\, B\, R\).

- 1 ABR incremental encoder 24 V, differential
- Encoder input monitoring
- 2 additional inputs, e.g. for latch input
- 24 VDC and GND for encoder supply

4.11.9.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC137A	X20 digital counter module, 1x ABR incremental encoder, 24 V (differential), 300 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 184: X20DC137A - Order data

4.11.9.3 Technical data

Product ID	X20DC137A
Short description	
I/O module	1 ABR incremental encoder 24 V, differential
General information	
B&R ID code	0xDD28
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input voltage	24 VDC (-15% / +20%)
Input current at 24 VDC	Approx. 3.3 mA
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input circuit	Sink
Additional functions	Latch input
Input resistance	7.03 kΩ

Table 185: X20DC137A - Technical data

Product ID	X20DC137A
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Encoder inputs	24 V, differential
Counter size	16/32-bit
Input frequency	Max. 300 kHz
Evaluation	4x
Encoder supply	Module-internal, max. 600 mA
Input filter	
Hardware	≤0.5 µs
Software	-
Common-mode range	-10 V ≤ V_{CM} ≤ +13 V
Overload behavior of the encoder supply	Short circuit protection, overload protection
Isolation voltage between encoder and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 185: X20DC137A - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.9.4 LED status indicators

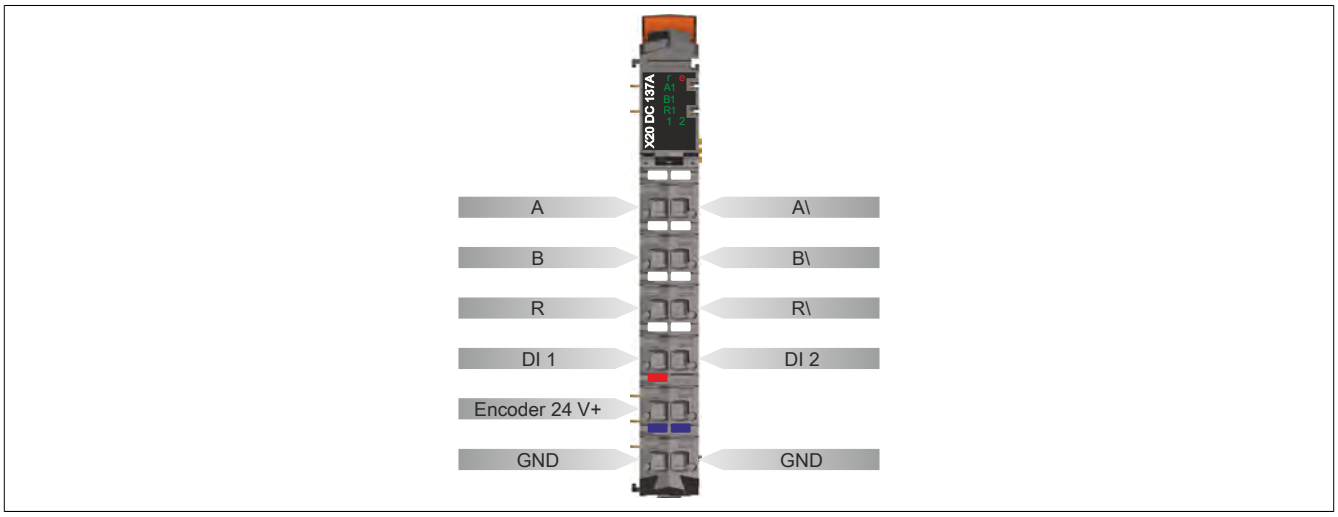
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	The encoder monitor has detected a line fault on the encoder inputs. The status bits must be evaluated in order to provide a more detailed definition of this error. The following error states are detected: • Open line • Short-circuit or voltage level too low
			On	Error or reset status
	A1	Green		Input state of counter input A
	B1	Green		Input state of counter input B
	R1	Green		Input state of reference pulse R
	1 - 2	Green		Input state of the corresponding digital input

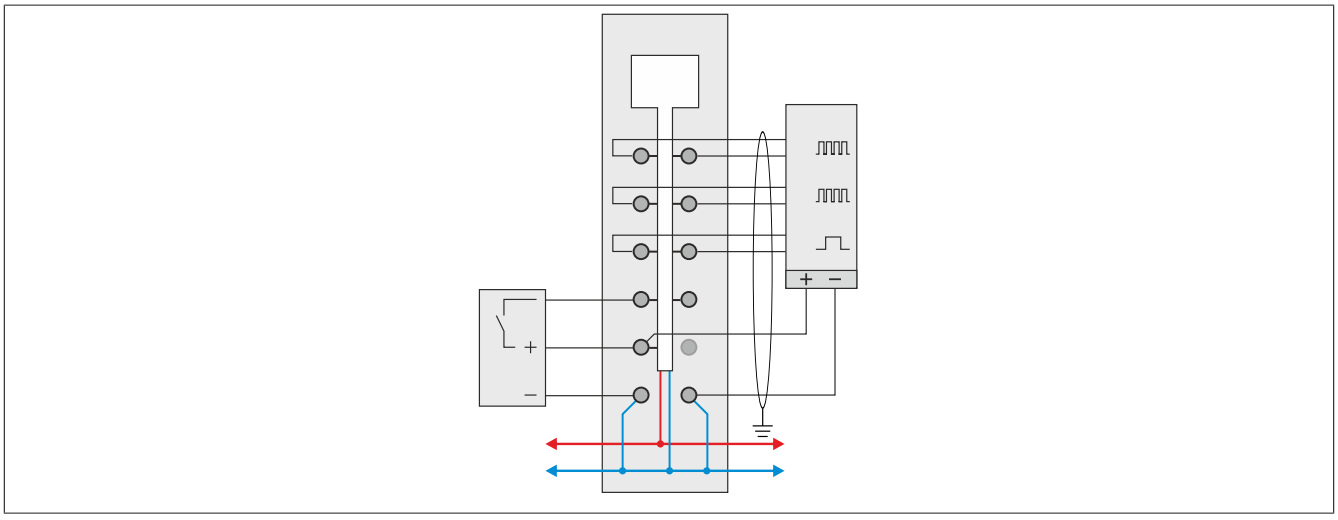
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.9.5 Pinout

Shielded cables must be used for all signal lines.

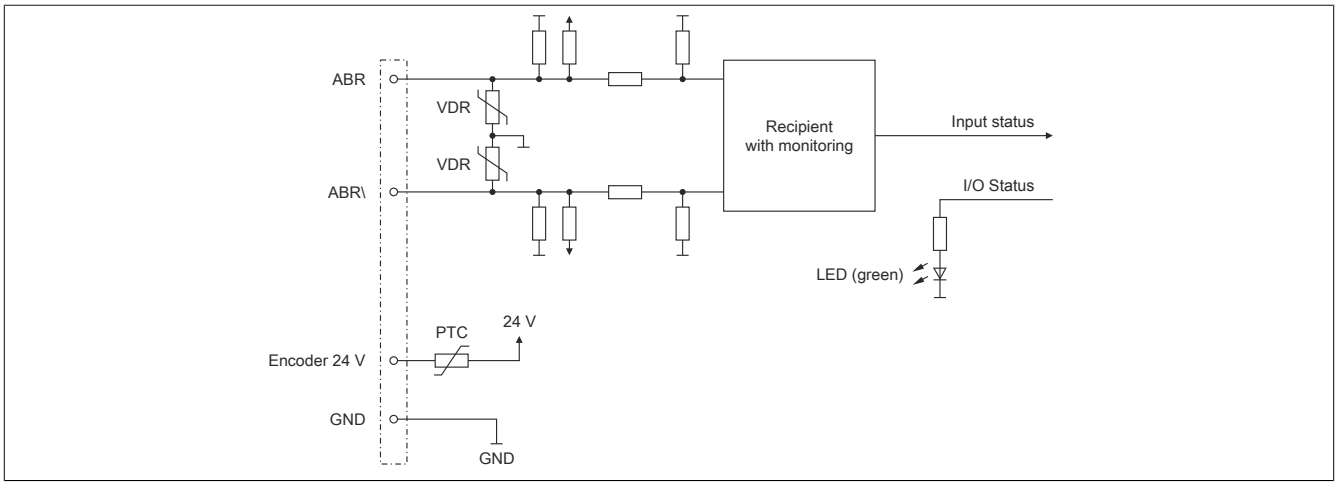


4.11.9.6 Connection example

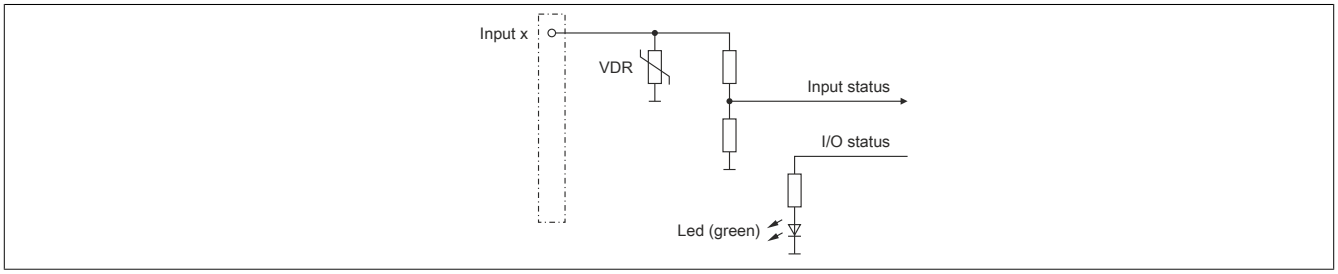


4.11.9.7 Input circuit diagram

Counter inputs



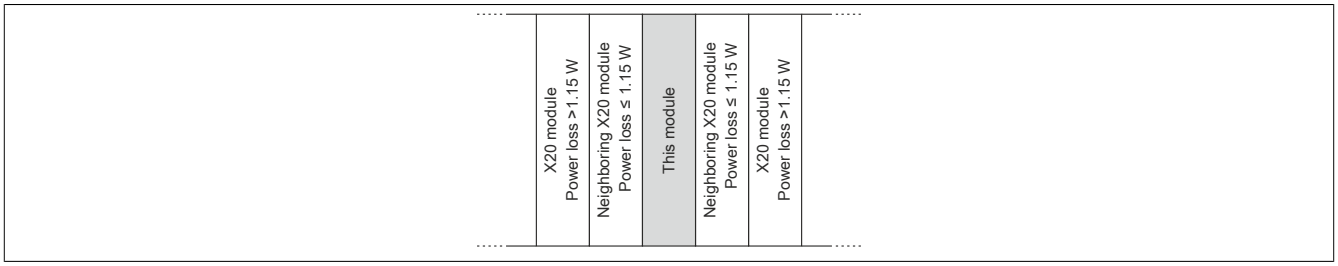
Standard inputs



4.11.9.8 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.11.9.9 Register description

4.11.9.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.9.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication						
683	SDCLifeCount	SINT	•			
6342	Encoder01	INT	•			
6340		DINT				
6310	Encoder01TimeValid	INT	•			
6308		DINT				
6358	Encoder01Latch	INT	•			
6356		DINT				
6153	Encoder commands	USINT			•	
	Encoder01Reset	Bit 0				
	Encoder01LatchEnable	Bit 1				
927	Input status of signal lines	USINT	•			
	Encoder01_A	Bit 0				
	Encoder01_B	Bit 1				
	Encoder01_R	Bit 2				
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
847	Status of signal lines	USINT	•			
	BW_Channel_A	Bit 0				
	BW_Channel_B	Bit 1				
	BW_Channel_R	Bit 2				
811	Acknowledging error status of signal lines	USINT			•	
	BW_QuitChannel_A	Bit 0				
	BW_QuitChannel_B	Bit 1				
	BW_QuitChannel_R	Bit 2				
6326	Encoder01TimeChanged	INT	•			
6324		DINT				
6303	Encoder01LatchCount	SINT	•			
843	Status of encoder supply	USINT	•			
	PowerSupply01	Bit 0				
Encoder - Configuration						
513	CfO_SIframeGenID	USINT				•
642	CfO_SystemCycleTime	UINT				•
769	CfO_PhyIOConfigCh01	USINT				•
771	CfO_PhyIOConfigCh02	USINT				•
773	CfO_PhyIOConfigCh03	USINT				•
777	CfO_PhyIOConfigCh04	USINT				•
779	CfO_PhyIOConfigCh05	USINT				•
815	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	CfO_BWQuitTime_0	UDINT				•
6145	CfO_CounterCycleSelect	USINT				•
6147	CfO_CounterMode	USINT				•
6149	CfO_LatchMode	USINT				•
6151	CfO_LatchComparator	USINT				•
6159	CfO_BWCNTEnableMaskChannel7_0	USINT				•

4.11.9.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication							
6342	0	Encoder01	INT	•			
6310	2	Encoder01TimeValid	INT	•			
6358	4	Encoder01Latch	INT	•			
6153	1	Encoder commands	USINT			•	
		Encoder01Reset	Bit 0				
		Encoder01LatchEnable	Bit 1				
927	7	Input status of signal lines	USINT	•			
		Encoder01_A	Bit 0				
		Encoder01_B	Bit 1				
		Encoder01_R	Bit 2				
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
847	6	Status of signal lines	USINT	•			
		BW_Channel_A	Bit 0				
		BW_Channel_B	Bit 1				
		BW_Channel_R	Bit 2				
811	0	Acknowledging error status of signal lines	USINT			•	
		BW_QuitChannel_A	Bit 0				
		BW_QuitChannel_B	Bit 1				
		BW_QuitChannel_R	Bit 2				
6326	-	Encoder01TimeChanged	INT		•		
6303	-	Encoder01LatchCount	SINT		•		
843	-	Status of encoder supply	USINT		•		
		PowerSupply01	Bit 0				
Encoder - Configuration							
513	-	CfO_SIframeGenID	USINT				•
642	-	CfO_SystemCycleTime	UINT				•
769	-	CfO_PhyIOConfigCh01	USINT				•
771	-	CfO_PhyIOConfigCh02	USINT				•
773	-	CfO_PhyIOConfigCh03	USINT				•
777	-	CfO_PhyIOConfigCh04	USINT				•
779	-	CfO_PhyIOConfigCh05	USINT				•
815	-	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	-	CfO_BWQuitTime_0	UDINT				•
6145	-	CfO_CounterCycleSelect	USINT				•
6147	-	CfO_CounterMode	USINT				•
6149	-	CfO_LatchMode	USINT				•
6151	-	CfO_LatchComparator	USINT				•
6159	-	CfO_BWCNTEnableMaskChannel7_0	USINT				•

1) The offset specifies the position of the register within the CAN object.

4.11.9.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.9.9.4 Encoder - Configuration

The following registers are used for setting functions and configuring the module.

4.11.9.9.4.1 Enabling error monitoring for the signal lines

Name:
CfO_BWCNTEnableMaskChannel7_0

This register requires individually enabling error monitoring for each of the signal channels. "Open line", "short circuit" and "voltage level too low" are reported as error states. Any errors that occur are reported in the error status registers BW_Channel_x.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Enable error monitoring for signal A lines	0	Error monitoring - Encoder Signal A disabled
		1	Error monitoring - Encoder Signal A enabled - Only default in bus controller function model
1	Enable error monitoring for signal B lines	0	Error monitoring - Encoder Signal B disabled
		1	Error monitoring - Encoder Signal B enabled - Only default in bus controller function model
2	Enable error monitoring for signal R lines	0	Error monitoring - Encoder Signal R disabled
		1	Error monitoring - Encoder Signal R enabled - Only default in bus controller function model
3 - 7	Reserved	0	

4.11.9.9.4.2 Timing for automatic error acknowledgment

Name:
CfO_BWQuitTime_0

This register can be used to enable an additional automatic acknowledgment of the error status through timing. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Data type	Value	Information
UDINT	0	No automatic acknowledgment - Only default in bus controller function model
	1 to 2.147.483.647	Time for automatic acknowledgment [µs]

4.11.9.9.4.3 Setting the latch mode

Name:
CfO_LatchMode

This register is used to set the latch mode:

- Single shot latch mode:
  The latch function must be enabled/set. After a successful latch procedure, the activation must be reset in order for a new latch procedure to be activated.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired.

A changed counter state on Encoder01LatchCount indicates that the latch procedure has been performed. The counter value is stored in the latch register Encoder01Latch.

Data type	Value	Information
USINT	0	Single shot latch procedure
	1	Continuous latch procedure

4.11.9.9.4.4 Signal channels for triggering latch procedure

Name:
CfO_LatchComparator

This register defines the signal channels and their level for triggering the latch procedure.

- This mainly configures which channels are linked to generate the latch event. All three signals from the encoder and digital input 1 can be used for the "AND" operation.
- The "active voltage level" needed for the latch procedure can now be used according to the physical signals.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Defines signal level for encoder signal A	0	Low
		1	High
1	Defines signal level for encoder signal B	0	Low
		1	High
2	Defines signal level for encoder signal R	0	Low
		1	High
3	Defines signal level for digital input 1	0	Low
		1	High
4	Use encoder signal A to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal A
5	Use encoder signal B to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal B
6	Use encoder signal R to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal R
7	Use digital input 1 to trigger latch procedure	0	Disabled
		1	Latch function linked to digital input 1

4.11.9.9.4.5 Physical configuration

The following registers must be set to the specified constant value for correct physical configuration:

Constant register "CfO_SIframeGenID"

Name:
CfO_SIframeGenID

Data type	Value	Information
USINT	9	Only default in the bus controller module

Constant register "CfO_SystemCycleTime"

Name:
CfO_SystemCycleTime

Cycle time of encoder acquisition in 1/8 µs steps. 1 encoder value is acquired as the counter value per cycle.

Data type	Value	Information
UINT	800	800 = 100 µs; only default in the bus controller module

Constant register "CfO_PhyIOConfigCh01"

Name:
CfO_PhyIOConfigCh01

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh02"

Name:
CfO_PhyIOConfigCh02

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh03"

Name:
CfO_PhyIOConfigCh03

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh04"

Name:
CfO_PhyIOConfigCh04

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh05"

Name:
CfO_PhyIOConfigCh05

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_BWQuitTimeSelChannel7_0"

Name:
CfO_BWQuitTimeSelChannel7_0

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_CounterCycleSelect"

Name:
CfO_CounterCycleSelect

Data type	Value	Information
USINT	2	Only default in the bus controller module

Constant register "CfO_CounterMode"

Name:
CfO_CounterMode

Data type	Value	Information
USINT	3	Only default in the bus controller module

4.11.9.9.5 Encoder - Communication

4.11.9.9.5.1 Counter for verifying the data frame

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.11.9.9.5.2 Display of the counter state

Name:
Encoder01

The counter state of the incremental encoder is displayed as a 16 or 32-bit counter value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.9.9.5.3 Net time of the last valid counter value

Name:
Encoder01TimeValid

The net time of the last valid counter value is the time of the last valid counter value (see "Cfo_SystemCycleTime" register) recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The net time of the last valid counter value that was read is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in milliseconds.
DINT[1)]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

4.11.9.9.5.4 Net time of the last counter value change

Name:
Encoder01TimeChanged

For slow X2X Link cycles, the net time of the last counter value change can be used to more accurately determine the speed.

The net time of the last counter value change is displayed as 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µsec.
DINT[1)]	-2.147.483.648 bis 2.147.483.647	

1) Can only be configured in the standard function model

4.11.9.9.5.5 Counter value at the time of the last latch

Name:
Encoder01Latch

The counter value at the time of the last latch is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.9.9.5.6 Counter value of latch event

Name:
Encoder01LatchCount

The latch events are counted and stored in a cyclic 8-bit counter. This counter is incremented with each latch event, thereby indicating a new occurrence. The new latched counter value is stored in the respective latch register.

Data type	Value
SINT	-128 to 127

4.11.9.9.5.7 Encoder commands

Name:
Encoder01Command

This register can be used to

1 reset the counter value. The counter is kept at zero until this command is reset.
2 enable the latch procedure. If the latch configuration is valid and matches the hardware signals, then this activation causes the counter value to be saved in the latch register.

The two different latch configurations that are possible (see section 4.11.3.8.4.3 "Setting the latch mode") must be handled as follows:

- Single shot latch mode:
  After successful latching, indicated by the latch event counter, activation must be reset before any more latching is possible. The activation must be set again if additional latching is needed.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired. The latch event counter is incremented with each event.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01Reset	0	Do not reset
		1	Set encoder value to 0
1	Encoder01LatchEnable	0	Do not activate latch
		1	Latching
2 - 7	Reserved	0	

4.11.9.9.5.8 Input status of signal lines

Name:
Encoder01_A
Encoder01_B
Encoder01_R
DigitalInput01 to DigitalInput02

This register displays the input status of the signal lines from the encoder and the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01_A	0/1	Input state of encoder signal A
1	Encoder01_B	0/1	Input state of encoder signal B
2	Encoder01_R	0/1	Input state of encoder signal R
3	Reserved	0	
4	DigitalInput01	0/1	Input state - Digital input 1
5	DigitalInput02	0/1	Input state - Digital input 2
6 - 7	Reserved	0	

4.11.9.9.5.9 Error status of signal lines

The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Status of signal lines

Name:
BW_Channel_A
BW_Channel_B
BW_Channel_R

This register displays the error states of the signal lines from the encoder. The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_Channel_A	0	No error in encoder signal A
		1	Open line, short circuit or voltage level too low
1	BW_Channel_B	0	No error in encoder signal B
		1	Open line, short circuit or voltage level too low
2	BW_Channel_R	0	No error in encoder signal R
		1	Open line, short circuit or voltage level too low
3 - 7	Reserved	0	

Acknowledging error status of signal lines

Name:
BW_QuitChannel_A
BW_QuitChannel_B
BW_QuitChannel_R

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_QuitChannel_A	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal A
1	BW_QuitChannel_B	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal B
2	BW_QuitChannel_R	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal R
3 - 7	Reserved	0	

Manual acknowledgment of latched error states

The latched error states of the signal lines from the encoder can be acknowledged manually. However, if there are still pending errors remaining, then the error status remains active. After successfully acknowledging the errors (latched error status = 0), the acknowledge bits must still be reset by the user or else a re-occurrence of an error could be overlooked by the user.

Example 1: **Cause of error corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user after the cause of error has been corrected. The latched error status changes to zero.

The manual acknowledge must now be reset so that any new errors will be recognized by the user.

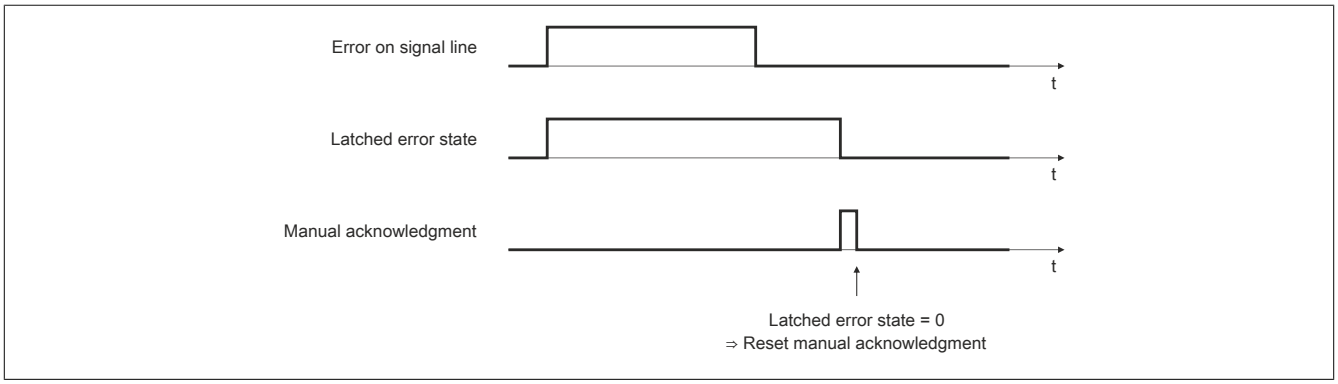


Figure 187: Cause of error corrected before being acknowledged

Example 2: **Cause of error not yet corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user before the cause of error has been corrected. The latched error status remains set because the error is still remaining.

Acknowledgment is only successful after the cause of error has been corrected. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

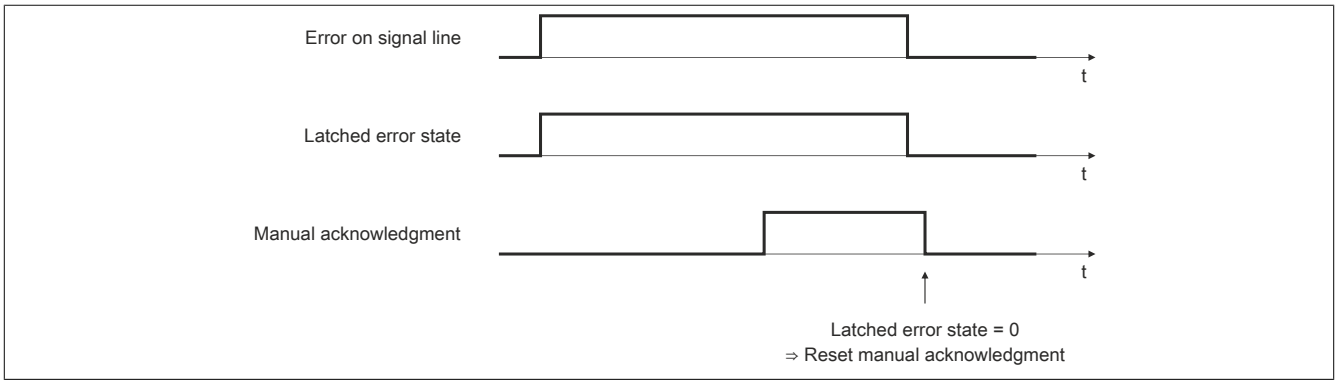


Figure 188: Cause of error not yet corrected before being acknowledged

Automatic acknowledgment of latched error states

In addition to manual acknowledgment, automatic acknowledgment of the latched error states after a specified amount of time can also be enabled. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages and for the validity of the counter value to be determined using its age.

If the time specification = 0, then only manual acknowledgment is possible.

Example 1: An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged as soon as the time expires. The latched error status changes to zero.

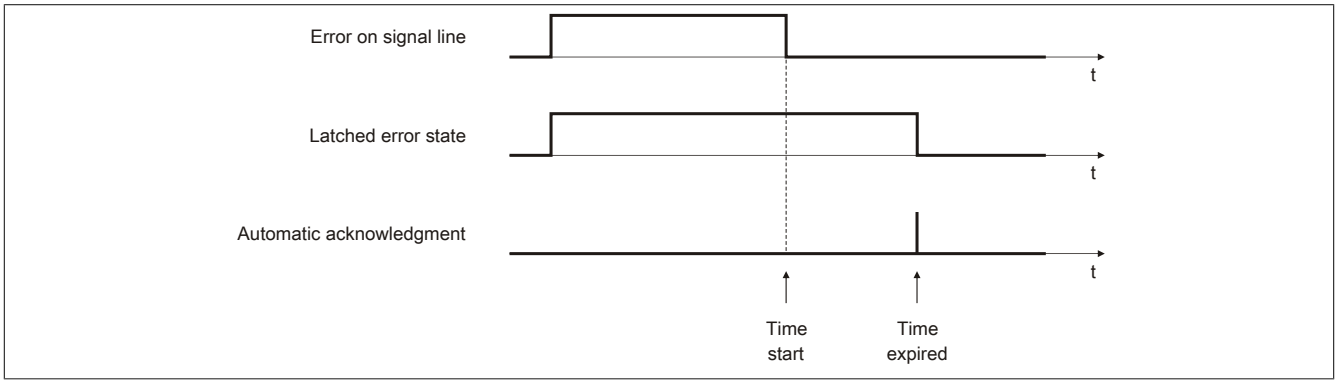


Figure 189: Latched error state acknowledged automatically

Example 2: Automatic and manual acknowledge used

An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged manually by the user before the time expires. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

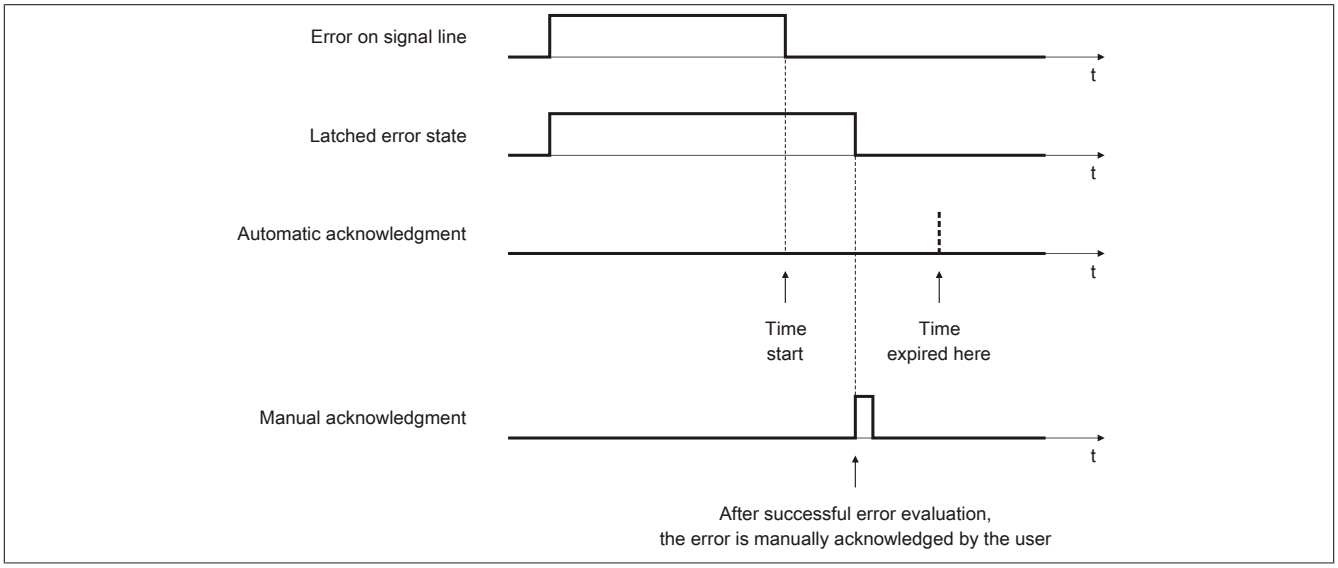


Figure 190: Automatic and manual acknowledge used

4.11.9.9.5.10 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.11.9.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.11.9.9.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
150 µs

4.11.10 X20(c)DC1396

4.11.10.1 General information

The module is equipped with 1 input for an ABR incremental encoder with 24 V encoder signal.

- 1 ABR incremental encoder 24 V
- 1 additional input e.g. for home enable switch
- 24 VDC and GND for encoder supply

4.11.10.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.11.10.3 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1396	X20 digital counter module, 1 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation	
X20cDC1396	X20 digital counter module, coated, 1 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 186: X20DC1396, X20cDC1396 - Order data

4.11.10.4 Technical data

Product ID	X20DC1396	X20cDC1396
Short description		
I/O module	1 ABR incremental encoder 24 V	
General information		
Input voltage	24 VDC -15 % / +20 %	
B&R ID code	0x1BAC	0xE502
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.4 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Encoder - Bus	Yes	
Reference enable switch - Bus	Yes	
Reference enable switch - Encoder	No	
Type of signal lines	Shielded cables must be used for all signal lines.	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Home enable switch		
Quantity	1	
Nominal voltage	24 VDC	
Input filter		
Hardware	≤2 µs	
Software	-	
Connection type	3-wire connections	
Input circuit	Sink	
Input current at 24 VDC	Approx. 3.3 mA	
Input resistance	7.19 kΩ	
Isolation voltage between home enable switch and bus	500 V_{eff}	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
ABR incremental encoder		
Encoder inputs	24 V, asymmetrical	
Counter size	16/32-bit	
Input frequency	Max. 100 kHz	
Evaluation	4x	
Encoder supply	Module-internal, max. 600 mA	
Input filter		
Hardware	≤2 µs	
Software	-	
Input current at 24 VDC	Approx. 1.3 mA	
Input resistance	18.4 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Overload behavior of the encoder supply	Short circuit protection, overload protection	
Isolation voltage between encoder and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	

Table 187: X20DC1396, X20cDC1396 - Technical data

Product ID	X20DC1396	X20cDC1396
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 187: X20DC1396, X20cDC1396 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.10.5 LED status indicators

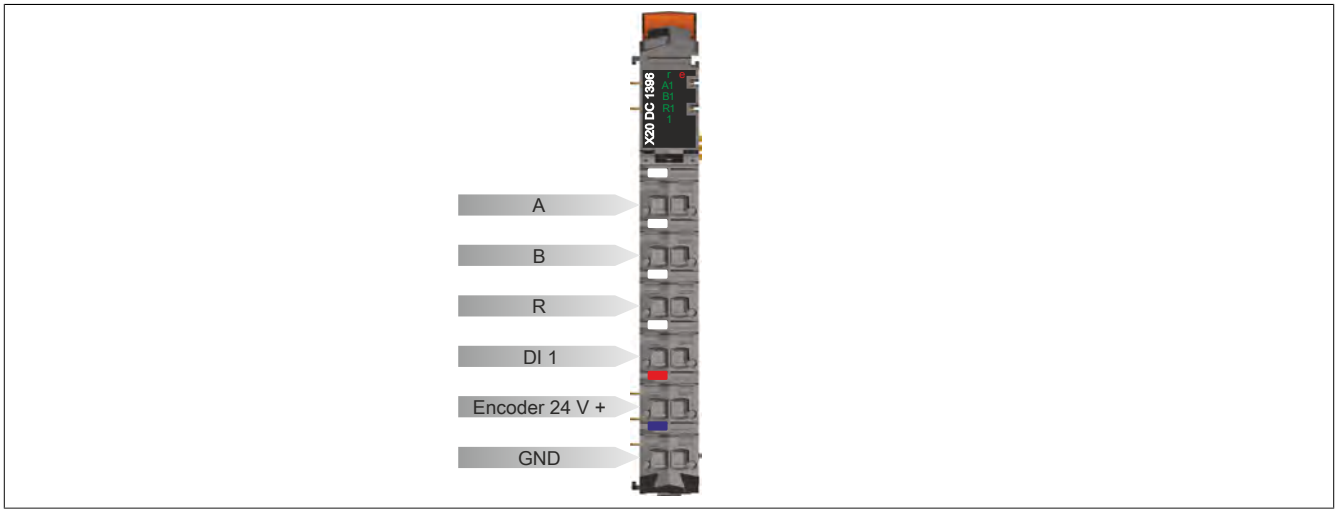
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	A1	Green		Input state of counter input A
	B1	Green		Input state of counter input B
	R1	Green		Input state of reference pulse R
	1	Green		Input state - Digital input

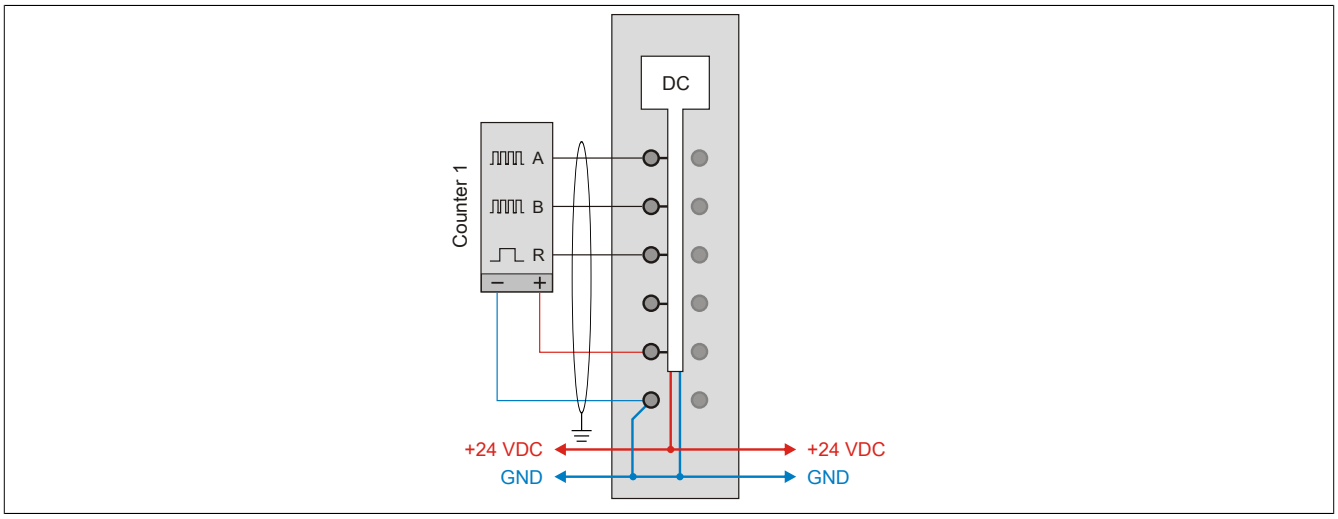
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.10.6 Pinout

Shielded cables must be used for all signal lines.

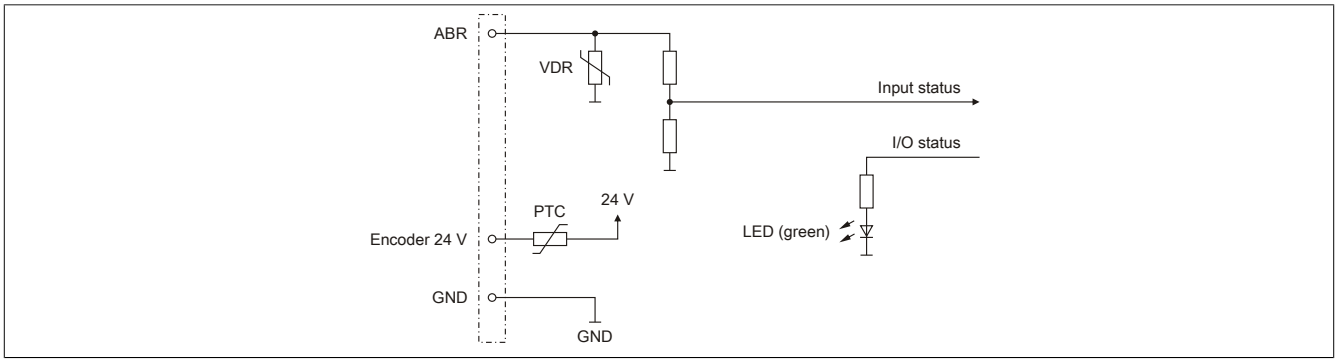


4.11.10.7 Connection example

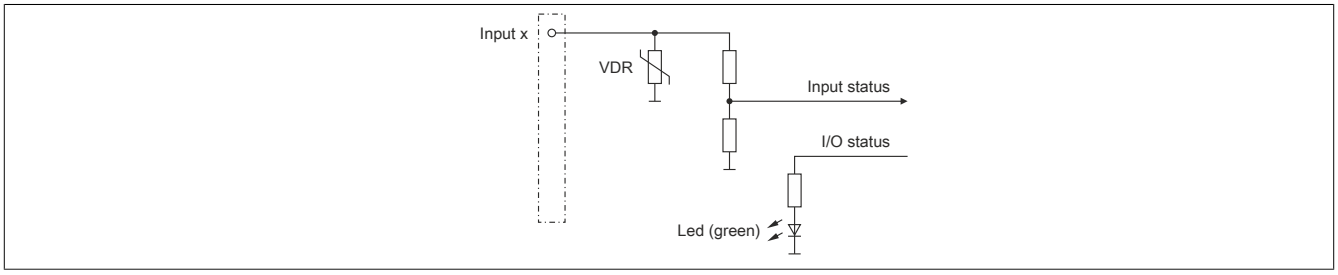


4.11.10.8 Input circuit diagram

Counter inputs



Standard input



4.11.10.9 Register description

4.11.10.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.10.9.2 Function model 0 - Standard and Function model 1 - Standard with 32-bit encoder counter value

The difference between function model 0 and function model 1 is the size of the data type for some registers.

- Function model 0 uses data type INT
- Function model 1 uses data type DINT (specified in parentheses)

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
4104	CfO_EdgeDetectFalling	USINT				•
4106	CfO_EdgeDetectRising	USINT				•
2064	CfO_PresetABR01_1(_32Bit)	(D)INT				•
2068	CfO_PresetABR01_2(_32Bit)	(D)INT				•
512	ConfigOutput24	UINT				•
522	ConfigOutput26	USINT				•
520	ConfigOutput27	USINT				•
Communication						
2116	ReferenceModeEncoder01	USINT			•	
2080	Encoder01	(D)INT	•			
264	Input state of the digital input	USINT	•			
	DigitalInput01	Bit 3				
2118	StatusInput01	USINT	•			
40	Status of encoder supply	USINT	•			
	PowerSupply01	Bit 0				

4.11.10.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
4104	-	CfO_EdgeDetectFalling	USINT				•
4106	-	CfO_EdgeDetectRising	USINT				•
2064	-	CfO_PresetABR01_1	INT				•
2068	-	CfO_PresetABR01_2	INT				•
512	-	ConfigOutput24	UINT				•
522	-	ConfigOutput26	USINT				•
520	-	ConfigOutput27	USINT				•
Communication							
2116	0	ReferenceModeEncoder01	USINT			•	
2080	0	Encoder01	INT	•			
264	2	Input state of the digital input	USINT	•			
		DigitalInput01	Bit 3				
2118	4	StatusInput01	USINT	•			
40	3	Status of encoder supply	USINT	•			
		PowerSupply01	Bit 0				

1) The offset specifies the position of the register within the CAN object.

4.11.10.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.10.9.4 ABR encoder - Configuration registers

4.11.10.9.4.1 Reference pulse

The following registers must be configured by a single acyclic write with the listed values so that the homing procedure is completed on the edge of the reference pulse.

The homing procedure can take place on:

- Rising edge
- Falling edge (default configuration)

Constant register "CfO_EdgeDetectFalling"

Name:

CfO_EdgeDetectFalling

Data type	Value	Filter
USINT	0x00	Configuration value for rising edge
	0x04	Configuration value for falling edge

Constant register "CfO_EdgeDetectRising"

Name:

CfO_EdgeDetectRising

Data type	Value	Filter
USINT	0x04	Configuration value for rising edge
	0x00	Configuration value for falling edge

Constant register "ConfigOutput24"

Name:

ConfigOutput24

This register contains the value for ABR encoder 1.

Data type	Value	Filter
UINT	0x1012	Configuration value for rising edge
	0x1002	Configuration value for falling edge

4.11.10.9.4.2 Setting the home position

Name:
Cfo_PresetABR01_1 to Cfo_PresetABR01_2

CfO_PresetABR01_1_32Bit to CfO_PresetABR01_2_32Bit (only in function model 1)

It is possible to specify two home positions with these registers through a one-off acyclic write, for example (default = 0). The configured values are applied to the counter values after a completed homing procedure.

Data type	Value
INT	-32,768 to 32,767
DINT[1)]	-2,147,483,648 to 2,147,483,647

1) Only in function model 1

4.11.10.9.4.3 Homing with reference enable input

Regardless of the referencing mode, it is possible using this register to prevent the home position from being applied when the corresponding reference input voltage level occurs (see 4.11.10.9.5.2 "Input state of the digital input": bit 3). The desired setting can be configured by a one-off acyclic write.

Voltage level for reference enable activation

Name:

ConfigOutput26

This register is used to configure the active voltage level of the digital input for the reference enable.

Data type	Value	Filter
USINT	0x00	Reference enable is active at 0 VDC
	0x08	Reference enable is active at 24 VDC

Reference enable of the input

Name:

ConfigOutput27

This register can be used to define whether the reference enable is activated.

Data type	Value	Filter
USINT	0x00	Reference enable input OFF (default)
	0x08	Reference enable input activated

4.11.10.9.5 ABR encoder - Configuration registers

4.11.10.9.5.1 Counter state of the encoder

Name:
Encoder01

The encoder values are represented as 16-bit or 32-bit counter values in this register.

Data type	Value
INT	-32,768 to 32,767
DINT[1)]	-2,147,483,648 to 2,147,483,647

1) Only in function model 1

4.11.10.9.5.2 Input state of the digital input

Name:
DigitalInput01

This register displays the input status of the encoder and the digital input.

Data type	Value
USINT	See bit structure.

Bit	Name	Value	Information
0	Encoder A	0 or 1	Input state
1	Encoder B	0 or 1	Input state
2	Encoder A + B	0 or 1	Input state of reference pulse
3	DigitalInput01	0 or 1	Input state - Digital input 1
4 - 7	Reserved	-	

4.11.10.9.5.3 Reading the referencing mode

Name:
ReferenceModeEncoder01

This register determines the referencing mode.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1		00	Referencing OFF
		01	Single shot referencing
		11	Continuous referencing
2 - 5		0	Bits permanently set = 0
6 - 7		00	Referencing OFF
		11	Bits permanently set = 1

This results in the following values:

Binary	Hex	Function
00000000	0x00	Referencing OFF
11000001	0xC1	Single shot referencing For a new start after the completed homing procedure: • Write value 0x00 • Wait until bit 0 to bit 3 of the StatusInput01 register takes on the value 0. Counter bits 4 to 7 are not erased • Switch homing procedure on again
11000011	0xC3	Continuous referencing Referencing occurs at every reference pulse.

It is important to know how the optional reference enable is configured. See section 4.11.10.9.4.3 "Homing with reference enable input"

4.11.10.9.5.4 Status of the homing procedure

Name:
StatusInput01

This register contains information regarding whether the referencing process is off, active or complete.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Reference pulse without homing[1)]	0	No reference impulse without homing has occurred yet
		1	At least a reference impulse without homing has occurred
1	State change	0 or 1	Changes with each reference pulse without homing
2	Reference pulse with homing[1)]	0	No homing has occurred yet
		1	At least one homing procedure has occurred
3	State change	0 or 1	Changes with each homing procedure that has taken place
4	Reference pulse	0	The last reference pulse didn't bring about a homing procedure
		1	The last reference pulse brought about a homing procedure
5 - 7	Counter	x	Free-running counter, increased with each reference pulse

1) Always 1 after the first reference pulse that has occurred

Examples of possible values:

Binary	Hex	Function
0x00000000	0x00	Referencing OFF or homing procedure already active
0x00111100	0x3CE	First homing procedure complete Reference value applied in the Encoder01 register
0xxxx11100	0xxB	Bits 5 to 7 are changed with each reference pulse
0xxxx1x100	0xxx	Continuously changing the bits with the "Continuous referencing" setting. The reference value is applied to the Encoder01 register on each reference pulse.

It is important to know how the optional reference enable (see section 4.11.10.9.4.3 "Homing with reference enable input" on page 967) is configured.

4.11.10.9.5.5 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.11.10.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

4.11.10.9.7 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

4.11.10.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
128 µs

4.11.11 X20DC1398

4.11.11.1 General information

This module is equipped with one input for SSI absolute encoders with 24 V encoder signal.

- 1 SSI absolute encoder 24 V
- 1 additional input
- 24 VDC and GND for encoder supply

4.11.11.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1398	X20 digital counter module, 1 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 188: X20DC1398 - Order data

4.11.11.3 Technical data

Product ID	X20DC1398
Short description	
I/O module	1 SSI absolute encoder 24 V
General information	
Input voltage	24 VDC -15 % / +20 %
B&R ID code	0x1BAE
Status indicators	I/O function per channel, operating state, module status
Diagnostics Module run/error	 Yes, using status LED and software
Power consumption Bus Internal I/O	 0.01 W 1.3 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation Encoder - Bus Channel - Bus Channel - Encoder	 Yes Yes No
Type of signal lines	Shielded cables must be used for all signal lines.
Certification CE cULus cCSAus HazLoc Class 1 Division 2 ATEX Zone 2 [1)] KC GL LR GOST-R	 Yes Yes Yes Yes Yes Yes Yes Yes
Digital inputs	
Quantity	1
Nominal voltage	24 VDC
Input current at 24 VDC	Approx. 3.3 mA
Input filter Hardware Software	 ≤2 µs -
Connection type	3-wire connections
Input circuit	Sink
Input resistance	7.19 kΩ

Table 189: X20DC1398 - Technical data

Product ID	X20DC1398
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
SSI absolute encoder	
Encoder inputs	24 V, asymmetrical
Counter size	32-bit
Max. transfer rate	125 kbit/s
Encoder supply	Module-internal, max. 600 mA
Keying	Gray/Binary
CLK: Output current	Max. 100 mA
DATA: Input resistance	18.4 kΩ
Isolation voltage between encoder and bus	500 V_{eff}
Overload behavior of the encoder supply	Short circuit protection, overload protection
Switching threshold	
Low	<5 VDC
High	>15 VDC
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 189: X20DC1398 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.11.4 LED status indicators

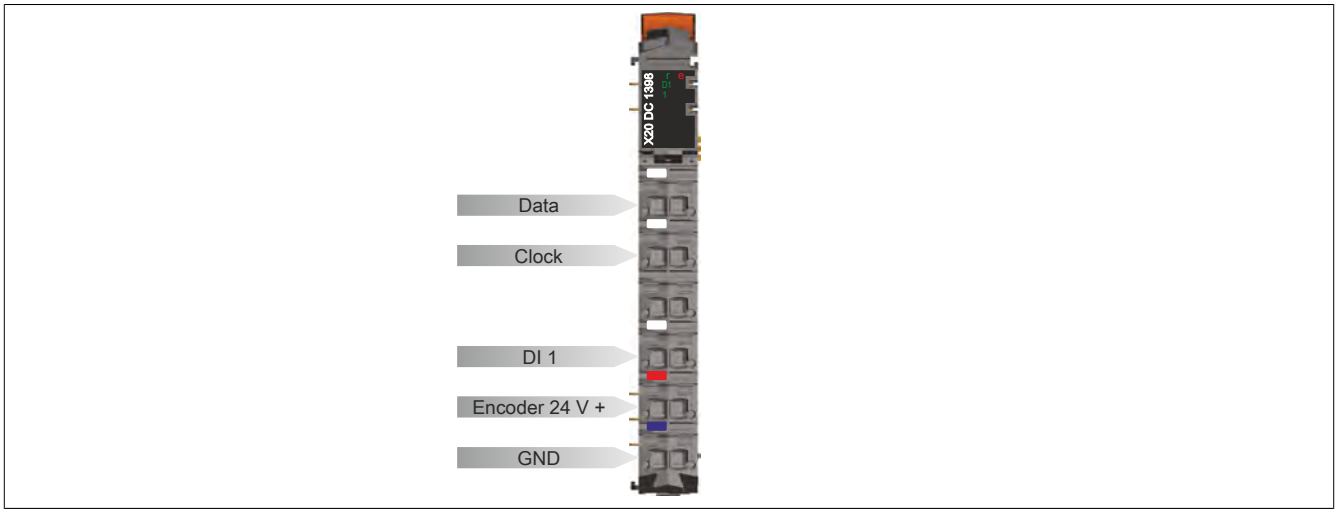
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	D1	Green		Input status - Data signal
	1	Green		Input state - Digital input

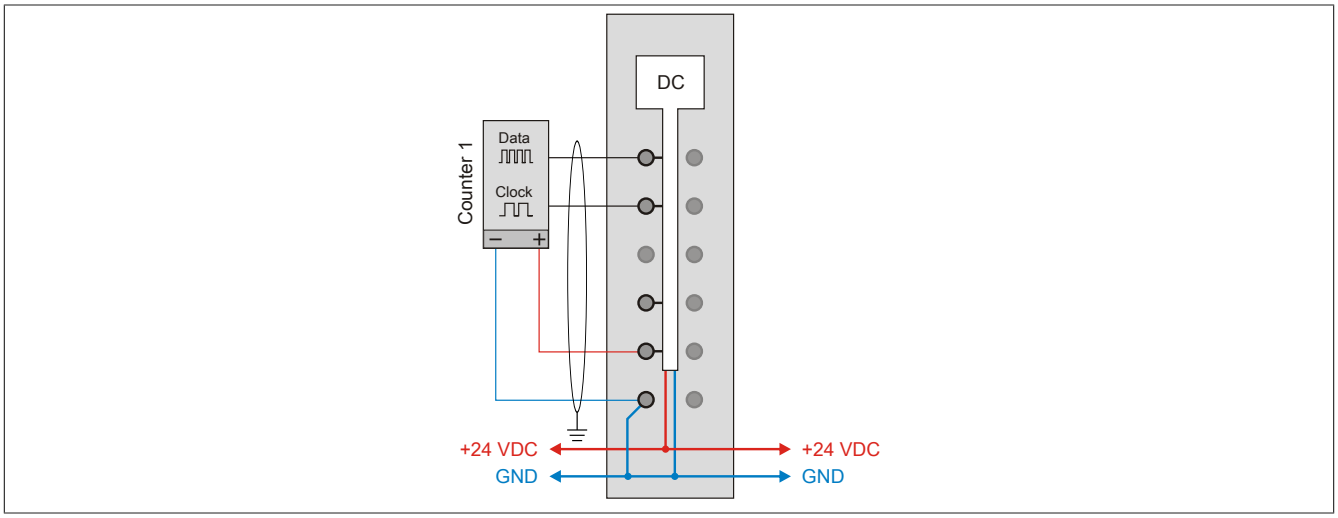
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.11.5 Pinout

Shielded cables must be used for all signal lines.

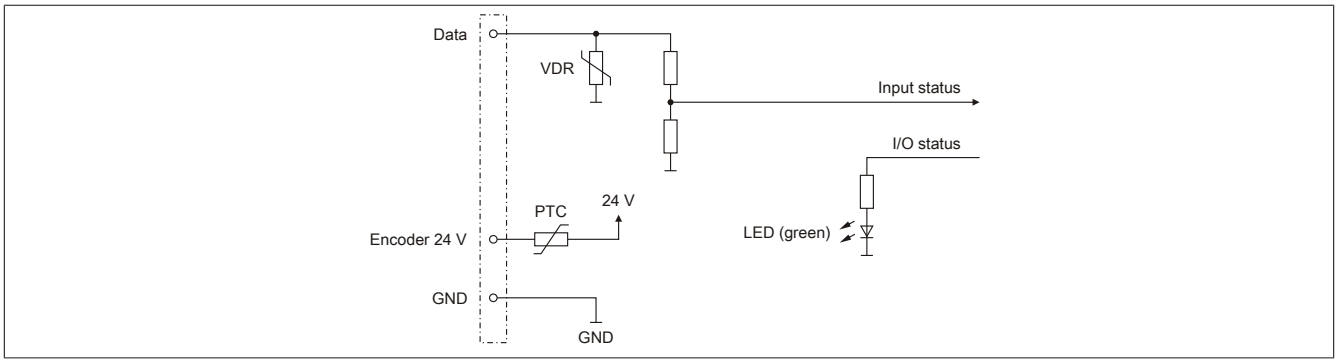


4.11.11.6 Connection example

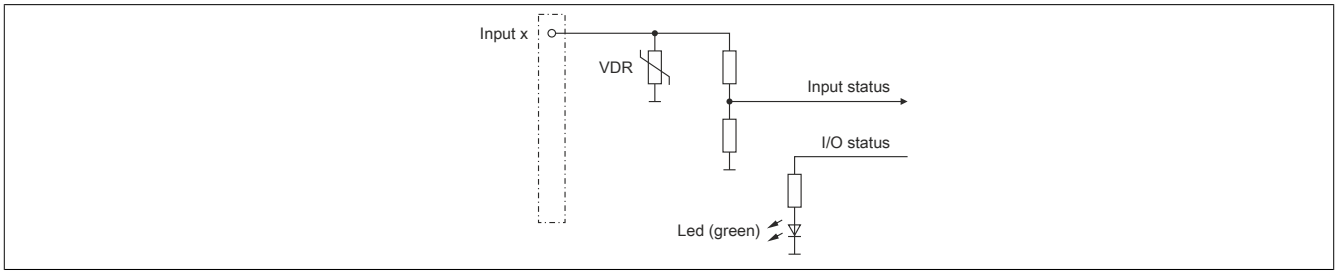


4.11.11.7 Input circuit diagram

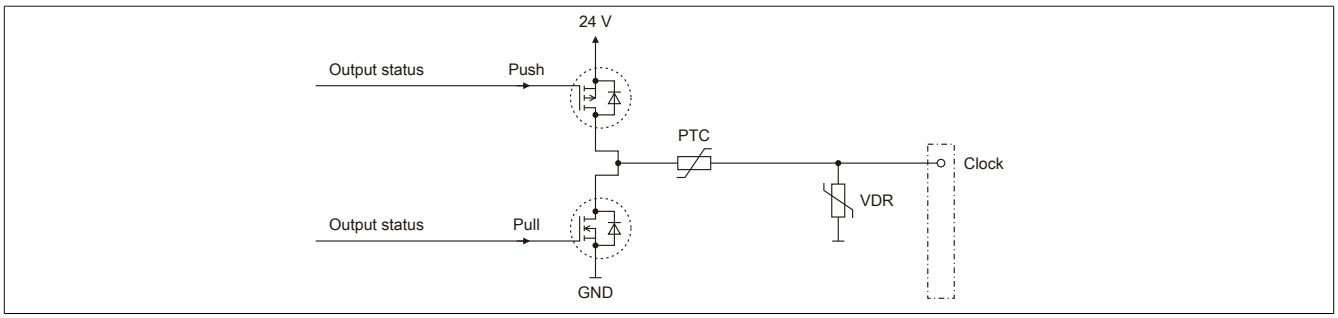
Counter input



Standard input



4.11.11.8 Output circuit diagram



4.11.11.9 Register description

4.11.11.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.11.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
7176	ConfigOutput14	UINT				•
7172	ConfigAdvanced	UDINT				•
Communication						
7184	Encoder01	UDINT	•			
264	Input state of the digital input 1	USINT	•			
	DigitalInput01	Bit 3				
40	Status of encoder supply	USINT	•			
	PowerSupply01	Bit 0				

4.11.11.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
7176	-	ConfigOutput14	UINT				•
7172	-	ConfigAdvanced	UDINT				•
Communication							
7184	0	Encoder01	UDINT	•			
264	4	Input state of the digital input 1	USINT	•			
		DigitalInput01	Bit 3				
40	5	Status of encoder supply	USINT	•			
		PowerSupply01	Bit 0				

1) The offset specifies the position of the register within the CAN object.

4.11.11.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.11.9.4 SSI encoder configuration register

4.11.11.9.4.1 Standard configuration

Name:
ConfigOutput14

This configuration register is used to set the coding, the clock rate and the number of bits. Default = 0. This must be set once using an acyclic write command.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	11	125 kHz
8 - 13	SSI number of bits		Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding

4.11.11.9.4.2 Extended configuration

Name:
ConfigAdvanced

This configuration register is used to set the coding, the clock rate, the number of bits and the monostable multivibrator settings. Default = 0. This must be set once using an acyclic write command.

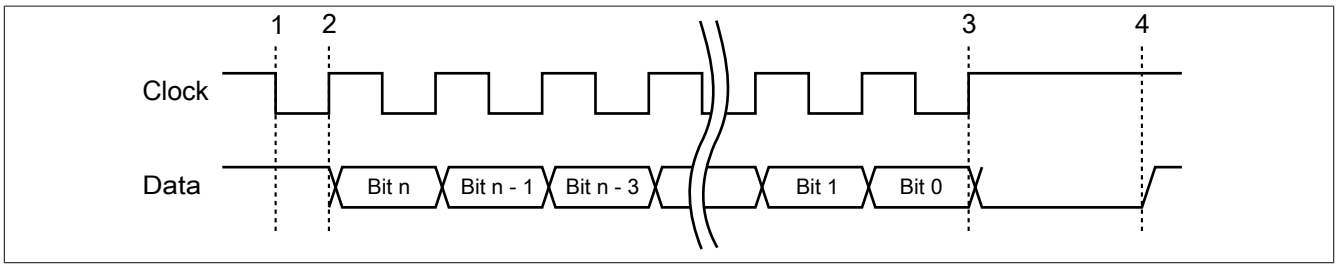
It only differs from ConfigOutput14 by data length and additional monostable multivibrator testing.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding
16 - 17	Monostable multivibrator check	00	Check OFF, no additional clock bit
		01	Check set to High level
		10	Check set to Low level
		11	Level is clocked but ignored
18 - 31	Reserved	0	

Transfer to synchronous serial interface



Measurement value processing

1 Starting bit ... Stores the measurement value
2 Output of first data bit
3 All data bits are transferred, monostable multivibrator time starts counting down.
4 Monostable multivibrator returns to its initial state. A new transfer can be started.

4.11.11.9.5 SSI encoder - Configuration registers

4.11.11.9.5.1 SSI position values

Name:
Encoder01

The SSI encoder value is displayed as a 32-bit position value. The SSI position value is generated synchronously with the X2X cycle.

Data type	Value	Filter
UDINT	0 to 4,294,967,295	SSI position

4.11.11.9.5.2 Input state of the digital input 1

Name:
DigitalInput01

This register displays the input state of the digital input.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
3	DigitalInput01	0 or 1	Input state - Digital input 1

4.11.11.9.5.3 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.11.11.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

4.11.11.9.7 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

4.11.11.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
128 µs

4.11.12 X20DC1976

4.11.12.1 General information

The module is equipped with 1 input for an ABR incremental encoder with 5 V encoder signal. The encoder inputs are monitored (A, B, R).

- 1 ABR incremental encoder 5 V, asymmetric
- Encoder input monitoring
- 2 additional inputs, e.g. for latch input
- 5 VDC, 24 VDC and GND for encoder supply

4.11.12.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC1976	X20 digital counter module, 1x ABR incremental encoder, 5 V (single ended), 250 kHz input frequency, 4x evaluation, encoder monitoring, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 190: X20DC1976 - Order data

4.11.12.3 Technical data

Product ID	X20DC1976
Short description	
I/O module	1 ABR incremental encoder 5 V
General information	
B&R ID code	0xA707
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input voltage	24 VDC (-15% / +20%)
Input current at 24 VDC	Approx. 3.3 mA
Input filter	
Hardware	<2 µs
Software	-
Connection type	3-wire connections
Input circuit	Sink
Additional functions	Latch input

Table 191: X20DC1976 - Technical data

Product ID	X20DC1976
Input resistance	7.03 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Encoder inputs	5 V, asymmetrical (single-ended)
Counter size	16/32-bit
Input frequency	Max. 250 kHz
Evaluation	4x
Encoder supply	
5 VDC	±5%, module-internal, max. 300 mA
24 VDC	Module-internal, max. 300 mA
Input filter	
Hardware	≤600 ns
Software	-
Common-mode range	-10 V ≤ V_{CM} ≤ +13.2 V
Overload behavior of the encoder supply	Short circuit protection, overload protection
Isolation voltage between encoder and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 191: X20DC1976 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.12.4 LED status indicators

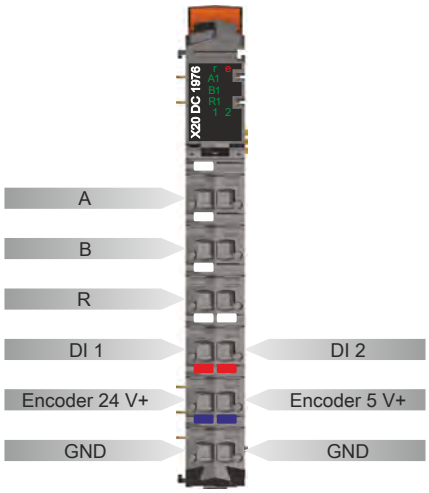
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	The encoder monitor has detected a line fault on the encoder inputs. The status bits must be evaluated in order to provide a more detailed definition of this error. The following error states are detected: • Open line • Short-circuit or voltage level too low
			On	Error or reset status
	A1	Green		Input state of counter input A
	B1	Green		Input state of counter input B
	R1	Green		Input state of reference pulse R
	1 - 2	Green		Input state of the corresponding digital input

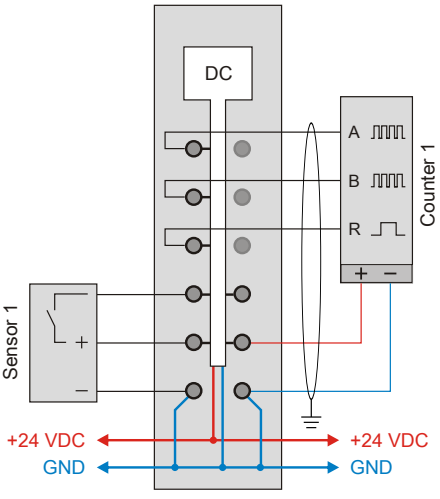
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.12.5 Pinout

Shielded cables must be used for all signal lines.

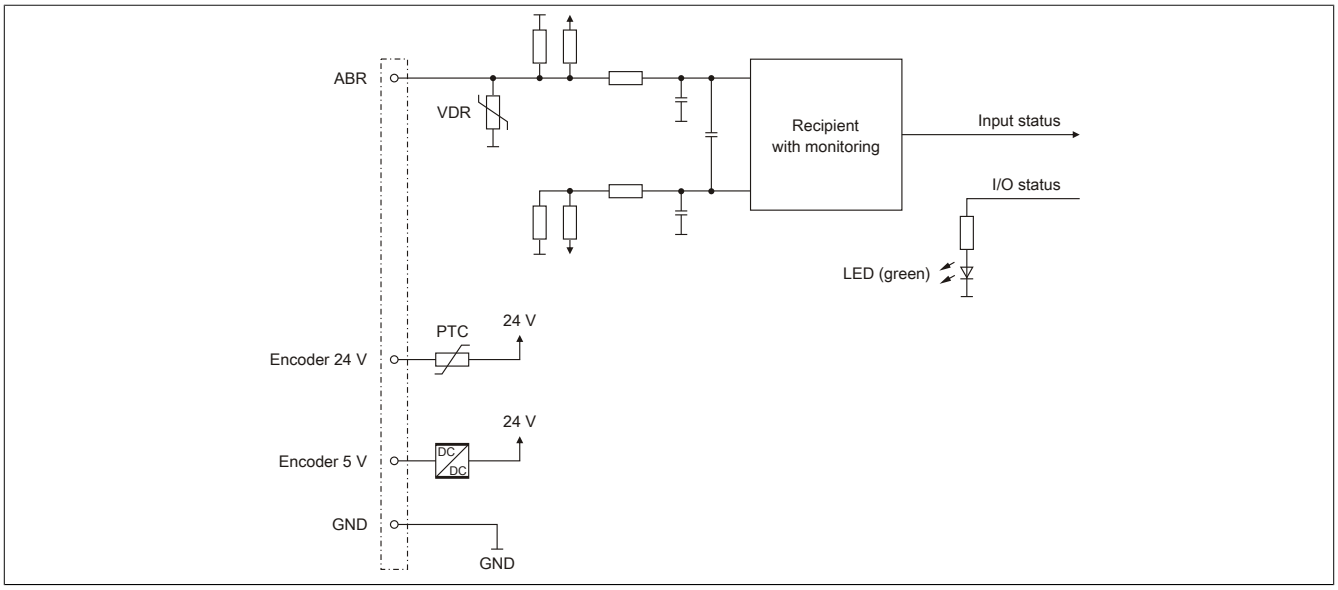


4.11.12.6 Connection example

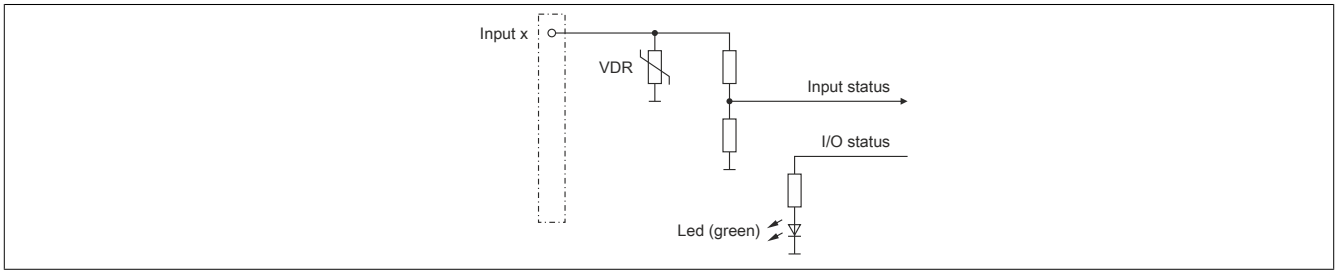


4.11.12.7 Input circuit diagram

Counter inputs



Standard inputs



4.11.12.8 Register description

4.11.12.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.12.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication						
683	SDCLifeCount	SINT	•			
6342	Encoder01	INT	•			
6340		DINT				
6310	Encoder01TimeValid	INT	•			
6308		DINT				
6358	Encoder01Latch	INT	•			
6356		DINT				
6153	Encoder commands	USINT			•	
	Encoder01Reset	Bit 0				
	Encoder01LatchEnable	Bit 1				
927	Input status of signal lines	USINT	•			
	Encoder01_A	Bit 0				
	Encoder01_B	Bit 1				
	Encoder01_R	Bit 2				
	DigitalInput01	Bit 4				
	DigitalInput02	Bit 5				
847	Status of signal lines	USINT	•			
	BW_Channel_A	Bit 0				
	BW_Channel_B	Bit 1				
	BW_Channel_R	Bit 2				
811	Acknowledging error status of signal lines	USINT			•	
	BW_QuitChannel_A	Bit 0				
	BW_QuitChannel_B	Bit 1				
	BW_QuitChannel_R	Bit 2				
6326	Encoder01TimeChanged	INT	•			
6324		DINT				
6303	Encoder01LatchCount	SINT	•			
843	Status of encoder supplies	USINT	•			
	PowerSupply01	Bit 0				
	PowerSupply02	Bit 1				
Encoder - Configuration						
513	CfO_SIframeGenID	USINT				•
642	CfO_SystemCycleTime	UINT				•
769	CfO_PhyIOConfigCh01	USINT				•
771	CfO_PhyIOConfigCh02	USINT				•
773	CfO_PhyIOConfigCh03	USINT				•
777	CfO_PhyIOConfigCh04	USINT				•
779	CfO_PhyIOConfigCh05	USINT				•
815	CfO_BWQuitTimeSelChannel7_0	USINT				•
820	CfO_BWQuitTime_0	UDINT				•
6145	CfO_CounterCycleSelect	USINT				•
6147	CfO_CounterMode	USINT				•
6149	CfO_LatchMode	USINT				•
6151	CfO_LatchComparator	USINT				•
6159	CfO_BWCNTEnableMaskChannel7_0	USINT				•

4.11.12.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Encoder - Communication							
6342	0	Encoder01	INT	●			
6310	2	Encoder01TimeValid	INT	●			
6358	4	Encoder01Latch	INT	●			
6153	1	Encoder commands	USINT			●	
		Encoder01Reset	Bit 0				
		Encoder01LatchEnable	Bit 1				
927	7	Input status of signal lines	USINT	●			
		Encoder01_A	Bit 0				
		Encoder01_B	Bit 1				
		Encoder01_R	Bit 2				
		DigitalInput01	Bit 4				
		DigitalInput02	Bit 5				
847	6	Status of signal lines	USINT	●			
		BW_Channel_A	Bit 0				
		BW_Channel_B	Bit 1				
		BW_Channel_R	Bit 2				
811	0	Acknowledging error status of signal lines	USINT			●	
		BW_QuitChannel_A	Bit 0				
		BW_QuitChannel_B	Bit 1				
		BW_QuitChannel_R	Bit 2				
6326	-	Encoder01TimeChanged	INT		●		
6303	-	Encoder01LatchCount	SINT		●		
843	-	Status of encoder supplies	USINT		●		
		PowerSupply01	Bit 0				
		PowerSupply02	Bit 1				
Encoder - Configuration							
513	-	CfO_SIframeGenID	USINT				●
642	-	CfO_SystemCycleTime	UINT				●
769	-	CfO_PhyIOConfigCh01	USINT				●
771	-	CfO_PhyIOConfigCh02	USINT				●
773	-	CfO_PhyIOConfigCh03	USINT				●
777	-	CfO_PhyIOConfigCh04	USINT				●
779	-	CfO_PhyIOConfigCh05	USINT				●
815	-	CfO_BWQuitTimeSelChannel7_0	USINT				●
820	-	CfO_BWQuitTime_0	UDINT				●
6145	-	CfO_CounterCycleSelect	USINT				●
6147	-	CfO_CounterMode	USINT				●
6149	-	CfO_LatchMode	USINT				●
6151	-	CfO_LatchComparator	USINT				●
6159	-	CfO_BWCNTEnableMaskChannel7_0	USINT				●

1) The offset specifies the position of the register within the CAN object.

4.11.12.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.12.8.4 Encoder - Configuration

The following registers are used for setting functions and configuring the module.

4.11.12.8.4.1 Enabling error monitoring for the signal lines

Name:
CfO_BWCNTEnableMaskChannel7_0

This register requires individually enabling error monitoring for each of the signal channels. "Open line", "short circuit" and "voltage level too low" are reported as error states. Any errors that occur are reported in the error status registers BW_Channel_x.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Enable error monitoring for signal A lines	0	Error monitoring - Encoder Signal A disabled
		1	Error monitoring - Encoder Signal A enabled - Only default in bus controller function model
1	Enable error monitoring for signal B lines	0	Error monitoring - Encoder Signal B disabled
		1	Error monitoring - Encoder Signal B enabled - Only default in bus controller function model
2	Enable error monitoring for signal R lines	0	Error monitoring - Encoder Signal R disabled
		1	Error monitoring - Encoder Signal R enabled - Only default in bus controller function model
3 - 7	Reserved	0	

4.11.12.8.4.2 Timing for automatic error acknowledgment

Name:
CfO_BWQuitTime_0

This register can be used to enable an additional automatic acknowledgment of the error status through timing. If a valid time is set, then the acknowledgment can still be made manually, the only difference is that automatic acknowledgment will take place on the module after the defined amount of time has passed. If the error state has not yet been corrected, then the error status remains and the time is reset. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages.
If the timing = 0, then acknowledgment is only possible using the cyclic acknowledgment registers.

Data type	Value	Information
UDINT	0	No automatic acknowledgment - Only default in bus controller function model
	1 to 2.147.483.647	Time for automatic acknowledgment [µs]

4.11.12.8.4.3 Setting the latch mode

Name:
CfO_LatchMode

This register is used to set the latch mode:

- Single shot latch mode:
  The latch function must be enabled/set. After a successful latch procedure, the activation must be reset in order for a new latch procedure to be activated.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired.

A changed counter state on Encoder01LatchCount indicates that the latch procedure has been performed. The counter value is stored in the latch register Encoder01Latch.

Data type	Value	Information
USINT	0	Single shot latch procedure
	1	Continuous latch procedure

4.11.12.8.4.4 Signal channels for triggering latch procedure

Name:
CfO_LatchComparator

This register defines the signal channels and their level for triggering the latch procedure.

- This mainly configures which channels are linked to generate the latch event. All three signals from the encoder and digital input 1 can be used for the "AND" operation.
- The "active voltage level" needed for the latch procedure can now be used according to the physical signals.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Defines signal level for encoder signal A	0	Low
		1	High
1	Defines signal level for encoder signal B	0	Low
		1	High
2	Defines signal level for encoder signal R	0	Low
		1	High
3	Defines signal level for digital input 1	0	Low
		1	High
4	Use encoder signal A to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal A
5	Use encoder signal B to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal B
6	Use encoder signal R to trigger latch procedure	0	Disabled
		1	Latch function linked to encoder signal R
7	Use digital input 1 to trigger latch procedure	0	Disabled
		1	Latch function linked to digital input 1

4.11.12.8.4.5 Physical configuration

The following registers must be set to the specified constant value for correct physical configuration:

Constant register "CfO_SIframeGenID"

Name:
CfO_SIframeGenID

Data type	Value	Information
USINT	9	Only default in the bus controller module

Constant register "CfO_SystemCycleTime"

Name:
CfO_SystemCycleTime

Cycle time of encoder acquisition in 1/8 µs steps. 1 encoder value is acquired as the counter value per cycle.

Data type	Value	Information
UINT	800	800 = 100 µs; only default in the bus controller module

Constant register "CfO_PhyIOConfigCh01"

Name:
CfO_PhyIOConfigCh01

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh02"

Name:
CfO_PhyIOConfigCh02

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh03"

Name:
CfO_PhyIOConfigCh03

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh04"

Name:
CfO_PhyIOConfigCh04

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_PhyIOConfigCh05"

Name:
CfO_PhyIOConfigCh05

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_BWQuitTimeSelChannel7_0"

Name:
CfO_BWQuitTimeSelChannel7_0

Data type	Value	Information
USINT	0	Only default in the bus controller module

Constant register "CfO_CounterCycleSelect"

Name:
CfO_CounterCycleSelect

Data type	Value	Information
USINT	2	Only default in the bus controller module

Constant register "CfO_CounterMode"

Name:
CfO_CounterMode

Data type	Value	Information
USINT	3	Only default in the bus controller module

4.11.12.8.5 Encoder - Communication

4.11.12.8.5.1 Counter for verifying the data frame

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.11.12.8.5.2 Display of the counter state

Name:
Encoder01

The counter state of the incremental encoder is displayed as a 16 or 32-bit counter value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.12.8.5.3 Net time of the last valid counter value

Name:
Encoder01TimeValid

The net time of the last valid counter value is the time of the last valid counter value (see "Cfo_SystemCycleTime" register) recorded on the module. The user is able to determine the validity of the counter value by evaluating its age in the program. This means that the module and error status bits do not have to be checked additionally to determine the validity of the value.

The net time of the last valid counter value that was read is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in milliseconds.
DINT[1)]	-2.147.483.648 to 2.147.483.647	

1) Can only be configured in the standard function model

4.11.12.8.5.4 Net time of the last counter value change

Name:
Encoder01TimeChanged

For slow X2X Link cycles, the net time of the last counter value change can be used to more accurately determine the speed.

The net time of the last counter value change is displayed as 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value	Information
INT	-32768 to 32767	NetTime in µsec.
DINT[1)]	-2.147.483.648 bis 2.147.483.647	

1) Can only be configured in the standard function model

4.11.12.8.5.5 Counter value at the time of the last latch

Name:
Encoder01Latch

The counter value at the time of the last latch is displayed as a 16 or 32-bit value. Only the 16-bit value is available in the bus controller function model.

Data type	Value
INT	-32768 to 32767
DINT[1)]	-2.147.483.648 bis 2.147.483.647

1) Can only be configured in the standard function model

4.11.12.8.5.6 Counter value of latch event

Name:
Encoder01LatchCount

The latch events are counted and stored in a cyclic 8-bit counter. This counter is incremented with each latch event, thereby indicating a new occurrence. The new latched counter value is stored in the respective latch register.

Data type	Value
SINT	-128 to 127

4.11.12.8.5.7 Encoder commands

Name:
Encoder01Command

This register can be used to

1 reset the counter value. The counter is kept at zero until this command is reset.
2 enable the latch procedure. If the latch configuration is valid and matches the hardware signals, then this activation causes the counter value to be saved in the latch register.

The two different latch configurations that are possible (see section 4.11.3.8.4.3 "Setting the latch mode") must be handled as follows:

- Single shot latch mode:
  After successful latching, indicated by the latch event counter, activation must be reset before any more latching is possible. The activation must be set again if additional latching is needed.
- Continuous latch mode:
  The latch function only has to be enabled/set as long as latching is desired. The latch event counter is incremented with each event.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01Reset	0	Do not reset
		1	Set encoder value to 0
1	Encoder01LatchEnable	0	Do not activate latch
		1	Latching
2 - 7	Reserved	0	

4.11.12.8.5.8 Input status of signal lines

Name:
Encoder01_A
Encoder01_B
Encoder01_R
DigitalInput01 to DigitalInput02

This register displays the input status of the signal lines from the encoder and the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder01_A	0/1	Input state of encoder signal A
1	Encoder01_B	0/1	Input state of encoder signal B
2	Encoder01_R	0/1	Input state of encoder signal R
3	Reserved	0	
4	DigitalInput01	0/1	Input state - Digital input 1
5	DigitalInput02	0/1	Input state - Digital input 2
6 - 7	Reserved	0	

4.11.12.8.5.9 Error status of signal lines

The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Status of signal lines

Name:
BW_Channel_A
BW_Channel_B
BW_Channel_R

This register displays the error states of the signal lines from the encoder. The error states are latched when they occur and are maintained until acknowledged. The counter and time registers are not updated if there are pending or unacknowledged errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_Channel_A	0	No error in encoder signal A
		1	Open line, short circuit or voltage level too low
1	BW_Channel_B	0	No error in encoder signal B
		1	Open line, short circuit or voltage level too low
2	BW_Channel_R	0	No error in encoder signal R
		1	Open line, short circuit or voltage level too low
3 - 7	Reserved	0	

Acknowledging error status of signal lines

Name:
BW_QuitChannel_A
BW_QuitChannel_B
BW_QuitChannel_R

This register can be used to acknowledge the latched error states of the signal lines from the encoder. However, if there are still pending errors remaining, then the error status remains active. After acknowledging the errors, the bits must also be reset or else any repetition of the error would be undetected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	BW_QuitChannel_A	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal A
1	BW_QuitChannel_B	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal B
2	BW_QuitChannel_R	0	No acknowledgment
		1	Acknowledgment of error status - Encoder signal R
3 - 7	Reserved	0	

Manual acknowledgment of latched error states

The latched error states of the signal lines from the encoder can be acknowledged manually. However, if there are still pending errors remaining, then the error status remains active. After successfully acknowledging the errors (latched error status = 0), the acknowledge bits must still be reset by the user or else a re-occurrence of an error could be overlooked by the user.

Example 1: **Cause of error corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user after the cause of error has been corrected. The latched error status changes to zero.

The manual acknowledge must now be reset so that any new errors will be recognized by the user.

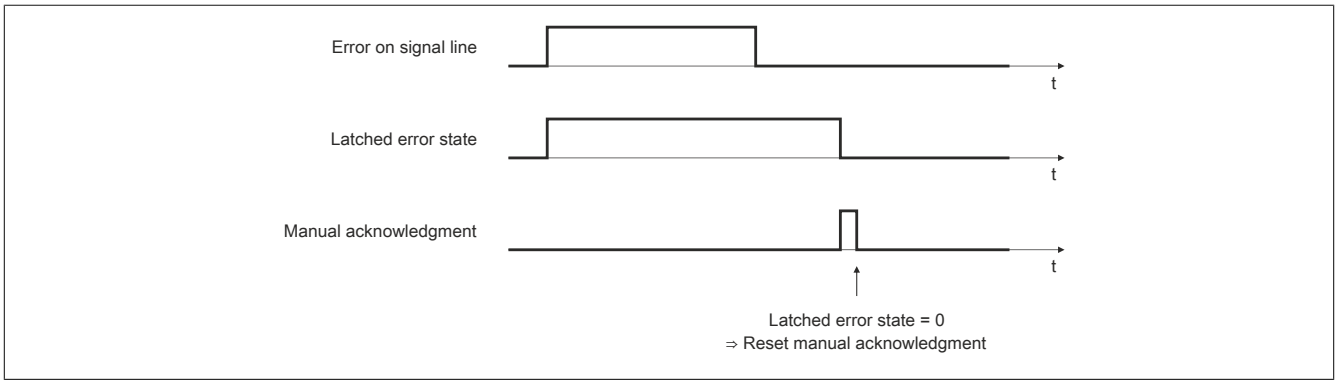


Figure 191: Cause of error corrected before being acknowledged

Example 2: **Cause of error not yet corrected before being acknowledged**

An error has occurred on a signal line. The error state is detected and latched by the module. The error is acknowledged by the user before the cause of error has been corrected. The latched error status remains set because the error is still remaining.

Acknowledgment is only successful after the cause of error has been corrected. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

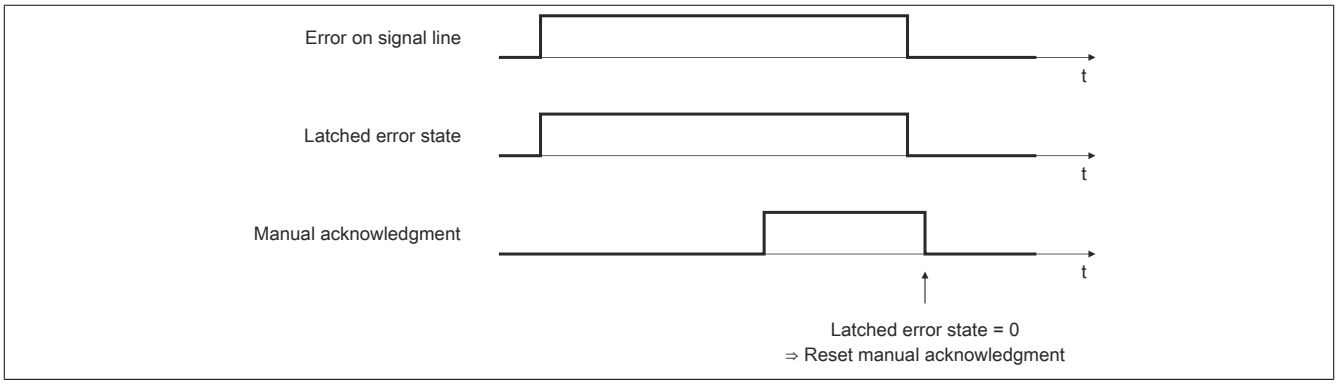


Figure 192: Cause of error not yet corrected before being acknowledged

Automatic acknowledgment of latched error states

In addition to manual acknowledgment, automatic acknowledgment of the latched error states after a specified amount of time can also be enabled. Make sure that the time is set long enough for the higher-level system to reliably detect the status messages and for the validity of the counter value to be determined using its age.

If the time specification = 0, then only manual acknowledgment is possible.

Example 1: An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged as soon as the time expires. The latched error status changes to zero.

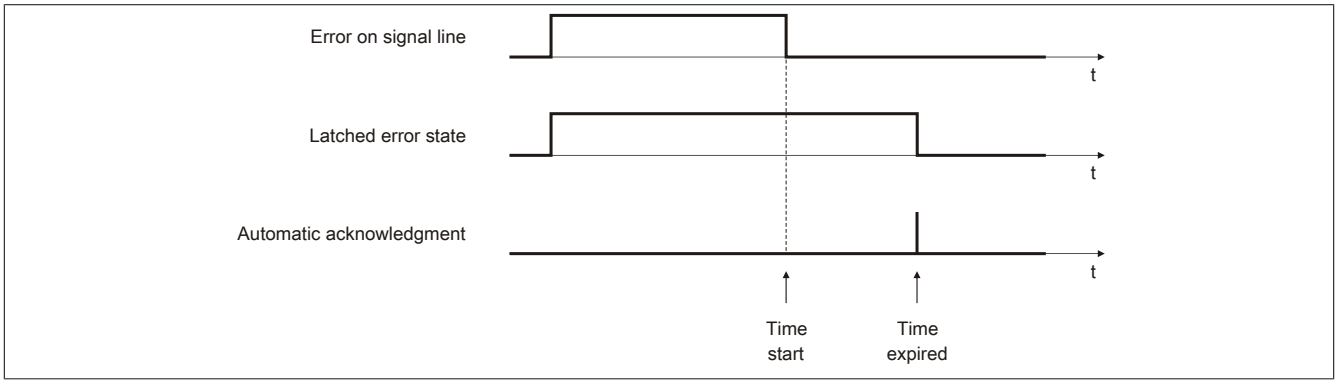


Figure 193: Latched error state acknowledged automatically

Example 2: Automatic and manual acknowledge used

An error has occurred on a signal line. The error state is detected and latched by the module. The time for automatic acknowledgment starts counting after the cause of error has been corrected. The error is acknowledged manually by the user before the time expires. The latched error status changes to zero. The manual acknowledge must now be reset so that any new errors will be recognized by the user.

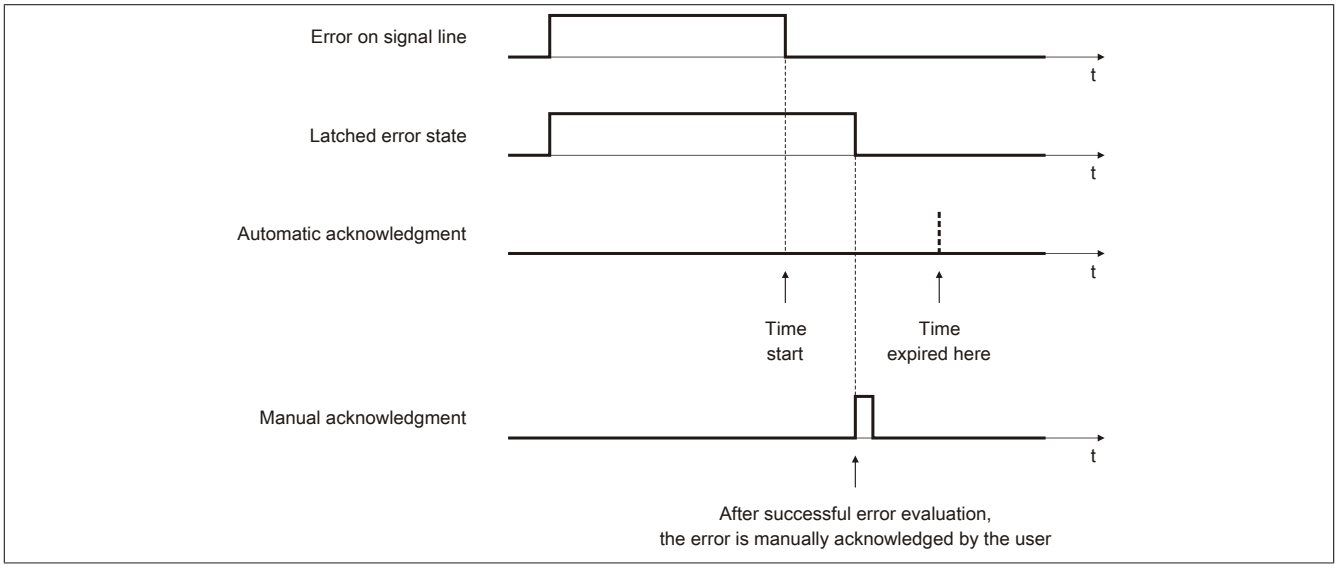


Figure 194: Automatic and manual acknowledge used

4.11.12.8.5.10 Status of encoder supplies

Name:
PowerSupply01 to PowerSupply02

This register shows the status of the integrated encoder supplies. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1	PowerSupply02	0	5 VDC encoder power supply OK
		1	5 VDC encoder power supply faulty
2 - 7	Reserved	-	

4.11.12.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.11.12.8.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
150 µs

4.11.13 X20DC2190

4.11.13.1 General information

This module can be used to determine paths and to calculate speeds at the same time. The ultrasonic transducer rods are connected directly to the RS422 interface. Communication to the transducer rod takes place using start/stop signals. With the DPI/IP protocol, it is also possible, for example, to read operational properties directly from the transducer. During service (when a transducer is being exchanged) the machine can be started again quickly without additional configuration work.

The module is designed for connecting 2 transducer rods with a total of up to 4 paths. That means, for example, that 2 ultrasonic transducers with 2 magnets each or one with 4 magnets can be used. The combination 3/1 is also possible. The module provides 24 VDC as an external supply for the sensor.

- Ultrasonic transducer module
- Path measurement (resolution 10 µm)
- Speed measurement (resolution 100 µm/s)
- 1, 2, 3 and 4 magnetic rod measurements possible
- DPI/IP protocol supported

4.11.13.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC2190	X20 digital counter module, ultrasonic transducer module, interfaces: EP start/stop, DPI/IP, 2 transducer rods, 4 path evaluation	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 192: X20DC2190 - Order data

4.11.13.3 Technical data

Product ID	X20DC2190
Short description	
I/O module	Ultrasonic transducer module, 2 transducer rods, 4 position detection, speed measurement
General information	
B&R ID code	0x2188
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Channels for path and speed measurements	
Quantity	2
Supported encoder types	Start/Stop interface EP start/stop interface DPI/IP interface
Encoder supply	
Voltage	24 VDC, module-internal, max. 150 mA
Monitoring	Configurable overvoltage/undervoltage monitoring (±10%, ±15%, ±20%, ±25%)
Short circuit protection	Rev. D0 and higher
Input and output level	RS422 differential level
Multi-magnet measurement	Yes, in combination per rod, max. 4 magnets total
Outputs	1.6 µs durational initialization pulse
Inputs	
Path measurement	Resolution = 0.01mm, measurement range = ±5.2m
Speed measurement	Resolution = 0.1 mm/s, measurement range = ±3.2 m/s
Precision	±50 ppm ±5 ppm/year
Short circuit protection	No
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 193: X20DC2190 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

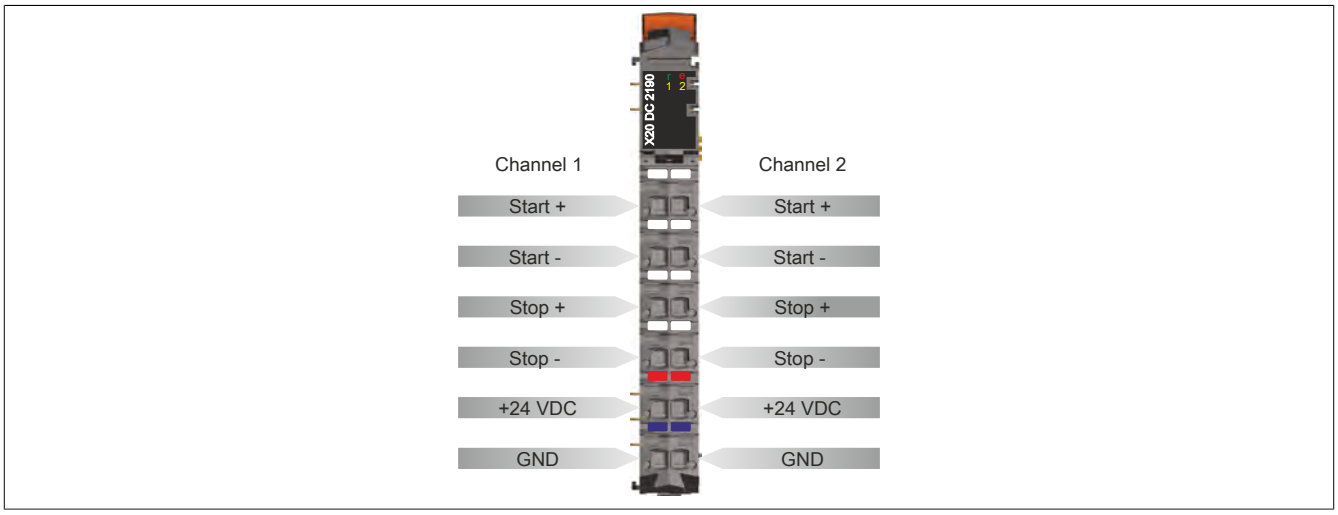
4.11.13.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	Reset mode
			Double flash	Boot mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 2	Yellow	Off	No transducer rod connected
			On	No transducer rod is connected to the respective measurement channel

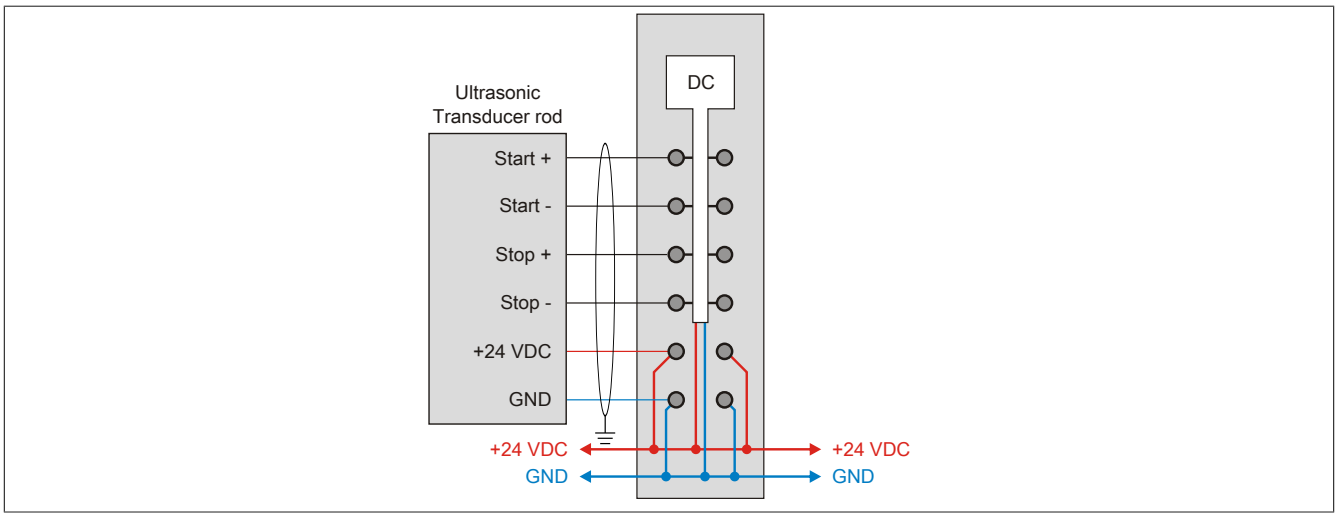
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.13.5 Pinout



The ultrasonic transducers should be connected using a shielded cable. The shield of the encoder cable is connected to the ground via the shield connection on the X20 bus module.

4.11.13.6 Connection example



4.11.13.7 Register description

4.11.13.7.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.13.7.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Synchronous register						
0	Position01	DINT	•			
4	Position02	DINT	•			
8	Position03	DINT	•			
12	Position04	DINT	•			
16	Speed01	INT	•			
18	Speed02	INT	•			
20	Speed03	INT	•			
22	Speed04	INT	•			
24	ErrorStatus01	USINT	•			
25	ErrorStatus02	USINT	•			
26	ErrorStatus03	USINT	•			
27	ErrorStatus04	USINT	•			
28	StatusInput01	USINT	•			
30	USSpeed01	UDINT			•	
34	USSpeed02	UDINT			•	
68	StatusOutput01	USINT			•	
Configuration registers						
38	ConfigOutput01	USINT				•
40	ConfigOutput02	UINT				•
60	ConfigOutput03	UDINT				•
64	ConfigOutput04	UDINT				•
134	ConfigOutput07	DINT				•
72	ConfigOutput08	DINT				•
84	ConfigOutput09	DINT				•
88	ConfigOutput10	DINT				•
92	ConfigOutput11	DINT				•
96	ConfigOutput12	DINT				•
100	ConfigOutput13	UDINT				•
104	ConfigOutput14	UDINT				•
76	ConfigOutput15	DINT				•
80	ConfigOutput16	DINT				•
138	ConfigOutput17	DINT				•
142	ConfigOutput18	DINT				•
146	ConfigOutput19	DINT				•
150	ConfigOutput20	DINT				•
154	ConfigOutput21	UDINT				•
158	ConfigOutput22	UDINT				•
42	ConfigOutput23	USINT				•
44	ConfigOutput24	USINT				•
Read configuration register						
38	ConfigOutput01Read	USINT		•		
40	ConfigOutput02Read	UINT		•		
60	ConfigOutput03Read	UDINT		•		
64	ConfigOutput04Read	UDINT		•		
134	ConfigOutput07Read	DINT		•		
72	ConfigOutput08Read	DINT		•		
84	ConfigOutput09Read	DINT		•		
88	ConfigOutput10Read	DINT		•		
92	ConfigOutput11Read	DINT		•		
96	ConfigOutput12Read	DINT		•		
100	ConfigOutput13Read	UDINT		•		
104	ConfigOutput14Read	UDINT		•		
76	ConfigOutput15Read	DINT		•		
80	ConfigOutput16Read	DINT		•		
138	ConfigOutput17Read	DINT		•		
142	ConfigOutput18Read	DINT		•		
146	ConfigOutput19Read	DINT		•		
150	ConfigOutput20Read	DINT		•		
154	ConfigOutput21Read	UDINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
158	ConfigOutput22Read	UDINT		●		
42	ConfigOutput23Read	USINT		●		
44	ConfigOutput24Read	USINT		●		
Status register						
108	StatusInput09	UDINT		●		
112	StatusInput10	UDINT		●		
116	StatusInput11	UDINT		●		
120	StatusInput12	UDINT		●		
162	StatusInput13	UDINT		●		
166	StatusInput14	UDINT		●		
170	StatusInput15	UDINT		●		
174	StatusInput16	UDINT		●		
178	StatusInput17	UDINT		●		
182	StatusInput18	UDINT		●		
186	StatusInput19	UDINT		●		
190	StatusInput20	UDINT		●		
194	StatusInput21	UDINT		●		
198	StatusInput22	UDINT		●		
202	StatusInput23	UDINT		●		
206	StatusInput24	UDINT		●		
210	StatusInput25	UDINT		●		
214	StatusInput26	UDINT		●		
218	StatusInput27	UDINT		●		
222	StatusInput28	UDINT		●		
226	StatusInput29	UDINT		●		
230	StatusInput30	UDINT		●		
234	StatusInput31	UDINT		●		
238	StatusInput32	UDINT		●		
242	StatusInput33	UDINT		●		
246	StatusInput34	UDINT		●		
250	StatusInput35	UDINT		●		
254	StatusInput36	UDINT		●		

4.11.13.7.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Synchronous register							
0	0	Position01	DINT	●			
4	8	Position02	DINT	●			
8	16	Position03	DINT	●			
12	24	Position04	DINT	●			
30	4	Speed01	INT	●			
32	12	Speed02	INT	●			
34	20	Speed03	INT	●			
36	28	Speed04	INT	●			
38	-	LB: Error status of Magnet 1 HB: Module status	UINT	●			
	6	ErrorStatus01	USINT	●			
	7	StatusInput01	USINT	●			
40	14	ErrorStatus02	USINT	●			
42	22	ErrorStatus03	USINT	●			
44	30	ErrorStatus04	USINT	●			
100	0	USSpeed01	UDINT			●	
109	8	USSpeed02	UDINT			●	
150	16	StatusOutput01	USINT			●	
Configuration registers							
2200	-	ConfigOutput01	USINT				●
2100	-	ConfigOutput02	UINT				●
2000	-	ConfigOutput03	UDINT				●
2004	-	ConfigOutput04	UDINT				●
2008	-	ConfigOutput07	DINT				●
2012	-	ConfigOutput08	DINT				●
2024	-	ConfigOutput09	DINT				●
2028	-	ConfigOutput10	DINT				●
2040	-	ConfigOutput11	DINT				●
2044	-	ConfigOutput12	DINT				●
2056	-	ConfigOutput13	UDINT				●
2060	-	ConfigOutput14	UDINT				●
2016	-	ConfigOutput15	DINT				●
2020	-	ConfigOutput16	DINT				●
2032	-	ConfigOutput17	DINT				●
2036	-	ConfigOutput18	DINT				●

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2048	-	ConfigOutput19	DINT				●
2052	-	ConfigOutput20	DINT				●
2064	-	ConfigOutput21	UDINT				●
2068	-	ConfigOutput22	UDINT				●
2201	-	ConfigOutput23	USINT				●
2202	-	ConfigOutput24	USINT				●
Read configuration register							
2200	-	ConfigOutput01Read	USINT		●		
2100	-	ConfigOutput02Read	UINT		●		
2000	-	ConfigOutput03Read	UDINT		●		
2004	-	ConfigOutput04Read	UDINT		●		
2008	-	ConfigOutput07Read	DINT		●		
2012	-	ConfigOutput08Read	DINT		●		
2024	-	ConfigOutput09Read	DINT		●		
2028	-	ConfigOutput10Read	DINT		●		
2040	-	ConfigOutput11Read	DINT		●		
2044	-	ConfigOutput12Read	DINT		●		
2056	-	ConfigOutput13Read	UDINT		●		
2060	-	ConfigOutput14Read	UDINT		●		
2016	-	ConfigOutput15Read	DINT		●		
2020	-	ConfigOutput16Read	DINT		●		
2032	-	ConfigOutput17Read	DINT		●		
2036	-	ConfigOutput18Read	DINT		●		
2048	-	ConfigOutput19Read	DINT		●		
2052	-	ConfigOutput20Read	DINT		●		
2064	-	ConfigOutput21Read	UDINT		●		
2068	-	ConfigOutput22Read	UDINT		●		
2201	-	ConfigOutput23Read	USINT		●		
2202	-	ConfigOutput24Read	USINT		●		
Status register							
2500	-	StatusInput09	UDINT		●		
2556	-	StatusInput10	UDINT		●		
2504	-	StatusInput11	UDINT		●		
2560	-	StatusInput12	UDINT		●		
2508	-	StatusInput13	UDINT		●		
2564	-	StatusInput14	UDINT		●		
2512	-	StatusInput15	UDINT		●		
2568	-	StatusInput16	UDINT		●		
2516	-	StatusInput17	UDINT		●		
2572	-	StatusInput18	UDINT		●		
2520	-	StatusInput19	UDINT		●		
2524	-	StatusInput20	UDINT		●		
2528	-	StatusInput21	UDINT		●		
2532	-	StatusInput22	UDINT		●		
2536	-	StatusInput23	UDINT		●		
2540	-	StatusInput24	UDINT		●		
2576	-	StatusInput25	UDINT		●		
2580	-	StatusInput26	UDINT		●		
2584	-	StatusInput27	UDINT		●		
2588	-	StatusInput28	UDINT		●		
2592	-	StatusInput29	UDINT		●		
2596	-	StatusInput30	UDINT		●		
2544	-	StatusInput31	UDINT		●		
2548	-	StatusInput32	UDINT		●		
2552	-	StatusInput33	UDINT		●		
2600	-	StatusInput34	UDINT		●		
2604	-	StatusInput35	UDINT		●		
2608	-	StatusInput36	UDINT		●		

1) The offset specifies the position of the register within the CAN object.

In the bus controller function model, the measurements made from the module are not synchronized with the X2X Link. The time between two measurements is defined by the configured recovery time for the rod (see section 4.11.13.7.12 "Channel configuration" on page 1003) unlike on the X2X where it is the smallest multiple of the X2X cycle time that is larger than the configured recovery time.

4.11.13.7.3.1 CAN I/O bus controller

The module occupies 4 analog logical slots on CAN-I/O.

4.11.13.7.4 Commissioning a transducer rod

Two registers need to be configured to initialize an ultrasonic transducer rod and receive valid measurements. The first step is to enter the length of the rod (see section 4.11.13.7.13 "Rod length 1 and 2" on page 1003). The wave propagation speed for the rod must then be defined (see section 4.11.13.7.9 "Ultrasonic speed specification" on page 1001). This information can usually be found directly on the transducer rod itself or in its data sheet.

If the plausibility limits remain set to 0 (default value), one of the respective ErrorStatus registers will now indicate faulty readings or plausibility errors. If this is the case, plausibility mode can be disabled using the "ConfigOutput01" register (see section 4.11.13.7.11 "Module configuration" on page 1002). This will cause the positions of the magnets to be displayed on the rod.

4.11.13.7.5 Reading the magnet position

Name:
Position01 - Position04

These registers contain the position of the individual magnets on the transducer rods.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647: Resolution 1 µm

4.11.13.7.6 Reading the magnet speed

Name:
Speed01 to Speed04

These registers contain the speed of the individual magnets on the transducer rods. A resolution of 0.1 mm/s is achieved by calculating the speed from 2 position values within a 100 ms interval.

Data type	Value
INT	-32768 to 32767: Resolution 0.1 mm/s

4.11.13.7.7 Error status

Name:
ErrorStatus01 to ErrorStatus04

These registers can be used to indicate the error status for individual channels.

Data type	Value
USINT	See bit structure.

Bit structure

Bit	Description
0 - 3	Counter for plausibility errors (cyclic)
4 - 7	Counter for mis-measurements (cyclic)

Possible reasons for plausibility errors:

- Configured max. or min. path of a magnet was exceeded
- Configured max. speed was exceeded

Possible reasons for faulty measurements:

- Configured rod length was exceeded
- Rod failure
- Missing measurement magnet

Information:

If the registers "USSpeed01" and "USSpeed02" are unequal to 0 after the module starts up, the respective error counters on slower fieldbus systems (e.g. CAN I/O) may continue to count until the module configuration is completed. In some cases, this is due problems between the respective rod and the default configuration.

4.11.13.7.8 Status information about the transducer rods

Name:
StatusInput01

This register displays the status information for the transducer rods.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Supply voltage too low	0	Supply voltage OK
		1	Supply voltage too low
1	Supply voltage too high	0	Supply voltage OK
		1	Supply voltage too high
2	Transducer Rod 1	0	Ok
		1	Deactivated or not initialized
3	Transducer Rod 2	0	Ok
		1	Deactivated or not initialized
4	Transducer Rod 1	0	Protocol error (invalid data)
		1	Protocol OK (valid data)
5	Transducer Rod 2	0	Protocol error (invalid data)
		1	Protocol OK (valid data)
6 - 7	Reserved		

Comment concerning bits 4 + 5

If this bit is set to "1", configuration data was successfully read from the measurement rod using DPI/IP or EP protocol. This data can now be read into the application using asynchronous access.

4.11.13.7.9 Ultrasonic speed specification

Name:
USSpeed01 to USSpeed02

The module does not perform any measurements on the respective rod while these registers have the value 0. Also disabled:

- Automatic check to determine whether a rod is connected
- Parameter upload via DPI/IP or EP protocol

If a value >0 but <1000cm/s is specified here, the module freezes all measurements and error counters of the corresponding rod, regardless of whether plausibility mode is enabled or not. Based on the default ultrasonic speed of 280,000 cm/s, however, periodic measurement start pulses continue to be generated according to the formula in section 4.11.13.7.12 "Channel configuration" on page 1003. In this case the rod check (inserted/not inserted and parameter upload) continues to be active.

As soon as a valid value (≥1000) is specified, the module recalculates the measurement rate (see section 4.11.13.7.12 "Channel configuration" on page 1003) and begins the position/speed measurement.

Data type	Value
UDINT	0 to 4,294,967,296: Resolution 1 cm/s

4.11.13.7.10 Applying new magnet offsets

Name:
StatusOutput01

This register makes it easier to more quickly determine new offsets (= zero positions) for the individual magnets. This approach is an alternative or additional method to determining an offset via configuration registers (see section 4.11.13.7.14 "Offset position on the transducer" on page 1004).

If the respective bit changes from 0 to 1 in "StatusOutput01" (see following table) then the current mechanical position of the respective magnet becomes the calculated zero position (register "Position0x" = 0).
From that moment, the current mechanical position will be subtracted from all future measured positions. This is essentially a type of referencing. The max. and min. magnet paths (see section 4.11.13.7.15 "Plausibility check configuration" on page 1004) are now based on the new zero position.
This process can be repeated at any time by setting the bit again.

Information:

An offset position determined in this manner *CANNOT* be read out. The registers "ConfigOutput07Read", "ConfigOutput08Read", "ConfigOutput15Read" and "ConfigOutput16Read" can only be used to read the current contents of "ConfigOutput07", "ConfigOutput08", "ConfigOutput15" and "ConfigOutput16".

Data type	Value
USINT	See bit structure.

Bit	Name	Value	Information
0	Magnet 1	0	No effect
		1	Apply offset magnet 1
...		...	
3	Magnet 4	0	No effect
		1	Apply offset magnet 4
4 - 7	Reserved		

4.11.13.7.11 Module configuration

Name:
ConfigOutput01

This register configures the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Plausibility mode	0	The plausibility error counter is incremented with each implausible measurement and the last plausible measurement value is "frozen" (default)
		1	The plausibility error counter is incremented with each implausible measurement and the implausible measurement value is forwarded to the controller
1	Reserved		
2 - 3	Tolerance for monitoring the supply voltage	00	25%
		01	20%
		10	15%
		11	10%
4 - 7	Magnet number	0000	4 magnets on channel 1, channel 2 not available
		0001	3 magnets on channel 1, 1 magnet on channel 2
		0010	2 magnets on channel 1, 2 magnets on channel 2
		0011	1 magnet on channel 1, 0 magnets on channel 2
		0100	2 magnets on channel 1, 0 magnets on channel 2
		0101	3 magnets on channel 1, 0 magnets on channel 2
		0110	2 magnets on channel 1, 1 magnet on channel 2
		0111	1 magnet on channel 1, 1 magnet on channel 2
		1xxx	Reserved

4.11.13.7.12 Channel configuration

Name:
ConfigOutput02

This register can be used to configure the individual channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Transducer Rod 1	000	User parameter
		001	DPI/IP (Balluf)
		010	EP Start/Stop (MTS)
		011	Reserved
		1xx	Reserved
3 - 4	Rod 1: Start/Stop IF type	00	Start/Stop Signal: Rising edge - rising edge
		01	Start/Stop Signal: Falling edge - falling edge
		10	Start/Stop Signal: Rising edge - falling edge (gate time)
		11	Only Stop Signal: Start when signal is triggered (initialization pulses)
5	Rod 1: Recovery time factor, minimum time between two measurements	0	3 x USW runtime for rod (default)
		1	2 x USW runtime for rod
6 - 7	Reserved		
8 - 10	Transducer Rod 2	000	User parameter
		001	DPI/IP (Balluf)
		010	EP Start/Stop (MTS)
		011	Reserved
		1xx	Reserved
11 - 12	Rod 2: Start/Stop IF type	00	Start/Stop Signal: Rising edge - rising edge
		01	Start/Stop Signal: Falling edge - falling edge
		10	Start/Stop Signal: Rising edge - falling edge (gate time)
		11	Only Stop Signal: Start when signal is triggered (initialization pulses)
13	Rod 2: Recovery time factor, minimum time between two measurements	0	3 x USW runtime for rod (default)
		1	2 x USW runtime for rod
14 - 15	Reserved		

Comment concerning bits 5 + 13

USW transducer rods require a certain recovery time between two measurements to allow the ultrasonic wave to fade. Otherwise there is a risk of interfering with the next measurement (especially when the rod has more than 1 magnet).

Depending on the setting, the module waits at least 2 or 3 times the runtime of the ultrasonic wave for the measurement rod (default = 3x). In the standard function module, the next measurement is then triggered synchronously with the next X2XLink cycle.

The runtime measurement is based on the settings for the rod length (plus a safety margin of 100mm) and the ultrasonic speed:

- USW runtime = (rod length + 100mm) / ultrasonic speed.

For their rods, BALLUFF recommends a recovery time equal to 3 times the maximum runtime of the ultrasonic wave for the measurement rod. This is the default setting for the module.

The setting can be switched to 2 times the runtime if the measurement rate is otherwise too slow. This may only be done after consulting the manufacturer of the transducer rods!

4.11.13.7.13 Rod length 1 and 2

Name:
ConfigOutput03 to ConfigOutput04

These registers are used to configure the length of the respective rod.

- Rod length 1: ConfigOutput03
- Rod length 2: ConfigOutput04

Data type	Value
UDINT	0 to 4,294,967,296: Resolution 1 mm

4.11.13.7.14 Offset position on the transducer

Name:
ConfigOutput07 to ConfigOutput08
ConfigOutput15 to ConfigOutput16

These registers are used to assign the respective magnet an offset position (= zero position) on the transducer. The max. and min. magnet paths refer to these specified offsets (see 4.11.13.7.15 "Plausibility check configuration" on page 1004). If the offset is changed using the StatusOutput01 register, this becomes the new zero position. This does not affect the contents of the offset register.

- Offset magnet 1: ConfigOutput07
- Offset magnet 2: ConfigOutput08
- Offset magnet 3: ConfigOutput15
- Offset magnet 4: ConfigOutput16

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647: Resolution 1 µm

4.11.13.7.15 Plausibility check configuration

These registers are used to configure the plausibility check (also see section 4.11.13.7.7 "Error status" on page 1000).

4.11.13.7.15.1 Min. plausible magnet position

Name:
ConfigOutput09 to ConfigOutput10
ConfigOutput17 to ConfigOutput18

These registers are used to assign the min. plausible magnet position based on the applicable offset.

- Min. path - magnet 1: ConfigOutput09
- Min. path - magnet 2: ConfigOutput10
- Min. path - magnet 3: ConfigOutput17
- Min. path - magnet 4: ConfigOutput18

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647: Resolution 1 µm

4.11.13.7.15.2 Max. plausible magnet position

Name:
ConfigOutput11 to ConfigOutput12
ConfigOutput19 to ConfigOutput20

These registers are used to assign the max. plausible magnet position based on the applicable offset.

- Max. path - magnet 1: ConfigOutput11
- Max. path - magnet 2: ConfigOutput12
- Max. path - magnet 3: ConfigOutput19
- Max. path - magnet 4: ConfigOutput20

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647: Resolution 1 µm

4.11.13.7.15.3 Max. plausible magnet speed

Name:
ConfigOutput13 to ConfigOutput14
ConfigOutput21 to ConfigOutput22

These registers are used to assign the max. plausible magnet speed.

- Max. speed - magnet 1: ConfigOutput13
- Max. speed - magnet 2: ConfigOutput14
- Max. speed - magnet 3: ConfigOutput21
- Max. speed - magnet 4: ConfigOutput22

Data type	Value
UDINT	0 to 4,294,967,296: Resolution 0.1 mm/s

4.11.13.7.16 Dead time for rods 1 and 2

Name:
ConfigOutput23 to ConfigOutput24

These registers are used to configure the dead time of the respective rod.

- Dead time for rod 1: ConfigOutput23
- Dead time for rod 2: ConfigOutput24

To prevent the multiple pulses that occur with some encoders from affecting the measurement, all pulses received within a configurable timespan from the beginning of the measurement are not evaluated. The range for the dead time lies between 0 and 255 µs. The following figure illustrates the effects of defining a dead time:

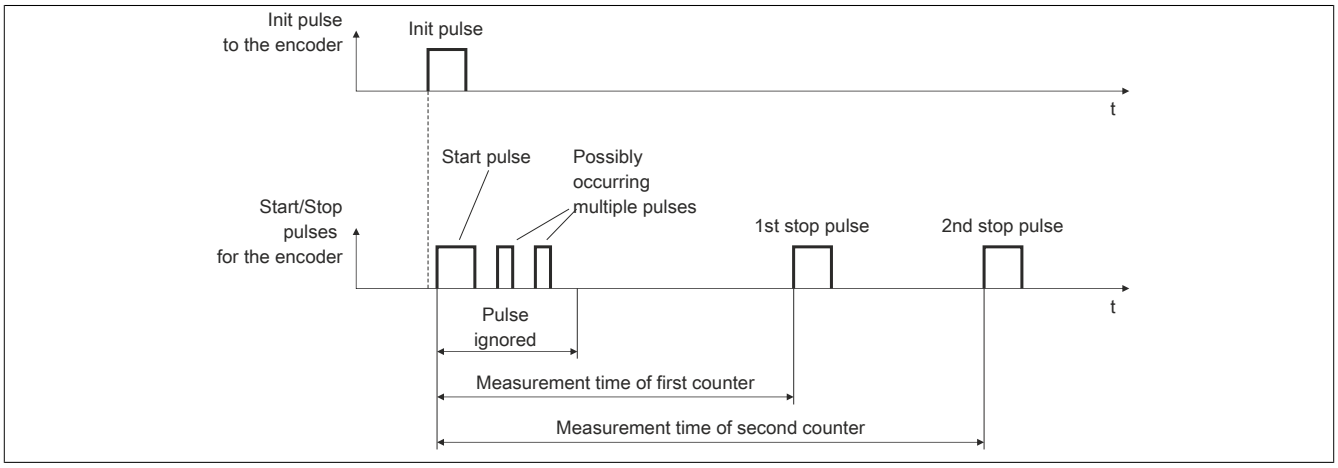


Figure 195: Pulse Ignored after Start Pulse

Data type	Value
USINT	0 to 255: Resolution 1 µs (default: 0 µs)

4.11.13.7.17 Read configuration register

Name:
ConfigOutput01Read to ConfigOutput04Read
ConfigOutput07Read to ConfigOutput24Read

These registers are used to read the states of the corresponding configuration registers.

4.11.13.7.18 Status register

Name:
StatusInput09 to StatusInput36

These registers are used to store the data read after a parameter upload from transducer rods with DPI/IP protocol or EP protocol. The registers "StatusInput19" to "StatusInput36" remain empty (0x0000) on transducer rods with EP protocol.

4.11.13.7.18.1 Parameter overview

The following parameters are stored in the status registers:

Register	Description	Supported by the protocol	
		DP/IP	EP
StatusInput09	Rod length 1 [mm]	●	●
StatusInput10	Rod length 2 [mm]	●	●
StatusInput11	Ultrasonic speed 1	●	●
StatusInput12	Ultrasonic speed 2	●	●
StatusInput13	Rod 1: Zero point offset [µm]	●	●
StatusInput14	Rod 2: Zero point offset [µm]	●	●
StatusInput15	Rod 1: Vendor ID (see transducer rod data sheet)	●	●
StatusInput16	Rod 2: Vendor ID (see transducer rod data sheet)	●	●
StatusInput17	Rod 1: Serial number (Hex coded)	●	●
StatusInput18	Rod 2: Serial number (Hex coded)	●	●
StatusInput19	Rod 1: Type ID 1 (MSB = letter 1)	●	0x0000
StatusInput20	Rod 1: Type ID 2 (MSB = letter 5)	●	0x0000
StatusInput21	Rod 1: Type ID 3 (MSB = letter 9)	●	0x0000
StatusInput22	Rod 1: Type ID 4 (MSB = letter 13)	●	0x0000
StatusInput23	Rod 1: Type ID 5 (MSB = letter 17)	●	0x0000
StatusInput24	Rod 1: Type ID 6 (MSB = letter 21)	●	0x0000
StatusInput25	Rod 2: Type ID 1 (MSB = letter 1)	●	0x0000
StatusInput26	Rod 2: Type ID 2 (MSB = letter 5)	●	0x0000
StatusInput27	Rod 2: Type ID 3 (MSB = letter 9)	●	0x0000
StatusInput28	Rod 2: Type ID 4 (MSB = letter 13)	●	0x0000
StatusInput29	Rod 2: Type ID 5 (MSB = letter 17)	●	0x0000
StatusInput30	Rod 2: Type ID 6 (MSB = letter 21)	●	0x0000
StatusInput31	Rod 1: Serial number ASCII 1 (MSB = letter 1)	●	0x0000
StatusInput32	Rod 1: Serial number ASCII 2 (MSB = letter 5)	●	0x0000
StatusInput33	Rod 1: Serial number ASCII 3 (MSB = letter 9)	●	0x0000
StatusInput34	Rod 2: Serial number ASCII 1 (MSB = letter 1)	●	0x0000
StatusInput35	Rod 2: Serial number ASCII 2 (MSB = letter 5)	●	0x0000
StatusInput36	Rod 2: Serial number ASCII 3 (MSB = letter 9)	●	0x0000

4.11.13.7.18.2 DPI/IP protocol (BALLUFF) / EP protocol (MTS)

Requirements for a successful upload of the transducer rod parameters to the module:

1. Selection of the communication protocol (DPI/IP or EP). See section . 4.11.13.7.12 "Channel configuration" on page 1003
2. Transducer rod must support the respective protocol.
3. If the transducer rod does not support the selected protocol, the module will detect this after a timeout of approx. 300 ms and will treat the rod as a "normal" transducer rod.

After the module is started or after a transducer rod is connected, the parameter upload should be complete within 200 to 400 ms.

A communication error causes the data upload to cancel. A new upload attempt can be initiated by the user by deactivating and reactivating the communication protocol using asynchronous access.

All rod parameters can be read to the controller using asynchronous access. The read parameters "rod length" and "ultrasonic speed" are **NOT** automatically uploaded to the module.

It is left up to the application whether the upload values for rod length 1 and rod length 2 or for ultrasonic speed 1 and ultrasonic speed 2 are uploaded.

Information:

Keep in mind that no position measurements can be performed on a rod while parameters are being uploaded. The module freezes all existing position/speed data for all magnets on the rod while the parameters are uploading. Parameters should therefore only be uploaded with the machine stopped, and this should be ensured by the application.

4.11.13.7.19 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

4.11.14 X20(c)DC2395

4.11.14.1 General information

This module is a multifunctional counter module. It can be connected to one SSI encoder, one ABR encoder, two AB encoders or four event counters. Two outputs are available for pulse width modulation. The functions can also be mixed.

- 24 VDC encoder inputs
- SSI, ABR, AB or event counters for inputs
- Pulse width modulation for outputs
- 24 VDC and GND for encoder supply

Information:

This module is a multifunctional module. Some bus controllers only support the default function model.

Default function model:

- **2x event counter (24 V)**
- **2x PWM output (24 V)**

4.11.14.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.11.14.3 Order data

Model number	Short description	Figure
	Counter functions	
X20DC2395	X20 digital counter module, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function	
X20cDC2395	X20 digital counter module, coated, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 194: X20DC2395, X20cDC2395 - Order data

4.11.14.4 Technical data

Product ID	X20DC2395	X20cDC2395
Short description		
I/O module	1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4x event counters or 2x pulse width modulation, time measurement, relative timestamp	
General information		
Input voltage	24 VDC -15 % / +20 %	
B&R ID code	0x1CD4	0xE503
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using the status LED and software (output error status)	
Power consumption		
Bus	0.01 W	
Internal I/O	1.4 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Output - Output	No	
Output - Bus	Yes	
Output - Encoder	No	
Encoder - Bus	Yes	
Encoder - Encoder	No	
Type of signal lines	Shielded cables must be used for all signal lines.	
Certification		
CE	Yes	
cULus	Yes	-
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Incremental encoder		
Quantity	2	
Encoder inputs	24 V, asymmetrical	
Counter size	16/32-bit	
Input frequency	Max. 100 kHz	
Evaluation	4x	
Encoder supply	Module-internal, max. 600 mA	
Overload behavior of the encoder supply	Short circuit protection, overload protection	
SSI absolute encoder		
Quantity	1	
Encoder inputs	24 V, asymmetrical	
Counter size	32-bit	
Max. transfer rate	125 kbit/s	
Encoder supply	Module-internal, max. 600 mA	
Keying	Gray/Binary	
CLK: Output current	Max. 100 mA	
Overload behavior of the encoder supply	Short circuit protection, overload protection	
Event counter		
Quantity	4	
Nominal voltage	24 VDC	
Signal form	Square wave pulse	
Evaluation	Each edge, cyclic counter	
Input frequency	Max. 100 kHz	
Input current at 24 VDC	Approx. 1.3 mA	
Input resistance	18.4 kΩ	
Isolation voltage between channel and bus	500 V_{eff}	
Counter frequency	200 kHz	
Counter size	16/32-bit	
Input filter		
Hardware	≤2 µs	
Software	-	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Edge detection / Time measurement		
Possible measurements	Gate time, period duration, edge offset for various channels	
Measurements per module	Up to 9	
Measurements per channel	Up to 2	
Counter size	16-bit	
Counter frequency		
Internal	8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, 62.5 kHz	

Table 195: X20DC2395, X20cDC2395 - Technical data

Product ID	X20DC2395	X20cDC2395
Signal form	Square wave pulse	
Measurement type	Continuous or triggered	
Digital outputs		
Design	Push / Pull / Push-Pull	
Quantity	2	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	0.1 A	
Total nominal current	0.2 A	
Output circuit	Sink or source	
Output protection	Thermal cutoff if overcurrent or short circuit occurs, integrated protection for switching inductances	
Pulse width modulation [2]		
Period duration	41.6 µs to 1.36 s	
Factor for period duration	n/48000 s, n = 2 to 65535	
Pulse duration	0 to 100 %	
Resolution for pulse duration	0.1%	
Actuator supply	Module-internal, max. 600 mA	
Diagnostic status	Output monitoring	
Leakage current when switched off	Max. 25 µA	
Residual voltage	<0.9 V at 0.1 A rated current	
Peak short circuit current	<10 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay		
0 -> 1	<2 µs	
1 -> 0	<2 µs	
Switching frequency		
Resistive load	Max. 24 kHz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Switching voltage + 0.6 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 195: X20DC2395, X20cDC2395 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Dead time when switching between push and pull: max. 1.5 µs.

4.11.14.5 LED status indicators

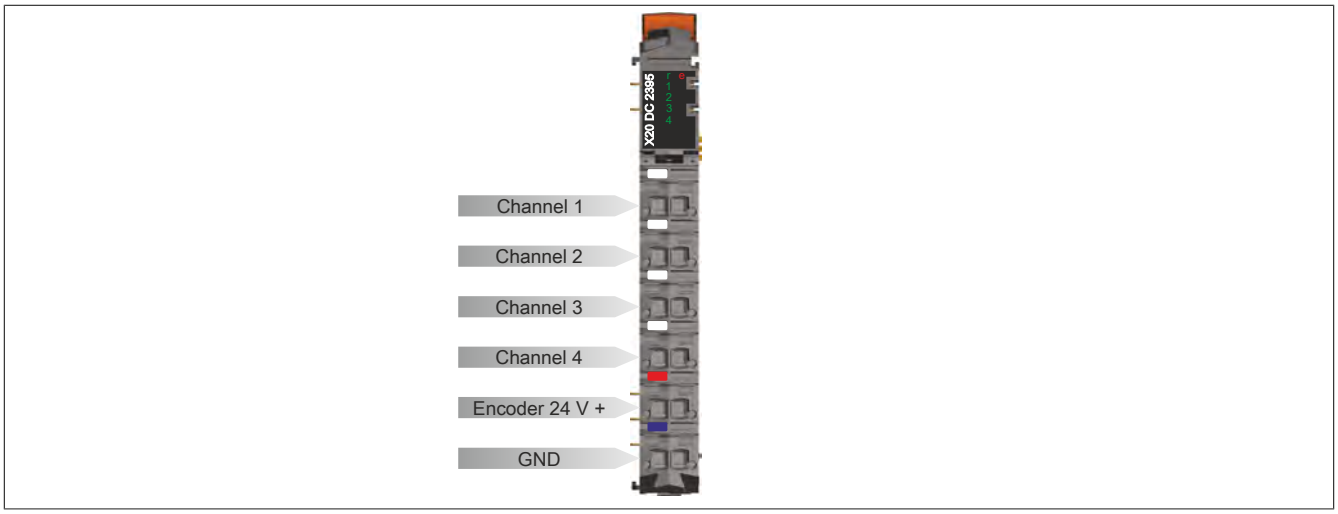
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 4	Green		Status of the corresponding digital signal

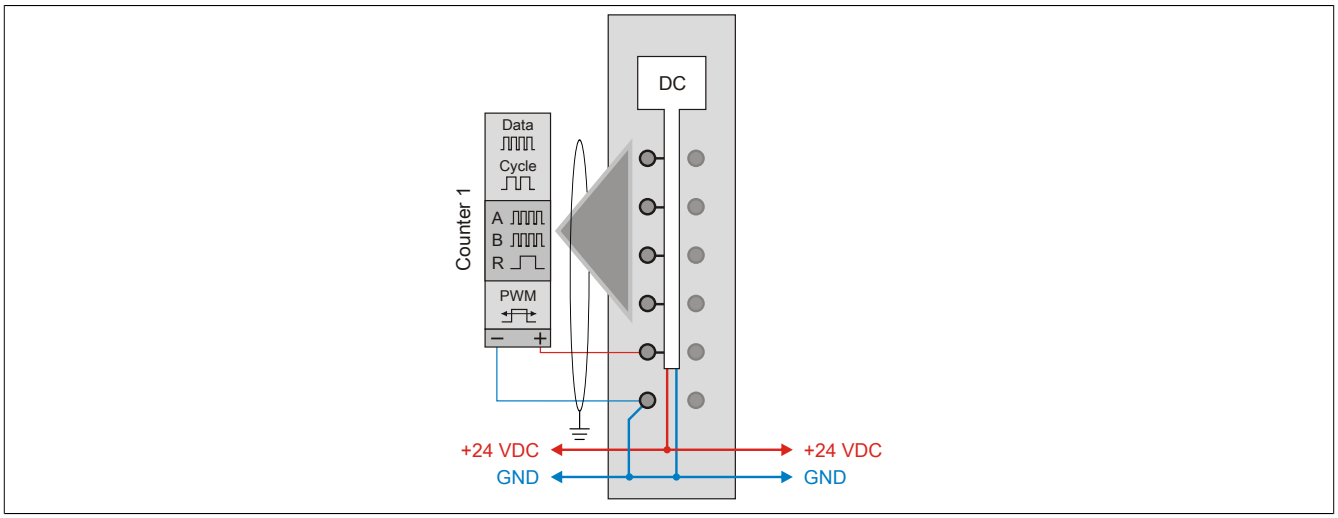
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.14.6 Pinout

Shielded cables must be used for all signal lines.



4.11.14.7 Connection example



4.11.14.8 Function overview

The following functions can be configured on the module. They cannot all be used at the same time due to the multiple use of the hardware channels and the limited cyclic data length.

- 4 digital channels, 2 of which can be configured as outputs
- 4 event counters with configurable counting direction and optional referencing via digital input
- 2 PWM outputs
- 2 up/down counters, each with optional latch inputs and comparator output
- 2 AB counters, each with optional latch inputs and comparator output
- 1 ABR encoder with configurable reference pulse edge and reference position, optional reference enable input, latch input and comparator output
- 1 SSI counter with optional latch input and comparator output
- 2 edge-triggered time measurement functions with configurable start edge based on current configuration settings

4.11.14.8.1 Description of channel assignments

The functions listed here are directly assigned to the respective hardware channels and cannot be changed:

Channel	Signal connections
1	• Digital input 1 • Event counter 1 • AB encoder 1 - signal line A • Up/down counter 1 - frequency • SSI encoder 1 - data line • ABR encoder 1 - signal line A
2	• Digital input 2 • Digital output 2 • Event counter 2 • PWM output 2 • AB encoder 1 - signal line B • Up/down counter 1 - direction • SSI encoder 1 - clock line • ABR encoder 1 - signal line B
3	• Digital input 3 • Event counter 3 • AB encoder 2 - signal line A • Up/down counter 2 - frequency • ABR encoder 1 - signal line R
4	• Digital input 4 • Digital output 4 • Event counter 4 • PWM output 4 • AB encoder 2 - signal line B • Up/down counter 2 - direction • ABR encoder 1 - reference enable input

Options available in addition to these basic functions, such as comparator outputs or latch inputs, can be configured freely to unused input/output channels.

4.11.14.8.2 Connection options

Channels 1 to 4 can be connected as follows:

Channel	Function					
1	I	Event counter	A	A	SSI data	
2	I/O	Event counter	B	B	SSI cycle	PWM
3	I	Event counter	A	R		
4	I/O	Event counter	B	Enable reference		PWM

The functions can also be mixed. For example:

Example 1	
Channel	**Function**
1	SSI data
2	SSI cycle
3	Event counter
4	PWM

Example 2	
Channel	**Function**
1	SSI data
2	SSI cycle
3	A
4	B

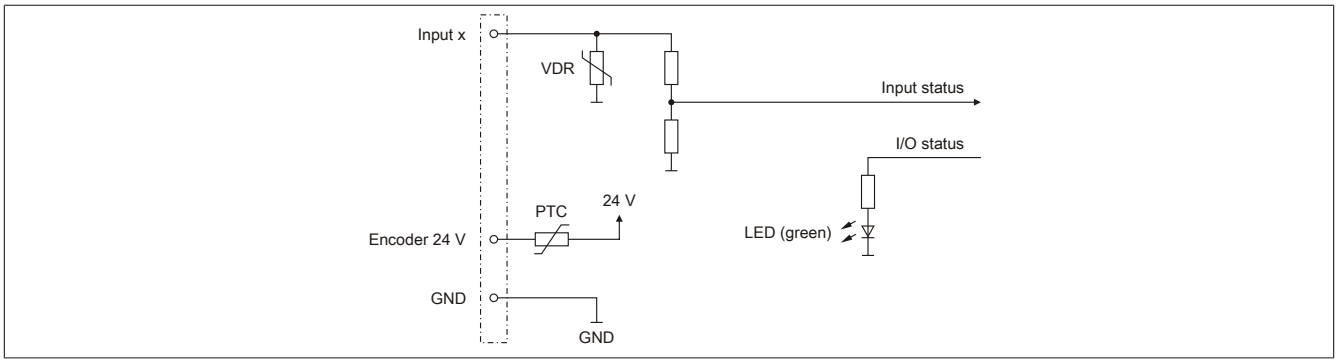
Example 3	
Channel	**Function**
1	Event counter
2	PWM
3	Event counter
4	PWM

Example 4	
Channel	**Function**
1	A
2	B
3	R
4	Enable reference

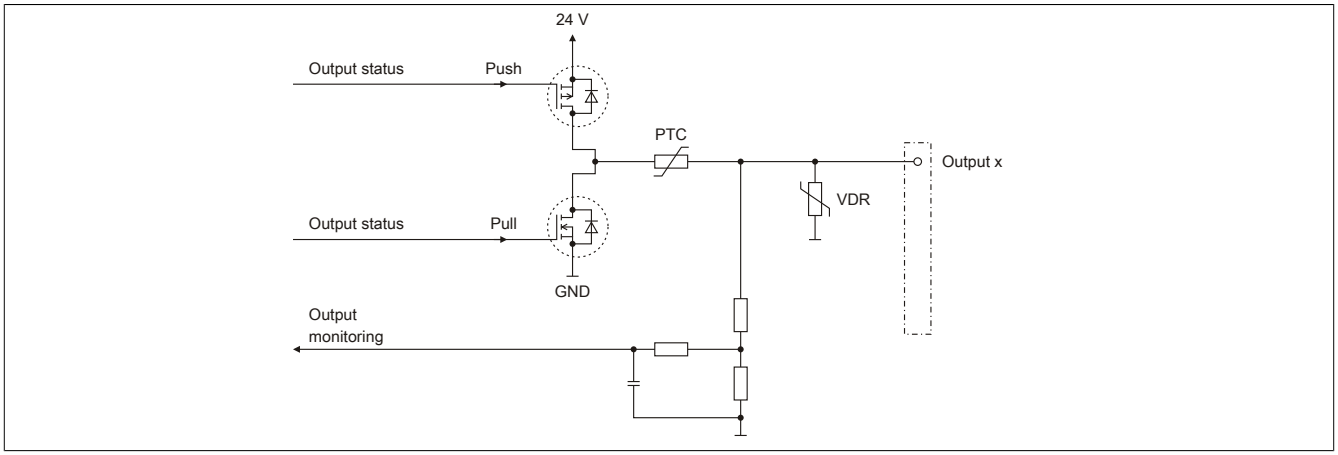
Example 5	
Channel	**Function**
1	A
2	B
3	Event counter
4	PWM

Example 6	
Channel	**Function**
1	Event counter
2	PWM
3	A
4	B

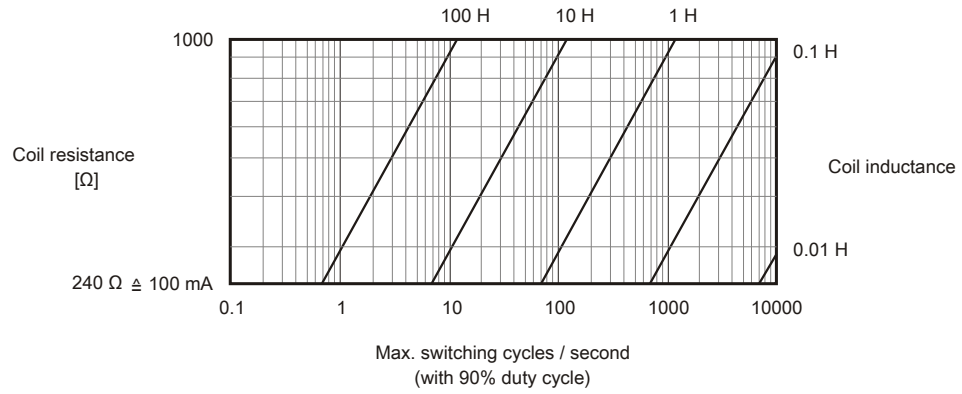
4.11.14.9 Input circuit diagram



4.11.14.10 Output circuit diagram



4.11.14.11 Switching inductive loads



4.11.14.12 Calculating the period duration

The outputs of the module can be operated as PWM outputs. The period duration is calculated using the following formula:

$$\text{Period duration} = \frac{n}{48000}\ \text{s}$$

A value of 2 to 65535 can be defined for n.

Example

n	Period duration	Frequency
2	416 µs	24 kHz
24000	500 ms	2 Hz
48000	1 s	1 Hz
65535	1.36 s	0.73 Hz

4.11.14.13 Register description

4.11.14.13.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.14.13.2 Function model 0 - Standard and Function model 1 - 32-bit counter

The following 2 models can be selected:

- 16-bit counter, Function model 0
- 32-bit counter, Function model 1 (identified in the table with a "(D)" in the data type and "(_32Bit)" in the name.)

The only difference between these two models is that they use either 16-bit or 32-bit registers for incremental counter functions. These include:

- ABR encoders
- AB encoders
- Up/down counters
- Event counters

All other module functions e.g. SSI, PWM and time measurement, as well as their data types, are identical for the two models.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module configuration - General						
(N-1) * 2	CfO_CFGchannel0N (Index N = 1 to 4)	USINT				●
64 + N * 2	CfO_LEDNsource (Index N = 0 to 3)	USINT				●
Configuration - Input for ABR encoders						
512	CfO_DIREKTIOevent0IDwr	UINT				●
516	CfO_DIREKTIOevent0mode	USINT				●
522	CfO_DIREKTIOevent0compState	UINT				●
520	CfO_Ev0CompMask	USINT				●
2,064	CfO_Counter1PresetValue1(_32Bit)	U(D)INT				●
2,068	CfO_Counter1PresetValue2(_32Bit)	U(D)INT				●
2,320	CfO_Counter2PresetValue1(_32Bit)	U(D)INT				●
2,324	CfO_Counter2PresetValue2(_32Bit)	U(D)INT				●
2,048	CfO_Counter1config	USINT				●
2,056	CfO_Counter1configReg0	USINT				●
2,058	CfO_Counter1configReg1	USINT				●
2,112	CfO_Counter1event0IDwr	UDINT				●
2,120	CfO_Counter1event0config	UINT				●
2,144	CfO_Counter1event1IDwr	UINT				●
2,152	CfO_Counter1event1config	UINT				●
2,148	CfO_Counter1event1mode	USINT				●
Configuration - Inputs for AB, up/down and event counters						
2,048	CfO_Counter1config	USINT				●
2,056	CfO_Counter1configReg0	USINT				●
2,058	CfO_Counter1configReg1	USINT				●
2,112	CfO_Counter1event0IDwr	UDINT				●
2,120	CfO_Counter1event0config	UINT				●
2,116	CfO_Counter1event0mode	USINT				●
2,144	CfO_Counter1event1IDwr	UINT				●
2,152	CfO_Counter1event1config	UINT				●
2,148	CfO_Counter1event1mode	USINT				●
2,304	CfO_Counter2config	USINT				●
2,312	CfO_Counter2configReg0	USINT				●
2,314	CfO_Counter2configReg1	USINT				●
2,368	CfO_Counter2event0IDwr	UINT				●
2,376	CfO_Counter2event0config	UINT				●
2,372	CfO_Counter2event0mode	USINT				●
2,400	CfO_Counter2event1IDwr	UINT				●
2,408	CfO_Counter2event1config	UINT				●
2,404	CfO_Counter2event1mode	USINT				●
Configuration - Inputs for SSI encoders						
7,176	CfO_SSI1cfg	UINT				●

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
7,180	CfO_SSI1control	USINT				●
7,168	CfO_SSI1eventIDwr	UINT				●
7,232	CfO_SSI1event0IDwr	UINT				●
7,240	CfO_SSI1event0config	UINT				●
7,236	CfO_SSI1event0mode	USINT				●
7,172	ConfigAdvanced01	UDINT				●
Configuration - Comparator function for ABR, AB, SSI encoders and up/down counters						
256	CfO_OutClearMask	USINT				●
258	CfO_OutSetMask	USINT				●
1,024	CfO_DIREKTIOoutevent0IDwr	UINT				●
1,034	CfO_DIREKTIOoutsetmask0	USINT				●
1,032	CfO_DIREKTIOoutclearmask0	USINT				●
1,066	CfO_DIREKTIOoutsetmask1	USINT				●
1,064	CfO_DIREKTIOoutclearmask1	USINT				●
1,056	CfO_DIREKTIOoutevent1IDwr	UINT				●
Configuration - Outputs for PWM (pulse width modulation)						
6,144	CfO_PWM0prescaler	UINT				●
6,160	CfO_PWM1prescaler	UINT				●
Module communication - General						
40	Status of encoder supply	USINT	●			
	PowerSupply01	Bit 0				
Communication - Digital inputs						
264	Input states of the channels	USINT	●			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput04	Bit 3				
Communication - Event counters						
2,080	EventCounter01	U(D)INT	●			
2,084	EventCounter02	U(D)INT	●			
2,336	EventCounter03	U(D)INT	●			
2,340	EventCounter04	U(D)INT	●			
Communication - Input for ABR encoders (optionally with comparator)						
2,080	ABREncoder01	(D)INT	●			
2,116	ReferenceModeABR01	USINT			●	
2,160	OriginComparator01	(D)INT			●	
2,164	MarginComparator01	U(D)INT			●	
264	Input states of the channels	USINT	●			
	ReferenceEnableSwitch01 (without comparator) ComparatorActualValue01 (with comparator)	Bit 3				
2,172	Latch01ABR01	(D)INT	●			
2,118	StatusABR01	USINT	●			
Communication - Input for AB						
2,080	ABEncoder01	(D)INT	●			
2,336	ABEncoder02	(D)INT	●			
2,160	OriginComparator01	(D)INT			●	
2,164	MarginComparator01	U(D)INT			●	
264	Input states of the channels	USINT	●			
	ComparatorActualValue01	Bit 3				
2,140	Latch01AB01	(D)INT	●			
2,172	Latch02AB01	(D)INT	●			
2,396	Latch01AB02	(D)INT	●			
2,428	Latch02AB02	(D)INT	●			
Communication - Up/down counters						
2,080	Counter01	U(D)INT	●			
2,336	Counter02	U(D)INT	●			
2,160	OriginComparator01	U(D)INT			●	
2,164	MarginComparator01	U(D)INT			●	
264	Input states of the channels	USINT	●			
	ComparatorActualValue01	Bit 3				
2,140	Latch01Counter01	U(D)INT	●			
2,172	Latch02Counter01	U(D)INT	●			
2,396	Latch01Counter02	U(D)INT	●			
2,428	Latch02Counter02	U(D)INT	●			
Communication - Input for SSI encoders						
7,184	SSIEncoder01	UDINT	●			
7,248	OriginComparator01	UDINT			●	
7,252	MarginComparator01	UDINT			●	
264	Input states of the channels	USINT	●			
	ComparatorActualValue01	Bit 3				
7,260	Latch01SSI01	UDINT	●			
Communication - Digital outputs						
260	Output states of the channels	USINT			●	
	DigitalOutput02	Bit 1				
	DigitalOutput04	Bit 3				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
264	Input states of the channels	USINT	●			
	StatusDigitalOutput02	Bit 1				
	StatusDigitalOutput04	Bit 3				
Communication - Outputs for PWM (pulse width modulation)						
6,146	PWMOutput02	UINT			●	
6,162	PWMOutput04	UINT			●	
Configuration - Edge detection						
4,104	CfO_EdgeDetectFalling	USINT				●
4,106	CfO_EdeDetectRising	USINT				●
4,108	CfO_FallingDisProtection	USINT				●
4,110	CfO_RisingDisProtection	USINT				●
Configuration - Time measurement						
4,336	CfO_EdgeTimeglobalenable	USINT				●
4344 + N * 8	CfO_EdgeTimeFallingMode0N (Index N = 1 to 4)	UINT				●
4472 + N * 8	CfO_EdgeTimeRisingMode0N (Index N = 1 to 4)	UINT				●
Communication - Time measurement						
4,342	Trigger rising edge detection	USINT			●	
	TriggerRisingCH01	Bit 0				
	...	...				
	TriggerRisingCH04	Bit 3				
4,350	Show first rising trigger edge	USINT	●			
	BusyTriggerRisingCH01	Bit 0				
	...	...				
	BusyTriggerRisingCH04	Bit 3				
4,340	Trigger falling edge detection	USINT			●	
	TriggerFallingCH01	Bit 0				
	...	...				
	TriggerFallingCH04	Bit 3				
4,348	Show first falling trigger edge	USINT	●			
	BusyTriggerFallingCH01	Bit 0				
	...	...				
	BusyTriggerFallingCH04	Bit 3				
4474 + N * 8	CountRisingCH0N (Index N = 1 to 4)	USINT	●			
4476 + N * 8	TimeStampRisingCH0N (Index N = 1 to 4)	UINT	●			
4478 + N * 8	TimeDiffRisingCH0N (Index N = 1 to 4)	UINT	●			
4346 + N * 8	CountFallingCH0N (Index N = 1 to 4)	USINT	●			
4348 + N * 8	TimeStampFallingCH0N (Index N = 1 to 4)	UINT	●			
4350 + N * 8	TimeDiffFallingCH0N (Index N = 1 to 4)	UINT	●			

4.11.14.13.3 Function model 254 - Bus controller

Unlike the function models 0 and 1, this model only offers a selection of functions with a limited scope of configuration on the module.

The following functions are provided and can be run at the same time:

- 2 event counter with configurable counting direction
- 2 PWM outputs

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
(N-1) * 2	-	CfO_CFGchannel0N (Index N = 1 to 4)	USINT				●
64 + N * 2	-	CfO_LEDNsource (Index N = 0 to 3)	USINT				●
2,056	-	CfO_Counter1configReg0	USINT				●
2,312	-	CfO_Counter2configReg0	USINT				●
Communication							
2,080	0	EventCounter01	UINT	●			
2,336	2	EventCounter03	UINT	●			
6,146	0	PWMOutput02	UINT			●	
6,162	2	PWMOutput04	UINT			●	
40	4	Status of encoder supply	USINT	●			
		PowerSupply01	Bit 0				

1) The offset specifies the position of the register within the CAN object.

4.11.14.13.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.14.13.4 General module registers

4.11.14.13.4.1 Configuring LED status indicators

Name:
CfO_LED0source to CfO_LED3source

These registers can be used to define how the module's LED status indicators are used. Blinking patterns can be generated from the application, and the status of the physical inputs and outputs can be indicated.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	MODE = 0	0	LED off
		1	Blinking quickly
		2	Blinking
		3	Blinking slowly
		4	Single flash
		5	Double flash
		6 to 15	Reserved
	MODE = 1 (inverted)	0	LED on
		1	Blinking quickly
		2	Blinking
		3	Blinking slowly
		4	Single flash
		5	Double flash
		6 to 15	Reserved
	MODE = 2	0 to 3	Number of the physical input channel
		4 to 15	Reserved
	MODE = 3	0 to 3	Number of the physical output channel
		4 to 15	Reserved
4 - 7	Selection of the mode for the LED status indicator	0	LED blinking pattern
		1	Inverted LED blinking pattern
		2	Displays a channel's physical input status
		3	Displays a channel's physical output status
		4 to 15	Reserved

4.11.14.13.4.2 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.11.14.13.5 Digital inputs and outputs

4.11.14.13.5.1 Configure physical channels

Name:
CfO_CFGchannel01 to CfO_CFGchannel04

This register can be used to configure physical I/O channels 1 to 4.

Information:

Except for bit 2 (inverted input), all other bits are only available for channels 2 and 4.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Push[1)]	0	Disabled
		1	Enabled
1	Pull[1)]	0	Disabled
		1	Enabled
2	Inverted input	0	Disabled
		1	Enabled
3	Inverted output	0	Disabled
		1	Enabled
4 - 7	Output type	0	Direct I/O
		1 to 5	Reserved
		6	PWM (channel-specific)
		7	SSI clock (channel-specific)

1) To configure a channel as an output, Push and/or Pull must be enabled.

4.11.14.13.5.2 Reset mask of the digital channels

Name:
CfO_OutClearMask

The settings in this register only affect the values written to registers 4.11.14.13.5.5 "DigitalOutput02 and 04".

- 0 allows manual reset of digital outputs using registers DigitalOutput02 and 04
- 1 prevents manual reset of digital outputs using registers DigitalOutput02 and 04

When "1" is used, the "output event function" can be used to reset the outputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	DigitalOutput02	0	Writing 0 to the DigitalOutput02 register resets the output
		1	Writing 0 from the DigitalOutput02 register does not reset the output
2	Reserved	-	
3	DigitalOutput04	0	Writing 0 to the DigitalOutput04 register resets the output
		1	Writing 0 from the DigitalOutput04 register does not reset the output
4 - 7	Reserved	-	

4.11.14.13.5.3 Set mask of the digital channels

Name:
CfO_OutSetMask

The settings in this register only affect the values written to registers 4.11.14.13.5.5 "DigitalOutput02 and 04".

- 0 allows manual setting of digital outputs using registers DigitalOutput02 and 04
- 1 prevents manual setting of digital outputs using registers DigitalOutput02 and 04

When "1" is used, the "output event function" can be used to set the outputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	DigitalOutput02	0	Writing 1 to the DigitalOutput02 register sets the output
		1	Writing 1 from the DigitalOutput02 register does not set the output
2	Reserved	-	
3	DigitalOutput04	0	Writing 1 to the DigitalOutput04 register sets the output
		1	Writing 1 from the DigitalOutput04 register does not set the output
4 - 7	Reserved	-	

4.11.14.13.5.4 Input states of the channels

Name:
see "Name in the AS I/O configuration"

This register reads the input status of a physical channel. The polarity settings are accounted for in the value (bit 2 in 4.11.14.13.5.1 "CfO_CFGchannel[x]" register).

The bits in this register are shown in the AS I/O mapping table under different names based on the function used in order to improve readability.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Physical input channel	Value	Name in the AS I/O configuration
0	Channel 1	0 or 1	DigitalInput01
1	Channel 2	0 or 1	DigitalInput02 StatusDigitalOutput02
2	Channel 3	0 or 1	DigitalInput03
3	Channel 4	0 or 1	DigitalInput04 StatusDigitalOutput04 ReferenceEnableSwitch01 ComparatorActualValue01
4 - 7	Reserved	-	

4.11.14.13.5.5 Output states of the channels

Name:
DigitalOutput02 and DigitalOutput04

The output status of a physical channel can be written using this register. In order to configure a channel as an output:

1 Bit 0 "Push" and/or bit 1 "Pull" must be enabled in the 4.11.14.13.5.1 "CfO_CFGchannel[x]" register.
2 Bits 4 to 7 in the 4.11.14.13.5.1 "CfO_CFGchannel[x]" register must be set to Direct I/O.
3 0 must be set for the respective channel in the 4.11.14.13.5.2 "CfO_OutClearMask" and 4.11.14.13.5.3 "CfO_OutSetMask" registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	DigitalOutput02	0 or 1	Output status of channel 2
2	Reserved	-	
3	DigitalOutput04	0 or 1	Output status of channel 4
4 - 7	Reserved	-	

4.11.14.13.6 Event functions

The module provides configurable event functions. An event function can be connected to physical I/O and the values derived from them (e.g. counters) or be purely used for internal processing.

Every event function has event inputs and outputs. Event functions can also have only inputs or only outputs. Each event output has a unique event ID. It is possible to configure when an event should be generated on an event output. The effect of an event is determined by the respective event function.

Event functions can also be linked to one another. The link takes place using the event input. Every event input has a 16-bit register to which the event number of the linked event output is written.

Information:

The module functions that can be configured in the AS I/O configuration are primarily based on these event functions and their links. Changes in the AS I/O configuration have multiple effects on event functions and their links.

4.11.14.13.6.1 List of event IDs

Various hardware and software functions send event IDs or require event IDs in order to start. The following table shows all of the IDs available to configure the module.

Event ID	Description	
Direct event inputs		
512	Comparator condition	FALSE
513	Comparator condition	TRUE
Counter comparator function		
2,112	Counter function 1	Event function 1; FALSE
2,113		Event function 1; TRUE
2,144		Event function 2; FALSE
2,145		Event function 2; TRUE
2,368	Counter function 2	Event function 1; FALSE
2,369		Event function 1; TRUE
2,400		Event function 2; FALSE
2,401		Event function 2; TRUE
Edge events		
4,096	Falling edge on I/O channel	Channel 1
...		...
4,099		Channel 4
4,112	Rising edge on I/O channel	Channel 1
...		...
4,115		Channel 4
4,128	Rising or falling edge on I/O channel	Channel 1
...		...
4,131		Channel 4
SSI counter events		
7,168	SSI valid	
7,169	SSI ready	
SSI comparator events		
7,232	SSI 1 comparator condition	FALSE
7,233		TRUE
Timerevents		
208	Timer1	50 µs
209	Timer2	100 µs
210	Timer3	200 µs
211	Timer4	400 µs
212	Timer5	800 µs
213	Timer6	1600 µs
214	Timer7	3200 µs
215	Timer8	3200 µs (time offset to timer 7)
Network functions		
224	SOAISOP (**s**ynchronous **o**ut **a**synchronous **i**n **s**tart of **p**rotocol)	
225	AOSISOP (**a**synchronous **o**ut **s**ynchronous **i**n **st**art of **p**rotocol)	
226	SOAIEOP (**s**ynchronous **o**ut **a**synchronous **i**n **e**nd of **p**rotocol)	
227	AOSIEOP (**a**synchronous **o**ut synchronous **i**n **e**nd of **p**rotocol)	
Idle event		
192	No-load operation	

Timer

There are 8 timer events that the module can generate.

Information:

The timers have the highest event priority. All other system functions are interrupted when a timer event occurs, and jitter for the amount of time it takes to process the event.

Idle event

Idle time is the time that remains after the system has processed all higher priority events and operations. The module performs the following functions during idle time:

- Handling of the asynchronous protocol
- Mechanism for (re-)linking events
- Operation of LEDs
- Execution of event event functions linked to the idle function

4.11.14.13.6.2 Edge events

For each physical input channel there are 3 event functions

- Falling edge
- Rising edge
- Falling and rising edge

The respective event is triggered when an edge is detected on the hardware input and the "CfO_EdgeDetectRising" and/or "CfO_EdgeDetectFalling" register has been configured for the respective channel.

Edges are detected by the hardware and processed for each interrupt. The interrupt handler uses an event distributor, which requires a specific amount of time for each edge to operate the hardware and execute linked event functions. To reduce this time, edge detection can be enabled/disabled individually for each channel. To optimize system load and I/O jitter, it is important to only enable edge detection where it is actually needed.

Information:

Edge detection can also be used for channels that are configured as outputs.

Event frequency limitation

To stabilize the system, there is a mechanism that limits the number of events created through edge recognition. At least one idle event must occur between two edge events for the same edge.

The "CfO_FallingDisProtection" and "CfO_RisingDisProtection" registers can be used to disable this limitation for each edge, and then an event will be generated for every edge. However, this can cause a system overload, i.e. I/O operation can fail for up to 100 ms before the module changes to the reset state.

Generate event on falling edge

Name:
CfO_EdgeDetectFalling

This register defines whether an event is generated on a falling edge.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	No event generated on falling edge.
		1	Events 4096 and 4128 are generated on falling edge.
...		...	
3	Channel 4	0	No event generated on falling edge.
		1	Events 4099 and 4131 are generated on falling edge.
4 - 7	Reserved	-	

Generate event on rising edge

Name:
CfO_EdgeDetectRising

This register defines whether an event is generated on a rising edge.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	No event generated on rising edge.
		1	Events 4112 and 4128 are generated on rising edge.
...		...	
3	Channel 4	0	No event generated on rising edge.
		1	Events 4115 and 4131 are generated on rising edge.
4 - 7	Reserved	-	

Enable limit for falling edges

Name:
CfO_FallingDisProtection

This register can be used to enable/disable the event frequency limit for falling edges on the respective channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Event frequency limit enabled.
		1	Event frequency limit disabled.
...		...	
3	Channel 4	0	Event frequency limit enabled.
		1	Event frequency limit disabled.
4 - 7	Reserved	-	

Enable limit for rising edges

Name:
CfO_RisingDisProtection

This register can be used to enable/disable the event frequency limit for rising edges on the respective channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Event frequency limit enabled.
		1	Event frequency limit disabled.
...		...	
3	Channel 4	0	Event frequency limit enabled.
		1	Event frequency limit disabled.
4 - 7	Reserved	-	

4.11.14.13.6.3 Direct input function

The module features a direct input function.

This event function is based on comparator functionality. If the event configured in the "CfO_DIREKTIOevent0IDwr" register occurs, the event function compares the status of all Direct I/O channels enabled in the "CfO_EvComp-Mask" register to a status defined in the "CfO_DIREKTIOeventcompState" register. The event that is generated depends on the results of this comparison.

- If the respective bits are the same, then event number 513 is generated
- If the respective bits are different, then event number 512 is generated

Configure event ID for input function

Name:
CfO_DIREKTIOevent0IDwr

This register holds the event ID generated by the direct input function. For a list of all possible event IDs, see 4.11.14.13.6.1 "List of event IDs"

Data type	Value	Information
INT	192 to 7,233	ID of event function

Configure the mode of the input function

Name:
CfO_DIREKTIOevent0mode

The mode in which the direct input function operates can be set in this register.

Comparator functions can be operated in 4 different modes. For a description, see "Comparator modes".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Single
		2	State change
		3	Continuous
2 - 7	Reserved	-	

Comparator status for comparator mask

Name:
CfO_DIREKTIOevent0compState

This register contains the status bits that are compared with the bits specified in the "CfO_Ev0CompMask" register, which contain the I/O input status, when an event is received.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator status of channel 1	0 or 1	
...		...	
3	Comparator status of channel 4	0 or 1	
4 - 7	Reserved	-	

Configure the comparator mask for the input function

Name:
CfO_Ev0CompMask

If a bit is set, then the input status of the respective channel is compared with that bit in the "CfO_DIREKTIOeventcompState" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Do not compare bit
		1	Compare bit in register
...		...	
3	Channel 4	0	Do not compare bit
		1	Compare bit in register
4 - 7	Reserved	0	

4.11.14.13.6.4 Direct output functions

The module has 2 of these event functions

The effect of executing this event function is similar to writing to the 4.11.14.13.5.5 "DigitalOutput02 and 04" registers. When this event function is triggered, however, the changed output states are passed on to the hardware immediately, regardless of the X2X cycle.

When this event function is used, the masks of the respective outputs (see 4.11.14.13.5.2 "CfO_OutClearMask" and 4.11.14.13.5.3 "CfO_OutSetMask" registers) must be set to 1. Otherwise the output status would constantly be overwritten by the values in the 4.11.14.13.5.5 "DigitalOutput02 and 04" registers.

Configure event ID for output function

Name:
CfO_DIREKTIOevent0IDwr to CfO_DIREKTIOevent1IDwr

These registers hold the event IDs that trigger the direct output function. For a list of all possible event IDs, see 4.11.14.13.6.1 "List of event IDs"

Data type	Value	Information
INT	192 to 7,233	ID of event function

Configure channels for resetting

Name:
CfO_DIREKTIOoutclearmask0 to CfO_DIREKTIOoutclearmask1

Writing "1" to the bit position that corresponds to a channel resets the output if the output event function is being executed. This corresponds to writing "0" to the 4.11.14.13.5.5 "DigitalOutput 02 and 04" registers.

The bit that corresponds to channels that should be reset should be set to "1" in the 4.11.14.13.5.2 "CfO_OutClearMask" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	Channel 2	0	Reset channel 2
		1	Do not reset channel 2
2	Reserved	-	
3	Channel 4	0	Reset channel 4
		1	Do not reset channel 4
4 - 7	Reserved	-	

Configure channels for setting

Name:
CfO_DIREKTIOoutsetmask0 to CfO_DIREKTIOoutsetmask1

Writing "1" to the bit position that corresponds to a channel sets the output if the output event function is being executed. This corresponds to writing "1" to the 4.11.14.13.5.5 "DigitalOutput 02 and 04" registers.

The bit that corresponds to channels that should be reset should be set to "1" in the 4.11.14.13.5.3 "CfO_OutSet-Mask" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	Channel 2	0	Set channel 2
		1	Do not set channel 2
2	Reserved	-	
3	Channel 4	0	Set channel 4
		1	Do not set channel 4
4	Reserved	-	

4.11.14.13.7 Counters and encoders

The module has 2 internal counter functions, each with 2 event counter registers. Each of these 2 counters is permanently assigned to 2 physical inputs. This assignment cannot be changed.

The counter registers perform different functions based on how the event functions are connected. The counter registers can be configured in the following ways:

- ABR counter
- AB counter
- Up/down counters
- Event counters

Different names are used for them in Automation Studio and in the register description to improve clarity.

Channel	Counter function	Counter register	Name in AS
1	1	1	ABEncoder01 ABREncoder01 Counter01 EventCounter01
2		2	EventCounter02
3	2	1	ABEncoder02 Counter02 EventCounter03
4		2	EventCounter04

4.11.14.13.7.1 Counter value calculation

There are 3 steps for calculating the state of any counter function

1. The counter value is based on the 2 absolute value counters "abs1" and "abs2". They are only used internally in the module and cannot be read. Depending on the mode, these registers show the respective physical input signals.

	Mode		
	Edge counters	AB encoders	Up/down counter
abs1	Edges of counter channel 1	Increments in positive direction	Counter channel 2 = 0: Edges of counter channel 1 in up direction
abs2	Edges of counter channel 2	Increments in negative direction	Counter channel 2 = 1 Edges of counter channel 1 in down direction

2. From the absolute value registers "abs1" and "abs2", 2 more counters are formed: "counter 1" and "counter 2". These are only used internally in the module and cannot be read. The following values are used for the calculation:

- Absolute value registers "abs1" and "abs2"
- SW_reference_counter 1 and 2: This reference value can be defined by the "CfO_CounterPresetValue" register to allow referencing <> 0.
- HW_reference_counter 1 and 2: In the "CfO_CounterEventMode" register, you can configure whether latched values should be copied to these registers when counter events occur.

counter1 = abs1 + SW_reference_counter1 - HW_reference_counter1
counter2 = abs2 + SW_reference_counter2 - HW_reference_counter2

3. The counter registers contain the sum of the two internal counters "counter 1" and "counter 2". The "CfO_CounterConfigReg" register allows you to define a sign for each "counter" register and define whether or not it should be used.

Counter register = counter1 + counter2

4.11.14.13.7.2 Sample configurations

All of the settings available in Automation Studio for AB encoders, ABR encoders, up/down counters and event counters are based on the two counter functions.
The following configuration examples show the values with which Automation Studio initializes the module registers in order to implement these functions.

I/O configuration - AB encoder

The following table shows how the module's various event functions can be linked in order to configure an AB encoder.

[x] stands for the respective counter function, either 1 or 2

Register	Value	Comment
For the function		
CfO_Counter[x]config	0x01	Mode = Up/down counter
CfO_Counter[x]configReg0	0x0D	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.14.13.7.1 "Counter value calculation" and "Examples of calculation configurations")
For the latch		
CfO_Counter[x]event0config	0x000D	Configuration of the calculation of the first value used for the latch
CfO_Counter[x]event0mode	0x03	Mode of the first counter event function - Continuous
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger Latch 1 ("Latch 01 - Channel" in the AS I/O configuration).
CfO_Counter[x]event1config	0x0D	Configuration of the calculation of the second value used for the latch
CfO_Counter[x]event1mode	0x03	Mode of the second counter event function - Continuous
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger Latch 2
For the comparator		
CfO_Counter1event1IDwr	0x00D0	Event number of Timer 1 (50 µs) **Information:** **The latch and comparator must not have the same event number!**
CfO_Counter1event1config	0x900D or 0xA00D	Configuration of the comparator for the second counter event
CfO_Counter1event1mode	0x03	Mode of the second counter event function - Continuous
CfO_DIREKTIOoutevent0IDwr	0x0861	TRUE event output of the second counter to trigger the direct output function (set outputs).
CfO_DIREKTIOoutsetmask0	0x08, 0x20, 0x80	Outputs that should be set when comparator condition = TRUE
CfO_DIREKTIOoutevent1IDwr	0x0860	FALSE event output of the second counter to trigger the direct output function (reset outputs).
CfO_DIREKTIOoutclearmask1	0x08, 0x20, 0x80	Outputs that should be reset when comparator condition = FALSE

I/O configuration - ABR encoder

The following table shows how the module's various event functions can be linked in order to configure an ABR encoder.

Register	Value	Comment
For the function		
CfO_Counter1PresetValue1	(any)	Desired offset value for referencing
CfO_Counter1event0IDwr	0x0201	Link between the first counter event and the "direct input" comparator condition TRUE
CfO_Counter1config	0x01	Mode = AB encoder
CfO_Counter1configReg0	0x0D	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.14.13.7.1 "Counter value calculation" and "Examples of calculation configurations")
CfO_DIREKTIOevent0IDwr	0x1002 or 0x1012	Selection of the desired input edge as trigger for the ABR encoder function
CfO_Counter1event0config	0x0000	Configuration of the first counter event (for referencing)
CfO_DIREKTIOevent0mode	0x03	Mode of the "direct input function" - Continuous
CfO_DIREKTIOevent0compState	0x00 or 0x08	Comparator status for the "direct input function"
CfO_Ev0CompMask	0x08	Comparator mask for the "direct input function"
For the latch		
CfO_Counter1event0config	0x000D	Configuration of the calculation of the value used for the latch
CfO_Counter1event0mode	0x03	Mode of the first counter event function - Continuous
CfO_Counter1event0IDwr	(any)	Number of the event that should trigger the latch
For the comparator		
CfO_Counter1event1IDwr	0x00D0	Event number of Timer 1 (50 µs) **Information:** **The latch and comparator must not have the same event number!**
CfO_Counter1event1config	0x900D or 0xA00D	Configuration of the comparator for the second counter event
CfO_Counter1event1mode	0x03	Mode of the second counter event function - Continuous
CfO_DIREKTIOoutevent0IDwr	0x0861	TRUE event output of the second counter to trigger the direct output function (set outputs).
CfO_DIREKTIOoutsetmask0	0x08, 0x20, 0x80	Outputs that should be set when comparator condition = TRUE
CfO_DIREKTIOoutevent1IDwr	0x0860	FALSE event output of the second counter to trigger the direct output function (reset outputs).
CfO_DIREKTIOoutclearmask1	0x08, 0x20, 0x80	Outputs that should be reset when comparator condition = FALSE

I/O configuration - Up/down counter

The following table shows how the module's various event functions can be linked in order to configure an up/down counter.

[x] stands for the respective counter function, either 1 or 2

Register	Value	Comment
For the function		
CfO_Counter[x]config	0x03	Counter mode = Up/down counter
CfO_Counter[x]configReg0	0x0D, 0x07	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.14.13.7.1 "Counter value calculation" and "Examples of calculation configurations")
For the latch		
CfO_Counter[x]event0config	0x0D, 0x07	Configuration of the calculation of the first value used for the latch
CfO_Counter[x]event0mode	0x03	Mode of the first counter function - Continuous
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger Latch 1
CfO_Counter[x]event1config	0x0D, 0x07	Configuration of the calculation of the second value used for the latch
CfO_Counter[x]event1mode	0x03	Mode of the second counter function - Continuous
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger Latch 2
For the comparator		
CfO_Counter1event1IDwr	0x00D0	Event number of Timer 1 (50 µs) **Information:** **The latch and comparator must not have the same event number!**
CfO_Counter1event1config	0x900D, 0xA00D or 0x9007, 0xA007	Configuration of the comparator for the second counter event
CfO_Counter1event1mode	0x03	Mode of the second counter event function - Continuous
CfO_DIREKTIOoutevent0IDwr	0x0861	TRUE event output of the second counter to trigger the direct output function (set outputs).
CfO_DIREKTIOoutsetmask0	0x08, 0x20, 0x80	Outputs that should be set when comparator condition = TRUE
CfO_DIREKTIOoutevent1IDwr	0x0860	FALSE event output of the second counter to trigger the direct output function (reset outputs).
CfO_DIREKTIOoutclearmask1	0x08, 0x20, 0x80	Outputs that should be reset when comparator condition = FALSE

I/O configuration - Event counter

The following table shows how the module's various event functions can be linked in order to configure an event counter.

[x] stands for the respective counter function, either 1 or 2

Register	Value	Comment
For event counters on channels 1 and 3		
CfO_Counter[x]configReg0	0x01 or 0x03	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.14.13.7.1 "Counter value calculation" and "Examples of calculation configurations")
CfO_Counter[x]event0mode	0x43	Mode of the first counter event function and referencing configuration
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger referencing
For event counters on channels 2 and 4		
CfO_Counter[x]configReg1	0x04 or 0x08	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.14.13.7.1 "Counter value calculation" and "Examples of calculation configurations")
CfO_Counter[x]event1mode	0x83	Mode of the second counter event function and referencing configuration
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger referencing

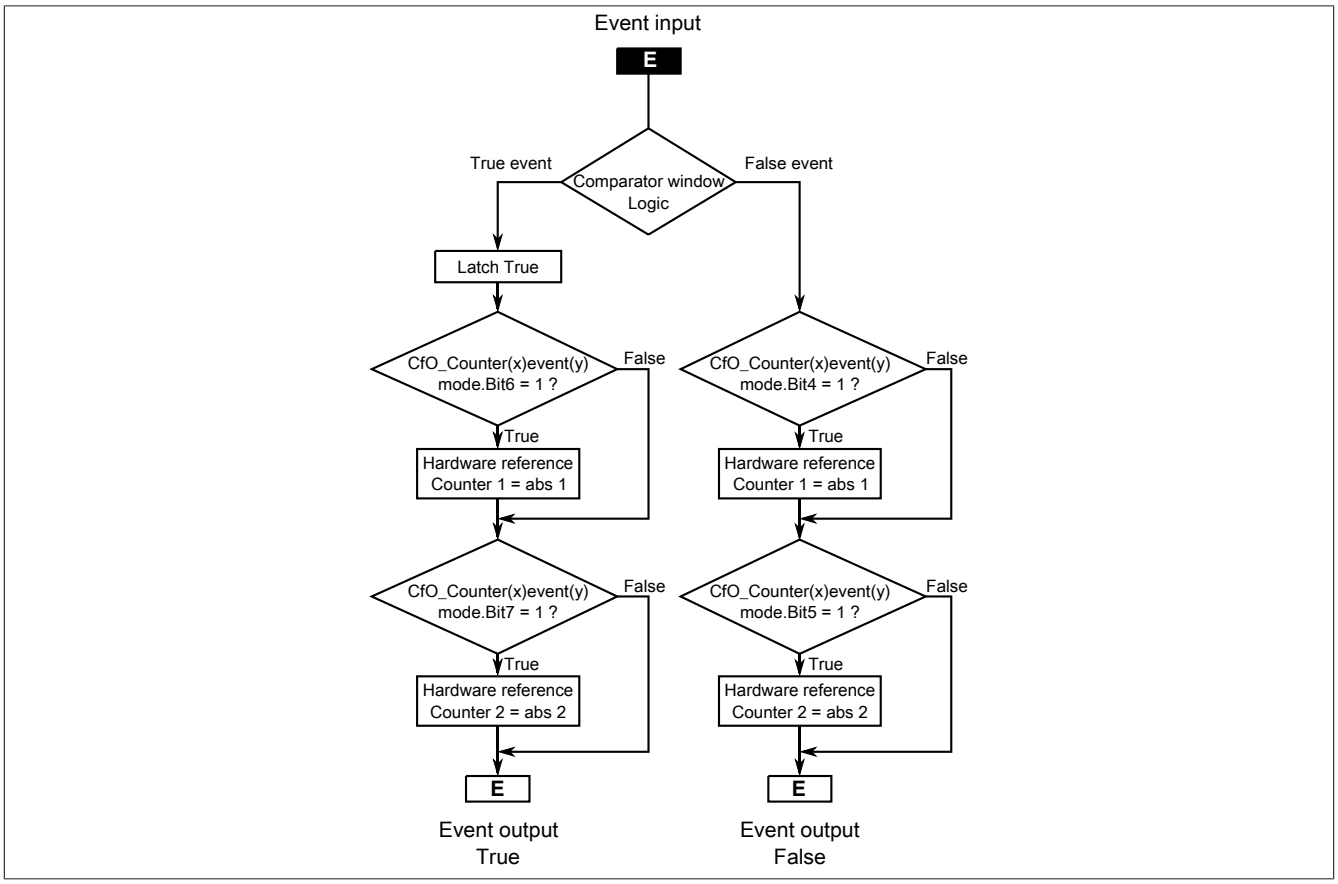
4.11.14.13.7.3 General event functions

Each of the 2 counter functions has 2 counter event functions. These consist of:

- Event ID that triggers the counter event function
- A window comparator
- Latch register for saving the counter value

When the counter event function is complete, a combined event ID in the range 2112 to 2401 (see 4.11.14.13.6.1 "List of event IDs") is sent.

Each counter event function also has the option to copy the current counter value to the "HW reference counter" when an event occurs (see 4.11.14.13.7.1 "Counter value calculation").



Configure counter mode

Name:
Counter function 1: CfO_Counter1config
Counter function 2: CfO_Counter2config

These registers are used to configure the mode of the counter function. Each counter function can be operated in 3 different modes.

	Counter function mode		
	Edge counters	**AB encoder**	**Up/down counter**
Counter channel 1[1)]	Counting pulses, edge counter 1	A	Metering pulses
Counter channel 2[1)]	Counting pulses, edge counter 2	B	Counting direction (0 = positive, 1 = negative)
Counter register 1	Counter value 1	Position	Counter value
Counter register 2	Counter value 2		

1) Corresponds to the physical channels of the counter functions. See 4.11.14.8.1 "Description of channel assignments".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Counter mode	00	Edge counters
		01	AB encoder
		11	Up/down counter
2 - 7	Reserved	-	

Configure calculation of internal counters

Name:
Counter function 1: CfO_Counter1configReg0 to CfO_Counter2configReg0
Counter function 2: CfO_Counter1configReg1 to CfO_Counter2configReg1

The calculation of the internal "counter1" and "counter2" registers can be configured in these registers. For information on using these internal registers, see 4.11.14.13.7.1 "Counter value calculation".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	counter 1 - use	0	0 is added instead of "counter 1"
		1	"counter 1" is used for addition
1	counter 1 - sign	0	The sign of the "counter 1" register is not changed for addition
		1	The sign of the "counter 1" register is reversed for addition
2	counter 2 - use	0	0 is added instead of "counter 2"
		1	"counter 2" is used for addition
3	counter 2 - sign	0	The sign of the "counter 2" register is not changed for addition
		1	The sign of the "counter 2" register is reversed for addition
4 - 7	Reserved	-	

Examples of calculation configurations

0b00000001	= 0x01	Only the "counter1 - use" bit is set, entering the contents of the "counter" (edge of counter event channel 1) directly in the counter register.
0b00000011	= 0x03	"counter 1 - use" and "counter1 - sign" bits are set. The sign is changed so that the counter register counts in the negative direction.
0b00001101	= 0x0d	Edges on counter input channel 1 increase the value in the counter register. Edges on counter input channel 2 decrease the value in the counter register. This value is the best setting for the modes "AB encoder" and "Up/down counter".

Offset value for referencing

Name:

Counter function 1: CfO_Counter1PresetValue1 to CfO_Counter2PresetValue1
Counter function 1: CfO_Counter1PresetValue1_32Bit to CfO_Counter2PresetValue1_32Bit

Counter function 2: CfO_Counter1PresetValue2 to CfO_Counter1PresetValue2
Counter function 2: CfO_Counter1PresetValue2_32Bit to CfO_Counter1PresetValue2_32Bit

"Preset value" in the AS I/O configuration.

These registers can be used to define an offset value for referencing. This value is copied to the internal SW_reference_counter register of the respective counter register.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

Counter register

Name:
Different names are used for these 4 registers depending on their function.

These 4 registers show the results of the counter value calculation for the respective register. Depending on the function, this corresponds to either the encoder position or the counter value.

For information on the relationship between physical channels and counter registers, see 4.11.14.13.7 "Counters and encoders" and 4.11.14.8.1 "Description of channel assignments"

Counter function 1		
Counter register	**Function**	**Name**
1	**AB encoders**	ABEncoder01
	ABR encoders	ABREncoder01
	Up/down counters	Counter01
	Event counters	EventCounter01
2	**Event counters**	EventCounter02

Counter function 2		
Counter register	**Function**	**Name**
1	**AB encoders**	ABEncoder02
	Up/down counters	Counter02
	Event counters	EventCounter03
2	**Event counters**	EventCounter04

Data type	Value	Information
INT	-32,768 to 32,767	Encoder position or counter value
DINT[1)]	-2,147,483,648 to 2,147,483,647	Encoder position or counter value

1) Only in function model 1

Status of the ABR encoder

Name:
StatusABR01

The referencing status of the ABR encoder is shown in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	0	
2	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
3	State change when referencing is complete	0 or 1	
4	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
5 - 7	Continuous counter	xxx	Increased with each reference pulse

Examples of possible values

0b00000000	= 0x00	Referencing OFF or homing procedure already active
0b00111100	= 0x3C	First reference complete, reference value applied in the "ABREncoder0" register
0bxxx11100	= 0xxB	Bits 5 to 7 are changed with each reference pulse
0bxxx1x100	= 0xxx	Bits changed continuously with the setting continuous referencing. With every reference pulse, the reference value is applied to the "ABREncoder0" register

Configure ABR referencing mode

Name:
ReferenceModeABR01

The bits in this register are used to configure the reaction to the configured reference pulse.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Sets the referencing mode	00	Referencing OFF
		01	Single shot referencing
		10	Reserved
		11	Continuous referencing
2 - 5	Reserved	-	
6 - 7	Reserved	11	Must always be 11!

This results in the following values:

0b00000000	= 0x00	Referencing OFF
0b11000001	= 0xC1	Single shot referencing → When starting over after the referencing process is complete, the value 0x00 must be written to start again. Wait until the "StatusABR" register also takes on the value 0x00, then the value 0xC1 can be written again.
0b11000011	= 0xC3	Continuous referencing → Referencing takes place automatically with every reference pulse

4.11.14.13.7.4 Comparator functions

The ABR and AB encoders and the up/down counter have a comparator function. It always works the same and is described here globally for all three.

The comparators are implemented in software form. They do not work actively but rather passively, i.e. the comparison is only carried out when an event is received. The event received is forwarded along the TRUE or FALSE branch depending on the status of the comparator condition. An event function like this generally also offers a latch for the TRUE and FALSE branch to save the value used for the comparator at the time of the event.

Comparator modes

Comparator functions can be operated in 4 different modes.

- **Off**
  Events are ignored.
- **Single**
  The event function is executed once and then disables itself automatically. To re-enable it, the "event function mode" must be changed, preferably to "off" and then to the desired mode. This setting allows a hardware latch to be simulated.
- **State change**
  The event function only responds when the comparator status has changed, i.e. from false to true (or vice versa). Only the first event for each status is processed, e.g. the first "true" of a sequence of events with the comparator condition "true". After the event function is enabled, the first incoming event is used to determine the starting status and therefore not forwarded. This setting allows a hardware comparator to be simulated.
- **Continuous**
  Each incoming event is forwarded to the true or false branch depending on the comparator condition. This setting allows event filters to be created.

Configure event ID for comparator

Name:
Counter function 1: CfO_Counter1event0IDwr to CfO_Counter1event1IDwr
Counter function 2: CfO_Counter2event0IDwr to CfO_Counter2event1IDwr

This register holds the event ID that should trigger the counter event function. For a list of all possible event IDs, see 4.11.14.13.6.1 "List of event IDs"

Data type	Value	Information
INT	192 to 7,233	ID of counter event function

Configure calculation of comparator

Name:
Counter function 1: CfO_Counter1event0config to CfO_Counter1event1config
Counter function 2: CfO_Counter2event0config to CfO_Counter2event1config

These registers are used to configure the counter event function for the respective counter function.

Bits 0 to 3 configure the calculation of the comparison or to latch the value. This calculation is similar to the calculation of the counter register (see 4.11.14.13.7.1 "Counter value calculation")

Bits 8 to 13 can be used to limit the number of bits used for the comparison. A mask is calculated as 2^n - 1 and linked with an "AND" operation. This makes it possible to generate a comparator pulse every 2^n increments.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	counter 1 - use	0	0 is added instead of "counter 1"
		1	"counter 1" is used for addition
1	counter 1 - sign	0	The sign of the "counter 1" register is not changed for addition
		1	The sign of the "counter 1" register is reversed for addition
2	counter 2 - use	0	0 is added instead of "counter 2"
		1	"counter 2" is used for addition
3	counter 1 - sign	0	The sign of the "counter 2" register is not changed for addition
		1	The sign of the "counter 2" register is reversed for addition
4 - 7	Reserved	-	
8 - 13	Number of bits for comparator mask	x	The mask value is calculated as 2^n-1, where n is value set in these bits. Default: 0
14	Reserved	-	
15	Margin comparator mode	0	MarginComparator01 >= (Current position - OriginComparator01)
		1	MarginComparator01 > (Current position - OriginComparator01)

Configure mode and latching of comparator function

Name:
Counter function 1: CfO_Counter1event0mode to CfO_Counter1event1mode
Counter function 2: CfO_Counter2event0mode to CfO_Counter2event1mode

In these registers you can set the mode for the comparator function and optional copying of the latched registers.

Comparator functions can be operated in 4 different modes. For a description, see "Comparator modes".

Bits 4 to 7 can be used to define hardware referencing actions.

Based on these bits, the values of the internal absolute value counters "abs1" and "abs2" can be copied to the respective "HW_reference_counter" register at every counter event (see 4.11.14.13.7.1 "Counter value calculation"). This function can be used to reference the counter values directly in the hardware.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Single
		2	State change
		3	Continuous
2 - 3	Reserved	-	
4	Copy abs1 counter value	0	No action
		1	When event is FALSE → hardware reference counter 1 = abs1
5	Copy abs2 counter value	0	No action
		1	When event is FALSE → hardware reference counter 2 = abs2
6	Copy abs1 counter value	0	No action
		1	When event is TRUE → hardware reference counter 1 = abs1
7	Copy abs2 counter value	0	No action
		1	When event is TRUE → hardware reference counter 2 = abs2

Comparator origin

Name:
OriginComparator01

This register is available for the AB and ABR encoders and the up/down counters.

It defines the position value at which the respective configured comparator output channel is set.

Data type	Value	Information
INT	-32,768 to 32,767	Comparator window origin, 16-bit
DINT	-2,147,483,648 to 2,147,483,647	Comparator window origin, 32-bit

Width of the comparator

Name:
MarginComparator01

This register is available for the AB and ABR encoders and the up/down counters.

It defines the width of the comparator window in the positive direction.

Data type	Value	Information
INT	-32,768 to 32,767	Width of comparator window, 16-bit
DINT	-2,147,483,648 to 2,147,483,647	Width of comparator window, 32-bit

Read latch position or counter value

Name:
Different names are used for these 4 registers depending on their function.

If the comparator returns "TRUE", then the current counter value is latched and copied to these registers. The calculation of the comparator value used for the latch can be configured in the "Configure calculation of comparator" register.

Counter function 1		
Event function	**Function**	**Name**
1	**AB encoders**	Latch01AB01
	Up/down counters	Latch01Counter01
2	**ABR encoders**	Latch01ABR01
	AB encoders	Latch02AB01
	Up/down counters	Latch02Counter01

Counter function 2		
Event function	**Function**	**Name**
1	**AB encoders**	Latch01AB02
	Up/down counters	Latch01Counter02
	Event counters	Latch02AB02
2	**Event counters**	Latch02Counter02

Data type	Value	Information
INT	-32,768 to 32,767	Latched encoder position or counter value
DINT[1)]	-2,147,483,648 to 2,147,483,647	Latched encoder position or counter value

1) Only in function model 1

4.11.14.13.8 SSI encoder interface

The module has 1 SSI encoders available, supported directly in the hardware. Two 24 V output channels are set for the SSI encoder and cannot be changed. (See also 4.11.14.8.1 "Description of channel assignments")

When using the SSI encoder, the corresponding clock channel can be configured in the 4.11.14.13.5.1 "CfO_CFGchannel" register as "Channel-specific" and "Push/Pull".

SSI encoders	Channel number
Data channel	1
Clock channel	2

4.11.14.13.8.1 SSI event functions

The SSI encoder consists of an event function and an event input. The SSI cycle is started when an event is received on this input.

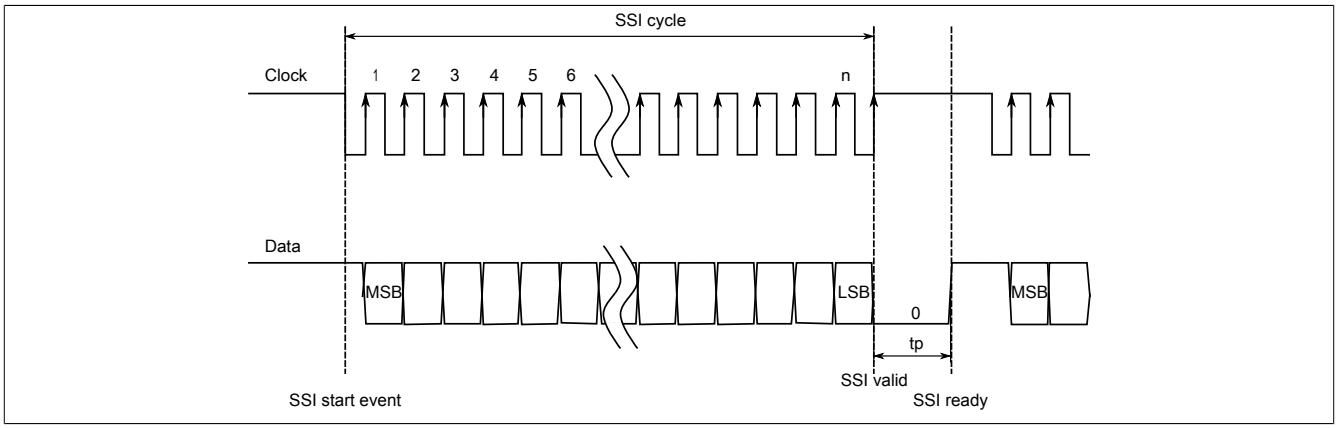
Information:

The SSI event function is not linked to an event by default, i.e. SSI functions are disabled.

Two events are sent from the SSI encoder interface..

- An "SSI valid" event is triggered immediately after the end of the SSI cycle if a new counter value is available.
- The "SSI ready" event then shows when the monoflop time has expired (tp in SSI encoder timing diagram). This is the earliest that the next SSI cycle can be started.

SSI encoder - Timing diagram



Configure event ID for SSI

Name:
CfO_SSI1eventIDwr

This register holds the event ID that should start the SSI cycle. For a list of all possible event IDs, see 4.11.14.13.6.1 "List of event IDs"

Normally this register is set to network event 225 "AOSISOP"- This ensures that the new encoder position is available at the next "I/O → Synchronous Frame" transfer. Check the SSI transfer time and the X2X cycle time, because the SSI cycle must be completed within this time.

Data type	Value	Information
INT	192 to 7,233	ID of event function

Configure SSI

Name:
CfO_SSI1cfg

This configuration register is used to set the coding, the clock rate and the number of bits. Default = 0. This must be set once using an acyclic write command.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	00	1 MHz
		01	500 kHz
		10	250 kHz
		11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding

SSI advanced configuration

Name:
ConfigAdvanced

This configuration register is used to set the coding, the clock rate, the number of bits and the monostable multivibrator settings. Default = 0. This must be set once using an acyclic write command.

It only differs from "CfO_SSI1cfg" by data length and additional monostable multivibrator testing.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	00	1 MHz
		01	500 kHz
		10	250 kHz
		11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding
16 - 17	Monostable multivibrator check	00	Check OFF, no additional clock bit
		01	Check set to High level
		10	Check set to Low level
		11	Level is clocked but ignored
18 - 31	Reserved	0	

Enable SSI event function

Name:
CfO_SSI1control

The two SSI encoder events can be enabled/disabled using this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Event: SSI valid	0	Not sent
		1	Sent
1	Event: SSI ready	0	Not sent
		1	Sent
2 - 7	Reserved	-	

Read SSI position

Name:
SSIEncoder01

The last transferred SSI position can be read out from this register. The SSI encoder value is displayed as a 32-bit position value. This position value is generated synchronously with the X2X cycle.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Last SSI position transferred

4.11.14.13.8.2 SSI comparator condition

The module has an assigned comparator function for the SSI function. These consist of:

- Event ID that triggers the comparator function
- The window comparator
- Latch register for saving the counter value

When the comparator function is complete, event ID 7232 or 7233 (see 4.11.14.13.6.1 "List of event IDs") is sent.

Configure event ID for SSI comparator

Name:
CfO_SSI1event0IDwr

This register holds the event ID that should start the SSI comparator function. For a list of all possible event IDs, see 4.11.14.13.6.1 "List of event IDs"

Data type	Value	Information
INT	192 to 7,233	ID of comparator function

Configure the mode of the SSI comparator function

Name:
CfO_SSI1event0mode

This register can be used to configure the mode of the comparator function.

Comparator functions can be operated in 4 different modes. For a description, see "Comparator modes".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Single
		2	State change
		3	Continuous
2 - 7	Reserved	-	

Configure calculation of SSI comparator

Name:
CfO_SSI1event0config

The calculation of the position value used for the comparator can be configured in this register.

The window comparator condition is calculated as follows:

```
counter_window_value = ssi_counter & (2^ssi_data_bits - 1)
diff = counter_window_value – origin_comparator
if ((diff & (2^(comparator_mask)-1)) <= margin_comparator)
condition = True;
else
condition = False;
```

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 5	SSI data bits	x	Number of data bits used for masking
6 - 7	Reserved	-	
8 - 13	Comparator mask	x	The mask value is calculated from 2^n-1, where n is the value configured in SSI data bits. Default: 0
14	Comparator mode	0	MarginComparator >= SSI position - OriginComparator
		1	MarginComparator > SSI position - OriginComparator

Origin of the SSI comparator

Name:
OriginComparator01_SSI

This register contains the origin of the window comparator.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Origin of the window comparator.

Width of the SSI comparator

Name:
MarginComparator01_SSI

This register provides the width of the window comparator.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Width of the SSI window comparator

Read SSI latch position

Name:
Latch01SSI01

If the SSI window comparator returns "True", then the current SSI position is latched and saved in this register.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Latched SSI position

4.11.14.13.9 PWM - Pulse width modulation

The module has 2 PWM functions available, supported directly by the hardware. A 24 V output channel is set for each PWM encoder and cannot be changed. (See also 4.11.14.8.1 "Description of channel assignments")

When using the PWM function, the corresponding channel can be configured in the 4.11.14.13.5.1 "CfO_CFGchannel" register as "Channel-specific".

PWM function	Channel
PWM1	2
PWM2	4

4.11.14.13.9.1 Configure PWM prescaler

Name:
CfO_PWM0prescaler to CfO_PWM1prescaler

The length of the PWM cycle is configured using this register. The base is a 48 MHz clock, which can be changed (divided) using the setting in this register. One PWM cycle consists of 1,000 of the resulting clocks after they have been divided. The period length of the PWM cycle is calculated as follows:

$$PWM\_cycle = 1000 \frac{prescale}{48000000} [s]$$

Data type	Value	Information
UINT	2 to 65,535	Prescaler for PWM cycle

4.11.14.13.9.2 Output PWM values

Name:
PWMOutput02 and PWMOutput04

In this register, a configuration is made for the percentage of the PWM cycle (in 1/10 % steps) that the PWM output is logical 1, i.e. ON.

Data type	Value	Information
UINT	0 to 1,000	PWM output always off
	2 to 999	Turn on time in 1/10% steps
	1,000	PWM output always on

4.11.14.13.10 Time measurement function

The module has a time measurement function for each I/O channel. It can be configured separately for rising and falling edges on each channel.
A starting edge can be configured for each time measurement function. When a configured starting edge occurs, the value of the internal timer is saved in a FIFO. This FIFO holds up to 16 elements. When the actual trigger edge occurs, the difference in time between the starting edge and the triggered edge is copied to the respective register.
Bits 8 to 11 "Previous start edge" of the 4.11.14.13.10.2 "CfO_EdgeTimeFallingMode" and 4.11.14.13.10.3 "CfO_EdgeTimeRisingMode" registers can be used to define which detected starting edge from the FIFO should be used to calculate the difference. Additionally, when the trigger edge occurs, the counter clocked internally using bits 12 to 15 "Time measurement resolution are copied to the 4.11.14.13.10.10 "TimeStampFallingCH" and 4.11.14.13.10.11 "TimeStampRisingCH" registers.

Information:

The time measurement function is an extension of edge detection, so all of the channels used must be configured there.

4.11.14.13.10.1 Enable time measurement function

Name:
CfO_EdgeTimeglobalenable

This register enables/disables the time measurement function for the entire module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Time measurement function	0	Disabled for entire module
		1	Enabled for entire module
1 - 7	Reserved	-	

4.11.14.13.10.2 Configure time measurement function for the falling edge

Name:
CfO_EdgeTimeFallingMode01 to CfO_EdgeTimeFallingMode04

These registers can be used to configure the time measurement function for the falling edge of the respective channel.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Selects the channel for the starting edge	0	Channel 1
		...	
		3	Channel 4
4	Selects the edge for the starting edge	0	The falling edge of the channel configured in bits 0 to 3 serves as the starting edge.
		1	The rising edge of the channel configured in bits 0 to 3 serves as the starting edge.
5 - 6	Reserved	-	
7	Trigger	0	Triggered[1)]
		1	Continuous[2)]
8 - 11	Previous start edge	0 to 15	The value determines which entry in the starting edge FIFO should be used to calculate the time difference.
12 - 15	Time measurement resolution	0	8 Mhz
		1	4 Mhz
		2	2 Mhz
		3	1 Mhz
		4	500 kHz
		5	250 kHz
		6	125 kHz
		7	625 kHz

1) The time measurement is triggered by the corresponding bit in the 4.11.14.13.10.5 "TriggerRisingCH" register.
2) Time measurement runs continuously and is triggered at every edge.

4.11.14.13.10.3 Configure time measurement function for the rising edge

Name:
CfO_EdgeTimeRisingMode01 to CfO_EdgeTimeRisingMode04

These registers can be used to configure the time measurement function for the rising edge of the respective channel.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Selects the channel for the starting edge	0	Channel 1
		...	
		3	Channel 4
4	Selects the edge for the starting edge	0	The falling edge of the channel configured in bits 0 to 3 serves as the starting edge.
		1	The rising edge of the channel configured in bits 0 to 3 serves as the starting edge.
5 - 6	Reserved	-	
7	Trigger	0	Triggered[1)]
		1	Continuous[2)]
8 - 11	Previous start edge	0 to 15	The value determines which entry in the starting edge FIFO should be used to calculate the time difference.
12 - 15	Time measurement resolution	0	8 Mhz
		1	4 Mhz
		2	2 Mhz
		3	1 Mhz
		4	500 kHz
		5	250 kHz
		6	125 kHz
		7	625 kHz

1) The time measurement is triggered by the corresponding bit in the 4.11.14.13.10.4 "TriggerRisingCH" register.
2) Time measurement runs continuously and is triggered at every edge.

4.11.14.13.10.4 Trigger falling edge detection

Name:
TriggerFallingCH01 to TriggerFallingCH04

If bit 7 "Trigger" is cleared in the 4.11.14.13.10.2 "CfO_EdgeTimeFallingMode" register, then detection of a falling edge on the respective input can be triggered using the respective bit in this register. After a bit has been set, the next falling edge on the corresponding channel is detected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TriggerFallingCH01	0	Falling edges on channel 1 are not detected
		1	The next falling edge on channel 1 will be detected
...		...	
3	TriggerFallingCH04	0	Falling edges on channel 4 are not detected
		1	The next falling edge on channel 4 will be detected
4 - 7	Reserved	-	

4.11.14.13.10.5 Trigger rising edge detection

Name:
TriggerRisingCH01 to TriggerRisingCH04

If bit 7 "Trigger" is cleared in the 4.11.14.13.10.3 "CfO_EdgeTimeRisingMode" register, then detection of a rising edge on the respective input can be triggered using the respective bit in this register. After a bit has been set, the next rising edge on the corresponding channel is detected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TriggerRisingCH01	0	Rising edges on channel 1 are not detected
		1	The next rising edge on channel 1 will be detected
...		...	
3	TriggerRisingCH04	0	Rising edges on channel 4 are not detected
		1	The next rising edge on channel 4 will be detected
4 - 7	Reserved	-	

4.11.14.13.10.6 Show first falling trigger edge

Name:
BusyTriggerFallingCH01 to BusyTriggerFallingCH04

If edges are triggered via the bits in the 4.11.14.13.10.4 "TriggerFallingCH" register, then a set bit in this register indicates that no falling edges have been detected on the respective channel since the corresponding bit was set in the "TriggerFallingCH" register. If a falling edge occurs on the respective channel, then the corresponding BusyTriggerFalling bit is cleared.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	BusyTriggerFallingCH01	0	Falling edge detected on channel 1
		1	Module waiting for a falling edge on channel 1
...		...	
3	BusyTriggerFallingCH04	0	Falling edge detected on channel 4
		1	Module waiting for a falling edge on channel 4
4 - 7	Reserved	-	

4.11.14.13.10.7 Show first rising trigger edge

Name:
BusyTriggerRisingCH01 to BusyTriggerRisingCH04

If edges are triggered via the bits in the 4.11.14.13.10.5 "TriggerRisingCH" register, then a set bit in this register indicates that no rising edges have been detected on the respective channel since the corresponding bit was set in the "TriggerRisingCH" register. If a rising edge occurs on the respective channel, then the corresponding BusyTriggerRising bit is cleared.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	BusyTriggerRisingCH01	0	Rising edge detected on channel 1
		1	Module waiting for a rising edge on channel 1
...		...	
3	BusyTriggerRisingCH04	0	Rising edge detected on channel 4
		1	Module waiting for a rising edge on channel 4
4 - 7	Reserved	-	

4.11.14.13.10.8 Count falling trigger edges

Name:
CountFallingCH01 to CountFallingCH04

These registers contain cyclic counters that are incremented with every detected falling edge on the respective channel.

Data type	Value	Information
USINT	0 to 255	Counter for falling edges

4.11.14.13.10.9 Count rising trigger edges

Name:
CountRisingCH01 to CountRisingCH04

These registers contain cyclic counters that are incremented with every detected rising edge on the respective channel.

Data type	Value	Information
USINT	0 to 255	Counter for rising edges

4.11.14.13.10.10 Time stamp of falling edge

Name:
TimeStampFallingCH01 to TimeStampFallingCH04

When a falling edge occurs on the respective channel, the current counter value of the module timer is copied to these registers.

Data type	Value	Information
UINT	0 to 65,535	Time stamp for rising edges

4.11.14.13.10.11 Time stamp of the rising edge

Name:
TimeStampRisingCH01 to TimeStampRisingCH04

When a rising edge occurs on the respective channel, the current counter value of the module timer is copied to these registers.

Data type	Value	Information
UINT	0 to 65,535	Time stamp for rising edges

4.11.14.13.10.12 Time difference of falling edge

Name:
TimeDiffFallingCH01 to TimeDiffFallingCH04

When a falling edge occurs on the respective channel, the time difference compared to the starting edge configured in bit 4 of the 4.11.14.13.10.2 "CfO_EdgeTimeFallingMode" register is copied to this register.

Data type	Value	Information
UINT	0 to 65,535	Time difference from starting edge

4.11.14.13.10.13 Time difference of rising edge

Name:
TimeDiffRisingCH01 to TimeDiffRisingCH04

When a rising edge occurs on the respective channel, the time difference compared to the starting edge configured in bit 4 of the 4.11.14.13.10.3 "CfO_EdgeTimeRisingMode" register is copied to this register.

Data type	Value	Information
UINT	0 to 65,535	Time difference from starting edge

4.11.14.13.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

4.11.14.13.12 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

4.11.14.13.13 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
128 µs

4.11.15 X20DC2396

4.11.15.1 General information

The module is equipped with two inputs for an ABR incremental encoder with 24 V encoder signal.

- 2 ABR incremental encoder 24 V
- 2 additional inputs e.g. for home enable switch
- 24 VDC and GND for encoder supply

4.11.15.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC2396	X20 digital counter module, 2 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 196: X20DC2396 - Order data

4.11.15.3 Technical data

Product ID	X20DC2396
Short description	
I/O module	2 ABR incremental encoder 24 V
General information	
Input voltage	24 VDC -15 % / +20 %
B&R ID code	0x1BAB
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Encoder - Bus	Yes
Encoder - Encoder	No
Reference enable switch - Bus	Yes
Reference enable switch - Encoder	No
Reference switch - Reference switch	No
Type of signal lines	Shielded cables must be used for all signal lines.
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Home enable switch	
Quantity	2
Nominal voltage	24 VDC
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections
Input circuit	Sink

Table 197: X20DC2396 - Technical data

Product ID	X20DC2396
Input current at 24 VDC	Approx. 3.3 mA
Input resistance	7.19 kΩ
Isolation voltage between home enable switch and bus	500 V_{eff}
Switching threshold	
Low	<5 VDC
High	>15 VDC
ABR incremental encoder	
Encoder inputs	24 V, asymmetrical
Counter size	16/32-bit
Input frequency	Max. 100 kHz
Evaluation	4x
Encoder supply	Module-internal, max. 600 mA
Input filter	
Hardware	≤2 µs
Software	-
Input current at 24 VDC	Approx. 1.3 mA
Input resistance	18.4 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Overload behavior of the encoder supply	Short circuit protection, overload protection
Isolation voltage between encoder and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 197: X20DC2396 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.15.4 LED status indicators

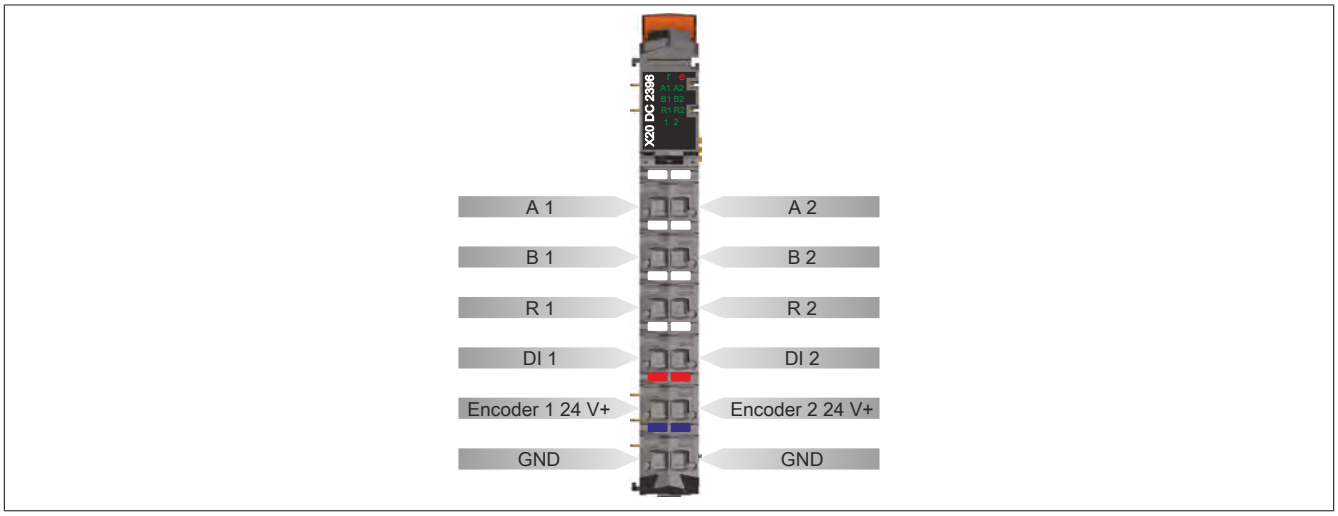
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	A1, A2	Green		Input state of counter input A1 or A2
	B1, B2	Green		Input state of counter input B1 or B2
	R1, R2	Green		Input state of reference pulse R1 or R2
	1 - 2	Green		Input state of the corresponding digital input

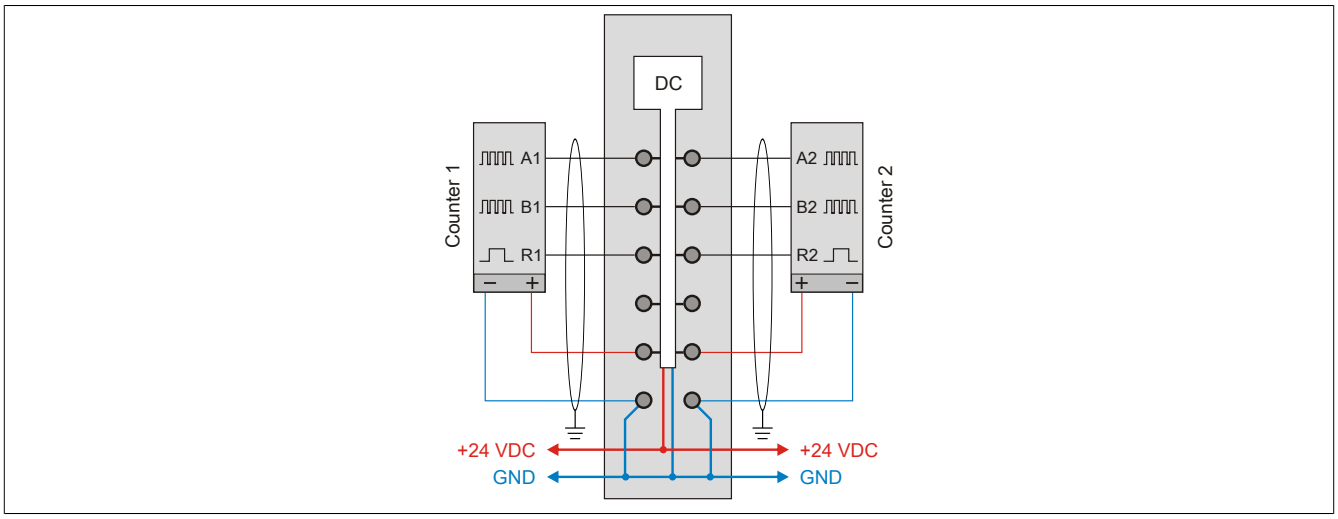
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.15.5 Pinout

Shielded cables must be used for all signal lines.

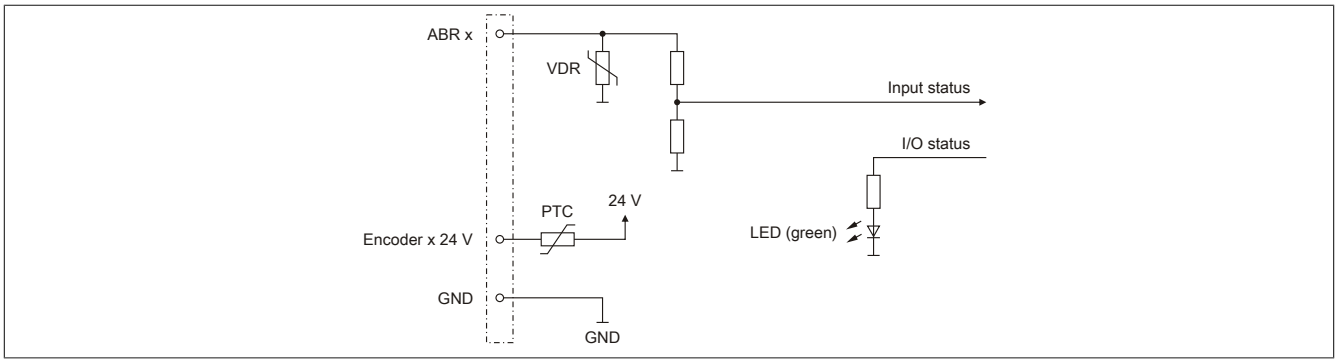


4.11.15.6 Connection example

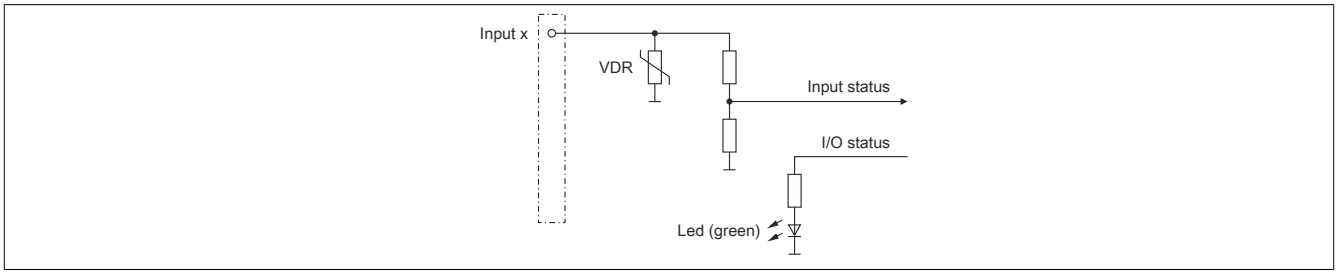


4.11.15.7 Input circuit diagram

Counter inputs



Standard inputs



4.11.15.8 Register description

4.11.15.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.15.8.2 Function model 0 - Standard and Function model 1 - Standard with 32-bit encoder counter value

The difference between function model 0 and function model 1 is the size of the data type for some registers.

- Function model 0 uses data type INT
- Function model 1 uses data type DINT (specified in parentheses)

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
4104	CfO_EdgeDetectFalling	USINT				•
4106	CfO_EdgeDetectRising	USINT				•
2064	CfO_PresetABR01_1(_32Bit)	(D)INT				•
2068	CfO_PresetABR01_2(_32Bit)	(D)INT				•
2576	CfO_PresetABR02_1(_32Bit)	(D)INT				•
2580	CfO_PresetABR02_2(_32Bit)	(D)INT				•
512	ConfigOutput24	UINT				•
522	ConfigOutput26	USINT				•
520	ConfigOutput27	USINT				•
544	ConfigOutput32	UINT				•
554	ConfigOutput34	USINT				•
552	ConfigOutput35	USINT				•
Communication						
2116	ReferenceModeEncoder01	USINT			•	
2628	ReferenceModeEncoder02	USINT			•	
2080	Encoder01	(D)INT	•			
2592	Encoder02	(D)INT	•			
264	Input state of digital inputs 1 to 2	USINT	•			
	DigitalInput01	Bit 3				
	DigitalInput02	Bit 7				
2118	StatusInput01	USINT	•			
2630	StatusInput02	USINT	•			
40	Status of encoder supply	USINT	•			
	PowerSupply01	Bit 0				

4.11.15.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
4104	-	CfO_EdgeDetectFalling	USINT				●
4106	-	CfO_EdgeDetectRising	USINT				●
2064	-	CfO_PresetABR01_1	INT				●
2068	-	CfO_PresetABR01_2	INT				●
2576	-	CfO_PresetABR02_1	INT				●
2580	-	CfO_PresetABR02_2	INT				●
512	-	ConfigOutput24	UINT				●
522	-	ConfigOutput26	USINT				●
520	-	ConfigOutput27	USINT				●
544	-	Constant register "ConfigOutput32"	UINT				●
554	-	ConfigOutput34	USINT				●
552	-	ConfigOutput35	USINT				●
Communication							
2116	0	ReferenceModeEncoder01	USINT			●	
2628	1	ReferenceModeEncoder02	USINT			●	
2080	0	Encoder01	INT	●			
2592	4	Encoder02	INT	●			
264	2	Input state of digital inputs 1 to 2	USINT	●			
		DigitalInput01	Bit 3				
		DigitalInput02	Bit 7				
2118	6	StatusInput01	USINT	●			
2630	7	StatusInput02	USINT	●			
40	3	Status of encoder supply	USINT	●			
		PowerSupply01	Bit 0				

1) The offset specifies the position of the register within the CAN object.

4.11.15.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.11.15.8.4 ABR encoder - Configuration registers

4.11.15.8.4.1 Reference pulse

The following registers must be configured by a single acyclic write with the listed values so that the homing procedure is completed on the edge of the reference pulse.

The homing procedure can take place on:

- Rising edge
- Falling edge (default configuration)

Constant register "CfO_EdgeDetectFalling"

Name:

CfO_EdgeDetectFalling

Data type	Value	Filter
USINT	0x00	Configuration value for rising edge
	0x04	Encoder 1 - Configuration value for falling edge
	0x40	Encoder 2 - Configuration value for falling edge
	0x44	Encoders 1 and 2 - Configuration value for falling edge

Constant register "CfO_EdgeDetectRising"

Name:

CfO_EdgeDetectRising

Data type	Value	Filter
USINT	0x00	Configuration value for falling edge (default 0x00)
	0x04	Encoder 1 - Configuration value for rising edge
	0x40	Encoder 2 - Configuration value for rising edge
	0x44	Encoders 1 and 2 - Configuration value for rising edge

Constant register "ConfigOutput24"

Name:

ConfigOutput24

This register contains the value for ABR encoder 1.

Data type	Value	Filter
UINT	0x1012	Configuration value for rising edge
	0x1002	Configuration value for falling edge

Constant register "ConfigOutput32"

Name:
ConfigOutput32

This register contains the value for ABR encoder 2.

Data type	Value	Filter
UINT	0x1016	Configuration value for rising edge
	0x1006	Configuration value for falling edge

4.11.15.8.4.2 Setting the home position

Name:
CfO_PresetABR01_1 to CfO_PresetABR01_2
CfO_PresetABR02_1 to CfO_PresetABR02_2

CfO_PresetABR01_1_32Bit to CfO_PresetABR01_2_32Bit
CfO_PresetABR02_1_32Bit to CfO_PresetABR02_2_32Bit (only in function model 1)

It is possible to specify two home positions for each encoder with these registers through a one-off acyclic write, for example (default = 0). The configured values are applied to the counter values after a completed homing procedure.

Data type	Value
INT	-32,768 to 32,767
DINT[1)]	-2,147,483,648 to 2,147,483,647

1) Only in function model 1

4.11.15.8.4.3 Homing with reference enable input

Regardless of the referencing mode, it is possible using this register to prevent the home position from being applied when the corresponding reference input voltage level occurs (see 4.11.15.8.5.2 "Input state of digital inputs 1 to 2": bit 7). The desired setting can be configured by a one-off acyclic write.

Voltage level for reference enable activation - ABR encoder 1

Name:

ConfigOutput26

The voltage level of the digital input 1 to activate reference enable is configured with this register.

Data type	Value	Filter
USINT	0x00	Reference enable is active at 0 VDC
	0x08	Reference enable is active at 24 VDC

Reference enable of the input - ABR encoder 1

Name:
ConfigOutput27

This register can be used to define whether the reference enable is activated.

Data type	Value	Filter
USINT	0x00	Reference enable input OFF (default)
	0x08	Reference enable input activated

Voltage level for reference enable activation - ABR encoder 2

Name:

ConfigOutput34

The voltage level of the digital input 2 to activate reference enable is configured with this register.

Data type	Value	Filter
USINT	0x00	Reference enable is active at 0 VDC
	0x80	Reference enable is active at 24 VDC

Reference enable of the input - ABR encoder 2

Name:
ConfigOutput35

This register can be used to define whether the reference enable is activated.

Data type	Value	Filter
USINT	0x00	Reference enable input OFF (default)
	0x80	Reference enable input activated

4.11.15.8.5 ABR encoder - Configuration registers

4.11.15.8.5.1 Counter state of the encoders

Name:
Encoder01 to Encoder02

The encoder values are displayed in this register.

Data type	Value
INT	-32,768 to 32,767
DINT[1)]	-2,147,483,648 to 2,147,483,647

1) Only in function model 1

4.11.15.8.5.2 Input state of digital inputs 1 to 2

Name:
DigitalInput01 to DigitalInput02.

This register displays the input status of the encoders and the digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder 1	0 or 1	Input state - Signal A
1		0 or 1	Input state - Signal B
2		0 or 1	Input state of reference pulse
3	DigitalInput01	0 or 1	Input state - Digital input 1
4	Encoder 2	0 or 1	Input state - Signal A
5		0 or 1	Input state - Signal B
6		0 or 1	Input state of reference pulse
7	DigitalInput02	0 or 1	Input state - Digital input 2

4.11.15.8.5.3 Reading the referencing mode

Name:
ReferenceModeEncoder01 to ReferenceModeEncoder02

This register determines the referencing mode.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1		00	Referencing OFF
		01	Single shot referencing
		11	Continuous referencing
2 - 5		0	Bits permanently set = 0
6 - 7		00	Referencing OFF
		11	Bits permanently set = 1

This results in the following values:

Binary	Hex	Function
00000000	0x00	Referencing OFF
11000001	0xC1	Single shot referencing For a new start after the completed homing procedure: • Write value 0x00 • Wait until bit 0 to bit 3 of the StatusInput01 register takes on the value 0. Counter bits 4 to 7 are not erased • Switch homing procedure on again
11000011	0xC3	Continuous referencing Referencing occurs at every reference pulse.

4.11.15.8.5.4 Status of the homing procedure

Name:
StatusInput01 (for encoder 1) to StatusInput02 (for encoder 2)

This register contains information regarding whether the referencing process is off, active or complete.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Reference pulse without homing[1)]	0	No reference impulse without homing has occurred yet
		1	At least a reference impulse without homing has occurred
1	State change	0 or 1	Changes with each reference pulse without homing
2	Reference pulse with homing[1)]	0	No homing has occurred yet
		1	At least one homing procedure has occurred
3	State change	0 or 1	Changes with each homing procedure that has taken place
4	Reference pulse	0	The last reference pulse didn't bring about a homing procedure
		1	The last reference pulse brought about a homing procedure
5 - 7	Counter	x	Free-running counter, increased with each reference pulse

1) Always 1 after the first reference pulse that has occurred

Examples of possible values:

Binary	Hex	Function
0x00000000	0x00	Referencing OFF or homing procedure already active
0x00111100	0x3CE	First homing procedure complete Reference value applied in the Encoder01 register
0xxxx11100	0xxB	Bits 5 to 7 are changed with each reference pulse
0xxxx1x100	0xxx	Continuously changing the bits with the "Continuous referencing" setting. The reference value is applied to the Encoder01 register on each reference pulse.

4.11.15.8.5.5 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.11.15.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

4.11.15.8.7 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

4.11.15.8.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
128 µs

4.11.16 X20DC2398

4.11.16.1 General information

This module is equipped with two inputs for SSI absolute encoders with 24 V encoder signal.

- 2 SSI absolute encoder 24 V
- 2 additional inputs
- 24 VDC and GND for encoder supply

4.11.16.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC2398	X20 digital counter module, 2 SSI absolute encoder, 24 V, 125 kbit/s, 32-bit	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 198: X20DC2398 - Order data

4.11.16.3 Technical data

Product ID	X20DC2398
Short description	
I/O module	2 SSI absolute encoder 24 V
General information	
Input voltage	24 VDC -15 % / +20 %
B&R ID code	0x1BAD
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.4 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Encoder - Bus	Yes
Encoder - Encoder	No
Channel - Bus	Yes
Channel - Encoder	No
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines.
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	2
Nominal voltage	24 VDC
Input current at 24 VDC	Approx. 3.3 mA
Input filter	
Hardware	≤2 µs
Software	-
Connection type	3-wire connections

Table 199: X20DC2398 - Technical data

Product ID	X20DC2398
Input circuit	Sink
Input resistance	7.19 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
SSI absolute encoder	
Encoder inputs	24 V, asymmetrical
Counter size	32-bit
Max. transfer rate	125 kbit/s
Encoder supply	Module-internal, max. 600 mA
Keying	Gray/Binary
CLK: Output current	Max. 100 mA
DATA: Input resistance	18.4 kΩ
Isolation voltage between encoder and bus	500 V_{eff}
Overload behavior of the encoder supply	Short circuit protection, overload protection
Switching threshold	
Low	<5 VDC
High	>15 VDC
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 199: X20DC2398 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.11.16.4 LED status indicators

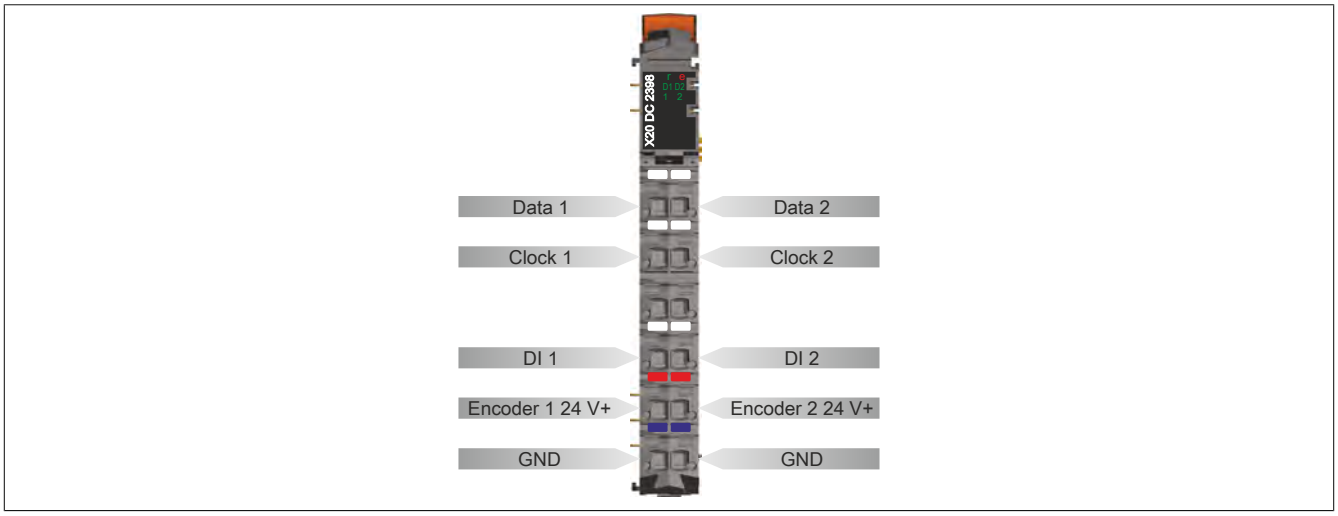
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	D1, D2	Green		Input state of data signal 1 or 2
	1 - 2	Green		Input state of the corresponding digital input

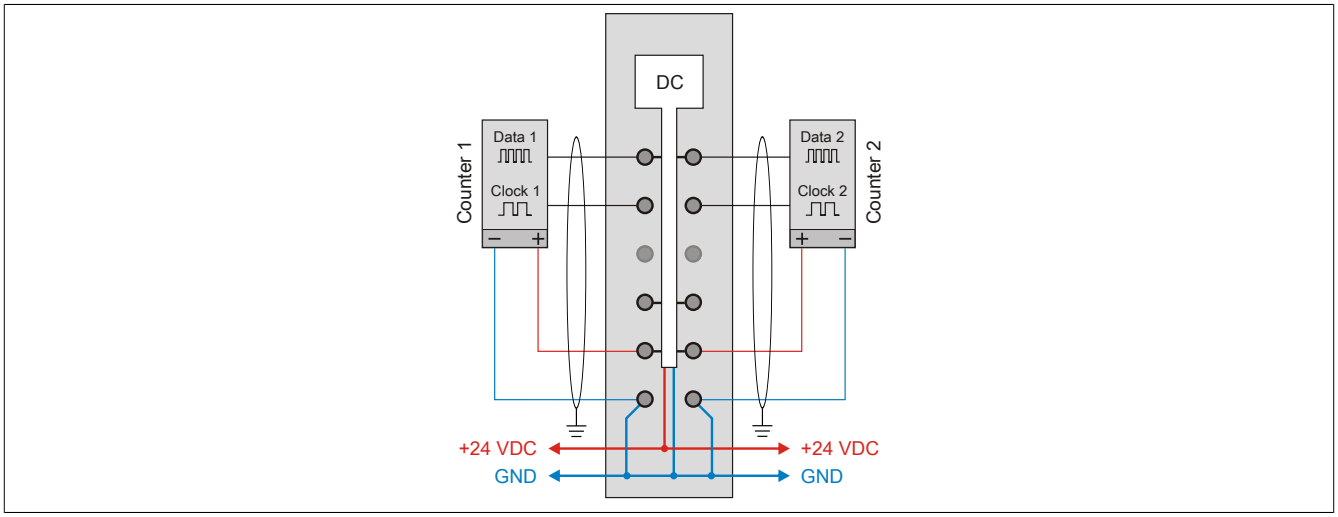
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.16.5 Pinout

Shielded cables must be used for all signal lines.

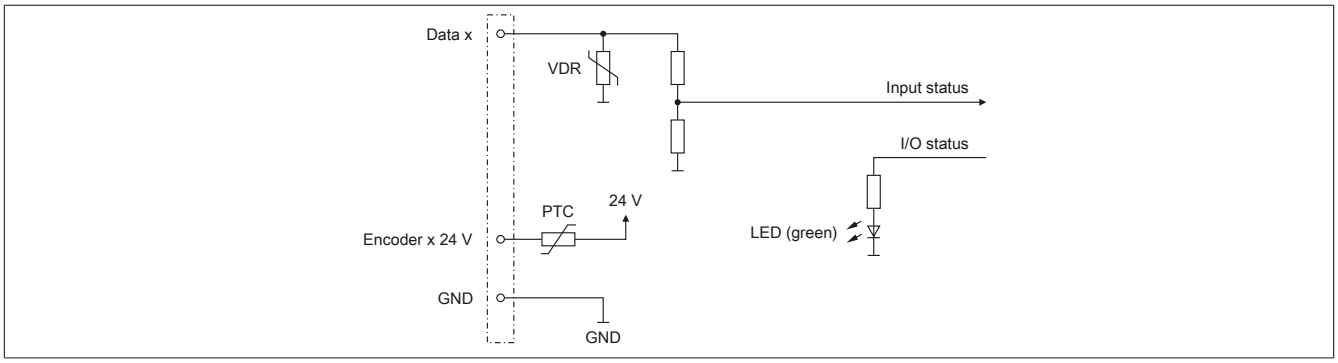


4.11.16.6 Connection example

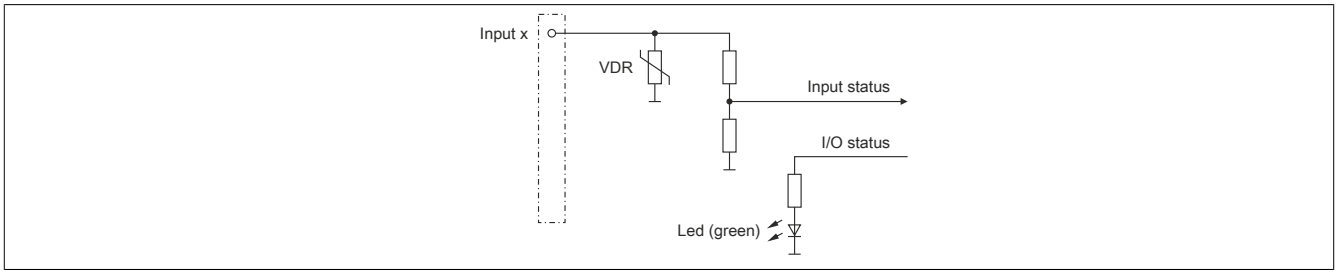


4.11.16.7 Input circuit diagram

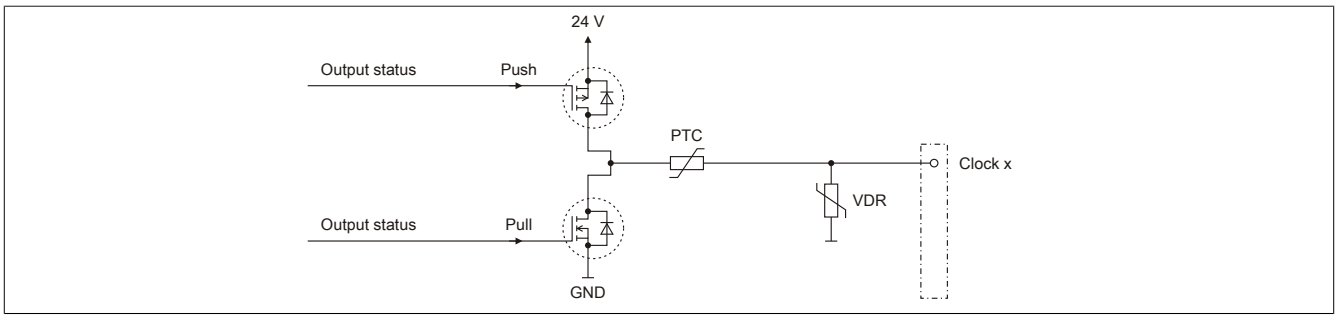
Counter inputs



Standard inputs



4.11.16.8 Output circuit diagram



4.11.16.9 Register description

4.11.16.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.16.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
7176	ConfigOutput15	UINT				•
7432	ConfigOutput16	UINT				•
7172	ConfigAdvanced01	UDINT				•
7428	ConfigAdvanced02	UDINT				•
Communication						
7184	Encoder01	UDINT	•			
7440	Encoder02	UDINT	•			
264	Input state of digital inputs 1 to 2	USINT	•			
	DigitalInput01	Bit 3				
	DigitalInput02	Bit 7				
40	Status of encoder supply	USINT	•			
	PowerSupply01	Bit 0				

4.11.16.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
7176	-	ConfigOutput15	UINT				•
7432	-	ConfigOutput16	UINT				•
7172	-	ConfigAdvanced01	UDINT				•
7428	-	ConfigAdvanced02	UDINT				•
Communication							
7184	0	Encoder01	UDINT	•			
7440	8	Encoder02	UDINT	•			
264	4	Input state of digital inputs 1 to 2	USINT	•			
		DigitalInput01	Bit 3				
		DigitalInput02	Bit 7				
40	5	Status of encoder supply	USINT	•			
		PowerSupply01	Bit 0				

1) The offset specifies the position of the register within the CAN object.

4.11.16.9.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.11.16.9.4 SSI encoder configuration register

4.11.16.9.4.1 Standard configuration

Name:
ConfigOutput15 to ConfigOutput 16

This configuration register is used to set the coding, the clock rate and the number of bits. Default = 0. This must be set once using an acyclic write command.

"ConfigOutput15": Configuration register for SSI encoder01 and
"ConfigOutput16": Configuration register for SSI encoder02

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits		
6 - 7	Clock rate	11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding

4.11.16.9.4.2 Extended configuration

Name:
ConfigAdvanced01 to ConfigAdvanced02

This configuration register is used to set the coding, the clock rate, the number of bits and the monostable multivibrator settings. Default = 0. This must be set once using an acyclic write command.

It only differs from register ConfigOutput15 + 16 by data length and additional monostable multivibrator testing.

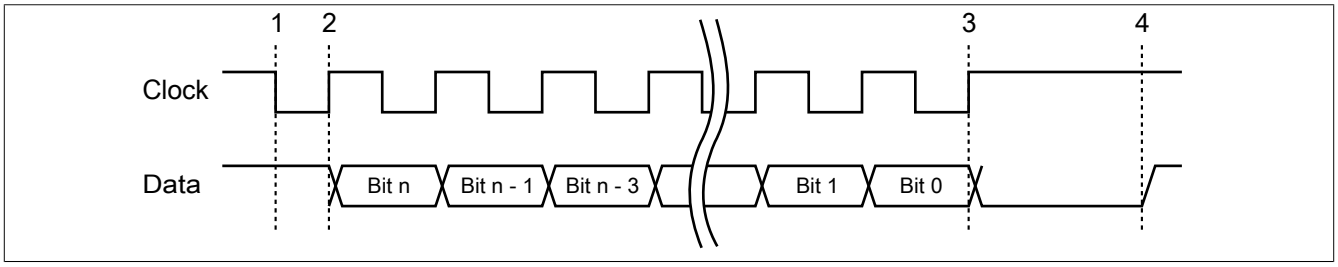
"ConfigAdvanced01": Configuration register for SSI encoder01 and
"ConfigAdvanced02": Configuration register for SSI encoder02

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding
16 - 17	Monostable multivibrator	00	Check OFF, no additional clock bit
		01	Check set to High level
		10	Check set to Low level
		11	Level is clocked but ignored
18 - 31	Reserved	0	

Transfer to synchronous serial interface



Measurement value processing

1 Starting bit ... Stores the measurement value
2 Output of first data bit
3 All data bits are transferred, monostable multivibrator time starts counting down.
4 Monostable multivibrator returns to its initial state. A new transfer can be started.

4.11.16.9.5 SSI encoder - Configuration registers

4.11.16.9.5.1 SSI position values

Name:
Encoder01 to Encoder02

The two SSI encoder values are displayed as 32-bit position values. The SSI position values are generated synchronously with the X2X cycle.

Data type	Value	Filter
UDINT	0 to 4,294,967,729	SSI position

4.11.16.9.5.2 Input state of digital inputs 1 to 2

Name:
DigitalInput01 to DigitalInput02

This register is used to indicate the input state of digital inputs 1 to 2.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
3	DigitalInput01	0 or 1	Input state - Digital input 1
7	DigitalInput02	0 or 1	Input state - Digital input 2

4.11.16.9.5.3 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.11.16.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

4.11.16.9.7 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

4.11.16.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
128 µs

4.11.17 X20DC4395

4.11.17.1 General information

This module is a multifunctional counter module. It can be connected to two SSI encoders, two ABR encoders, four AB encoders or eight event counters. Four outputs are available for pulse width modulation. The functions can also be mixed.

- 24 VDC encoder inputs
- SSI, ABR, AB or event counters for inputs
- Pulse width modulation for outputs
- 24 VDC and GND for encoder supply

Information:

This module is a multifunctional module. Some bus controllers only support the default function model.

Default function model:

- **1x ABR incremental encoder (24 V)**
- **1x SSI absolute encoder (24 V)**
- **1x event counter (24 V)**
- **2x PWM output (24 V)**

4.11.17.2 Order data

Model number	Short description	Figure
	Counter functions	
X20DC4395	X20 digital counter module, 2 SSI absolute encoder, 24 V, 2 ABR incremental encoder, 24 V, 4 AB incremental encoders, 24 V, 8 event counters or 4 PWM, local time measurement function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 200: X20DC4395 - Order data

4.11.17.3 Technical data

Product ID	X20DC4395
Short description	
I/O module	2 SSI absolute encoder, 24 V, 2 ABR incremental encoder, 24 V, 4 AB incremental encoders, 24 V, 8x event counters or 4x pulse width modulation, time measurement, relative timestamp
General information	
Input voltage	24 VDC -15 % / +20 %
B&R ID code	0x1CC5
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using the status LED and software (output error status)
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Output - Output	No
Output - Bus	Yes
Output - Encoder	No
Encoder - Bus	Yes
Encoder - Encoder	No
Type of signal lines	Shielded cables must be used for all signal lines.
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Incremental encoder	
Quantity	4
Encoder inputs	24 V, asymmetrical
Counter size	16/32-bit
Input frequency	Max. 100 kHz
Evaluation	4x
Encoder supply	Module-internal, max. 600 mA
Overload behavior of the encoder supply	Short circuit protection, overload protection
SSI absolute encoder	
Quantity	2
Encoder inputs	24 V, asymmetrical
Counter size	32-bit
Max. transfer rate	125 kbit/s
Encoder supply	Module-internal, max. 600 mA
Keying	Gray/Binary
CLK: Output current	Max. 100 mA
Overload behavior of the encoder supply	Short circuit protection, overload protection
Event counter	
Quantity	8
Nominal voltage	24 VDC
Signal form	Square wave pulse
Evaluation	Each edge, cyclic counter
Input frequency	Max. 100 kHz
Input current at 24 VDC	Approx. 1.3 mA
Input resistance	18.4 kΩ
Isolation voltage between channel and bus	500 V_{eff}
Counter frequency	200 kHz
Counter size	16/32-bit
Input filter	
Hardware	≤2 µs
Software	-
Switching threshold	
Low	<5 VDC
High	>15 VDC
Edge detection / Time measurement	
Possible measurements	Gate time, period duration, edge offset for various channels
Measurements per module	Up to 9
Measurements per channel	Up to 2
Counter size	16-bit
Counter frequency	
Internal	8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, 62.5 kHz

Table 201: X20DC4395 - Technical data

Product ID	X20DC4395
Signal form	Square wave pulse
Measurement type	Continuous or triggered
Digital outputs	
Design	Push / Pull / Push-Pull
Quantity	4
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.1 A
Total nominal current	0.4 A
Output circuit	Sink or source
Output protection	Thermal cutoff if overcurrent or short circuit occurs, integrated protection for switching inductances
Pulse width modulation [2]	
Period duration	41.6 µs to 1.36 s
Factor for period duration	n/48000 s, n = 2 to 65535
Pulse duration	0 to 100 %
Resolution for pulse duration	0.1%
Actuator supply	Module-internal, max. 600 mA
Diagnostic status	Output monitoring
Leakage current when switched off	Max. 25 µA
Residual voltage	<0.9 V at 0.1 A rated current
Peak short circuit current	<10 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<2 µs
1 -> 0	<2 µs
Switching frequency	
Resistive load	Max. 24 kHz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Switching voltage + 0.6 VDC
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 201: X20DC4395 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Dead time when switching between push and pull: max. 1.5 µs.

4.11.17.4 LED status indicators

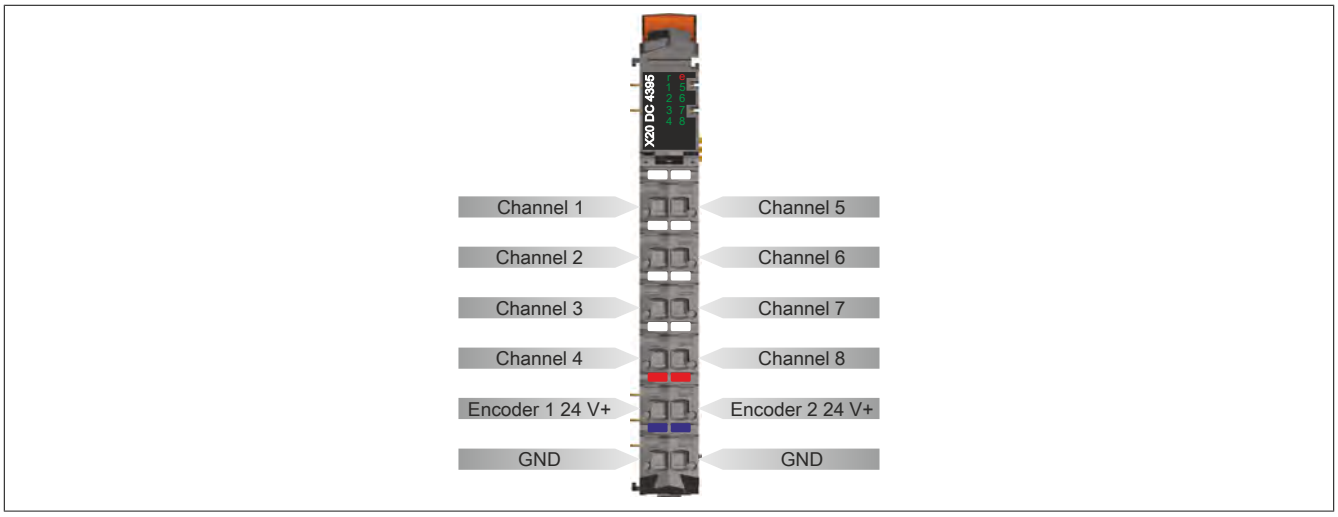
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 8	Green		Status of the corresponding digital signal

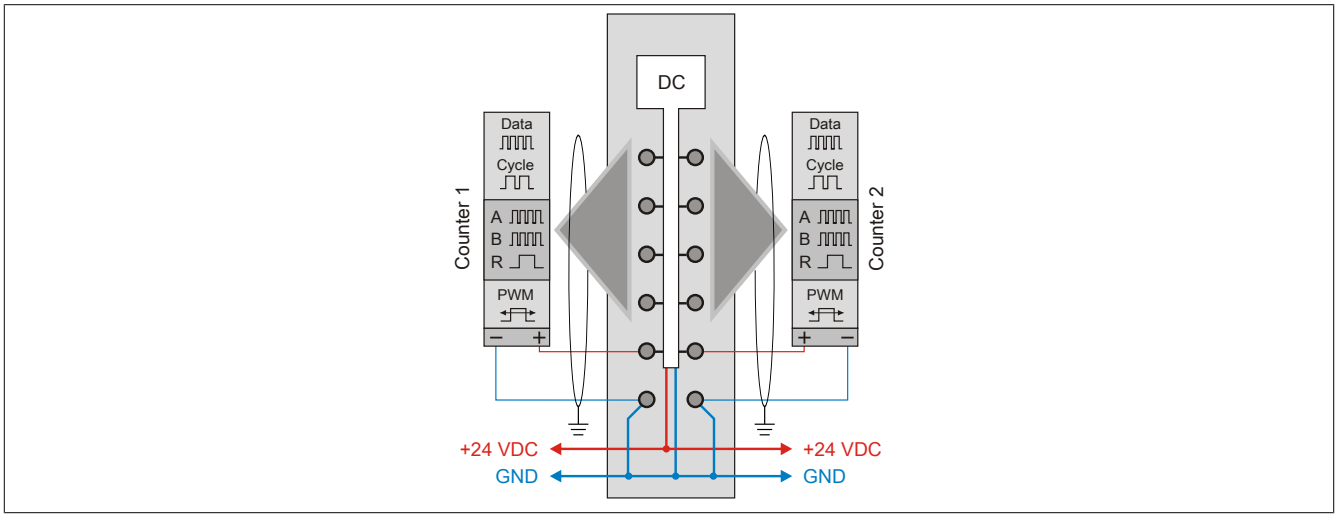
1) Depending on the configuration, a firmware update can take up to several minutes.

4.11.17.5 Pinout

Shielded cables must be used for all signal lines.



4.11.17.6 Connection example



4.11.17.7 Function overview

The following functions can be configured on the module. They cannot all be used at the same time due to the multiple use of the hardware channels and the limited cyclic data length.

- 8 digital channels, 4 of which can be configured as outputs
- 8 event counters with configurable counting direction and optional referencing via digital input
- 4 PWM outputs
- 4 up/down counters, each with optional latch inputs and comparator output
- 4 AB counters, each with optional latch inputs and comparator output
- 2 ABR encoder with configurable reference pulse edge and reference position, optional reference enable input, latch input and comparator output
- 2 SSI counter with optional latch input and comparator output
- 2 edge-triggered time measurement functions with configurable start edge based on current configuration settings

4.11.17.7.1 Description of channel assignments

The functions listed here are directly assigned to the respective hardware channels and cannot be changed:

Channel	Signal connections
1	• Digital input 1 • Event counter 1 • AB encoder 1 - signal line A • Up/down counter 1 - frequency • SSI encoder 1 - data line • ABR encoder 1 - signal line A
2	• Digital input 2 • Digital output 2 • Event counter 2 • PWM output 2 • AB encoder 1 - signal line B • Up/down counter 1 - direction • SSI encoder 1 - clock line • ABR encoder 1 - signal line B
3	• Digital input 3 • Event counter 3 • AB encoder 2 - signal line A • Up/down counter 2 - frequency • ABR encoder 1 - signal line R
4	• Digital input 4 • Digital output 4 • Event counter 4 • PWM output 4 • AB encoder 2 - signal line B • Up/down counter 2 - direction • ABR encoder 1 - reference enable input
5	• Digital input 5 • Event counter 5 • AB encoder 3 - signal line A • Up/down counter 3 - frequency • SSI encoder 2 - data line • ABR encoder 2 - signal line A
6	• Digital input 6 • Digital output 6 • Event counter 6 • PWM output 6 • AB encoder 3 - signal line B • Up/down counter 3 - direction • SSI encoder 2 - clock line • ABR encoder 2 - signal line B
7	• Digital input 7 • Event counter 7 • AB encoder 4 - signal line A • Up/down counter 4 - frequency • ABR encoder 2 - signal line R
8	• Digital input 8 • Digital output 8 • Event counter 8 • PWM output 8 • AB encoder 4 - signal line B • Up/down counter 4 - direction • ABR encoder 2 - reference enable input

Options available in addition to these basic functions, such as comparator outputs or latch inputs, can be configured freely to unused input/output channels.

4.11.17.7.2 Connection options

Channels 1 to 8 can be connected as follows:

Channel	Function					
1	I	Event counter	A	A	SSI data	
2	I/O	Event counter	B	B	SSI cycle	PWM
3	I	Event counter	A	R		
4	I/O	Event counter	B	Enable reference		PWM
5	I	Event counter	A	A	SSI data	
6	I/O	Event counter	B	B	SSI cycle	PWM
7	I	Event counter	A	R		
8	I/O	Event counter	B	Enable reference		PWM

The functions can also be mixed. For example:

Example 1	
Channel	Function
1	SSI data
2	SSI cycle
3	Event counter
4	PWM
5	A
6	B
7	Event counter
8	PWM

Example 2	
Channel	Function
1	SSI data
2	SSI cycle
3	A
4	B
5	Event counter
6	Event counter
7	Event counter
8	Event counter

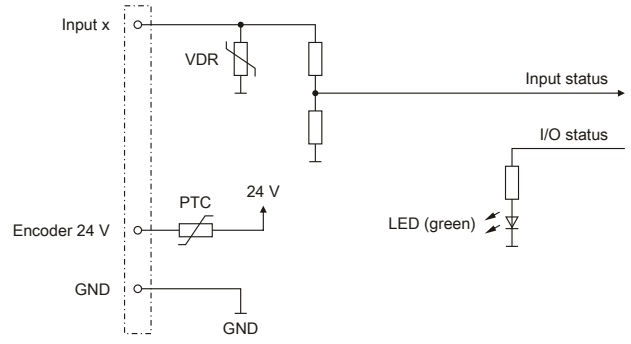
Example 3	
Channel	Function
1	Event counter
2	PWM
3	Event counter
4	PWM
5	SSI data
6	SSI cycle
7	A
8	B

Example 4	
Channel	Function
1	A
2	B
3	R
4	Enable reference
5	A
6	B
7	R
8	Enable reference

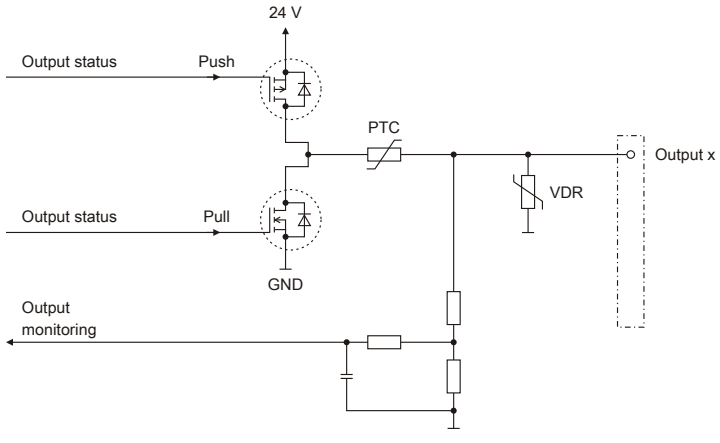
Example 5	
Channel	Function
1	A
2	B
3	Event counter
4	PWM
5	A
6	B
7	Event counter
8	Event counter

Example 6	
Channel	Function
1	Event counter
2	Event counter
3	Event counter
4	PWM
5	SSI data
6	SSI cycle
7	A
8	B

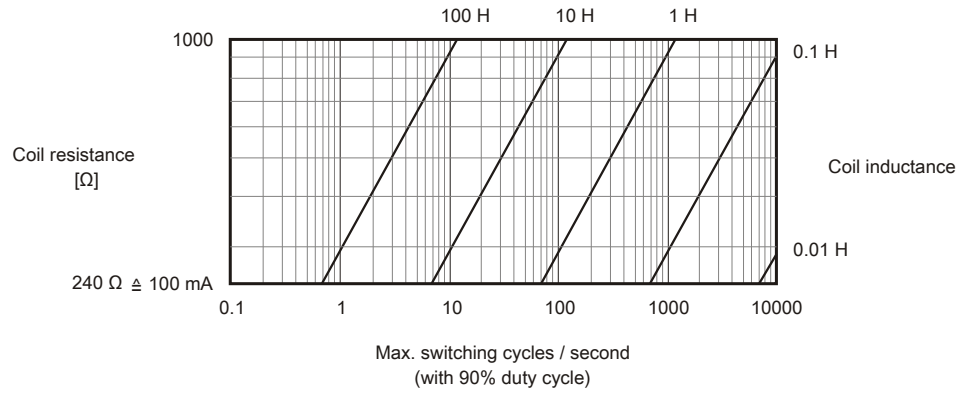
4.11.17.8 Input circuit diagram



4.11.17.9 Output circuit diagram



4.11.17.10 Switching inductive loads



4.11.17.11 Calculating the period duration

The outputs of the module can be operated as PWM outputs. The period duration is calculated using the following formula:

$$\text{Period duration} = \frac{n}{48000}\ \text{s}$$

A value of 2 to 65535 can be defined for n.

Example

n	Period duration	Frequency
2	416 µs	24 kHz
24000	500 ms	2 Hz
48000	1 s	1 Hz
65535	1.36 s	0.73 Hz

4.11.17.12 Register description

4.11.17.12.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.11.17.12.2 Function model 0 - Standard and Function model 1 - 32-bit counter

The following 2 models can be selected:

- 16-bit counter, Function model 0
- 32-bit counter, Function model 1 (identified in the table with a "(D)" in the data type and "(_32Bit)" in the name.)

The only difference between these two models is that they use either 16-bit or 32-bit registers for incremental counter functions. These include:

- ABR encoders
- AB encoders
- Up/down counters
- Event counters

All other module functions e.g. SSI, PWM and time measurement, as well as their data types, are identical for the two models.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module configuration - General						
(N-1) * 2	CfO_CFGchannel0N (Index N = 1 to 8)	USINT				●
64 + N * 2	CfO_LEDNsource (Index N = 0 to 7)	USINT				●
Configuration - Input for ABR encoders						
512	CfO_DIREKTIOevent0IDwr	UINT				●
544	CfO_DIREKTIOevent1IDwr	UINT				●
516	CfO_DIREKTIOevent0mode	USINT				●
548	CfO_DIREKTIOevent1mode	USINT				●
522	CfO_DIREKTIOevent0compState	UINT				●
544	CfO_DIREKTIOevent1compState	UINT				●
520	CfO_Ev0CompMask	USINT				●
552	CfO_Ev1CompMask	USINT				●
2064 + (N-1) * 256	CfO_CounterNPresetValue1(_32Bit) (Index N = 1 to 4)	U(D)INT				●
2068 + (N-1) * 256	CfO_CounterNPresetValue2(_32Bit) (Index N = 1 to 4)	U(D)INT				●
2048 + (N-1) * 256	CfO_CounterNconfig (Index N = 1 to 4)	USINT				●
2056 + (N-1) * 256	CfO_CounterNconfigReg0 (Index N = 1 to 4)	USINT				●
2058 + (N-1) * 256	CfO_CounterNconfigReg1 (Index N = 1 to 4)	USINT				●
2112 + (N-1) * 256	CfO_CounterNevent0IDwr (Index N = 1 to 4)	UDINT				●
2120 + (N-1) * 256	CfO_CounterNevent0config (Index N = 1 to 4)	UINT				●
2144 + (N-1) * 256	CfO_CounterNevent1IDwr (Index N = 1 to 4)	UINT				●
2152 + (N-1) * 256	CfO_CounterNevent1config (Index N = 1 to 4)	UINT				●
2148 + (N-1) * 256	CfO_CounterNevent1mode (Index N = 1 to 4)	USINT				●
Configuration - Inputs for AB, up/down and event counters						
2048 + (N-1) * 256	CfO_CounterNconfig (Index N = 1 to 4)	USINT				●
2056 + (N-1) * 256	CfO_CounterNconfigReg0 (Index N = 1 to 4)	USINT				●
2058 + (N-1) * 256	CfO_CounterNconfigReg1 (Index N = 1 to 4)	USINT				●
2112 + (N-1) * 256	CfO_CounterNevent0IDwr (Index N = 1 to 4)	UDINT				●
2120 + (N-1) * 256	CfO_CounterNevent0config (Index N = 1 to 4)	UINT				●
2116 + (N-1) * 256	CfO_CounterNevent0mode (Index N = 1 to 4)	USINT				●
2144 + (N-1) * 256	CfO_CounterNevent1IDwr (Index N = 1 to 4)	UINT				●
2152 + (N-1) * 256	CfO_CounterNevent1config (Index N = 1 to 4)	UINT				●
2148 + (N-1) * 256	CfO_CounterNevent1mode (Index N = 1 to 4)	USINT				●
Configuration - Inputs for SSI encoders						
7,176	CfO_SSI1cfg	UINT				●
7,432	CfO_SSI2cfg	UINT				●
7,180	CfO_SSI1control	USINT				●
7,436	CfO_SSI2control	USINT				●
7,168	CfO_SSI1eventIDwr	UINT				●
7,424	CfO_SSI2eventIDwr	UINT				●
7,232	CfO_SSI1event0IDwr	UINT				●
7,488	CfO_SSI2event0IDwr	UINT				●

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
7,240	CfO_SSI1event0config	UINT				●
7,496	CfO_SSI2event0config	UINT				●
7,236	CfO_SSI1event0mode	USINT				●
7,492	CfO_SSI2event0mode	USINT				●
7,172	ConfigAdvanced01	UDINT				●
7,428	ConfigAdvanced02	UDINT				●
Configuration - Comparator function for ABR, AB, SSI encoders and up/down counters						
256	CfO_OutClearMask	USINT				●
258	CfO_OutSetMask	USINT				●
1,024	CfO_DIREKTIOoutevent0IDwr	UINT				●
1034 + N * 32	CfO_DIREKTIOoutsetmaskN (Index N = 0 to 3)	USINT				●
1032 + N * 32	CfO_DIREKTIOoutclearmaskN (Index N = 0 to 3)	USINT				●
1,066	CfO_DIREKTIOoutsetmask1	USINT				●
1,064	CfO_DIREKTIOoutclearmask1	USINT				●
1024 + N * 32	CfO_DIREKTIOouteventNIDwr (Index N = 0 to 3)	UINT				●
Configuration - Outputs for PWM (pulse width modulation)						
6144 + N * 16	CfO_PWMNprescaler (Index N = 0 to 3)	UINT				●
Module communication - General						
40	Status of encoder supply	USINT	●			
	PowerSupply01	Bit 0				
Communication - Digital inputs						
264	Input states of the channels	USINT	●			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
Communication - Event counters						
2,080	EventCounter01	U(D)INT	●			
2,084	EventCounter02	U(D)INT	●			
2,336	EventCounter03	U(D)INT	●			
2,340	EventCounter04	U(D)INT	●			
2,592	EventCounter05	U(D)INT	●			
2,596	EventCounter06	U(D)INT	●			
2,848	EventCounter07	U(D)INT	●			
2,852	EventCounter08	U(D)INT	●			
Communication - Input for ABR encoders (optionally with comparator)						
2,080	ABREncoder01	(D)INT	●			
2,592	ABREncoder02	(D)INT	●			
2,116	ReferenceModeABR01	USINT			●	
2,628	ReferenceModeABR02	USINT			●	
2,160	OriginComparator01	(D)INT			●	
2,164	MarginComparator01	U(D)INT			●	
264	Input states of the channels	USINT	●			
	ComparatorActualValue02	Bit 1				
	ReferenceEnableSwitch01 (without comparator) ComparatorActualValue01 (with comparator) ComparatorActualValue02 (with comparator)	Bit3				
	ComparatorActualValue01	Bit 5				
	ReferenceEnableSwitch02 (without comparator) ComparatorActualValue01 (with comparator) ComparatorActualValue02 (with comparator)	Bit 7				
2,172	Latch01ABR01	(D)INT	●			
2,684	Latch01ABR02	(D)INT	●			
2,118	StatusABR01	USINT	●			
2,630	StatusABR02	USINT	●			
Communication - Input for AB						
2080 + (N-1) * 256	ABEncoder0N (Index N = 1 to 4)	(D)INT	●			
2,336	ABEncoder02	(D)INT	●			
2,160	OriginComparator01	(D)INT			●	
2,164	MarginComparator01	U(D)INT			●	
264	Input states of the channels	USINT	●			
	ComparatorActualValue03	Bit 1				
	ComparatorActualValue01 ComparatorActualValue03	Bit 3				
	ComparatorActualValue01	Bit 5				
	ComparatorActualValue01 ComparatorActualValue03	Bit 7				
2140 + (N-1) * 256	Latch01AB0N (Index N = 1 to 4)	(D)INT	●			
2172 + (N-1) * 256	Latch02AB0N (Index N = 1 to 4)	(D)INT	●			
Communication - Up/down counters						
2080 + (N-1) * 256	Counter0N (Index N = 1 to 4)	U(D)INT	●			
2,160	OriginComparator01	U(D)INT			●	
2,164	MarginComparator01	U(D)INT			●	
264	Input states of the channels	USINT	●			
	ComparatorActualValue03	Bit 1				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
	ComparatorActualValue01 ComparatorActualValue03	Bit 3				
	ComparatorActualValue01	Bit 5				
	ComparatorActualValue01 ComparatorActualValue03	Bit 7				
2140 + (N-1) * 256	Latch01Counter0N (Index N = 1 to 4)	U(D)INT	•			
2172 + (N-1) * 256	Latch02Counter0N (Index N = 1 to 4)	U(D)INT	•			
Communication - Input for SSI encoders						
7,184	SSIEncoder01	UDINT	•			
7,440	SSIEncoder02	UDINT	•			
7,248	OriginComparator01	UDINT			•	
7,504	OriginComparator02	UDINT			•	
7,252	MarginComparator01	UDINT			•	
7,508	MarginComparator02	UDINT			•	
264	Input states of the channels	USINT	•			
	ComparatorActualValue02	Bit 1				
	ComparatorActualValue01 ComparatorActualValue02	Bit 3				
	ComparatorActualValue01	Bit 5				
	ComparatorActualValue01 ComparatorActualValue02	Bit 7				
7,260	Latch01SSI01	UDINT	•			
7,516	Latch01SSI02	UDINT	•			
Communication - Digital outputs						
260	Output states of the channels	USINT			•	
	DigitalOutput02	Bit 1				
	DigitalOutput04	Bit 3				
	DigitalOutput06	Bit 5				
	DigitalOutput08	Bit 7				
264	Input states of the channels	USINT	•			
	StatusDigitalOutput02	Bit 1				
	StatusDigitalOutput04	Bit 3				
	StatusDigitalOutput06	Bit 5				
	StatusDigitalOutput08	Bit 7				
Communication - Outputs for PWM (pulse width modulation)						
6130 + N * 8	PWMOutput0N (Index N = 2,4,6,8)	UINT			•	
Configuration - Edge detection						
4,104	CfO_EdgeDetectFalling	USINT				•
4,106	CfO_EdgeDetectRising	USINT				•
4,108	CfO_FallingDisProtection	USINT				•
4,110	CfO_RisingDisProtection	USINT				•
Configuration - Time measurement						
4,336	CfO_EdgeTimeglobalenable	USINT				•
4344 + N * 8	CfO_EdgeTimeFallingMode0N (Index N = 1 to 8)	UINT				•
4472 + N * 8	CfO_EdgeTimeRisingMode0N (Index N = 1 to 8)	UINT				•
Communication - Time measurement						
4,342	Trigger rising edge detection	USINT			•	
	TriggerRisingCH01	Bit 0				
	...	...				
	TriggerRisingCH08	Bit 7				
4,350	Show first rising trigger edge	USINT	•			
	BusyTriggerRisingCH01	Bit 0				
	...	...				
	BusyTriggerRisingCH08	Bit 7				
4,340	Trigger falling edge detection	USINT			•	
	TriggerFallingCH01	Bit 0				
	...	...				
	TriggerFallingCH08	Bit 7				
4,348	Show first falling trigger edge	USINT	•			
	BusyTriggerFallingCH01	Bit 0				
	...	...				
	BusyTriggerFallingCH08	Bit 7				
4474 + N * 8	CountRisingCH0N (Index N = 1 to 8)	USINT	•			
4476 + N * 8	TimeStampRisingCH0N (Index N = 1 to 8)	UINT	•			
4478 + N * 8	TimeDiffRisingCH0N (Index N = 1 to 8)	UINT	•			
4346 + N * 8	CountFallingCH0N (Index N = 1 to 8)	USINT	•			
4348 + N * 8	TimeStampFallingCH0N (Index N = 1 to 8)	UINT	•			
4350 + N * 8	TimeDiffFallingCH0N (Index N = 1 to 8)	UINT	•			

4.11.17.12.3 Function model 254 - Bus controller

Unlike the function models 0 and 1, this model only offers a selection of functions with a limited scope of configuration on the module.

The following functions are provided and can be run at the same time:

- SSI encoders
- ABR encoder with configurable reference pulse edge and reference position
- 1 event counter with configurable counting direction
- 2 PWM outputs

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Module configuration - General							
N * 2 - 2	-	CfO_CFGchannel0N (Index N = 1 to 8)	USINT				●
N * 2 + 64	-	CfO_LEDNsource (Index N = 0 to 7)	USINT				●
Configuration - ABR encoder							
512	-	CfO_DIREKTIOevent0IDwr	UINT				●
544	-	CfO_DIREKTIOevent1IDwr	UINT				●
2,560	-	CfO_Counter3config	USINT				●
2,568	-	CfO_Counter3configReg0	USINT				●
2,570	-	CfO_Counter3configReg1	USINT				●
2,576	-	CfO_Counter3PresetValue1	UINT				●
2,580		CfO_Counter3PresetValue2	UINT				●
2,624	-	CfO_Counter3event0IDwr	UINT				●
2,632	-	CfO_Counter3event0config	UINT				●
2,628	-	CfO_Counter3event0mode	USINT				●
2,656	-	CfO_Counter3event1IDwr	UINT				●
2,664	-	CfO_Counter3event1config	UINT				●
2,660	-	CfO_Counter3event1mode	USINT				●
4,104	-	CfO_EdgeDetectFalling	USINT				●
4,106	-	CfO_EdgeDetectRising	USINT				●
Configuration - Event counter							
2,304	-	CfO_Counter2config	USINT				●
2,312	-	CfO_Counter2configReg0	USINT				●
2,314	-	CfO_Counter2configReg1	USINT				●
2,368	-	CfO_Counter2event0IDwr	UINT				●
2,376	-	CfO_Counter2event0config	UINT				●
2,372	-	CfO_Counter2event0mode	USINT				●
2,400	-	CfO_Counter2event1IDwr	UINT				●
2,408	-	CfO_Counter2event1config	UINT				●
2,404	-	CfO_Counter2event1mode	USINT				●
Configuration - SSI encoder							
7,176	-	CfO_SSI1cfg	UINT				●
7,180	-	CfO_SSI1control	USINT				●
7,168	-	CfO_SSI1eventIDwr	UINT				●
7,232	-	CfO_SSI1event0IDwr	UINT				●
7,240	-	CfO_SSI1event0config	UINT				●
7,236	-	CfO_SSI1event0mode	USINT				●
7,172	-	ConfigAdvanced01	UDINT				●
Configuration - PWM (pulse width modulation)							
6,160	-	CfO_PWM1prescaler	UINT				●
6,192	-	CfO_PWM3prescaler	UINT				●
Module communication - General							
40	6	Status of encoder supply	USINT	●			
		PowerSupply01	Bit 0				
Communication - Counters and encoders							
2,336	4	EventCounter03	UINT	●			
2,592	8	ABREncoder02	INT	●			
2,628	10	ReferenceModeABR02	USINT			●	
2,630	10	StatusABR02	USINT	●			
7,184	0	SSIEncoder01	UDINT	●			
Communication - PWM (pulse width modulation)							
6,162	0	PWMOutput04	UINT			●	
6,194	8	PWMOutput08	UINT			●	

1) The offset specifies the position of the register within the CAN object.

4.11.17.12.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.11.17.12.4 General module registers

4.11.17.12.4.1 Configuring LED status indicators

Name:
CfO_LED0source to CfO_LED7source

These registers can be used to define how the module's LED status indicators are used. Blinking patterns can be generated from the application, and the status of the physical inputs and outputs can be indicated.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	MODE = 0	0	LED off
		1	Blinking quickly
		2	Blinking
		3	Blinking slowly
		4	Single flash
		5	Double flash
		6 to 15	Reserved
	MODE = 1 (inverted)	0	LED on
		1	Blinking quickly
		2	Blinking
		3	Blinking slowly
		4	Single flash
		5	Double flash
		6 to 15	Reserved
	MODE = 2	0 to 7	Number of the physical input channel
		8 to 15	Reserved
	MODE = 3	0 to 7	Number of the physical output channel
		8 to 15	Reserved
4 - 7	Selection of the mode for the LED status indicator	0	LED blinking pattern
		1	Inverted LED blinking pattern
		2	Displays a channel's physical input status
		3	Displays a channel's physical output status
		4 to 15	Reserved

4.11.17.12.4.2 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.11.17.12.5 Digital inputs and outputs

4.11.17.12.5.1 Configure physical channels

Name:
CfO_CFGchannel01 to CfO_CFGchannel08

This register can be used to configure physical I/O channels 1 to 8.

Information:

Except for bit 2 (inverted input), all other bits are only available for channels 2, 4, 6 and 8.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Push[1)]	0	Disabled
		1	Enabled
1	Pull[1)]	0	Disabled
		1	Enabled
2	Inverted input	0	Disabled
		1	Enabled
3	Inverted output	0	Disabled
		1	Enabled
4 - 7	Output type	0	Direct I/O
		1 to 5	Reserved
		6	PWM (channel-specific)
		7	SSI clock (channel-specific)

1) To configure a channel as an output, Push and/or Pull must be enabled.

4.11.17.12.5.2 Reset mask of the digital channels

Name:
CfO_OutClearMask

The settings in this register only affect the values written to registers 4.11.17.12.5.5 "DigitalOutput02 to 08".

- 0 allows manual reset of digital outputs using registers DigitalOutput02 to 08
- 1 prevents manual reset of digital outputs using registers DigitalOutput02 to 08

When "1" is used, the "output event function" can be used to reset the outputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	DigitalOutput02	0	Writing 0 to the DigitalOutput02 register resets the output
		1	Writing 0 from the DigitalOutput02 register does not reset the output
2	Reserved	-	
3	DigitalOutput04	0	Writing 0 to the DigitalOutput04 register resets the output
		1	Writing 0 from the DigitalOutput04 register does not reset the output
4	Reserved	-	
5	DigitalOutput06	0	Writing 0 to the DigitalOutput06 register resets the output
		1	Writing 0 from the DigitalOutput06 register does not reset the output
6	Reserved	-	
7	DigitalOutput08	0	Writing 0 to the DigitalOutput08 register resets the output
		1	Writing 0 from the DigitalOutput08 register does not reset the output

4.11.17.12.5.3 Set mask of the digital channels

Name:
CfO_OutSetMask

The settings in this register only affect the values written to registers 4.11.17.12.5.5 "DigitalOutput02 to 08".

- 0 allows manual setting of digital outputs using registers DigitalOutput02 to 04
- 1 prevents manual setting of digital outputs using registers DigitalOutput02 to 04

When "1" is used, the "output event function" can be used to reset the outputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	DigitalOutput02	0	Writing 1 to the DigitalOutput02 register sets the output
		1	Writing 1 from the DigitalOutput02 register does not set the output
2	Reserved	-	
3	DigitalOutput04	0	Writing 1 to the DigitalOutput04 register sets the output
		1	Writing 1 from the DigitalOutput04 register does not set the output
4	Reserved	-	
5	DigitalOutput06	0	Writing 1 to the DigitalOutput06 register sets the output
		1	Writing 1 from the DigitalOutput06 register does not set the output
6	Reserved	-	
7	DigitalOutput08	0	Writing 1 to the DigitalOutput08 register sets the output
		1	Writing 1 from the DigitalOutput08 register does not set the output

4.11.17.12.5.4 Input states of the channels

Name:
see "Name in the AS I/O configuration"

This register reads the input status of a physical channel. The polarity settings are accounted for in the value (bit 2 in 4.11.17.12.5.1 "CfO_CFGchannel[x]" register).

The bits in this register are shown in the AS I/O mapping table under different names based on the function used in order to improve readability.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Physical input channel	Value	Name in the AS I/O configuration
0	Channel 1	0 or 1	DigitalInput01
1	Channel 2	0 or 1	DigitalInput02 StatusDigitalOutput02 ComparatorActualValue02 ComparatorActualValue03
2	Channel 3	0 or 1	DigitalInput03
3	Channel 4	0 or 1	DigitalInput04 StatusDigitalOutput04 ReferenceEnableSwitch01 ComparatorActualValue01 ComparatorActualValue02 ComparatorActualValue03
4	Channel 5	0 or 1	DigitalInput05
5	Channel 6	0 or 1	DigitalInput06 StatusDigitalOutput06 ComparatorActualValue01
6	Channel 7	0 or 1	DigitalInput07
7	Channel 8	0 or 1	DigitalInput08 StatusDigitalOutput08 ReferenceEnableSwitch02 ComparatorActualValue01 ComparatorActualValue02 ComparatorActualValue03

4.11.17.12.5.5 Output states of the channels

Name:
DigitalOutput02 to DigitalOutput08

The output status of a physical channel can be written using this register. In order to configure a channel as an output:

1 Bit 0 "Push" and/or bit 1 "Pull" must be enabled in the 4.11.17.12.5.1 "CfO_CFGchannel[x]" register.
2 Bits 4 to 7 in the 4.11.17.12.5.1 "CfO_CFGchannel[x]" register must be set to Direct I/O.
3 0 must be set for the respective channel in the 4.11.17.12.5.2 "CfO_OutClearMask" and 4.11.17.12.5.3 "CfO_OutSetMask" registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	DigitalOutput02	0 or 1	Output status of channel 2
2	Reserved	-	
3	DigitalOutput04	0 or 1	Output status of channel 4
4	Reserved	-	
5	DigitalOutput06	0 or 1	Output status of channel 6
6	Reserved	-	
7	DigitalOutput08	0 or 1	Output status of channel 8

4.11.17.12.6 Event functions

The module provides configurable event functions. An event function can be connected to physical I/O and the values derived from them (e.g. counters) or be purely used for internal processing.

Every event function has event inputs and outputs. Event functions can also have only inputs or only outputs. Each event output has a unique event ID. It is possible to configure when an event should be generated on an event output. The effect of an event is determined by the respective event function.

Event functions can also be linked to one another. The link takes place using the event input. Every event input has a 16-bit register to which the event number of the linked event output is written.

Information:

The module functions that can be configured in the AS I/O configuration are primarily based on these event functions and their links. Changes in the AS I/O configuration have multiple effects on event functions and their links.

4.11.17.12.6.1 List of event IDs

Various hardware and software functions send event IDs or require event IDs in order to start. The following table shows all of the IDs available to configure the module.

Event ID	Description	
Direct event inputs		
512	Comparator condition 1	FALSE
513		TRUE
544	Comparator condition 2	FALSE
545		TRUE
576	Comparator condition 3	FALSE
577		TRUE
608	Comparator condition 4	FALSE
609		TRUE
Counter comparator function		
2,112	Counter function 1	Event function 1; FALSE
2,113		Event function 1; TRUE
2,144		Event function 2; FALSE
2,145		Event function 2; TRUE
2,368	Counter function 2	Event function 1; FALSE
2,369		Event function 1; TRUE
2,400		Event function 2; FALSE
2,401		Event function 2; TRUE
2,624	Counter function 3	Event function 1; FALSE
2,625		Event function 1; TRUE
2,656		Event function 2; FALSE
2,657		Event function 2; TRUE
2,880	Counter function 4	Event function 1; FALSE
2,881		Event function 1; TRUE
2,912		Event function 2; FALSE
2,913		Event function 2; TRUE
Edge events		
4,096	Falling edge on I/O channel	Channel 1
...		...
4,103		Channel 8
4,112	Rising edge on I/O channel	Channel 1
...		...
4,119		Channel 8
4,128	Rising or falling edge on I/O channel	Channel 1
...		...
4,135		Channel 8
SSI counter events		
7,168	SSI 1	SSI valid
7,169		SSI ready
7,424	SSI 2	SSI valid
7,425		SSI ready
SSI comparator events		
7,232	SSI 1 comparator condition	FALSE
7,233		TRUE
7,488	SSI 2 comparator condition	FALSE
7,489		TRUE
Timerevents		
208	Timer1	50 µs
209	Timer2	100 µs
210	Timer3	200 µs
211	Timer4	400 µs
212	Timer5	800 µs
213	Timer6	1600 µs
214	Timer7	3200 µs
215	Timer8	3200 µs (time offset to timer 7)
Network functions		
224	SOAISOP (**s**ynchronous **o**ut **a**synchronous **i**n **s**tart of **p**rotocol)	
225	AOSISOP (**a**synchronous **o**ut **s**ynchronous **i**n **st**art of **p**rotocol)	
226	SOAIEOP (**s**ynchronous **o**ut **a**synchronous **i**n **e**nd of **p**rotocol)	
227	AOSIEOP (**a**synchronous **o**ut synchronous **i**n **e**nd of **p**rotocol)	
Idle event		
192	No-load operation	

Timer

There are 8 timer events that the module can generate.

Information:

The timers have the highest event priority. All other system functions are interrupted when a timer event occurs, and jitter for the amount of time it takes to process the event.

Idle event

Idle time is the time that remains after the system has processed all higher priority events and operations. The module performs the following functions during idle time:

- Handling of the asynchronous protocol
- Mechanism for (re-)linking events
- Operation of LEDs
- Execution of event event functions linked to the idle function

4.11.17.12.6.2 Edge events

For each physical channel there are 3 event functions

- Falling edge
- Rising edge
- Falling and rising edge

The respective event is triggered when an edge is detected on the hardware input and the "CfO_EdgeDetectRising" and/or "CfO_EdgeDetectFalling" register has been configured for the respective channel.

Edges are detected by the hardware and processed for each interrupt. The interrupt handler uses an event distributor, which requires a specific amount of time for each edge to operate the hardware and execute linked event functions. To reduce this time, edge detection can be enabled/disabled individually for each channel. To optimize system load and I/O jitter, it is important to only enable edge detection where it is actually needed.

Information:

Edge detection can also be used for channels that are configured as outputs.

Event frequency limitation

To stabilize the system, there is a mechanism that limits the number of events created through edge recognition. At least one idle event must occur between two edge events for the same edge.

The "CfO_FallingDisProtection" and "CfO_RisingDisProtection" registers can be used to disable this limitation for each edge, and then an event will be generated for every edge. However, this can cause a system overload, i.e. I/O operation can fail for up to 100 ms before the module changes to the reset state.

Generate event on falling edge

Name:
CfO_EdgeDetectFalling

This register defines whether an event is generated on a falling edge.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	No event generated on falling edge.
		1	Events 4096 and 4128 are generated on falling edge.
...		...	
7	Channel 8	0	No event generated on falling edge.
		1	Events 4103 and 4135 are generated on falling edge.

Generate event on rising edge

Name:
CfO_EdgeDetectRising

This register defines whether an event is generated on a rising edge.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	No event generated on rising edge.
		1	Events 4112 and 4128 are generated on rising edge.
...		...	
7	Channel 8	0	No event generated on rising edge.
		1	Events 4119 and 4135 are generated on rising edge.

Enable limit for falling edges

Name:
CfO_FallingDisProtection

This register can be used to enable/disable the event frequency limit for falling edges on the respective channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Event frequency limit enabled.
		1	Event frequency limit disabled.
...		...	
7	Channel 7	0	Event frequency limit enabled.
		1	Event frequency limit disabled.

Enable limit for rising edges

Name:
CfO_RisingDisProtection

This register can be used to enable/disable the event frequency limit for rising edges on the respective channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Event frequency limit enabled.
		1	Event frequency limit disabled.
...		...	
7	Channel 8	0	Event frequency limit enabled.
		1	Event frequency limit disabled.

4.11.17.12.6.3 Direct input functions

The module has 2 "direct input functions"

These event functions are based on comparator functionality. If the event configured in the "CfO_DIREKTIO-event0IDwr" register occurs, the event function compares the status of all Direct I/O channels enabled in the "CfO_EvCompMask" register to a status defined in the "CfO_DIREKTIOeventcompState" register. The event that is generated depends on the results of this comparison.

- If the respective bits are the same, then event number 513 or 545 is generated
- If the respective bits are different, then event number 512 or 544 is generated

Configure event ID for input function

Name:
CfO_DIREKTIOevent0IDwr to CfO_DIREKTIOevent1IDwr

This register holds the event ID generated by the direct input function. For a list of all possible event IDs, see 4.11.17.12.6.1 "List of event IDs"

Data type	Value	Information
INT	192 to 7,289	ID of event function

Configure the mode of the input function

Name:
CfO_DIREKTIOevent0mode to CfO_DIREKTIOevent1mode

The mode in which the direct input function operates can be set in this register.

Comparator functions can be operated in 4 different modes. For a description, see "Comparator modes".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Single
		2	State change
		3	Continuous
2 - 7	Reserved	-	

Comparator status for comparator mask

Name:
CfO_DIREKTIOevent0compState to CfO_DIREKTIOevent1compState

This register contains the status bits that are compared with the bits specified in the "CfO_Ev0CompMask" register, which contain the I/O input status, when an event is received.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator status of channel 1	0 or 1	
...		...	
7	Comparator status of channel 8	0 or 1	

Configure the comparator mask for the input function

Name:
CfO_Ev0CompMask to CfO_Ev1CompMask

If a bit is set, then the input status of the respective channel is compared with that bit in the "CfO_DIREKTIOevent-compState" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Do not compare bit
		1	Compare bit in register
...		...	
7	Channel 8	0	Do not compare bit
		1	Compare bit in register

4.11.17.12.6.4 Direct output functions

The module has 4 of these event functions

The effect of executing this event function is similar to writing to the 4.11.17.12.5.5 "DigitalOutput02 to 08" registers. When this event function is triggered, however, the changed output states are passed on to the hardware immediately, regardless of the X2X cycle.

When this event function is used, the masks of the respective outputs (see 4.11.17.12.5.2 "CfO_OutClearMask" and 4.11.17.12.5.3 "CfO_OutSetMask" registers) must be set to 1. Otherwise the output status would constantly be overwritten by the values in the 4.11.17.12.5.5 "DigitalOutput02 to 08" registers.

Configure event ID for output function

Name:
CfO_DIREKTIOevent0IDwr to CfO_DIREKTIOevent3IDwr

These registers hold the event IDs that trigger the direct output function. For a list of all possible event IDs, see 4.11.17.12.6.1 "List of event IDs"

Data type	Value	Information
INT	192 to 7,489	ID of event function

Configure channels for resetting

Name:
CfO_DIREKTIOoutclearmask0 to CfO_DIREKTIOoutclearmask3

Writing "1" to the bit position that corresponds to a channel resets the output if the output event function is being executed. This corresponds to writing "0" to the 4.11.17.12.5.5 "DigitalOutput 02 to 08" registers.

The bit that corresponds to channels that should be reset should be set to "1" in the 4.11.17.12.5.2 "CfO_OutClearMask" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	Channel 2	0	Reset channel 2
		1	Do not reset channel 2
2	Reserved	-	
3	Channel 4	0	Reset channel 4
		1	Do not reset channel 4
4	Reserved	-	
5	Channel 6	0	Reset channel 6
		1	Do not reset channel 6
6	Reserved	-	
7	Channel 8	0	Reset channel 8
		1	Do not reset channel 8

Configure channels for setting

Name:
CfO_DIREKTIOoutsetmask0 to CfO_DIREKTIOoutsetmask3

Writing "1" to the bit position that corresponds to a channel sets the output if the output event function is being executed. This corresponds to writing "1" to the 4.11.17.12.5.5 "DigitalOutput 02 to 08" registers.

The bit that corresponds to channels that should be reset should be set to "1" in the 4.11.17.12.5.3 "CfO_OutSet-Mask" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	Channel 2	0	Set channel 2
		1	Do not set channel 2
2	Reserved	-	
3	Channel 4	0	Set channel 4
		1	Do not set channel 4
4	Reserved	-	
5	Channel 6	0	Set channel 6
		1	Do not set channel 6
6	Reserved	-	
7	Channel 8	0	Set channel 8
		1	Do not set channel 8

4.11.17.12.7 Counters and encoders

The module has 4 internal counter functions, each with 2 event counter registers. Each of these 4 counters is permanently assigned to 2 physical inputs. This assignment cannot be changed.

The counter registers perform different functions based on how the event functions are connected. The counter registers can be configured in the following ways:

- ABR counter
- AB counter
- Up/down counters
- Event counters

Different names are used for them in Automation Studio and in the register description to improve clarity.

Channel	Counter function	Counter register	Name in AS
1	1	1	ABEncoder01 ABREncoder01 Counter01 EventCounter01
2		2	EventCounter02
3	2	1	ABEncoder02 Counter02 EventCounter03
4		2	EventCounter04
5	3	1	ABEncoder03 ABREncoder02 Counter03 EventCounter05
6		2	EventCounter06
7	4	1	ABEncoder04 Counter04 EventCounter07
8		2	EventCounter08

4.11.17.12.7.1 Counter value calculation

There are 3 steps for calculating the state of any counter function

1. The counter value is based on the 2 absolute value counters "abs1" and "abs2". These are only used internally in the module and cannot be read. Depending on the mode, these registers show the respective physical input signals.

	Mode		
	Edge counters	AB encoders	Up/down counter
abs1	Edges of counter channel 1	Increments in positive direction	Counter channel 2 = 0: Edges of counter channel 1 in up direction
abs2	Edges of counter channel 2	Increments in negative direction	Counter channel 2 = 1 Edges of counter channel 1 in down direction

2. From the absolute value registers "abs1" and "abs2", 2 more counters are formed: "counter 1" and "counter 2". They are only used internally in the module and cannot be read. The following values are used for the calculation:

- Absolute value registers "abs1" and "abs2"
- SW_reference_counter 1 and 2: This reference value can be defined by the "CfO_CounterPresetValue" register to allow referencing <> 0.
- HW_reference_counter 1 and 2: In the "CfO_CounterEventMode" register, you can configure whether latched values should be copied to these registers when counter events occur.

counter1 = abs1 + SW_reference_counter1 - HW_reference_counter1
counter2 = abs2 + SW_reference_counter2 - HW_reference_counter2

3. The counter registers contain the sum of the two internal counters "counter 1" and "counter 2". The "CfO_CounterConfigReg" register allows you to define a sign for each "counter" register and define whether or not it should be used.

Counter register = counter1 + counter2

4.11.17.12.7.2 Sample configurations

All of the settings available in Automation Studio for AB encoders, ABR encoders, up/down counters and event counters are based on the two counter functions.
The following configuration examples show the values with which Automation Studio initializes the module registers in order to implement these functions.

I/O configuration - AB encoder

The following table shows how the module's various event functions can be linked in order to configure an AB encoder.

[x] stands for the respective counter function, from 1 to 4

Register	Value	Comment
For the function		
CfO_Counter[x]config	0x01	Mode = Up/down counter
CfO_Counter[x]configReg0	0x0D	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.17.12.7.1 "Counter value calculation" and "Examples of calculation configurations")
For the latch		
CfO_Counter[x]event0config	0x000D	Configuration of the calculation of the first value used for the latch
CfO_Counter[x]event0mode	0x03	Mode of the first counter event function - Continuous
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger Latch 1 ("Latch 01 - Channel" in the AS I/O configuration).
CfO_Counter[x]event1config	0x0D	Configuration of the calculation of the second value used for the latch
CfO_Counter[x]event1mode	0x03	Mode of the second counter event function - Continuous
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger Latch 2
For the comparator		
CfO_Counter1event1IDwr CfO_Counter3event1IDwr	0x00D0	Event number of Timer 1 (50 µs) **Information:** **The latch and comparator must not have the same event number!**
CfO_Counter1event1config CfO_Counter3event1config	0x900D or 0xA00D	Configuration of the comparator for the second counter event
CfO_Counter1event1mode CfO_Counter3event1mode	0x03	Mode of the second counter event function - Continuous
CfO_DIREKTIOoutevent0IDwr CfO_DIREKTIOoutevent2IDwr	0x0861 0x0A61	TRUE event output of the second counter to trigger the direct output function (set outputs).
CfO_DIREKTIOoutsetmask0 CfO_DIREKTIOoutsetmask2	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be set when comparator condition = TRUE
CfO_DIREKTIOoutevent1IDwr CfO_DIREKTIOoutevent3IDwr	0x0860 0x0A60	FALSE event output of the second counter to trigger the direct output function (reset outputs).
CfO_DIREKTIOoutclearmask1 CfO_DIREKTIOoutclearmask3	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be reset when comparator condition = FALSE

I/O configuration - ABR encoder

The following table shows how the module's various event functions can be linked in order to configure an ABR encoder.

Register	Value	Comment
For the function		
CfO_Counter1PresetValue1 CfO_Counter3PresetValue1	(any)	Desired offset value for referencing
CfO_Counter1event0IDwr CfO_Counter3event0IDwr	0x0201	Link between the first counter event and the "direct input" comparator condition TRUE
CfO_Counter1config CfO_Counter3config	0x01	Mode = AB encoder
CfO_Counter1configReg0 CfO_Counter3configReg0	0x0D	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.17.12.7.1 "Counter value calculation" and "Examples of calculation configurations")
CfO_DIREKTIOevent0IDwr CfO_DIREKTIOevent1IDwr	0x1002 or 0x1012	Selection of the desired input edge as trigger for the ABR encoder function
CfO_Counter1event0config CfO_Counter3event0config	0x0000	Configuration of the first counter event (for referencing)
CfO_DIREKTIOevent0mode CfO_DIREKTIOevent1mode	0x03	Mode of the "direct input function" - Continuous
CfO_DIREKTIOevent0compState CfO_DIREKTIOevent1compState	0x00 or 0x08	Comparator status for the "direct input function"
CfO_Ev0CompMask CfO_Ev1CompMask	0x08	Comparator mask for the "direct input function"
For the latch		
CfO_Counter1event0config CfO_Counter3event1config	0x000D	Configuration of the calculation of the value used for the latch
CfO_Counter1event0mode CfO_Counter3event1mode	0x03	Mode of the first counter event function - Continuous
CfO_Counter1event0IDwr CfO_Counter3event1IDwr	(any)	Number of the event that should trigger the latch
For the comparator		
CfO_Counter1event1IDwr CfO_Counter3event1IDwr	0x00D0	Event number of Timer 1 (50 µs) **Information:** **The latch and comparator must not have the same event number!**
CfO_Counter1event1config CfO_Counter3event1config	0x900D or 0xA00D	Configuration of the comparator for the second counter event
CfO_DIREKTIOoutevent0IDwr CfO_DIREKTIOoutevent2IDwr	0x0861 0x0A61	TRUE event output of the second counter to trigger the direct output function (set outputs).
CfO_DIREKTIOoutsetmask0 CfO_DIREKTIOoutsetmask2	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be set when comparator condition = TRUE
CfO_DIREKTIOoutevent1IDwr CfO_DIREKTIOoutevent3IDwr	0x0860 0x0A60	FALSE event output of the second counter to trigger the direct output function (reset outputs).
CfO_DIREKTIOoutclearmask1 CfO_DIREKTIOoutclearmask3	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be reset when comparator condition = FALSE

I/O configuration - Up/down counter

The following table shows how the module's various event functions can be linked in order to configure an up/down counter.

[x] stands for the respective counter function, from 1 to 4

Register	Value	Comment
For the function		
CfO_Counter[x]config	0x03	Counter mode = Up/down counter
CfO_Counter[x]configReg0	0x0D, 0x07	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.17.12.7.1 "Counter value calculation" and "Examples of calculation configurations")
For the latch		
CfO_Counter[x]event0config	0x0D, 0x07	Configuration of the calculation of the first value used for the latch
CfO_Counter[x]event0mode	0x03	Mode of the first counter function - Continuous
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger Latch 1
CfO_Counter[x]event1config	0x0D, 0x07	Configuration of the calculation of the second value used for the latch
CfO_Counter[x]event1mode	0x03	Mode of the second counter function - Continuous
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger Latch 2
For the comparator		
CfO_Counter1event1IDwr CfO_Counter3event1IDwr	0x00D0	Event number of Timer 1 (50 µs) **Information:** **The latch and comparator must not have the same event number!**
CfO_Counter1event1config CfO_Counter3event1config	0x900D, 0xA00d or 0x9007, 0xA007	Configuration of the comparator for the second counter event
CfO_Counter1event1mode CfO_Counter3event1Imode	0x03	Mode of the second counter event function - Continuous
CfO_DIREKTIOoutevent0IDwr CfO_DIREKTIOoutevent2IDwr	0x0861	TRUE event output of the second counter to trigger the direct output function (set outputs).
CfO_DIREKTIOoutsetmask0 CfO_DIREKTIOoutsetmask2	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be set when comparator condition = TRUE
CfO_DIREKTIOoutevent1IDwr CfO_DIREKTIOoutevent3IDwr	0x0860 0x0A60	FALSE event output of the second counter to trigger the direct output function (reset outputs).
CfO_DIREKTIOoutclearmask1 CfO_DIREKTIOoutclearmask3	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be reset when comparator condition = FALSE

I/O configuration - Event counter

The following table shows how the module's various event functions can be linked in order to configure an event counter.

[x] stands for the respective counter function, from 1 to 4

Register	Value	Comment
For event counters on channels 1, 3, 5 and 7		
CfO_Counter[x]configReg0	0x01 or 0x03	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.17.12.7.1 "Counter value calculation" and "Examples of calculation configurations")
CfO_Counter[x]event0mode	0x43	Mode of the first counter event function and referencing configuration
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger referencing
For event counters on channels 2, 4, 6 and 8		
CfO_Counter[x]configReg1	0x04 or 0x08	Configure the calculation of the internal "counter1" and "counter2" registers (see 4.11.17.12.7.1 "Counter value calculation" and "Examples of calculation configurations")
CfO_Counter[x]event1mode	0x83	Mode of the second counter event function and referencing configuration
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger referencing

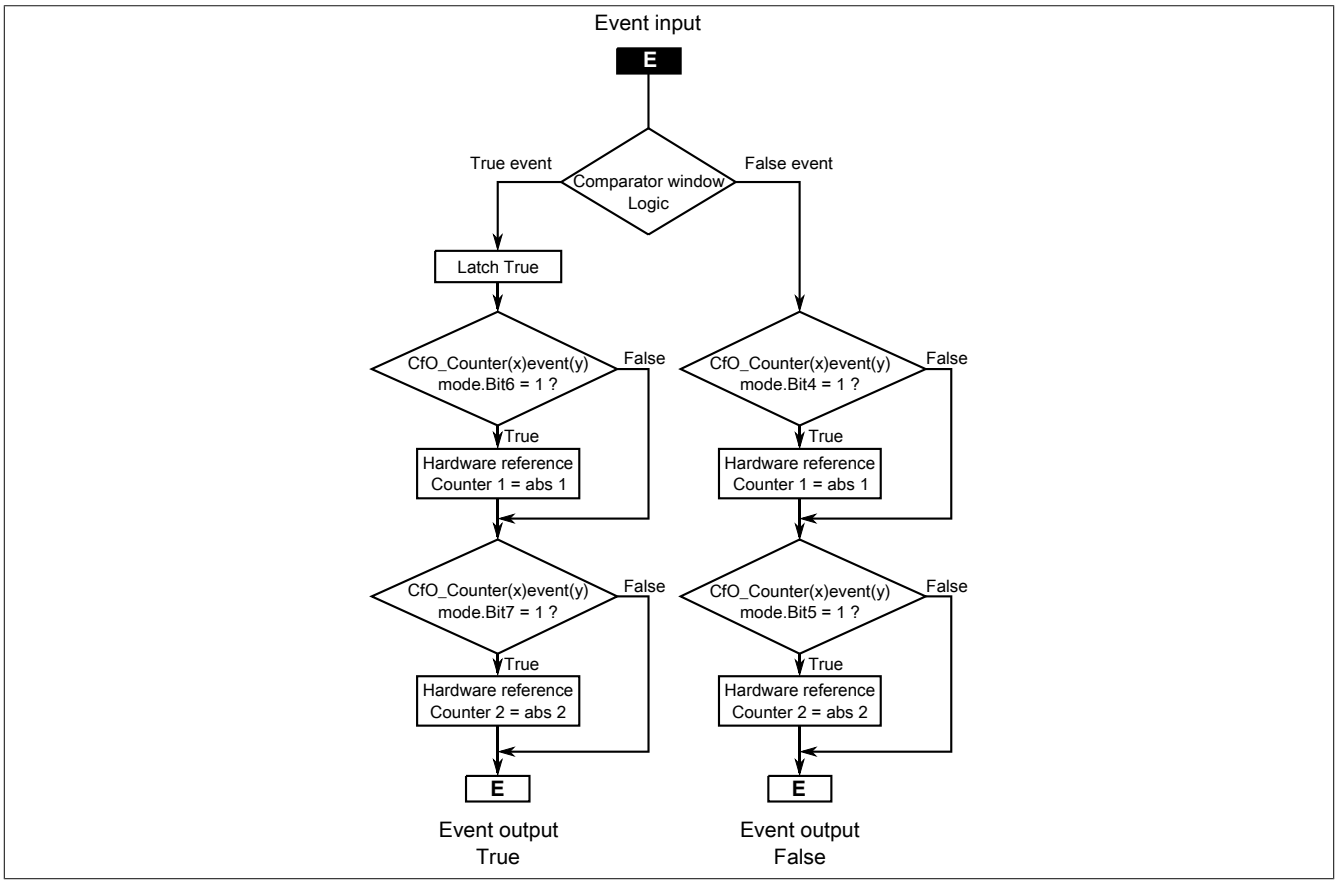
4.11.17.12.7.3 General event functions

Each of the 4 counter functions has 2 counter event functions. These consist of:

- Event ID that triggers the counter event function
- A window comparator
- Latch register for saving the counter value

When the counter event function is complete, a combined event ID in the range 2112 to 2913 (see 4.11.17.12.6.1 "List of event IDs") is sent.

Each counter event function also has the option to copy the current counter value to the "HW reference counter" when an event occurs (see 4.11.17.12.7.1 "Counter value calculation").



Configure counter mode

Name:
CfO_Counter1config to CfO_Counter4config

These registers are used to configure the mode of the counter function. Each counter function can be operated in 3 different modes.

	Counter function mode		
	Edge counters	**AB encoder**	**Up/down counter**
Counter channel 1[1)]	Counting pulses, edge counter 1	A	Metering pulses
Counter channel 2[1)]	Counting pulses, edge counter 2	B	Counting direction (0 = positive, 1 = negative)
Counter register 1	Counter value 1	Position	Counter value
Counter register 2	Counter value 2		

1) Corresponds to the physical channels of the counter functions. See 4.11.17.7.1 "Description of channel assignments".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Counter mode	00	Edge counters
		01	AB encoder
		11	Up/down counter
2 - 7	Reserved	-	

Configure calculation of internal counters

Name:
CfO_Counter1configReg0 to CfO_Counter4configReg0 ("counter 1")
CfO_Counter1configReg1 to CfO_Counter4configReg1 ("counter 2")

The calculation of the internal "counter1" and "counter2" registers can be configured in these registers. For information on using these internal registers, see 4.11.17.12.7.1 "Counter value calculation".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	counter 1 - use	0	0 is added instead of "counter 1"
		1	"counter 1" is used for addition
1	counter 1 - sign	0	The sign of the "counter 1" register is not changed for addition
		1	The sign of the "counter 1" register is reversed for addition
2	counter 2 - use	0	0 is added instead of "counter 2"
		1	"counter 2" is used for addition
3	counter 2 - sign	0	The sign of the "counter 2" register is not changed for addition
		1	The sign of the "counter 2" register is reversed for addition
4 - 7	Reserved	-	

Examples of calculation configurations

0b00000001	= 0x01	Only the "counter1 - use" bit is set, entering the contents of the "counter" (edge of counter event channel 1) directly in the counter register.
0b00000011	= 0x03	"counter 1 - use" and "counter1 - sign" bits are set. The sign is changed so that the counter register counts in the negative direction.
0b00001101	= 0x0d	Edges on counter input channel 1 increase the value in the counter register. Edges on counter input channel 2 decrease the value in the counter register. This value is the best setting for the modes "AB encoder" and "Up/down counter".

Offset value for referencing

Name:
CfO_Counter1PresetValue1 to CfO_Counter4PresetValue1
CfO_Counter1PresetValue1_32Bit to CfO_Counter4PresetValue1_32Bit (SW_reference_counter1)

CfO_Counter1PresetValue2 to CfO_Counter4PresetValue2
CfO_Counter1PresetValue2_32Bit to CfO_Counter4PresetValue2_32Bit (SW_reference_counter2)

These registers can be used to define an offset value for referencing. This value is copied to the internal SW_reference_counter register of the respective counter register.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

Counter register

Name:
Different names are used for these 8 registers depending on their function.

These 8 registers show the results of the counter value calculation for the respective register. Depending on the function, this corresponds to either the encoder position or the counter value.

For information on the relationship between physical channels and counter registers, see 4.11.17.12.7 "Counters and encoders" and 4.11.17.7.1 "Description of channel assignments"

Counter 1 - Counter channel 1		
Counter register	**Function**	**Name**
1	**AB encoders**	ABEncoder01
	ABR encoders	ABREncoder01
	Up/down counters	Counter01
	Event counters	EventCounter01
2	**Event counters**	EventCounter02

Counter 1 - Counter channel 2		
Counter register	**Function**	**Name**
1	**AB encoders**	ABEncoder02
	Up/down counters	Counter02
	Event counters	EventCounter03
2	**Event counters**	EventCounter04

Counter 2 - Counter channel 1		
Counter register	**Function**	**Name**
1	**AB encoders**	ABEncoder03
	ABR encoders	ABREncoder02
	Up/down counters	Counter03
	Event counters	EventCounter05
2	**Event counters**	EventCounter06

Counter 2 - Counter channel 2		
Counter register	**Function**	**Name**
1	**AB encoders**	ABEncoder04
	Up/down counters	Counter04
	Event counters	EventCounter07
2	**Event counters**	EventCounter08

Data type	Value	Information
INT	-32,768 to 32,767	Encoder position or counter value
DINT[1)]	-2,147,483,648 to 2,147,483,647	Encoder position or counter value

1) Only in function model 1

Status of the ABR encoder

Name:
StatusABR01 to StatusABR02

The referencing status of the ABR encoder is shown in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	0	
2	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
3	State change when referencing is complete	0 or 1	State change when referencing is complete
4	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
5 - 7	Continuous counter	xxx	Increased with each reference pulse

Examples of possible values

0b00000000	= 0x00	Referencing OFF or homing procedure already active
0b00111100	= 0x3C	First reference complete, reference value applied in the "ABREncoder0" register
0bxxx11100	= 0xxB	Bits 5 to 7 are changed with each reference pulse
0bxxx1x100	= 0xxx	Bits changed continuously with the setting continuous referencing. With every reference pulse, the reference value is applied to the "ABREncoder0" register

Configure ABR referencing mode

Name:
ReferenceModeABR01 to ReferenceModeABR02

The bits in this register are used to configure the reaction to the configured reference pulse.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Sets the referencing mode	00	Referencing OFF
		01	Single shot referencing
		10	Reserved
		11	Continuous referencing
2 - 5	Reserved	-	
6 - 7	Reserved	11	Must always be 11!

This results in the following values:

0b00000000	= 0x00	Referencing OFF
0b11000001	= 0xC1	Single shot referencing → When starting over after the referencing process is complete, the value 0x00 must be written to start again. Wait until the "StatusABR" register also takes on the value 0x00, then the value 0xC1 can be written again.
0b11000011	= 0xC3	Continuous referencing → Referencing takes place automatically with every reference pulse

4.11.17.12.7.4 Comparator functions

The ABR and AB encoders and the up/down counter have a comparator function. It always works the same and is described here globally for all three.

The comparators are implemented in software form. They do not work actively but rather passively, i.e. the comparison is only carried out when an event is received. The event received is forwarded along the TRUE or FALSE branch depending on the status of the comparator condition. An event function like this generally also offers a latch for the TRUE and FALSE branch to save the value used for the comparator at the time of the event.

Comparator modes

Comparator functions can be operated in 4 different modes.

- **Off**
  Events are ignored.
- **Single**
  The event function is executed once and then disables itself automatically. To re-enable it, the "event function mode" must be changed, preferably to "off" and then to the desired mode. This setting allows a hardware latch to be simulated.
- **State change**
  The event function only responds when the comparator status has changed, i.e. from false to true (or vice versa). Only the first event for each status is processed, e.g. the first "true" of a sequence of events with the comparator condition "true". After the event function is enabled, the first incoming event is used to determine the starting status and therefore not forwarded. This setting allows a hardware comparator to be simulated.
- **Continuous**
  Each incoming event is forwarded to the true or false branch depending on the comparator condition. This setting allows event filters to be created.

Configure event ID for comparator

Name:
CfO_Counter1event0IDwr to CfO_Counter4event0IDwr (event function 1)
CfO_Counter1event1IDwr to CfO_Counter4event1IDwr (event function 2)

This register holds the event ID that should trigger the counter event function. For a list of all possible event IDs, see 4.11.17.12.6.1 "List of event IDs"

Data type	Value	Information
INT	192 to 7,489	ID of counter event function

Configure calculation of comparator

Name:
CfO_Counter1event0config to CfO_Counter4event0config (event function 1)
CfO_Counter1event1config to CfO_Counter4event1config (event function 2)

These registers are used to configure the counter event function for the respective counter function.

Bits 0 to 3 configure the calculation of the comparison or to latch the value. This calculation is similar to the calculation of the counter register (see 4.11.17.12.7.1 "Counter value calculation")

Bits 8 to 13 can be used to limit the number of bits used for the comparison. A mask is calculated as 2^n - 1 and linked with an "AND" operation. This makes it possible to generate a comparator pulse every 2^n increments.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	counter 1 - use	0	0 is added instead of "counter 1"
		1	"counter 1" is used for addition
1	counter 1 - sign	0	The sign of the "counter 1" register is not changed for addition
		1	The sign of the "counter 1" register is reversed for addition
2	counter 2 - use	0	0 is added instead of "counter 2"
		1	"counter 2" is used for addition
3	counter 1 - sign	0	The sign of the "counter 2" register is not changed for addition
		1	The sign of the "counter 2" register is reversed for addition
4 - 7	Reserved	-	
8 - 13	Number of bits for comparator mask	x	The mask value is calculated as 2^n-1, where n is value set in these bits. Default: 0
14	Reserved	-	
15	Margin comparator mode	0	MarginComparator >= (Current position - OriginComparator)
		1	MarginComparator > (Current position - OriginComparator)

Configure mode and latching of comparator function

Name:
CfO_Counter1event0mode to CfO_Counter4event0mode (event function 1)
CfO_Counter1event1mode to CfO_Counter4event1mode (event function 2)

In these registers you can set the mode for the comparator function and optional copying of the latched registers.

Comparator functions can be operated in 4 different modes. For a description, see "Comparator modes".

Bits 4 to 7 can be used to define hardware referencing actions.

Based on these bits, the values of the internal absolute value counters "abs1" and "abs2" can be copied to the respective "HW_reference_counter" register at every counter event (see 4.11.17.12.7.1 "Counter value calculation"). This function can be used to reference the counter values directly in the hardware.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Single
		2	State change
		3	Continuous
2 - 3	Reserved	-	
4	Copy abs1 counter value	0	No action
		1	When event is FALSE → hardware reference counter 1 = abs1
5	Copy abs2 counter value	0	No action
		1	When event is FALSE → hardware reference counter 2 = abs2
6	Copy abs1 counter value	0	No action
		1	When event is TRUE → hardware reference counter 1 = abs1
7	Copy abs2 counter value	0	No action
		1	When event is TRUE → hardware reference counter 2 = abs2

Comparator origin

Name:
OriginComparator01 to OriginComparator02 (ABR encoder)
OriginComparator01 and OriginComparator03 (AB encoder and up/down counter)

This register is available for the AB and ABR encoders and the up/down counters.

It defines the position value at which the respective configured comparator output channel is set.

Data type	Value	Information
INT	-32,768 to 32,767	Comparator window origin, 16-bit
DINT	-2,147,483,648 to 2,147,483,647	Comparator window origin, 32-bit

Width of the comparator

Name:
MarginComparator01 to MarginComparator02 (ABR encoder)
MarginComparator01 and MarginComparator03 (AB encoder and up/down counter)

This register is available for the AB and ABR encoders and the up/down counters.

It defines the width of the comparator window in the positive direction.

Data type	Value	Information
INT	-32,768 to 32,767	Width of comparator window, 16-bit
DINT	-2,147,483,648 to 2,147,483,647	Width of comparator window, 32-bit

Read latch position or counter value

Name:
Different names are used for these 4 registers depending on their function.

If the comparator returns "TRUE", then the current counter value is latched and copied to these registers. The calculation of the comparator value used for the latch can be configured in the "CfO_Counter[x]event[y]config" register.

Counter 1 - Latch 1		
Event function	**Function**	**Name**
1	**AB encoders**	Latch01AB01
	Up/down counters	Latch01Counter01
2	**AB encoders**	Latch02AB01
	ABR encoders	Latch01ABR01
	Up/down counters	Latch02Counter01

Counter 1 - Latch 2		
Event function	**Function**	**Name**
1	**AB encoders**	Latch01AB02
	Up/down counters	Latch01Counter02
2	**AB encoders**	Latch02AB02
	Up/down counters	Latch02Counter02

Counter 2 - Latch 1		
Event function	**Function**	**Name**
1	**AB encoders**	Latch01AB03
	Up/down counters	Latch01Counter03
2	**AB encoders**	Latch02AB03
	ABR encoders	Latch01ABR02
	Up/down counters	Latch02Counter03

Counter 2 - Latch 2		
Event function	**Function**	**Name**
1	**AB encoders**	Latch01AB04
	Up/down counters	Latch01Counter04
2	**AB encoders**	Latch02AB04
	Up/down counters	Latch02Counter04

Data type	Value	Information
INT	-32,768 to 32,767	Latched encoder position or counter value
DINT[1)]	-2,147,483,648 to 2,147,483,647	Latched encoder position or counter value

1) Only in function model 1

4.11.17.12.8 SSI encoder interface

The module has 2 SSI encoders available, supported directly in the hardware. Two 24 V output channels are set for each SSI encoder and cannot be changed. (See also 4.11.17.7.1 "Description of channel assignments")

When using the SSI encoder, the corresponding clock channel can be configured in the 4.11.17.12.5.1 "CfO_CFGchannel" register as "Channel-specific" and "Push/Pull".

Encoder	Data channel	Clock channel
SSI1	1	2
SSI2	5	6

4.11.17.12.8.1 SSI event functions

Each of the two SSI encoders consists of an event function and an event input. The SSI cycle is started when an event is received on this input.

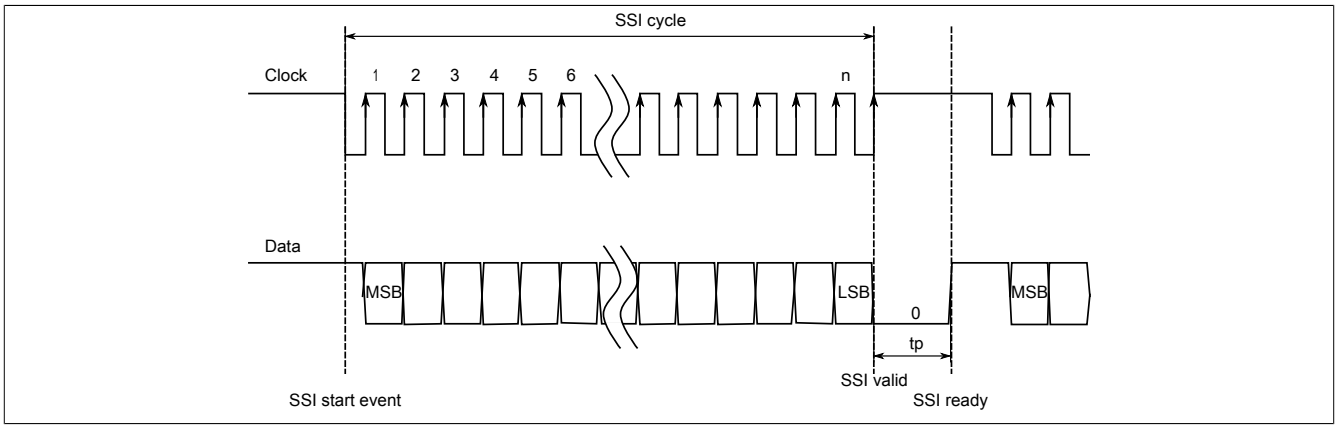
Information:

The SSI event function is not linked to an event by default, i.e. SSI functions are disabled.

Two events are sent from the SSI encoder interface..

- An "SSI valid" event is triggered immediately after the end of the SSI cycle if a new counter value is available.
- The "SSI ready" event then shows when the monoflop time has expired (tp in SSI encoder timing diagram). This is the earliest that the next SSI cycle can be started.

SSI encoder - Timing diagram



Configure event ID for SSI

Name:
CfO_SSI1event0IDwr to CfO_SSI2event0IDwr

This register holds the event ID that should start the SSI cycle. For a list of all possible event IDs, see 4.11.17.12.6.1 "List of event IDs"

Normally this register is set to network event 225 "AOSISOP"- This ensures that the new encoder position is available at the next "I/O → Synchronous Frame" transfer. Check the SSI transfer time and the X2X cycle time, because the SSI cycle must be completed within this time.

Data type	Value	Information
INT	192 to 7,233	ID of event function

Configure SSI

Name:
CfO_SSI1cfg to CfO_SSI2cfg

This configuration register is used to set the coding, the clock rate and the number of bits. Default = 0. This must be set once using an acyclic write command.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	00	1 MHz
		01	500 kHz
		10	250 kHz
		11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding

SSI advanced configuration

Name:
ConfigAdvanced01 to ConfigAdvanced02

This configuration register is used to set the coding, the clock rate, the number of bits and the monostable multivibrator settings. Default = 0. This must be set once using an acyclic write command.

It only differs from "CfO_SSI1cfg" by data length and additional monostable multivibrator testing.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	00	1 MHz
		01	500 kHz
		10	250 kHz
		11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary coding
		1	Gray coding
16 - 17	Monostable multivibrator check	00	Check OFF, no additional clock bit
		01	Check set to High level
		10	Check set to Low level
		11	Level is clocked but ignored
18 - 31	Reserved	0	

Enable SSI event function

Name:
CfO_SSI1control to CfO_SSI2control

The two SSI encoder events can be enabled/disabled using this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Event: SSI valid	0	Not sent
		1	Sent
1	Event: SSI ready	0	Not sent
		1	Sent
2 - 7	Reserved	-	

Read SSI position

Name:
SSIEncoder01 to SSIEncoder02

The last transferred SSI position can be read out from this register. The SSI encoder value is displayed as a 32-bit position value. This position value is generated synchronously with the X2X cycle.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Last SSI position transferred

4.11.17.12.8.2 SSI comparator condition

The module has an assigned comparator function for the SSI function. These consist of:

- Event ID that triggers the comparator function
- The window comparator
- Latch register for saving the counter value

When the comparator function is complete, event ID 7232 to7489 (see 4.11.17.12.6.1 "List of event IDs") is sent.

Configure event ID for SSI comparator

Name:
CfO_SSI1eventIDwr to CfO_SSI2eventIDwr

This register holds the event ID that should start the SSI comparator function. For a list of all possible event IDs, see 4.11.17.12.6.1 "List of event IDs"

Data type	Value	Information
INT	192 to 7,233	ID of comparator function

Configure the mode of the SSI comparator function

Name:
CfO_SSI1event0mode to CfO_SSI2event0mode

This register can be used to configure the mode of the comparator function.

Comparator functions can be operated in 4 different modes. For a description, see "Comparator modes".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Single
		2	State change
		3	Continuous
2 - 7	Reserved	-	

Configure calculation of SSI comparator

Name:
CfO_SSI1event0config and CfO_SSI2event0config

The calculation of the position value used for the comparator can be configured in this register.

The window comparator condition is calculated as follows:

```
counter_window_value = ssi_counter & (2^ssi_data_bits - 1)
diff = counter_window_value – origin_comparator
if ((diff & (2^(comparator_mask)-1)) <= margin_comparator)
condition = True;
else
condition = False;
```

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 5	SSI data bits	x	Number of data bits used for masking
6 - 7	Reserved	-	
8 - 13	Comparator mask	x	The mask value is calculated from 2^n-1, where n is the value configured in SSI data bits. Default: 0
14	Comparator mode	0	MarginComparator >= SSI position - OriginComparator
		1	MarginComparator > SSI position - OriginComparator

Origin of the SSI comparator

Name:
OriginComparator01_SSI to OriginComparator02_SSI

This register contains the origin of the window comparator.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Origin of the window comparator.

Width of the SSI comparator

Name:
MarginComparator01_SSI to MarginComparator02_SSI

This register provides the width of the window comparator.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Width of the SSI window comparator

Read SSI latch position

Name:
Latch01SSI01 to Latch01SSI02

If the SSI window comparator returns "True", then the current SSI position is latched and saved in this register.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Latched SSI position

4.11.17.12.9 PWM - Pulse width modulation

The module has 4 PWM functions available, supported directly by the hardware. A 24 V output channel is set for each PWM encoder and cannot be changed. (See also 4.11.17.7.1 "Description of channel assignments")

When using the PWM function, the corresponding channel can be configured in the 4.11.17.12.5.1 "CfO_CFGchannel" register as "Channel-specific".

PWM function	Channel
PWM1	2
PWM2	4
PWM3	6
PWM4	8

4.11.17.12.9.1 Configure PWM prescaler

Name:
CfO_PWM0prescaler to CfO_PWM3prescaler

The length of the PWM cycle is configured using this register. The base is a 48 MHz clock, which can be changed (divided) using the setting in this register. One PWM cycle consists of 1,000 of the resulting clocks after they have been divided. The period length of the PWM cycle is calculated as follows:

$$PWM\_cycle = 1000 \frac{prescale}{48000000} [s]$$

Data type	Value	Information
UINT	2 to 65,535	Prescaler for PWM cycle

4.11.17.12.9.2 Output PWM values

Name:
PWMOutput02, PWMOutput04, PWMOutput06, PWMOutput08

In this register, a configuration is made for the percentage of the PWM cycle (in 1/10 % steps) that the PWM output is logical 1, i.e. ON.

Data type	Value	Information
UINT	0 to 1,000	PWM output always off
	2 to 999	Turn on time in 1/10% steps
	1,000	PWM output always on

4.11.17.12.10 Time measurement function

The module has a time measurement function for each I/O channel. It can be configured separately for rising and falling edges on each channel.
A starting edge can be configured for each time measurement function. When a configured starting edge occurs, the value of the internal timer is saved in a FIFO. This FIFO holds up to 16 elements. When the actual trigger edge occurs, the difference in time between the starting edge and the triggered edge is copied to the respective register.
Bits 8 to 11 "Previous start edge" of the 4.11.17.12.10.2 "CfO_EdgeTimeFallingMode" and 4.11.17.12.10.3 "CfO_EdgeTimeRisingMode" registers can be used to define which detected starting edge from the FIFO should be used to calculate the difference. Additionally, when the trigger edge occurs, the counter clocked internally using bits 12 to 15 "Time measurement resolution are copied to the 4.11.17.12.10.10 "TimeStampFallingCH" and 4.11.17.12.10.11 "TimeStampRisingCH" registers.

Information:

The time measurement function is an extension of edge detection, so all of the channels used must be configured there.

4.11.17.12.10.1 Enable time measurement function

Name:
CfO_EdgeTimeglobalenable

This register enables/disables the time measurement function for the entire module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Time measurement function	0	Disabled for entire module
		1	Enabled for entire module
1 - 7	Reserved	-	

4.11.17.12.10.2 Configure time measurement function for the falling edge

Name:
CfO_EdgeTimeFallingMode01 to CfO_EdgeTimeFallingMode08

These registers can be used to configure the time measurement function for the falling edge of the respective channel.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Selects the channel for the starting edge	0	Channel 1
		...	
		7	Channel 8
4	Selects the edge for the starting edge	0	The falling edge of the channel configured in bits 0 to 3 serves as the starting edge.
		1	The rising edge of the channel configured in bits 0 to 3 serves as the starting edge.
5 - 6	Reserved	-	
7	Trigger	0	Triggered[1)]
		1	Continuous[2)]
8 - 11	Previous start edge	0 to 15	The value determines which entry in the starting edge FIFO should be used to calculate the time difference.
12 - 15	Time measurement resolution	0	8 Mhz
		1	4 Mhz
		2	2 Mhz
		3	1 Mhz
		4	500 kHz
		5	250 kHz
		6	125 kHz
		7	625 kHz

1) The time measurement is triggered by the corresponding bit in the 4.11.17.12.10.5 "TriggerRisingCH" register.
2) Time measurement runs continuously and is triggered at every edge.

4.11.17.12.10.3 Configure time measurement function for the rising edge

Name:
CfO_EdgeTimeRisingMode01 to CfO_EdgeTimeRisingMode08

These registers can be used to configure the time measurement function for the rising edge of the respective channel.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Selects the channel for the starting edge	0	Channel 1
		...	
		7	Channel 8
4	Selects the edge for the starting edge	0	The falling edge of the channel configured in bits 0 to 3 serves as the starting edge.
		1	The rising edge of the channel configured in bits 0 to 3 serves as the starting edge.
5 - 6	Reserved	-	
7	Trigger	0	Triggered[1)]
		1	Continuous[2)]
8 - 11	Previous start edge	0 to 15	The value determines which entry in the starting edge FIFO should be used to calculate the time difference.
12 - 15	Time measurement resolution	0	8 Mhz
		1	4 Mhz
		2	2 Mhz
		3	1 Mhz
		4	500 kHz
		5	250 kHz
		6	125 kHz
		7	625 kHz

1) The time measurement is triggered by the corresponding bit in the 4.11.17.12.10.5 "TriggerRisingCH" register.
2) Time measurement runs continuously and is triggered at every edge.

4.11.17.12.10.4 Trigger falling edge detection

Name:
TriggerFallingCH01 to TriggerFallingCH08

If bit 7 "Trigger" is cleared in the 4.11.17.12.10.2 "CfO_EdgeTimeFallingMode" register, then detection of a falling edge on the respective input can be triggered using the respective bit in this register. After a bit has been set, the next falling edge on the corresponding channel is detected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TriggerFallingCH01	0	Falling edges on channel 1 are not detected
		1	The next falling edge on channel 1 will be detected
...		...	
7	TriggerFallingCH08	0	Falling edges on channel 8 are not detected
		1	The next falling edge on channel 8 will be detected

4.11.17.12.10.5 Trigger rising edge detection

Name:
TriggerRisingCH01 to TriggerRisingCH08

If the "Continued/triggered" bit is cleared in the 4.11.17.12.10.3 "CfO_EdgeTimeRisingMode" register, then detection of a rising edge on the respective input can be triggered using the respective bit in this register. After a bit has been set, the next rising edge on the corresponding channel is detected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Trigger rising edge - Channel 1	0	Rising edges on channel 1 are not detected
		1	The next rising edge on channel 1 will be detected
...		-	
7	Trigger rising edge - Channel 8	0	Rising edges on channel 8 are not detected
		1	The next rising edge on channel 8 will be detected

4.11.17.12.10.6 Show first falling trigger edge

Name:
BusyTriggerFallingCH01 to BusyTriggerFallingCH08

If edges are triggered via the bits in the 4.11.17.12.10.4 "TriggerFallingCH" register, then a set bit in this register indicates that no falling edges have been detected on the respective channel since the corresponding bit was set in the "TriggerFallingCH" register. If a falling edge occurs on the respective channel, then the corresponding BusyTriggerFalling bit is cleared.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	BusyTriggerFallingCH01	0	Falling edge detected on channel 1
		1	Module waiting for a falling edge on channel 1
...		...	
7	BusyTriggerFallingCH08	0	Falling edge detected on channel 8
		1	Module waiting for a falling edge on channel 8

4.11.17.12.10.7 Show first rising trigger edge

Name:
BusyTriggerRisingCH01 to BusyTriggerRisingCH08

If edges are triggered via the bits in the 4.11.17.12.10.5 "TriggerRisingCH" register, then a set bit in this register indicates that no rising edges have been detected on the respective channel since the corresponding bit was set in the "TriggerRisingCH" register. If a rising edge occurs on the respective channel, then the corresponding BusyTriggerRising bit is cleared.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	BusyTriggerRisingCH01	0	Rising edge detected on channel 1
		1	Module waiting for a rising edge on channel 1
...		...	
7	BusyTriggerRisingCH08	0	Rising edge detected on channel 8
		1	Module waiting for a rising edge on channel 8

4.11.17.12.10.8 Count falling trigger edges

Name:
CountFallingCH01 to CountFallingCH08

These registers contain cyclic counters that are incremented with every detected falling edge on the respective channel.

Data type	Value	Information
USINT	0 to 255	Counter for falling edges

4.11.17.12.10.9 Count rising trigger edges

Name:
CountRisingCH01 to CountRisingCH08

These registers contain cyclic counters that are incremented with every detected rising edge on the respective channel.

Data type	Value	Information
USINT	0 to 255	Counter for rising edges

4.11.17.12.10.10 Time stamp of falling edge

Name:
TimeStampFallingCH01 to TimeStampFallingCH08

When a falling edge occurs on the respective channel, the current counter value of the module timer is copied to these registers.

Data type	Value	Information
UINT	0 to 65,535	Time stamp for rising edges

4.11.17.12.10.11 Time stamp of the rising edge

Name:
TimeStampRisingCH01 to TimeStampRisingCH08

When a rising edge occurs on the respective channel, the current counter value of the module timer is copied to these registers.

Data type	Value	Information
UINT	0 to 65,535	Time stamp for rising edges

4.11.17.12.10.12 Time difference of falling edge

Name:
TimeDiffFallingCH01 to TimeDiffFallingCH08

When a falling edge occurs on the respective channel, the time difference compared to the starting edge configured in bit 4 of the 4.11.17.12.10.2 "CfO_EdgeTimeFallingMode" register is copied to this register.

Data type	Value	Information
UINT	0 to 65,535	Time difference from starting edge

4.11.17.12.10.13 Time difference of rising edge

Name:
TimeD-iffRisingCH01 to TimeDiffRisingCH08

When a rising edge occurs on the respective channel, the time difference compared to the starting edge configured in bit 4 of the 4.11.17.12.10.3 "CfO_EdgeTimeRisingMode" register is copied to this register.

Data type	Value	Information
UINT	0 to 65,535	Time difference from starting edge

4.11.17.12.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

4.11.17.12.12 Maximum cycle time

The maximum cycle time defines how far the bus cycle can be increased without internal counter overflows causing module malfunctions.

Minimum cycle time
16 ms

4.11.17.12.13 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
128 µs

4.12 CPUs

The X20 CPUs are a powerful addition to the X20 system. With the exception of the entry level model, all CPUs are based on Intel ATOM™ processors, which are available in various performance classes. Each CPU is available with either one or three slots for interface modules.

Flexible communication options onboard

In addition to one CompactFlash, two USB and two RS232 interfaces, there are also two independent Ethernet interfaces. One of them is a standard gigabit Ethernet interface for TCP/IP data traffic.

Behind the second female RJ45 connector, there is a pure Fast Ethernet interface (100 Mbit/s) that serves as a POWERLINK interface. This means that no additional POWERLINK interface is needed to operate a POWERLINK network.

Easy maintenance

A special feature of the CPU modules is that they are operated fan-free. The CPU can be operated throughout the full temperature range of the X20 system (-25 to 60°C). Depending on the model, derating may be required over 55°C.

The built-in SRAM buffer battery can be exchanged during operation as long as local regulations allow it. When the battery is exchanged with the power off, the SRAM is buffered for approximately 1 minute. This makes maintenance work very simple.

4.12.1 Brief information

Product ID	Short description	on page
X20CP1301	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 1 GB flash drive onboard, 1 insert slot for X20 interface modules, 1 USB interface, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including power supply module, 3x X20TB1F terminal blocks, slot cover and X20 locking plate X20AC0SR1 (right) included	1112
X20CP1381	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included	1112
X20CP1382	X20 CPU, with integrated I/O, x86-400, 256 MB DDR3 RAM, 32 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included	1112
X20CP1483	X20 CPU, x86 100 MHz Intel compatible, 32 MB DRAM, 128 kB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1168
X20CP1483-1	X20 CPU, x86 100 MHz Intel compatible, 64 MB DRAM, 128 kB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1168
X20CP1583	X20 CPU, ATOM 333 MHz compatible, 128 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1185
X20CP1584	X20 CPU, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1185
X20CP1585	X20 CPU, ATOM 1.0 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1185
X20CP1586	X20 CPU, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1185
X20CP3583	X20 CPU, ATOM 333 MHz compatible, 128 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1189
X20CP3584	X20 CPU, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.	1189
X20CP3585	X20 CPU, ATOM 1.0 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.	1189
X20CP3586	X20 CPU, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.	1189
X20cCP1584	X20 CPU, coated, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1185
X20cCP1586	X20 CPU, coated, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1185
X20cCP3584	X20 CPU, coated, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1189
X20cCP3586	X20 CPU, coated, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.	1189

4.12.2 X20CP1301, X20CP1381 and X20CP1382

4.12.2.1 General information

Compact CPUs are available with processor speeds of 200 MHz and 400 MHz. Depending on the variant, up to 256 MB RAM and up to 32 kB nonvolatile onboard RAM is available. A built-in flash drive is available to store up to 2 GB of application and other data.

All CPUs come equipped with Ethernet, USB and one RS232 interface. In both performance classes, integrated POWERLINK and CAN bus interfaces are also available. If additional fieldbus connections are needed, all CPUs can be upgraded with an interface module from the standard X20 product range. These CPUs do not require fans or batteries and are therefore maintenance-free. 30 different digital inputs and outputs and two analog inputs are integrated in the devices. One analog input can be used for PT1000 resistance temperature measurement.

- CPU is Intel® ATOM™ 400 MHz compatible with integrated I/O processor
- Ethernet, POWERLINK with poll-response chaining and USB onboard
- 1 slot for modular interface expansion
- 30 digital inputs/outputs and two analog inputs integrated in the device
- 1/2 GB flash drive onboard
- 128/256 MB DDR3 SDRAM
- Fanless
- No battery
- Battery-backed real-time clock

4.12.2.2 Order data

Model number	Short description
	X20 CPUs
X20CP1301	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 1 GB flash drive onboard, 1 insert slot for X20 interface modules, 1 USB interface, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including power supply module, 3x X20TB1F terminal blocks, slot cover and X20 locking plate X20AC0SR1 (right) included
X20CP1381	X20 CPU, with integrated I/O, x86-200, 128 MB DDR3 RAM, 16 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included
X20CP1382	X20 CPU, with integrated I/O, x86-400, 256 MB DDR3 RAM, 32 kB FRAM, 2 GB flash drive on board, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 CAN bus interface, 1 POWERLINK interface, 1 Ethernet interface 10/100 Base-T, 14 digital inputs, 24 VDC, sink, 4 digital inputs, 2 µs, 24 VDC, sink, 4 digital outputs, 24 VDC, 0.5 A, source, 4 digital outputs, 2 µs, 24 VDC, 0.2 A, 4 digital inputs/outputs, 24 VDC, 0.5 A, 2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA, 1 PT1000 instead of an analog input, including supply module, 3x X20TB1F terminal blocks, slot cover and X20AC0SR1 locking plate (right) included

Table 202: Order data

Content of delivery

Model number	Quantity	Short description
-	1	Interface module slot cover
X20AC0SR1	1	X20 locking plate, right
X20TB1F	3	X20 terminal block, 16-pin, 24 VDC keyed

Table 203: Content of delivery

4.12.2.3 Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
Short description			
Interfaces	1x RS232, 1x Ethernet, 1x USB, 1x X2X Link	1x RS232, 1x Ethernet, 1x POWERLINK, 2x USB, 1x X2X Link, 1x CAN bus	
System module	CPU		
General information			
Cooling	Fanless		
B&R ID code	0xE35B	0xE35C	0xDABB
Status indicators	CPU function, Ethernet, RS232, CPU supply, I/O supply, I/O function per channel	CPU function, Ethernet, POWERLINK, RS232, CAN bus, CAN bus terminating resistor, CPU supply, I/O supply, I/O function per channel	
Diagnostics			
Outputs	Digital outputs: Yes, using status LED and software (output error status)		
CPU function	Yes, using status LED		
CAN bus data transfer	-	Yes, using status LED	
RS232 data transfer	Yes, using status LED		
Inputs	Analog inputs: Yes, using status LED and software		
Ethernet	Yes, using status LED		
I/O supply	Yes, using status LED		
POWERLINK	-	Yes, using status LED	
Supply voltage monitoring	Yes, using status LED		
Overtemperature	Yes, using software		
Terminating resistor	-	Yes, using status LED	
CPU redundancy possible	No		
ACOPOS capability	Yes		
reACTION-capable I/O channels	No		
Visual Components support	Yes		
Power consumption without interface module and USB	4.3 W	4.8 W	5.5 W
Internal power consumption of the X2X Link and I/O supply [1]			
Bus	0.8 W		
Internal I/O	0.8 W		
Additional power dissipation caused by the actuators (resistive) [W]	-		
Electrical isolation			
Power supply			
I/O feed - I/O supply	No		
CPU/X2X Link feed - CPU/IF6	Yes		
IF1 - IF2	Yes		
IF1 - IF3	-	Yes	
IF1 - IF4	No		
IF1 - IF5	-	No	
IF1 - IF6	Yes		
IF1 - IF7	-	No	
IF2 - IF3	-	Yes	
IF2 - IF4	Yes		
IF2 - IF5	-	Yes	
IF2 - IF6	Yes		
IF2 - IF7	-	Yes	
IF3 - IF4	-	Yes	
IF3 - IF5	-	Yes	
IF3 - IF6	-	Yes	
IF3 - IF7	-	Yes	
IF4 - IF5	-	No	
IF4 - IF6	Yes		
IF4 - IF7	-	No	
IF5 - IF6	-	Yes	
IF5 - IF7	-	No	
IF6 - IF7	-	Yes	
Channel - Bus	Yes		
Channel - Channel	No		
Channel - PLC	No		
PLC - IF1 (RS232)	No		
PLC - IF2 (Ethernet)	Yes		
PLC - IF3 (POWERLINK)	-	Yes	
PLC - IF4 (USB)	No		
PLC - IF5 (USB)	-	No	
PLC - IF6 (X2X Link)	Yes		
PLC - IF7 (CAN bus)	-	No	
Type of signal lines [2]	Shielded cables must be used for all fast digital inputs/outputs, cable length: max. 20 m		

Table 204: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
Certification			
CE		Yes	
cULus		Yes	
ATEX Zone 2 [3]		Yes	
GOST-R		Yes	
CPU and X2X Link supply			
Input voltage		24 VDC -15 % / +20 %	
Input current		Max. 1 A	
Fuse		Integrated, cannot be replaced	
Reverse polarity protection		Yes	
X2X Link supply output			
Nominal output power		2 W	
Parallel operation		Yes [4]	
Redundant operation		Yes [5]	
Input I/O supply			
Input voltage		24 VDC -15 % / +20 %	
Fuse		Required line fuse: Max. 10 A, slow-blow	
Output I/O supply			
Rated output voltage		24 VDC	
Permitted contact load		10 A	
Controller			
Real-time clock		Buffering for at least 300 hours at 25°C, 1 s resolution, -18 to 28 ppm accuracy at 25°C	
FPU		Yes	
Processor			
Type		Vx86EX	
Clock frequency	200 MHz		400 MHz
L1 cache			
Data code		16 kB	
Program code		16 kB	
L2 cache		128 kB	
Integrated I/O processor		Processes I/O data points in the background	
Modular interface slots		1	
Remanent variables	16 kB FRAM, buffering >10 years [6]		32 kB FRAM, buffering >10 years [6]
Shortest task class cycle time	2 ms		1 ms
Typical instruction cycle time	0.0419 µs		0.0199 µs
Standard memory			
RAM	128 MB DDR3 SDRAM		256 MB DDR3 SDRAM
Program memory			
Type	1 GB eMMC flash memory		2 GB eMMC flash memory
Data retention		10 years	
Writable data amount			
Guaranteed		40 TB	
Results for 5 years		21.9 GB/day	
Guaranteed clear/write cycles		20,000	
Error correction coding (ECC)		Yes	
Interfaces			
IF1 interface			
Signal		RS232	
Design		Connection made using 16-pin X20TB1F terminal block	
Max. distance		900 m	
Transfer rate		Max. 115.2 kbit/s	
IF2 interface			
Signal		Ethernet	
Design		1x RJ45 shielded	
Cable length		Max. 100 m between 2 stations (segment length)	
Transfer rate		10/100 Mbit/s	
Transmission			
Physical layer		10BASE-T / 100BASE-TX	
Half-duplex		Yes	
Full-duplex		Yes	
Autonegotiation		Yes	
Auto-MDI / MDIX		Yes	
IF3 interface			
Fieldbus	-	POWERLINK managing or controlled node	
Type	-	Type 4 [7]	
Design	-	1x RJ45 shielded	
Cable length	-	Max. 100 m between 2 stations (segment length)	
Transfer rate	-	100 Mbit/s	
Transmission			
Physical layer	-	100BASE-TX	
Half-duplex	-	Yes	
Full-duplex	-	No	
Autonegotiation	-	Yes	
Auto-MDI / MDIX	-	Yes	

Table 204: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
IF4 interface			
Type		USB 1.1/2.0	
Design		Type A	
Max. output current		0.5 A	
IF5 interface			
Type	-	USB 1.1/2.0	
Design	-	Type A	
Max. output current	-	0.1 A	
IF6 interface			
Fieldbus		X2X Link master	
IF7 interface			
Signal	-	CAN bus	
Design	-	Connection made using 16-pin X20TB1F terminal block	
Max. distance	-	1000 m	
Transfer rate	-	Max. 1 Mbit/s	
Terminating resistor	-	Integrated in the module	
Controller	-	SJA 1000	
Digital inputs			
Quantity	14 standard inputs, 4 high-speed inputs and 4 mixed channels, configurable as inputs or outputs using software		
Nominal voltage	24 VDC		
Input voltage	24 VDC -15 % / +20 %		
Input current at 24 VDC	X1 - Standard inputs: Typ. 3.5 mA X2 - Standard inputs: Typ. 2.68 mA X2 - High-speed inputs: Typ. 3.5 mA X3 - Mixed channels: Typ. 2.68 mA		
Input filter			
Hardware	Standard inputs and mixed channels: ≤200 µs High-speed inputs: ≤2 µs, when used as standard inputs: ≤200 µs		
Software	Default 1 ms, configurable between 0 and 25 ms in 0.1 ms intervals		
Connection type	1-wire connections		
Input circuit	Sink		
Additional functions	X2 - High-speed digital inputs: 2x 250 kHz event counting, 2x AB counter, ABR incremental encoder, direction/frequency, period measurement, gate measurement, differential time measurement, edge counters, edge times		
Input resistance	X1 - Standard inputs: 6.8 kΩ X2 - Standard inputs: 8.9 kΩ X2 - High-speed inputs: 6.8 kΩ X3 - Mixed channels: 8.9 kΩ		
Switching threshold			
Low	<5 VDC		
High	>15 VDC		
AB incremental encoder			
Quantity	2		
Encoder inputs	24 V, asymmetrical		
Counter size	32-bit		
Input frequency	Max. 100 kHz		
Evaluation	4x		
Encoder supply	Module-internal, max. 300 mA		
Overload behavior of the encoder supply	Short circuit protection, overload protection		
ABR incremental encoder			
Quantity	1		
Encoder inputs	24 V, asymmetrical		
Counter size	32-bit		
Input frequency	Max. 100 kHz		
Evaluation	4x		
Encoder supply	Module-internal, max. 300 mA		
Overload behavior of the encoder supply	Short circuit protection, overload protection		
Event counter			
Quantity	2		
Signal form	Square wave pulse		
Evaluation	1x		
Input frequency	Max. 250 kHz		
Counter frequency	250 kHz		
Counter size	32-bit		
Time measurement			
Possible measurements	Period measurement, gate measurement, differential time measurement, edge counter, edge times		
Measurements per module	Each function up to 4x		
Counter size	32-bit		
Timestamp	1 µs resolution		
Signal form	Square wave pulse		
Analog inputs			
Quantity	2 [8)]		
Input	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections		
Input type	Differential input		

Table 204: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
Digital converter resolution			
Voltage	±12-bit		
Current	12-bit		
Conversion time	1 channel enabled: 100 µs 2 channels enabled: 200 µs		
Output format			
Data type	INT		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV		
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA		
Input impedance in signal range			
Voltage	20 MΩ		
Current	-		
Load			
Voltage	-		
Current	<300 Ω		
Input protection	Protection against wiring with supply voltage		
Permitted input signal			
Voltage	Max. ±30 V		
Current	Max. ±50 mA		
Output of the digital value during overload	Configurable		
Conversion procedure	SAR		
Input filter	3rd-order low pass / cutoff frequency 1 kHz		
Max. error at 25°C			
Voltage			
Gain	0.18% (Rev. <C0: 0.37%) [9]		
Offset	0.04% (Rev. <C0: 0.25%) [10]		
Current			
Gain	0 to 20 mA = 0.15% (Rev. <C0: 0.52%) / 4 to 20 mA = 0.25% [9]		
Offset	0 to 20 mA = 0.1% (Rev. <C0: 0.4%) / 4 to 20 mA = 0.15% [11]		
Max. gain drift			
Voltage	0.017 %/°C [9]		
Current	0 to 20 mA = 0.015 %/°C / 4 to 20 mA = 0.023 %/°C [9]		
Max. offset drift			
Voltage	0.008 %/°C [10]		
Current	0 to 20 mA = 0.008 %/°C / 4 to 20 mA = 0.012 %/°C [11]		
Common-mode rejection			
DC	70 dB		
50 Hz	70 dB		
Common-mode range	±12 V		
Crosstalk between channels	<-70 dB		
Nonlinearity			
Voltage	<0.025% [10]		
Current	<0.05% [11]		
Temperature inputs resistance measurement			
Quantity	1		
Input	Resistance measurement with constant current supply for 2-wire connections		
Digital converter resolution	13-bit		
Conversion time	Only temperature input enabled: 200 µs Temperature and analog input enabled: 400 µs		
Conversion procedure	SAR		
Output format	INT or UINT for resistance measurement		
Sensor			
PT1000	-200 to 850°C		
Resistance measurement range	0.1 to 4000 Ω		
Temperature sensor resolution	1 LSB = 0x0005 = 0.16°C		
Resistance measurement resolution	1 LSB = 0x0005 = 0.49 Ω		
Input filter	1st-order low pass / cutoff frequency 7 Hz		
Sensor standard	IEC/EN 60751		
Common-mode range	1 V		
Linearization method	Internal		
Measuring current	1 mA		
Permitted input signal	Short-term max. ±30 V		
Max. error at 25°C			
Gain	0.3% (Rev. <C0: 1.93%) [12]		
Offset	0.15% (Rev. <C0: 0.32%) [13]		
Max. gain drift	0.023 %/°C [12]		
Max. offset drift	0.012 %/°C [13]		
Nonlinearity	<0.05% [13]		
Standardized value range for resistance measurement	0.1 Ω to 4000 Ω	0.1 Ω to 4000.0 Ω	0.1 Ω to 4000 Ω
Crosstalk between channels	<-70 dB		
Common-mode rejection			
50 Hz	>60 dB		

Table 204: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
Temperature sensor standardization			
PT1000	-200 to 850°C		
Digital outputs			
Design	Standard outputs and mixed channels: FET positive switching High-speed outputs: Push-Pull		
Quantity	4 standard outputs, 4 high-speed outputs and 4 mixed channels, configurable as inputs or outputs using software		
Nominal voltage	24 VDC		
Switching voltage	24 VDC -15 % / +20 %		
Nominal output current	Standard outputs and mixed channels: 0.5 A High-speed outputs: 0.2 A		
Total nominal current	Standard outputs and mixed channels: 4 A High-speed outputs: 0.8 A		
Connection type	1-wire connections		
Output circuit	Standard outputs and mixed channels: Source High-speed outputs: Sink or source		
Output protection [14]	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")		
Pulse width modulation [15]			
Period duration	5 to 65535 µs corresponds to 200 kHz to 15 Hz		
Pulse duration	0.0 to 100.0%, minimum 2.5 µs		
Resolution for pulse duration	0.1% of the configured frequency		
Diagnostic status	Standard outputs and mixed channels: Output monitoring with 10 ms delay High-speed outputs: Output monitoring with 10 µs delay		
Leakage current when switched off	Standard outputs and mixed channels: 5 µA High-speed outputs: 25 µA		
$R_{DS(on)}$	140 mΩ [16]		
Residual voltage	Standard outputs and mixed channels: <0.1 V at 0.5 A rated current High-speed outputs: <0.9 V at 0.1 A rated current		
Peak short circuit current	Standard outputs and mixed channels: <3 A High-speed outputs: <20 A		
Switching on after overload or short circuit cutoff	Standard outputs and mixed channels: Approx. 10 ms (depends on the module temperature) High-speed outputs: No switch on		
Switching delay			
0 -> 1	Standard outputs and mixed channels: <300 µs High-speed outputs: <3 µs		
1 -> 0	Standard outputs and mixed channels: <300 µs High-speed outputs: <3 µs		
Switching frequency			
Resistive load [17]	Standard outputs and mixed channels: Max. 500 Hz High-speed outputs: 50 kHz, max. 200 kHz (see section "Switching frequency derating for high-speed digital outputs")		
Inductive load	See section "Switching inductive loads"		
Braking voltage when switching off inductive loads	Standard outputs and mixed channels: Typ. 45 VDC		
Operating conditions			
Mounting orientation			
Horizontal	Yes		
Vertical	Yes		
Installation at elevations above sea level			
0 to 2000 m	No limitations		
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m		
EN 60529 protection	IP20		
Environmental conditions			
Temperature			
Operation			
Horizontal installation	-25 to 60°C		-25 to 60°C (Rev. <D0: -25 to 55°C)
Vertical installation	-25 to 50°C		
Derating	See section "Switching frequency derating for high-speed digital outputs".		
Storage	-40 to 85°C		
Transport	-40 to 85°C		
Relative humidity			
Operation	5 to 95%, non-condensing		
Storage	5 to 95%, non-condensing		
Transport	5 to 95%, non-condensing		
Mechanical characteristics			
Note	X20 locking plate (right) included in delivery 3 X20 terminal blocks (16-pin) included in delivery Interface module slot cover included in delivery		

Table 204: Technical data

Product ID	X20CP1301	X20CP1381	X20CP1382
Dimensions			
Width		164 mm	
Height		99 mm	
Depth		75 mm	
Weight	300 g	310 g	

Table 204: Technical data

1) The specified values are maximum values. The exact calculation is available with the other module documentation for download from the B&R website.
2) See section "X20 shielding brackets".
3) Ta min.: 0°C
   Ta max.: See environmental conditions
4) When operated in parallel, the nominal power of 2 W is not permitted to be added to the total power.
5) Up to 2 W bus load.
6) Can be set in Automation Studio.
7) See the POWERLINK section of the AS help system under "General information, Hardware - IF/LS".
8) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
9) Based on the current measured value.
10) Based on the 20 V measurement range.
11) Based on the 20 mA measurement range.
12) Based on the current resistance value.
13) Based on the entire resistance measurement range.
14) For high-speed digital outputs, derating must be applied at switching frequencies >50 kHz (see section "Switching frequency derating for high-speed digital outputs"). Overtemperature protection is not provided.
15) The high-speed digital outputs can be used for pulse width modulation.
16) Only for standard outputs and mixed channels.
17) Standard outputs and mixed channels: At loads ≤1 kΩ.

4.12.2.4 LED status indicators on the integrated X1 I/O slot

Figure	LED	Color	Status	Description
	E	Red	On	SERVICE mode
			Blinking	The "E" LED blinks red and the "RF" LED blinks yellow when there is a license violation.
			Double flash	BOOT mode (during firmware update)[1)]
	R	Green	On	Application running
			Blinking	Boot mode system start: CPU initializing the application, all bus systems and I/O modules[1)]
		Red	On	Reset in progress
	RF	Yellow	On	SERVICE or BOOT mode
			Blinking	The "RF" LED blinks yellow and the "E" LED blinks red when there is a license violation.
	SE	Green/Red		Status/Error LED. The statuses of this LED are described in section 4.12.2.4.1 ""S/E" LED".
	ET	Green	On	A link to the peer station has been established.
			Blinking	A link to the peer station has been established. The LED blinks when Ethernet activity is taking place on the bus.
	PL	Green	On	A link to the POWERLINK peer station has been established.
			Blinking	A link to the POWERLINK peer station has been established. The LED blinks when Ethernet activity is taking place on the bus.
	A1 - A2	Green	Off	Open line or disconnected sensor
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK
	1 - 4	Green		Input state of the corresponding digital input
	C	Yellow	On	CPU transmitting or receiving data via the CAN bus interface
	S	Yellow	On	CPU transmitting or receiving data via the RS232 interface
	T	Yellow	On	The terminating resistor integrated in the CPU is switched on.
	DC	Yellow	On	CPU power supply OK

Table 205: LED status indicators on the integrated X1 I/O slot

1) The process can take several minutes depending on the configuration.

4.12.2.4.1 "S/E" LED

The Status/Error LED is a green/red dual LED. The LED status can have different meanings depending on the operating mode.

4.12.2.4.1.1 Ethernet mode

In this mode, the interface is operated as an Ethernet interface.

Green - Status	Description
On	Interface being operated as an Ethernet interface

Table 206: Status/Error LED - Ethernet operating mode

4.12.2.4.1.2 POWERLINK

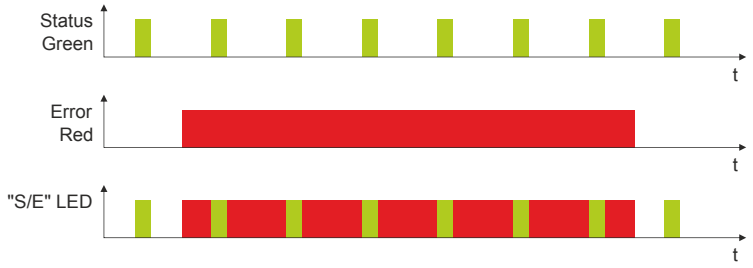
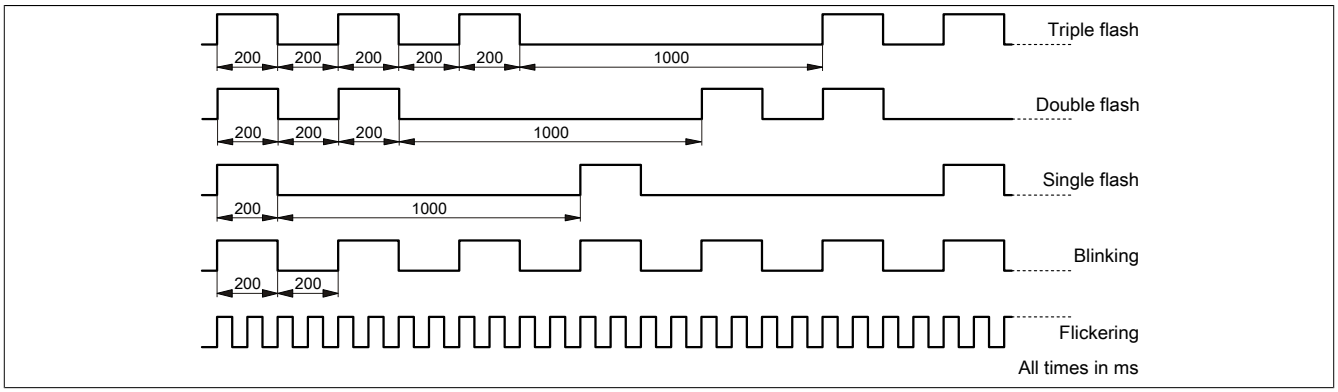
Red - Error	Description
On	The module is in an error mode (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: The LED blinks red several times immediately after startup. This is not an error.

Table 207: Status/Error LED as Error LED - POWERLINK operating mode

Green - Status	Description
Off	**Mode** The module is in NOT_ACTIVE mode or: • Switched off • Starting up • Not configured correctly in Automation Studio • Defective **Managing node (MN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to PRE_OPERATIONAL_1 mode. If POWERLINK communication is detected before the time expires, however, then the MN will not be started. **Controlled node (CN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to BASIC_ETHERNET mode. If POWERLINK communication is detected before this time expires, however, the module switches immediately to PRE_OPERATIONAL_1 mode.
Green flickering (approx. 10 Hz)	**Mode** The module is in BASIC_ETHERNET mode. The interface is being operated as an Ethernet TCP/IP interface. **Managing node (MN)** This state can only be changed by resetting the module. **Controlled node (CN)** If POWERLINK communication is detected while in this state, the module will transition to the PRE_OPERATIONAL_1 state.
Single flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_1 mode. **Managing node (MN)** The MN starts "reduced cycle" operation. Cyclic communication is not yet taking place. **Controlled node (CN)** The module can be configured by the MN in this state. The CN waits until it receives an SoC frame and then switches to the PRE_OPERATIONAL_2 mode. An LED lit red in this state indicates failure of the MN.
Double flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_2 mode. **Managing node (MN)** The MN begins cyclic communication (cyclic input data is not yet being evaluated). The CNs are configured in this state. **Controlled node (CN)** The module can be configured by the MN in this state. A command then switches the module to READY_TO_OPERATE mode. An LED lit red in this mode indicates failure of the MN.
Triple flash (approx. 1 Hz)	**Mode** The module is in the READY_TO_OPERATE state. **Managing node (MN)** Cyclic and asynchronous communication is taking place. Any received PDO data is ignored. **Controlled node (CN)** The configuration of the module is completed. Normal cyclic and asynchronous communication is taking place. The PDO data sent corresponds to the PDO mapping. Cyclic data is not yet being evaluated, however. An LED lit red in this mode indicates failure of the MN.
On	**Mode** The module is in PRE_OPERATIONAL_2 mode. PDO mapping is active and cyclic data is being evaluated.
Blinking (approx. 2.5 Hz)	**Mode** The module is in STOPPED mode. **Managing node (MN)** This status is not possible for the MN. **Controlled node (CN)** No output data is produced or input data supplied. It is only possible to enter or leave this mode after the MN has given the appropriate command.

Table 208: Status/Error LED as Status LED - POWERLINK operating mode



4.12.2.4.2 System failure error codes

Incorrect configuration or defective hardware can cause a system stop error.

The error code is indicated by the red Error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. The error code is output cyclically every 2 seconds.

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	●	●	●	-	Pause	●	●	●	-	Pause
Hardware error: The module or a system component is defective and must be replaced.	-	●	●	-	Pause	-	●	●	-	Pause

Table 209: Status/Error ("S/E") LED - System failure error codes

Key: ● ... 150 ms
- ... 600 ms
Pause ... 2 second delay

4.12.2.5 LED status indicators on the integrated X2 I/O slot

Figure	LED	Color	Status	Description
	1 - 14	Green		Input state of the corresponding digital input

Table 210: LED status indicators on the integrated X2 I/O slot

4.12.2.6 LED status indicators on the integrated X3 I/O slot

Figure	LED	Color	Status	Description
	DC	Yellow	On	I/O supply OK
	E	Red	Off	Everything OK
			Double flash	No power to module
	1 - 4	Yellow		Output status of the corresponding digital output
	5 - 8	Yellow		Input or output status of the corresponding digital input or output
	9 - 12	Yellow		Output status of the corresponding high-speed digital output

Table 211: LED status indicators on the integrated X3 I/O slot

4.12.2.7 Operating and connection elements

X20CP1301

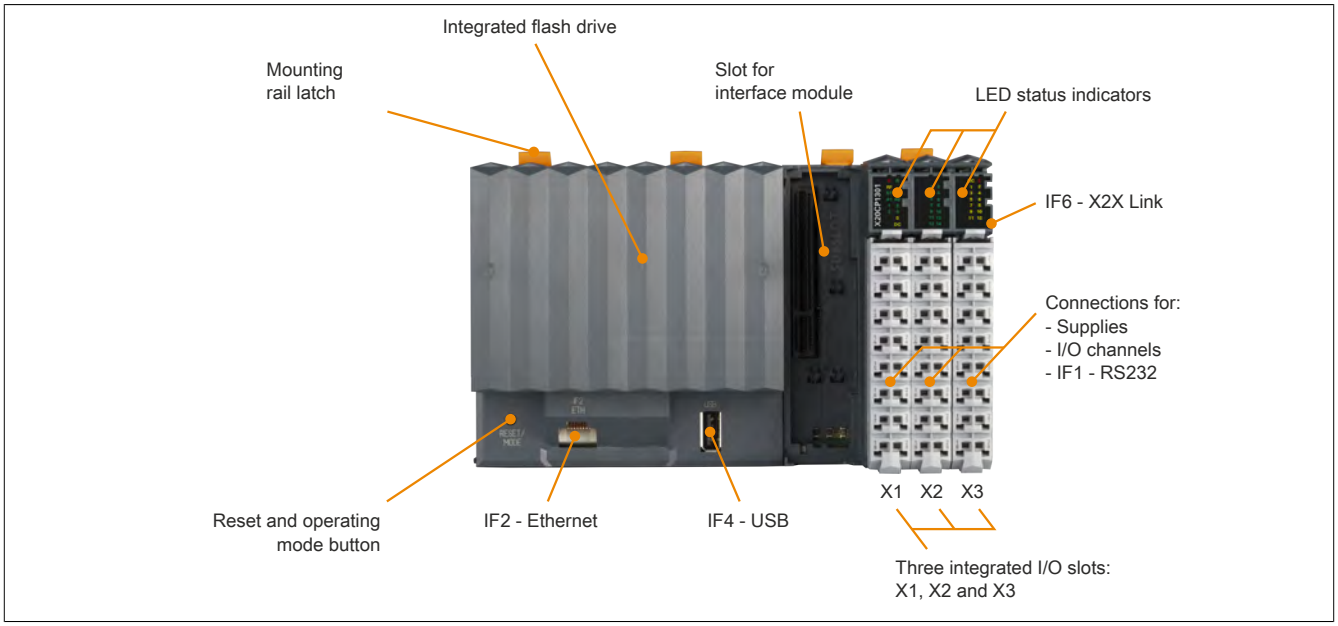


Figure 196: Operating elements for X20CP1301

X20CP1381 and X20CP1382

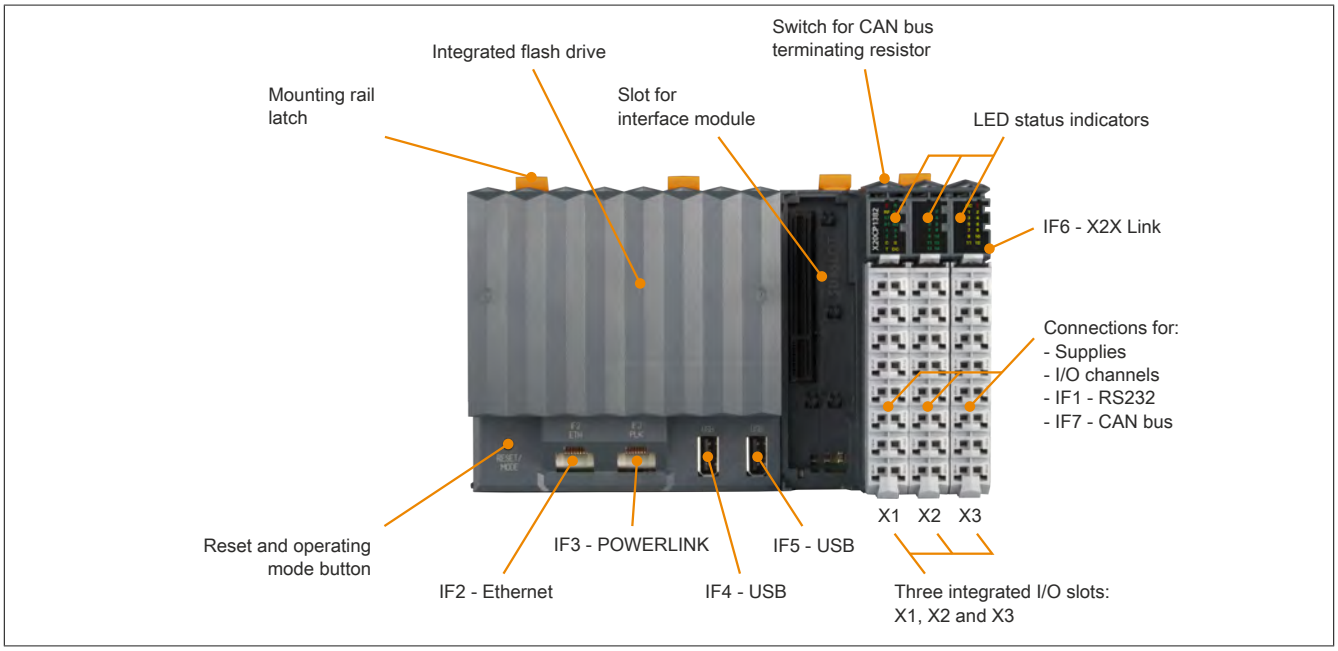


Figure 197: Operating elements for X20CP1381 and X20CP1382

4.12.2.8 Flash drive

These CPUs require application memory in order to operate. This application memory is integrated on a flash drive.

4.12.2.9 Reset and operating mode button

Figure 198: Reset and operating mode button

4.12.2.9.1 Reset

The button must be pressed for less than 2 seconds to trigger a reset. This triggers a hardware reset on the CPU, which means that:

- All application programs are stopped.
- All outputs are set to zero.

The PLC then boots into service mode by default. The boot mode that follows after pressing the reset button can be defined in Automation Studio.

- Service mode (default)
- Warm restart
- Cold restart
- Diagnostic mode

4.12.2.9.2 Operating mode

Three operating modes can be configured using different button sequences:

Operating mode	Button sequence	Description
BOOT	Boot mode is enabled by the following button sequence: • Press the button for less than two seconds. As soon as the "R" LED on the X1 I/O slot is lit **RED**, the button can be released. • Then press the button within two seconds for longer than two seconds. As soon as the "R" LED is no longer lit, the button can be released.	The default Automation Runtime system is started and the runtime system can be installed via the online interface (Automation Studio). User flash memory is deleted only after the download begins.
RUN	Press the button for less than two seconds. As soon as the "R" LED on the X1 I/O slot is lit **RED**, the button can be released.	RUN mode: The triggering and boot behavior are the same as what happens when a hardware reset is triggered (see section 4.12.2.9.1 "Reset" on page 1123).
DIAGNOSE	Press the button for more than 2 seconds. The "R" LED on the X1 I/O slot lights up **RED** and then goes out. As soon as the "R" LED is no longer lit, the button can be released.	Boots the CPU in diagnostic mode. Program sections in User RAM and User FlashPROM are not initialized. After diagnostic mode, the CPU always boots with a cold restart.

Table 212: Operating mode description

4.12.2.10 CPU supply

A power supply is integrated in these compact CPUs. It has a feed for the CPU, X2X Link and the internal I/O supply. The supply for the CPU and X2X Link is electrically isolated.

The connections are located on the X3 I/O slot.

4.12.2.10.1 Compact CPU supply concept

To ensure proper operation of compact CPUs, the following items must be taken into consideration:

The supply concept	Description
CPU and I/O GND	The GND contact is provided five times on the terminal blocks of the integrated I/O slots. All GND contacts are connected to one another. The GND contacts of the CPU and I/O supply therefore use the same voltage.
Plug-in X20 I/O modules	Supply of X20 I/O modules that can be connected to the compact CPU: • X2X Link: Supplied by the CPU supply • I/O channels: Supplied by the I/O supply
Integrated X1 I/O slot	All digital and analog signals as well as the RS232 and CAN bus interface are supplied by the CPU supply. Their operation is therefore guaranteed even if there is no I/O supply.
Integrated X2 I/O slot	• All digital signals are supplied by the CPU supply. Their operation is therefore guaranteed even if there is no I/O supply. • The encoder supply is supplied by the I/O supply. If the encoder is not to be connected to the E-stop chain, then it must be connected to an external power supply or it will be supplied by the CPU supply.
Integrated X3 I/O slot	• All 12 digital signals are supplied by the I/O supply. • The status messages for each channel also work without an I/O supply. This guarantees that status messages will continue to be transferred during an E-stop. • The status of the I/O supply is indicated by a separate status message. **Caution!** **Channels 5 to 8 are designed as mixed channels. If one of these channels is being used, it is absolutely essential to ensure that there is no external voltage present on the I/O channel when the I/O supply is cut off. Otherwise, power will be regenerated back to the plus terminal of the I/O supply via the I/O channel. This will result in defective components.** **The following solutions are available for preventing power regeneration from occurring:** • **The I/O supply of the CPU is not permitted to be switched off, which allows the reference potential to be maintained.** • **If the I/O supply is switched off anyway (e.g. as part of the E-stop chain), then the sensor/actuator supplies must also be switched off. This prevents potential power regeneration and protects components from being destroyed.**

Table 213: Compact CPU supply concept

4.12.2.10.2 Pinout

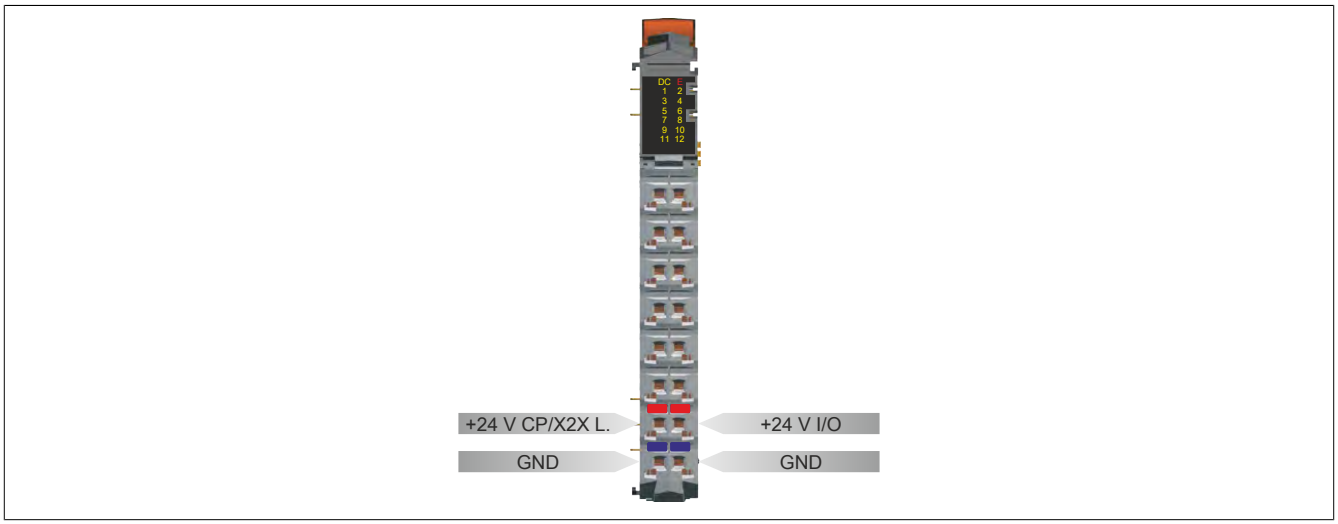


Figure 199: Integrated power supply - Pinout

4.12.2.10.3 Connection example

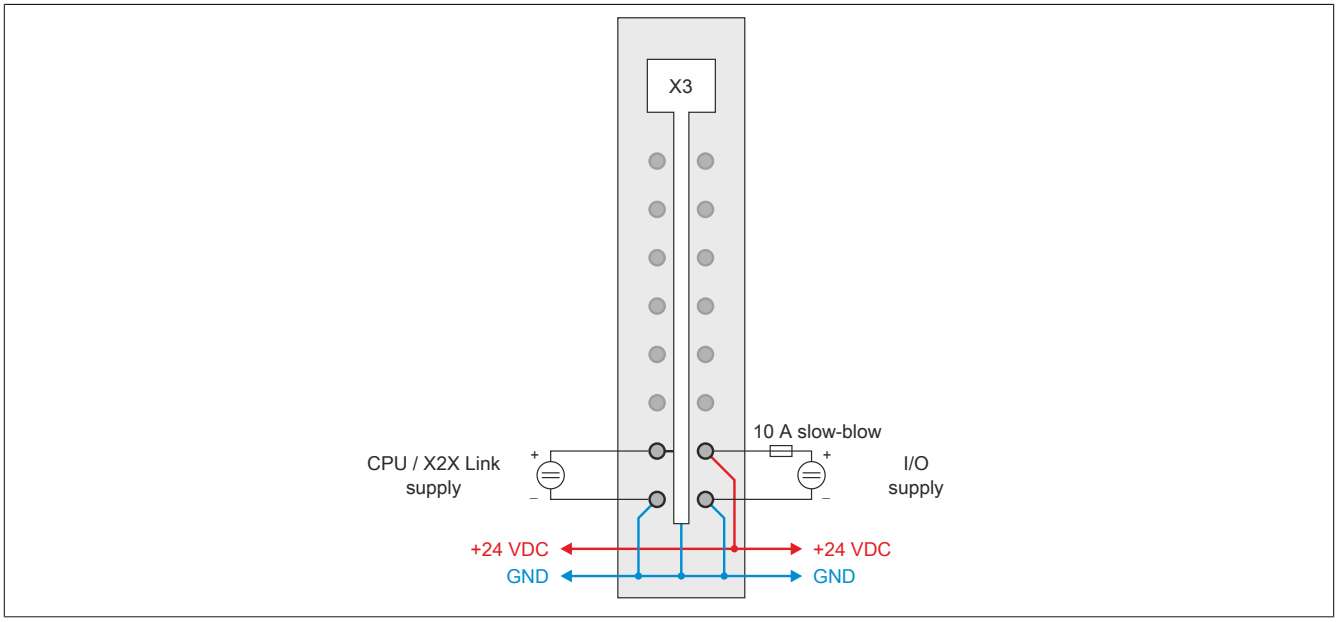


Figure 200: CPU supply - Connection example

4.12.2.11 RS232 interface (IF1)

The non-electrically isolated RS232 interface is primarily intended to serve as an online interface for communication with the programming device. It is located on the X1 I/O slot.

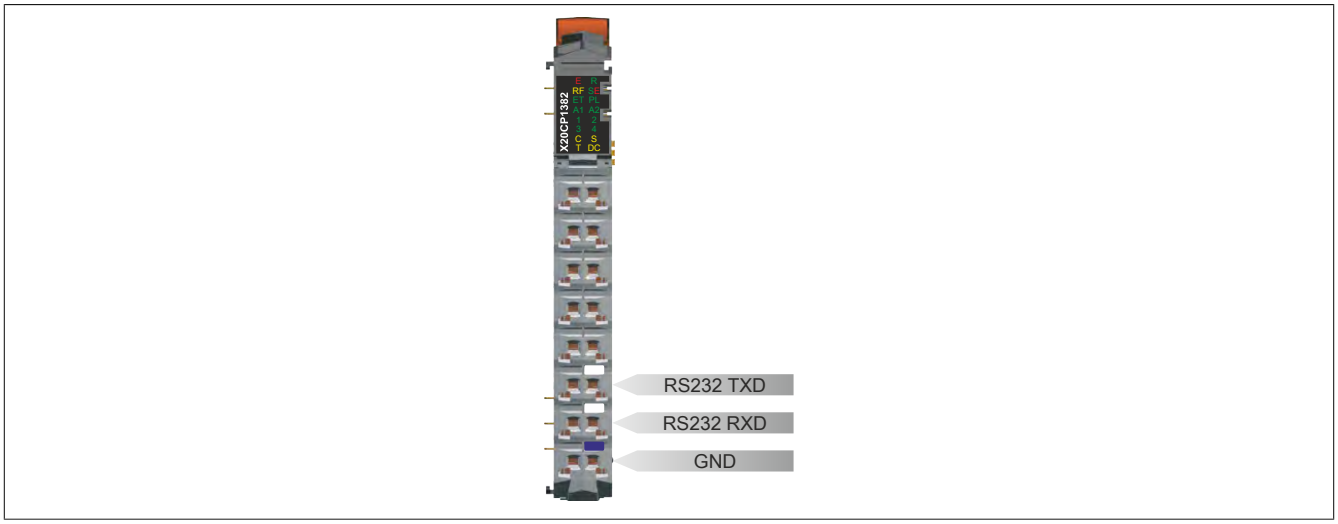
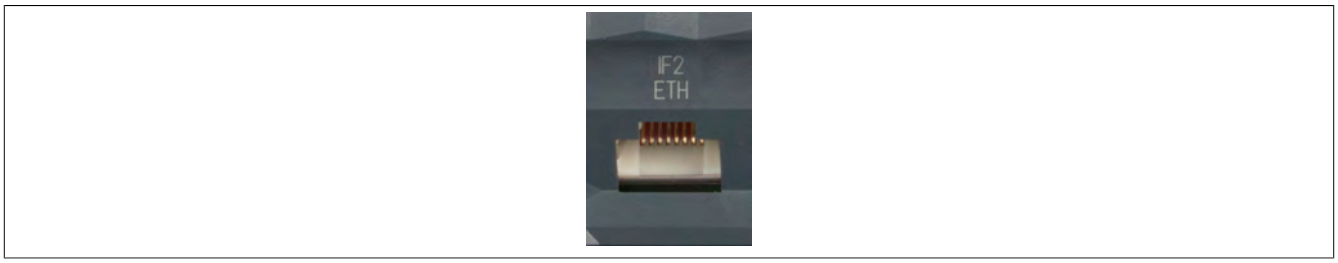


Figure 201: RS232 interface (IF1) on the X1 I/O slot - Pinout

4.12.2.12 Ethernet interface (IF2)



The IF2 interface is designed for 10BASE-T / 100BASE-TX transmission.

The INA2000 station number can be set using the Automation Studio software.

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section at www.br-automation.com.

Information:

The Ethernet interface (IF2) is not suited for POWERLINK (see section 4.12.2.13 "POWERLINK interface (IF3)" on page 1127).

Pinout

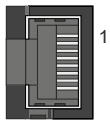
Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	TXD	Transmit data
	2	TXD\	Transmit data\
	3	RXD	Receive data
	4	Termination	
	5	Termination	
	6	RXD\	Receive data\
	7	Termination	
	8	Termination	

Table 214: Pinout

4.12.2.13 POWERLINK interface (IF3)

Compact CPUs X20CP1381 and X20CP1382 are equipped with a POWERLINK interface.

POWERLINK

Node numbers between 0x01 and 0xF0 are permitted. The node number can be configured using software.

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node.
0xF0	Operation as a managing node.
0xF1 - 0xFF	Reserved, switch position not permitted

Table 215: POWERLINK node number

Ethernet mode

In this mode, the interface is operated as an Ethernet interface. The INA2000 station number can be set using the Automation Studio software.

Pinout

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section at www.br-automation.com.

Pin	Assignment	
1	RxD	Receive data
2	RxD\	Receive data\
3	TxD	Transmit data
4	Termination	
5	Termination	
6	TxD\	Transmit data\
7	Termination	
8	Termination	

Table 216: POWERLINK interface (IF3) - Pinout

4.12.2.14 USB interfaces (IF4 and IF5)

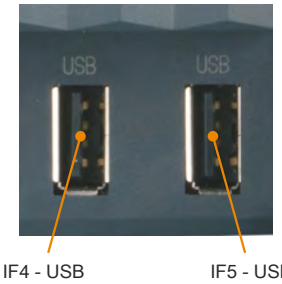


Figure 202: USB interfaces (IF4 and IF5)

IF4 and IF5 are non-electrically isolated USB interfaces. The connection is made using a USB 2.0 interface. Only IF4 is available on the entry level CPU.

The USB interfaces can only be used for devices approved by B&R (e.g. floppy disk drive, DiskOnKey or dongle).

Information:

- **USB interfaces cannot be used for online communication with a programming device.**
- **Only devices isolated from GND can be connected to the USB interfaces.**
- **The USB interfaces can handle up to the following current:**
  - **IF4: Max. 0.5 A**
  - **IF5: Max. 0.1 A**

4.12.2.15 CAN bus interface (IF7)

With the exception of the entry level CPU, all compact CPUs are equipped with a non-electrically isolated CAN bus interface. It is located on the X1 I/O slot.

4.12.2.15.1 Pinout

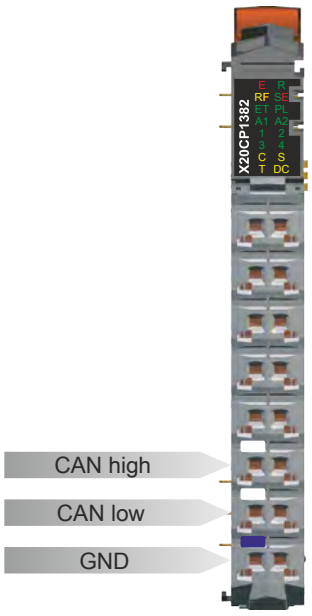


Figure 203: CAN bus interface (IF7) on the X1 I/O slot - Pinout

4.12.2.15.2 Terminating resistor

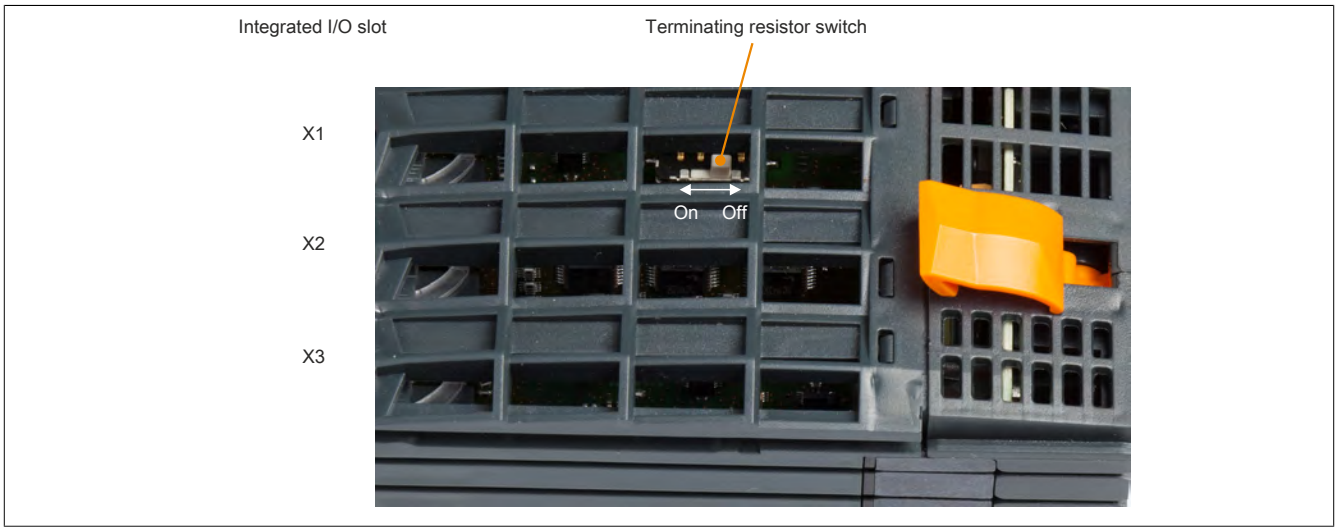


Figure 204: Switch positions for the CAN bus terminating resistor

A terminating resistor is already installed on the X1 I/O slot. It can be turned on and off with a switch on top of the housing. An active terminating resistor is indicated by the "T" LED.

4.12.2.16 Slot for interface modules

These CPUs are equipped with one slot for interface modules.

Various bus and network systems can easily be integrated into the X20 system by selecting the corresponding interface module.

4.12.2.17 Overtemperature cutoff

To prevent damage, a shutdown/reset is triggered on the CPU when the processor reaches 95°C.

The following errors are entered in the logbook:

Error number	Error description
9204	WARNING: System halted because of temperature check
9210	WARNING: Boot by watchdog or manual reset

Table 217: Logbook entries after overtemperature cutoff

4.12.2.18 Data and real-time clock buffering

Compact CPUs are not designed for use with batteries. This makes them completely maintenance-free. The following features make operation without a backup battery possible.

Data and real-time clock buffering	Type of buffering	Note
Remanent variables	FRAM	This FRAM stores its contents ferroelectrically. Unlike normal SRAM, this does not require a battery.
Real-time clock	Gold foil capacitor	The real-time clock is buffered for approx. 1000 hours by a gold foil capacitor. The gold foil capacitor is completely charged after 3 continuous hours of operation.

4.12.2.19 Programming the system flash memory

General information

In order for the application project to be executed on the CPU, the Automation Runtime operating system, system components and application project must be installed on the flash drive.

Installation over an online connection

These CPUs come standard with an Automation Runtime system (with limited functionality) already installed. This runtime system is started in boot mode (see section 4.12.2.9 "Reset and operating mode button" on page 1123 or an invalid flash drive). Some of its tasks include initializing the Ethernet and integrated serial RS232 interfaces so that it is possible to download a runtime system.

1. Switch on the supply voltage for the CPU. The CPU starts with the default Automation Runtime in boot mode (see section 4.12.2.9 "Reset and operating mode button" on page 1123 or an invalid flash drive).
2. Establish a physical online connection between the programming device (PC or industrial PC) and the CPU (e.g. over an Ethernet network or the RS232 interface).
3. Before you can establish an online connection via Ethernet, the CPU must be assigned an IP address. Search for available B&R target system in the local network by selecting **Online / Settings** from the Automation Studio menu and then clicking the **Browse targets** button. The CPU should appear in the list. If the CPU has not already received an IP address from a DHCP server, right-click on it and select **Set IP parameters** from the shortcut menu. All necessary network configurations can be made on a temporary basis in this dialog box (should be identical to the settings defined in the project).
4. Configure an online connection in Automation Studio. For details about the configuration: See AS help system under "Automation Software / Communication / Online communication"
5. Start the download procedure by selecting **Services** from the **Project** menu. Then select **Transfer Automation Runtime** from the pop-up menu. Now follow the instructions provided by Automation Studio.

4.12.2.20 I/O channels

Compact CPUs are equipped with three integrated I/O slots. These devices have 30 digital inputs/outputs and two analog inputs. One analog input can also be used for PT1000 resistance temperature measurement.

Information about the functions of the high-speed digital inputs and outputs can be found in the section 4.12.2.24 "Functions of the high-speed digital inputs/outputs" on page 1138.

Overview of available I/O channels:

Integrated I/O	Quantity	I/O slot	Description
Digital inputs	14	X1: DI 1 to DI 4 X2: DI 1 to DI 10	24 VDC, sink, ≥0.5 ms, configurable software filter
High-speed digital inputs	4	X2: DI 11 to DI 14	24 VDC, sink, 2 µs, configurable software filter
Digital outputs	4	X3: DO 1 to DO 4	24 VDC, 0.5 A, source
Fast digital outputs	4	X3: DO 9 to DO 12	24 VDC, 0.2 A, 2 µs
Digital inputs/outputs	4	X3: DI 5 / DO 5 to DI 8 / DO 8	24 VDC, 0.5 A, configurable software filter
Analog inputs	2	X1: AI 1 to AI 2	±10 V / 0 to 20 mA or 4 to 20 mA, 12-bit, 1 ms
Temperature inputs	1	X1: AI 1 (Sensor + and Sense -)	PT1000 resistance temperature measurement Measurement takes place using the AI 1 analog input.

Table 218: I/O channels on compact CPUs

4.12.2.21 Pinout

X1 I/O slot - Pinout

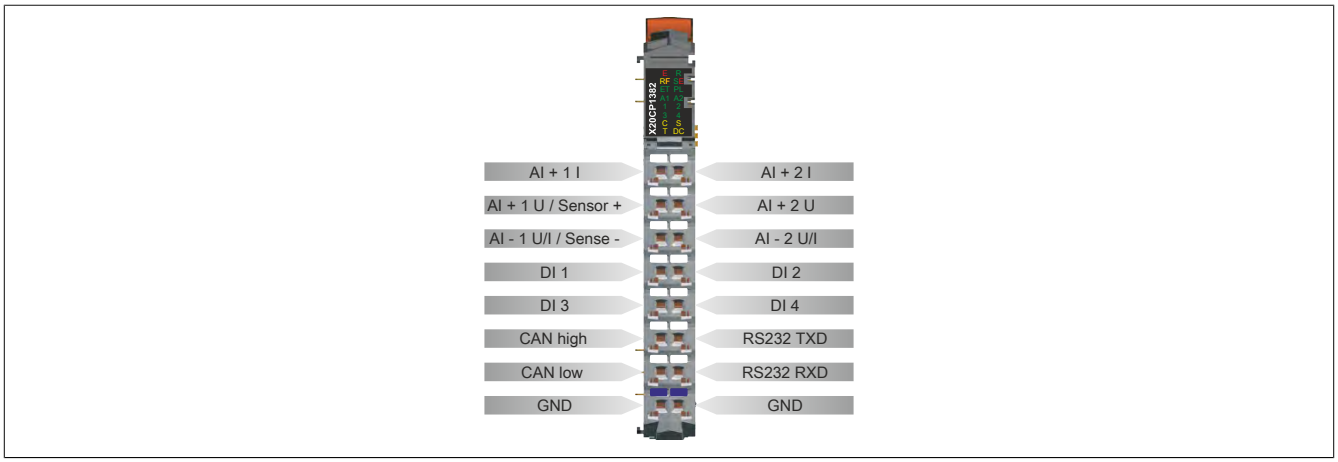


Figure 205: Pinout of the integrated X1 I/O slot

X2 I/O slot - Pinout

To prevent crosstalk, each signal line of the fast digital inputs should be shielded individually. The maximum cable length is 20 m.

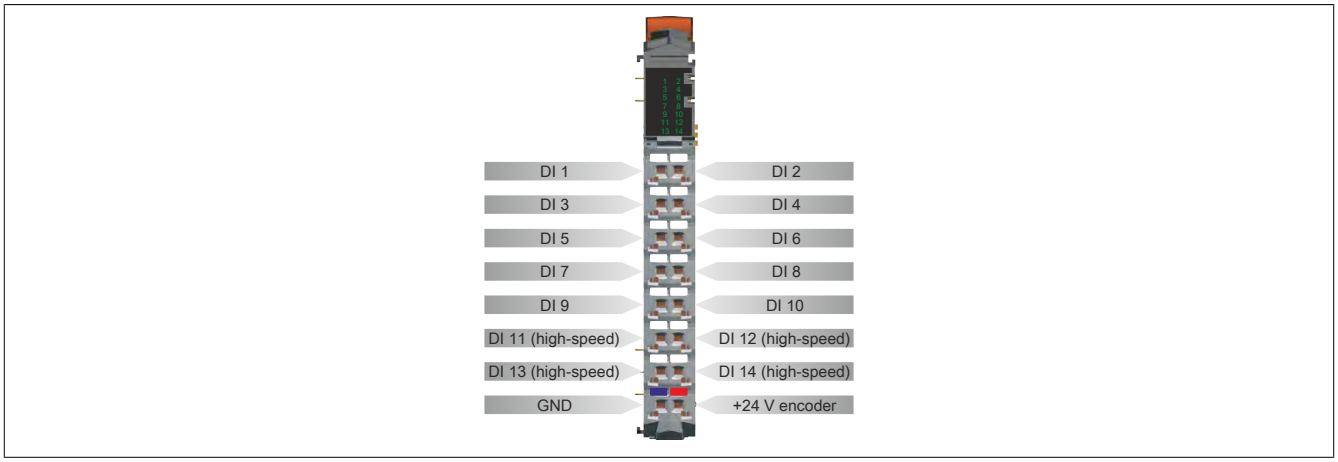


Figure 206: Pinout of the integrated X2 I/O slot

X3 I/O slot - Pinout

To ensure proper operation of the digital mixed channels (DI 5 / DO 5 to DI 8 / DO 8), it is important to observe the notes in section 4.12.2.10.1 "Compact CPU supply concept" on page 1124.

To prevent crosstalk, each signal line of the fast digital outputs should be shielded individually. The maximum cable length is 20 m.

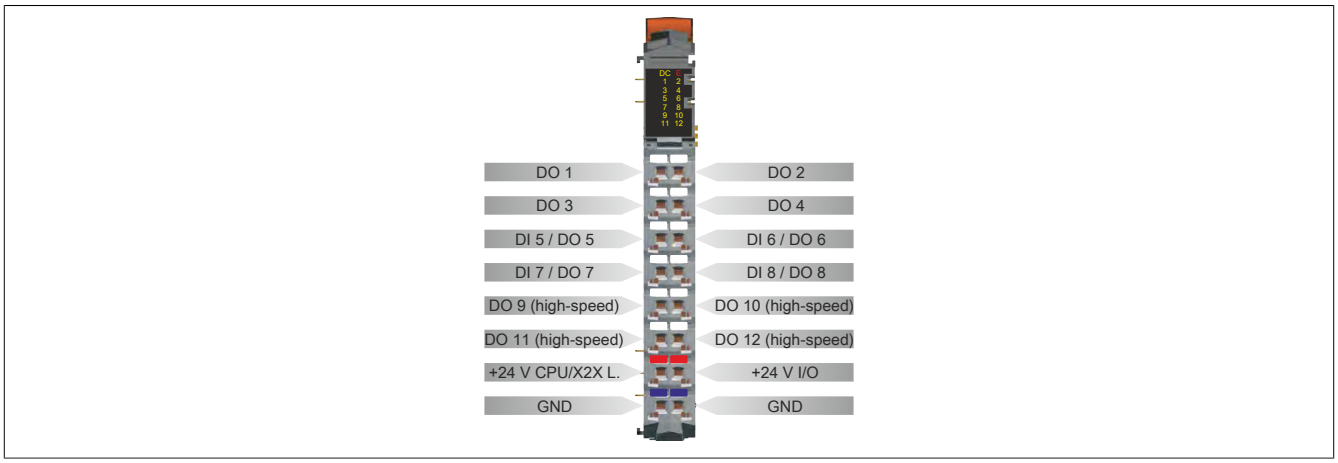


Figure 207: Pinout of the integrated X3 I/O slot

4.12.2.22 Connection examples

4.12.2.22.1 X1 I/O slot - Connection examples

Voltage/Current measurement, digital inputs and CAN bus

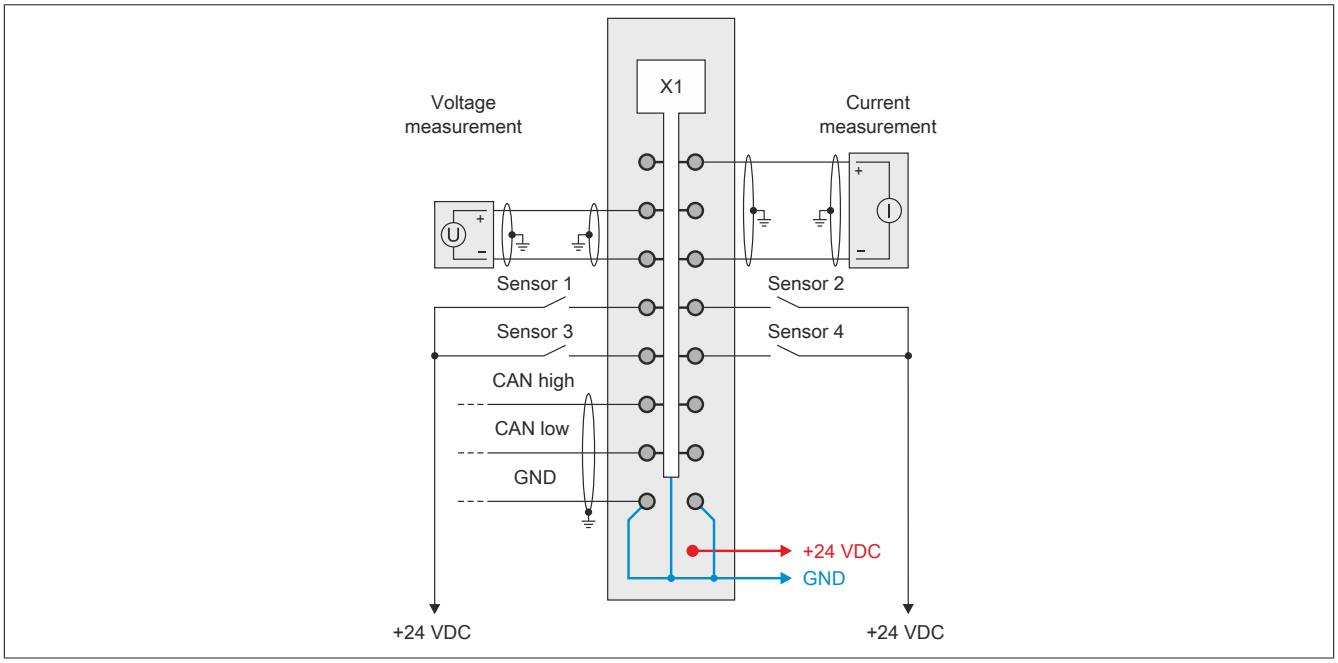


Figure 208: Connection example 1 for integrated X1 I/O slot

PT1000 resistance temperature measurement, voltage measurement, digital inputs and RS232

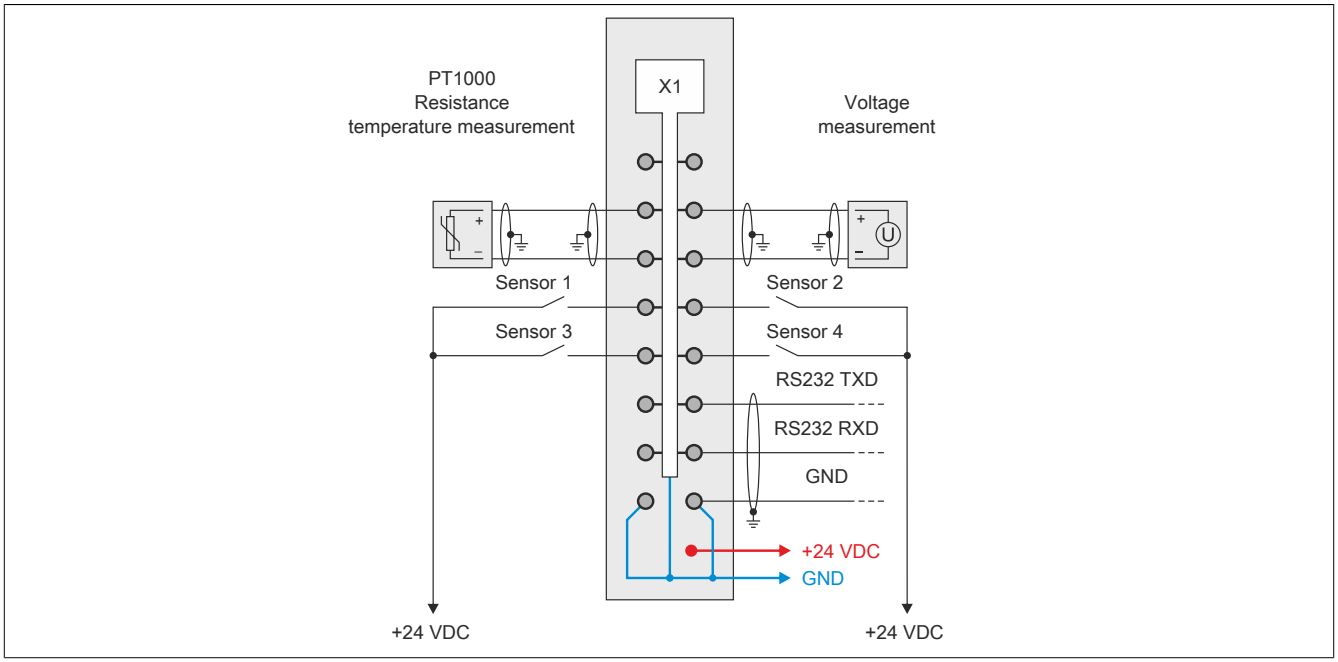


Figure 209: Connection example 2 for integrated X1 I/O slot

4.12.2.22.2 X2 I/O slot - Connection example

Digital inputs and ABR incremental encoder

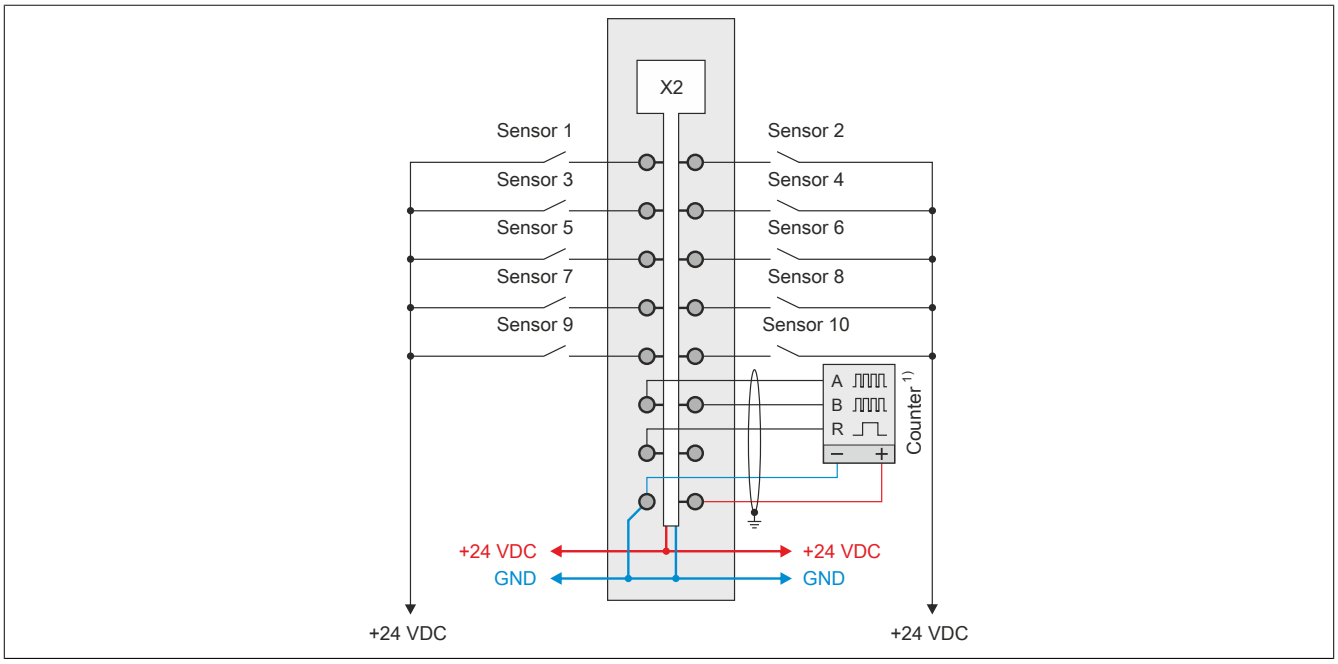


Figure 210: Connection example 1 for integrated X2 I/O slot

1) Observe the wiring guidelines from the encoder manufacturer.

DI11 to DI14 are used as fast digital inputs

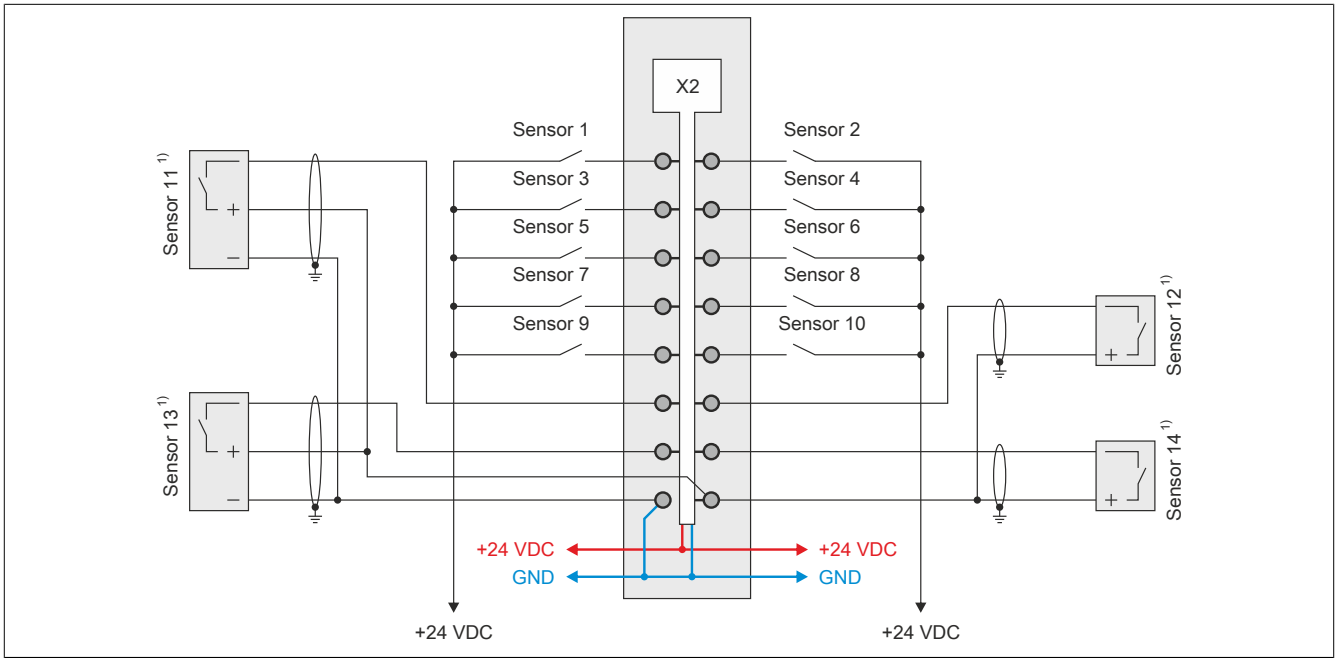


Figure 211: Connection example 2 for integrated X2 I/O slot

1) Observe the wiring guidelines from the sensor manufacturer.

4.12.2.22.3 X3 I/O slot - Connection example

Digital inputs/outputs, direction/frequency (DF), PWM, CPU / X2X Link supply and I/O supply

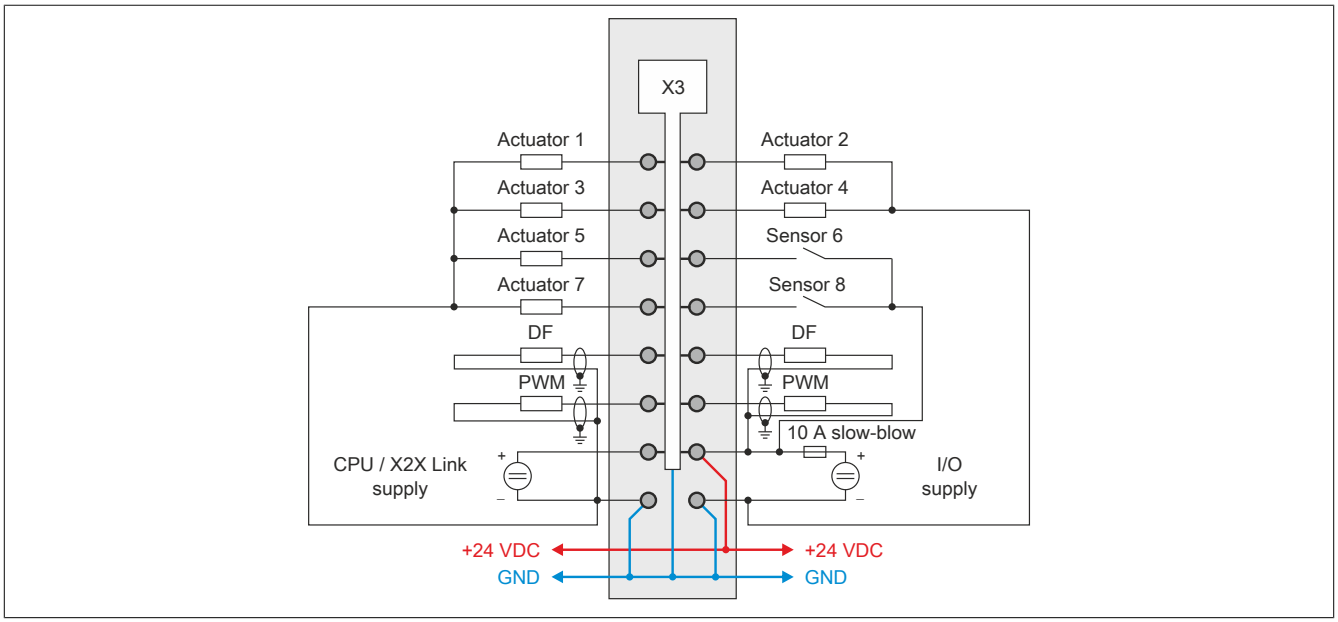


Figure 212: Connection example for integrated X3 I/O slot

4.12.2.23 X20 shielding bracket

The X20 shielding bracket (model number X20AC0SF7.0010) is installed below the X20 system. The shield is pressed against the shielding bracket using ground terminals from another manufacturer (e.g. PHOENIX or WAGO) or a cable tie.

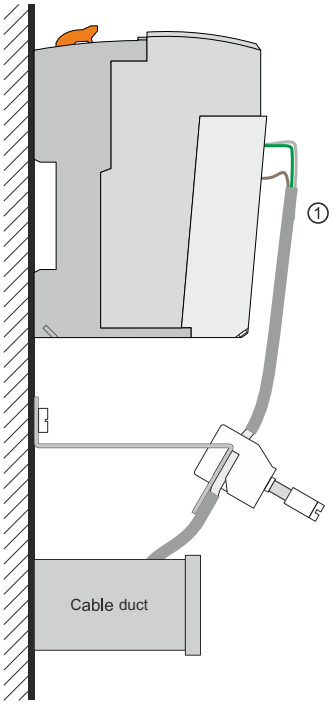
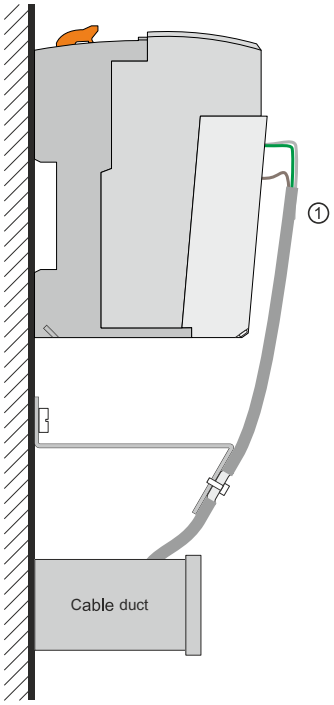
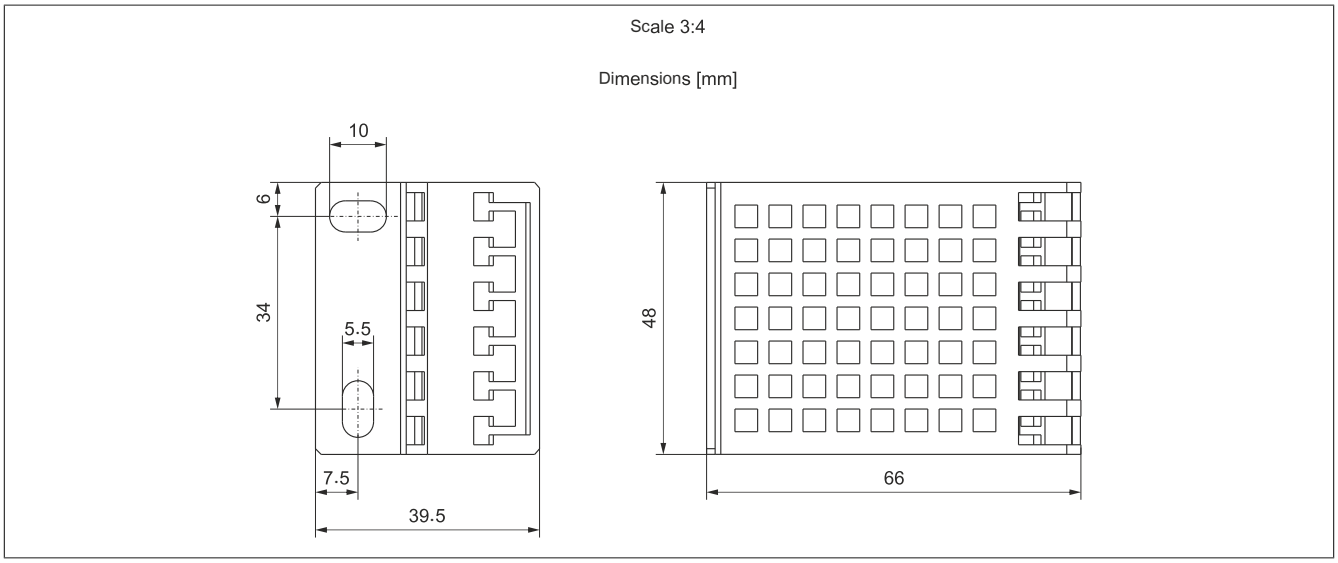
Attaching the shield with a ground terminal	Attaching the shield with a cable tie
	

Table 219: Cable shielding via X20 shielding bracket

To reduce the EMC emissions most effectively, the cable shield must reach as high as possible after the cable tie (see ① in the diagram above).

Dimensions



Content of delivery

- 10 X20 shielding brackets
- Installation template

4.12.2.24 Functions of the high-speed digital inputs/outputs

4.12.2.24.1 Functions of the high-speed digital inputs

Possible functions

The high-speed digital inputs DI 11 to DI 14 can be configured for the following functions:

Channel	Counter function				Edge detection	
DI 11	Event counter 1	A	A	D - Direction	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times
DI 12		B	B	F - Frequency	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times
DI 13	Event counter 2	A	R	R	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times
DI 14		B	E - Reference enable	E - Reference enable	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times

Table 220: Possible functions of the high-speed digital inputs DI 11 to DI 14

Please note

The following points must be taken into account to correctly configure the high-speed digital inputs:

- The counter functions are mutually exclusive. Only one type of counter function can be selected at a time. It is not possible to select two event counters (DI 11 and DI 13) at the same time together with an AB or DF counter (each on DI 13 and DI 14)!
- It is possible to select a counter function and edge detection at the same time.
- A position or counter latch is possible when configuring the high-speed inputs as a 2x event counter, ABR incremental encoder or DF function.

Examples of possible configurations

Channel	Configuration 1	Configuration 2	Configuration 3	Configuration 4
DI 11	Event counter 1	• Edge counters • Edge times	A	D
DI 12	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times	B	F
DI 13	Event counter 2	A	R	R
DI 14	• Period measurement • Gate measurement • Differential time measurement	B	E - Reference enable	E - Reference enable

Channel	Configuration 5	Configuration 6	Configuration 7	Configuration 8
DI 11	Event counter 1	A	• Period measurement • Gate measurement • Differential time measurement	D - Direction
DI 12	• Edge counters • Edge times	B	• Period measurement • Gate measurement • Differential time measurement	F - Frequency
DI 13	Event counter 2	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times	• Edge counters • Edge times
DI 14	• Period measurement • Gate measurement • Differential time measurement	• Edge counters • Edge times	• Edge counters • Edge times	• Period measurement • Gate measurement • Differential time measurement

4.12.2.24.2 Functions of the high-speed digital outputs

Possible functions

The high-speed digital outputs DO 9 to DO 12 can be configured for the following functions:

Channel	Function	
DO 9	PWM - Pulse width modulation	D - Direction
DO 10	PWM - Pulse width modulation	F - Frequency
DO 11	PWM - Pulse width modulation	D - Direction
DO 12	PWM - Pulse width modulation	F - Frequency

Table 221: Possible functions of the high-speed digital inputs DO 9 to DO 12

Examples of possible configurations

Channel	Configuration 1	Configuration 2	Configuration 3	Configuration 4
DO 9	PWM - Pulse width modulation	D - Direction	PWM - Pulse width modulation	D - Direction
DO 10	PWM - Pulse width modulation	F - Frequency	PWM - Pulse width modulation	F - Frequency
DO 11	D - Direction	PWM - Pulse width modulation	PWM - Pulse width modulation	D - Direction
DO 12	F - Frequency	PWM - Pulse width modulation	PWM - Pulse width modulation	F - Frequency

4.12.2.25 Input/Output circuit diagram

4.12.2.25.1 Input circuit diagram of the analog inputs and temperature input on X1

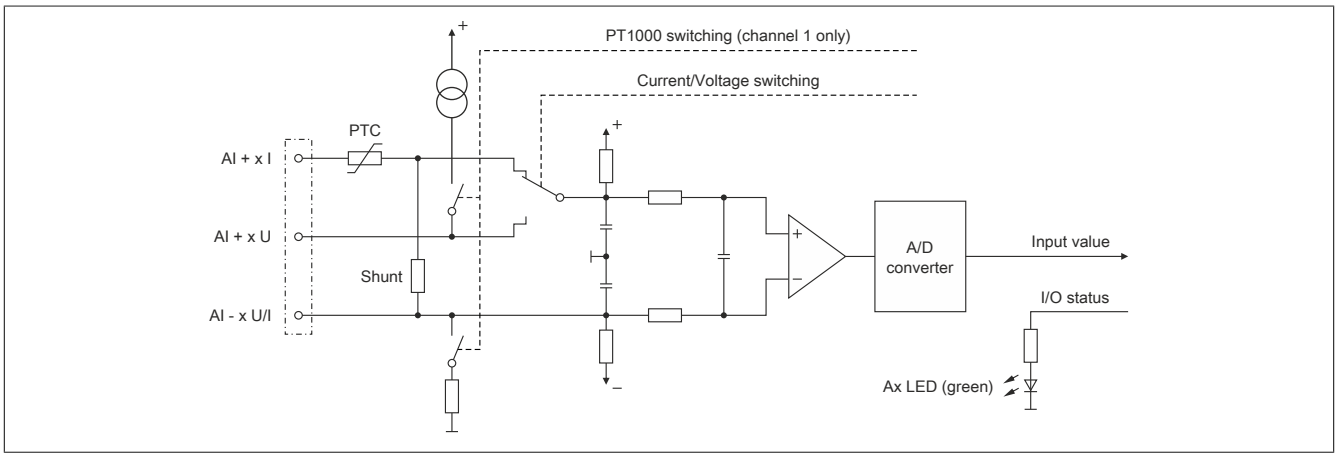


Figure 213: Input circuit diagram of the analog inputs and temperature input on the integrated X1 I/O slot

4.12.2.25.2 Input circuit diagram of the digital inputs

4.12.2.25.2.1 Input circuit diagram of the digital inputs on X1 and the high-speed digital inputs on X2

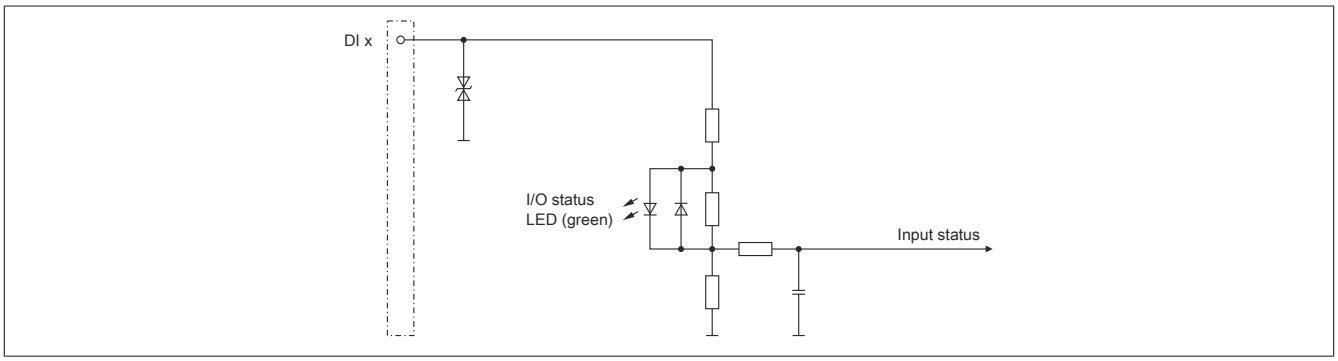


Figure 214: Input circuit diagram of the digital inputs on the integrated X1 I/O slot and the high-speed digital inputs on the integrated X2 I/O slot

4.12.2.25.2.2 Input circuit diagram of the digital inputs on X2

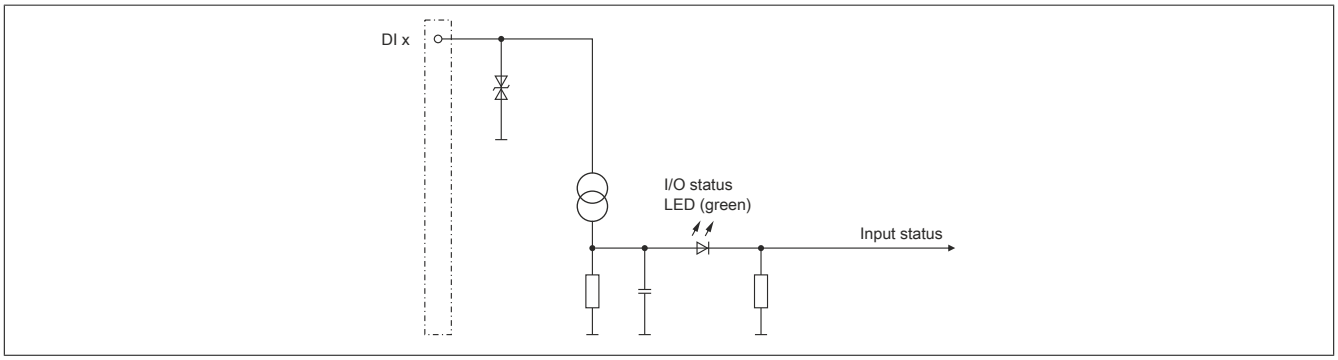


Figure 215: Input circuit diagram of the digital inputs on the integrated X2 I/O slot

4.12.2.25.3 Output circuit diagram of the digital outputs

4.12.2.25.3.1 Output circuit diagram of the digital outputs on X3

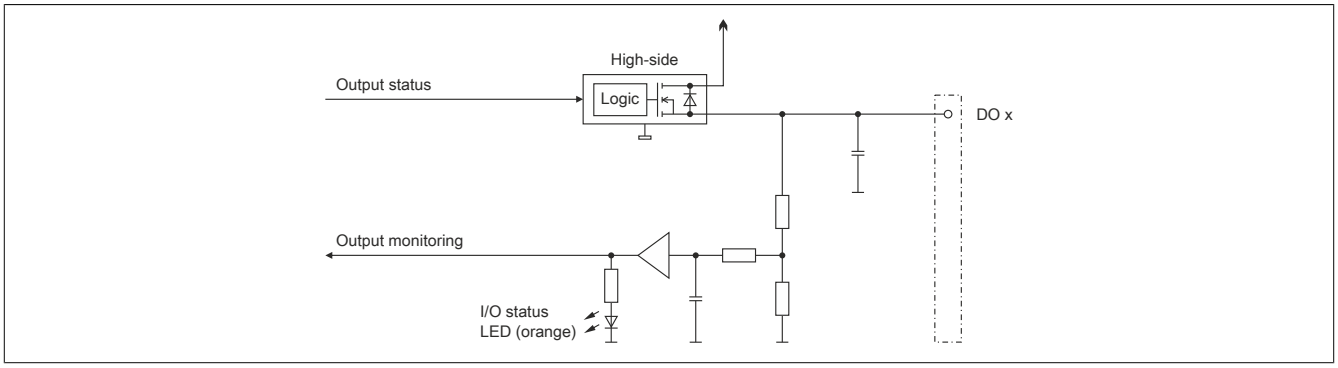


Figure 216: Output circuit diagram of the digital outputs on the integrated X3 I/O slot

4.12.2.25.3.2 Output circuit diagram of the high-speed digital outputs on X3

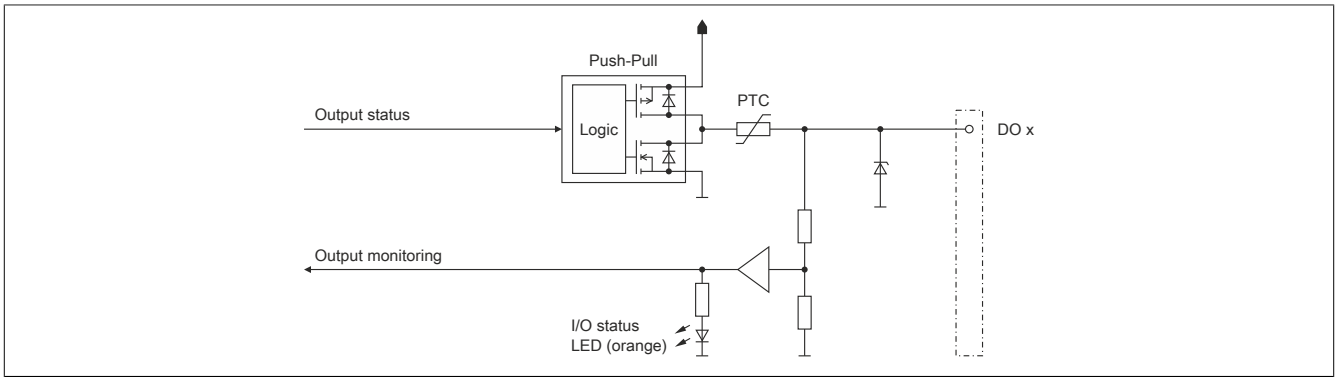


Figure 217: Output circuit diagram of the fast digital outputs on the integrated X3 I/O slot

4.12.2.25.4 Input/Output circuit diagram of the digital mixed channels on X3

To ensure proper operation of the digital mixed channels (DI 5 / DO 5 to DI 8 / DO 8), it is important to observe the notes in section 4.12.2.10.1 "Compact CPU supply concept" on page 1124.

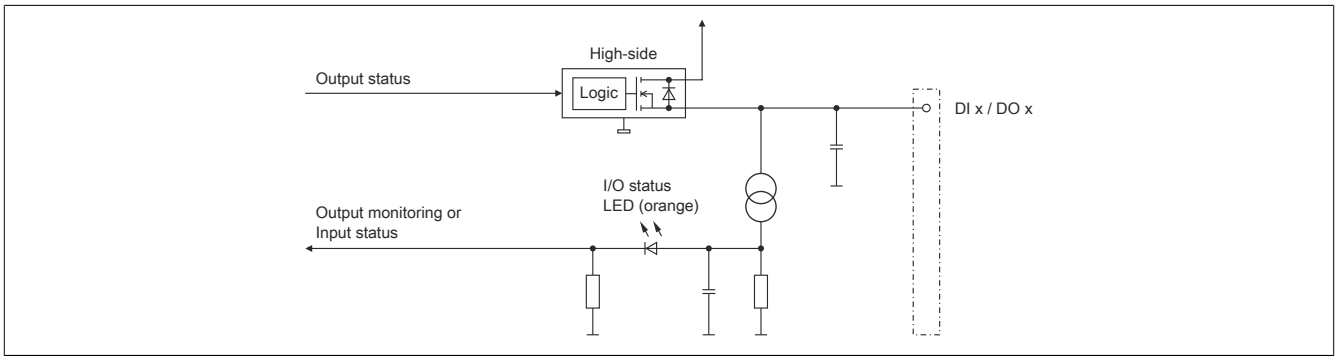


Figure 218: Input/Output circuit diagram of the digital mixed channels on the integrated X3 I/O slot

4.12.2.25.5 Circuit diagram for the encoder supply on X2

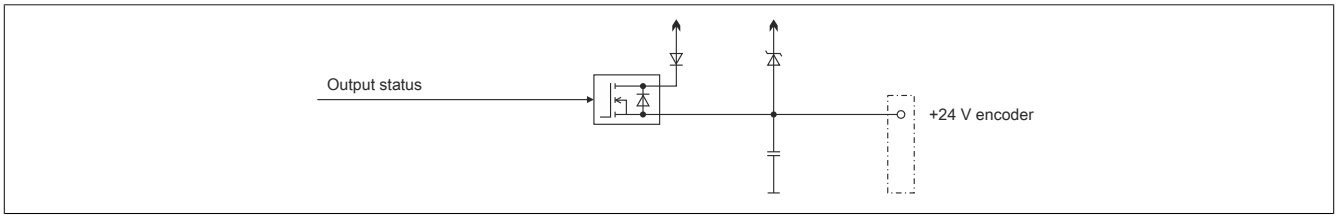


Figure 219: Circuit diagram of the encoder supply on the integrated X2 I/O slot

4.12.2.25.6 Circuit diagram of the CPU, X2X Link and I/O supply on X3

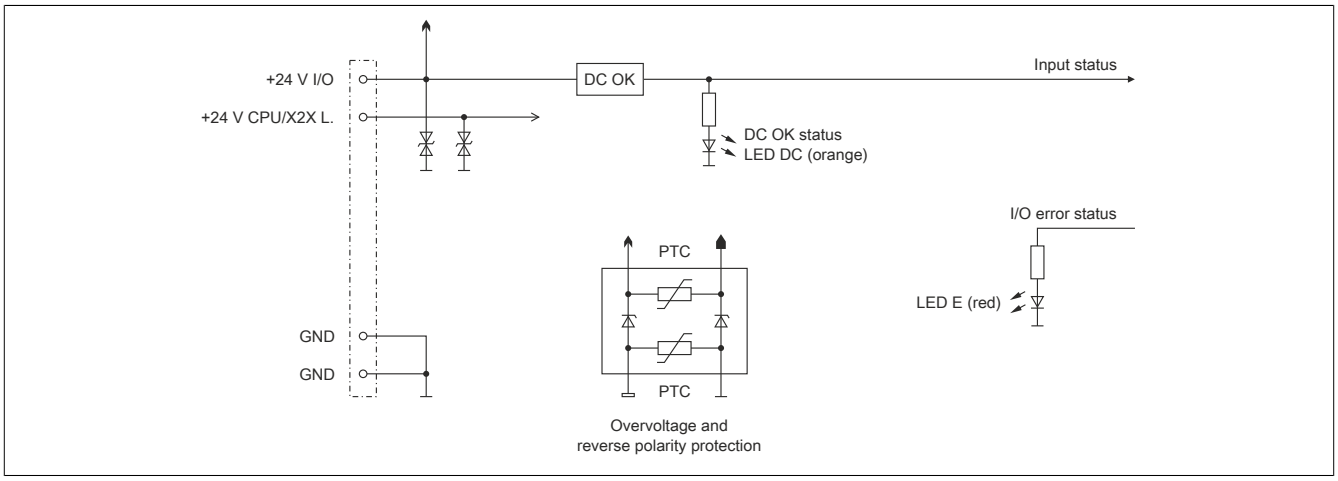


Figure 220: Circuit diagram of the CPU, X2X Link and I/O supply on the integrated X3 I/O slot

4.12.2.26 Switching frequency derating for high-speed digital outputs

The high-speed digital outputs can be switched with a frequency of max. 200 kHz. Derating may be necessary depending on the mounting orientation and operating temperature.

Switching frequency derating for horizontal mounting orientations

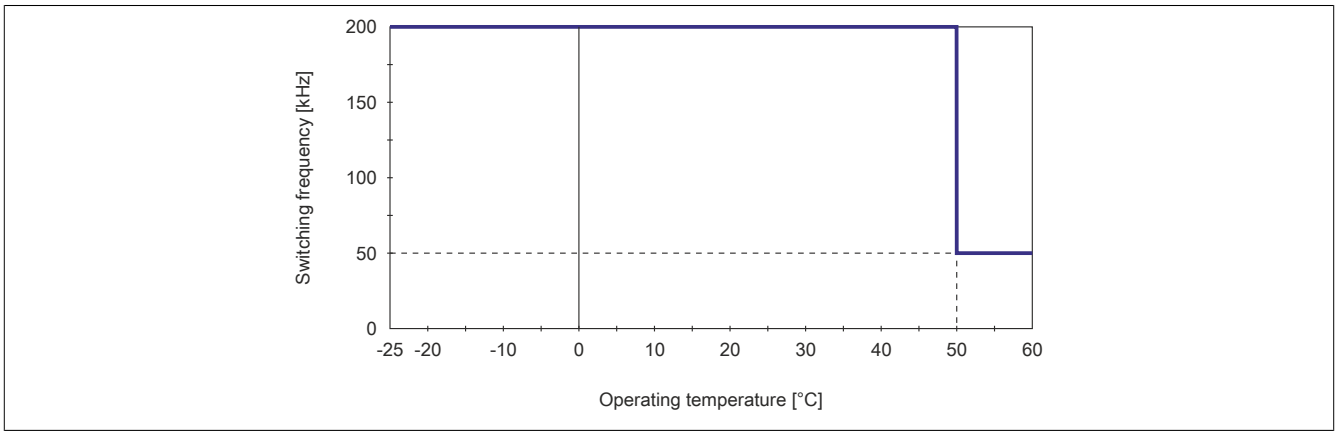


Figure 221: Switching frequency derating for high-speed digital outputs with horizontal mounting orientations

Switching frequency derating for vertical mounting orientations

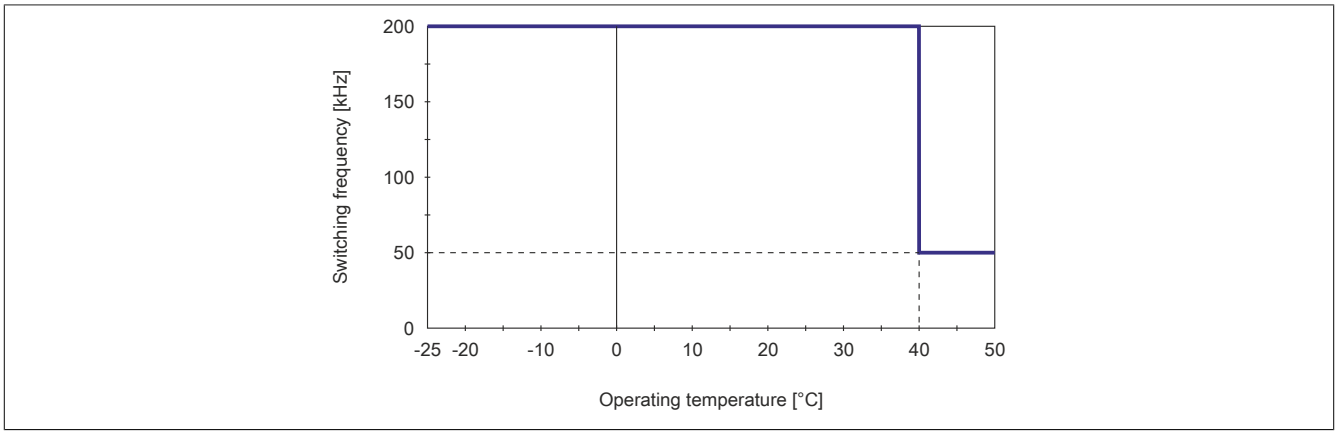
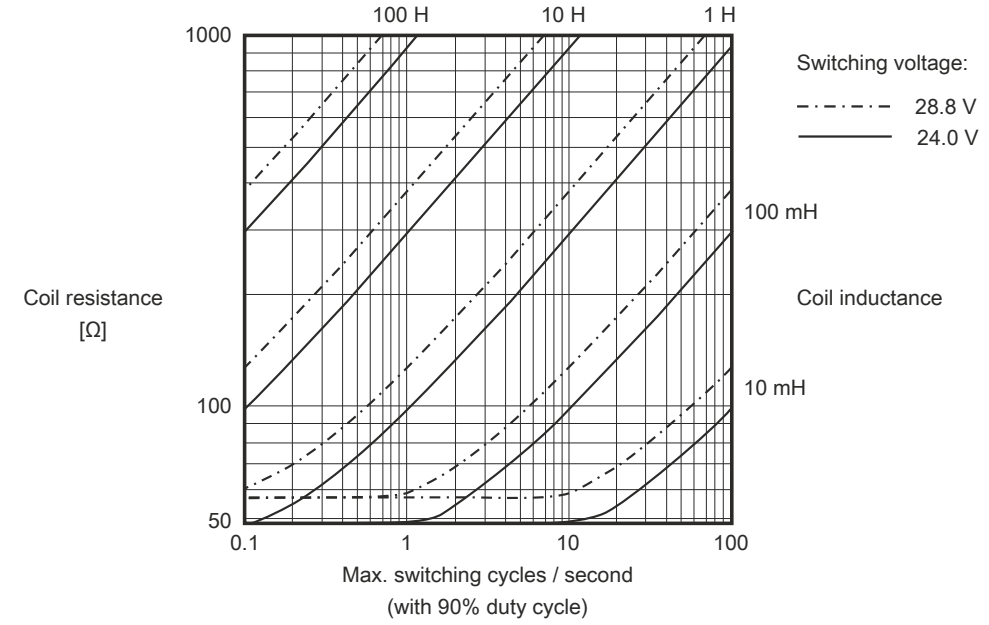


Figure 222: Switching frequency derating for high-speed digital outputs with vertical mounting orientations

4.12.2.27 Switching inductive loads



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.12.2.28 Register description

4.12.2.28.1 Register overview of the I/O data points on the integrated X1 I/O slot

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
X1 - Configuration						
2048	X1CfO_DI_Filter	USINT				•
2128	X1CfO_AI_Mode	USINT				•
2112	X1CfO_AI1_Filter	USINT				•
2116	X1CfO_AI1_LowerLim	INT				•
2118	X1CfO_AI1_UpperLim	INT				•
2120	X1CfO_AI2_Filter	USINT				•
2124	X1CfO_AI2_LowerLim	INT				•
2126	X1CfO_AI2_UpperLim	INT				•
X1 - Communication						
0	Digital inputs	USINT	•			
	DigitalInput01	Bit 0				
	DigitalInput02	Bit 1				
	DigitalInput03	Bit 2				
	DigitalInput04	Bit 3				
64	AnalogInput01	INT	•			
		UINT	•			
66	AnalogInput02	INT	•			
80	StatusInput01	USINT	•			

4.12.2.28.1.1 Digital inputs

Unfiltered

The input status is recorded in a 100 µs cycle.

Filtered

The filtered status is transferred in a 100 µs cycle.

Filtering takes place asynchronously in an interval of 100 µs.

Digital input filter

Name:
X1CfO_DI_Filter

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs.

Data type	Value	Filter
USINT	0	No SW filter
	1	0.1 ms
	...	...
	250	25 ms - Higher values are limited to this value

Input state of digital inputs 1 to 4

Name:
DigitalInput01 to DigitalInput04

This register is used to indicate the input state of digital inputs 1 to 4.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status of digital input 1
...		...	
3	DigitalInput04	0 or 1	Input status of digital input 4

4.12.2.28.1.2 Analog inputs

Analog input values are recorded in a fixed interval. The time required for conversion/updating depends on the number of analog inputs and on the input signal:

Input signal	Time required for conversion/updating
1 current/voltage input	100 µs
1 temperature/resistance input	200 µs
2 current/voltage inputs	200 µs
1 current/voltage input and 1 temperature/resistance input	400 µs

Analog input values

Name:
AnalogInput01

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC
	0 to 32,767	Current signal 0 to 20 mA (with 0 to 20 mA configuration)
	-8,192 to 32,767	Current signal 0 to 20 mA (with 4 to 20 mA configuration)
	-2,000 to 8,500	PT1000 signal -200.0 to 850.0°C
UINT	0 to 40,000	Resistance signal 0 to 4000.0 Ω

Name:
AnalogInput02

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC
	0 to 32,767	Current signal 0 to 20 mA (with 0 to 20 mA configuration)
	-8,192 to 32,767	Current signal 0 to 20 mA (with 4 to 20 mA configuration)

Input status

Name:
StatusInput01

This register holds the status of the analog inputs. A change in the monitoring status generates an error message. The following states are monitored depending on the settings:

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

Limiting the analog value

In addition to the status information, the analog value is set to the limit values listed below by default when an error occurs (see "Limit values"). The analog value is limited to the new values if the limit values were changed.

Input filter

The analog inputs are equipped with a configurable input filter.

Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

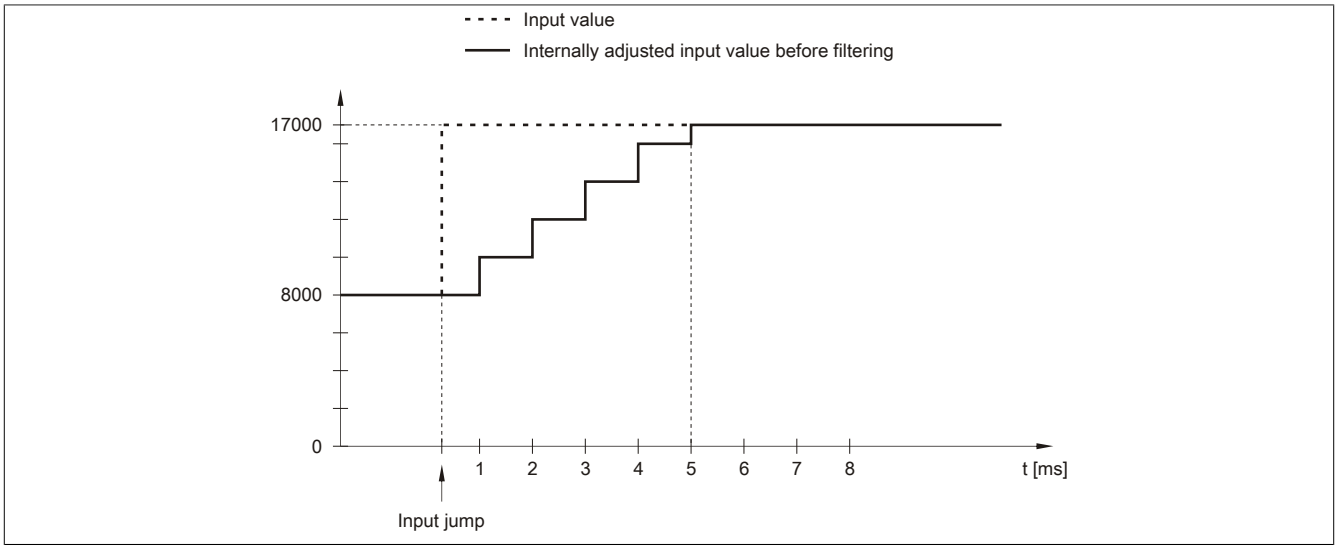


Figure 223: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

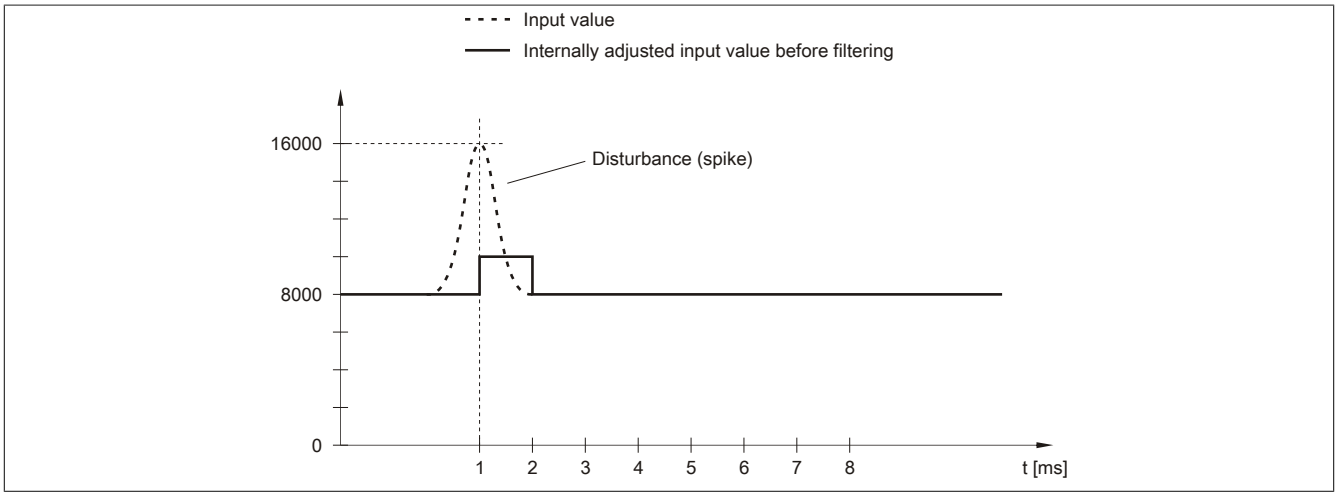


Figure 224: Adjusted input value for disturbance

Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

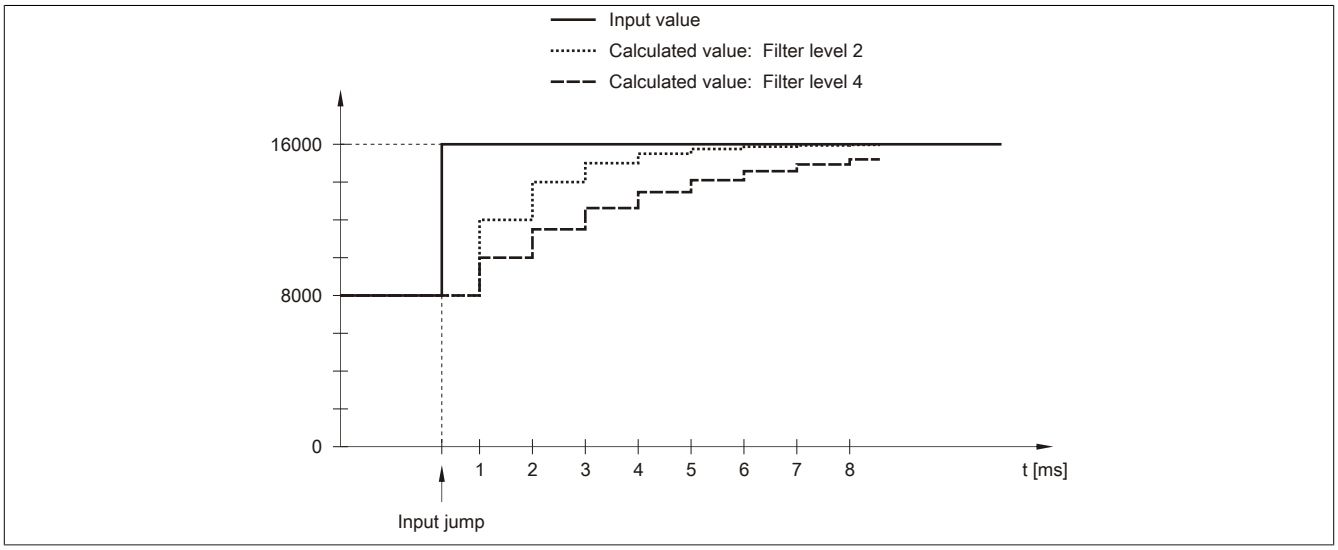


Figure 225: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

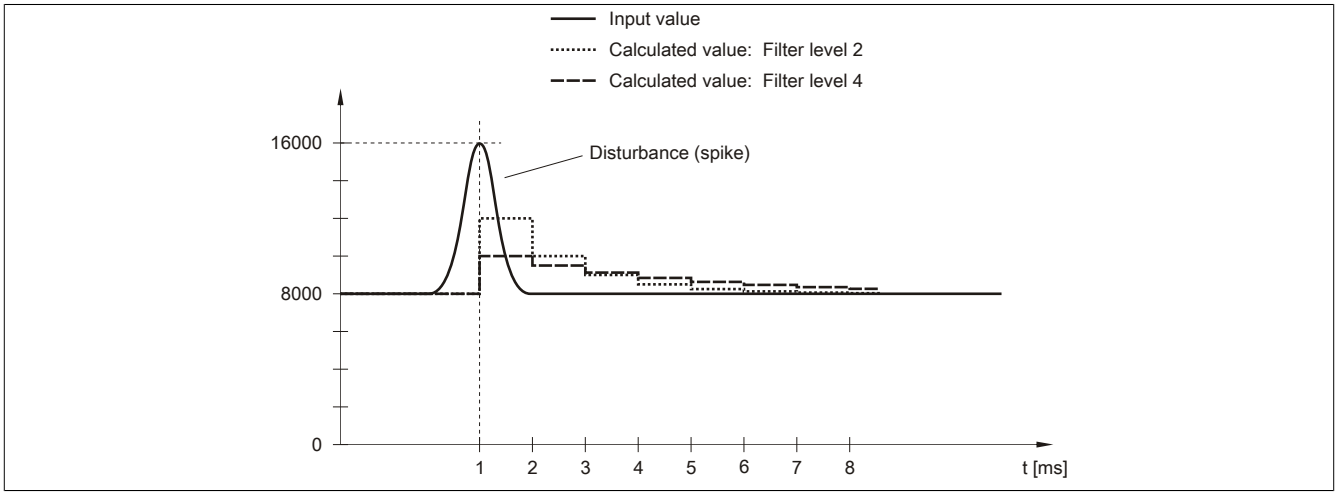


Figure 226: Calculated value during disturbance

Configuring the input filter

Name:
X1CfO_AI1_Filter

X1CfO_AI2_Filter

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

Channel type

Name:
X1CfO_AI_Mode

This register can be used to define the type and range of signal measurement.

Each channel is capable of handling current, voltage or resistance signals. This differentiation is made using multiple connection terminal points and an integrated switch. The switch is automatically activated depending on the specified configuration. The following input signals can be set:

Input signal	On channel
±10 V voltage signal (default)	1 and 2
0 to 20 mA current signal	1 and 2
4 to 20 mA current signal	1 and 2
PT1000 measurement	1
Resistance measurement	1

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Analog input - Channel 1	000	Channel disabled
		001	±10 V voltage signal
		010	0 to 20 mA current signal
		011	4 to 20 mA current signal
		100	PT1000 measurement
		101	Resistance measurement
3	Reserved	0	
4 - 5	Analog input - Channel 2	00	Channel disabled
		01	±10 V voltage signal
		10	0 to 20 mA current signal
		11	4 to 20 mA current signal
6 - 7	Reserved	0	

Limit values

The input signal is monitored at the upper and lower limit values. By default the following limits are set for each mode:

Limit value (default)	Voltage signal ±10 V		Current signal 0 to 20 mA		Current signal 4 to 20 mA	
Upper maximum limit value	10 V	32767 (0x7FFF)	20 mA	32767 (0x7FFF)	20 mA	32767 (0x7FFF)
Lower minimum limit value	-10 V	-32767 (0x8001)	0 mA	0[1)]	4 mA	0[2)]

Table 222: Limit values for voltage and current signals

1) The analog value is limited down to 0.
2) Due to the default limit value, the analog value is limited to a minimum of 0 at currents <4 mA.

Limit value (default)	Temperature measurement		Resistance measurement	
Upper maximum limit value	800.0°C	8000 (0x1F40)	4000.0 Ω	32767 (0x7FFF)
Lower minimum limit value	-200.0°C	-2000 (0xF830)	0 Ω	0

Table 223: Limit values for temperature and resistance measurement

Other limit values can be defined if necessary. These are activated automatically by writing the limit value register (see "Lower limit value" and "Upper limit value"). From this point on, the analog values will be monitored and limited according to the new limits. The results of monitoring are displayed in the status register (see "Input status").

Application example of setting limit values

A negative limit value must be configured in order to measure values <4 mA with a current signal of 4 to 20 mA: 0 mA corresponds to the value -8192 (0xE000).

Lower limit value

Name:
X1CfO_AI1_LowerLim
X1CfO_AI2_LowerLim

These registers can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set (see "Input status").

Data type	Value
INT	-32,768 to 32,767
UINT	0 to 65535

Information:

When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.

Upper limit value

Name:
X1CfO_AI1_UpperLim
X1CfO_AI2_UpperLim

These registers can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set (see "Input status").

Data type	Value
INT	0 to 32,767
UINT	0 to 65535

4.12.2.28.2 Register overview of the I/O data points on the integrated X2 I/O slot

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
X2 - Configuration						
7168	X2CfO_EdgeDetectUnit01Mode	USINT				●
7169	X2CfO_EdgeDetectUnit01Master	USINT				●
7170	X2CfO_EdgeDetectUnit01Slave	USINT				●
7184	X2CfO_EdgeDetectUnit02Mode	USINT				●
7185	X2CfO_EdgeDetectUnit02Master	USINT				●
7186	X2CfO_EdgeDetectUnit02Slave	USINT				●
6144	X2CfO_DI_Filter	USINT				●
6528	X2CfO_CounterMode	USINT				●
6400	X2CfO_Latch01Mode	USINT				●
6401	X2CfO_Latch01Comparator	USINT				●
6416	X2CfO_Latch02Mode	USINT				●
6417	X2CfO_Latch02Comparator	USINT				●
X2 - Communication						
4096	Digital inputs	USINT	●			
	DigitalInput01	Bit 0				
	DigitalInput02	Bit 1				
	DigitalInput03	Bit 2				
	DigitalInput04	Bit 3				
	DigitalInput05	Bit 4				
	DigitalInput06	Bit 5				
	DigitalInput07	Bit 6				
	DigitalInput08	Bit 7				
4097	Digital inputs	USINT	●			
	DigitalInput09	Bit 0				
	DigitalInput10	Bit 1				
	DigitalInput11	Bit 2				
	DigitalInput12	Bit 3				
	DigitalInput13	Bit 4				
	DigitalInput14	Bit 5				
5120	EdgeDetect01Mastertime	DINT	●			
5124	EdgeDetect01Difference	DINT	●			
5128	EdgeDetect01Mastercount	INT	●			
5136	EdgeDetect02Mastertime	DINT	●			
5140	EdgeDetect02Difference	DINT	●			
5144	EdgeDetect02Mastercount	INT	●			
4384	Counter 1	USINT			●	
	Counter01Reset	Bit 0				
	Latch01Enable	Bit 1				
4352	Counter01Value	DINT	●			
4356	Counter01Latch	DINT	●			
4360	Counter01TimeChanged	DINT	●			
4364	Counter01TimeValid	DINT	●			
4368	Latch01Count	SINT	●			
4448	Counter 2	USINT			●	
	Counter02Reset	Bit 0				
	Latch02Enable	Bit 1				
4416	Counter02Value	DINT	●			
4420	Counter02Latch	DINT	●			
4424	Counter02TimeChanged	DINT	●			
4428	Counter02TimeValid	DINT	●			
4432	Latch02Count	SINT	●			

4.12.2.28.2.1 Digital inputs

Unfiltered

The input status is recorded in a 100 µs cycle.

Filtered

The filtered status is transferred in a 100 µs cycle.

Filtering takes place asynchronously in an interval of 100 µs.

Digital input filter

Name:
X2CfO_DI_Filter

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs.

Data type	Value	Filter
USINT	0	No SW filter
	1	0.1 ms
	...	...
	250	25 ms - Higher values are limited to this value

Input state of digital inputs 1 to 14

Name:
DigitalInput01 to DigitalInput14

These registers are used to indicate the input state of digital inputs 1 to 14.

Data type	Value
USINT	See bit structure.

Bit structure of register 4096:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status of digital input 1
...		...	
7	DigitalInput08	0 or 1	Input status of digital input 8

Bit structure of register 4097:

Bit	Name	Value	Information
0	DigitalInput09	0 or 1	Input status of digital input 9
...		...	
5	DigitalInput14	0 or 1	Input status of digital input 14

4.12.2.28.2.2 Edge detection

Digital inputs 11 to 14 can be used for fast edge detection. This runs parallel to all other functions such as counters, etc. This function does not use the digital input filter.

The edge detection function measures edges with µs precision. 2 units are available. A master and a slave edge can be configured for each unit. At each master edge, the timestamp of the master edge and the differential time to the previous slave edge (if present) are logged. A "Master count" can always be utilized to determine how many edges have been detected since the last task class cycle. The timestamp is based on the system time of the CPU.

The combination of rising/falling edges of each channel can be used to configure the following functions for each unit:

Function	Description
Edge time	Measure an edge time
Period duration	Measure the master and differential time
Gate time	Measure the master and differential time
Time offset	Measure the master and differential time of edges on different channels

Edge detection unit - Mode settings

The edge detection unit needs to be configured according to the desired function.

Function	Description
Basic timestamp, master edge mode	The current system time is saved as the master time at the time of the edge.
Timestamp and/or differential time, master and slave edge mode	The slave edge starts the measurement and the system time is saved temporarily. When the master edge occurs, the current system time is saved as the master time and the difference between the master and slave edges is calculated.

Name:
X2CfO_EdgeDetectUnit01Mode
X2CfO_EdgeDetectUnit02Mode

These registers are used to configure the mode of the basic function for either just the master edge or both master and slave edges.

Data type	Value	Information
USINT	0x00	Edge detection disabled on Unit0x: Time measurement not possible
	0x80	Edge detection enabled on Unit0x: Reaction only possible for master edge, no differential measurement possible
	0xC0	Edge detection enabled on Unit0x: Reaction possible for configured master and slave edges

Edge detection unit - Selection of master edge

Name:
X2CfO_EdgeDetectUnit01Master
X2CfO_EdgeDetectUnit02Master

These registers are used to select the source of the master edge for the respective unit. Either the rising or falling edge of one of the 4 fast digital input channels can be selected. Only one edge can be selected for each unit.

Data type	Value	Information
USINT	0	Digital input channel 11: Rising edge
	2	Digital input channel 12: Rising edge
	4	Digital input channel 13: Rising edge
	6	Digital input channel 14: Rising edge
	1	Digital input channel 11: Falling edge
	3	Digital input channel 12: Falling edge
	5	Digital input channel 13: Falling edge
	7	Digital input channel 14: Falling edge

Edge detection unit - Selection of slave edge

Name:
X2CfO_EdgeDetectUnit01Slave
X2CfO_EdgeDetectUnit02Slave

These registers are used to select the source of the slave edge for the respective unit. Either the rising or falling edge of one of the 4 fast digital input channels can be selected. Only one edge can be selected for each unit.

Data type	Value	Information
USINT	0	Digital input channel 11: Rising edge
	2	Digital input channel 12: Rising edge
	4	Digital input channel 13: Rising edge
	6	Digital input channel 14: Rising edge
	1	Digital input channel 11: Falling edge
	3	Digital input channel 12: Falling edge
	5	Digital input channel 13: Falling edge
	7	Digital input channel 14: Falling edge

Edge detection unit - Master edge counter

Name:
EdgeDetect01Mastercount
EdgeDetect02Mastercount

These registers hold the counter values of the detected master edges. The counter value is used to detect new measurements.

Data type	Value	Information
INT	-32,768 to 32,767	Running counter: Number of detected master edges

Edge detection unit - Master edge timestamp

Name:
EdgeDetect01Mastertime
EdgeDetect02Mastertime

The exact CPU system time of the respective unit is saved to these registers when a master edge occurs. If multiple master edges occur within a single cycle (task class), then the time of the last edge is shown.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	CPU system time of master edge [µs]

Edge detection unit - Time difference

Name:
EdgeDetect01Difference
EdgeDetect02Difference

The difference between the master edge and the slave edge of the respective unit is saved to these registers. If multiple measurement periods are completed within a single cycle (task class), then the time difference from the last period is shown.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Time difference between master edge and slave edge [µs]

4.12.2.28.2.3 Counter functions

Fast digital inputs 11 to 14 can be used for counter functions. This function does not use the digital input filter. The following functions are available. Only one of these basic configurations can be enabled at a time:

- 2x event counter with latch function
- 2x AB incremental counter without latch function
- DF counter function
- ABR counter function

Configuring the counter function

The following counter functions can be configured:

Counter function	Description
2x event counter with latch function	Input 11 for event counter 1 and input 13 for event counter 2 can be used simultaneously as event counters. Both rising and falling edges are counted. The latch function of all 4 inputs can be used.
2x AB incremental counter without latch function	Inputs 11 and 12 as AB counter 1 and inputs 13 and 14 as AB counter 2. Since no more fast inputs are available, the latch function is not available.
DF counter: Direction/Frequency with latch function	The D, F and R signals are linked to inputs 11, 12 and 13. Signal D defines the positive (Level = 0) or negative (Level = 1) counting direction. The latch function of all 4 inputs can be used.
ABR counter with latch function	The A, B and R signals are linked to inputs 11, 12 and 13. The latch function of all 4 inputs can be used.

Name:
X2CfO_CounterMode

This register configures the counter function:

Data type	Value	Information
USINT	0	2x event counter with latch function
	1	2x AB incremental counter without latch function
	2	DF counter with latch function
	3	ABR counter with latch function

Configuring the mode of the latch function

Name:
X2CfO_Latch01Mode
X2CfO_Latch02Mode

This register sets the mode of the latch function. The following latch functions can be configured:

Latch function	Description
Single shot latch mode	The latch function must be enabled/set. After a successful latch procedure the function must first be reset. Then it can be enabled again.
Continuous latch mode	The latch function only has to be enabled/set as long as latching is desired.

A changed counter value on "LatchCount" indicates that the latch procedure has been performed (see "Counter value of latch events"). The counter value is stored in the latch register (see "Latched counter value").

Data type	Value	Information
USINT	0	Single shot latch mode
	1	Continuous latch mode

Configuring the latch signals

Name:
X2CfO_Latch01Comparator
X2CfO_Latch02Comparator

This register defines the inputs and their level for triggering the latch procedure.

- This defines which inputs are linked to generate the latch event. All 4 digital input signals can be used for an "AND" connection.
- The "active voltage level" needed for the latch procedure can be defined to adjust for the physical signals. It is not possible to configure a high and low level at the same time.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Value	Information
0	0	Input 11 high level disabled
	1	Input 11 high level enabled for comparator
1	0	Input 12 high level disabled
	1	Input 12 high level enabled for comparator
2	0	Input 13 high level disabled
	1	Input 13 high level enabled for comparator
3	0	Input 14 high level disabled
	1	Input 14 high level enabled for comparator
4	0	Input 11 low level disabled
	1	Input 11 low level enabled for comparator
5	0	Input 12 low level disabled
	1	Input 12 low level enabled for comparator
6	0	Input 13 low level disabled
	1	Input 13 low level enabled for comparator
7	0	Input 14 low level disabled
	1	Input 14 low level enabled for comparator

Clear counter value and enable/disable latch function

Name:
Counter01Reset
Counter02Reset
Latch01Enable
Latch02Enable

The respective bits in these registers clear the counter value or start the latch procedure.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Counter0xReset	0	Do not reset the counter
		1	Reset the counter
1	Latch0xEnable	0	Do not latch the counter
		1	Latch the counter
2 - 7	Reserved	0	

Counter value

Name:
Counter01Value
Counter02Value

The current counter values are saved in these registers.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Current counter value

Latched counter value

Name:
Counter01Latch
Counter02Latch

As soon as the latch conditions have been met, the value of the respective counter is copied to these registers.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Latched counter value

Counter value of latch events

Name:
Latch01Count
Latch02Count

These registers hold the counter values of the latch events. This allows detection of whether a new latched counter value has been saved.

Data type	Value	Information
DINT	-128 to 127	Running counter: Number of detected latch events

Timestamp of last counter change

Name:
Counter01TimeChanged
Counter02TimeChanged

The CPU system time at the time of the last change to the counter value is saved in these registers.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	The CPU system time at the time of the last change to the counter value

Timestamp of last valid counter value

Name:
Counter01TimeValid
Counter02TimeValid

The CPU system time at the time of the last valid counter value is saved in these registers.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	CPU system time of current counter value

4.12.2.28.3 Register overview of the I/O data points on the integrated X3 I/O slot

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
X3 - Configuration						
10240	X3CfO_DI_Filter	USINT				•
10752	X3CfO_Mov01Mode	USINT				•
10756	X3CfO_Mov01SpeedLimit	UDINT				•
10768	X3CfO_Mov02Mode	USINT				•
10772	X3CfO_Mov02SpeedLimit	UDINT				•
12032	X3CfO_PhyIOConfigCh01	USINT				•
12033	X3CfO_PhyIOConfigCh02	USINT				•
12034	X3CfO_PhyIOConfigCh03	USINT				•
12035	X3CfO_PhyIOConfigCh04	USINT				•
12036	X3CfO_PhyIOConfigCh05	USINT				•
12037	X3CfO_PhyIOConfigCh06	USINT				•
12038	X3CfO_PhyIOConfigCh07	USINT				•
12039	X3CfO_PhyIOConfigCh08	USINT				•
12040	X3CfO_PhyIOConfigCh09	USINT				•
12041	X3CfO_PhyIOConfigCh10	USINT				•
12042	X3CfO_PhyIOConfigCh11	USINT				•
12043	X3CfO_PhyIOConfigCh12	USINT				•
X3 - Communication						
8192	Digital inputs	USINT	•			
	DigitalInput05	Bit 0				
	DigitalInput06	Bit 1				
	DigitalInput07	Bit 2				
	DigitalInput08	Bit 3				
8208	Digital outputs	USINT			•	
	DigitalOutput01	Bit 0				
	DigitalOutput02	Bit 1				
	DigitalOutput03	Bit 2				
	DigitalOutput04	Bit 3				
	DigitalOutput05	Bit 4				
	DigitalOutput06	Bit 5				
	DigitalOutput07	Bit 6				
	DigitalOutput08	Bit 7				
8209	Digital outputs	USINT			•	
	DigitalOutput09	Bit 0				
	DigitalOutput10	Bit 1				
	DigitalOutput11	Bit 2				
	DigitalOutput12	Bit 3				
8193	Status feedback	USINT	•			
	StatusDigitalOutput01	Bit 0				
	StatusDigitalOutput02	Bit 1				
	StatusDigitalOutput03	Bit 2				
	StatusDigitalOutput04	Bit 3				
	StatusDigitalOutput05	Bit 4				
	StatusDigitalOutput06	Bit 5				
	StatusDigitalOutput07	Bit 6				
	StatusDigitalOutput08	Bit 7				
8194	Status feedback	USINT	•			
	StatusDigitalOutput09	Bit 0				
	StatusDigitalOutput10	Bit 1				
	StatusDigitalOutput11	Bit 2				
	StatusDigitalOutput12	Bit 3				
4864	PWMPeriod09	UINT			•	
4866	PWMOutput09	INT			•	
4880	PWMPeriod10	UINT			•	
4882	PWMOutput10	INT			•	
4896	PWMPeriod11	UINT			•	
4898	PWMOutput11	INT			•	
4912	PWMPeriod12	UINT			•	
4914	PWMOutput12	INT			•	
8704	Movement 1	USINT			•	
	Mov01Enable	Bit 1				
8706	Mov01Speed	INT			•	
8708	Mov01Position	DINT	•			
8720	Movement 2	USINT			•	
	Mov02Enable	Bit 2				
8722	Mov02Speed	INT			•	
8724	Mov02Position	DINT	•			
8196	StatusInput01	BOOL	•			

4.12.2.28.3.1 Physical configuration of I/O channels

These registers are used to define the functionality of the channels. Depending on the desired configuration, the following assignments can be made with respect to the existing software and hardware:

- A physical configuration as input or output for mixed channels
- An explicit assignment as direct I/O channel: i.e. digital input or digital output
- An explicit assignment as PWM output
- An explicit assignment as D or F movement output

Physical configuration

Name:
X3CfO_PhyIOConfigCh01 to X3CfO_PhyIOConfigCh12

These registers are used to configure the functionality of the channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Name:
X3CfO_PhyIOConfigCh01 to X3CfO_PhyIOConfigCh04

Channels 1 to 4 are digital outputs and can only be used as direct I/O channel.

Bit	Description	Value	Information
0 - 7		0	Direct I/O operation of output

Name:
X3CfO_PhyIOConfigCh05 to X3CfO_PhyIOConfigCh08

Channels 5 to 8 are digital mixed channels and can be configured as either input or output.

Bit	Description	Value	Information
0 - 1		00	Configured as digital output
		01	Reserved
		10	Reserved
		11	Configured as digital input
2 - 7		0	Direct I/O operation of output

Name:
X3CfO_PhyIOConfigCh09 to X3CfO_PhyIOConfigCh12

Channels 9 to 12 are fast digital outputs and can be configured as direct I/O, PWM or movement channels.

Bit	Description	Value	Information
0 - 3	Reserved	0	
4 - 5		00	Direct I/O operation of output
		01	Output operated as PWM
		10	Reserved
		11	Output operated as D/F movement
6 - 7	Reserved	0	

4.12.2.28.3.2 Monitoring of the I/O supply voltage

Name:
StatusInput01

The status of the I/O supply voltage is shown in this register.

Data type	Value	Information
USINT	0	I/O supply voltage within permitted range
	1	I/O supply voltage not connected or outside of the permitted range

4.12.2.28.3.3 Digital inputs

Unfiltered

The input status is recorded in a 100 µs cycle.

Filtered

The filtered status is transferred in a 100 µs cycle.

Filtering takes place asynchronously in an interval of 100 µs.

Digital input filter

Name:
X3CfO_DI_Filter

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs.

Data type	Value	Filter
USINT	0	No SW filter
	1	0.1 ms
	...	...
	250	25 ms - Higher values are limited to this value

Input state of digital inputs 5 to 8

Name:
DigitalInput05 to DigitalInput08

This register is used to indicate the input state of digital inputs 5 to 8.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput05	0 or 1	Input status of digital input 5
...		...	
3	DigitalInput08	0 or 1	Input status of digital input 8

4.12.2.28.3.4 Digital outputs

The output status is processed in a 100 µs cycle.

Switching state of digital outputs 1 to 12

Name:
DigitalOutput01 to DigitalOutput12

These registers are used to store the switching state of digital outputs 1 to 12.

Data type	Value
USINT	See bit structure.

Bit structure:

Register 8208:

Bit	Description	Value	Information
0	DigitalOutput01	0	Digital output 1 reset
		1	Digital output 1 set
...		...	
7	DigitalOutput08	0	Digital output 8 reset
		1	Digital output 8 set

Register 8209:

Bit	Description	Value	Information
0	DigitalOutput09	0	Digital output 9 reset
		1	Digital output 9 set
...		...	
3	DigitalOutput12	0	Digital output 12 reset
		1	Digital output 12 set

4.12.2.28.3.5 Monitoring status of the digital outputs

The error states of the outputs must be programmed in the application. The status information that is read is the actual voltage state on the channel (set or reset). The error state is therefore determined by a difference between the data points "DigitalOutputxx" and the corresponding "StatusDigitalOutputxx".

At least 3 system ticks are needed internally to read the output status. This is the reason for the delay after which the earliest possible comparison can be made after a change in the status of the output.

The digital input filter is not applied to this status information.

Status of digital outputs 1 to 12

Name:
StatusDigitalOutput01 to StatusDigitalOutput12

These registers are used to indicate the status of digital outputs 1 to 12.

Data type	Value
USINT	See bit structure.

Bit structure:

Register 8193:

Bit	Description	Value	Information
0	StatusDigitalOutput01	0	Channel 1: Digital output reset or short circuit
		1	Channel 1: Digital output set or voltage feedback
...		...	
7	StatusDigitalOutput08	0	Channel 8: Digital output reset or short circuit
		1	Channel 8: Digital output set or voltage feedback

Register 8194:

Bit	Description	Value	Information
0	StatusDigitalOutput09	0	Channel 9: Digital output reset or short circuit
		1	Channel 9: Digital output set or voltage feedback
...		...	
3	StatusDigitalOutput12	0	Channel 12: Digital output reset or short circuit
		1	Channel 12: Digital output set or voltage feedback

4.12.2.28.3.6 Pulse width modulation (PWM) function

Digital inputs 9 to 12 can be configured as PWM outputs. Two data points are available per channel for controlling the PWM signal.

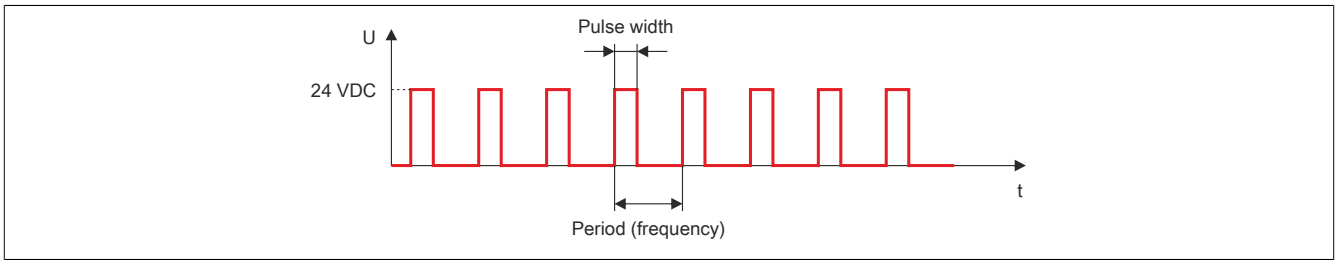


Figure 227: The PWM signal is controlled by setting the pulse width and the duration of the period

Period duration of the PWM outputs

Name:
PWMPeriod09 to PWMPeriod12

These registers are used to define the duration of the period, i.e. the time base for the respective PWM output. This time represents the 100% value, which can be resolved to 0.1% through the duty cycle.

Data type	Value	Information
UINT	5 to 65,535	Duration of period, between 5 and 65535 µs: Corresponds to a frequency of 200 kHz to ≈15 Hz

Duty cycle of the PWM outputs

Name:
PWMOutput09 to PWMOutput12

These registers output the duty cycle of the respective PWM output in a resolution of 0.1% of the period.

Data type	Value	Information
INT	0 to 1000	Duty cycle of the output in 0 to 100.0%

Example: Period duration T [µs] with a duty cycle of 25% equals a duty time of t_1 [µs].

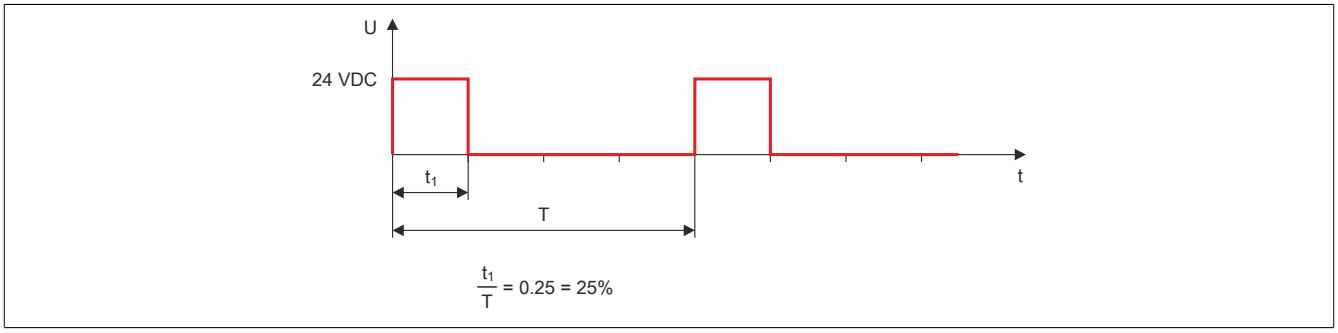


Figure 228: Duty time as a function of the period and the duty cycle

4.12.2.28.3.7 DF movement generator function

Digital output channels 9 to 12 can be configured as 2 independently functioning movement generators (Direction/Frequency) for stepper motor control. The movement generators are assigned to the following channels:

Movement generator	Channel	Function
1	DO 9	D: Direction
	DO 10	F: Frequency
2	DO 11	D: Direction
	DO 12	F: Frequency

The frequency is output via the respective F channel, and the direction is output via the respective D channel. The switchover between directions (movement/counter) takes place via the sign of the speed setpoint.

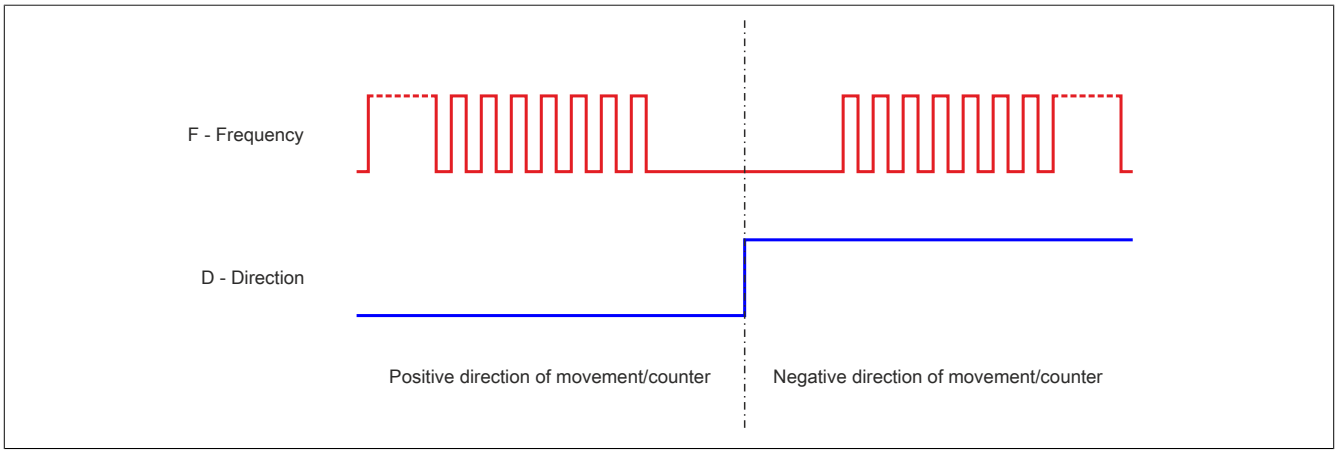


Figure 229: Frequency output via F channel, direction output via D channel

The respective output must be configured correctly in order to completely process the movement function (see "Physical configuration").

The data points described below are available for configuring and controlling the respective movements.

Configuring the movement mode

Name:
X3Cfo_Mov01Mode
X3Cfo_Mov02Mode

These registers are used to configure how the speed setpoint is interpreted. The difference between the two modes is whether edges or periods are output for each increment of the setpoint.

Data type	Value	Information
USINT	0	Edge mode: Each increment generates an edge on the output
	1	Pulse mode: Each increment generates a period on the output

Edge mode

4 increments of the speed setpoint correspond to 2 periods on the output:

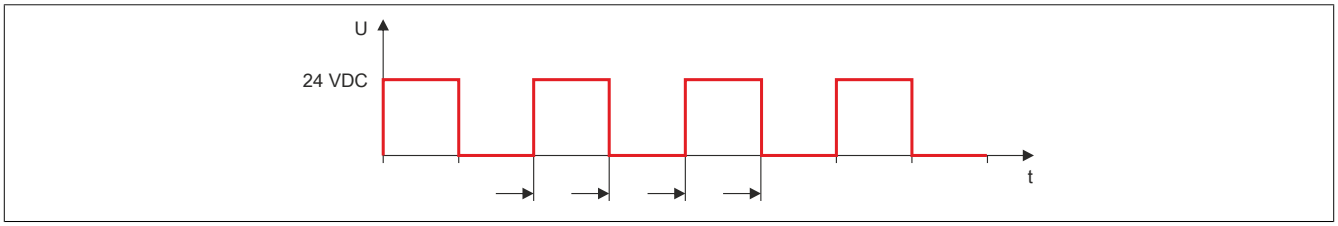


Figure 230: Interpretation of the speed setpoint with edge output for each increment

Pulse mode

2 increments of the speed setpoint correspond to 2 periods on the output:

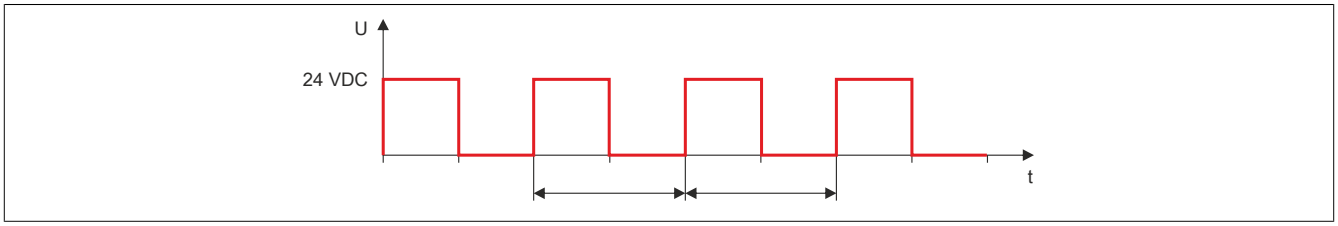


Figure 231: Interpretation of the speed setpoint with period output for each increment

Configuring the maximum speed of the movement

The maximum speed or output frequency of the movement is configured in order to protect the digital output, the actuator/drive being controlled and/or the mechanical system.

Name:
X3Cfo_Mov01SpeedLimit
X3Cfo_Mov02SpeedLimit

These registers are used to configure the maximum speed / output frequency permitted in the system. It is important that the limit values for edge and pulse mode are different.

Edge mode

Data type	Value	Information
UDINT	10 to 400,000	Speed [increments per second]

Pulse mode

Data type	Value	Information
UDINT	5 to 200,000	Speed [increments per second]

Activates the movement

When a movement is active, the two channels are operated according to the preset values.

Name:
Mov01Enable
Mov02Enable

These registers are used to enable or disable the movement function.

Mov01Enable

Data type	Value	Information
USINT	0	Movement 1 disabled
	2	Movement 1 enabled: The speed setpoint is evaluated

Mov02Enable

Data type	Value	Information
USINT	0	Movement 2 disabled
	4	Movement 2 enabled: The speed setpoint is evaluated

Speed and direction control of the movement

The following parameters are important for speed and direction control of the movement:

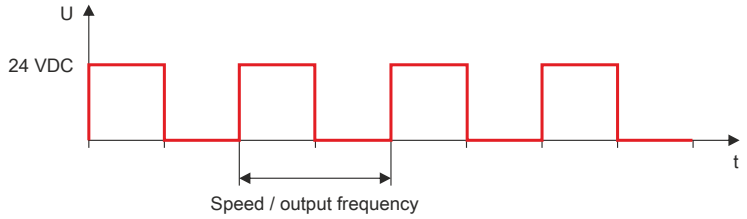
Characteristic value	Description
Speed control	The joint axes receive this speed setpoint from the standard application. 0 to ±32767 correspond to 0 to ±100% of the configured maximum speed
Direction control	The direction of movement is defined by the sign of the speed setpoint: 0 to +32767 correspond to 0 to the maximum speed in the positive direction of movement 0 to -32767 correspond to 0 to the maximum speed in the negative direction of movement
Resolution of the speed setpoint	The resolution of the speed setpoint is: Maximum speed / 32767
Relationship: Speed / Frequency	The relationship between speed and output frequency is: (Speed setpoint / Maximum speed) * 32767 

Table 224: Parameters for speed and direction control of the movement

Name:
Mov01Speed
Mov02Speed

These registers are used to set the speed of the movement.

Data type	Value	Information
INT	0 to 32,767	Speed setpoint 0 to 100%: Movement output F = 0 to maximum speed
		Positive direction of movement: Movement output D = 0
	0 to -32,767	Speed setpoint 0 to 100%: Movement output F = 0 to maximum speed
		Negative direction of movement: Movement output D = 1

Position feedback for movement

The position feedback is represented by a fixed point value [16.16]:

- HighWord = whole number increments
- LowWord = positions after the decimal of the increments

Name:
Mov01Position
Mov02Position

These registers show the current position of the movement.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Position value in fixed point format [16.16]

4.12.3 X20CP1483 and X20CP1483-1

4.12.3.1 General information

The x86 100 MHz-compatible X20CP1483 is the entry-level X20 CPU. With an optimal price/performance ratio, it has the same basic features as the larger CPUs and offers sufficient performance for most standard applications.

USB and Ethernet are included in every CPU. In addition, every CPU has a POWERLINK connection for real-time communication.
In addition, a multi-purpose slot is provided for an additional interface module.

- Intel x86 100 MHz-compatible with additional I/O processor
- Ethernet, POWERLINK V1/V2 and USB onboard
- Modular expansion of interfaces
- CompactFlash as removable application memory
- Fanless
- Extremely compact

4.12.3.2 Order data - X20CP148x

Model number	Short description
	X20 CPUs
X20CP1483	X20 CPU, x86 100 MHz Intel compatible, 32 MB DRAM, 128 kB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1483-1	X20 CPU, x86 100 MHz Intel compatible, 64 MB DRAM, 128 kB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
	Required accessories
	CompactFlash cards
0CFCRD.0128E.01	CompactFlash 128 MB WD extended temp.
0CFCRD.0512E.01	CompactFlash 512 MB WD extended temp.
5CFCRD.016G-06	CompactFlash 16 GB B&R (SLC)
5CFCRD.0512-06	CompactFlash 512 MB B&R (SLC)
5CFCRD.1024-06	CompactFlash 1 GB B&R (SLC)
5CFCRD.2048-06	CompactFlash 2 GB B&R (SLC)
5CFCRD.4096-06	CompactFlash 4 GB B&R (SLC)
5CFCRD.8192-06	CompactFlash 8 GB B&R (SLC)
	Optional accessories
	Batteries
0AC201.91	Lithium batteries 4 pcs., 3 V / 950 mAh button cell We hereby state that the lithium cells contained in this shipment qualify as "partly regulated". Handle with care. If the package is damaged, inspect the cells, repack intact cells and protect cells against short circuits. For emergency information, call RENATA SA at + 41 61 319 28 27
4A0006.00-000	Lithium battery, 3 V / 950 mAh, button cell

Table 225: X20CP1483, X20CP1483-1 - Order data

Included in delivery

Model number	Short description
4A0006.00-000	Backup battery (see also section 4.12.3.19 "Exchanging the lithium battery")
-	Interface module slot covers
X20AC0SR1	X20 locking plate, right
X20TB12	X20 terminal block, 12-pin, 24 V keyed

Table 226: X20 CPUs - Contents of delivery

4.12.3.3 Technical data - X20CP148x

Product ID	X20CP1483	X20CP1483-1
Short description		
Interfaces	1x RS232, 1x Ethernet, 1x POWERLINK (V1/V2), 2x USB, 1x X2X Link	
System module	CPU	
General information		
Cooling	Fanless	
B&R ID code	0xA239	0xAEC5
Status indicators	CPU function, overtemperature, Ethernet, POWERLINK, CompactFlash, battery	
Diagnostics		
Battery	Yes, using status LED and software	
CPU function	Yes, using status LED	
CompactFlash	Yes, using status LED	
Ethernet	Yes, using status LED	
POWERLINK	Yes, using status LED	
Overtemperature	Yes, using status LED	
ACOPOS capability	Yes	
Visual Components support	Yes	
Power consumption without memory card, interface module and USB	6 W	
Internal power consumption of the X2X Link and I/O supply [1]		
Bus	1.42 W	
Internal I/O	0.6 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
IF1 - IF2	Yes	
IF1 - IF3	Yes	
IF1 - IF4	No	
IF1 - IF5	No	
IF1 - IF6	Yes	
IF2 - IF3	Yes	
IF2 - IF4	Yes	
IF2 - IF5	Yes	
IF2 - IF6	Yes	
IF3 - IF4	Yes	
IF3 - IF5	Yes	
IF3 - IF6	Yes	
IF4 - IF5	No	
IF4 - IF6	Yes	
IF5 - IF6	Yes	
PLC - IF1	No	
PLC - IF2	Yes	
PLC - IF3	Yes	
PLC - IF4	No	
PLC - IF5	No	
PLC - IF6	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	
GL	Yes	
GOST-R	Yes	
CPU and X2X Link supply		
Input voltage	24 VDC -15% / +20%	
Input current	Max. 2.2 A	
Fuse	Integrated, cannot be replaced	
Reverse polarity protection	Yes	
X2X Link supply output		
Nominal output power	7 W [3]	
Parallel operation	Yes [4]	
Redundant operation	Yes	
Input I/O supply		
Input voltage	24 VDC -15% / +20%	
Fuse	Required line fuse: Max. 10 A, slow-blow	
Output I/O supply		
Rated output voltage	24 VDC	
Permitted contact load	10 A	
Supply - General information		
Status indicators	Overload, operating status, module status, RS232 data transfer	

Table 227: X20CP1483, X20CP1483-1 - Technical data

Product ID	X20CP1483	X20CP1483-1
Diagnostics		
RS232 data transfer	Yes, using status LED	
Module run/error	Yes, using status LED and software	
Overload	Yes, using status LED and software	
Electrical isolation		
I/O feed - I/O supply	No	
CPU/X2X Link feed - CPU/X2X Link supply	Yes	
Controller		
CompactFlash slot	1	
Real-time clock	Nonvolatile, 1 s resolution, -10 to 10 ppm accuracy at 25°C	
FPU	Yes	
Processor		
Type	x86 100 comp.	
Clock frequency	100 MHz	
L2 cache	-	
L1 cache for data and program code	16 kB	
Integrated I/O processor	Processes I/O data points in the background	
Modular interface slots	1	
Remanent variables	Max. 32 kB [5]	
Shortest task class cycle time	1 ms	
Typical instruction cycle time	0.09 µs	
Data buffering		
Battery monitoring	Yes	
Lithium battery	At least 3 years	
Standard memory		
RAM	32 MB SDRAM	64 MB SDRAM
User RAM	128 kB SRAM [6]	
Interfaces		
IF1 interface		
Signal	RS232	
Design	Connection made using 12-pin X20TB12 terminal block	
Max. distance	900 m	
Transfer rate	Max. 115.2 kbit/s	
IF2 interface		
Signal	Ethernet	
Design	1x RJ45 shielded	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	10/100 Mbit/s	
Transmission		
Physical layer	10 BASE-T/100 BASE-TX	
Half-duplex	Yes	
Full-duplex	Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
IF3 interface		
Fieldbus	POWERLINK (V1/V2) managing or controlled node	
Type	Type 4 [7]	
Design	1x RJ45 shielded	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100 BASE-TX	
Half-duplex	Yes	
Full-duplex	POWERLINK mode: No / Ethernet mode: Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
IF4 interface		
Type	USB 1.1	
Design	Type A	
IF5 interface		
Type	USB 1.1	
Design	Type A	
IF6 interface		
Fieldbus	X2X Link master	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	

Table 227: X20CP1483, X20CP1483-1 - Technical data

Product ID	X20CP1483	X20CP1483-1
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order application memory (CompactFlash) separately Backup battery included in delivery X20 locking plate (right) included in delivery X20 terminal block (12-pin) included in delivery Interface module slot covers included in delivery	
Dimensions		
Width	150 mm	
Height	99 mm	
Depth	85 mm	
Weight	300 g	

Table 227: X20CP1483, X20CP1483-1 - Technical data

1) The specified values are maximum values. The exact calculation is included as a data sheet in the module documentation and can be downloaded from the B&R website.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) When operated at temperatures above 55°C, a derating of the nominal output power to 5 W for the X2X Link supply must be taken into consideration.
4) In parallel operation, only 75% of the rated power can be assumed. It is important to make sure that all power supplies operated in parallel are switched on and off at the same time.
5) Can be configured in Automation Studio.
6) Minus configured remanent variables.
7) See the POWERLINK help system under "General information, Hardware - IF/LS".

4.12.3.4 X20 CPUs - Status LEDs

Figure	LED	Color	Status	Description
	R/E	Green	On	Application running
			Blinking	Boot mode system start: CPU initializing the application, all bus systems and I/O modules[1)]
		Red	On	SERVICE mode
			Blinking	The "R/E" LED blinks red and the "RDY/F" LED blinks yellow when there is a license violation.
			Double flash	BOOT mode (during firmware update)[1)]
	RDY/F	Yellow	On	SERVICE or BOOT mode
			Blinking	The "RDY/F" LED blinks yellow and the "R/E" LED blinks red when there is a license violation.
	S/E	Green/Red		Status/Error LED. The statuses of this LED are described in section 4.12.3.4.1 ""S/E" LED".
	PLK	Green	On	A link to the POWERLINK peer station has been established.
			Blinking	A link to the POWERLINK peer station has been established. The LED blinks when Ethernet activity is taking place on the bus.
	ETH	Green	On	A link to the peer station has been established.
			Blinking	A link to the peer station has been established. Indicates Ethernet activity is taking place on the bus.
	CF	Green	On	CompactFlash inserted and detected
		Yellow	On	CompactFlash read/write access
	DC	Yellow	On	CPU power supply OK
		Red	On	Backup battery empty

1) The process can take several minutes depending on the configuration.

4.12.3.4.1 "S/E" LED

The Status/Error LED is a green/red dual LED. The LED status can have different meanings depending on the operating mode.

4.12.3.4.1.1 Ethernet mode

In this mode, the interface is operated as an Ethernet interface.

Green - Status	Description
On	Interface being operated as an Ethernet interface

Table 228: Status/Error LED - Ethernet operating mode

4.12.3.4.1.2 POWERLINK V1

Status LED		Status of the POWERLINK node
Green	Red	
On	Off	The POWERLINK node is running with no errors.
Off	On	A system error has occurred. The error type can be read using the PLC logbook. An irreparable problem has occurred. The system cannot properly carry out its tasks. This state can only be changed by resetting the module.
Blinking alternately		The POWERLINK managing node has failed. This error code can only occur when operated as a controlled node. This means that the configured node number lies within the range 0x01 - 0xFD.
Off	Blinking	System failure. The red blinking LED signals an error code (see section 4.12.2.4.2 "System failure error codes").
Off	Off	Module is: • Off • Starting up • Not configured correctly in Automation Studio • Defective

Table 229: Status/Error LED - POWERLINK V1 operating mode

4.12.3.4.1.3 POWERLINK V2

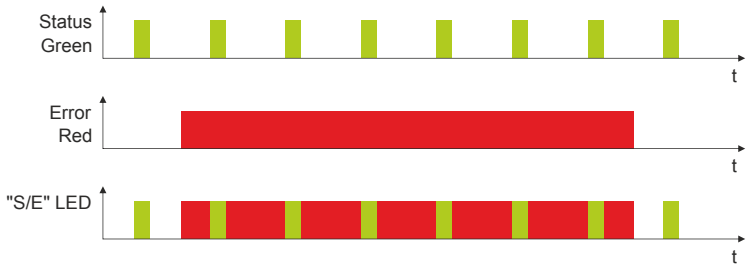
Red - Error	Description
On	The module is in an error mode (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: The LED blinks red several times immediately after startup. This is not an error.

Table 230: Status/Error LED as Error LED - POWERLINK operating mode

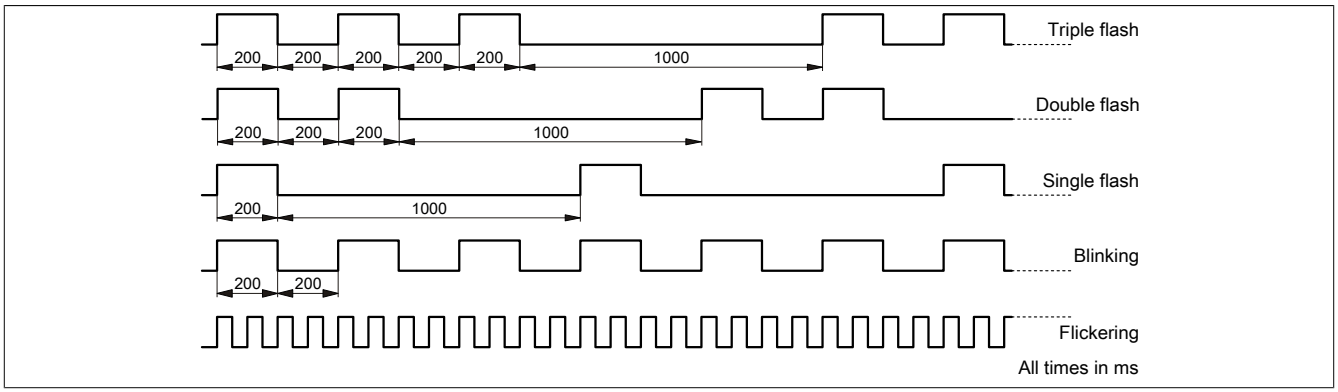
Green - Status	Description
Off	**Mode** The module is in NOT_ACTIVE mode or: • Switched off • Starting up • Not configured correctly in Automation Studio • Defective **Managing node (MN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to PRE_OPERATIONAL_1 mode. If POWERLINK communication is detected before the time expires, however, then the MN will not be started. **Controlled node (CN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to BASIC_ETHERNET mode. If POWERLINK communication is detected before this time expires, however, the module switches immediately to PRE_OPERATIONAL_1 mode.
Green flickering (approx. 10 Hz)	**Mode** The module is in BASIC_ETHERNET mode. The interface is being operated as an Ethernet TCP/IP interface. **Managing node (MN)** This state can only be changed by resetting the module. **Controlled node (CN)** If POWERLINK communication is detected while in this state, the module will transition to the PRE_OPERATIONAL_1 state.
Single flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_1 mode. **Managing node (MN)** The MN starts "reduced cycle" operation. Cyclic communication is not yet taking place. **Controlled node (CN)** The module can be configured by the MN in this state. The CN waits until it receives an SoC frame and then switches to the PRE_OPERATIONAL_2 mode. An LED lit red in this state indicates failure of the MN.

Table 231: Status/Error LED as Status LED - POWERLINK operating mode

Green - Status	Description
Double flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_2 mode. **Managing node (MN)** The MN begins cyclic communication (cyclic input data is not yet being evaluated). The CNs are configured in this state. **Controlled node (CN)** The module can be configured by the MN in this state. A command then switches the module to READY_TO_OPERATE mode. An LED lit red in this mode indicates failure of the MN.
Triple flash (approx. 1 Hz)	**Mode** The module is in the READY_TO_OPERATE state. **Managing node (MN)** Cyclic and asynchronous communication is taking place. Any received PDO data is ignored. **Controlled node (CN)** The configuration of the module is completed. Normal cyclic and asynchronous communication is taking place. The PDO data sent corresponds to the PDO mapping. Cyclic data is not yet being evaluated, however. An LED lit red in this mode indicates failure of the MN.
On	**Mode** The module is in PRE_OPERATIONAL_2 mode. PDO mapping is active and cyclic data is being evaluated.
Blinking (approx. 2.5 Hz)	**Mode** The module is in STOPPED mode. **Managing node (MN)** This status is not possible for the MN. **Controlled node (CN)** No output data is produced or input data supplied. It is only possible to enter or leave this mode after the MN has given the appropriate command.

Table 231: Status/Error LED as Status LED - POWERLINK operating mode

Status LEDs - Blinking patterns



4.12.3.4.2 System failure error codes

Incorrect configuration or defective hardware can cause a system stop error.

The error code is indicated by the red Error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. The error code is output cyclically every 2 seconds.

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	●	●	●	-	Pause	●	●	●	-	Pause
Hardware error: The module or a system component is defective and must be replaced.	-	●	●	-	Pause	-	●	●	-	Pause

Table 232: Status/Error ("S/E") LED - System failure error codes

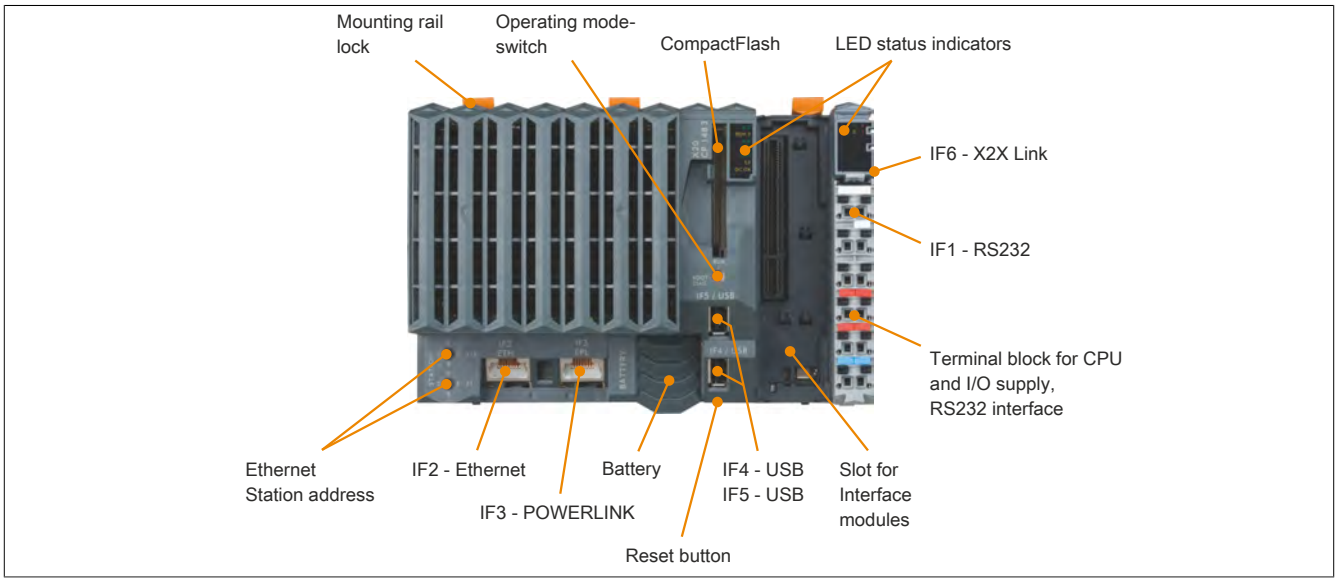
Key:
- ● ... 150 ms
- \- ... 600 ms
- Pause ... 2 second delay

4.12.3.5 LED status indicators for the integrated power supply

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • The X2X Link supply for the power supply is overloaded • I/O supply too low • Input voltage for X2X Link supply too low
	e + r	Red on / Green single flash		Invalid firmware
	S	Yellow	Off	No RS232 activity
			On	The LED lights up when data is being sent or received via the RS232 interface.
	I	Red	Off	The X2X Link supply is within the valid limits
			On	The X2X Link supply for the power supply is overloaded

4.12.3.6 Operating and connection elements



4.12.3.7 Slot for application memory

These CPUs require application memory in order to operate. The application memory is provided in the form of a CompactFlash card. It is not included with the CPUs, but must be ordered separately as an accessory.

Information:

The CompactFlash card must not be removed during operation.

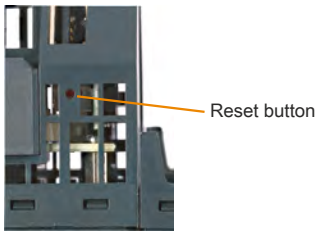
4.12.3.8 Operating mode switch

The operating mode switch is used to set the operating mode.

Switch position	Operating mode	Description
BOOT	BOOT	When the switch is in this position, the default B&R Automation Runtime (AR) system is started and the runtime system can be installed via the online interface (B&R Automation Studio). User flash memory is deleted only after the download begins.
RUN	RUN	RUN mode
DIAG	DIAGNOSE	Boots the CPU in diagnostic mode. Program sections in User RAM and User FlashPROM are not initialized. After diagnostic mode, the CPU always boots with a cold restart.

Table 233: X20 CPUs - Operating modes

4.12.3.9 Reset button



The reset button is located below the USB interfaces on the bottom of the housing. It can be pressed with any small pointed object (e.g. paper clip). Pressing the reset button triggers a hardware reset, which means:

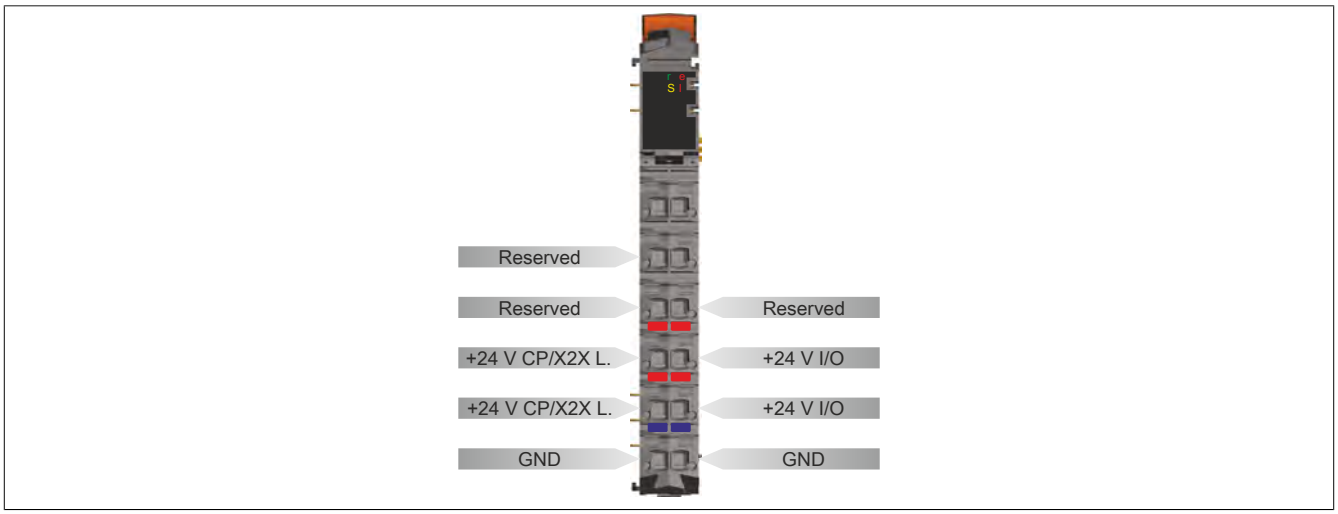
- All application programs are stopped.
- All outputs are set to zero.

The PLC then boots into Service mode by default. The boot mode that follows after pressing the reset button can be defined in Automation Studio.

4.12.3.10 CPU supply

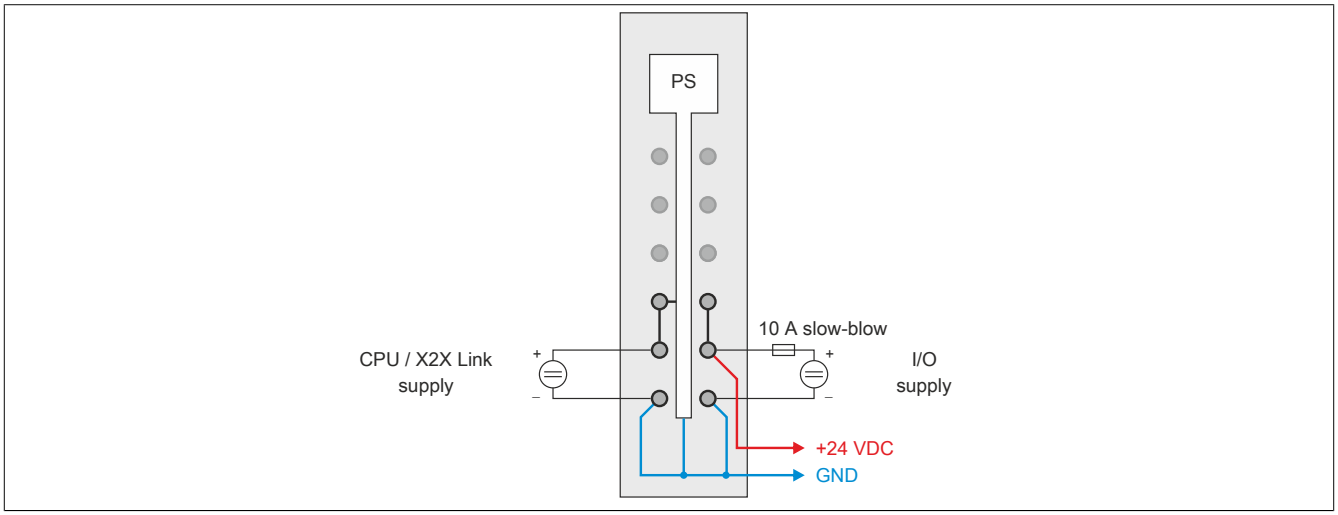
A power supply is integrated in the X20 CPUs. It has a feed for the CPU, the X2X Link and the internal I/O supply. Supply for the CPU and X2X Link is electrically isolated.

Pinout of the integrated power supply

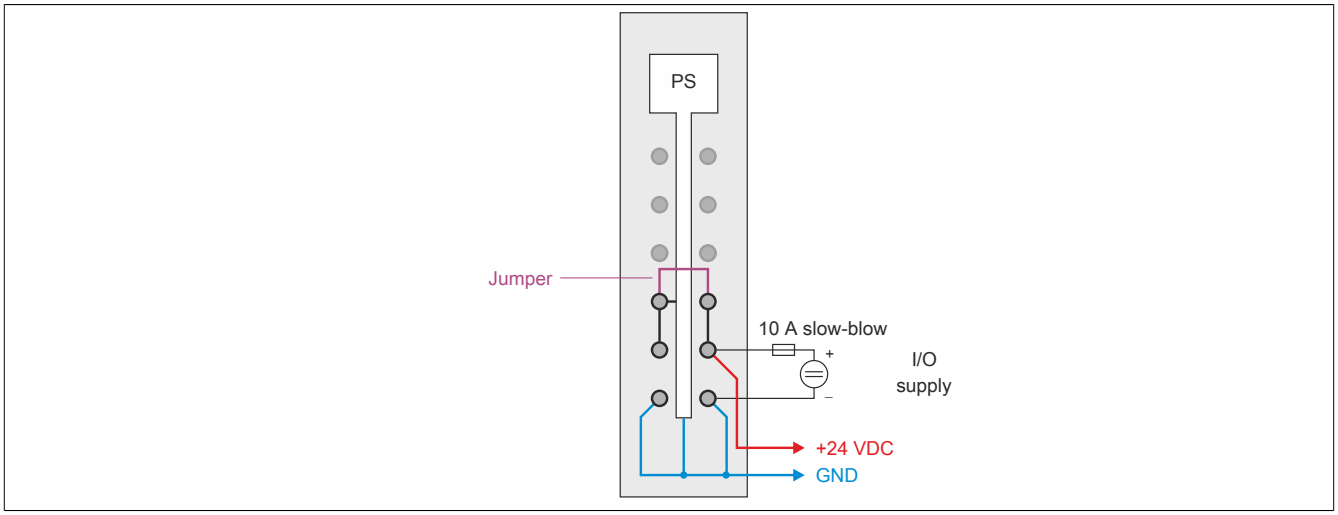


Connection examples

Connection example with 2 separate supplies

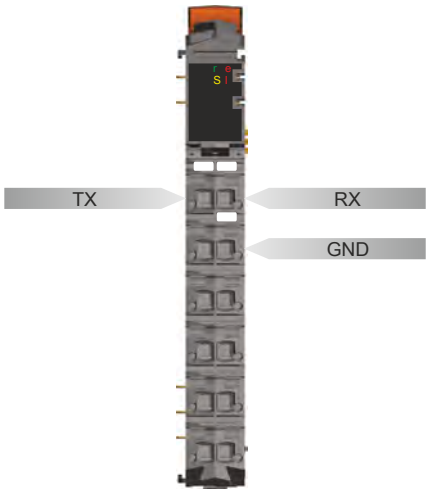


Connection example with a supply and jumper



4.12.3.11 RS232 interface (IF1)

The non-electrically isolated RS232 interface is primarily intended to serve as an online interface for communication with the programming device.



4.12.3.12 Ethernet interface (IF2)

The IF2 is executed as the10 BASE-T / 100 BASE-TX interface.

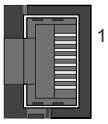
The INA2000 station number of the Ethernet interface is set using the two hex switches.

Information about cabling X20 modules with an Ethernet interface can be found on the B&R website in the module's download section at www.br-automation.com.

Information:

The Ethernet interface (IF2) is not suited for POWERLINK (see 4.12.3.13 "POWERLINK interface (IF3)").

Pinout

Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	TXD	Transmit data
	2	TXD\	Transmit data\
	3	RXD	Receive data
	4	Termination	
	5	Termination	
	6	RXD\	Receive data\
	7	Termination	
	8	Termination	

4.12.3.13 POWERLINK interface (IF3)

POWERLINK V1

Switch position	Description
0x00	Operation as managing node.
0x01 - 0xFD	Node number of the POWERLINK node. Operation as controlled node.
0xFE - 0xFF	Reserved, switch position not permitted

Table 234: POWERLINK V1 - Node numbers

POWERLINK V2

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node.
0xF0	Operation as a managing node.
0xF1 - 0xFF	Reserved, switch position not permitted

Table 235: POWERLINK node number

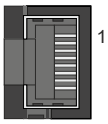
Ethernet mode

Starting with Automation Studio Version V2.5.3 and with Automation Runtime V2.90, the interface can be operated as an Ethernet interface.

The INA2000 station number can be set using the B&R Automation Studio software.

Pinout

Information about cabling X20 modules with an Ethernet interface can be found on the B&R website in the module's download section at www.br-automation.com.

Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.12.3.14 USB interfaces (IF4 and IF5)

IF4 and IF5 are USB interfaces. The connection is made using a USB 1.1 interface.

The USB interfaces can only be used for devices approved by B&R (e.g. floppy disk drive, DiskOnKey or dongle).

Information:

USB interfaces cannot be used for online communication with a programming device.

4.12.3.15 Slots for interface modules

The CPUs have one or three slots for interface modules.

Various bus and network systems can easily be integrated into the X20 system by selecting the corresponding interface module.

4.12.3.16 Overtemperature cutoff

To prevent damage, a shut-off/reset is triggered on the CPU when the processor reaches 100°C.

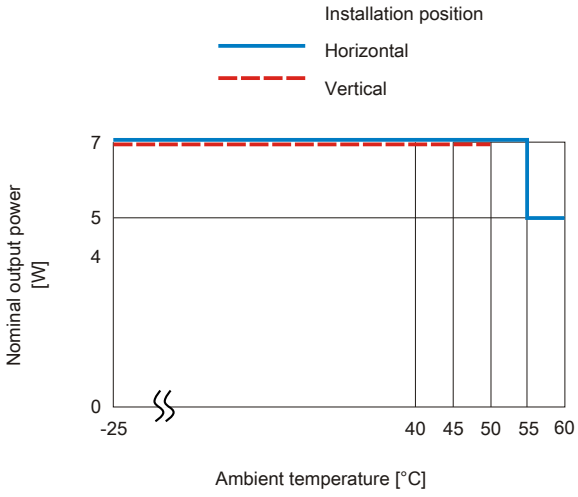
The following errors are entered in the logbook:

Error number	Error description
9204	WARNING: System halted because of temperature check
9210	WARNING: Boot by watchdog or manual reset

Table 236: X20 CPUs - Logbook entries after overtemperature cutoff

4.12.3.17 Derating

There is no derating when operated below 55°C. Above 55°C, the nominal output power for the X2X Link supply must be reduced to 5 W.



4.12.3.18 Data / Real-time clock buffering

The CPUs are buffered by a backup battery. The following areas are buffered:

- Remanent variables
- User RAM
- System RAM
- Real-time clock

Battery monitoring

The battery voltage is checked cyclically. The cyclic load test of the battery does not considerably shorten the battery life, instead it gives an early warning of weakened buffer capacity.

The status information "Battery OK" is available from the system library function "BatteryInfo" and the CPU's I/O mapping.

Replacement interval for battery

The battery should be replaced every 4 years. The replacement intervals recommended by B&R reflect the batteries' average service life and operating conditions. It does not represent the maximum buffer duration.

4.12.3.19 Exchanging the lithium battery

The CPUs have a lithium battery. The lithium battery is found in a separate compartment on the bottom of the module and protected by a cover.

Backup battery data

Model number 4A0006.00-000 0AC201.91	 1 pcs. 4 pcs.
Short description	Lithium battery, 3 V / 950 mAh, button cell
Storage temperature	-20 to 60°C
Storage time	Max. 3 years at 30°C
Relative humidity	0 to 95%, non-condensing

Table 237: X20 CPUs - Backup battery data

Important information about the battery exchange

The product design allows the battery to be changed with the PLC switched either on or off. In some countries, safety regulations do not allow batteries to be changed while the module is switched on. To prevent data loss, the battery must be changed within 1 min. with the power off.

Warning!

The battery must be replaced by a Typ CR2477N Renata battery only. The use of another battery may present a risk of fire or explosion.

The battery may explode if handled improperly. Do not recharge, disassemble or dispose of in fire.

Procedure for exreplacing the battery

1. Touch the mounting rail or ground connection (not the power supply!) in order to discharge any electrostatic charge from your body.
2. Remove the cover for the lithium battery. Do this by sliding it down and away from the CPU.

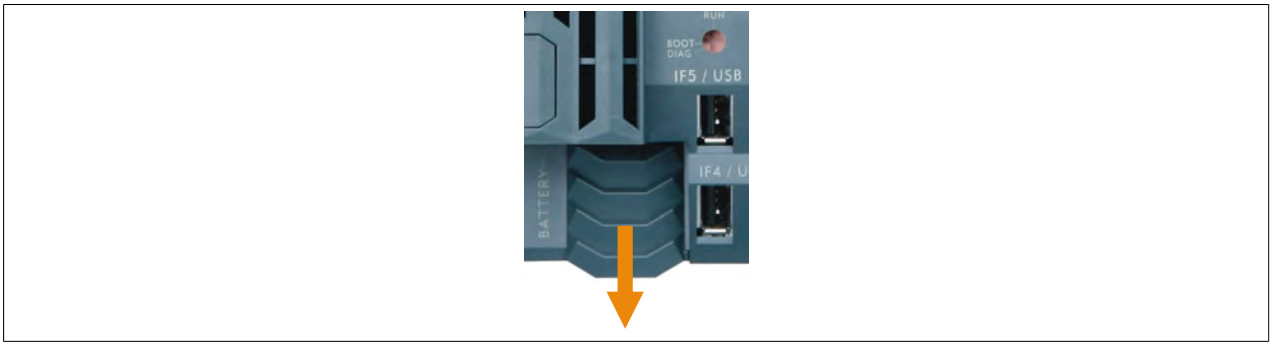


Figure 232: X20 CPUs - Remove lithium battery cover

3. Remove the battery from the holder (do not use pliers or uninsulated tweezers -> risk of short circuiting). The battery should not be held by its edges. **Insulated** tweezers may also be used to remove the battery.

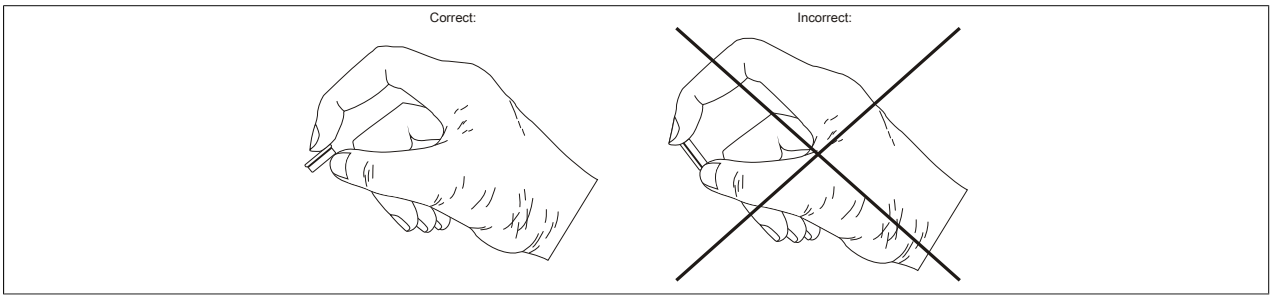


Figure 233: X20 CPUs - Correct grip for the battery

4. Insert the new battery with the correct polarity. To do this, lay the battery with the "+" side up on the right part of the battery holder under the USB interface IF4. Then secure the battery in the holder by pressing above the left part of the battery holder.
5. Replace the cover.

Information:

Lithium batteries are considered hazardous waste. Used batteries should be disposed of in accordance with applicable local regulations.

4.12.3.20 Programming the system flash memory

General information

In order for the application project to be executed on the CPU, the Automation Runtime operating system, the system components and the application project must be installed on the CompactFlash card.

Creating a CompactFlash using a USB card reader

The easiest way to perform an initial installation is by creating a fully programmed CompactFlash card using a USB card reader.

1. Creating and configuring a project in Automation Studio
2. In Automation Studio, select **Tools / Create CompactFlash**
3. In the dialog box that opens, select a CompactFlash card and then generate it
4. Insert the finished CompactFlash into the CPU and turn on the CPU's supply voltage
5. CPU booting

For details about commissioning: See help system under "Automation Software / Getting Started"

Installation over an online connection

The CPUs are delivered with a default B&R Automation Runtime system (with limited functions) already installed. This runtime system is started in Boot mode (operating mode switch in the BOOT position or no CompactFlash / invalid CompactFlash inserted). It initializes the Ethernet interface and onboard serial RS232 interface, making it possible to download a new runtime system.

1. Insert the CompactFlash card and switch on the power to the CPU. When the switch is in the BOOT position, a new or invalid CompactFlash card starts the CPU with the default B&R Automation Runtime system.
2. Establish a physical online connection between the programming device (PC or industrial PC) and the CPU (e.g. over an Ethernet network or the RS232 interface).
3. Before you can establish an online connection via Ethernet, the CPU must be assigned an IP address. In Automation Studio, select **Settings** from the Online menu and then click on the **Browse targets** button to search for B&R target systems on the local network. The CPU should appear in the list. If the CPU has not already received an IP address from a DHCP server, right-click on it and select **Set IP parameters** from the shortcut menu. All necessary network configurations can be made on a temporary basis in this dialog box (should be identical to the settings defined in the project).
4. Configure online connection in B&R Automation Studio. For details about the configuration: See help system under "Automation Software / Communication / Online communication"
5. Start the download procedure by selecting the **Services** command from the **Project** menu. Then select **Transfer Automation Runtime** from the pop-up menu. Now follow the instructions provided by B&R Automation Studio.

4.12.4 X20(c)CP158x and X20(c)CP358x

4.12.4.1 General information

Based on state-of-the-art Intel® ATOM™ processor technology, X20 CPUs cover a wide spectrum of requirements. They can be implemented in solutions ranging from standard applications to those requiring the highest levels of performance.

The series starts with Intel® ATOM™ processor 333 MHz compatible models – X20CP1583 and X20CP3583. With an optimum price/performance ratio, it has the same basic features as all of the larger CPUs.

The basic model includes USB, Ethernet, POWERLINK V1/V2 and replaceable CompactFlash card. The standard Ethernet interface is capable of handling communication in the gigabit range. For improved real-time network performance, the onboard POWERLINK interface supports poll response chaining mode (PRC).
In addition, there are up to three multi-purpose slots for additional interface modules.

- Intel® ATOM™ 1600/1000/600 Performance with integrated I/O processor
- Entry-level CPU is Intel® ATOM™ 333 MHz-compatible with integrated I/O processor
- Ethernet, POWERLINK V1/V2 with poll response chaining and onboard USB
- 1 or 3 slots for modular interface expansion
- CompactFlash as removable application memory
- Up to 512 MB DDR2-SRAM according to performance requirements
- CPU redundancy possible
- Fanless
- Extremely compact

4.12.4.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.12.4.3 Order data - X20CP158x

Model number	Short description
	X20 CPUs
X20CP1583	X20 CPU, ATOM 333 MHz compatible, 128 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1584	X20 CPU, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCP1584	X20 CPU, coated, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1585	X20 CPU, ATOM 1.0 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP1586	X20 CPU, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCP1586	X20 CPU, coated, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
	Required accessories
	CompactFlash cards
0CFCRD.0128E.01	CompactFlash 128 MB WD extended temp.
0CFCRD.0512E.01	CompactFlash 512 MB WD extended temp.
5CFCRD.016G-06	CompactFlash 16 GB B&R (SLC)
5CFCRD.0512-06	CompactFlash 512 MB B&R (SLC)
5CFCRD.1024-06	CompactFlash 1 GB B&R (SLC)
5CFCRD.2048-06	CompactFlash 2 GB B&R (SLC)
5CFCRD.4096-06	CompactFlash 4 GB B&R (SLC)
5CFCRD.8192-06	CompactFlash 8 GB B&R (SLC)
	Optional accessories
	Batteries
0AC201.91	Lithium batteries 4 pcs., 3 V / 950 mAh button cell We hereby state that the lithium cells contained in this shipment qualify as "partly regulated". Handle with care. If the package is damaged, inspect the cells, repack intact cells and protect cells against short circuits. For emergency information, call RENATA SA at + 41 61 319 28 27
4A0006.00-000	Lithium battery, 3 V / 950 mAh, button cell

Table 238: X20CP1583, X20CP1584, X20cCP1584, X20CP1585, X20CP1586, X20cCP1586 - Order data

Included in delivery

Model number	Short description
4A0006.00-000	Backup battery (see also section 4.12.3.19 "Exchanging the lithium battery")
-	Interface module slot covers
X20AC0SR1	X20 locking plate, right
X20TB12	X20 terminal block, 12-pin, 24 V keyed

Table 239: X20 CPUs - Contents of delivery

4.12.4.4 Technical data - X20CP158x

Product ID	X20CP1583	X20CP1584	X20cCP1584	X20CP1585	X20CP1586	X20cCP1586
Short description						
Interfaces	1x RS232, 1x Ethernet, 1x POWERLINK (V1/V2), 2x USB, 1x X2X Link					
System module	CPU					
General information						
Cooling	Fanless					
B&R ID code	0xD45B	0xC370	0xE21B	0xC3AE	0xC3B0	0xE21C
Status indicators	CPU function, overtemperature, Ethernet, POWERLINK, CompactFlash, battery					
Diagnostics						
Battery	Yes, using status LED and software					
CPU function	Yes, using status LED					
CompactFlash	Yes, using status LED					
Ethernet	Yes, using status LED					
POWERLINK	Yes, using status LED					
Overtemperature	Yes, using status LED					
CPU redundancy possible	No					
ACOPOS capability	Yes					
Visual Components support	Yes					
Power consumption without interface module and USB	8.2 W	8.6 W		8.8 W	9.7 W	
Internal power consumption of the X2X Link and I/O supply [1]						
Bus	1.42 W					
Internal I/O	0.6 W					
Additional power dissipation caused by the actuators (resistive) [W]	-					
Electrical isolation						
IF1 - IF2	Yes					
IF1 - IF3	Yes					
IF1 - IF4	No					
IF1 - IF5	No					
IF1 - IF6	Yes					
IF2 - IF3	Yes		-		Yes	-
IF2 - IF4	Yes					
IF2 - IF5	Yes					
IF2 - IF6	Yes		-		Yes	-
IF3 - IF4	Yes					
IF3 - IF5	Yes					
IF3 - IF6	Yes		-		Yes	-
IF4 - IF5	No					
IF4 - IF6	Yes					
IF5 - IF6	Yes					
PLC - IF1	No					
PLC - IF2	Yes					
PLC - IF3	Yes					
PLC - IF4	No					
PLC - IF5	No					
PLC - IF6	Yes					
Certification						
CE	Yes					
cULus	Yes					
ATEX Zone 2 [2]	Yes					
KC	-	Yes	-		Yes	-
GL	Yes					
GOST-R	Yes					
CPU and X2X Link supply						
Input voltage	24 VDC -15% / +20%					
Input current	Max. 1.5 A					
Fuse	Integrated, cannot be replaced					
Reverse polarity protection	Yes					
X2X Link supply output						
Nominal output power	7 W [3]					
Parallel operation	Yes [4]					
Redundant operation	Yes					
Input I/O supply						
Input voltage	24 VDC -15% / +20%					
Fuse	Required line fuse: Max. 10 A, slow-blow					
Output I/O supply						
Rated output voltage	24 VDC					
Permitted contact load	10 A					
Supply - General information						
Status indicators	Overload, operating status, module status, RS232 data transfer					

Table 240: X20CP1583, X20CP1584, X20cCP1584, X20CP1585, X20CP1586, X20cCP1586 - Technical data

Product ID	X20CP1583	X20CP1584	X20cCP1584	X20CP1585	X20CP1586	X20cCP1586
Diagnostics						
RS232 data transfer	Yes, using status LED					
Module run/error	Yes, using status LED and software					
Overload	Yes, using status LED and software					
Electrical isolation						
I/O feed - I/O supply	No					
CPU/X2X Link feed - CPU/X2X Link supply	Yes					
Controller						
CompactFlash slot	1					
Real-time clock	Nonvolatile, 1 s resolution, -10 to 10 ppm accuracy at 25°C					
FPU	Yes					
Processor						
Type		ATOM™ E620T		ATOM™ E640T	Atom™ E680T	
Clock frequency	333 MHz	0.6 GHz		1 GHz	1.6 GHz	
L1 cache						
Data code	24 kB					
Program code	32 kB					
L2 cache	-	512 kB				
Integrated I/O processor	Processes I/O data points in the background					
Modular interface slots	1					
Remanent variables	Max. 64 kB [5]	Max. 256 kB [5]			Max. 1 MB [5]	
Shortest task class cycle time	800 µs	400 µs		200 µs	100 µs	
Typical instruction cycle time	0.01 µs	0.0075 µs		0.0044 µs	0.0027 µs	
Data buffering						
Battery monitoring	Yes					
Lithium battery	Min. 2 years at 23°C ambient temperature					
Standard memory						
RAM	128 MB DDR2 SDRAM	256 MB DDR2 SDRAM			512 MB DDR2 SDRAM	
User RAM	1 MB SRAM [6]					
Interfaces						
IF1 interface						
Signal	RS232					
Design	Connection made using 12-pin X20TB12 terminal block					
Max. distance	900 m					
Transfer rate	Max. 115.2 kbit/s					
IF2 interface						
Signal	Ethernet					
Design	1x shielded RJ45 port					
Cable length	Max. 100 m between 2 stations (segment length)					
Transfer rate	10/100/1000 Mbit/s					
Transmission						
Physical layer	10 BASE-T/100 BASE-TX/1000 BASE-T					
Half-duplex	Yes					
Full-duplex	Yes					
Autonegotiation	Yes					
Auto-MDI / MDIX	Yes					
IF3 interface						
Fieldbus	POWERLINK (V1/V2) managing or controlled node					
Type	Type 4 [7]					
Design	1x shielded RJ45 port					
Cable length	Max. 100 m between 2 stations (segment length)					
Transfer rate	100 Mbit/s					
Transmission						
Physical layer	100 BASE-TX					
Half-duplex	Yes					
Full-duplex	POWERLINK mode: No / Ethernet mode: Yes					
Autonegotiation	Yes					
Auto-MDI / MDIX	Yes					
IF4 interface						
Type	USB 1.1/2.0					
Design	Type A					
IF5 interface						
Type	USB 1.1/2.0					
Design	Type A					
IF6 interface						
Fieldbus	X2X Link master					
Operating conditions						
Mounting orientation						
Horizontal	Yes					
Vertical	Yes					

Table 240: X20CP1583, X20CP1584, X20cCP1584, X20CP1585, X20CP1586, X20cCP1586 - Technical data

Product ID	X20CP1583	X20CP1584	X20cCP1584	X20CP1585	X20CP1586	X20cCP1586
Installation at elevations above sea level						
0 to 2000 m	No limitations					
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m					
EN 60529 protection	IP20					
Environmental conditions						
Temperature						
Operation						
Horizontal installation	-25 to 60°C					
Vertical installation	-25 to 50°C					
Derating	See section "Derating"					
Storage	-40 to 85°C					
Transport	-40 to 85°C					
Relative humidity						
Operation	5 to 95%, non-condensing		Up to 100%, condensing	5 to 95%, non-condensing		Up to 100%, condensing
Storage	5 to 95%, non-condensing					
Transport	5 to 95%, non-condensing					
Mechanical characteristics						
Note	Order application memory (CompactFlash) separately Backup battery included in delivery X20 locking plate (right) included in delivery X20 terminal block (12-pin) included in delivery Interface module slot covers included in delivery					
Dimensions						
Width	150 mm					
Height	99 mm					
Depth	85 mm					
Weight	400 g					

Table 240: X20CP1583, X20CP1584, X20cCP1584, X20CP1585, X20CP1586, X20cCP1586 - Technical data

1) The specified values are maximum values. The exact calculation is included as a data sheet in the module documentation and can be downloaded from the B&R website.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) When operated at temperatures above 55°C, a derating of the rated output current to 5 W for the X2X Link supply must be taken into consideration.
4) In parallel operation, only 75% of the rated power can be assumed. It is important to make sure that all power supplies operating in parallel are switched on and off at the same time.
5) Can be configured in Automation Studio.
6) 1 MB SRAM minus the configured remanent variables.
7) See the POWERLINK online help documentation under "Communication, POWERLINK, General information, Hardware - IF/LS".

4.12.4.5 Order data - X20CP358x

Model number	Short description
	X20 CPUs
X20CP3583	X20 CPU, ATOM 333 MHz compatible, 128 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP3584	X20 CPU, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.
X20cCP3584	X20 CPU, coated, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20CP3585	X20 CPU, ATOM 1.0 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.
X20CP3586	X20 CPU, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000BASE-T, 1 POWERLINK interface, incl. supply module, 1 terminal block, slot cover and X20 locking plate (right) included, order application memory separately.
X20cCP3586	X20 CPU, coated, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
	Required accessories
	CompactFlash cards
0CFCRD.0128E.01	CompactFlash 128 MB WD extended temp.
0CFCRD.0512E.01	CompactFlash 512 MB WD extended temp.
5CFCRD.016G-06	CompactFlash 16 GB B&R (SLC)
5CFCRD.0512-06	CompactFlash 512 MB B&R (SLC)
5CFCRD.1024-06	CompactFlash 1 GB B&R (SLC)
5CFCRD.2048-06	CompactFlash 2 GB B&R (SLC)
5CFCRD.4096-06	CompactFlash 4 GB B&R (SLC)
5CFCRD.8192-06	CompactFlash 8 GB B&R (SLC)
	Optional accessories
	Batteries
0AC201.91	Lithium batteries 4 pcs., 3 V / 950 mAh button cell We hereby state that the lithium cells contained in this shipment qualify as "partly regulated". Handle with care. If the package is damaged, inspect the cells, repack intact cells and protect cells against short circuits. For emergency information, call RENATA SA at + 41 61 319 28 27
4A0006.00-000	Lithium battery, 3 V / 950 mAh, button cell

Table 241: X20CP3583, X20CP3584, X20cCP3584, X20CP3585, X20CP3586, X20cCP3586 - Order data

Included in delivery

Model number	Short description
4A0006.00-000	Backup battery (see also section 4.12.3.19 "Exchanging the lithium battery")
-	Interface module slot covers
X20AC0SR1	X20 locking plate, right
X20TB12	X20 terminal block, 12-pin, 24 V keyed

Table 242: X20 CPUs - Contents of delivery

4.12.4.6 X20CP358x - Technical data

Product ID	X20CP3583	X20CP3584	X20cCP3584	X20CP3585	X20CP3586	X20cCP3586
Short description						
Interfaces	1x RS232, 1x Ethernet, 1x POWERLINK (V1/V2), 2x USB, 1x X2X Link					
System module	CPU					
General information						
Cooling	Fanless					
B&R ID code	0xD45C	0xC3AD	0xE21D	0xC3AF	0xBF2B	0xE21E
Status indicators	CPU function, overtemperature, Ethernet, POWERLINK, CompactFlash, battery					
Diagnostics						
Battery	Yes, using status LED and software					
CPU function	Yes, using status LED					
CompactFlash	Yes, using status LED					
Ethernet	Yes, using status LED					
POWERLINK	Yes, using status LED					
Overtemperature	Yes, using status LED					
CPU redundancy possible	No	Yes				
ACOPOS capability	Yes					
Visual Components support	Yes					
Power consumption without interface module and USB	8.2 W	8.6 W		8.8 W	9.7 W	
Internal power consumption of the X2X Link and I/O supply [1]						
Bus	1.42 W					
Internal I/O	0.6 W					
Additional power dissipation caused by the actuators (resistive) [W]	-					
Electrical isolation						
IF1 - IF2	Yes					
IF1 - IF3	Yes					
IF1 - IF4	No					
IF1 - IF5	No					
IF1 - IF6	Yes					
IF2 - IF3	Yes		-	Yes		-
IF2 - IF4	Yes					
IF2 - IF5	Yes					
IF2 - IF6	Yes		-	Yes		-
IF3 - IF4	Yes					
IF3 - IF5	Yes					
IF3 - IF6	Yes		-	Yes		-
IF4 - IF5	No					
IF4 - IF6	Yes					
IF5 - IF6	Yes					
PLC - IF1	No					
PLC - IF2	Yes					
PLC - IF3	Yes					
PLC - IF4	No					
PLC - IF5	No					
PLC - IF6	Yes					
Certification						
CE	Yes					
cULus	Yes					
ATEX Zone 2 [2]	Yes					
KC	-	Yes	-	Yes		-
GL	Yes					
GOST-R	Yes					
CPU and X2X Link supply						
Input voltage	24 VDC -15% / +20%					
Input current	Max. 1.5 A					
Fuse	Integrated, cannot be replaced					
Reverse polarity protection	Yes					
X2X Link supply output						
Nominal output power	7 W [3]					
Parallel operation	Yes [4]					
Redundant operation	Yes					
Input I/O supply						
Input voltage	24 VDC -15% / +20%					
Fuse	Required line fuse: Max. 10 A, slow-blow					
Output I/O supply						
Rated output voltage	24 VDC					
Permitted contact load	10 A					
Supply - General information						
Status indicators	Overload, operating status, module status, RS232 data transfer					

Table 243: X20CP3583, X20CP3584, X20cCP3584, X20CP3585, X20CP3586, X20cCP3586 - Technical data

Product ID	X20CP3583	X20CP3584	X20cCP3584	X20CP3585	X20CP3586	X20cCP3586
Diagnostics						
RS232 data transfer	Yes, using status LED					
Module run/error	Yes, using status LED and software					
Overload	Yes, using status LED and software					
Electrical isolation						
I/O feed - I/O supply	No					
CPU/X2X Link feed - CPU/X2X Link supply	Yes					
Controller						
CompactFlash slot	1					
Real-time clock	Nonvolatile, 1 s resolution, -10 to 10 ppm accuracy at 25°C					
FPU	Yes					
Processor						
Type		ATOM™ E620T		ATOM™ E640T	Atom™ E680T	
Clock frequency	333 MHz	0.6 GHz		1 GHz	1.6 GHz	
L1 cache						
Data code	24 kB					
Program code	32 kB					
L2 cache	-	512 kB				
Integrated I/O processor	Processes I/O data points in the background					
Modular interface slots	3					
Remanent variables	Max. 64 kB [5]	Max. 256 kB [5]			Max. 1 MB [5]	
Shortest task class cycle time	800 µs	400 µs		200 µs	100 µs	
Typical instruction cycle time	0.01 µs	0.0075 µs		0.0044 µs	0.0027 µs	
Data buffering						
Battery monitoring	Yes					
Lithium battery	Min. 2 years at 23°C ambient temperature					
Standard memory						
RAM	128 MB DDR2 SDRAM	256 MB DDR2 SDRAM			512 MB DDR2 SDRAM	
User RAM	1 MB SRAM [6]					
Interfaces						
IF1 interface						
Signal	RS232					
Design	Connection made using 12-pin X20TB12 terminal block					
Max. distance	900 m					
Transfer rate	Max. 115.2 kbit/s					
IF2 interface						
Signal	Ethernet					
Design	1x shielded RJ45 port					
Cable length	Max. 100 m between 2 stations (segment length)					
Transfer rate	10/100/1000 Mbit/s					
Transmission						
Physical layer	10 BASE-T/100 BASE-TX/1000 BASE-T					
Half-duplex	Yes					
Full-duplex	Yes					
Autonegotiation	Yes					
Auto-MDI / MDIX	Yes					
IF3 interface						
Fieldbus	POWERLINK (V1/V2) managing or controlled node					
Type	Type 4 [7]					
Design	1x shielded RJ45 port					
Cable length	Max. 100 m between 2 stations (segment length)					
Transfer rate	100 Mbit/s					
Transmission						
Physical layer	100 BASE-TX					
Half-duplex	Yes					
Full-duplex	POWERLINK mode: No / Ethernet mode: Yes					
Autonegotiation	Yes					
Auto-MDI / MDIX	Yes					
IF4 interface						
Type	USB 1.1/2.0					
Design	Type A					
IF5 interface						
Type	USB 1.1/2.0					
Design	Type A					
IF6 interface						
Fieldbus	X2X Link master					
Operating conditions						
Mounting orientation						
Horizontal	Yes					
Vertical	Yes					

Table 243: X20CP3583, X20CP3584, X20cCP3584, X20CP3585, X20CP3586, X20cCP3586 - Technical data

Product ID	X20CP3583	X20CP3584	X20cCP3584	X20CP3585	X20CP3586	X20cCP3586
Installation at elevations above sea level						
0 to 2000 m	No limitations					
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m					
EN 60529 protection	IP20					
Environmental conditions						
Temperature						
Operation						
Horizontal installation	-25 to 60°C					
Vertical installation	-25 to 50°C					
Derating	See section "Derating"					
Storage	-40 to 85°C					
Transport	-40 to 85°C					
Relative humidity						
Operation	5 to 95%, non-condensing		Up to 100%, condensing	5 to 95%, non-condensing		Up to 100%, condensing
Storage	5 to 95%, non-condensing					
Transport	5 to 95%, non-condensing					
Mechanical characteristics						
Note	Order application memory (CompactFlash) separately Backup battery included in delivery X20 locking plate (right) included in delivery X20 terminal block (12-pin) included in delivery Interface module slot covers included in delivery					
Dimensions						
Width	200 mm					
Height	99 mm					
Depth	85 mm					
Weight	470 g		-	470 g		-

Table 243: X20CP3583, X20CP3584, X20cCP3584, X20CP3585, X20CP3586, X20cCP3586 - Technical data

1) The specified values are maximum values. The exact calculation is included as a data sheet in the module documentation and can be downloaded from the B&R website.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) When operated at temperatures above 55°C, a derating of the rated output current to 5 W for the X2X Link supply must be taken into consideration.
4) In parallel operation, only 75% of the rated power can be assumed. It is important to make sure that all power supplies operating in parallel are switched on and off at the same time.
5) Can be configured in Automation Studio.
6) 1 MB SRAM minus the configured remanent variables.
7) See the POWERLINK online help documentation under "Communication, POWERLINK, General information, Hardware - IF/LS".

4.12.4.7 X20 CPUs - Status LEDs

Figure	LED	Color	Status	Description
	R/E	Green	On	Application running
			Blinking	Boot mode system start: CPU initializing the application, all bus systems and I/O modules[1)]
		Red	On	SERVICE mode
			Blinking	The "R/E" LED blinks red and the "RDY/F" LED blinks yellow when there is a license violation.
			Double flash	BOOT mode (during firmware update)[1)]
	RDY/F	Yellow	On	SERVICE or BOOT mode
			Blinking	The "RDY/F" LED blinks yellow and the "R/E" LED blinks red when there is a license violation.
	S/E	Green/Red		Status/Error LED. The statuses of this LED are described in section 4.12.3.4.1 ""S/E" LED".
	PLK	Green	On	A link to the POWERLINK peer station has been established.
			Blinking	A link to the POWERLINK peer station has been established. The LED blinks when Ethernet activity is taking place on the bus.
	ETH	Green	On	A link to the peer station has been established.
			Blinking	A link to the peer station has been established. Indicates Ethernet activity is taking place on the bus.
	CF	Green	On	CompactFlash inserted and detected
		Yellow	On	CompactFlash read/write access
	DC	Yellow	On	CPU power supply OK
		Red	On	Backup battery empty

1) The process can take several minutes depending on the configuration.

4.12.4.7.1 "S/E" LED

The Status/Error LED is a green/red dual LED. The LED status can have different meanings depending on the operating mode.

4.12.4.7.1.1 Ethernet mode

In this mode, the interface is operated as an Ethernet interface.

Green - Status	Description
On	Interface being operated as an Ethernet interface

Table 244: Status/Error LED - Ethernet operating mode

4.12.4.7.1.2 POWERLINK V1

Status LED		Status of the POWERLINK node
Green	Red	
On	Off	The POWERLINK node is running with no errors.
Off	On	A system error has occurred. The error type can be read using the PLC logbook. An irreparable problem has occurred. The system cannot properly carry out its tasks. This state can only be changed by resetting the module.
Blinking alternately		The POWERLINK managing node has failed. This error code can only occur when operated as a controlled node. This means that the configured node number lies within the range 0x01 - 0xFD.
Off	Blinking	System failure. The red blinking LED signals an error code (see section 4.12.2.4.2 "System failure error codes").
Off	Off	Module is: • Off • Starting up • Not configured correctly in Automation Studio • Defective

Table 245: Status/Error LED - POWERLINK V1 operating mode

4.12.4.7.1.3 POWERLINK V2

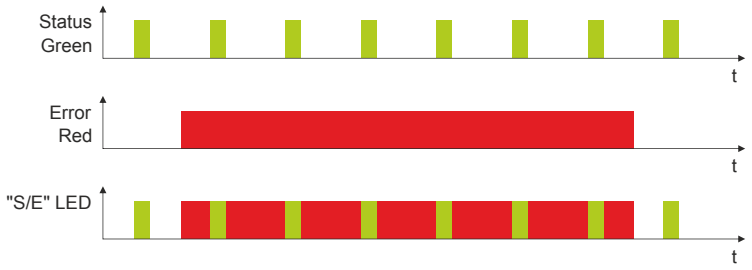
Red - Error	Description
On	The module is in an error mode (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: The LED blinks red several times immediately after startup. This is not an error.

Table 246: Status/Error LED as Error LED - POWERLINK operating mode

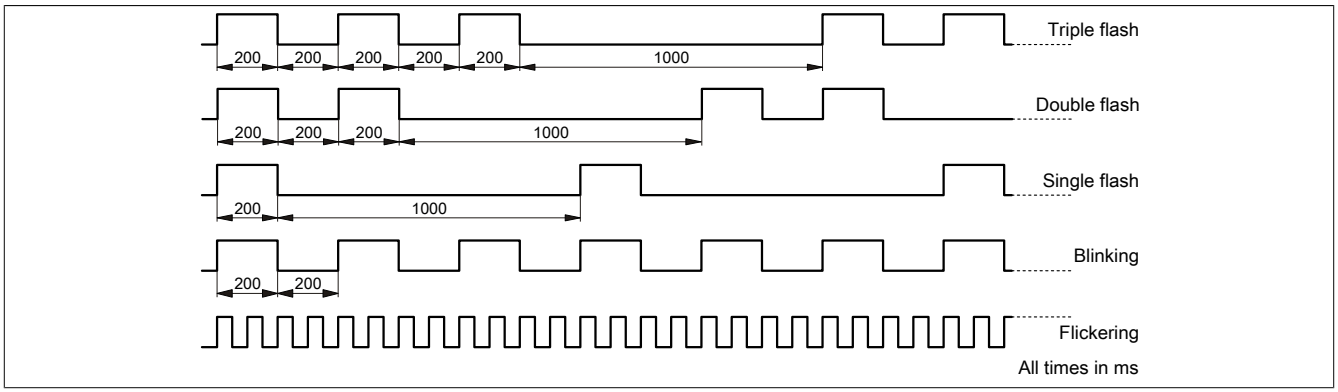
Green - Status	Description
Off	**Mode** The module is in NOT_ACTIVE mode or: • Switched off • Starting up • Not configured correctly in Automation Studio • Defective **Managing node (MN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to PRE_OPERATIONAL_1 mode. If POWERLINK communication is detected before the time expires, however, then the MN will not be started. **Controlled node (CN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to BASIC_ETHERNET mode. If POWERLINK communication is detected before this time expires, however, the module switches immediately to PRE_OPERATIONAL_1 mode.
Green flickering (approx. 10 Hz)	**Mode** The module is in BASIC_ETHERNET mode. The interface is being operated as an Ethernet TCP/IP interface. **Managing node (MN)** This state can only be changed by resetting the module. **Controlled node (CN)** If POWERLINK communication is detected while in this state, the module will transition to the PRE_OPERATIONAL_1 state.
Single flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_1 mode. **Managing node (MN)** The MN starts "reduced cycle" operation. Cyclic communication is not yet taking place. **Controlled node (CN)** The module can be configured by the MN in this state. The CN waits until it receives an SoC frame and then switches to the PRE_OPERATIONAL_2 mode. An LED lit red in this state indicates failure of the MN.

Table 247: Status/Error LED as Status LED - POWERLINK operating mode

Green - Status	Description
Double flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_2 mode. **Managing node (MN)** The MN begins cyclic communication (cyclic input data is not yet being evaluated). The CNs are configured in this state. **Controlled node (CN)** The module can be configured by the MN in this state. A command then switches the module to READY_TO_OPERATE mode. An LED lit red in this mode indicates failure of the MN.
Triple flash (approx. 1 Hz)	**Mode** The module is in the READY_TO_OPERATE state. **Managing node (MN)** Cyclic and asynchronous communication is taking place. Any received PDO data is ignored. **Controlled node (CN)** The configuration of the module is completed. Normal cyclic and asynchronous communication is taking place. The PDO data sent corresponds to the PDO mapping. Cyclic data is not yet being evaluated, however. An LED lit red in this mode indicates failure of the MN.
On	**Mode** The module is in PRE_OPERATIONAL_2 mode. PDO mapping is active and cyclic data is being evaluated.
Blinking (approx. 2.5 Hz)	**Mode** The module is in STOPPED mode. **Managing node (MN)** This status is not possible for the MN. **Controlled node (CN)** No output data is produced or input data supplied. It is only possible to enter or leave this mode after the MN has given the appropriate command.

Table 247: Status/Error LED as Status LED - POWERLINK operating mode

Status LEDs - Blinking patterns



4.12.4.7.2 System failure error codes

Incorrect configuration or defective hardware can cause a system stop error.

The error code is indicated by the red Error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. The error code is output cyclically every 2 seconds.

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	●	●	●	-	Pause	●	●	●	-	Pause
Hardware error: The module or a system component is defective and must be replaced.	-	●	●	-	Pause	-	●	●	-	Pause

Table 248: Status/Error ("S/E") LED - System failure error codes

Key:
- ● ... 150 ms
- \- ... 600 ms
- Pause ... 2 second delay

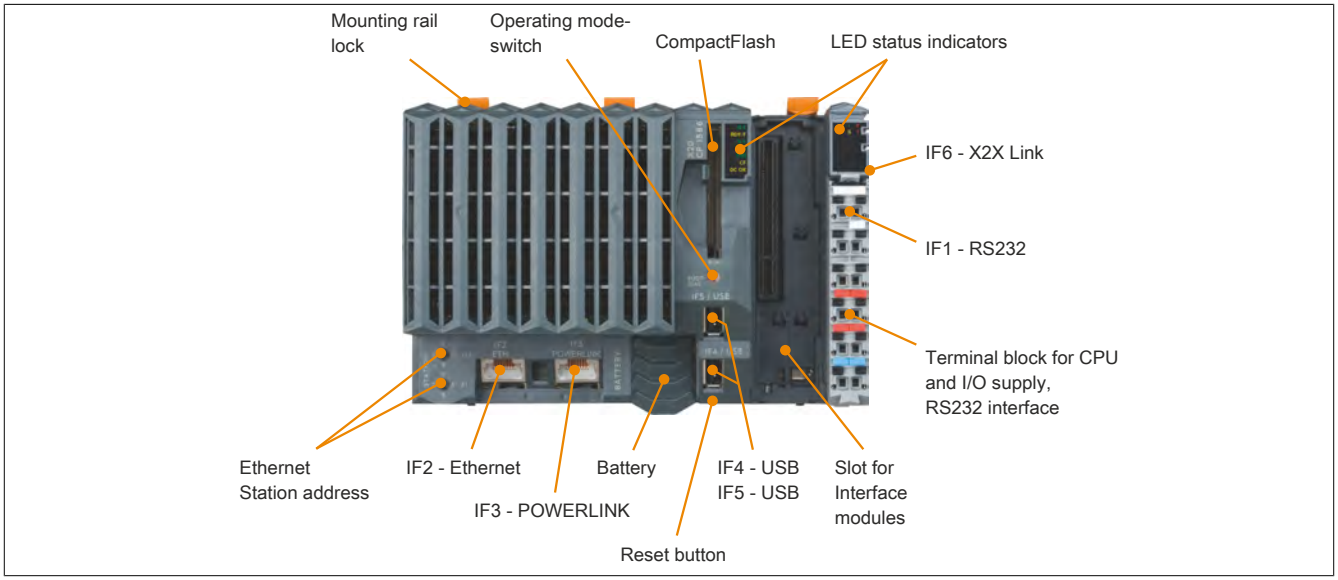
4.12.4.8 LED status indicators for the integrated power supply

For a description of the various operating modes, see section 2.11.1 "re LEDs".

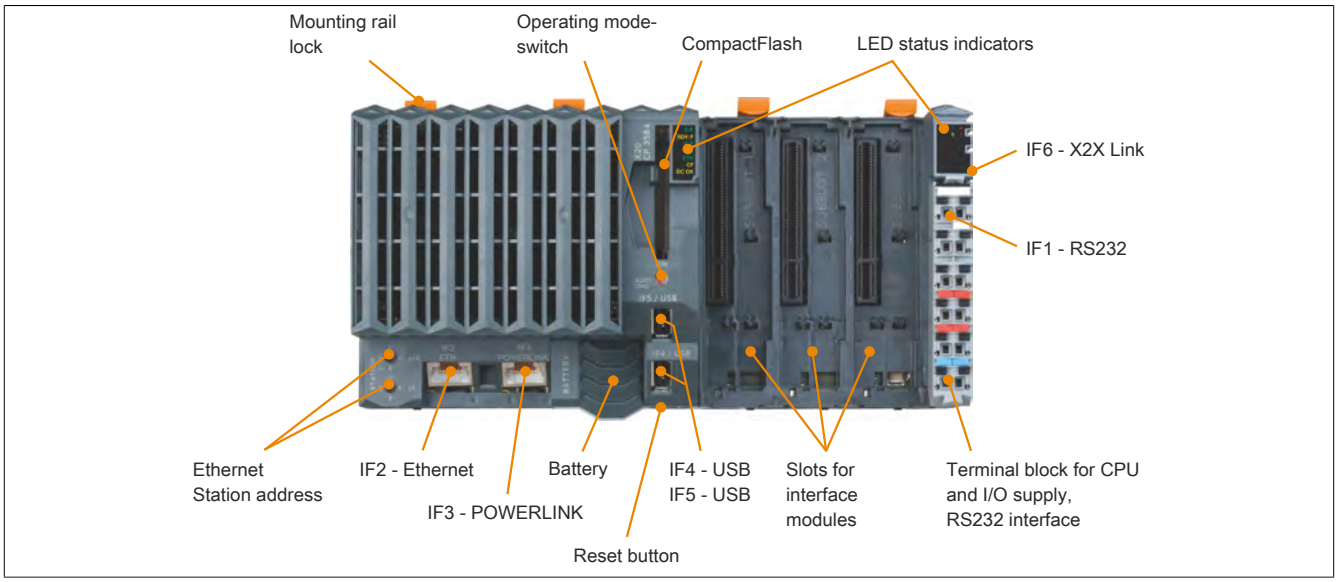
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • The X2X Link supply for the power supply is overloaded • I/O supply too low • Input voltage for X2X Link supply too low
	e + r	Red on / Green single flash		Invalid firmware
	S	Yellow	Off	No RS232 activity
			On	The LED lights up when data is being sent or received via the RS232 interface.
	I	Red	Off	The X2X Link supply is within the valid limits
			On	The X2X Link supply for the power supply is overloaded

4.12.4.9 Operating and connection elements

X20CP158x



X20CP358x



4.12.4.10 Slot for application memory

These CPUs require application memory in order to operate. The application memory is provided in the form of a CompactFlash card. It is not included with the CPUs, but must be ordered separately as an accessory.

Information:

The CompactFlash card must not be removed during operation.

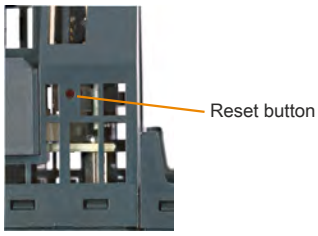
4.12.4.11 Operating mode switch

The operating mode switch is used to set the operating mode.

Switch position	Operating mode	Description
BOOT	BOOT	When the switch is in this position, the default B&R Automation Runtime (AR) system is started and the runtime system can be installed via the online interface (B&R Automation Studio). User flash memory is deleted only after the download begins.
RUN	RUN	RUN mode
DIAG	DIAGNOSE	Boots the CPU in diagnostic mode. Program sections in User RAM and User FlashPROM are not initialized. After diagnostic mode, the CPU always boots with a cold restart.

Table 249: X20 CPUs - Operating modes

4.12.4.12 Reset button



The reset button is located below the USB interfaces on the bottom of the housing. It can be pressed with any small pointed object (e.g. paper clip). Pressing the reset button triggers a hardware reset, which means:

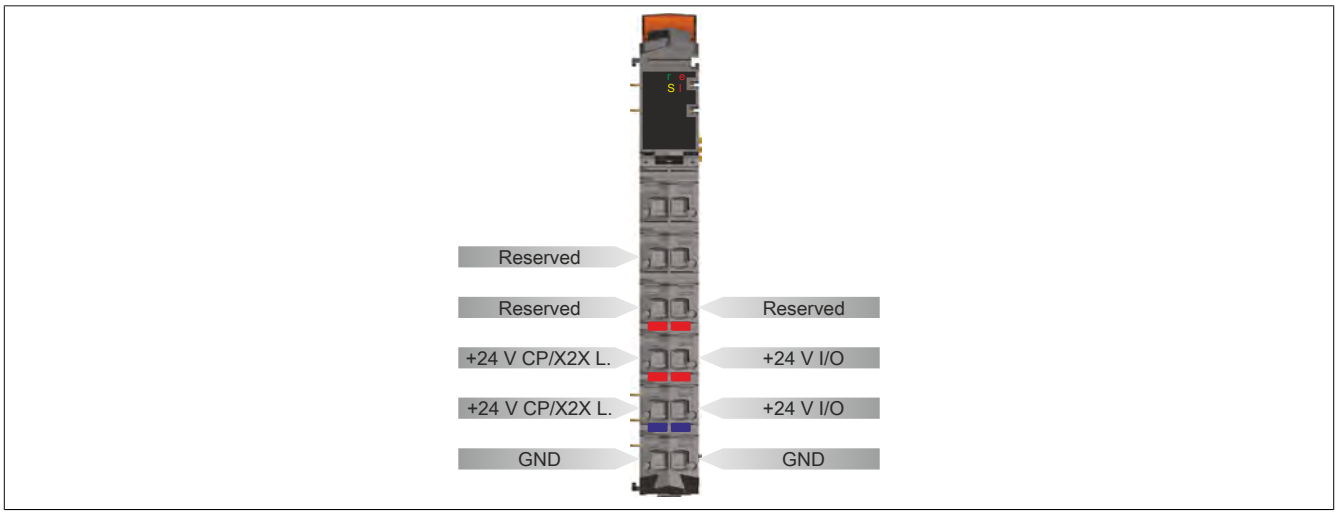
- All application programs are stopped.
- All outputs are set to zero.

The PLC then boots into Service mode by default. The boot mode that follows after pressing the reset button can be defined in Automation Studio.

4.12.4.13 CPU supply

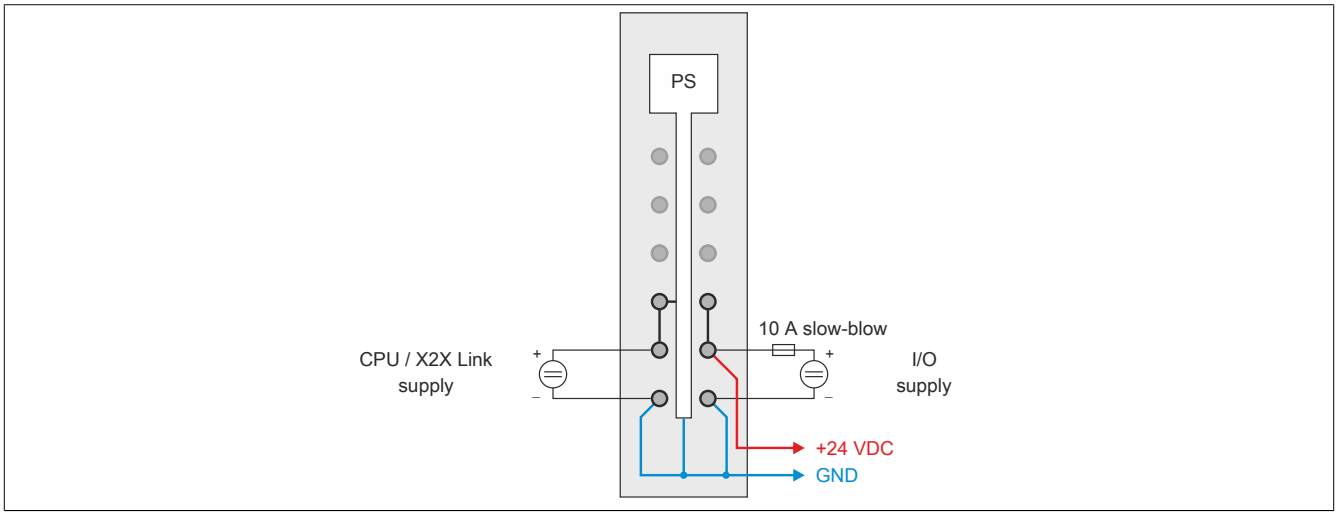
A power supply is integrated in the X20 CPUs. It has a feed for the CPU, the X2X Link and the internal I/O supply. Supply for the CPU and X2X Link is electrically isolated.

Pinout of the integrated power supply

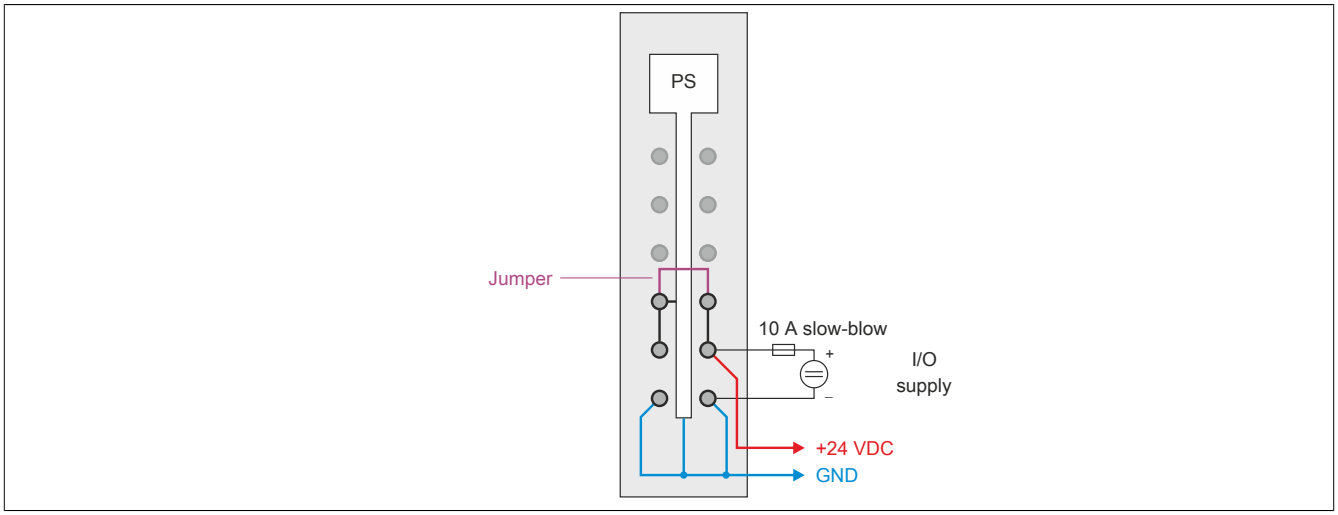


Connection examples

Connection example with 2 separate supplies

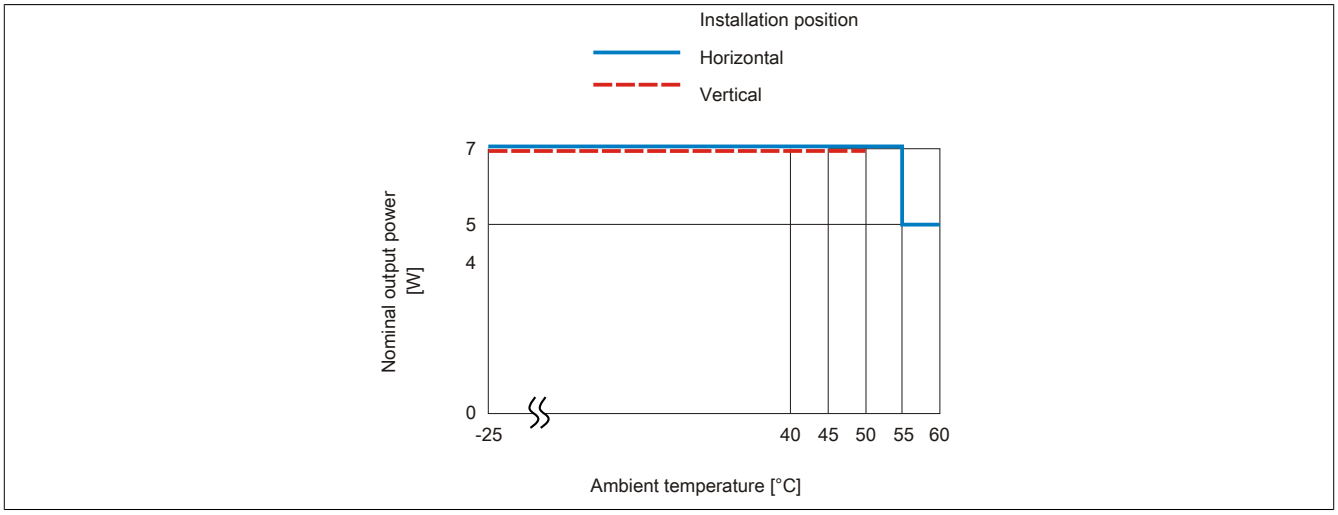


Connection example with a supply and jumper



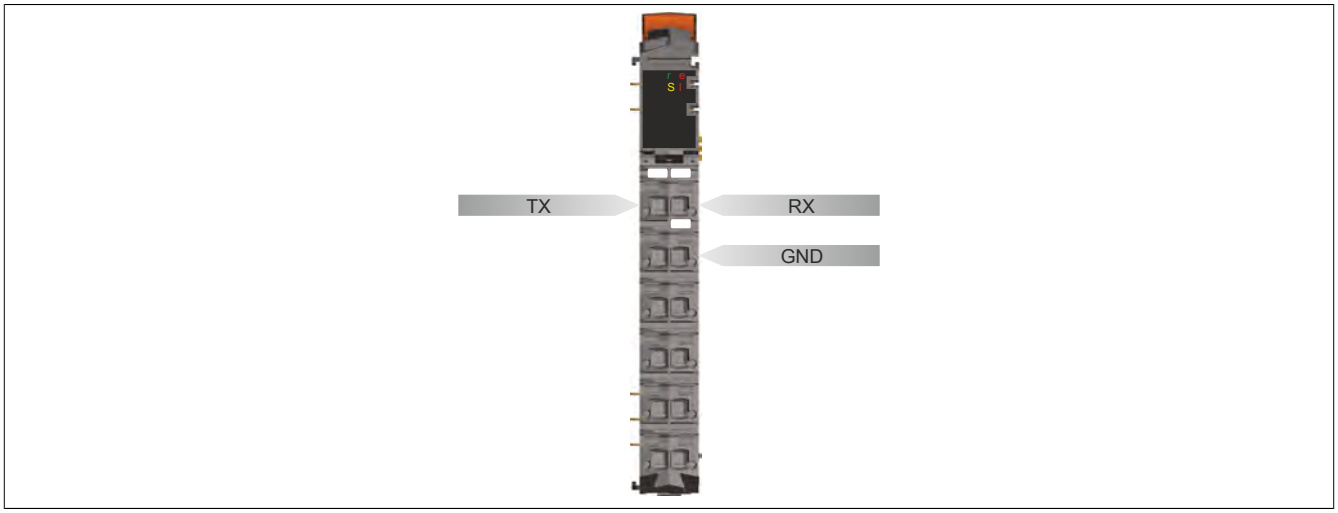
4.12.4.14 Derating

There is no derating when operated below 55°C. Above 55°C, the nominal output power for the X2X Link supply must be reduced to 5 W.



4.12.4.15 RS232 interface (IF1)

The non-electrically isolated RS232 interface is primarily intended to serve as an online interface for communication with the programming device.



4.12.4.16 Ethernet interface (IF2)

The IF2 is executed as the10 BASE-T / 100 BASE-TX / 1000 BASE-T gigabit Ethernet interface.

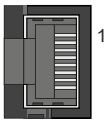
The INA2000 station number of the Ethernet interface is set using the two hex switches.

Information about cabling X20 modules with an Ethernet interface can be found on the B&R website in the module's download section at www.br-automation.com.

Information:

The Ethernet interface (IF2) is not suitable for POWERLINK (see 4.12.4.17 "POWERLINK interface (IF3)").

Pinout

Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45 port	1	D1+	Data 1+
	2	D1-	Data 1-
	3	D2+	Data 2+
	4	D3+	Data 3+
	5	D3-	Data 3-
	6	D2-	Data 2-
	7	D4+	Data 4+
	8	D4-	Data 4-

4.12.4.17 POWERLINK interface (IF3)

POWERLINK V1

Switch position	Description
0x00	Operation as managing node.
0x01 - 0xFD	Node number of the POWERLINK node. Operation as controlled node.
0xFE - 0xFF	Reserved, switch position not permitted

Table 250: POWERLINK V1 - Node numbers

POWERLINK V2

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node.
0xF0	Operation as a managing node.
0xF1 - 0xFF	Reserved, switch position not permitted

Table 251: POWERLINK node number

Ethernet mode

In this mode, the interface is operated as an Ethernet interface. The INA2000 station number can be set using the B&R Automation Studio software.

Pinout

Information about cabling X20 modules with an Ethernet interface can be found on the B&R website in the module's download section at www.br-automation.com.

Pin	Assignment	
1	RxD	Receive data
2	RxD\	Receive data\
3	TxD	Transmit data
4	Termination	
5	Termination	
6	TxD\	Transmit data\
7	Termination	
8	Termination	

Table 252: X20 CPUs - Pinout for POWERLINK interface (IF3)

4.12.4.18 USB interfaces (IF4 and IF5)

IF4 and IF5 are USB interfaces. The connection is made using a USB 1.1/2.0 interface.

The USB interfaces can only be used for devices approved by B&R (e.g. floppy disk drive, DiskOnKey or dongle).

Information:

USB interfaces cannot be used for online communication with a programming device.

Only devices isolated from GND can be connected to the USB interfaces.

4.12.4.19 Slots for interface modules

The CPUs have one or three slots for interface modules.

Various bus and network systems can easily be integrated into the X20 system by selecting the corresponding interface module.

4.12.4.20 Overtemperature cutoff

To prevent damage, the CPU is cut off and reset when the processor reaches 110°C or the circuit board reaches 95°C.

The following errors are entered in the logbook:

Error number	Error description
9204	WARNING: System halted because of temperature check
9210	WARNING: Boot by watchdog or manual reset

Table 253: X20 CPUs - Logbook entries after overtemperature cutoff

4.12.4.21 Data / Real-time clock buffering

The CPUs are buffered by a backup battery. The following areas are buffered:

- Remanent variables
- User RAM
- System RAM
- Real-time clock

Battery monitoring

The battery voltage is checked cyclically. The cyclic load test of the battery does not considerably shorten the battery life, instead it gives an early warning of weakened buffer capacity.

The status information "Battery OK" is available from the system library function "BatteryInfo" and the CPU's I/O mapping.

Replacement interval for battery

The battery should be replaced every 4 years. The replacement intervals recommended by B&R reflect the batteries' average service life and operating conditions. It does not represent the maximum buffer duration.

4.12.4.22 Exchanging the lithium battery

The CPUs have a lithium battery. The lithium battery is found in a separate compartment on the bottom of the module and protected by a cover.

Backup battery data

Model number 4A0006.00-000 0AC201.91	 1 pcs. 4 pcs.
Short description	Lithium battery, 3 V / 950 mAh, button cell
Storage temperature	-20 to 60°C
Storage time	Max. 3 years at 30°C
Relative humidity	0 to 95%, non-condensing

Table 254: X20 CPUs - Backup battery data

Important information about the battery exchange

The product design allows the battery to be changed with the PLC switched either on or off. In some countries, safety regulations do not allow batteries to be changed while the module is switched on. To prevent data loss, the battery must be changed within 1 min. with the power off.

Warning!

The battery must be replaced by a Typ CR2477N Renata battery only. The use of another battery may present a risk of fire or explosion.

The battery may explode if handled improperly. Do not recharge, disassemble or dispose of in fire.

Procedure for exreplacing the battery

1. Touch the mounting rail or ground connection (not the power supply!) in order to discharge any electrostatic charge from your body.
2. Remove the cover for the lithium battery. Do this by sliding it down and away from the CPU.

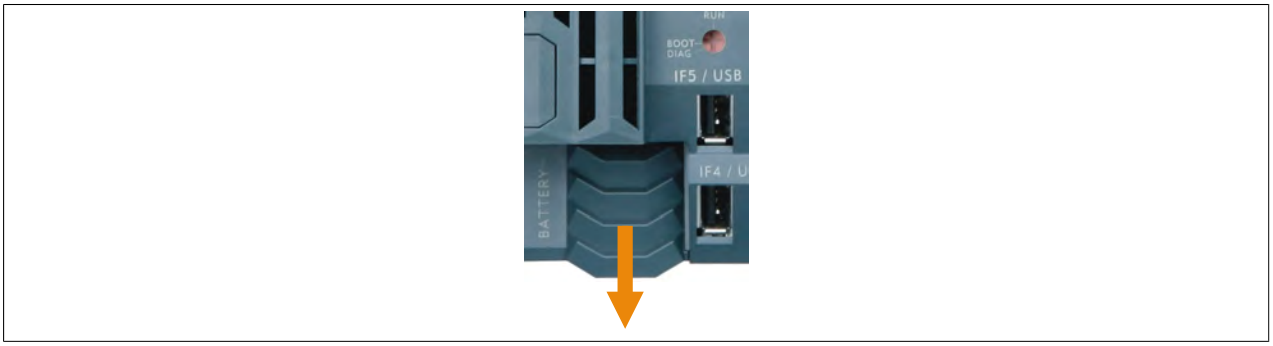


Figure 234: X20 CPUs - Remove lithium battery cover

3. Remove the battery from the holder (do not use pliers or uninsulated tweezers -> risk of short circuiting). The battery should not be held by its edges. **Insulated** tweezers may also be used to remove the battery.

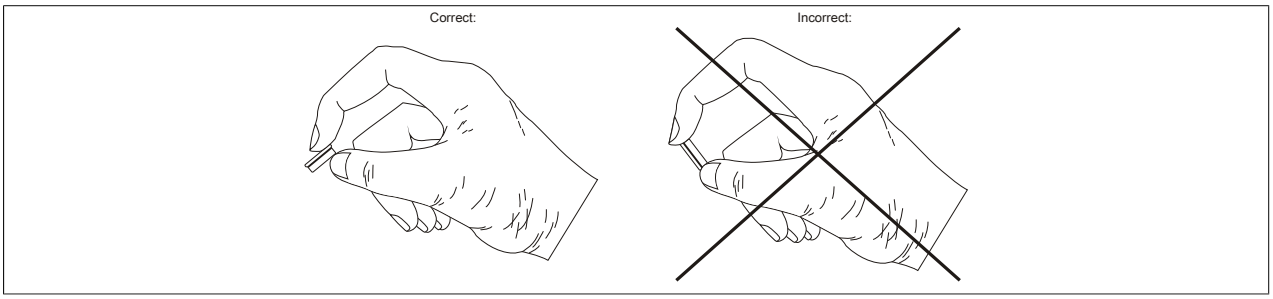


Figure 235: X20 CPUs - Correct grip for the battery

4. Insert the new battery with the correct polarity. To do this, lay the battery with the "+" side up on the right part of the battery holder under the USB interface IF4. Then secure the battery in the holder by pressing above the left part of the battery holder.
5. Replace the cover.

Information:

Lithium batteries are considered hazardous waste. Used batteries should be disposed of in accordance with applicable local regulations.

4.12.4.23 Programming the system flash memory

General information

In order for the application project to be executed on the CPU, the Automation Runtime operating system, the system components and the application project must be installed on the CompactFlash card.

Creating a CompactFlash using a USB card reader

The easiest way to perform an initial installation is by creating a fully programmed CompactFlash card using a USB card reader.

1. Creating and configuring a project in Automation Studio
2. In Automation Studio, select **Tools / Create CompactFlash**
3. In the dialog box that opens, select a CompactFlash card and then generate it
4. Insert the finished CompactFlash into the CPU and turn on the CPU's supply voltage
5. CPU booting

For details about commissioning: See help system under "Automation Software / Getting Started"

Installation over an online connection

The CPUs are delivered with a default B&R Automation Runtime system (with limited functions) already installed. This runtime system is started in Boot mode (operating mode switch in the BOOT position or no CompactFlash / invalid CompactFlash inserted). It initializes the Ethernet interface and onboard serial RS232 interface, making it possible to download a new runtime system.

1. Insert the CompactFlash card and switch on the power to the CPU. When the switch is in the BOOT position, a new or invalid CompactFlash card starts the CPU with the default B&R Automation Runtime system.
2. Establish a physical online connection between the programming device (PC or industrial PC) and the CPU (e.g. over an Ethernet network or the RS232 interface).
3. Before you can establish an online connection via Ethernet, the CPU must be assigned an IP address. In Automation Studio, select **Settings** from the Online menu and then click on the **Browse targets** button to search for B&R target systems on the local network. The CPU should appear in the list. If the CPU has not already received an IP address from a DHCP server, right-click on it and select **Set IP parameters** from the shortcut menu. All necessary network configurations can be made on a temporary basis in this dialog box (should be identical to the settings defined in the project).
4. Configure online connection in B&R Automation Studio. For details about the configuration: See help system under "Automation Software / Communication / Online communication"
5. Start the download procedure by selecting the **Services** command from the **Project** menu. Then select **Transfer Automation Runtime** from the pop-up menu. Now follow the instructions provided by B&R Automation Studio.

4.12.4.24 Information regarding switching from X20CPx48x to X20CPx58x

- A hardware upgrade is required for some X20 IFxxxx interface modules. This can be installed from Automation Studio by selecting **Tools/Upgrades** from the menu.
  In addition, some modules specify a specific hardware revision. The following table provides an overview:

Model number	Minimum upgrade version	Minimum hardware revision
X20IF1020	1.1.5.1	H0
X20IF1030	1.1.5.1	I0
X20IF1041-1	-	-
X20IF1043-1	-	-
X20IF1051-1	-	-
X20IF1053-1	-	-
X20IF1061	-	E0
X20IF1061-1	-	-
X20IF1063	1.1.5.0	-
X20IF1063-1	-	-
X20IF1065	-	-
X20IF1072	1.0.5.1	-
X20IF1082	1.2.2.0	-
X20IF1082-2	1.2.1.0	-
X20IF1086-2	1.1.1.0	-
X20IF1091	1.0.5.1	-
X20IF10A1-1	-	-
X20IF10D1-1	-	-
X20IF10D3-1	-	-
X20IF10E1-1	-	-
X20IF10E3-1	-	-
X20IF10G3-1	-	-
X20IF10H3-1	-	-
X20IF2772	1.0.6.1	-
X20IF2792	1.0.5.1	-

Table 255: X20 CPUs - Minimum upgrade version and minimum hardware revision for X20 IFxxxx interface modules

- The X20CPx58x CPUs are supported by B&R Automation Studio V3.0.90.20 and higher.
- If an X20CPx48x is to be replaced by an X20CPx58x in an existing Automation Studio configuration, the X20CPx58x may not be listed as one of the available options even though the upgrade for the CPU has already been installed. If this is the case, it is necessary to upgrade the X20CPx48x.
- Starting with Automation Runtime 4.x, USB devices are integrated in Automation Runtime dynamically so that they no longer need to be configured in Automation Studio. In order to use a USB device, its internal device name needs to be obtained at runtime. For an example, see the Automation Studio help system for the library "AsUSB / Examples".

4.13 Digital input modules

Digital input modules convert binary process signals into the internal signal level required by the PLC. The states of the digital inputs are indicated with status LEDs.

4.13.1 Brief information

Product ID	Short description	on page
X20DI0471	X20 digital input module, 10 inputs, 48 VDC, sink, configurable input filter, 1-wire connections	1208
X20DI2371	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 3-wire connections	1215
X20DI2372	X20 digital input module, 2 inputs, 24 VDC, source, configurable input filter, 3-wire connections	1221
X20DI2377	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 2 event counters 50 kHz, 3-wire connections	1227
X20DI2653	X20 digital input module, 2 inputs, 100 to 240 VAC, 240 V keyed, 3-wire connections	1235
X20DI4371	X20 digital input module, 4 inputs, 24 VDC, sink, configurable input filter, 3-wire connections	1241
X20DI4372	X20 digital input module, 4 inputs, 24 VDC, source, configurable input filter, 3-wire connections	1248
X20DI4375	X20 digital input module, 4 inputs, 24 VDC, sink, configurable input filter, open line and short circuit detection, 3-wire connections	1254
X20DI4653	X20 digital input module, 4 inputs, 100 to 240 VAC, 240 V keyed, 2-wire connections	1265
X20DI4760	X20 digital input module, 4 NAMUR inputs, 8.05 V	1271
X20DI6371	X20 digital input module, 6 inputs, 24 VDC, sink, configurable input filter, 2-wire connections	1280
X20DI6372	X20 digital input module, 6 inputs, 24 VDC, source, configurable input filter, 2-wire connections	1286
X20DI6373	X20 digital input module, 6 inputs, 24 VDC, sink/source, all inputs floating, configurable input filter, 2-wire connections	1292
X20DI6553	X20 digital input module, 6 inputs, 100 to 120 VAC, 240 V keyed, 1-wire connections	1298
X20DI8371	X20 digital input module, 8 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	1304
X20DI9371	X20 digital input module, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	1310
X20DI9372	X20 digital input module, 12 inputs, 24 VDC, source, configurable input filter, 1-wire connections	1317
X20DID371	X20 digital input module, 8 inputs, 24 VDC, sink, configurable input filter, 2-wire connections	1324
X20DIF371	X20 digital input module, 16 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	1330
X20cDI4371	X20 digital input module, coated, 4 inputs, 24 VDC, sink, configurable input filter, 3-wire connections	1241
X20cDI4375	X20 digital input module, coated, 4 inputs, 24 VDC, sink, configurable input filter, open line and short circuit detection, 3-wire connections	1254
X20cDI4760	X20 digital input module, coated, 4 NAMUR inputs, 8.05 V	1271
X20cDI6371	X20 digital input module, coated, 6 inputs, 24 VDC, sink, configurable input filter, 2-wire connections	1280
X20cDI6372	X20 digital input module, coated, 6 inputs, 24 VDC, source, configurable input filter, 2-wire connections	1286
X20cDI9371	X20 digital input module, coated, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	1310
X20cDI9372	X20 digital input module, coated, 12 inputs, 24 VDC, source, configurable input filter, 1-wire connections	1317

4.13.2 X20DI0471

4.13.2.1 General information

The module is equipped with 10 inputs for 1-wire connections. It is designed for a nominal voltage 4.75 to 60 VDC.

- 10 digital inputs
- 4.75 to 60 VDC inputs
- Sink circuit
- 1-wire connections
- Configurable software input filter for entire module

4.13.2.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI0471	X20 digital input module, 10 inputs, 48 VDC, sink, configurable input filter, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 256: X20DI0471 - Order data

4.13.2.3 Technical data

Product ID	X20DI0471
Short description	
I/O module	10 digital inputs 4.75 to 60 VDC for 1-wire connections
General information	
B&R ID code	0xE7CE
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	TBD
Internal I/O	TBD
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	4.75 to 60 VDC
Input voltage	0 to 60 VDC
Reference voltage	4.75 to 60 VDC
Input current	0.5 to 1 mA
Input filter	
Hardware	≤100 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	1-wire connections
Input circuit	Sink
Reference voltage input resistance	20 kΩ
Switching threshold	
Low	≤0.2 x U_{ref}
High	≥0.6 x U_{ref}
Reference voltage monitoring	Yes
Isolation voltage between channel and bus	TBD V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm

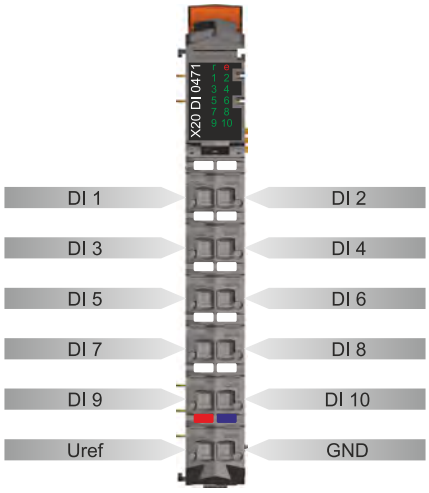
Table 257: X20DI0471 - Technical data

4.13.2.4 LED status indicators

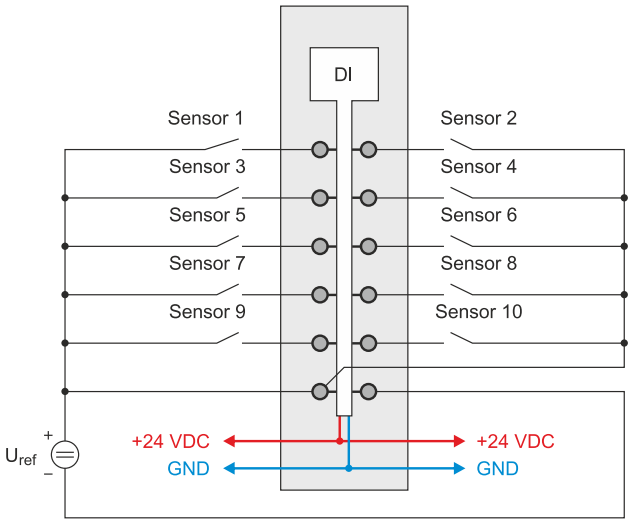
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 10	Green		Input state of the corresponding digital input

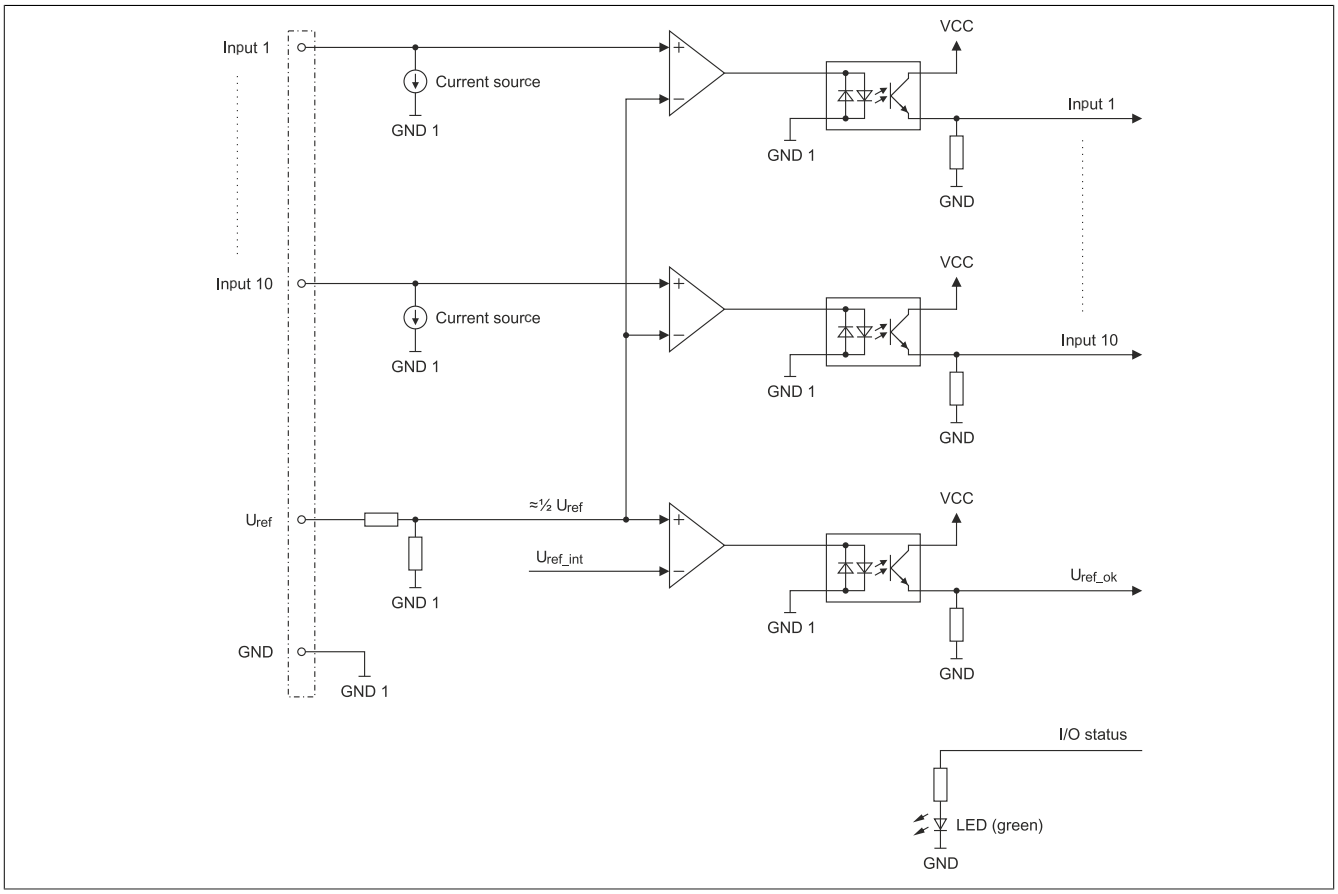
4.13.2.5 Pinout



4.13.2.6 Connection example

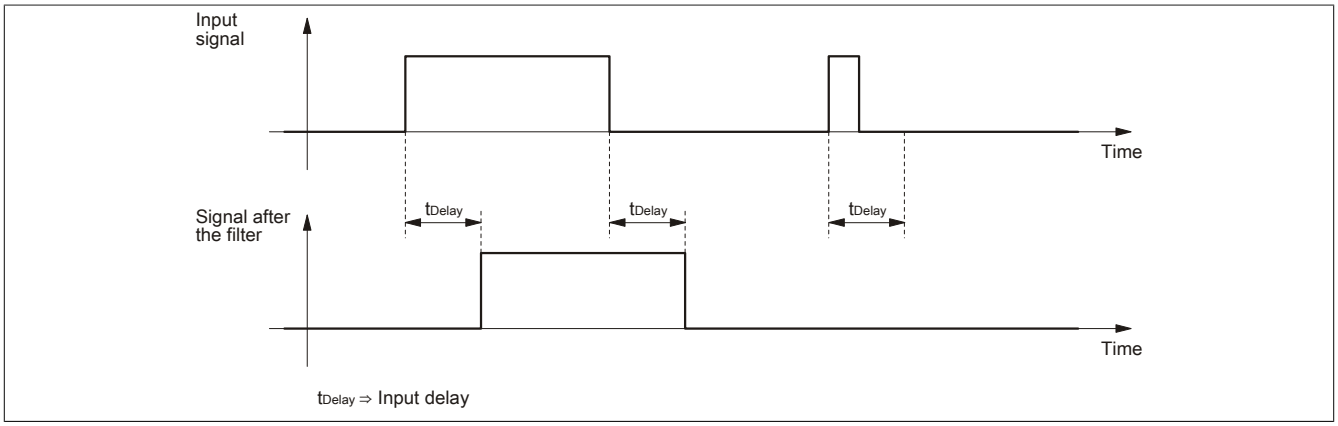


4.13.2.7 Input circuit diagram



4.13.2.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.2.9 Register description

4.13.2.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.2.9.2 Function model 0 - default

Register	Fixed offset	Register name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
-	1	DigitalInput	UINT	•			
0	1	Input state of digital inputs 1 to 8	USINT				
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
1	2	Input state of digital inputs 9 to 10	USINT	•			
		DigitalInput09	Bit 0				
		DigitalInput10	Bit 1				
		ReferenceStatus	Bit 7				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.2.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Register name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input state of digital inputs 1 to 8	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
1	1	Input state of digital inputs 9 to 10	USINT	•			
		DigitalInput09	Bit 0				
		DigitalInput10	Bit 1				
		ReferenceStatus	Bit 7				
18	-	ConfigOutput01	USINT				•

1) The offset specifies the position of the register within the CAN object.

4.13.2.9.3.1 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN-I/O.

4.13.2.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.2.9.5 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.2.9.5.1 Details related to use

The table shows how the register must be defined in relation to the function model and which parameter is available for this in the Automation Studio configuration.

Function model	Value or path for the configuration parameter
All	General / Input filter [0.1 ms]

4.13.2.9.6 Input state of digital inputs 1 to 10

Register name:
DigitalInput or
DigitalInput01 to DigitalInput10

This register indicates the input state of digital inputs 1 to 10 and the status of the reference voltage.

The reference voltage is monitored. The status is output in bit 7. The nominal voltage is 4.75 to 60 VDC.

Reference voltage	Status of the digital inputs in relation to the input voltage	
U_{ref} < 4.75 V	All digital inputs are in a low state regardless of the voltage on the inputs.	
U_{ref} ≥ 4.75 V	$U_{In} \leq 0.2 * U_{ref}$	The digital input is low
	$U_{In} \geq 0.6 * U_{ref}$	The digital input is high
	$0.2 * U_{ref} < U_{In} < 0.6 * U_{ref}$	This area is inconclusive. The digital input is either low or high.

Example

The reference voltage U_{ref} = 48 VDC

Calculation of the switching threshold:

Switching threshold low = 48 * 0.2 = 9.6 VDC

Switching threshold high = 48 * 0.6 = 28.8 VDC

Status of the digital inputs in relation to the input voltage:

Input voltage	State of the digital input
$U_{In} \leq 9.6$ VDC	The digital input is low
9.6 VDC < U_{In} < 28.8 VDC	The digital input is either low or high (inconclusive).
$U_{In} \geq 28.8$ VDC	The digital input is high

Only function model 0 - Standard

The "Packed inputs" setting in the Automation Studio I/O configuration is used to determine whether all of the bits from this register should be set up individually as data points in the Automation Studio I/O mapping ("DigitalInput01" to "DigitalInput10") or whether this register should be displayed as an individual UINT data point ("DigitalInput").

Data type	Value	Information	
UINT	0x0000 to 0x83FF	Packed inputs = On	
		0xy000 to 0xy3FF	Status of digital inputs 1 to 10
		0x0yyy	Reference voltage U_{ref} < 4.75 V
		0x8yyy	Reference voltage U_{ref} ≥ 4.75 V
USINT	See bit structure.	Packed inputs = Off or Function model <> 0 - Standard	

Bit structure:

Register 0

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

Register 1

Bit	Name	Value	Information
0	DigitalInput09	0 or 1	Input state - Digital input 9
1	DigitalInput10	0 or 1	Input state - Digital input 10
2 - 6	Reserved		
7	ReferenceStatus	0	Reference voltage U_{ref} < 4.75 V
		1	Reference voltage U_{ref} ≥ 4.75 V

4.13.2.9.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.2.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.3 X20DI2371

4.13.3.1 General Information

The module is equipped with 2 inputs for 3-wire connections.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 digital inputs
- Sink connection
- 3-wire connections
- 24 VDC and GND for sensor supply
- Software input filter can be configured for entire module

4.13.3.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI2371	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 258: X20DI2371 - Order data

4.13.3.3 Technical data

Product ID	X20DI2371
Short description	
I/O module	2 digital inputs 24 VDC for 3-wire connections
General information	
B&R ID code	0x1B8D
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.12 W
Internal I/O	0.29 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 3.75 mA
Input filter	
Hardware	≤100 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	3-wire connections
Input circuit	Sink
Input resistance	Typ. 6.4 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Sensor supply	
Power consumption	Max. 12.0 W 2)
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 VDC
Summation current	0.5 A
Short circuit protection	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 259: X20DI2371 - Technical data

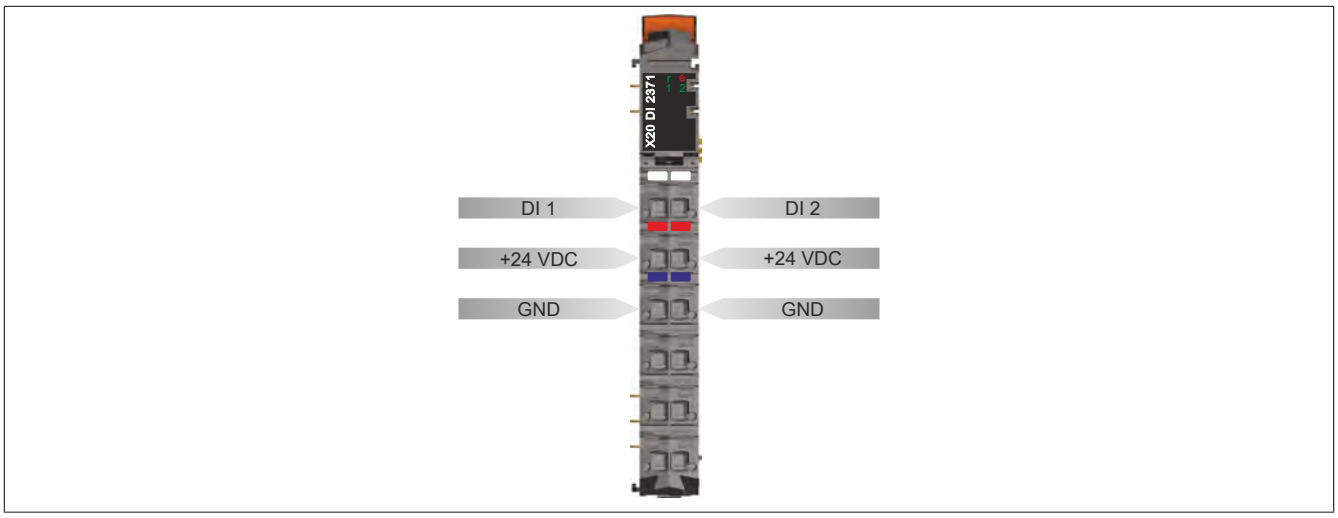
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.13.3.4 Status LEDs

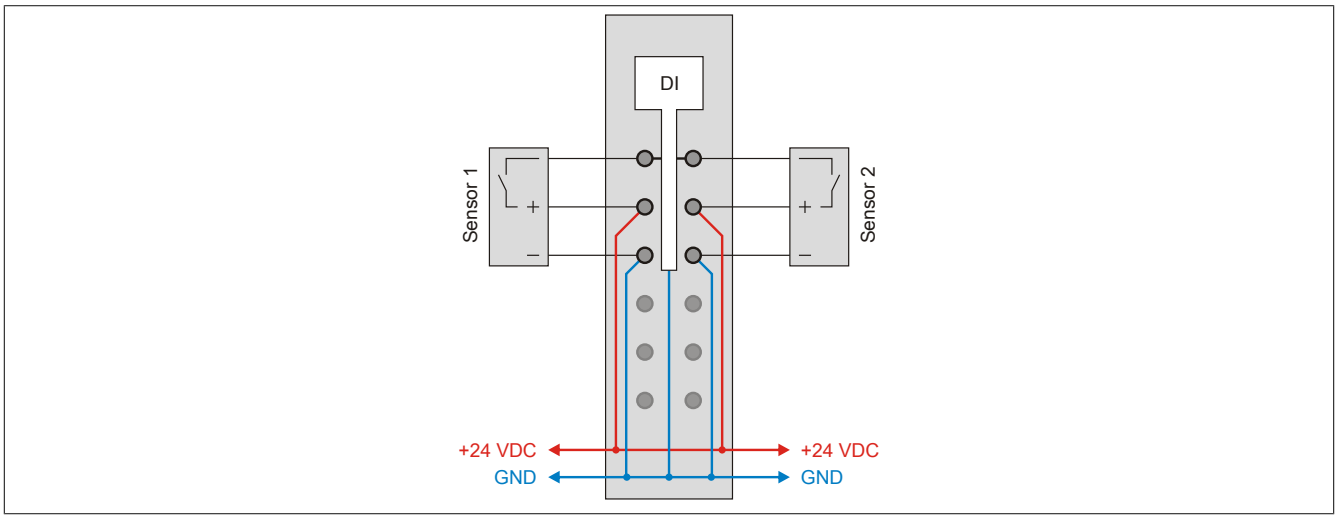
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green		Input status of the corresponding digital input

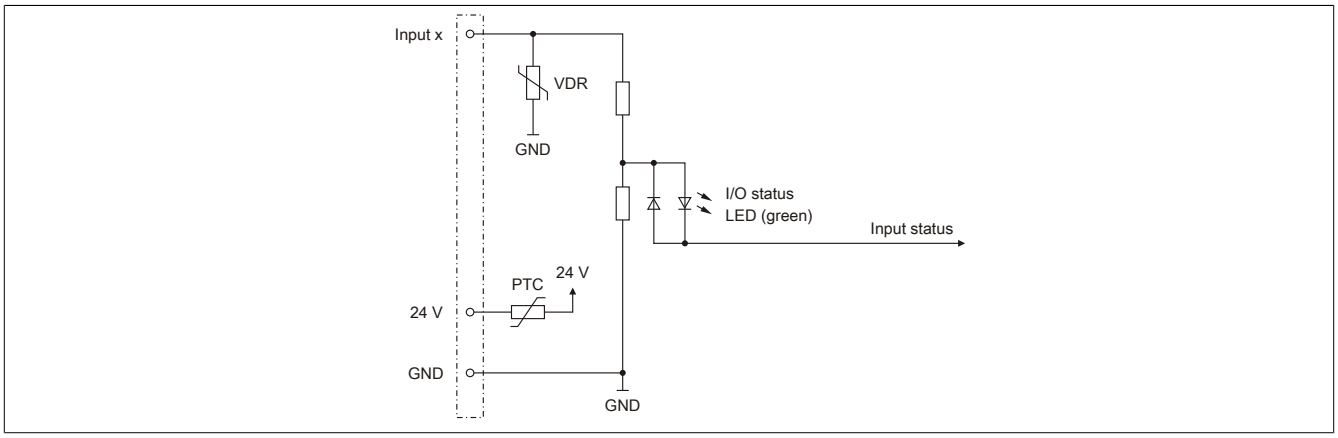
4.13.3.5 Pinout



4.13.3.6 Connection example

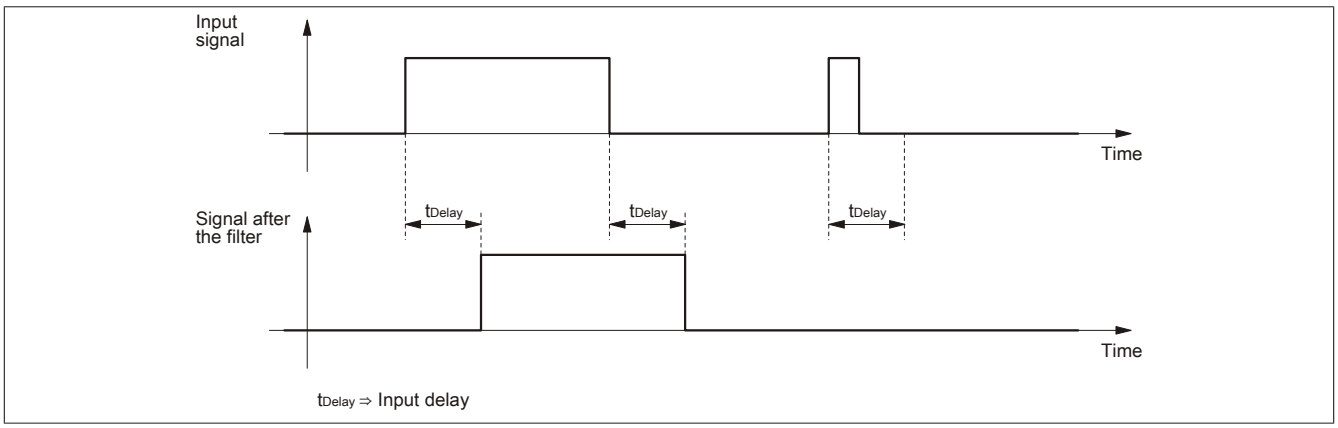


4.13.3.7 Input circuit diagram



4.13.3.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.3.9 Register description

4.13.3.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.3.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		DigitalInput02	Bit 1				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.3.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	Input status of digital inputs 1 to 2	USINT	•			
		DigitalInput01	Bit 0				
		DigitalInput02	Bit 1				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.3.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.3.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.3.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.3.9.4.2 Input status of digital inputs 1 to 2

Name:
DigitalInput or
DigitalInput01 to DigitalInput02

The input status of digital inputs 1 to 2 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput02") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 3	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
1	DigitalInput02	0 or 1	Input status - Digital input 2

4.13.3.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.3.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.4 X20DI2372

4.13.4.1 General Information

The module is equipped with 2 inputs for 3-wire connections.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 digital inputs
- Source connection
- 3-wire connections
- 24 VDC and GND for sensor supply
- Software input filter can be configured for entire module

4.13.4.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI2372	X20 digital input module, 2 inputs, 24 VDC, source, configurable input filter, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 260: X20DI2372 - Order data

4.13.4.3 Technical data

Product ID	X20DI2372
Short description	
I/O module	2 digital inputs 24 VDC for 3-wire connections
General information	
B&R ID code	0x22A7
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.12 W
Internal I/O	0.29 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 3.75 mA
Input filter	
Hardware	≤100 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	3-wire connections
Input circuit	Source
Input resistance	Typ. 6.4 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Sensor supply	
Power consumption	Max. 12 W 2)
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 VDC
Summation current	0.5 A
Short circuit protection	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 261: X20DI2372 - Technical data

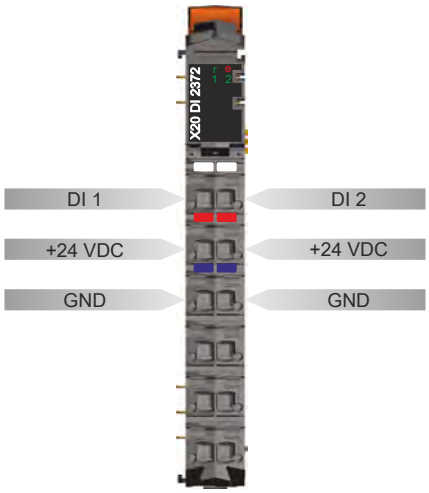
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.13.4.4 Status LEDs

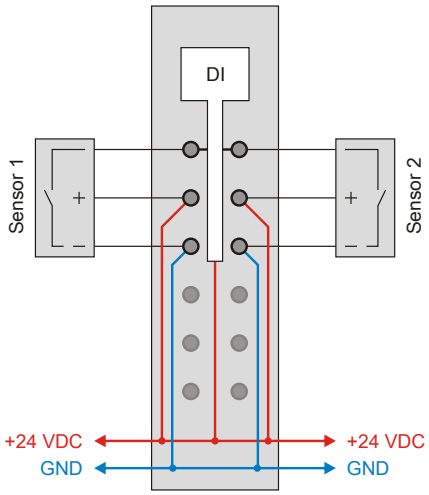
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green		Input status of the corresponding digital input

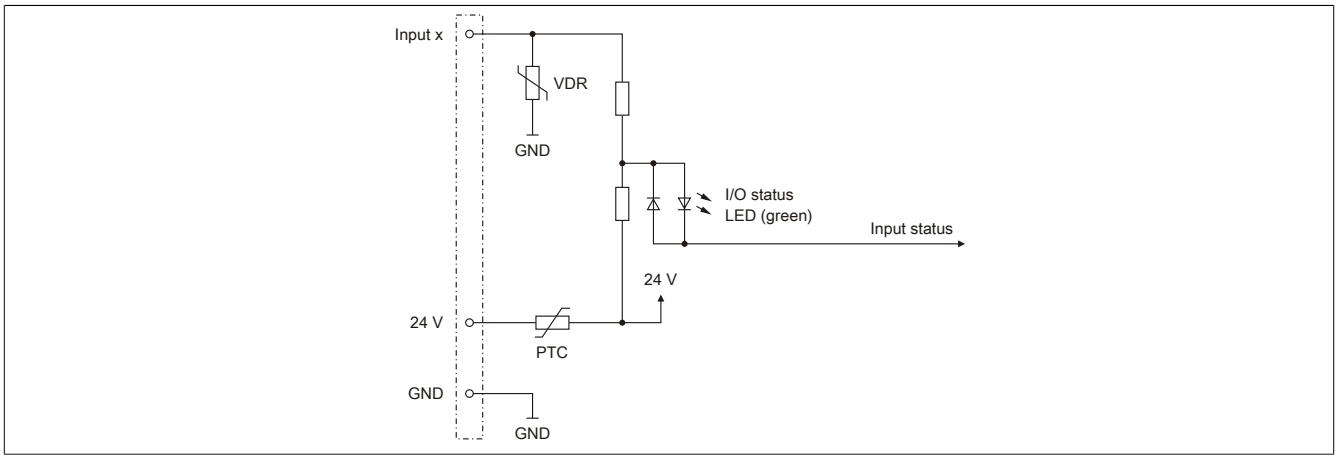
4.13.4.5 Pinout



4.13.4.6 Connection example

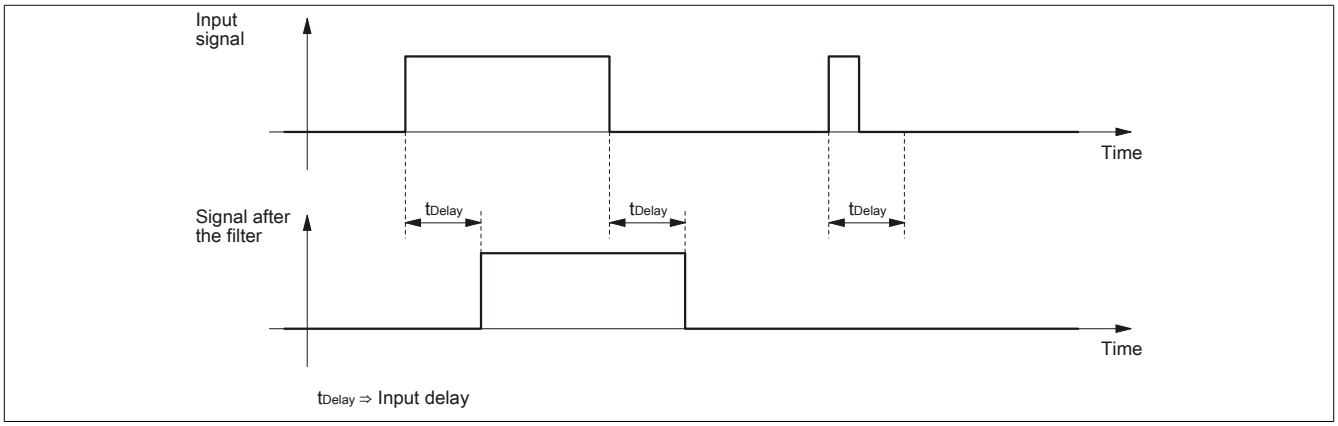


4.13.4.7 Input circuit diagram



4.13.4.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.4.9 Register description

4.13.4.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.4.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		DigitalInput02	Bit 1				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.4.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	Input status of digital inputs 1 to 2	USINT	•			
		DigitalInput01	Bit 0				
		DigitalInput02	Bit 1				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.4.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.4.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.4.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.4.9.4.2 Input status of digital inputs 1 to 2

Name:
DigitalInput or
DigitalInput01 to DigitalInput02

The input status of digital inputs 1 to 2 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput02") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 3	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
1	DigitalInput02	0 or 1	Input status - Digital input 2

4.13.4.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.4.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.5 X20DI2377

4.13.5.1 General Information

The module is equipped with two inputs for 3-wire connections. Both inputs can be configured as event counters. Gate measurement is only ever possible on one channel.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 digital inputs
- Sink connection
- 3-wire connections
- 2 counter inputs with 50 kHz counter frequency
- Gate measurement
- 24 VDC and GND for sensor supply
- Software input filter can be configured for entire module

4.13.5.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI2377	X20 digital input module, 2 inputs, 24 VDC, sink, configurable input filter, 2 event counters 50 kHz, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 262: X20DI2377 - Order data

4.13.5.3 Technical data

Product ID	X20DI2377
Short description	
I/O module	2 digital inputs 24 VDC for 3-wire connections, special functions
General information	
B&R ID code	0x1B8E
Status indicators	I/O function per channel, operating state, module status
Diagnostics Module run/error	 Yes, using status LED and software
Power consumption Bus Internal I/O	 0.15 W 0.82 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation Channel - Bus Channel - Channel	 Yes No
Certification CE cULus cCSAus HazLoc Class 1 Division 2 ATEX Zone 2 [1)] KC GL LR GOST-R	 Yes Yes Yes Yes Yes Yes Yes Yes
Digital inputs	
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %

Table 263: X20DI2377 - Technical data

Product ID	X20DI2377
Input current at 24 VDC	Typ. 10.5 mA
Input filter	
Hardware	≤10 µs
Software	Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	3-wire connections
Input circuit	Sink
Additional functions	50 kHz event counting, gate measurement
Input resistance	Typ. 2.23 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Event counter	
Quantity	2
Signal form	Square wave pulse
Evaluation	Every rising edge, cyclic counter
Input frequency	Max. 50 kHz
Counter 1	Input 1
Counter 2	Input 2
Counter frequency	Max. 50 kHz
Counter size	16-bit
Gate measurement	
Number of gate measurements	1
Signal form	Square wave pulse
Evaluation	Rising edge - falling edge
Counter frequency	
Internal	48 MHz, 24 MHz, 12 MHz, 6 MHz, 3 MHz, 1.5 MHz, 750 kHz, 375 kHz, 187.5 kHz
Counter size	16-bit
Length of pause between pulses	≥100 µs
Pulse length	≥20 µs
Supported inputs	Input 1 or Input 2
Sensor supply	
Power consumption	Max. 12 W [2]
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 VDC
Summation current	0.5 A
Short circuit protection	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 263: X20DI2377 - Technical data

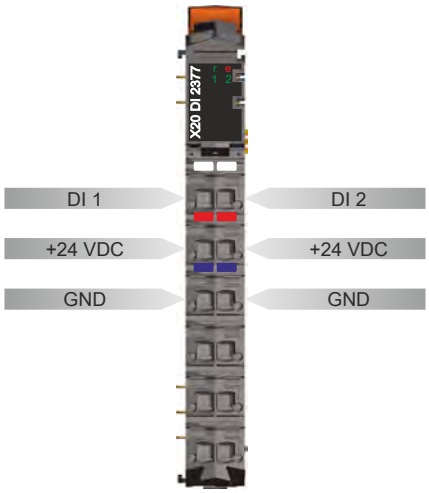
1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.13.5.4 Status LEDs

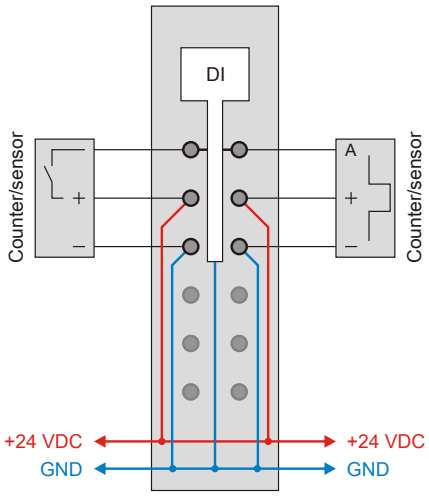
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green		Input status of the corresponding digital input

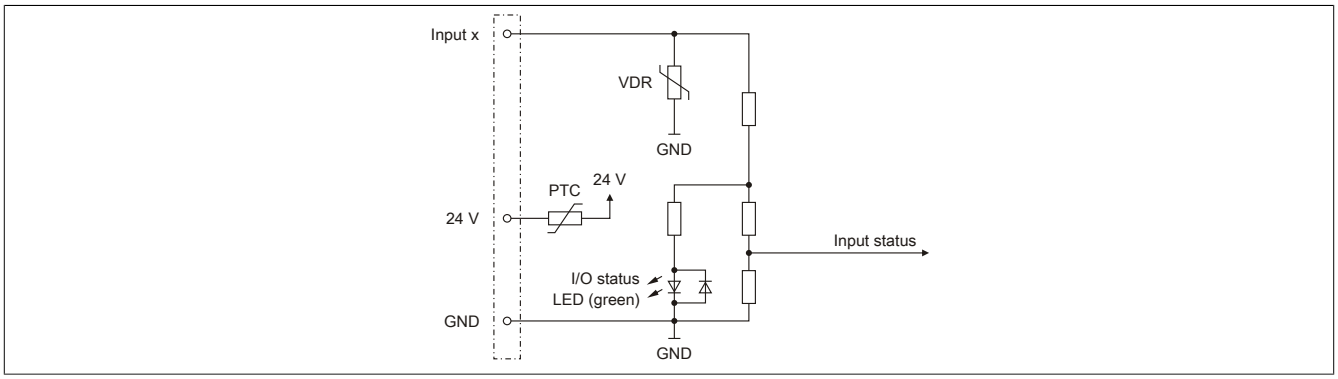
4.13.5.5 Pinout



4.13.5.6 Connection example

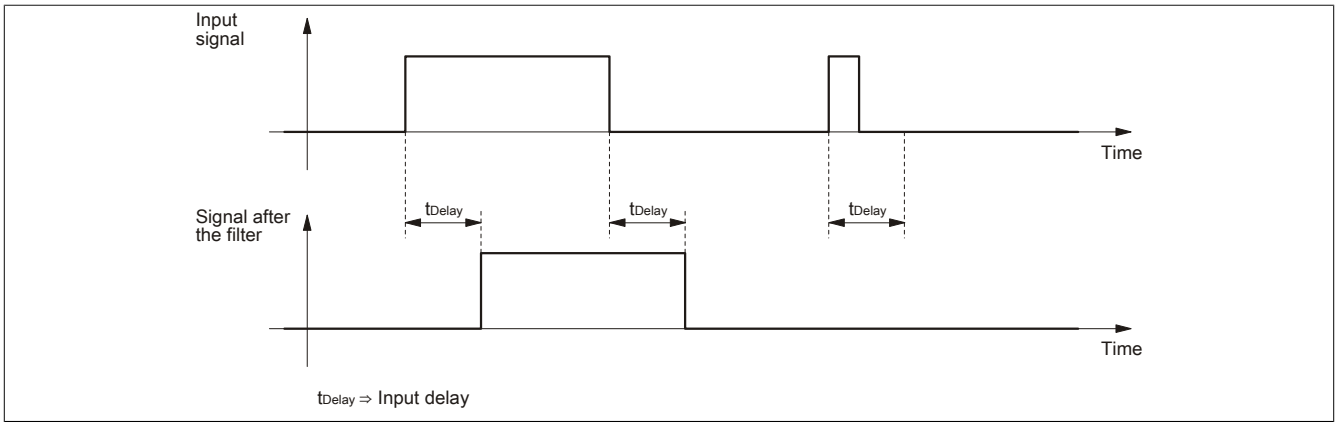


4.13.5.7 Input circuit diagram



4.13.5.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



Information:

The input filter is applied to digital inputs in event counter mode with software

The input filter is NOT applied in event counter mode without software.

4.13.5.9 Register description

4.13.5.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.5.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
0	DigitalInput	USINT	•			
	DigitalInput01	Bit 0				
	DigitalInput02	Bit 1				
4	Counter01	USINT	•			
6	Counter02	USINT	•			
20	Counter configuration	USINT			•	
	ResetCounter01	Bit 5				
22	Counter configuration	USINT			•	
	ResetCounter02	Bit 5				
18	ConfigOutput01	USINT				•
20	ConfigOutput02	USINT				•
22	ConfigOutput03	USINT				•

4.13.5.9.3 Function model 1 - Input latch

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
26	Input status of digital latch inputs 1 - 2	USINT	•			
	DigitalInputLatch01	Bit 0				
	DigitalInputLatch02	Bit 1				
28	Acknowledge digital inputs	USINT			•	
	DigitalInput01LatchQuitt	Bit 0				
	DigitalInput02LatchQuitt	Bit 1				
4	Counter01	USINT	•			
6	Counter02	USINT	•			
20	Counter configuration	USINT			•	
	ResetCounter01	Bit 5				
22	Counter configuration	USINT			•	
	ResetCounter02	Bit 5				
18	ConfigOutput01	USINT				•
20	ConfigOutput02	USINT				•
22	ConfigOutput03	USINT				•

4.13.5.9.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
4	0	Counter01	USINT	•			
6	2	Counter02	USINT	•			
20	-	Counter configuration	USINT				•
		ResetCounter01	Bit 5				
22	-	Counter configuration	USINT				•
		ResetCounter02	Bit 5				
18	-	ConfigOutput01	USINT				•
20	-	ConfigOutput02	USINT				•
22	-	ConfigOutput03	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.5.9.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.13.5.9.5 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.5.9.5.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.5.9.5.2 Input status of digital inputs 1 to 2

Name:
DigitalInput or
DigitalInput01 to DigitalInput02

The input status of digital inputs 1 to 2 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput02") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 3	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
1	DigitalInput02	0 or 1	Input status - Digital input 2

4.13.5.9.5.3 Input status of digital latch inputs 1 - 2

Name:
DigitalInputLatch01 to DigitalInputLatch02

The input status of digital inputs 1 to 2 after expiration of the input filter time is mapped in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInputLatch01	0 or 1	Input status of digital input 1 after expiration of the delay time
1	DigitalInputLatch02	0 or 1	Input status of digital input 2 after expiration of the delay time

4.13.5.9.6 Counter operation

The following operation modes can be selected:

- Event counter mode
- Event counter mode with software (processed after the input filter)
- Gate measurement

Event counter mode

The rising (positive) edges are registered on the counter input.

The counter state is registered with a fixed offset with respect to the network cycle and transferred in the same cycle.

Event counter mode with software

The rising (positive) edges are registered on the counter input. But the edges are first processed through the configured software filter.

The counter state is registered with a fixed offset with respect to the network cycle and transferred in the same cycle.

Gate measurement

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF) and corrected with the adjustable prescaler.

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

Information:

Only one of the counter channels at a time can be used for gate measurement.

4.13.5.9.6.1 Event or gate counter

Name:
Counter01 to Counter02

This register displays the results of the individual counters.

Event counter or gate measurement (16-bit counter value) depending on operating mode.

Data type	Value
USINT	Counter value

4.13.5.9.6.2 Counter configuration

Name:
ConfigOutput02 to ConfigOutput03

This register can be used to configure the individual counters.

Data type	Value
USINT	See bit structure.

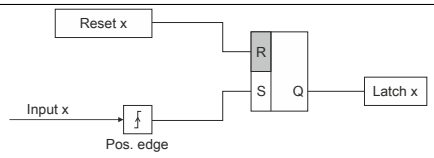
Bit structure:

Bit	Name	Value	Information
0 - 3	Counter frequency	0	48 MHz (only with gate measurement)
		1	3 MHz (only with gate measurement)
		1	**Event counter** via software (only in event counter operation)
		2	187.5 kHz (only with gate measurement)
		3	24 MHz (only with gate measurement)
		4	12 MHz (only with gate measurement)
		5	6 MHz (only with gate measurement)
		6	1.5 MHz (only with gate measurement)
		7	750 kHz (only with gate measurement)
		8	375 kHz (only with gate measurement)
4	Reserved	0	
5	ResetCounter01 or ResetCounter02	0	No influence on the counter
		1	Clear counter (at rising edge)
6 - 7		0	Event counter measurement
		1	Gate measurement

4.13.5.9.7 Rising edge input latch

Using this function, the rising edges of the input signal can be latched with a resolution of 200 µs. With the "Acknowledge - input latch" function, the input latch is either reset or prevented from latching.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	Status
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

4.13.5.9.7.1 Acknowledge digital inputs

Name:
DigitalInput01LatchQuitt to DigitalInput02LatchQuitt

This register is used to reset the input latches channel by channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01LatchQuitt	0	No influence on the latch status
		1	Resets the latch status
1	DigitalInput02LatchQuitt	0	No influence on the latch status
		1	Resets the latch status
2 - 7	Reserved	-	

4.13.5.9.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

4.13.5.9.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs

4.13.6 X20DI2653

4.13.6.1 General Information

The module is equipped with 2 inputs for 3-wire connections. It is designed for an input voltage of 100 to 240 VAC.

- 2 digital inputs
- 100 to 240 VAC inputs
- 50 Hz or 60 Hz
- 3-wire connections
- 240 V coded

Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.13.6.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI2653	X20 digital input module, 2 inputs, 100 to 240 VAC, 240 V keyed, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 264: X20DI2653 - Order data

4.13.6.3 Technical data

Product ID	X20DI2653
Short description	
I/O module	2 digital inputs 100 to 240 VAC for 3-wire connections
General information	
B&R ID code	0x2544
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
External I/O supply	Yes, using software (typical threshold 85 VAC)
Power consumption	
Bus	0.14 W
Internal I/O	-
External I/O	0.55 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	100 to 240 VAC
Input filter	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Hardware	
1 -> 0	≤30 ms
0 -> 1	≤40 ms
Connection type	3-wire connections
Rated frequency	47 to 63 Hz
Switching threshold	
Low	<40 VAC
High	>79 VAC
Isolation voltage between channel and bus	1 minute 2500 VAC
Input voltage	
Maximum	264 VAC
Input current	
100 VAC / 60 Hz	4 mA (Rev. ≥ E0), 5 mA (Rev. < E0)
240 VAC / 50 Hz	8.5 mA (Rev. ≥ E0), 11 mA (Rev. < E0)
Sensor supply	
Voltage	Equal to the module supply
Summation current	2 A_{eff}
Short circuit protection	No
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM12 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 265: X20DI2653 - Technical data

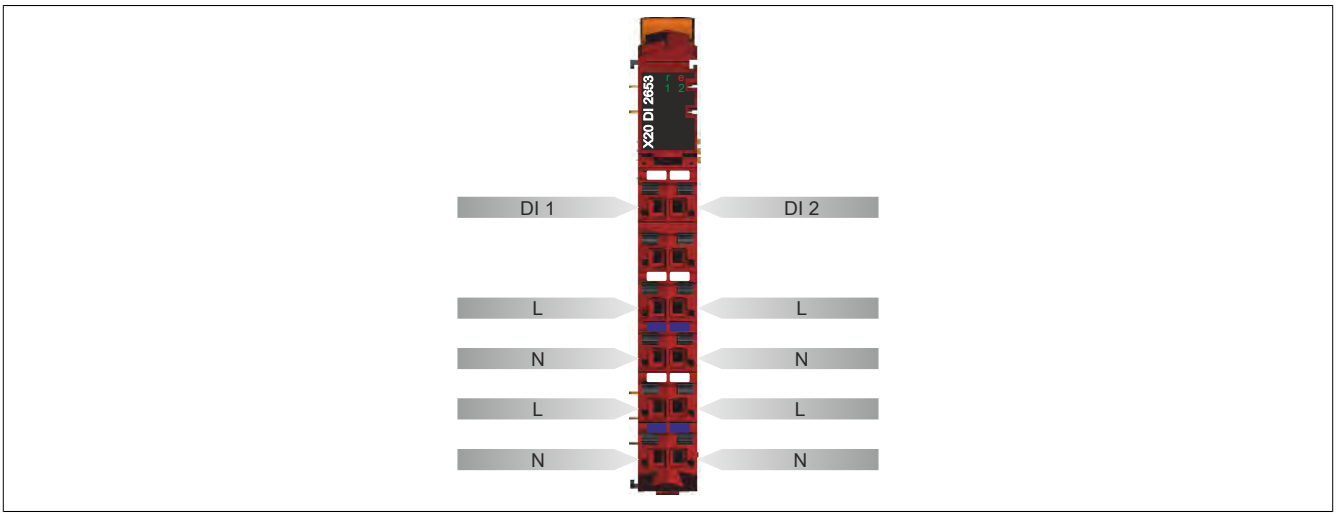
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.6.4 Status LEDs

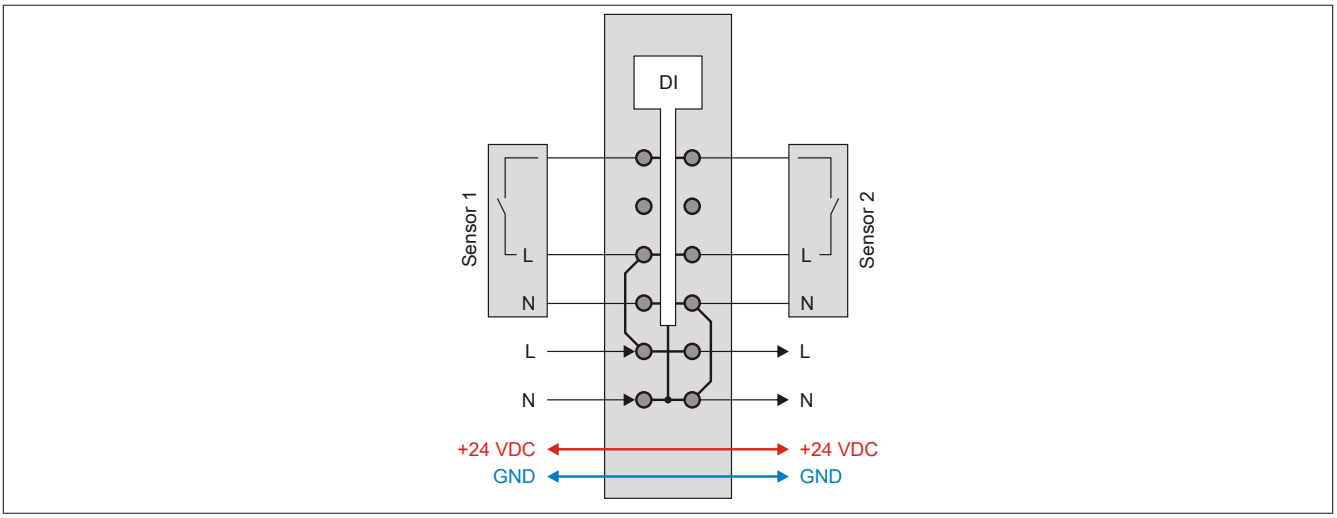
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Double flash	External supply is too low or not connected
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green		Input status of the corresponding digital input

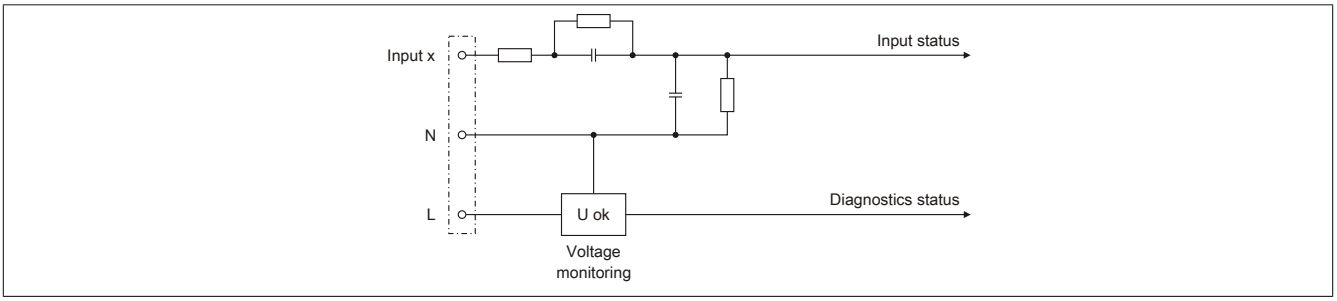
4.13.6.5 Pinout



4.13.6.6 Connection example

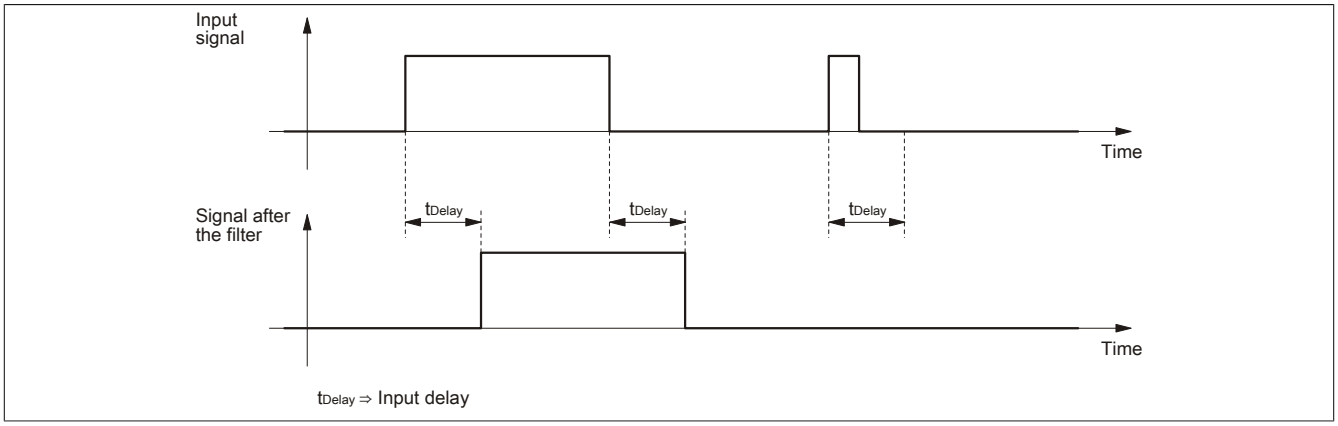


4.13.6.7 Input circuit diagram



4.13.6.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.6.9 Register description

4.13.6.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.6.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		DigitalInput02	Bit 1				
		PowerSupply	Bit 7				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.6.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 2	USINT	•			
		DigitalInput01	Bit 0				
		DigitalInput02	Bit 1				
		PowerSupply	Bit 7				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.6.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.6.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.6.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.6.9.4.2 Input status of digital inputs 1 to 2

Name:
DigitalInput or
DigitalInput01 to DigitalInput02
PowerSupply

The input status of digital inputs 1 to 2 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01", "DigitalInput02" and "PowerSupply") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 255	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
1	DigitalInput02	0 or 1	Input status - Digital input 2
2 - 6	Reserved	0	
7	PowerSupply	0	Supply voltage too low
		1	Supply voltage >80 VAC

4.13.6.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.6.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.7 X20(c)DI4371

4.13.7.1 General Information

The module is equipped with four inputs for 3-wire connections.

- 4 digital inputs
- Sink connection
- 3-wire connections
- 4 counter inputs with 1 kHz counter frequency
- 24 VDC and GND for sensor supply
- Software input filter can be configured for entire module

4.13.7.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.13.7.3 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI4371	X20 digital input module, 4 inputs, 24 VDC, sink, configurable input filter, 3-wire connections	
X20cDI4371	X20 digital input module, coated, 4 inputs, 24 VDC, sink, configurable input filter, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 266: X20DI4371, X20cDI4371 - Order data

4.13.7.4 Technical data

Product ID	X20DI4371	X20cDI4371
Short description		
I/O module	4 digital inputs 24 VDC for 3-wire connections	
General information		
B&R ID code	0x1B92	0xE21F
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Power consumption		
Bus	0.14 W	
Internal I/O	0.59 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Digital inputs		
Nominal voltage	24 VDC	
Input voltage	24 VDC -15% / +20%	
Input current at 24 VDC	Typ. 3.75 mA	
Input filter		
Hardware	≤100 µs	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Connection type	3-wire connections	
Input circuit	Sink	
Input resistance	Typ. 6.4 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Event counter		
Quantity	4	
Signal form	Square wave pulse	
Evaluation	Configurable edge event, cyclic counter	
Input frequency	Max. 1 kHz	
Counter 1	Input 1	
Counter 2	Input 2	
Counter 3	Input 3	
Counter 4	Input 4	
Counter frequency	Max. 1 kHz (when input filter switched off)	
Counter size	16-bit	
Sensor supply		
Power consumption	Max. 12 W [2]	
Voltage	Module supply minus voltage drop for short circuit protection	
Voltage drop for short circuit protection at 500 mA	Max. 2 VDC	
Summation current	0.5 A	
Short circuit protection	Yes	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 267: X20DI4371, X20cDI4371 - Technical data

Product ID	X20DI4371	X20cDI4371
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 267: X20DI4371, X20cDI4371 - Technical data

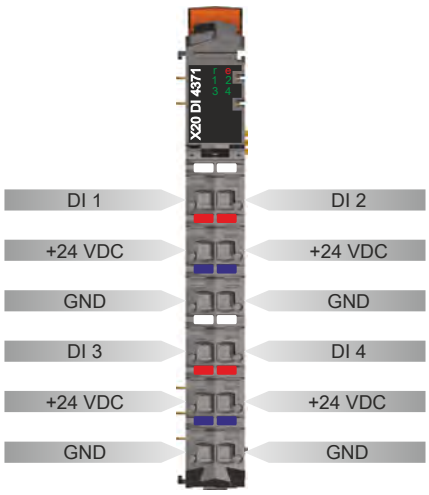
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.13.7.5 Status LEDs

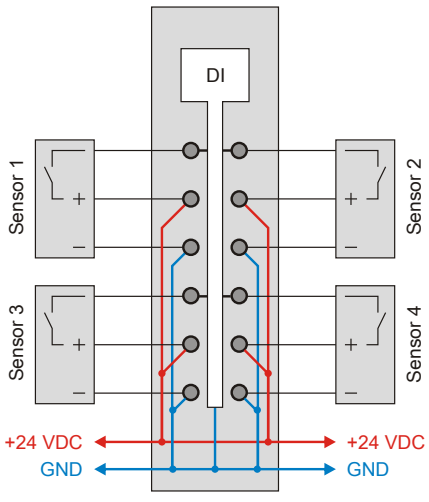
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green		Input status of the corresponding digital input

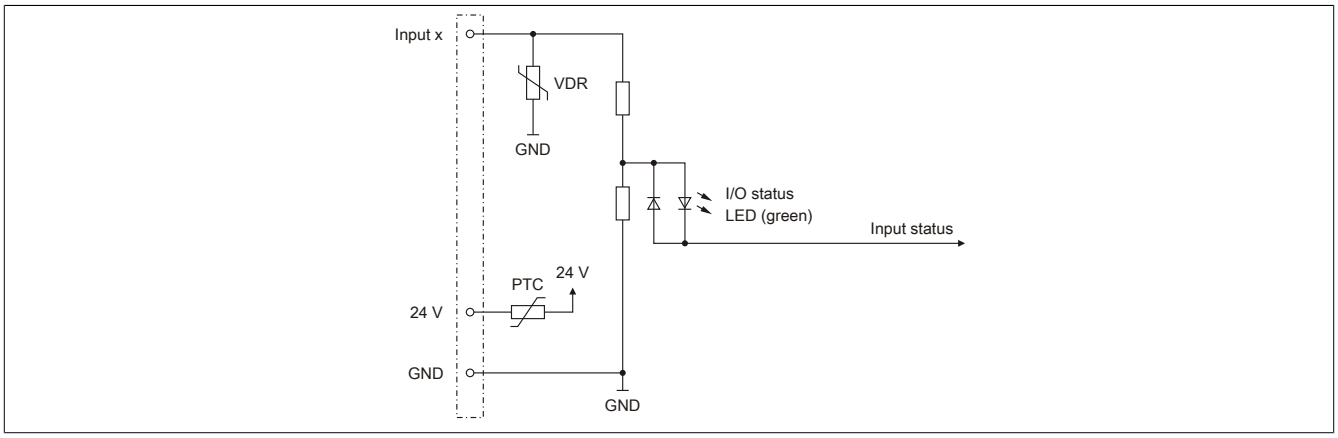
4.13.7.6 Pinout



4.13.7.7 Connection example

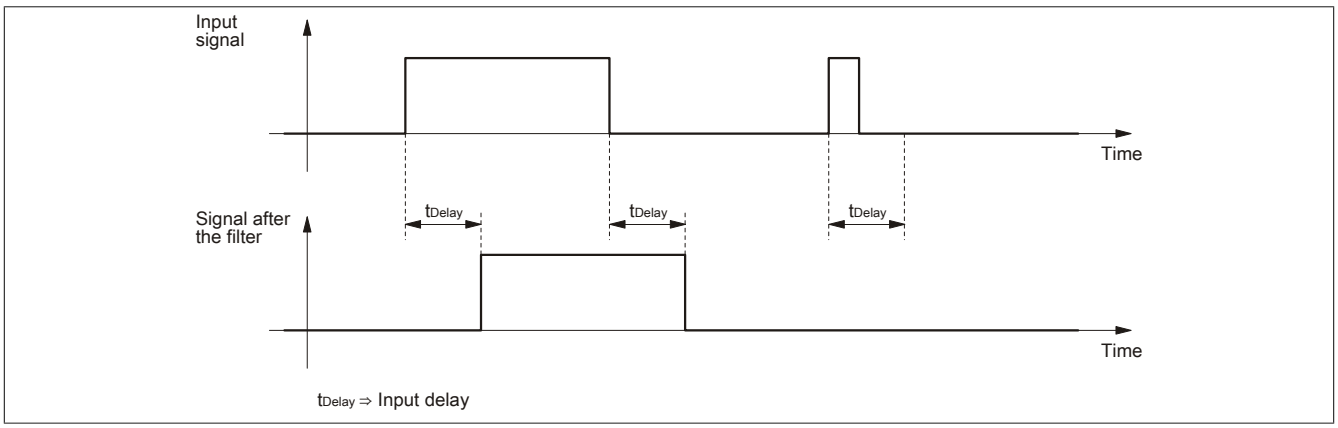


4.13.7.8 Input circuit diagram



4.13.7.9 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.7.10 Register description

4.13.7.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.7.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.7.10.3 Function model 1 - Event counter

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	Input status of digital inputs 1 to 4	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
4	2	Counter01	UINT	•			
6	4	Counter02	UINT	•			
8	6	Counter03	UINT	•			
10	8	Counter04	UINT	•			
12	0	Resets the counter registers	USINT			•	
		ResetCounter01	Bit 0				
		...	...				
		ResetCounter04	Bit 3				
18	-	ConfigOutput01	USINT				•
14	-	ConfigOutput02	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.7.10.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 4	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.7.10.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.7.10.5 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.7.10.5.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.7.10.5.2 Input status of digital inputs 1 to 4

Name:
DigitalInput or
DigitalInput01 to DigitalInput04

The input status of digital inputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput04") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 15	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input status - Digital input 4

4.13.7.10.6 The event counter function model

Starting with hardware variant F0 and firmware version 801, the module has four software counters for signal edges. Each counter register can be configured individually for falling, rising or both edges.

4.13.7.10.6.1 Counter register

Name:
Counter01 to Counter04

These registers provide the current counter value for the configured events.

Data type	Value
UINT	0 to 65535

4.13.7.10.6.2 Resets the counter registers

Name:
ResetCounter01 to ResetCounter04

Using these data points, the corresponding counter registers can be reset to 0.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	ResetCounter01	0	No change
		1	Counter register 1 is reset
...		...	
3	ResetCounter04	0	No change
		1	Counter register 4 is reset

Information:

A counter is only reset if a positive edge is detected on the reset bit.

A continually set reset bit does not prevent counting in the counter register.

4.13.7.10.6.3 Configuration of the edges

Name:
ConfigOutput02

This register is used to configure which event will be assessed on the channel input for the respective counter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Rising edge on input 1	0	Event is not counted
		1	Event increments Counter01
...		...	
3	Rising edge on input 4	0	Event is not counted
		1	Event increments Counter04
4	Falling edge on input 1	0	Event is not counted
		1	Event increments Counter01
...		...	
7	Falling edge on input 4	0	Event is not counted
		1	Event increments Counter04

4.13.7.10.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.7.10.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.8 X20DI4372

4.13.8.1 General Information

The module is equipped with 4 inputs for 3-wire connections.

- 4 digital inputs
- Source connection
- 3-wire connections
- 24 VDC and GND for sensor supply
- Software input filter can be configured for entire module

4.13.8.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI4372	X20 digital input module, 4 inputs, 24 VDC, source, configurable input filter, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 268: X20DI4372 - Order data

4.13.8.3 Technical data

Product ID	X20DI4372
Short description	
I/O module	4 digital inputs 24 VDC for 3-wire connections
General information	
B&R ID code	0x22A8
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.14 W
Internal I/O	0.59 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 3.75 mA
Input filter	
Hardware	≤100 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	3-wire connections
Input circuit	Source
Input resistance	Typ. 6.4 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Sensor supply	
Power consumption	Max. 12 W 2)
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 VDC
Summation current	0.5 A
Short circuit protection	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 269: X20DI4372 - Technical data

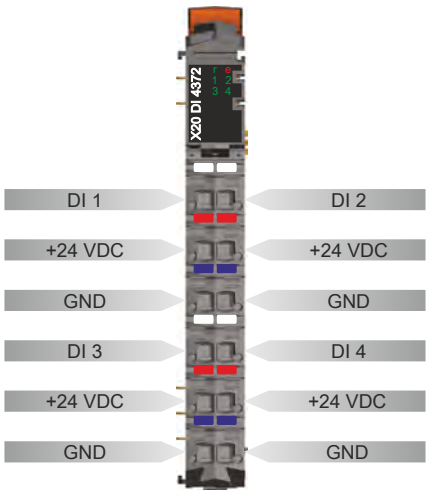
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.13.8.4 Status LEDs

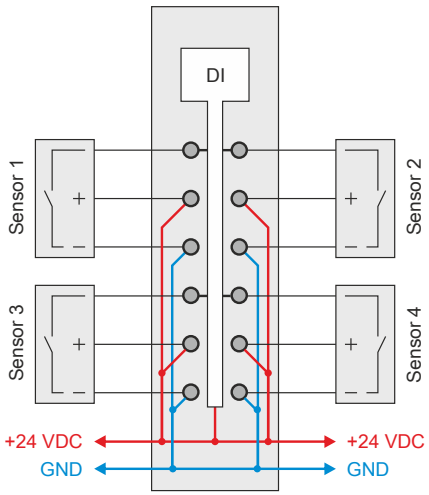
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green		Input status of the corresponding digital input

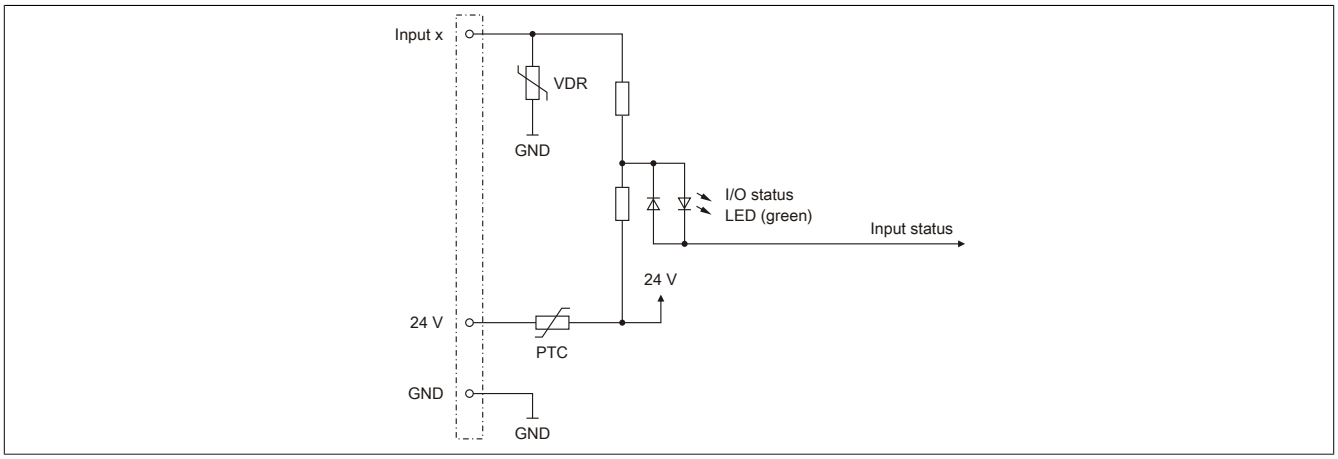
4.13.8.5 Pinout



4.13.8.6 Connection example

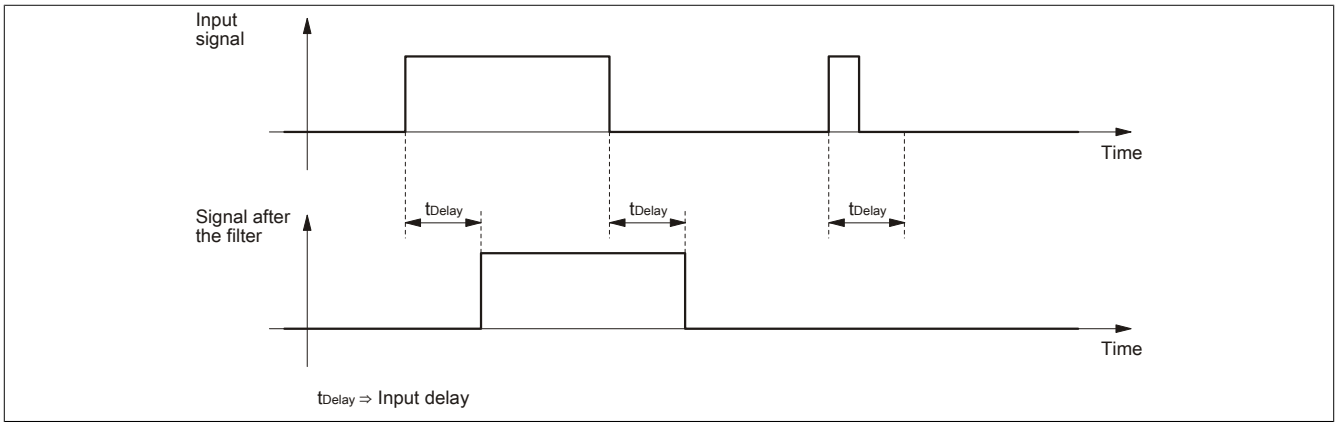


4.13.8.7 Input circuit diagram



4.13.8.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.8.9 Register description

4.13.8.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.8.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.8.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 4	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.8.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.8.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.8.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.8.9.4.2 Input status of digital inputs 1 to 4

Name:
DigitalInput or
DigitalInput01 to DigitalInput04

The input status of digital inputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput04") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 15	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input status - Digital input 4

4.13.8.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.8.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.9 X20(c)DI4375

4.13.9.1 General Information

The module is equipped with 4 inputs for 3-wire connections. It has open circuit and short circuit detection. This detection can be switched off individually for each channel.

- 4 digital inputs
- Sink connection
- 3-wire connections
- 24 VDC and GND for sensor supply
- Open circuit and short circuit detection, can be switched off individually for each channel
- Software input filter can be configured for entire module

4.13.9.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.13.9.3 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI4375	X20 digital input module, 4 inputs, 24 VDC, sink, configurable input filter, open line and short circuit detection, 3-wire connections	
X20cDI4375	X20 digital input module, coated, 4 inputs, 24 VDC, sink, configurable input filter, open line and short circuit detection, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 270: X20DI4375, X20cDI4375 - Order data

4.13.9.4 Technical data

Product ID	X20DI4375	X20cDI4375
Short description		
I/O module	4 digital inputs 24 VDC for 3-wire connections, open line and short circuit detection, detection can be switched off individually for each channel	
General information		
B&R ID code	0xA911	0xE220
Status indicators	I/O function per channel, operating state, module status, sensor line, sensor supply	
Diagnostics		
Module run/error	Yes, using status LED and software	
Open line	Yes, using status LED and software	
Short circuit	Yes, using status LED and software	
Sensor supply	Yes, using status LED and software	
Other channel errors	Yes, using status LED and software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.1 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 1)	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Digital inputs		
Nominal voltage	24 VDC	
Input filter		
Hardware	0.8 ms	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Connection type	3-wire connections	
Input circuit	Sink	
Sensor supply	4x 50 mA	
Open circuit and short circuit detection	Yes, can be switched off individually for each channel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 271: X20DI4375, X20cDI4375 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.9.5 Status LEDs

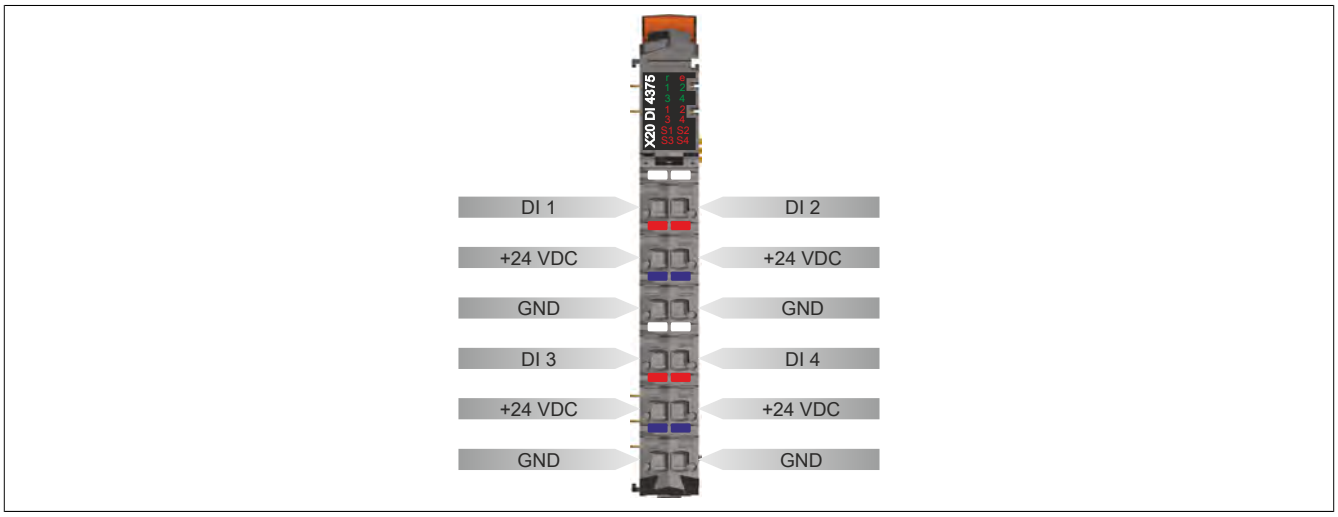
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Summary status for channel error → Check the red channel LEDs 1 - 4
			Double flash	Module supply below lower limit
			Triple flash	Converter error (or transition between single and double flash)
	1 - 4	Green		Input status of the corresponding digital input
	1 - 4	Red	Off	No error detected
			Single flash	Short circuit of respective digital input with +24 VDC
			Blinking	Open circuit or the measured value is below the lower switch off threshold
			Single flash, inverse	Other channel error
	S1 - S4	Red	Off	Sensor supply OK
			On	Sensor supply monitor has detected something

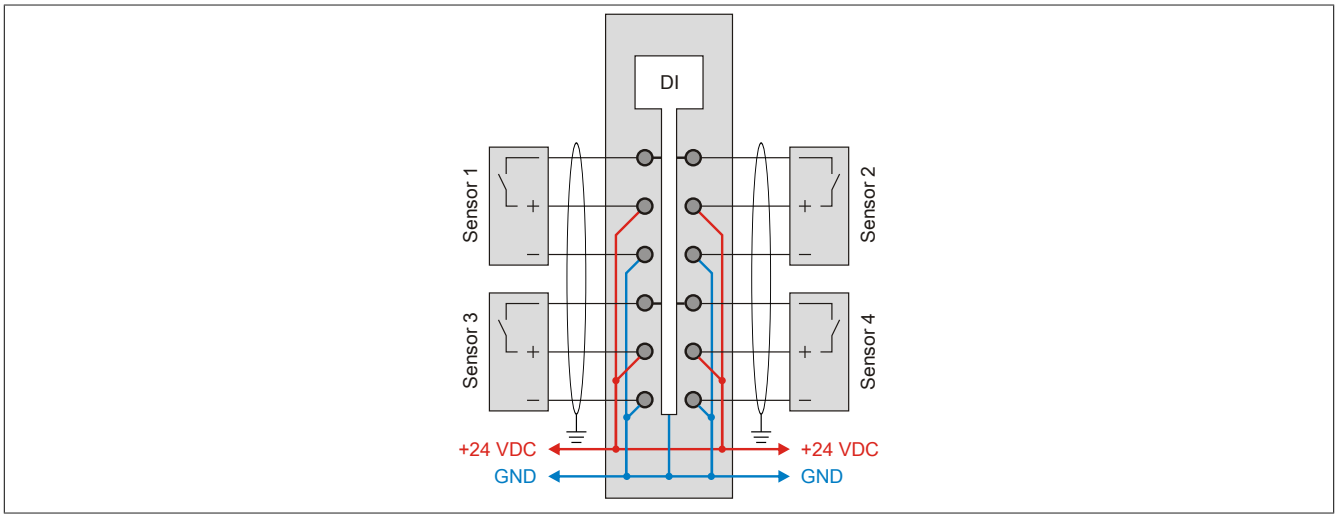
1) Depending on the configuration, a firmware update can take up to several minutes.

4.13.9.6 Pinout

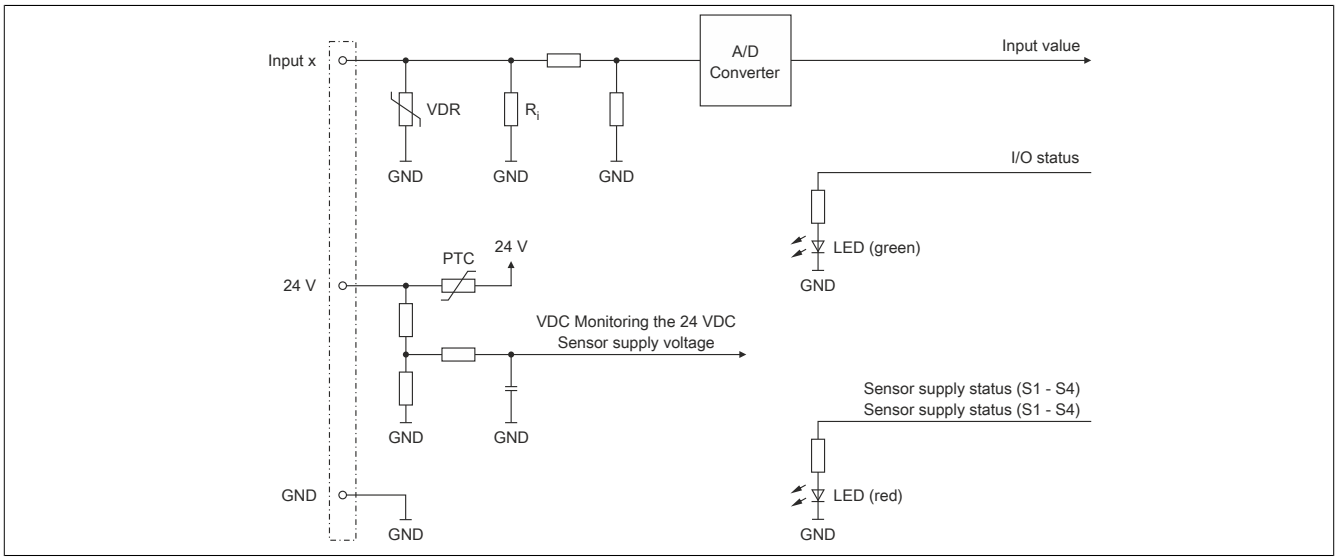
Shielded cables should be used for all connections.



4.13.9.7 Connection example

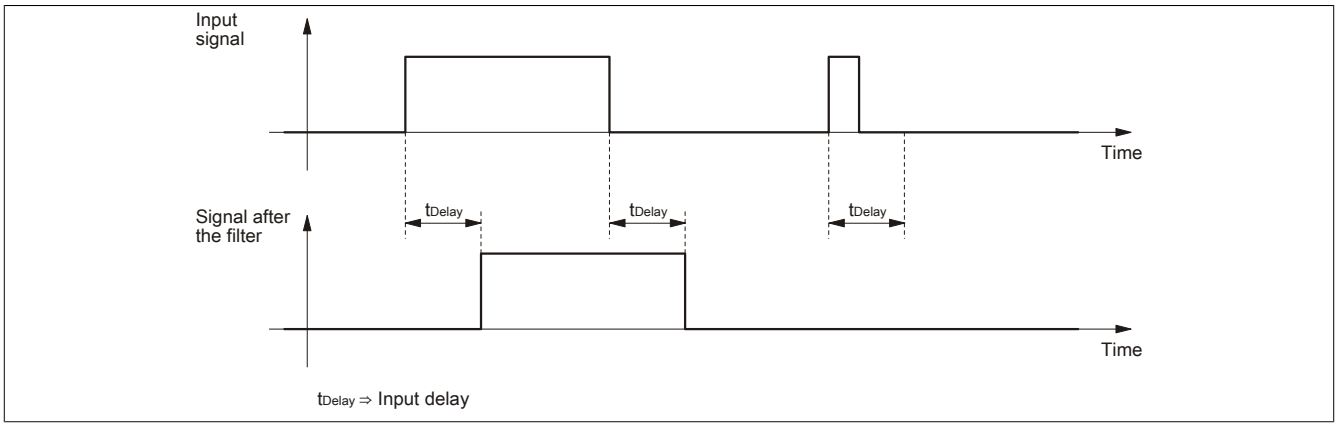


4.13.9.8 Input circuit diagram



4.13.9.9 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.9.14.4.1 "ConfigOutput02" on page 1260. Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.9.10 Open circuit and short circuit detection

General Information

The X20DI4375 digital input module is equipped with open line and short circuit detection. To do this the sensor needs to be connected to the necessary resistances.

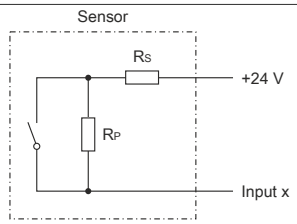
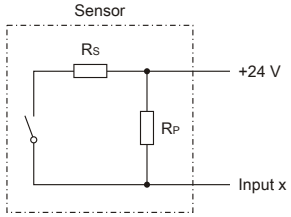
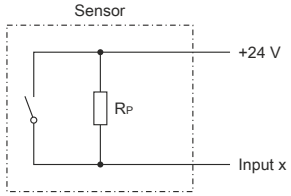
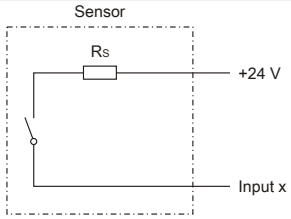
Sensor connections

The resistances are connected to the sensor parallel or in series. The following values are defined for the resistances:

Resistance	Range
Serial	1 - 2 kΩ (10%)
Parallel	10 - 20 kΩ (10%)

Connection options

To guarantee error-free functionality of the open circuit and short circuit detection, the +24 VDC sensor supply from the module must absolutely be used.

Sensor connections	Description	Detection	Setting in configuration register
	Standard connection	-	0
	Series and parallel resistance	Open circuit and short circuit	1
	Parallel and series resistor	Open circuit and short circuit	2
	Parallel resistance	Open line	3
	Series resistor	Short circuit	4

4.13.9.11 Error status

The following errors are detected by the module and can be evaluated separately for each channel:

- Sensor line short circuit
- Sensor line open circuit
- Sensor supply
- Other channel error

4.13.9.12 Timestamp

Each converted value is given a timestamp. The time of the last conversion can be read.

4.13.9.13 Configuration

The sensor connections and therefore the sensor monitoring are set in the configuration register. Sensor monitoring and the settings in the configuration register are described in section 4.13.9.10 "Open circuit and short circuit detection" on page 1257.

4.13.9.14 Register description

4.13.9.14.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.9.14.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2305	DigitalInput	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput04	Bit 3				
	StateDigitalInput01	Bit 4				
	...	...				
	StateDigitalInput04	Bit 7				
2307	StatusInput01	USINT	•			
	SC_DigitalInput01	Bit 0				
	...	...				
	SC_DigitalInput04	Bit 3				
2309	StatusInput02	USINT	•			
	WB_DigitalInput01	Bit 0				
	...	...				
	WB_DigitalInput04	Bit 3				
2311	StatusInput03	USINT	•			
	SM_DigitalInput01	Bit 0				
	...	...				
	SM_DigitalInput04	Bit 3				
2313	StatusInput04		•			
	IE_DigitalInput01	Bit 0				
	...	...				
	IE_DigitalInput01	Bit 3				
2324	SampleTimeStamp	UDINT	•			
2050	ConfigOutput01	UINT				•
2053	ConfigOutput02	USINT				•

4.13.9.14.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2305	0	Input status of digital inputs 1 to 4	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
		StateDigitalInput01	Bit 4				
		...	...				
		StateDigitalInput04	Bit 7				
2307	-	Short circuit monitoring of channels 1 to 4	USINT		•		
		SC_DigitalInput01	Bit 0				
		...	...				
		SC_DigitalInput04	Bit 3				
2309	-	Open line monitoring on channels 1 to 4	USINT		•		
		WB_DigitalInput01	Bit 0				
		...	...				
		WB_DigitalInput04	Bit 3				
2311	-	Voltage monitoring on channels 1 to 4	USINT		•		
		SM_DigitalInput01	Bit 0				
		...	...				
		SM_DigitalInput04	Bit 3				
2313	-	Error monitoring on channels 1 to 4			•		
		IE_DigitalInput01	Bit 0				
		...	...				
		IE_DigitalInput01	Bit 3				
2324	-	SampleTimeStamp	UDINT		•		
2050	-	ConfigOutput01	UINT				•
2053	-	ConfigOutput02	USINT				•

1) The offset specifies the position of the register within the CAN object.

4.13.9.14.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.9.14.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.9.14.4.1 Digital input filter

Name:
ConfigOutput02

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.9.14.4.2 Input status of digital inputs 1 to 4

Name:
DigitalInput or
DigitalInput01 to DigitalInput04
StateDigitalInput01 to StateDigitalInput04

The input status and status of digital inputs 1 to 4 are mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput04" and "StateDigitalInput01" through "StateDigitalInput04") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 255	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input status - Digital input 4
4	StateDigitalInput01	0	No error
		1	Short-circuit, open line, sensor monitoring error or other channel error
...		...	
7	StateDigitalInput04	0	No error
		1	Short-circuit, open line, sensor monitoring error or other channel error

4.13.9.14.5 Short circuit monitoring of channels 1 to 4

Name:
StatusInput01 or
SC_DigitalInput01 to SC_DigitalInput04

This register indicates whether a short circuit has occurred on the individual channels.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("SC_DigitalInput01" through "SC_DigitalInput04") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 15	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	SC_DigitalInput01	0	No error
		1	Short circuit on channel 1
...		...	
3	SC_DigitalInput04	0	No error
		1	Short circuit on channel 4
4 - 7	Reserved		

4.13.9.14.6 Open line monitoring on channels 1 to 4

Name:
StatusInput02 or
WB_DigitalInput01 to WB_DigitalInput04

This register indicates whether an open line has occurred on the individual channels.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("WB_DigitalInput01" through "WB_DigitalInput04") or whether this register should be displayed as an individual USINT data point ("StatusInput02").

Data type	Value	Information
USINT	0 to 15	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	WB_DigitalInput01	0	No error
		1	Open line on channel 1
...		...	
3	WB_DigitalInput04	0	No error
		1	Open line on channel 4
4 - 7	Reserved	-	

4.13.9.14.7 Voltage monitoring on channels 1 to 4

Name:
StatusInput03 or
SM_DigitalInput01 to SM_DigitalInput04

This register monitors the voltage supply on the individual channels.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("SM_DigitalInput01" through "SM_DigitalInput04") or whether this register should be displayed as an individual USINT data point ("StatusInput03").

Data type	Value	Information
USINT	0 to 15	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	SM_DigitalInput01	0	No error
		1	Sensor supply error on channel 1
...		...	
3	SM_DigitalInput04	0	No error
		1	Sensor supply error on channel 4
4 - 7	Reserved	-	

4.13.9.14.8 Error monitoring on channels 1 to 4

Name:
StatusInput04 or
IE_DigitalInput01 to IE_DigitalInput04

This register indicates whether any other errors have occurred on the individual channels.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("IE_DigitalInput01" through "IE_DigitalInput04") or whether this register should be displayed as an individual USINT data point ("StatusInput04").

Data type	Value	Information
USINT	0 to 15	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	IE_DigitalInput01	0	No error
		1	Other error on channel 1
...		...	
3	IE_DigitalInput04	0	No error
		1	Other error on channel 4
4 - 7	Reserved	-	

4.13.9.14.9 Timestamp of last conversion

Name:
SampleTimeStamp

This register shows the timestamp of the last conversion in µs.

Data type	Value
UDINT	Timestamp of the last conversion in µs

4.13.9.14.10 Configuration of line status monitoring

Name:
ConfigOutput01

This register is used to configure short circuit monitoring and line status monitoring on the inputs.

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 3	Channel configuration - Channel 1	0	Standard
		1	Serial/Parallel: R-1k in series with (R-10k parallel to the switch)
		2	Parallel/Serial: R-10k parallel to (R-1k in series with switch)
		3	Parallel: R-10k parallel to switch
		4	Serial: R-1k in series with switch
		5 to 15	Inactive
4 - 7	Channel configuration - Channel 2	0 to 15	See Channel configuration - Channel 1
8 - 11	Channel configuration - Channel 3	0 to 15	See Channel configuration - Channel 1
12 - 15	Channel configuration - Channel 4	0 to 15	See Channel configuration - Channel 1

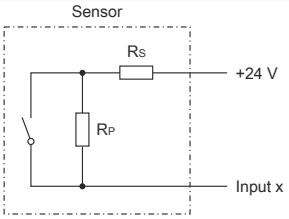
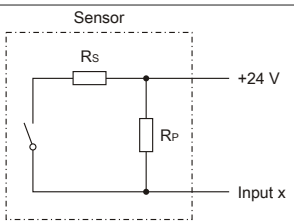
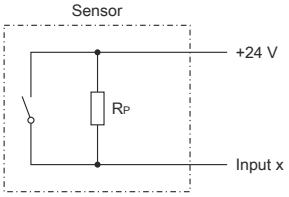
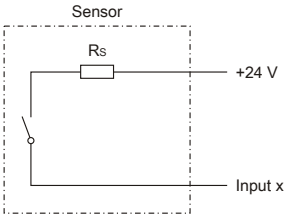
The name R-1k indicates a resistance in the permitted range of 1000 Ohm to 2000 Ohm with an accuracy of 10%.

The name R-10k indicates a resistance in the permitted range of 10000 Ohm to 20000 Ohm with an accuracy of 10%.

Information:

Inputs that are not being used should be set to the type "Standard" or "Serial" to prevent mistakes.

Configuration Possibilities:

Value	Configuration	Diagram	Information
0	**Standard**		Short-circuit detection and line break monitoring is not possible when using this configuration.
1	**Serial/parallel**		Short-circuit detection and line break monitoring is possible with this configuration.
2	**Parallel/serial**		Short-circuit detection and line break monitoring is possible with this configuration.
3	**Parallel**		This configuration allows line break monitoring. Short-circuit detection is not possible when using this configuration.
4	**Serial**		This configuration allows short circuit detection. Line break monitoring is not possible when using this configuration.

4.13.9.14.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
All channels	150 µs

4.13.9.14.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
All channels	150 µs

4.13.10 X20DI4653

4.13.10.1 General Information

The module is equipped with 4 inputs for 2-wire connections. It is designed for an input voltage of 100 to 240 VAC.

- 4 digital inputs
- 100 to 240 VAC inputs
- 50 Hz or 60 Hz
- 2-wire connections
- 240 V coded

> **Danger!**
>
> **Risk of electric shock!**
>
> **The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.**

4.13.10.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI4653	X20 digital input module, 4 inputs, 100 to 240 VAC, 240 V keyed, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 272: X20DI4653 - Order data

4.13.10.3 Technical data

Product ID	X20DI4653
Short description	
I/O module	4 digital inputs 100 to 240 VAC for 2-wire connections
General information	
B&R ID code	0x2545
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
External I/O supply	Yes, using software (typical threshold 85 VAC)
Power consumption	
Bus	0.17 W
Internal I/O	-
External I/O	0.91 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1]	Yes
KC	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	100 to 240 VAC
Input filter	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Hardware	
1 -> 0	≤30 ms
0 -> 1	≤40 ms
Connection type	2-wire connections
Rated frequency	47 to 63 Hz
Switching threshold	
Low	<40 VAC
High	>79 VAC
Isolation voltage between channel and bus	1 minute 2500 VAC
Input voltage	
Maximum	264 VAC
Input current	
100 VAC / 60 Hz	4 mA (Rev. ≥ E0), 5 mA (Rev. < E0)
240 VAC / 50 Hz	8.5 mA (Rev. ≥ E0), 11 mA (Rev. < E0)
Sensor supply	
Voltage	Equal to the module supply
Short circuit protection	No
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM12 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 273: X20DI4653 - Technical data

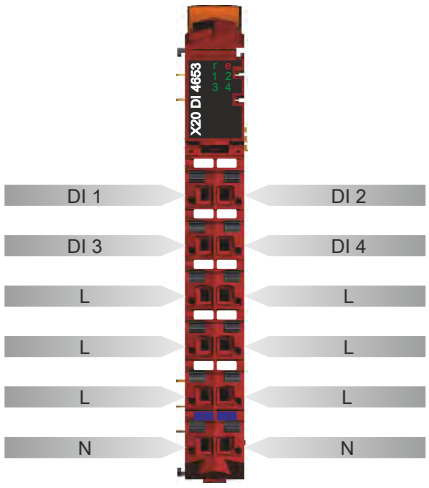
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.10.4 Status LEDs

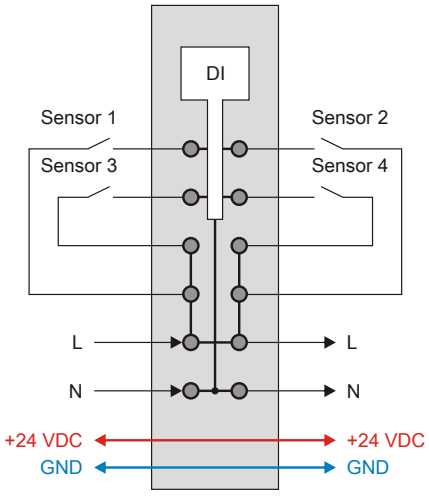
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Double flash	External supply is too low or not connected
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green		Input status of the corresponding digital input

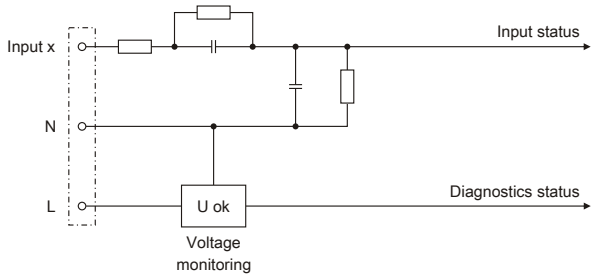
4.13.10.5 Pinout



4.13.10.6 Connection example

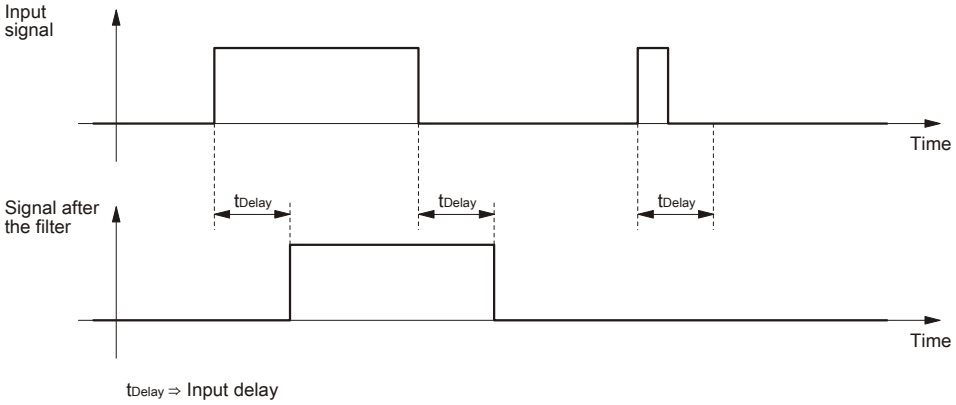


4.13.10.7 Input circuit diagram



4.13.10.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.10.9 Register description

4.13.10.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.10.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
		PowerSupply	Bit 7				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.10.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 4	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
		PowerSupply	Bit 7				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.10.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.10.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.10.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.10.9.4.2 Input status of digital inputs 1 to 4

Name:
DigitalInput or
DigitalInput01 to DigitalInput04
PowerSupply

The input status of digital inputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput02" and "PowerSupply") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 15	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input status - Digital input 4
4 - 6	Reserved	0	
7	PowerSupply	0	Supply voltage too low
		1	Supply voltage >80 VAC

4.13.10.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.10.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.11 X20(c)DI4760

4.13.11.1 General Information

The module is used to transfer digital signals from NAMUR encoders according to EN 60947-5-6. In addition to NAMUR encoders, normal switches can also be used.

- 4 digital inputs
- Input module for NAMUR encoders
- Open line and short circuit detection
- Each input can be used as a counter input

4.13.11.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.13.11.3 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI4760	X20 digital input module, 4 NAMUR inputs, 8.05 V	
X20cDI4760	X20 digital input module, coated, 4 NAMUR inputs, 8.05 V	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 274: X20DI4760, X20cDI4760 - Order data

4.13.11.4 Technical data

Product ID	X20DI4760	X20cDI4760
Short description		
I/O module	4 NAMUR inputs, special function	
General information		
B&R ID code	0x2105	0xE221
Status indicators	I/O function by channel, open line and short circuit detection by channel, operating status, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Short circuit	Yes, using status LED and software	
Open line	Yes, using status LED and software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.5 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Event counter		
Quantity	4	
Signal form	Symmetrical square wave pulse or corresponding minimum pulse duration [2]	
Evaluation	Every rising edge, cyclic counter	
Counter size	8-bit	
Input frequency		
1 input active	Max. 1600 Hz	
2 inputs active	Max. 1100 Hz	
3 inputs active	Max. 870 Hz	
4 inputs active	Max. 680 Hz	
NAMUR inputs		
Open line detection	<350 µA	
Input circuit	For NAMUR encoders in accordance with EN 60947-5-6	
Isolation voltage between channel and bus	500 V_{eff}	
Short circuit detection	>7 mA	
No load voltage	8.05 V ±0.33%	
Switching amplifier internal resistance	1 kΩ ±1%	
Max. short circuit current	8.2 mA	
Input delay		
1 input active	≤310 µs	
2 inputs active	≤450 µs	
3 inputs active	≤570 µs	
4 inputs active	≤735 µs	
Switching threshold		
Area	1.2 mA to 2.1 mA	
Switching hysteresis	Typ. 300 µA	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 275: X20DI4760, X20cDI4760 - Technical data

Product ID	X20DI4760	X20cDI4760
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 275: X20DI4760, X20cDI4760 - Technical data

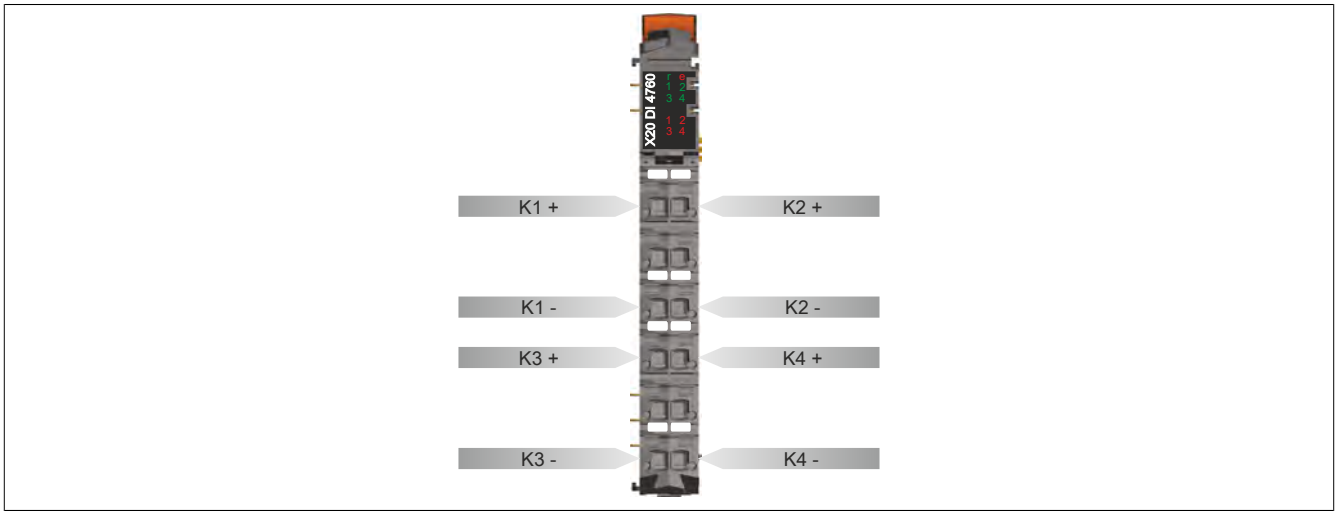
1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Minimum pulse duration: t[s] ≥ 1/(2 x f_{max}[Hz])

4.13.11.5 Status LEDs

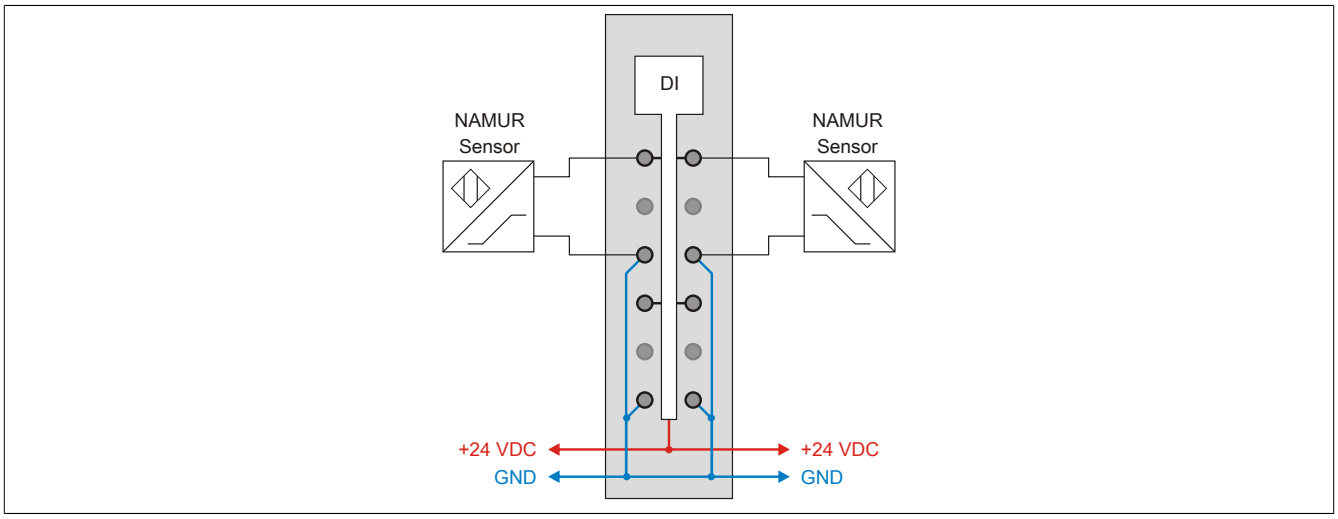
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Error on at least one channel
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Off	Open line or input status log. 0
			On	Short circuit or input status log. 1
	1 - 4	Red	Off	The sensor is ready for operation
			Blinking 1Hz	Open line on corresponding channel
			On	Short circuit on corresponding channel

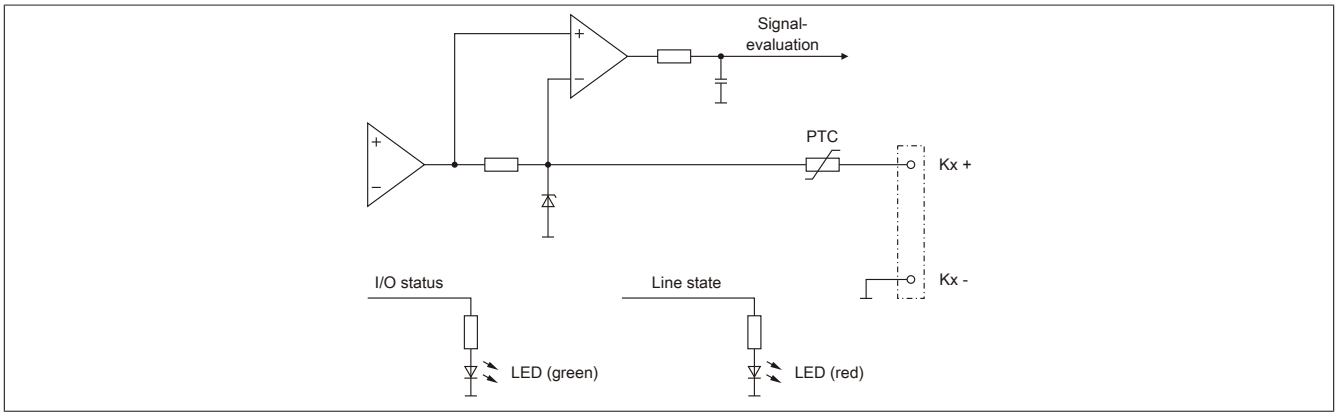
4.13.11.6 Pinout



4.13.11.7 Connection example

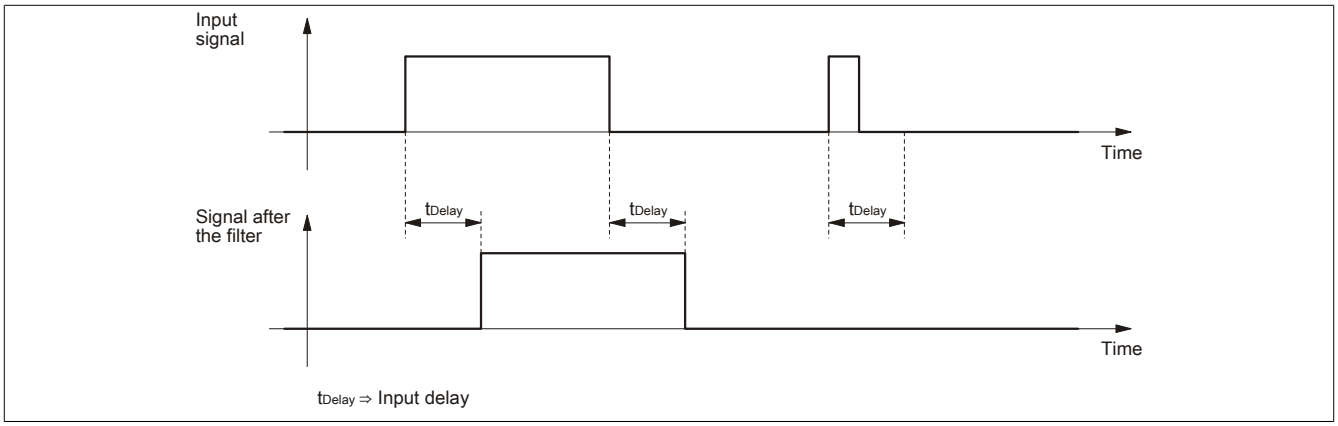


4.13.11.8 Input circuit diagram

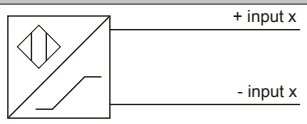
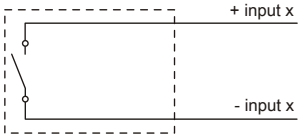
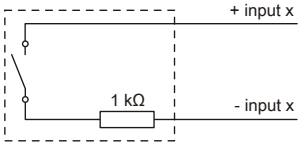
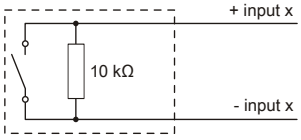
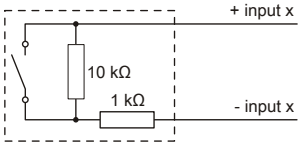


4.13.11.9 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.11.12.4.1 "ConfigOutput03" on page 1277. Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



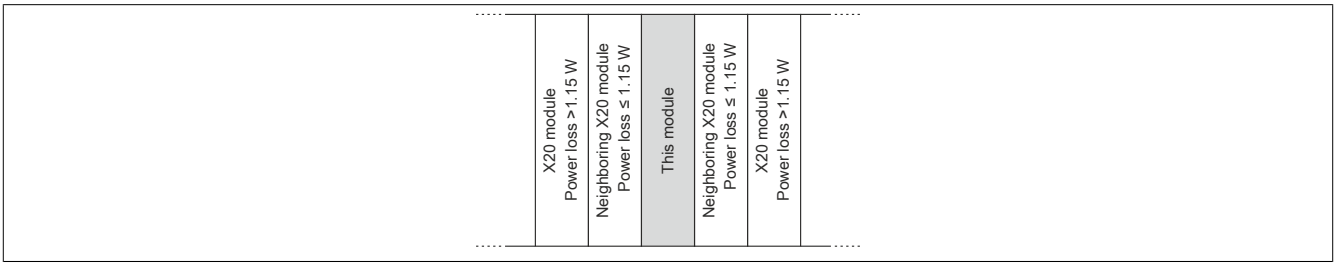
4.13.11.10 Examples of possible signal generators

Proximity switch	
Switch in accordance with EN 60947-5-6 (NAMUR)	
Mechanical contacts (instead of NAMUR encoders)	
Without open line detection and without short circuit detection	
Without open line detection and with short circuit detection	
With open line detection and without short circuit detection	
With open line detection and with short circuit detection	

4.13.11.11 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.13.11.12 Register description

4.13.11.12.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.11.12.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
0	DigitalInput	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput04	Bit 3				
4	Counter01	USINT	•			
6	Counter02	USINT	•			
8	Counter03	USINT	•			
10	Counter04	USINT	•			
30	StatusInput	USINT	•			
	ShortCircuit01	Bit 0				
	...	...				
	ShortCircuit04	Bit 3				
	OpenLine01	Bit 4				
	...	...				
	OpenLine04	Bit 7				
16	OutputConfig01	USINT				•
18	OutputConfig02	USINT				•
20	OutputConfig03	USINT				•

4.13.11.12.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 4	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
4	-	Counter01	USINT		•		
6	-	Counter02	USINT		•		
8	-	Counter03	USINT		•		
10	-	Counter04	USINT		•		
30	-	Status of channels 1 to 4	USINT		•		
		ShortCircuit01	Bit 0				
		...	...				
		ShortCircuit04	Bit 3				
		OpenLine01	Bit 4				
		...	...				
		OpenLine04	Bit 7				
16	-	ConfigOutput01	USINT				•
18	-	ConfigOutput02	USINT				•
20	-	ConfigOutput03	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.11.12.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.11.12.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.11.12.4.1 Digital input filter

Name:
ConfigOutput03

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.11.12.4.2 Input status of digital inputs 1 to 4

Name:
DigitalInput or
DigitalInput01 to DigitalInput04
PowerSupply

The input status of digital inputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput02" and "PowerSupply") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 15	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input status - Digital input 4
4 - 6	Reserved	0	
7	PowerSupply	0	Supply voltage too low
		1	Supply voltage >80 VAC

4.13.11.12.5 Positive edge counter on digital inputs

Name:
Counter01 to Counter04

These registers cyclically count the positive edges on the individual channels.

Data type	Value
USINT	Positive edge counter on channel, cyclic

4.13.11.12.6 Status of channels 1 to 4

Name:
StatusInput01 and
ShortCircuit01 to ShortCircuit04
OpenLine01 to OpenLine04

This register indicates whether an open line or overflow has occurred on the individual channels.

Only function model 0 - Standard:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("ShortCircuit01" to "ShortCircuit04" and "OpenLine01" to "OpenLine04") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Values	Information
USINT	0 to 255	Packed inputs = On
	See bit structure.	Packed inputs = Off or Function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	ShortCircuit01	0	No error
		1	Overload on channel 1
...		...	
3	ShortCircuit04	0	No error
		1	Overload on channel 4
4	OpenLine01	0	No error
		1	Open line on channel 1
...		...	
7	OpenLine04	0	No error
		1	Open line on channel 4

4.13.11.12.7 Function expansion

Firmware version 802 is offered for hardware variant 7 or higher of the module. This and subsequent firmware versions provide the user with new configuration possibilities.

4.13.11.12.7.1 Disabling channels and status messages

Name:
OutputConfig01

This register can be used to (de)activate individual channels or just their status responses.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel 1	0	Channel enabled
		1	Channel disabled
...		...	
3	Channel 4	0	Channel enabled
		1	Channel disabled
4	Status message - Channel 1	0	Status message activated
		1	Status message deactivated
...		...	
7	Status message - Channel 4	0	Status message activated
		1	Status message deactivated

4.13.11.12.7.2 Replacement values during overload

Name:
OutputConfig02

This register can be used to specify defined replacement values for the individual channels according to the error situation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Overload - Channel 1	0	Replacement value when overload is FALSE
		1	Replacement value when overload is TRUE
...		...	
3	Overload - Channel 4	0	Replacement value when overload is FALSE
		1	Replacement value when overload is TRUE
4	Open line - Channel 1	0	Replacement value when open line is FALSE
		1	Replacement value when open line is TRUE
...		...	
7	Open line - Channel 4	0	Replacement value when open line is FALSE
		1	Replacement value when open line is TRUE

4.13.11.12.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.11.12.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.12 X20(c)DI6371

4.13.12.1 General Information

The module is equipped with six inputs for 1 or 2-wire connections. The X20 6-pin terminal block can be used for universal 1-line wiring. Two-line wiring can be implemented using the 12-pin terminal block. The inputs on the module are designed for sink connections.

- 6 digital inputs
- Sink connection
- 2-wire connections
- 24 VDC for sensor supply
- Software input filter can be configured for entire module
- 1-wire connection type with 6-pin terminal block

4.13.12.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.13.12.3 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI6371	X20 digital input module, 6 inputs, 24 VDC, sink, configurable input filter, 2-wire connections	
X20cDI6371	X20 digital input module, coated, 6 inputs, 24 VDC, sink, configurable input filter, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 276: X20DI6371, X20cDI6371 - Order data

4.13.12.4 Technical data

Product ID	X20DI6371	X20cDI6371
Short description		
I/O module	6 digital inputs 24 VDC for 1- or 2-wire connections	
General information		
B&R ID code	0x1B93	0xE222
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Power consumption		
Bus	0.15 W	
Internal I/O	0.88 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Digital inputs		
Nominal voltage	24 VDC	
Input voltage	24 VDC -15% / +20%	
Input current at 24 VDC	Typ. 3.75 mA	
Input filter		
Hardware	≤100 µs	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Connection type	1- or 2-wire connections	
Input circuit	Sink	
Input resistance	Typ. 6.4 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Sensor supply		
Voltage	Module supply minus voltage drop for short circuit protection	
Voltage drop for short circuit protection at 500 mA	Max. 2 VDC	
Summation current	0.5 A	
Short circuit protection	Yes	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 277: X20DI6371, X20cDI6371 - Technical data

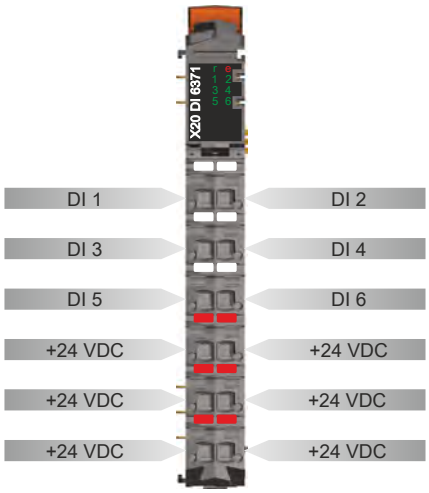
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.12.5 Status LEDs

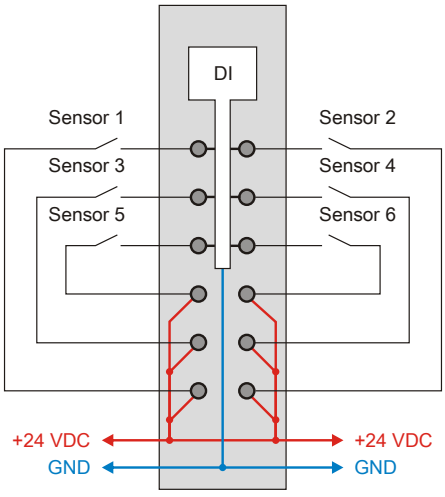
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Green		Input status of the corresponding digital input

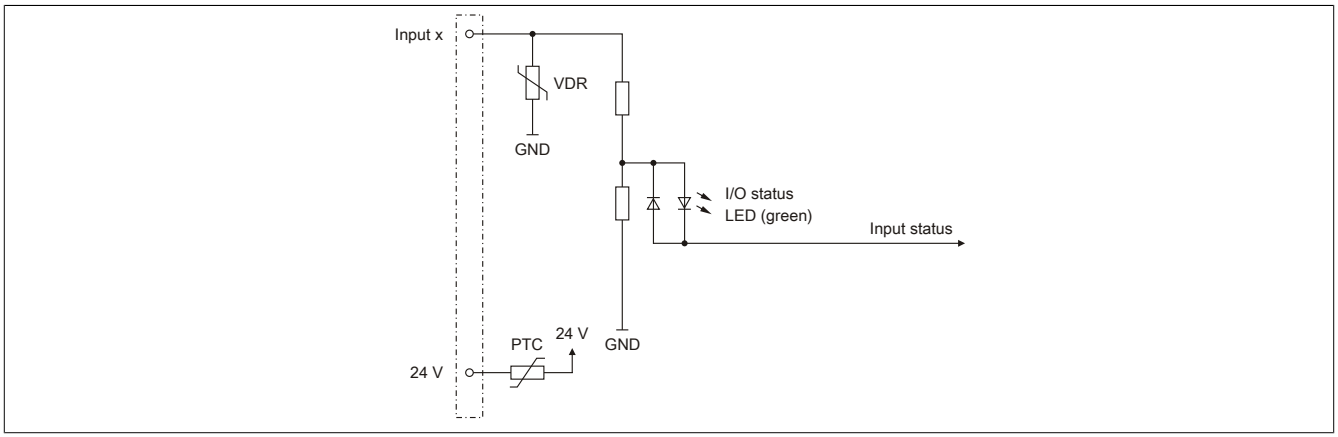
4.13.12.6 Pinout



4.13.12.7 Connection example

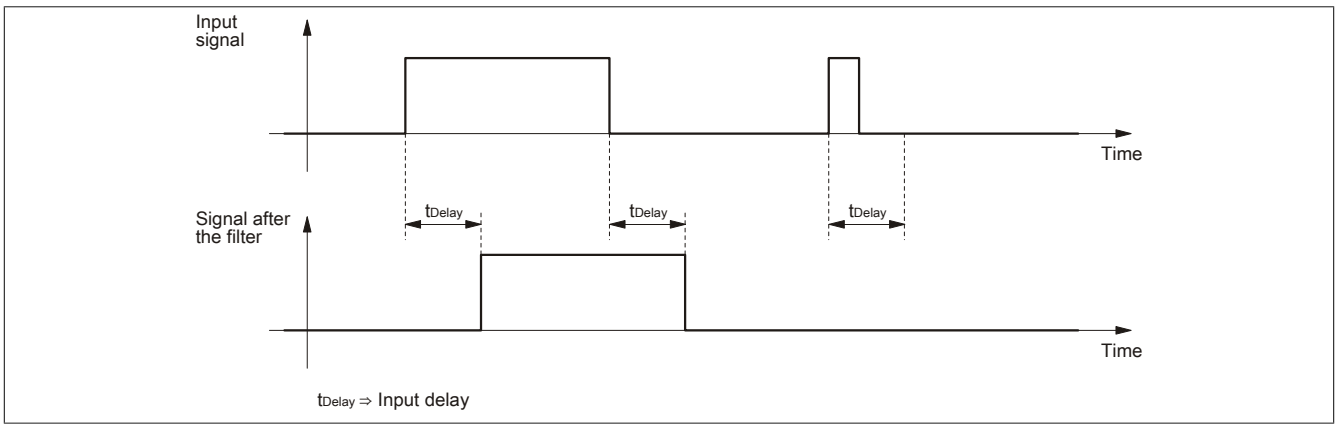


4.13.12.8 Input circuit diagram



4.13.12.9 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.12.10 Register description

4.13.12.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.12.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.12.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 6	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.12.10.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.12.10.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.12.10.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.12.10.4.2 Input status of digital inputs 1 to 6

Name:
DigitalInput or
DigitalInput01 to DigitalInput06

The input status of digital inputs 1 to 6 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput06") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 63	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
5	DigitalInput06	0 or 1	Input status - Digital input 6

4.13.12.10.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.12.10.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.13 X20(c)DI6372

4.13.13.1 General Information

The module is equipped with six inputs for 1 or 2-wire connections. The X20 6-pin terminal block can be used for universal 1-line wiring. Two-line wiring can be implemented using the 12-pin terminal block. The inputs on the module are designed for source connections.

- 6 digital inputs
- Source connection
- 2-wire connections
- 24 VDC for sensor supply
- Software input filter can be configured for entire module
- 1-wire connection type with 6-pin terminal block

4.13.13.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.13.13.3 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI6372	X20 digital input module, 6 inputs, 24 VDC, source, configurable input filter, 2-wire connections	
X20cDI6372	X20 digital input module, coated, 6 inputs, 24 VDC, source, configurable input filter, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 278: X20DI6372, X20cDI6372 - Order data

4.13.13.4 Technical data

Product ID	X20DI6372	X20cDI6372
Short description		
I/O module	6 digital inputs 24 VDC for 1- or 2-wire connections	
General information		
B&R ID code	0x1B94	0xE223
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Power consumption		
Bus	0.15 W	
Internal I/O	0.88 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Digital inputs		
Nominal voltage	24 VDC	
Input voltage	24 VDC -15% / +20%	
Input current at 24 VDC	Typ. 3.75 mA	
Input filter		
Hardware	≤100 µs	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Connection type	1- or 2-wire connections	
Input circuit	Source	
Input resistance	Typ. 6.4 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 279: X20DI6372, X20cDI6372 - Technical data

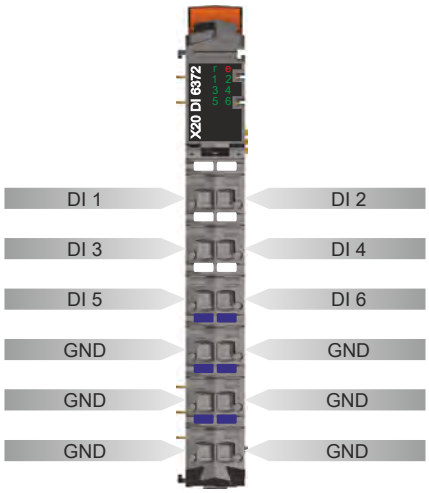
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.13.5 Status LEDs

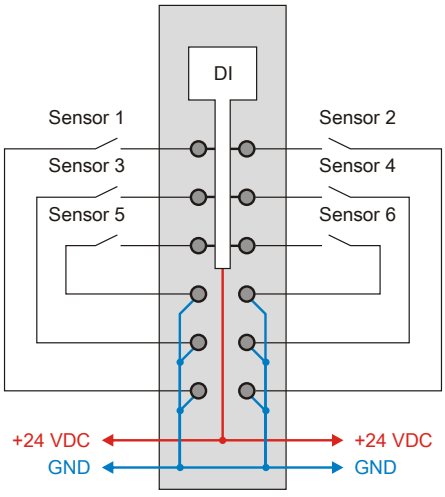
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Green		Input status of the corresponding digital input

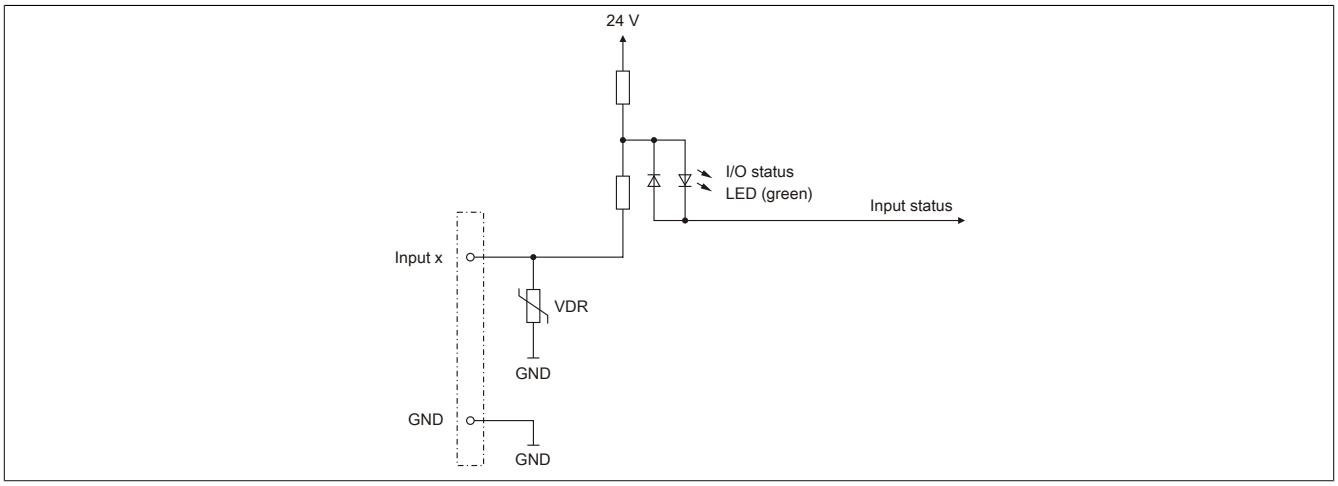
4.13.13.6 Pinout



4.13.13.7 Connection example

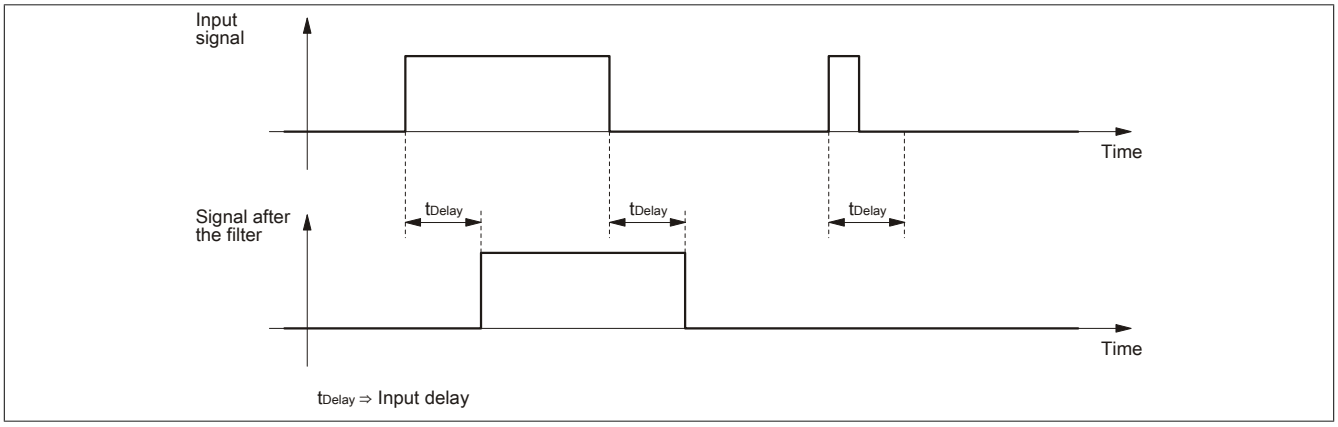


4.13.13.8 Input circuit diagram



4.13.13.9 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.13.10 Register description

4.13.13.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.13.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.13.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 6	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.13.10.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.13.10.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.13.10.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.13.10.4.2 Input status of digital inputs 1 to 6

Name:
DigitalInput or
DigitalInput01 to DigitalInput06

The input status of digital inputs 1 to 6 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput06") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 63	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
5	DigitalInput06	0 or 1	Input status - Digital input 6

4.13.13.10.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.13.13.10.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.13.14 X20DI6373

4.13.14.1 General Information

The module has 6 inputs. The input circuit can be sink or source thanks to the potential-free design of the inputs.

- 6 digital inputs
- Sink/Source connection
- Software input filter can be configured for entire module

4.13.14.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI6373	X20 digital input module, 6 inputs, 24 VDC, sink/source, all inputs floating, configurable input filter, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 280: X20DI6373 - Order data

4.13.14.3 Technical data

Product ID	X20DI6373
Short description	
I/O module	6 digital floating inputs - 24 VDC
General information	
B&R ID code	0xA7A2
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.15 W
Internal I/O	0.88 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 3.75 mA
Input filter	
Hardware	≤100 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Input circuit	Sink or source
Input resistance	Typ. 6.4 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately, Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 281: X20DI6373 - Technical data

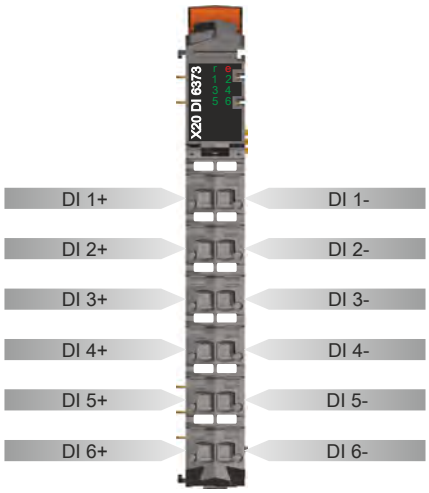
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.14.4 Status LEDs

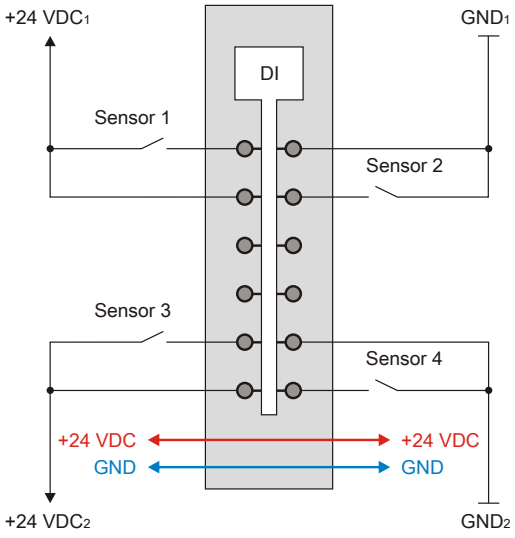
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Green		Input status of the corresponding digital input

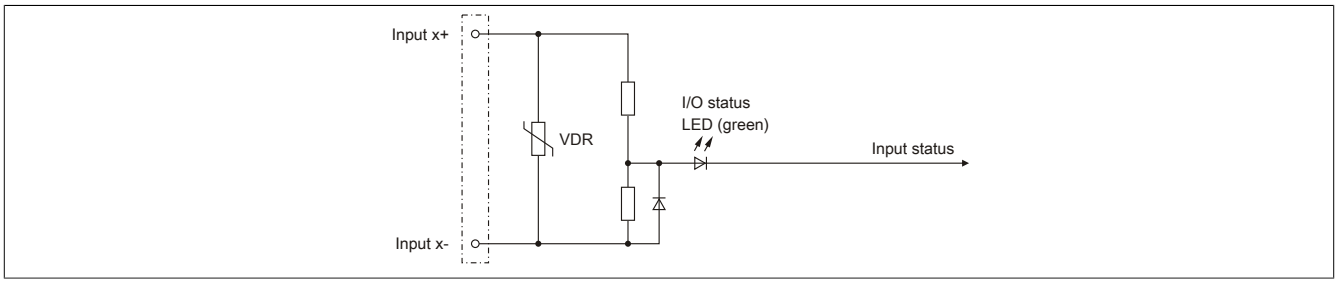
4.13.14.5 Pinout



4.13.14.6 Connection example

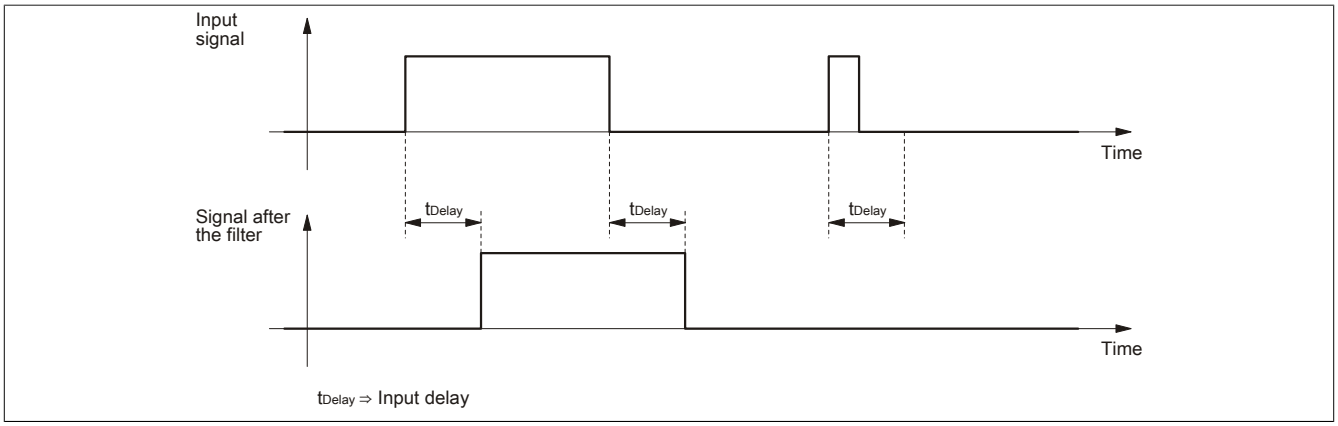


4.13.14.7 Input circuit diagram



4.13.14.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.14.9 Register description

4.13.14.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.14.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.14.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 6	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.14.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.14.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.14.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.14.9.4.2 Input status of digital inputs 1 to 6

Name:
DigitalInput or
DigitalInput01 to DigitalInput06

The input status of digital inputs 1 to 6 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput06") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 63	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
5	DigitalInput06	0 or 1	Input status - Digital input 6

4.13.14.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

4.13.14.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs

4.13.15 X20DI6553

4.13.15.1 General Information

The module is equipped with 6 inputs for 1-wire connections. It is designed for an input voltage of 100 to 120 VAC.

- 6 digital inputs
- 100 to 120 VAC inputs
- 50 Hz or 60 Hz
- 1-wire connections
- 240 V coded

> **Danger!**
>
> **Risk of electric shock!**
>
> **The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.**

4.13.15.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI6553	X20 digital input module, 6 inputs, 100 to 120 VAC, 240 V keyed, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 282: X20DI6553 - Order data

4.13.15.3 Technical data

Product ID	X20DI6553
Short description	
I/O module	6 digital inputs 100 to 120 VAC for 1-wire connections
General information	
B&R ID code	0x256F
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
External I/O supply	Yes, using software (typical threshold 85 VAC)
Power consumption	
Bus	0.21 W
Internal I/O	-
External I/O	0.68 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1]	Yes
KC	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	100 to 120 VAC
Input filter	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Hardware	
1 -> 0	≤30 ms
0 -> 1	≤15 ms
Connection type	1-wire connections
Rated frequency	47 to 63 Hz
Switching threshold	
Low	<20 VAC
High	>79 VAC
Isolation voltage between channel and bus	1 minute 1500 VAC
Input voltage	
Maximum	132 VAC
Input current	
120 VAC / 50 Hz	8.5 mA
120 VAC / 60 Hz	10 mA
Sensor supply	
Voltage	Equal to the module supply
Short circuit protection	No
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM12 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 283: X20DI6553 - Technical data

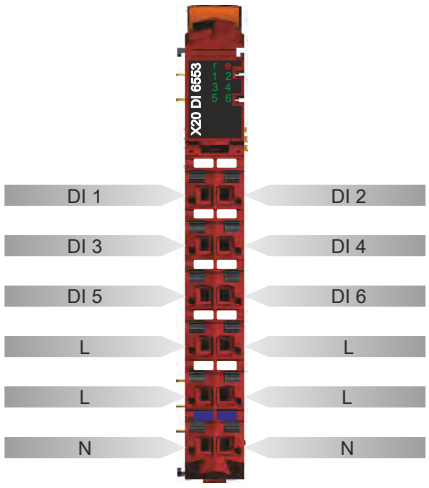
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.15.4 Status LEDs

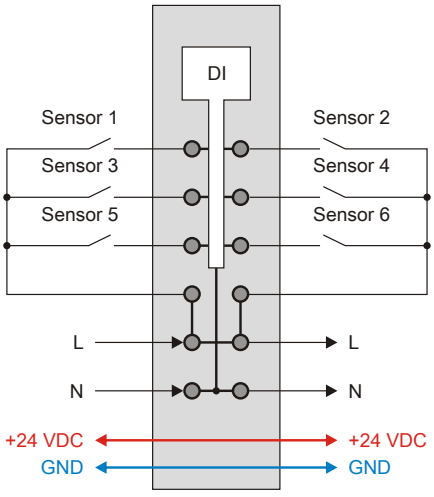
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Double flash	External supply is too low or not connected
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Green		Input status of the corresponding digital input

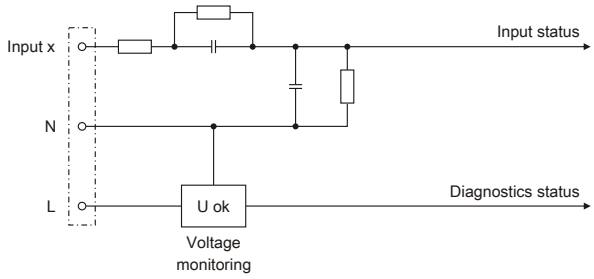
4.13.15.5 Pinout



4.13.15.6 Connection example

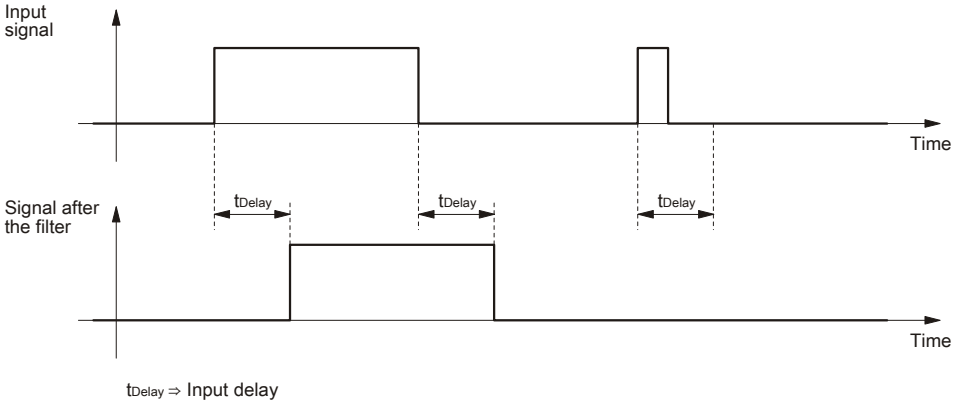


4.13.15.7 Input circuit diagram



4.13.15.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.15.9 Register description

4.13.15.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.15.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
		PowerSupply	Bit 7				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.15.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 6	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput06	Bit 5				
		PowerSupply	Bit 7				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.15.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.15.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.15.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.15.9.4.2 Input status of digital inputs 1 to 6

Name:
DigitalInput or
DigitalInput01 to DigitalInput06
PowerSupply

The input status of digital inputs 1 to 6 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput02" and "PowerSupply") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 63	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
5	DigitalInput04	0 or 1	Input status - Digital input 6
6	Reserved	0	
7	PowerSupply	0	Supply voltage too low
		1	Supply voltage >80 VAC

4.13.15.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

4.13.15.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs

4.13.16 X20DI8371

4.13.16.1 General Information

The module is equipped with eight inputs for 1-wire connections. The module is designed for sink input wiring.

- 8 digital inputs
- Sink connection
- 1-wire connections
- Software input filter can be configured for entire module

4.13.16.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI8371	X20 digital input module, 8 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 284: X20DI8371 - Order data

4.13.16.3 Technical data

Product ID	X20DI8371
Short description	
I/O module	8 digital inputs 24 VDC for 1-wire connections
General information	
B&R ID code	0xA4AB
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.18 W
Internal I/O	-
External I/O	1.2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 3.75 mA
Input filter	
Hardware	≤100 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	1-wire connections
Input circuit	Sink
Input resistance	Typ. 6.4 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 285: X20DI8371 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

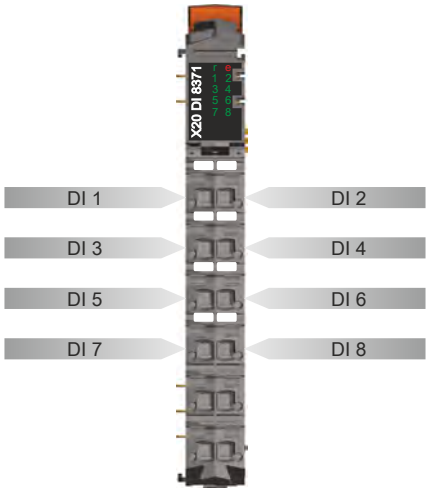
4.13.16.4 Status LEDs

For a description of the various operating modes, see section 2.11.1 "re LEDs".

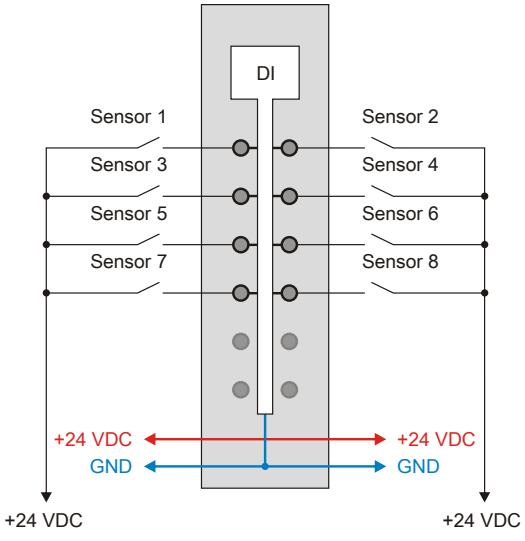
Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			Double flash	BOOT mode (during firmware update)[1)]
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Green		Input status of the corresponding digital input

1) Depending on the configuration, a firmware update can take up to several minutes.

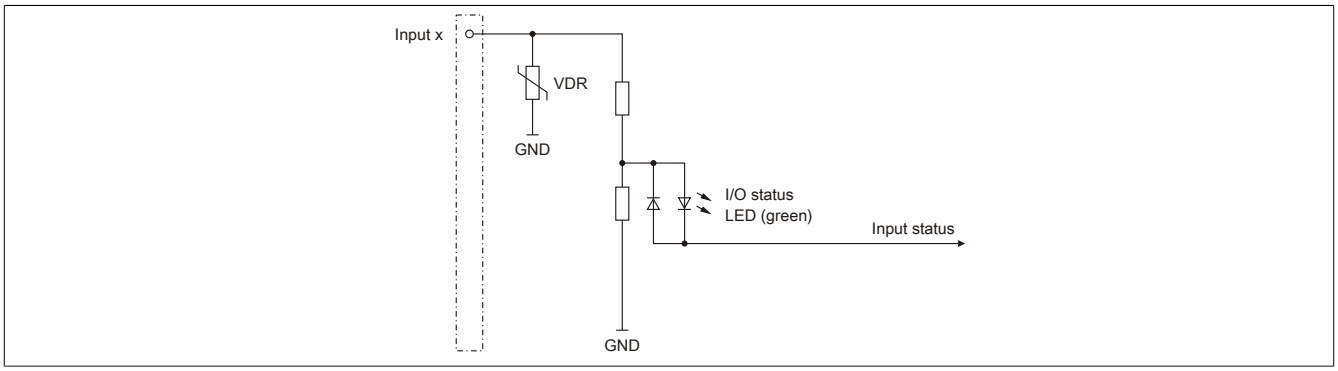
4.13.16.5 Pinout



4.13.16.6 Connection example

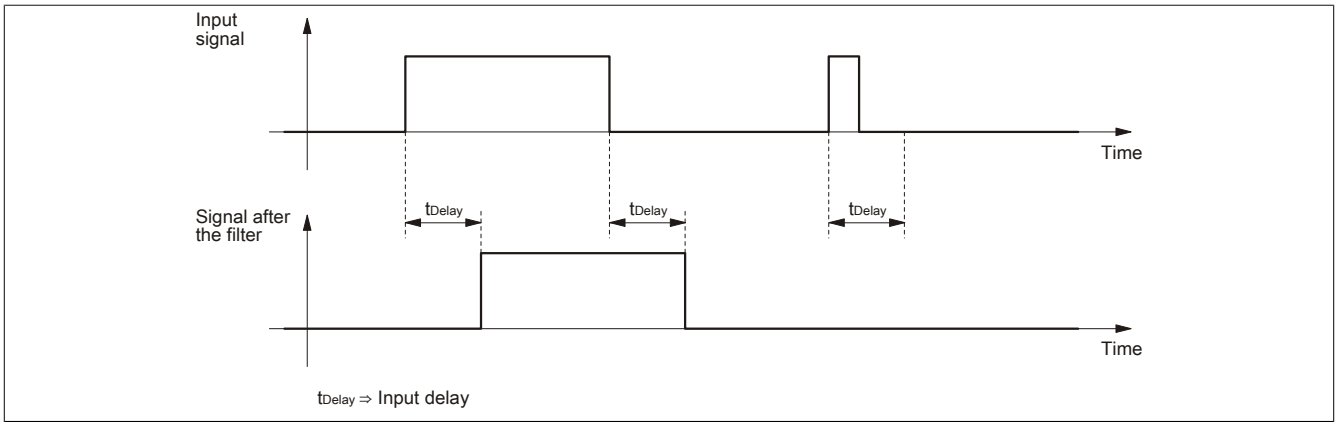


4.13.16.7 Input circuit diagram



4.13.16.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.16.9 Register description

4.13.16.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.16.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.16.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.16.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.16.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.16.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.16.9.4.2 Input state of digital inputs 1 to 8

Name:
DigitalInput or
DigitalInput01 to DigitalInput08

This register is used to indicate the input state of digital inputs 1 to 8.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput08") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 255	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

4.13.16.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

4.13.16.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs

4.13.17 X20(c)DI9371

4.13.17.1 General Information

The module is equipped with 12 inputs for 1-wire connections. The module is designed for sink input wiring.

- 12 digital inputs
- Sink connection
- 1-wire connections
- Software input filter can be configured for entire module

4.13.17.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.13.17.3 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI9371	X20 digital input module, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	
X20cDI9371	X20 digital input module, coated, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 286: X20DI9371, X20cDI9371 - Order data

4.13.17.4 Technical data

Product ID	X20DI9371	X20cDI9371
Short description		
I/O module	12 digital inputs 24 VDC for 1-wire connections	
General information		
B&R ID code	0x1B95	0xD574
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Power consumption		
Bus	0.18 W	
Internal I/O	-	
External I/O	1.75 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Digital inputs		
Nominal voltage	24 VDC	
Input voltage	24 VDC -15 % / +20 %	
Input current at 24 VDC	Typ. 3.75 mA	
Input filter		
Hardware	≤100 µs	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Connection type	1-wire connections	
Input circuit	Sink	
Input resistance	Typ. 6.4 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 287: X20DI9371, X20cDI9371 - Technical data

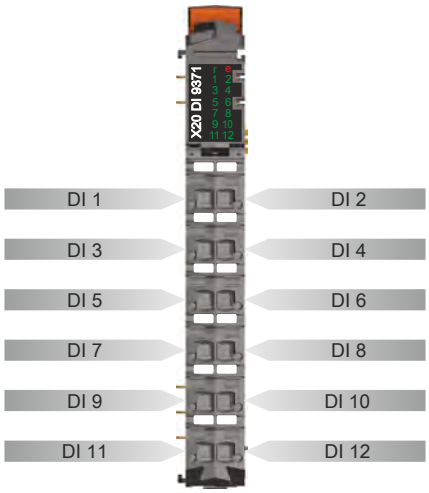
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.17.5 Status LEDs

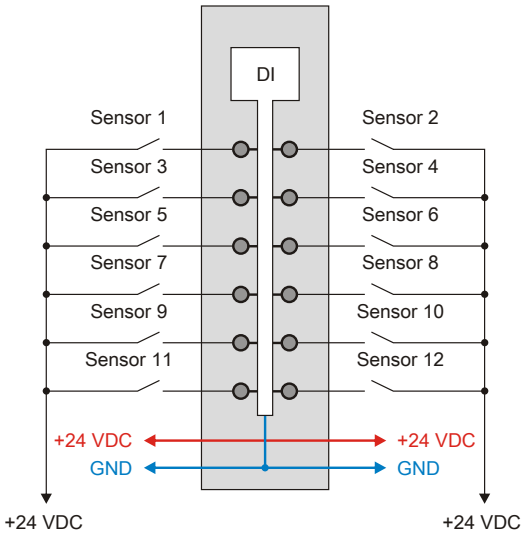
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 12	Green		Input status of the corresponding digital input

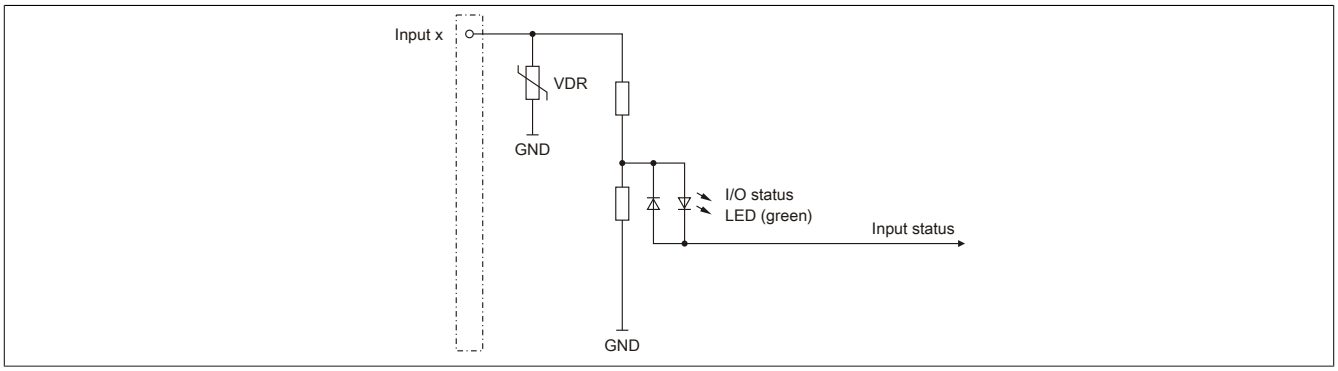
4.13.17.6 Pinout



4.13.17.7 Connection example

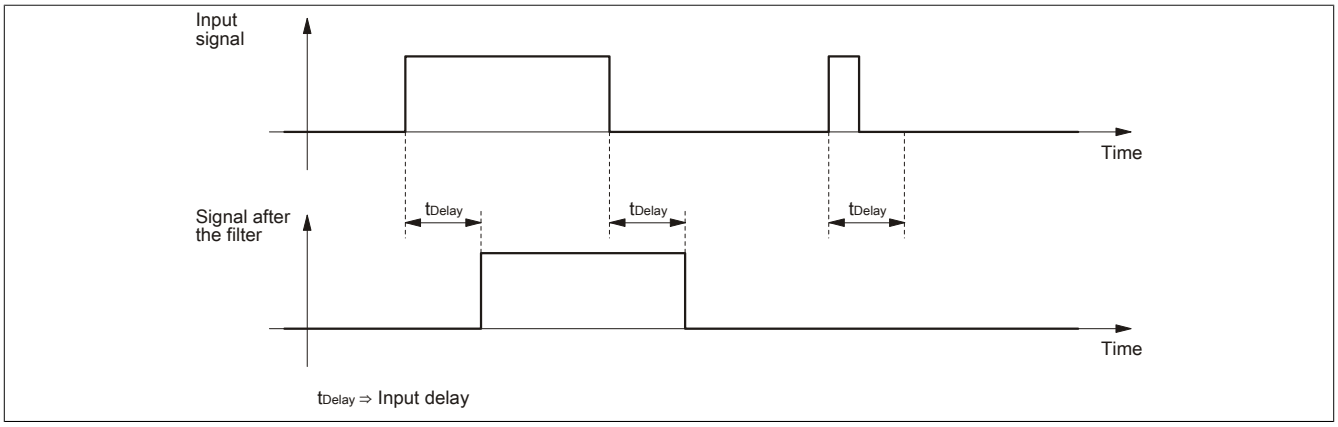


4.13.17.8 Input circuit diagram



4.13.17.9 Input filter

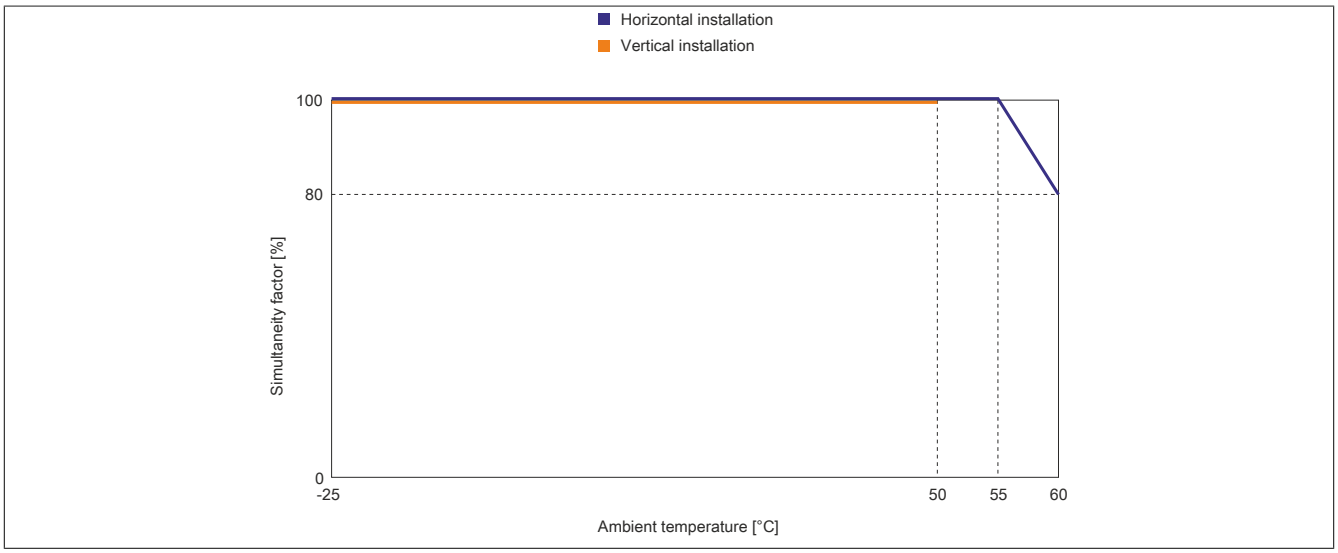
An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



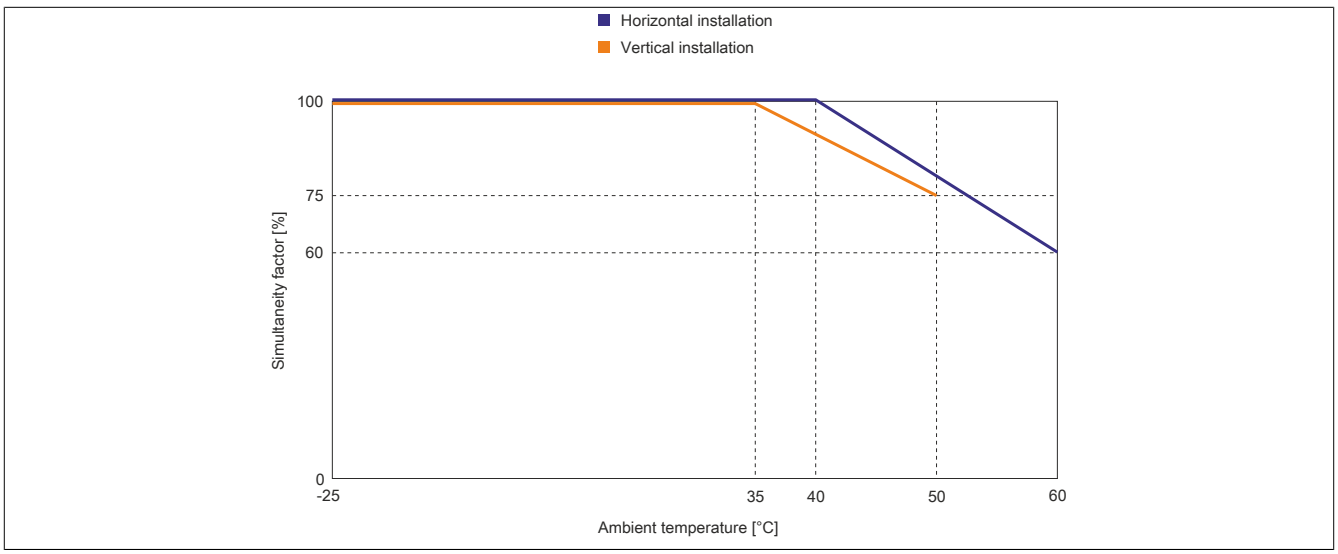
4.13.17.10 Derating

Be aware of the derating values below for the simultaneity factor.

Derating of simultaneity factor at 24 VDC input voltage



Derating of simultaneity factor at 28.8 VDC input voltage



4.13.17.11 Register description

4.13.17.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.17.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
-	1	DigitalInput	UINT	•			
0	1	Input status of digital inputs 1 to 8	USINT				
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
1	2	Input status of digital inputs 9 to 12	USINT	•			
		DigitalInput09	Bit 0				
		...	...				
		DigitalInput12	Bit 3				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.17.11.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 8	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
1	1	Input status of digital inputs 9 to 12	USINT	•			
		DigitalInput09	Bit 0				
		...	...				
		DigitalInput12	Bit 3				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.17.11.3.1 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN-I/O.

4.13.17.11.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.17.11.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.17.11.4.2 Input state of digital inputs 1 to 12

Name:
DigitalInput or
DigitalInput01 to DigitalInput12

This register indicates the input state of digital inputs 1 to 12.

Only function model 0 - Standard

The "Packed inputs" setting in the Automation Studio I/O configuration is used to determine whether all of the bits from these registers should be set up individually as data points in the Automation Studio I/O mapping ("DigitalInput01" to "DigitalInput12") or whether this register should be displayed as an individual UINT data point ("DigitalInput").

Data type	Values	Information
UINT	0 to 4095	Packed inputs = On
USINT	See bit structure.	Packed inputs = Off or Function model <> 0 - Standard

Bit structure:

Register 0

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

Register 1

Bit	Name	Value	Information
0	DigitalInput09	0 or 1	Input state - Digital input 9
...		...	
3	DigitalInput12	0 or 1	Input state - Digital input 12

4.13.17.11.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

4.13.17.11.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs

4.13.18 X20(c)DI9372

4.13.18.1 General Information

The module is equipped with 12 inputs for 1-wire connections. The module is designed for source input wiring.

- 12 digital inputs
- Source connection
- 1-wire connections
- Software input filter can be configured for entire module

4.13.18.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.13.18.3 Order data

Model number	Short description	Figure
	Digital inputs	
X20DI9372	X20 digital input module, 12 inputs, 24 VDC, source, configurable input filter, 1-wire connections	
X20cDI9372	X20 digital input module, coated, 12 inputs, 24 VDC, source, configurable input filter, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 288: X20DI9372, X20cDI9372 - Order data

4.13.18.4 Technical data

Product ID	X20DI9372	X20cDI9372
Short description		
I/O module	12 digital inputs 24 VDC for 1-wire connections	
General information		
B&R ID code	0x1D28	0xE224
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Power consumption		
Bus	0.18 W	
Internal I/O	1.75 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Digital inputs		
Nominal voltage	24 VDC	
Input voltage	24 VDC -15% / +20%	
Input current at 24 VDC	Typ. 3.75 mA	
Input filter		
Hardware	≤100 µs	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Connection type	1-wire connections	
Input circuit	Source	
Input resistance	Typ. 6.4 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 289: X20DI9372, X20cDI9372 - Technical data

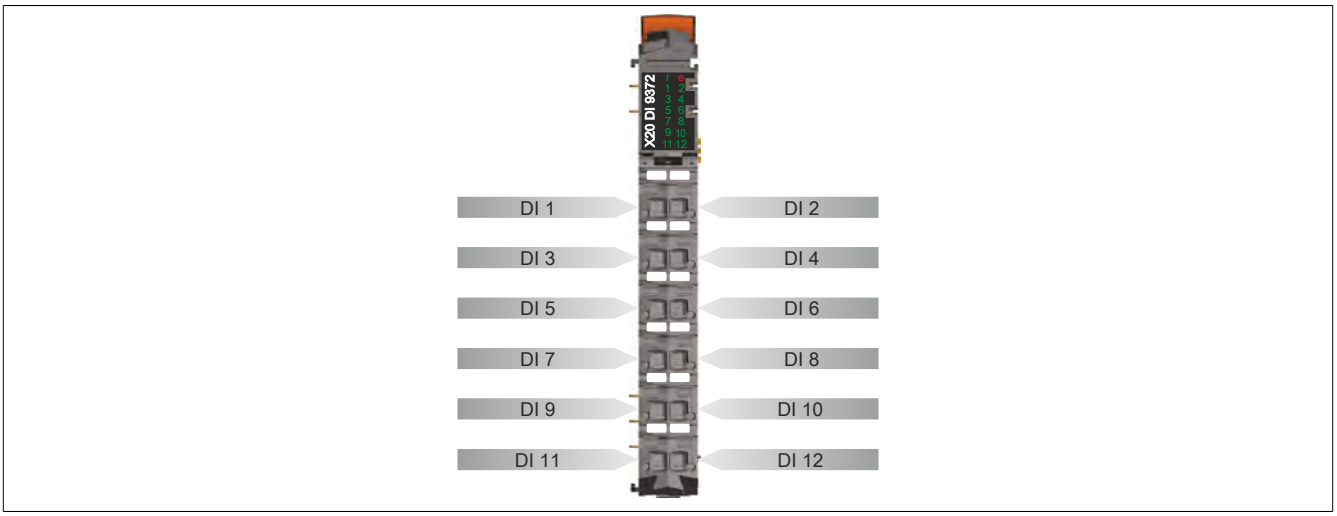
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.18.5 Status LEDs

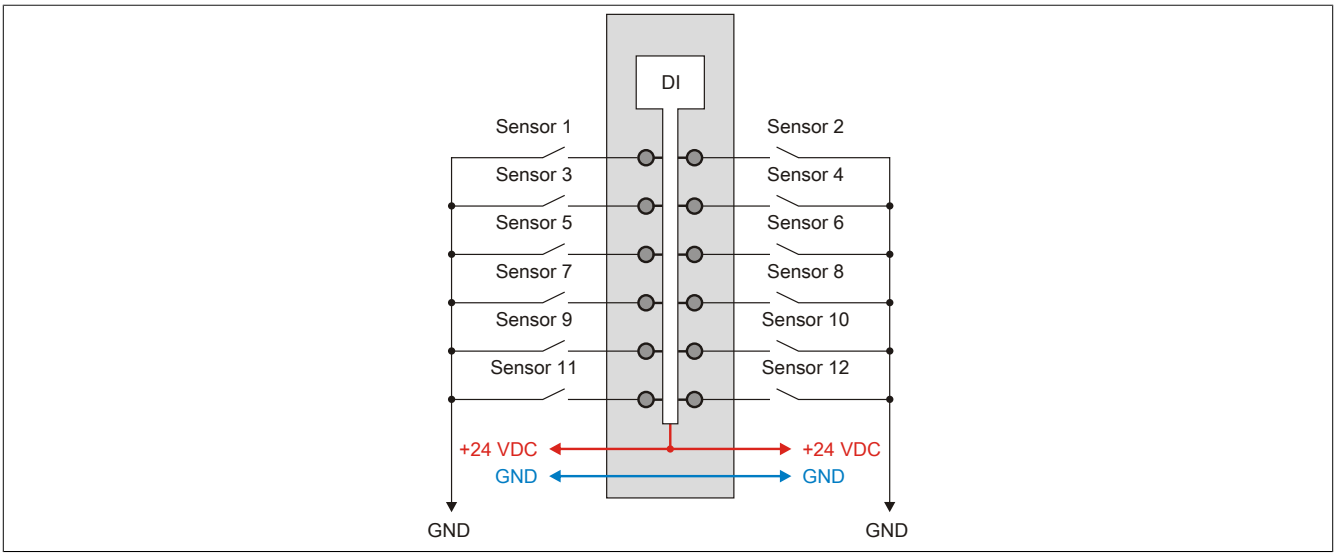
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
	e + r	Red on / Green single flash		Invalid firmware
	1 - 12	Green		Input status of the corresponding digital input

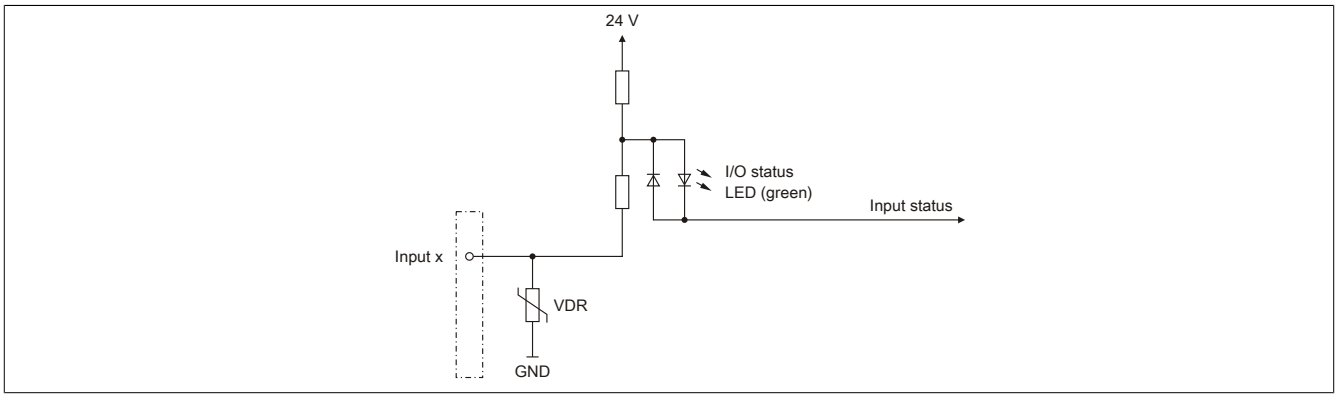
4.13.18.6 Pinout



4.13.18.7 Connection example

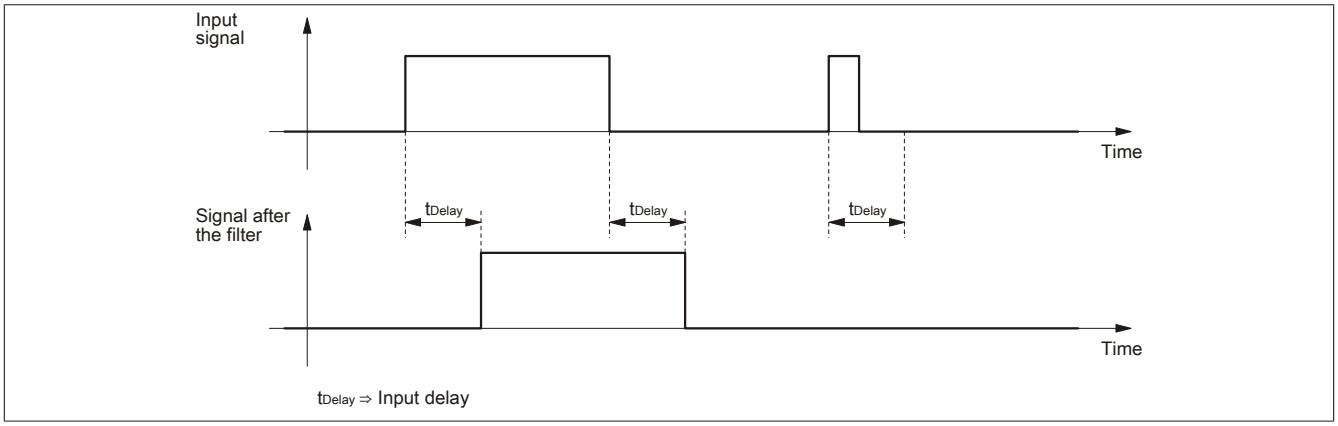


4.13.18.8 Input circuit diagram



4.13.18.9 Input filter

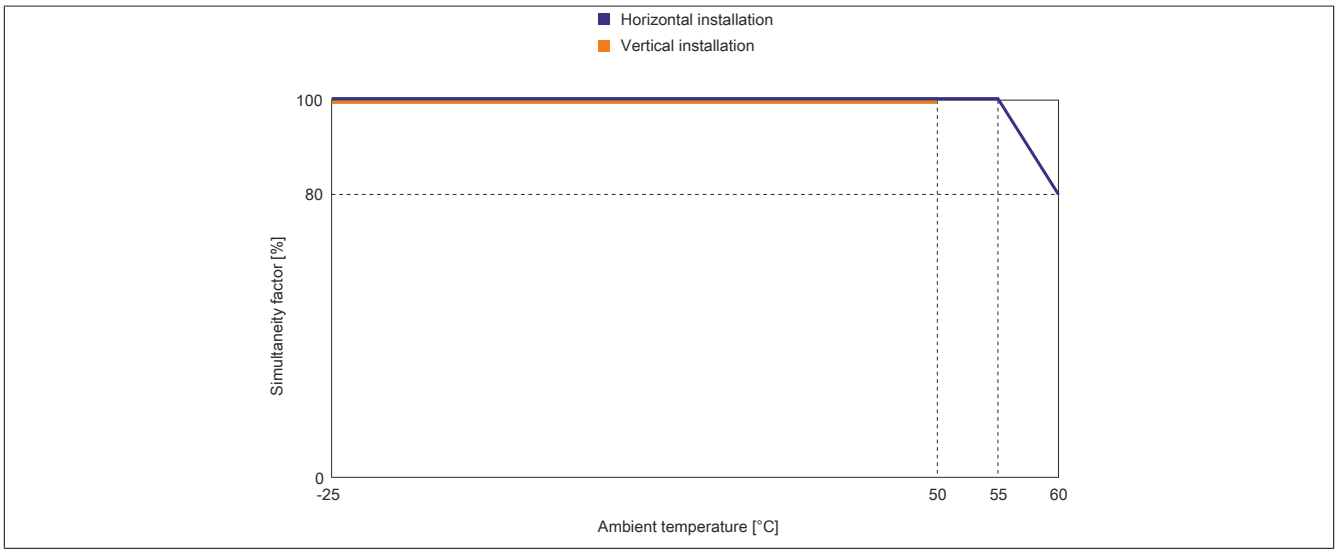
An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



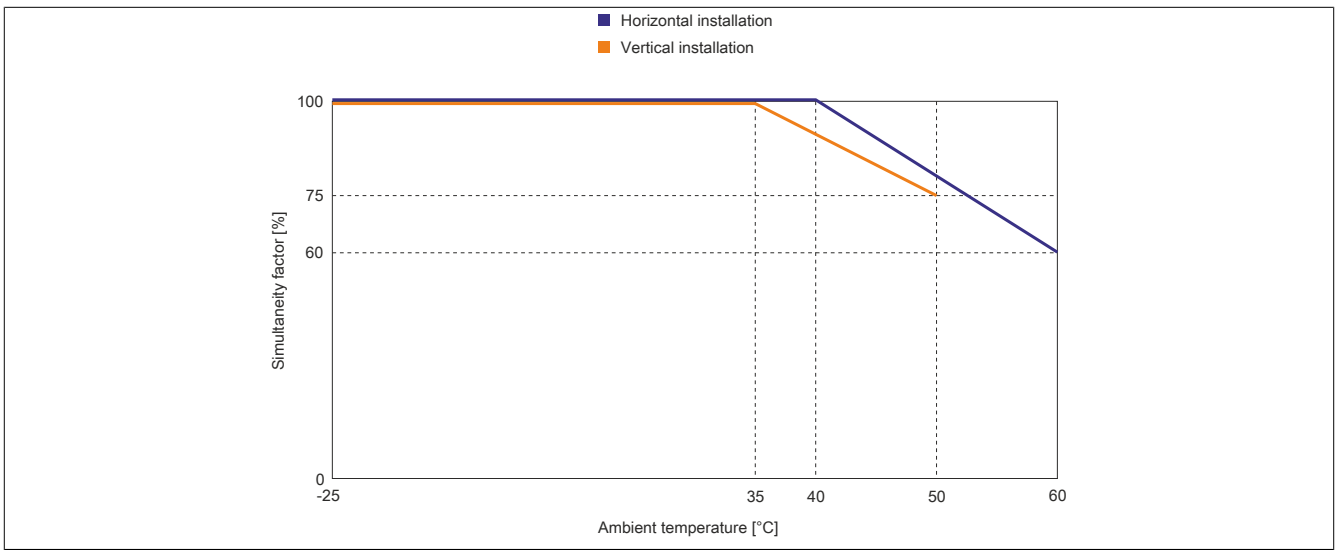
4.13.18.10 Derating

Be aware of the derating values below for the simultaneity factor.

Derating of simultaneity factor at 24 VDC input voltage



Derating of simultaneity factor at 28.8 VDC input voltage



4.13.18.11 Register description

4.13.18.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.18.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
-	1	DigitalInput	UINT	•			
0	1	Input status of digital inputs 1 to 8	USINT				
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
1	2	Input status of digital inputs 9 to 12	USINT	•			
		DigitalInput09	Bit 0				
		...	...				
		DigitalInput12	Bit 3				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.18.11.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 8	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
1	1	Input status of digital inputs 9 to 12	USINT	•			
		DigitalInput09	Bit 0				
		...	...				
		DigitalInput12	Bit 3				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.18.11.3.1 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN-I/O.

4.13.18.11.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.18.11.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.18.11.4.2 Input state of digital inputs 1 to 12

Name:
DigitalInput or
DigitalInput01 to DigitalInput12

This register indicates the input state of digital inputs 1 to 12.

Only function model 0 - Standard

The "Packed inputs" setting in the Automation Studio I/O configuration is used to determine whether all of the bits from these registers should be set up individually as data points in the Automation Studio I/O mapping ("DigitalInput01" to "DigitalInput12") or whether this register should be displayed as an individual UINT data point ("DigitalInput").

Data type	Values	Information
UINT	0 to 4095	Packed inputs = On
USINT	See bit structure.	Packed inputs = Off or Function model <> 0 - Standard

Bit structure:

Register 0

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

Register 1

Bit	Name	Value	Information
0	DigitalInput09	0 or 1	Input state - Digital input 9
...		...	
3	DigitalInput12	0 or 1	Input state - Digital input 12

4.13.18.11.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

4.13.18.11.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs

4.13.19 X20DID371

4.13.19.1 General Information

The module is equipped with 8 inputs for 1-wire or 2-wire connections. The module is designed for sink input wiring.

- 8 digital inputs
- Sink connection
- 2-wire connections
- 24 VDC for sensor supply
- Software input filter can be configured for entire module

4.13.19.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DID371	X20 digital input module, 8 inputs, 24 VDC, sink, configurable input filter, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 290: X20DID371 - Order data

4.13.19.3 Technical data

Product ID	X20DID371
Short description	
I/O module	8 digital inputs 24 VDC for 1- or 2-wire connections
General information	
B&R ID code	0xC0E7
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.13 W
Internal I/O	1.2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 3.75 mA
Input filter	
Hardware	≤100 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	1- or 2-wire connections
Input circuit	Sink
Input resistance	Typ. 6.4 kΩ
Sensor supply	0.5 A summation current
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 291: X20DID371 - Technical data

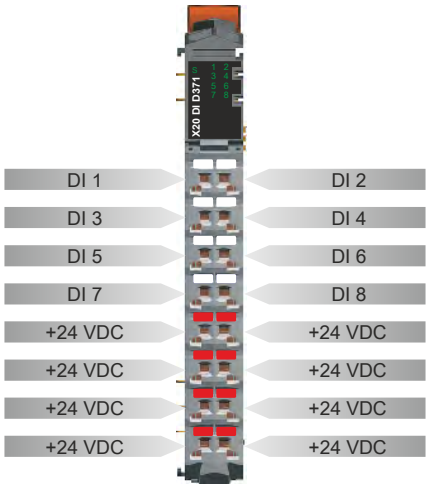
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.13.19.4 Status LEDs

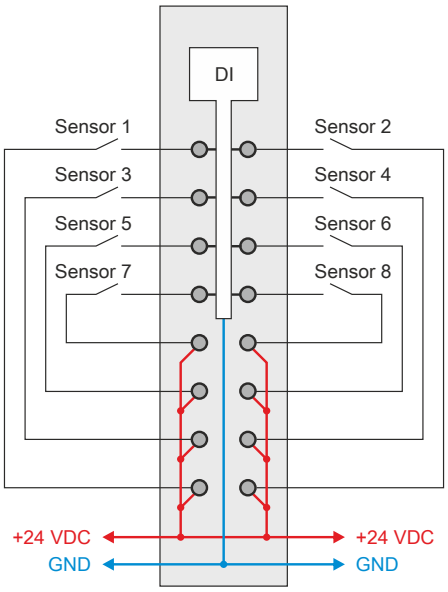
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	Module supply not connected or everything OK
		Red on / Green single flash		Invalid firmware
	1 - 8	Green		Input status of the corresponding digital input

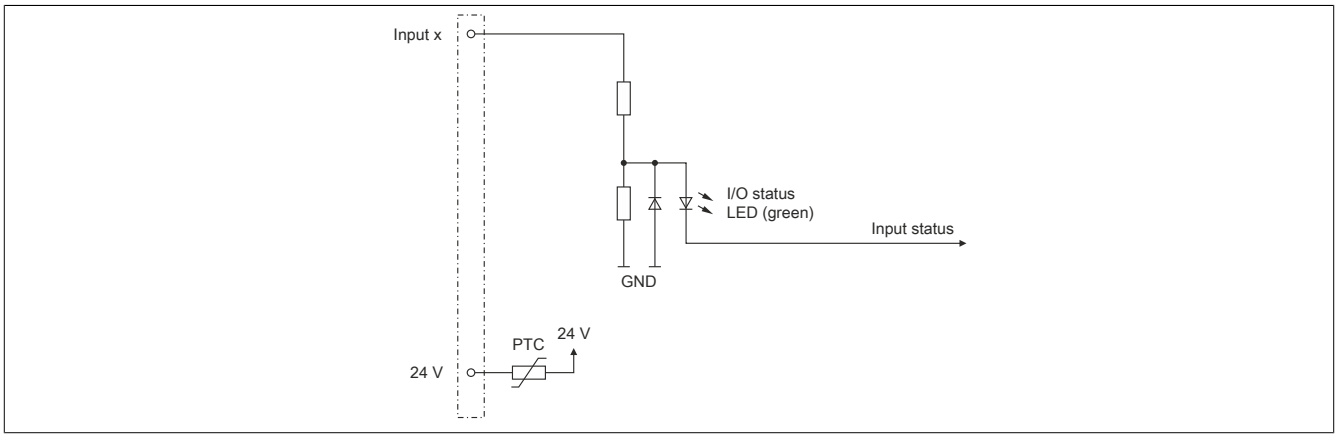
4.13.19.5 Pinout



4.13.19.6 Connection example

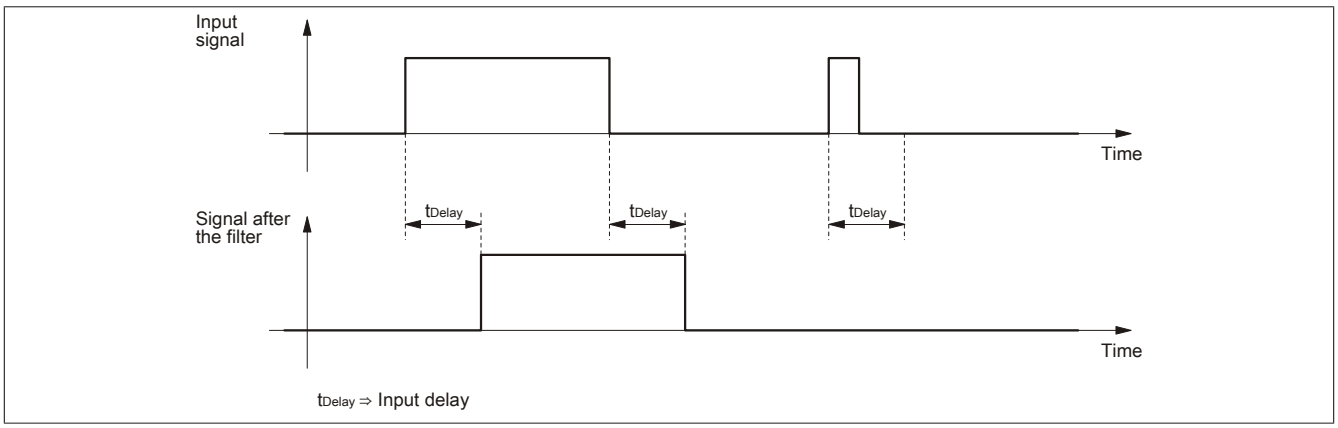


4.13.19.7 Input circuit diagram



4.13.19.8 Input filter

An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



4.13.19.9 Register description

4.13.19.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.19.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.19.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input state of digital inputs 1 to 8	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.19.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.13.19.9.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.19.9.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.19.9.4.2 Input state of digital inputs 1 to 8

Name:
DigitalInput or
DigitalInput01 to DigitalInput08

This register is used to indicate the input state of digital inputs 1 to 8.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput08") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 255	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

4.13.19.9.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

4.13.19.9.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs

4.13.20 X20DIF371

4.13.20.1 General Information

The module is equipped with 16 inputs for 1-wire connections. The module is designed for sink input wiring.

- 16 digital inputs
- Sink connection
- 1-wire connections
- Software input filter can be configured for entire module

4.13.20.2 Order data

Model number	Short description	Figure
	Digital inputs	
X20DIF371	X20 digital input module, 16 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 292: X20DIF371 - Order data

4.13.20.3 Technical data

Product ID	X20DIF371
Short description	
I/O module	16 digital inputs 24 VDC for 1-wire connections
General information	
B&R ID code	0xC0E8
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.18 W
Internal I/O	-
External I/O	1.47 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 2.68 mA
Input filter	
Hardware	≤100 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	1-wire connections
Input circuit	Sink
Input resistance	Typ. 8.9 kΩ
Simultaneity	
With 24 V I/O supply	100% 2)
With 28.8 V I/O supply	75% 2)
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 293: X20DIF371 - Technical data

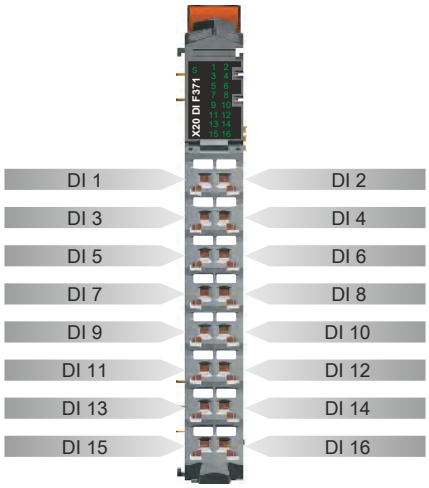
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Derating must be taken into consideration.

4.13.20.4 Status LEDs

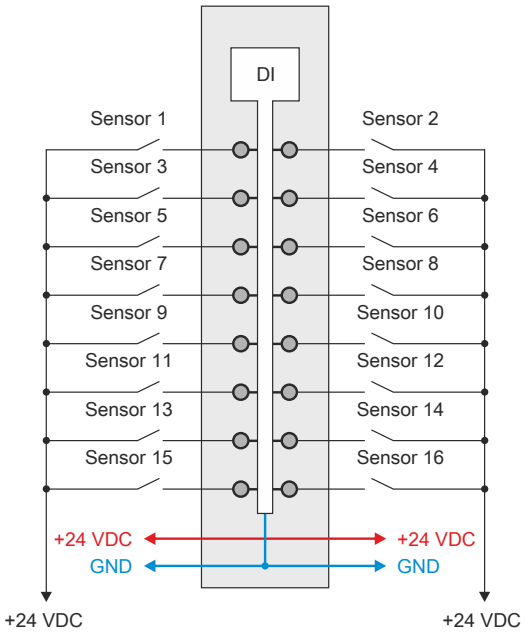
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	Module supply not connected or everything OK
		Red on / Green single flash		Invalid firmware
	1 - 16	Green		Input status of the corresponding digital input

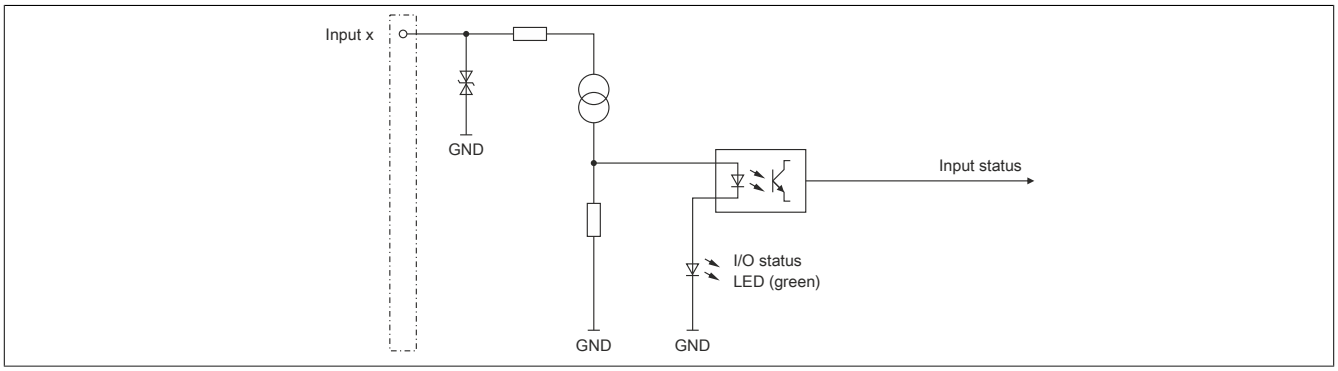
4.13.20.5 Pinout



4.13.20.6 Connection example

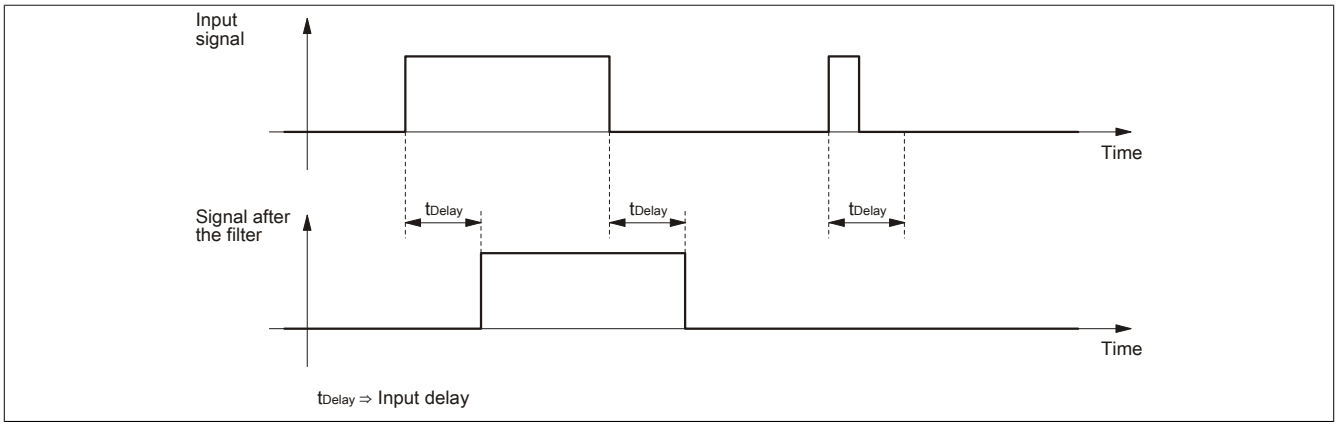


4.13.20.7 Input circuit diagram



4.13.20.8 Input filter

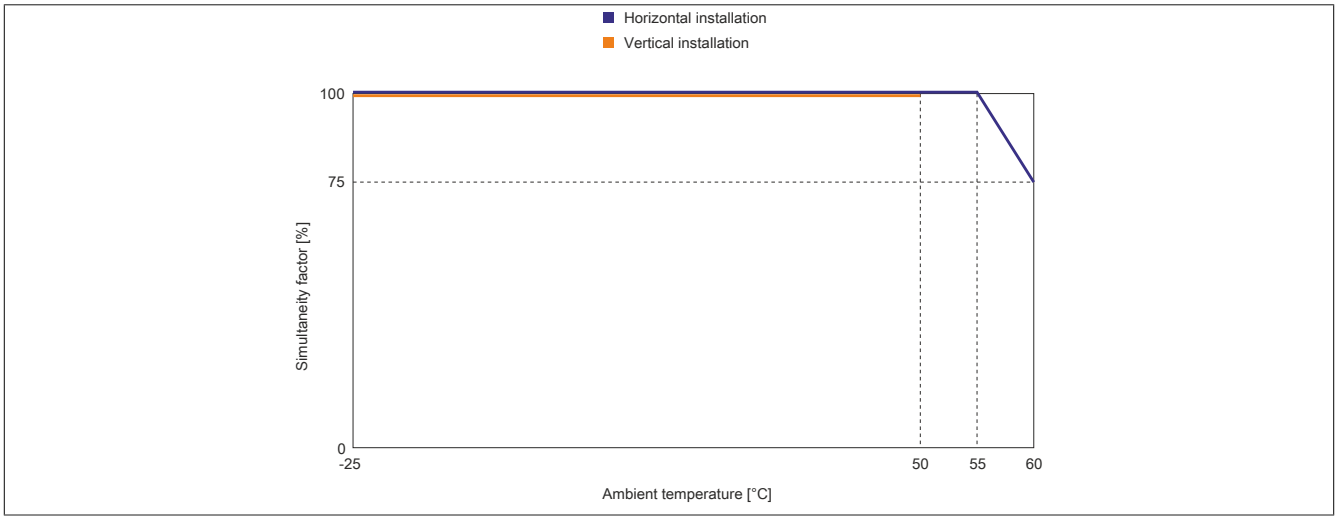
An input filter is available for each input. The input delay can be set using register 4.13.2.9.5 "ConfigOutput01". Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



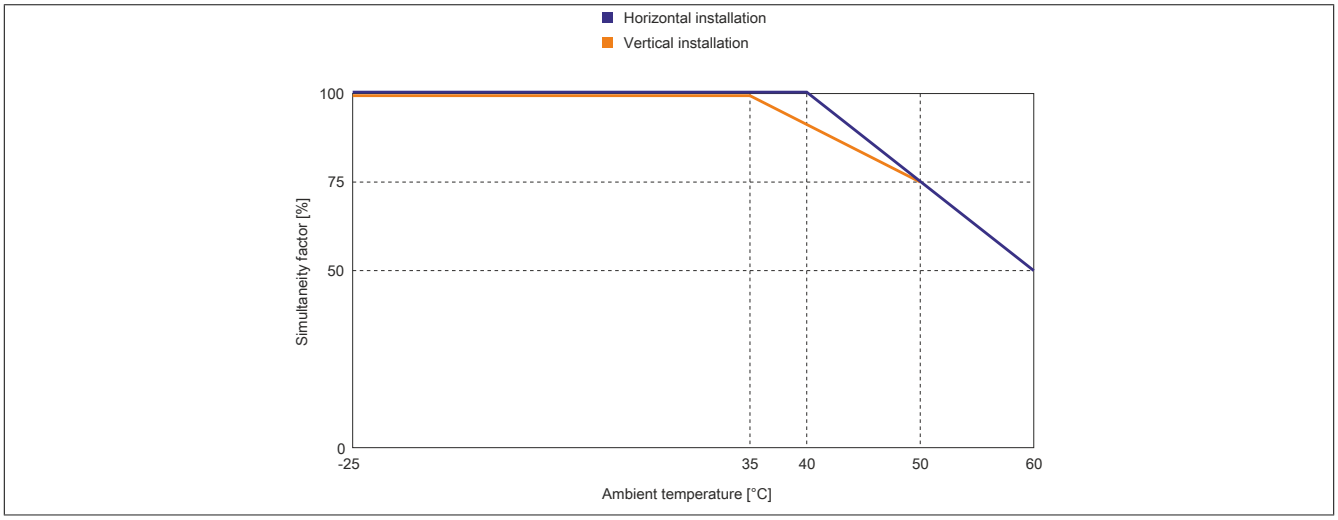
4.13.20.9 Derating

Be aware of the derating values below for the simultaneity factor.

Derating of simultaneity factor at 24 VDC input voltage



Derating of simultaneity factor at 28.8 VDC input voltage



4.13.20.10 Register description

4.13.20.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.13.20.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
-	1	DigitalInput	UINT	•			
0	1	Input status of digital inputs 1 to 8	USINT				
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
1	2	Input status of digital inputs 9 to 16	USINT	•			
		DigitalInput09	Bit 0				
		...	...				
		DigitalInput16	Bit 7				
18	-	ConfigOutput01	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.13.20.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input status of digital inputs 1 to 8	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
1	1	Input status of digital inputs 9 to 16	USINT	•			
		DigitalInput09	Bit 0				
		...	...				
		DigitalInput16	Bit 7				
18	-	ConfigOutput01	USINT				•

1) The offset specifies where the register is within the CAN object.

4.13.20.10.3.1 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN-I/O.

4.13.20.10.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.13.20.10.4.1 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.13.20.10.4.2 Input status of digital inputs 1 to 16

Name:
DigitalInput or
DigitalInput01 to DigitalInput16

The input status of digital inputs 9 to 16 is mapped in this register.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput16") or whether this register should be displayed as an individual UINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 65535	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Register 0:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input status - Digital input 8

Register 1:

Bit	Name	Value	Information
0	DigitalInput09	0 or 1	Input status - Digital input 9
...		...	
7	DigitalInput16	0 or 1	Input status - Digital input 16

4.13.20.10.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	100 µs
With filtering	150 µs

4.13.20.10.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	100 µs
With filtering	200 µs

4.14 Digital mixed modules

Digital mixed modules are a combination of digital input and output modules. The states of the digital inputs or outputs are shown by the status LEDs.

4.14.1 Brief information

Product ID	Short description	on page
X20DM9324	X20 digital mixed module, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source 1-wire connections	1338
X20cDM9324	X20 digital mixed module, coated, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source, 1-wire connections	1338

4.14.2 X20(c)DM9324

4.14.2.1 General information

This module is equipped with 8 inputs and 4 outputs for 1-wire connections. The inputs are designed for sink connections, the outputs for source connections.

- 8 digital inputs, sink connections
- 4 digital outputs, source connections
- 1-wire connections
- Configurable software input filter for entire module
- Integrated output protection

4.14.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.14.2.3 Order data

Model number	Short description	Figure
	Digital inputs/outputs	
X20DM9324	X20 digital mixed module, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source 1-wire connections	
X20cDM9324	X20 digital mixed module, coated, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 294: X20DM9324, X20cDM9324 - Order data

4.14.2.4 Technical data

Product ID	X20DM9324	X20cDM9324
Short description		
I/O module	8 digital inputs 24 VDC for 1-wire connections, 4 digital outputs 24 VDC for 1-wire connections	
General information		
Nominal voltage	24 VDC	
B&R ID code	0x20B9	0xE225
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	
Power consumption		
Bus	0.21 W	
Internal I/O	0.5 W	
External I/O	1.17 W	
Additional power dissipation caused by the actuators (resistive) [W] [1]	+0.21	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
Digital inputs		
Input voltage	24 VDC -15 % / +20 %	
Input current at 24 VDC	Typ. 3.75 mA	
Input filter		
Hardware	≤100 µs	
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Connection type	1-wire connections	
Input circuit	Sink	
Input resistance	Typ. 6.4 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Digital outputs		
Design	FET positive switching	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	0.5 A	
Total nominal current	2 A	
Connection type	1-wire connections	
Output circuit	Source	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	5 µA	
$R_{DS(on)}$	210 mΩ	
Residual voltage	<0.3 V at 0.5 A rated current	
Max. continuous current	6 A	
Peak short circuit current	<12 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay		
0 -> 1	<300 µs	
1 -> 0	<300 µs	
Switching frequency		
Resistive load	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	

Table 295: X20DM9324, X20cDM9324 - Technical data

Product ID	X20DM9324	X20cDM9324
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 295: X20DM9324, X20cDM9324 - Technical data

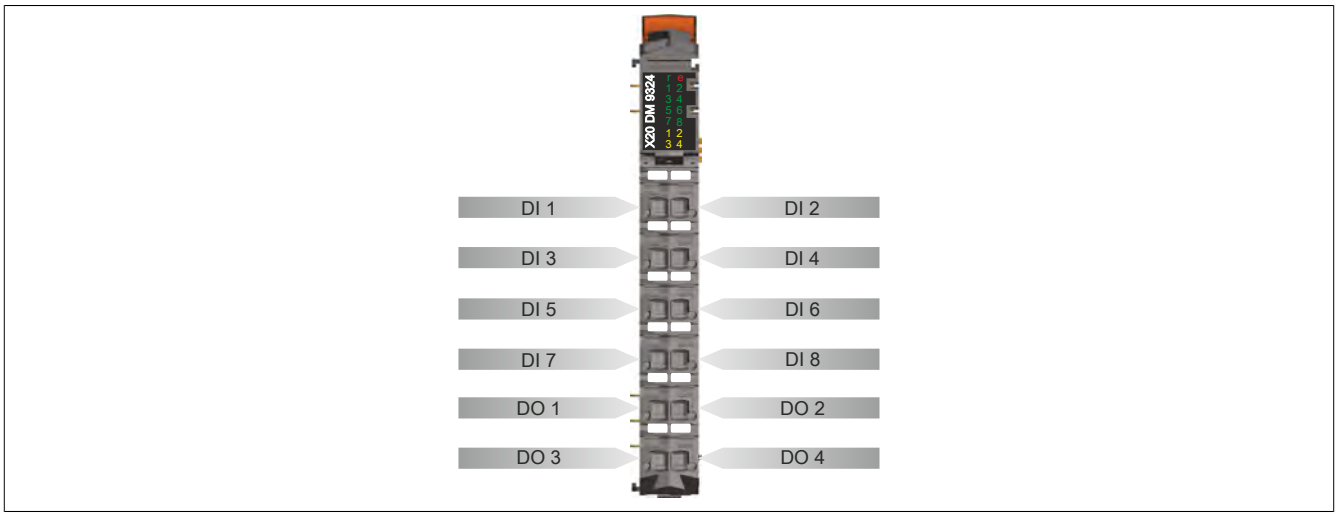
1) Number of outputs x $R_{DS(on)}$ x nominal output current[2]
2) Ta min.: 0°C
   Ta max.: See environmental conditions

4.14.2.5 Status LEDs

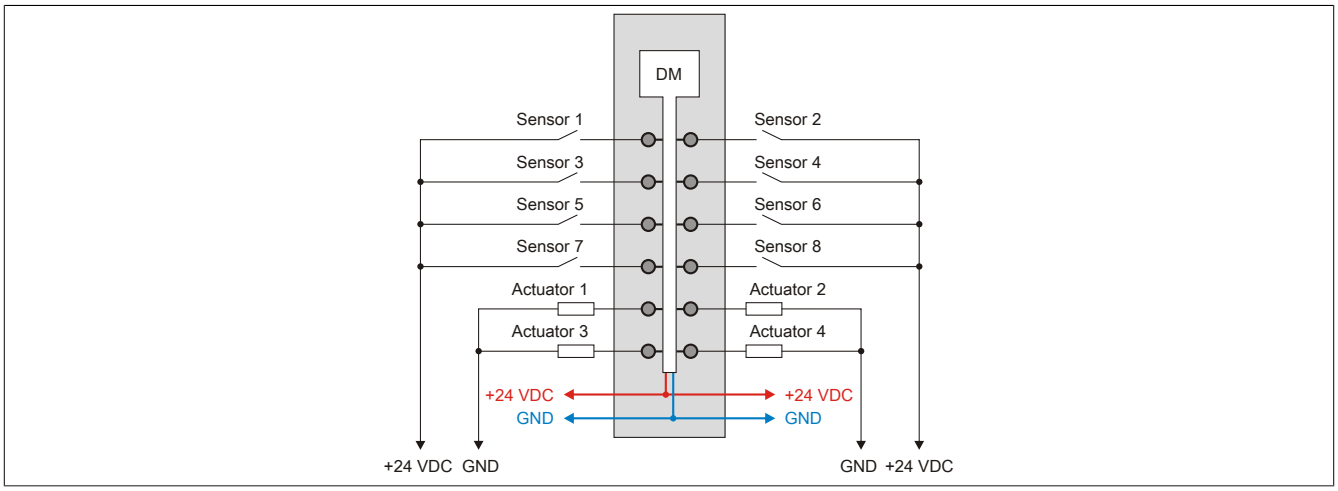
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Green		Input status of the corresponding digital input
	1 - 4	Orange		Output status of the corresponding digital output

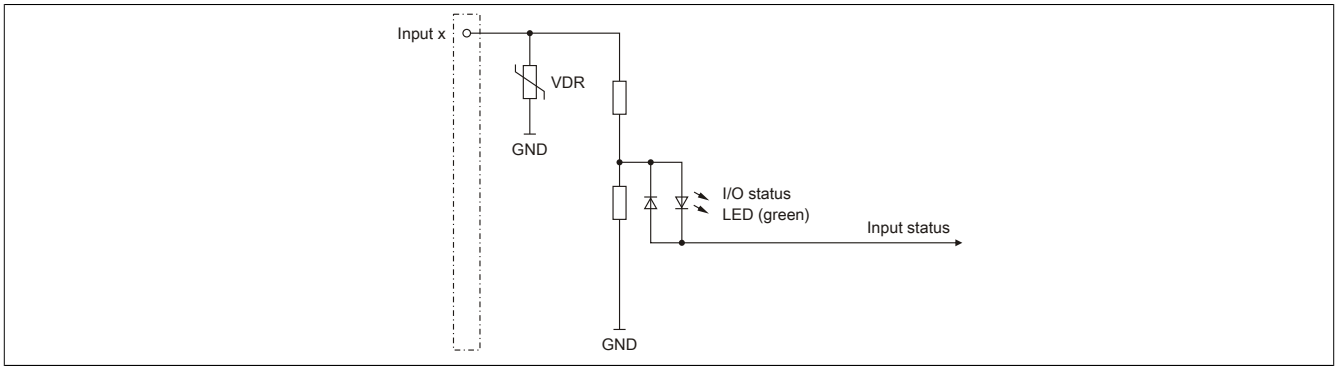
4.14.2.6 Pinout



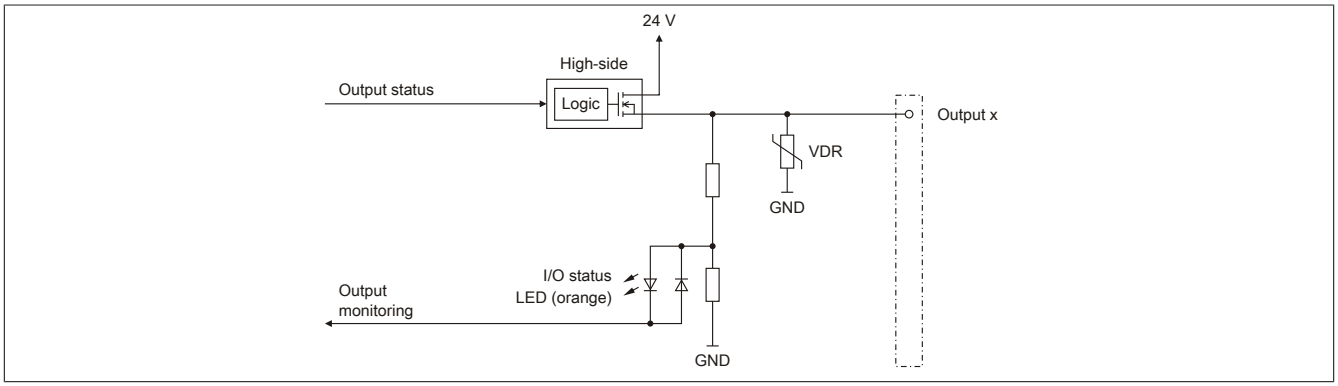
4.14.2.7 Connection example



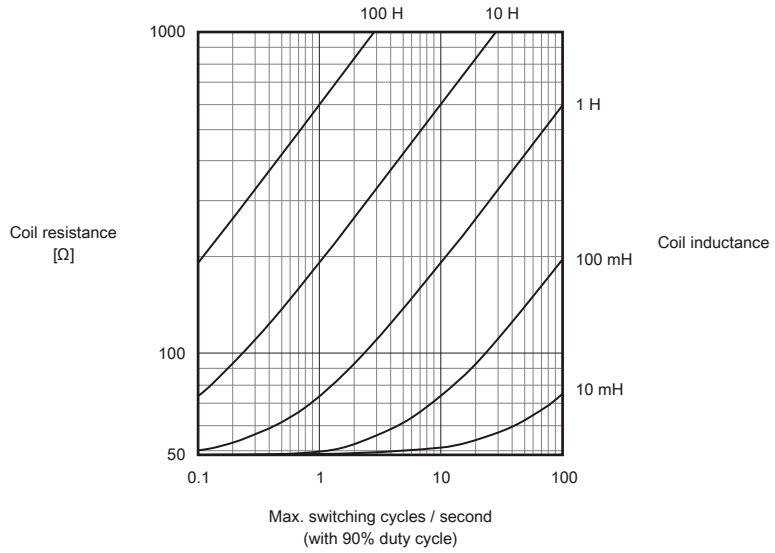
4.14.2.8 Input circuit diagram



4.14.2.9 Output circuit diagram



4.14.2.10 Switching inductive loads



4.14.2.11 Register description

4.14.2.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.14.2.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
2	0	DigitalOutput				•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
18	-	ConfigOutput01	USINT				•
30	2	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
			...				
		StatusDigitalOutput04	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.14.2.11.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Input state of digital inputs 1 to 8	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
2	0	Switching state of digital outputs 1 to 4				•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
18	-	ConfigOutput01	USINT				•
30	-	Status of digital outputs 1 to 4	USINT		•		
		StatusDigitalOutput01	Bit 0				
			...				
		StatusDigitalOutput04	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.14.2.11.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.14.2.11.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.14.2.11.4.1 Input state of digital inputs 1 to 8

Name:
DigitalInput or
DigitalInput01 to DigitalInput08

This register is used to indicate the input state of digital inputs 1 to 8.

Function model 0 - Standard only:

The "packed inputs" setting in the AS I/O configuration is used to determine whether all of this register's bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput08") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 255	Packed inputs = on
	See bit structure	Packed inputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

4.14.2.11.4.2 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.14.2.11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.14.2.11.5.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

4.14.2.11.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.14.2.11.6.1 Status of digital outputs 1 to 4

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput04

The status of digital outputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit		Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
3	StatusDigitalOutput04	0	Channel 04: No error
		1	Channel 04: Short circuit or overload

4.14.2.11.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.14.2.11.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	100 µs
With filtering	200 µs

4.15 Digital output modules

Digital output modules are used to control external loads (relays, motors, solenoids). The states of the digital outputs are indicated by status LEDs.

4.15.1 Brief information

Product ID	Short description	on page
X20DO2321	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, sink, 3-wire connections	1349
X20DO2322	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, source, 3-wire connections	1357
X20DO2623	X20 digital output module, 2 outputs, 100-240 VAC, 1 A, source, 240 V keyed, 3-wire connections	1365
X20DO2633	X20 digital output module, 2 triac outputs, 12 to 240 VAC, 2 A, L switching, phase angle control, 240 V keyed	1374
X20DO2649	X20 digital output module, 2 relays, changeover contacts, 240 VAC / 5 A, 24 VDC / 5 A	1390
X20DO4321	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, sink, 3-wire connections	1396
X20DO4322	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections	1404
X20DO4331	X20 digital output module, 4 outputs, 24 VDC, 2 A, sink, 3-wire connections	1413
X20DO4332	X20 digital output module, 4 outputs, 24 VDC, 2 A, source, 3-wire connections	1423
X20DO4529	X20 digital output module, 4 relays, changeover contacts, 115 VAC / 0.5 A, 24 VDC / 1 A	1433
X20DO4613	X20 digital output module, 4 triac coupler outputs, 12 to 240 VAC, 50 mA, zero-crossing detection, 240 V keyed,...	1439
X20DO4623	X20 digital output module, 4 outputs, 100-240 VAC, 0.5 A, source, 240 V keyed, 2-wire connections	1452
X20DO4633	X20 digital output module, 4 triac outputs, 12 to 240 VAC, 1 A, L switching, phase angle control, 240 V keyed	1461
X20DO4649	X20 digital output module, 4 relays, N.O. contacts, 240 VAC / 5 A	1477
X20DO6321	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections	1483
X20DO6322	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections	1490
X20DO6325	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, open line and overload detection, 2-wire connections	1498
X20DO6529	X20 digital output module, 6 relays, normally open contacts, 115 VAC / 0.5 A, 30 VDC / 1 A	1509
X20DO6639	X20 digital output module, 6 relays, normally open contacts, 240 VAC / 2 A, 30 VDC / 2 A	1515
X20DO8232	X20 digital output module, 8 outputs, 12 VDC, 2 A, source, supply directly on module, 1-wire connections	1521
X20DO8322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 1-wire connections	1532
X20DO8323	X20 digital output module, 8 outputs, 12 to 24 V, 0.5 A, sink/source, 1-wire connections, full bridge, half bridge, thermal overload protection	1539
X20DO8331	X20 digital output module, 8 outputs, 24 VDC, 2 A, sink, supply directly on module, 1-wire connections	1548
X20DO8332	X20 digital output module, 8 outputs, 24 VDC, 2 A, source, supply directly on module, 1-wire connections	1560
X20DO9321	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections	1572
X20DO9322	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections	1580
X20DOD322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 2-wire connections	1588
X20DOF322	X20 digital output module, 16 outputs, 24 VDC, 0.5 A, source, 1-wire connections	1594
X20cDO2633	X20 digital output module, coated, 2 triac outputs, 12 to 240 VAC, 2 A, L switching, phase angle control, 240 V keyed	1374
X20cDO4322	X20 digital output module, coated, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections	1404
X20cDO4332	X20 digital output module, coated, 4 outputs, 24 VDC, 2 A, source, 3-wire connections	1423
X20cDO4633	X20 digital output module, coated, 4 triac outputs, 12 to 240 VAC, 1 A, L switching, phase angle control, 240 V keyed	1461
X20cDO4649	X20 digital output module, coated, 4 relays, N.O. contacts, 240 VAC / 5 A	1477
X20cDO6321	X20 digital output module, coated, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections	1483
X20cDO6322	X20 digital output module, coated, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections	1490
X20cDO6639	X20 digital output module, coated, 6 relays, normally open contacts, 240 VAC / 2 A, 30 VDC / 2 A	1515
X20cDO8331	X20 digital output module, coated, 8 outputs, 24 VDC, 2 A, sink, supply directly on module, 1-wire connections	1548
X20cDO8332	X20 digital output module, coated, 8 outputs, 24 VDC, 2 A, source, supply directly on module, 1-wire connections	1560
X20cDO9321	X20 digital output module, coated, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections	1572
X20cDO9322	X20 digital output module, coated, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections	1580

4.15.2 Calculation of the additional power dissipation resulting from actuators

Calculation of power dissipation when specifying $R_{DS(on)}$

Explaining output load with an X20DO4332 example

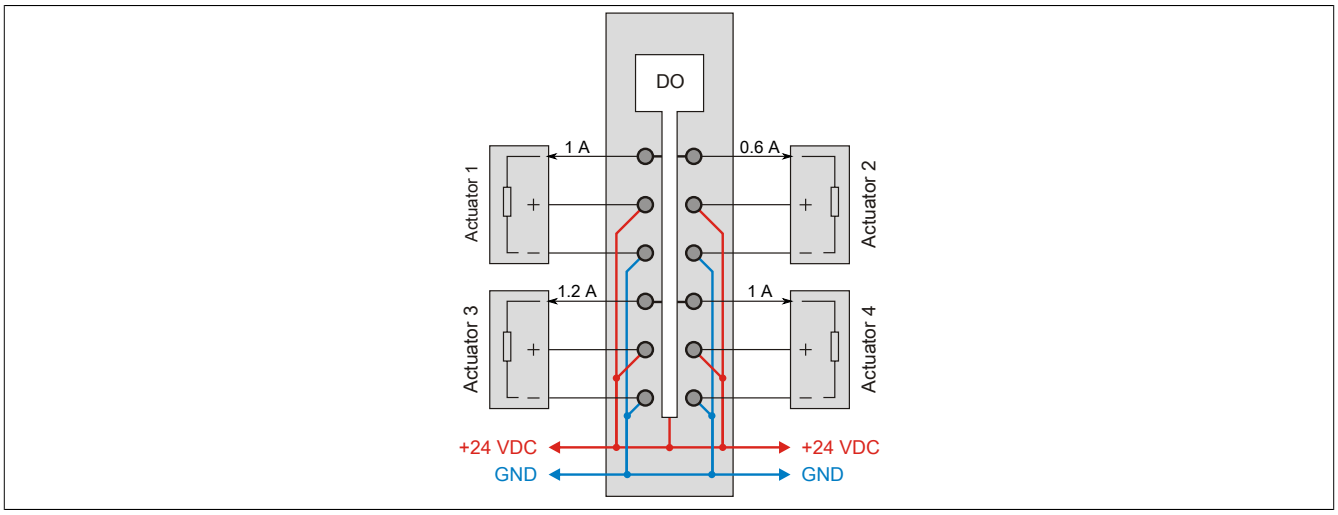


Figure 236: Calculation of power dissipation when specifying $R_{DS(on)}$

Theoretically highest power dissipation resulting from actuators:

Number of outputs * RDS_{on} * nominal output current² = power dissipation

4 * 140 mΩ * 2 A^2 = 2.24 W

Power dissipation resulting from actuators in this example:

140 mΩ * (1 A^2 + 0.6 A^2 + 1.2 A^2 + 1 A^2) = 0.532 W

Power dissipation calculation when specifying the residual voltage

Explaining output load with an X20DO4623 example

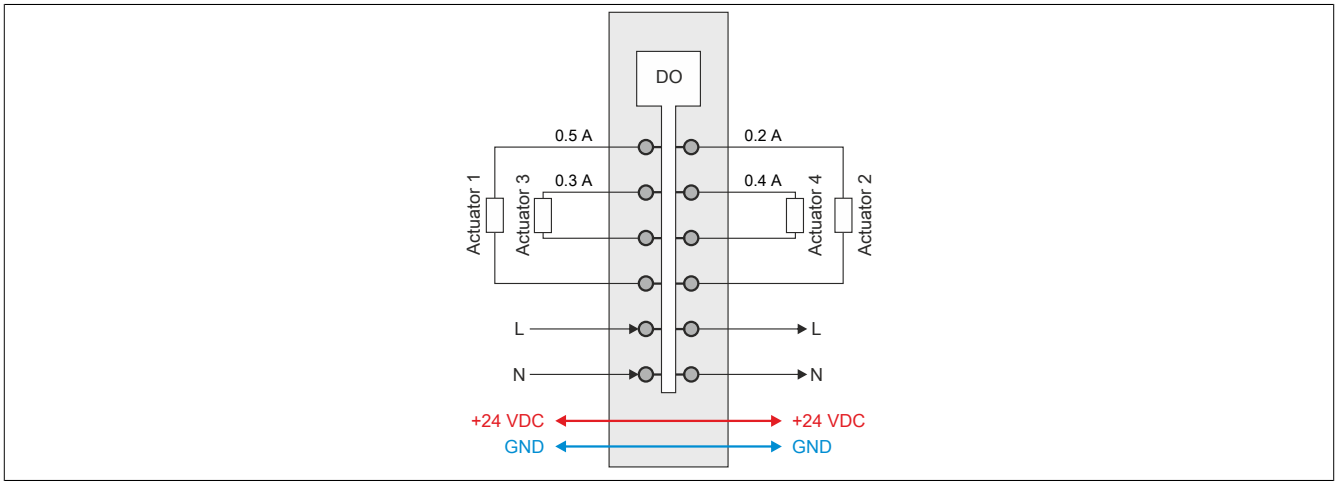


Figure 237: Power dissipation calculation when specifying the residual voltage

Theoretically highest power dissipation resulting from actuators:

Number of outputs * residual voltage * nominal output current = power dissipation

4 * 1.6 V * 0.5 A = 3.2 W

Power dissipation resulting from actuators in this example:

1.6 V * (0.5 A + 0.2 A + 0.3 A + 0.4 A) = 2.24 W

Power dissipation calculation when specifying the contact resistance

Explaining output load with an X20DO4649 example

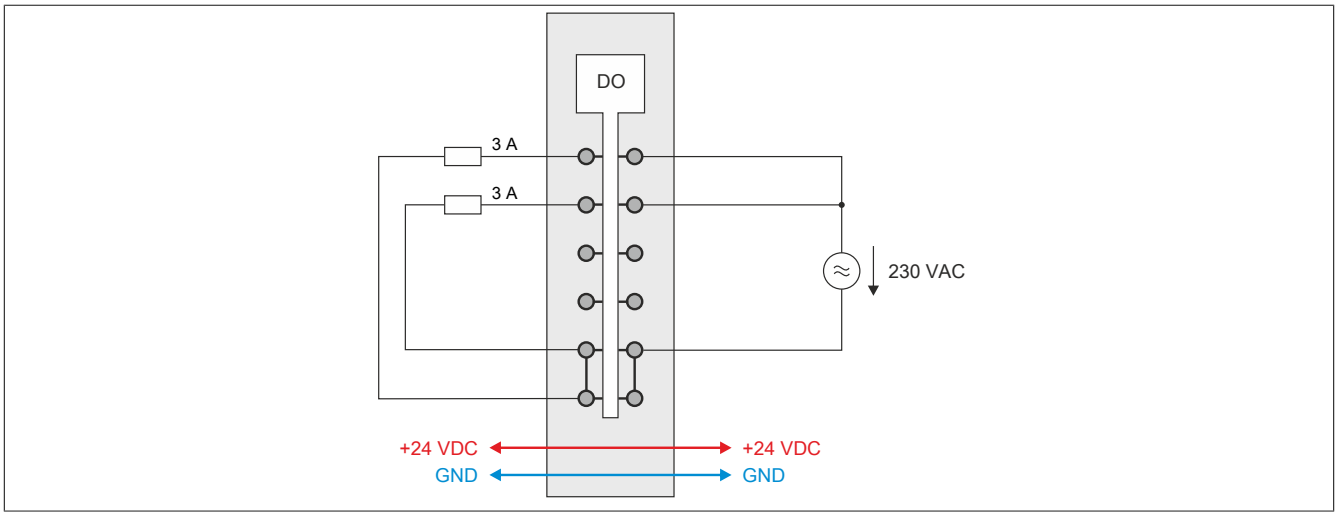


Figure 238: Power dissipation calculation when specifying the contact resistance

Theoretically highest power dissipation resulting from actuators:

Number of outputs * contact resistance * nominal output current^2 = power dissipation

4 * 15 mΩ * 5 A^2 = 1.5 W

Power dissipation resulting from actuators in this example:

15 mΩ * (3 A^2 + 3 A^2) = 0.27 W

4.15.3 X20DO2321

4.15.3.1 General information

The module is equipped with 2 outputs for 3-wire connections. It is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 digital outputs
- Sink connection
- 3-wire connections
- 24 VDC and GND for actuator supply
- Integrated output protection
- OSP mode

4.15.3.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO2321	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, sink, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 296: X20DO2321 - Order data

4.15.3.3 Technical data

Product ID	X20DO2321
Short description	
I/O module	2 digital outputs 24 VDC for 3-wire connections
General information	
B&R ID code	0x22B3
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.13 W
Internal I/O	0.3 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+0.06
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Design	FET negative switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	1 A
Connection type	3-wire connections
Output circuit	Sink

Table 297: X20DO2321 - Technical data

Product ID	X20DO2321
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")
Actuator supply	0.5 A in total for output-independent actuator supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	75 µA
$R_{DS(on)}$	120 mΩ
Peak short circuit current	<7 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load	Max. 500 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 50 VDC
Isolation voltage between channel and bus	500 V_{eff}
Actuator supply	
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 V
Short circuit protection	Yes
Power consumption	
Actuator supply	Max. 12 W [3]
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 297: X20DO2321 - Technical data

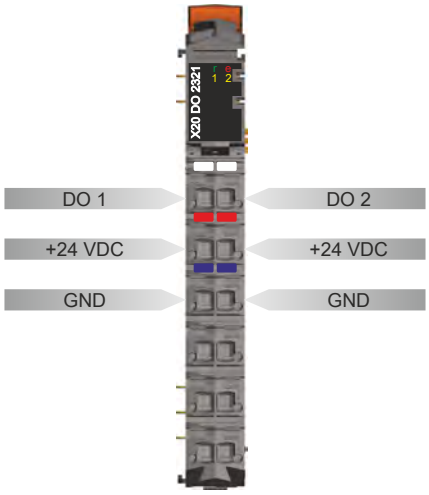
1) Number of outputs x $R_{DS(on)}$ x Nominal output current² (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.15.3.4 Status LEDs

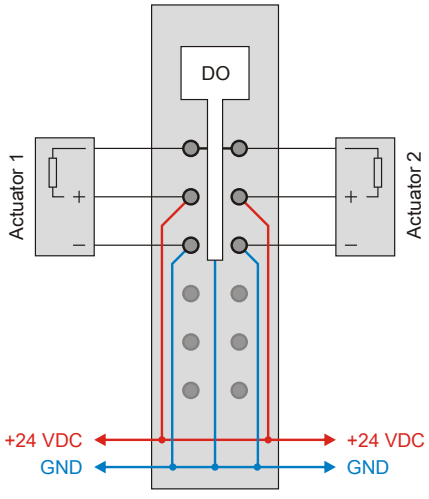
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	Reset mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Orange		Output status of the corresponding digital output

4.15.3.5 Pinout



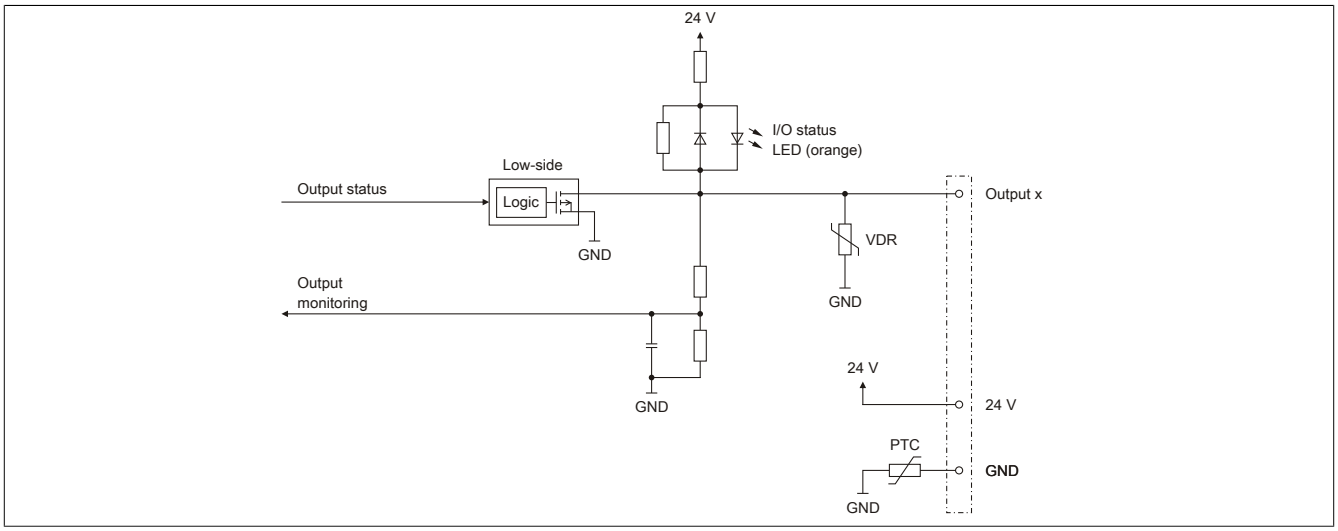
4.15.3.6 Connection example



4.15.3.7 OSP hardware requirements

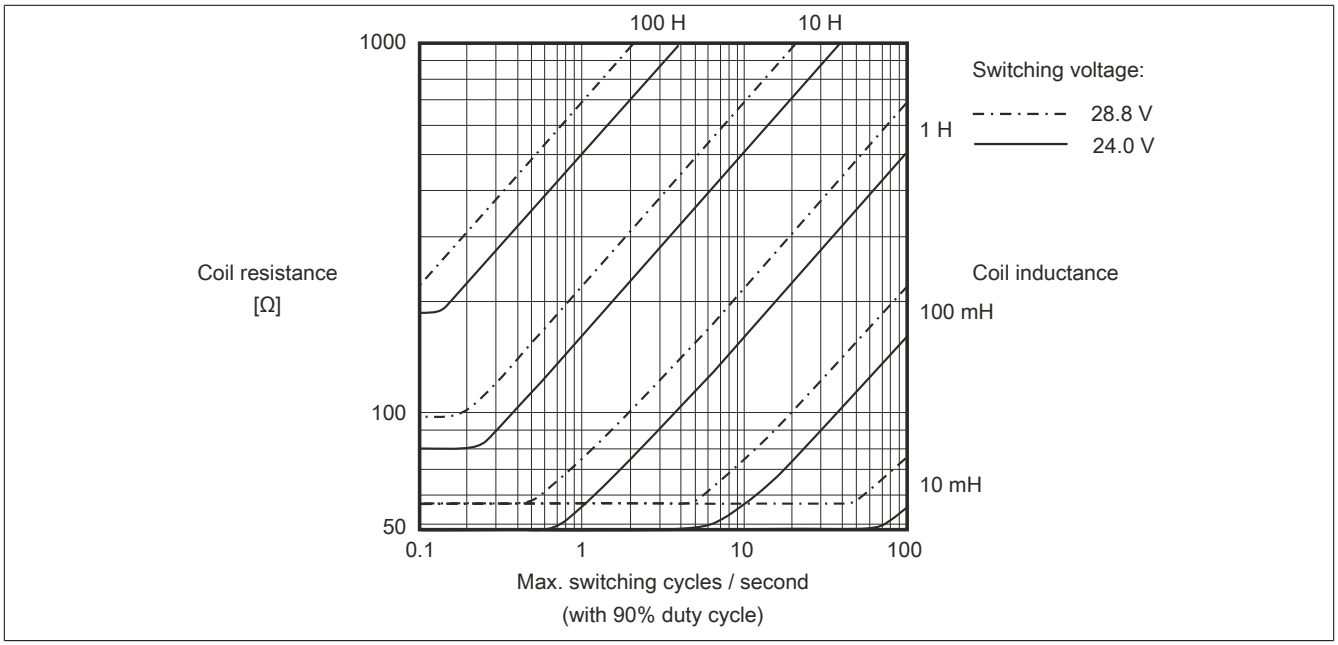
In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.3.8 Output circuit diagram



4.15.3.9 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.3.10 Register description

4.15.3.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.3.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.3.10.3 Function model 1 - OSP

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	1	Status of digital outputs 1 to 2	USINT	•			
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				
34	1	Activating the OSP output in the module	USINT			•	
		OSPValid	Bit 0				
32	-	CfgOSPMode	USINT				•
36	-	CfgOSPValue	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.3.10.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	-	Status of digital outputs 1 to 2	USINT		•		
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				

1) The offset specifies where the register is within the CAN object.

4.15.3.10.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.3.10.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.3.10.5.1 Switching state of digital outputs 1 to 2

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput02

This register is used to store the switching state of digital outputs 1 to 2.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 3	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
1	DigitalOutput02	0	Digital output 02 reset
		1	Digital output 02 set

4.15.3.10.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.3.10.6.1 Status of digital outputs 1 to 2

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput02

The status of digital outputs 1 to 2 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 3	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
1	StatusDigitalOutput02	0	Channel 02: No error
		1	Channel 02: Short circuit or overload

4.15.3.10.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.3.10.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.3.10.7.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.3.10.7.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.3.10.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.3.10.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.4 X20DO2322

4.15.4.1 General information

The module is equipped with 2 outputs for 3-wire connections. It is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 digital outputs
- Source connection
- 3-wire connections
- 24 VDC and GND for actuator supply
- Integrated output protection
- OSP mode

4.15.4.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO2322	X20 digital output module, 2 outputs, 24 VDC, 0.5 A, source, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 298: X20DO2322 - Order data

4.15.4.3 Technical data

Product ID	X20DO2322
Short description	
I/O module	2 digital outputs 24 VDC for 3-wire connections
General information	
B&R ID code	0x1B96
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.13 W
Internal I/O	0.33 W
Additional power dissipation caused by the actuators (resistive) [W] [1]	+0.1
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital outputs	
Design	FET positive switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	1 A
Connection type	3-wire connections

Table 299: X20DO2322 - Technical data

Product ID	X20DO2322
Output circuit	Source
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")
Actuator supply	0.5 A in total for output-independent actuator supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
$R_{DS(on)}$	210 mΩ
Max. continuous current	6 A
Peak short circuit current	<12 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay [3]	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load [3]	Max. 500 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 50 VDC
Isolation voltage between channel and bus	500 V_{eff}
Actuator supply	
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 V
Short circuit protection	Yes
Power consumption	
Actuator supply	Max. 12 W [4]
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 299: X20DO2322 - Technical data

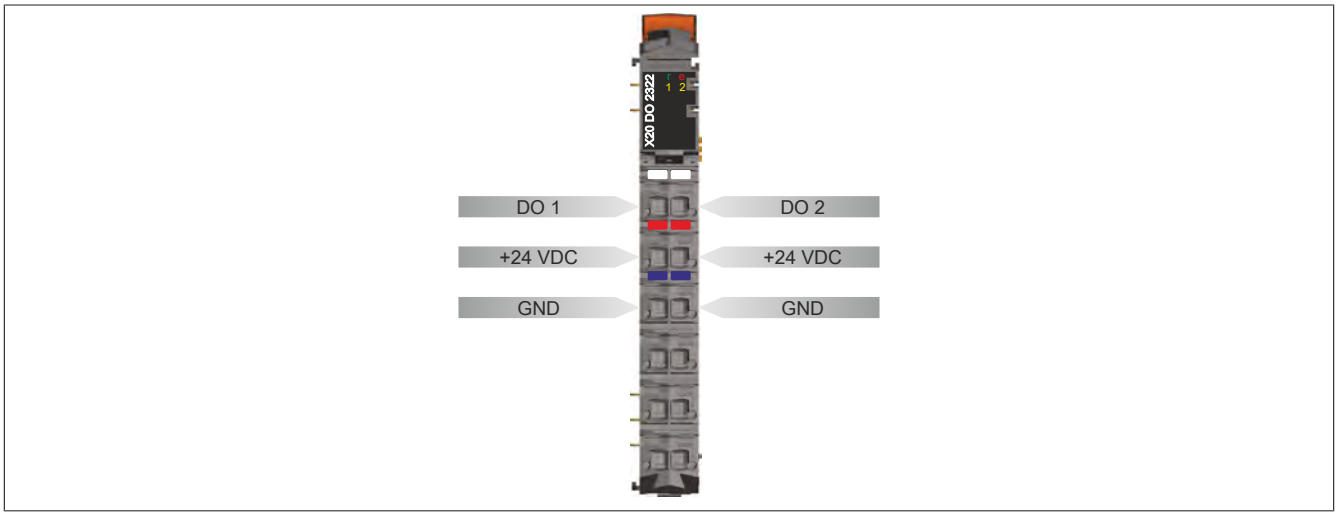
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) At loads ≤ 1 kΩ
4) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.15.4.4 Status LEDs

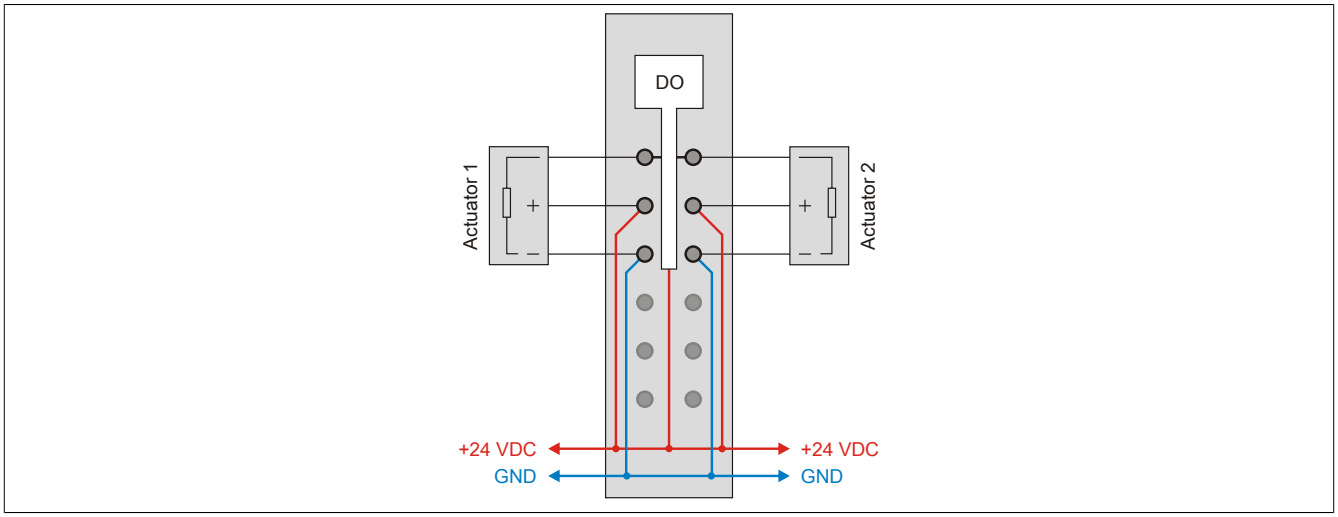
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Orange		Output status of the corresponding digital output

4.15.4.5 Pinout



4.15.4.6 Connection example



Caution!

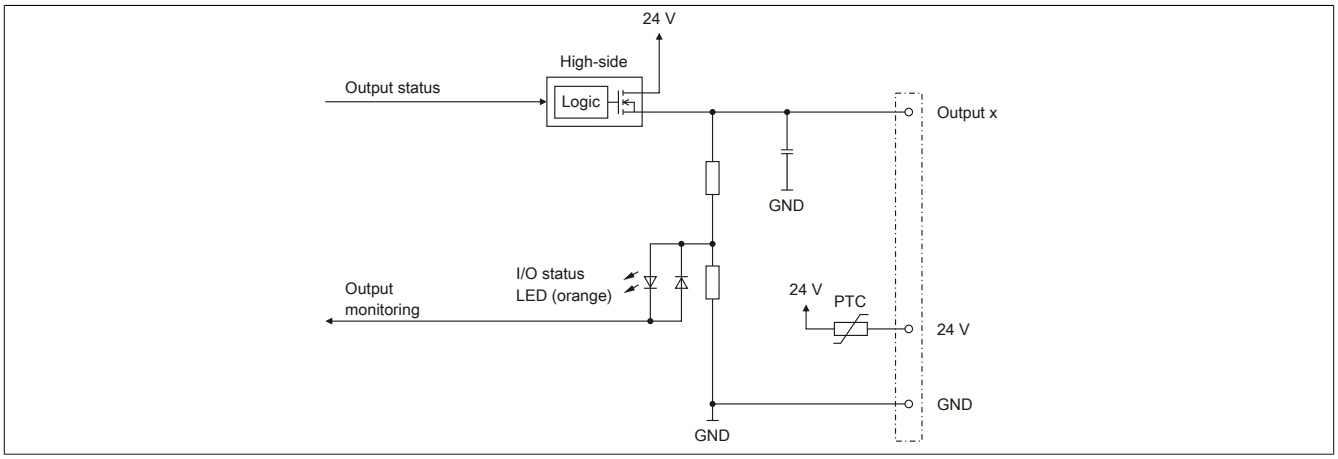
If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

Therefore sufficient cable cross sections or external safety measures must be used.

4.15.4.7 OSP hardware requirements

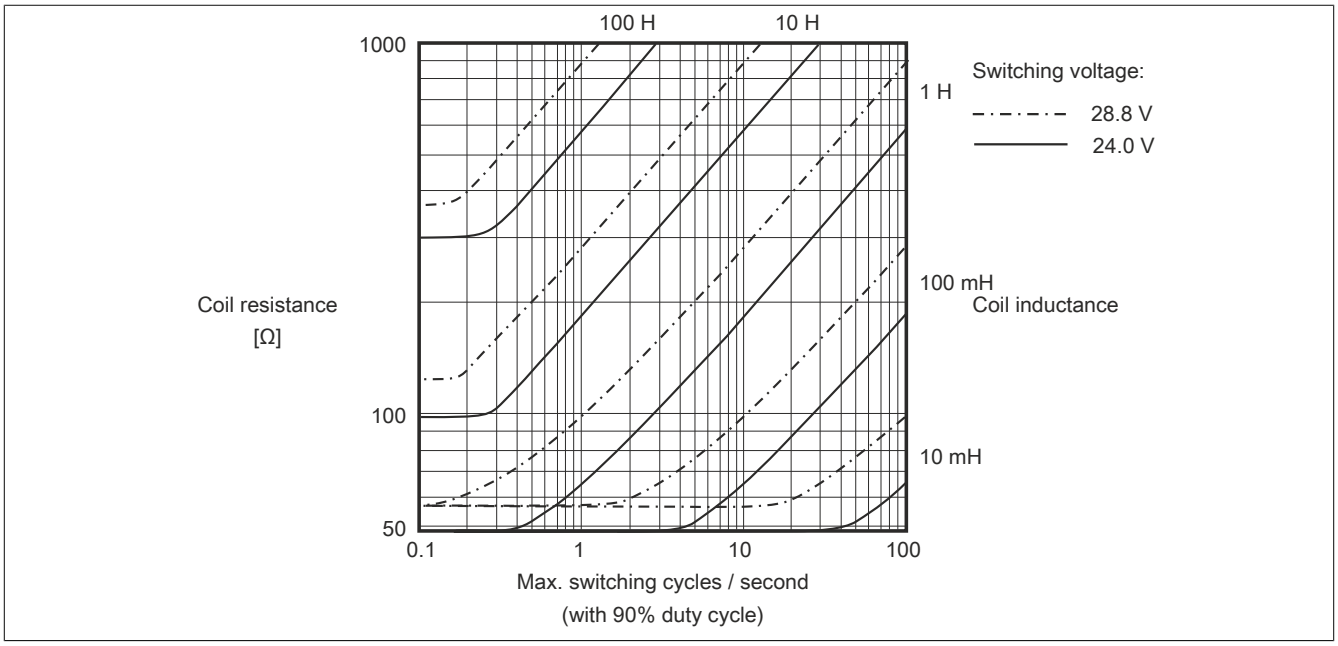
In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.4.8 Output circuit diagram



4.15.4.9 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.4.10 Register description

4.15.4.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.4.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.4.10.3 Function model 1 - OSP

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	1	Status of digital outputs 1 to 2	USINT	•			
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				
34	1	Activating the OSP output in the module	USINT			•	
		OSPValid	Bit 0				
32	-	CfgOSPMode	USINT				•
36	-	CfgOSPValue	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.4.10.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
30	-	Status of digital outputs 1 to 2	USINT		•		
		StatusDigitalOutput01	Bit 0				
		StatusDigitalOutput02	Bit 1				

1) The offset specifies where the register is within the CAN object.

4.15.4.10.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.4.10.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.4.10.5.1 Switching state of digital outputs 1 to 2

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput02

This register is used to store the switching state of digital outputs 1 to 2.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 3	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
1	DigitalOutput02	0	Digital output 02 reset
		1	Digital output 02 set

4.15.4.10.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.4.10.6.1 Status of digital outputs 1 to 2

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput02

The status of digital outputs 1 to 2 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 3	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
1	StatusDigitalOutput02	0	Channel 02: No error
		1	Channel 02: Short circuit or overload

4.15.4.10.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.4.10.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.4.10.7.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.4.10.7.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.4.10.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.4.10.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.5 X20DO2623

4.15.5.1 General information

The module is a digital output module that is equipped with 2 SSR outputs with zero cross-over switches and uses 3-line connections. The module is also equipped with integrated full-wave control. The supply (L and N) is fed directly to the module.

- 2 digital outputs
- Outputs with integrated snubber circuit
- Outputs with 100 to 240 VAC
- L switching
- 50 Hz or 60 Hz
- 3-wire connections
- Integrated full-wave control
- 240 V coding

Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.15.5.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO2623	X20 digital output module, 2 outputs, 100-240 VAC, 1 A, source, 240 V keyed, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 300: X20DO2623 - Order data

4.15.5.3 Technical data

Product ID	X20DO2623
Short description	
I/O module	2 digital SSR outputs 100 to 240 VAC for 3-wire connections
General information	
B&R ID code	0x267B
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED
Power consumption	
Bus	0.35 W
Internal I/O	-
External I/O	0.38 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+3
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Design	SSR
Wiring	L switching
Nominal voltage	100 to 240 VAC
Max. voltage	264 VAC
Rated frequency	47 to 63 Hz
Nominal output current	1 A
Total nominal current	1 A
Surge current	40 A (20 ms), 10 A (1 s)
Connection type	3-wire connections
Zero crossing switches	Yes
Leakage current	Max. 10 mA at 240 V
Residual voltage (on-state voltage)	1.5 V
Switching delay	
At 50 Hz	
0 -> 1	≤11 ms
1 -> 0	≤11 ms
At 60 Hz	
0 -> 1	≤9.3 ms
1 -> 0	≤9.3 ms
Isolation voltage between channel and bus	Tested at 2500 VAC
Voltage monitoring L - N	No
Overvoltage protection between L and N	Yes
Output voltage	
Minimum	80 VAC
Protective circuit	
External	Generally a varistor or fuse
Internal	Snubber circuit (RC element)
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C

Table 301: X20DO2623 - Technical data

Product ID	X20DO2623
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM12 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 301: X20DO2623 - Technical data

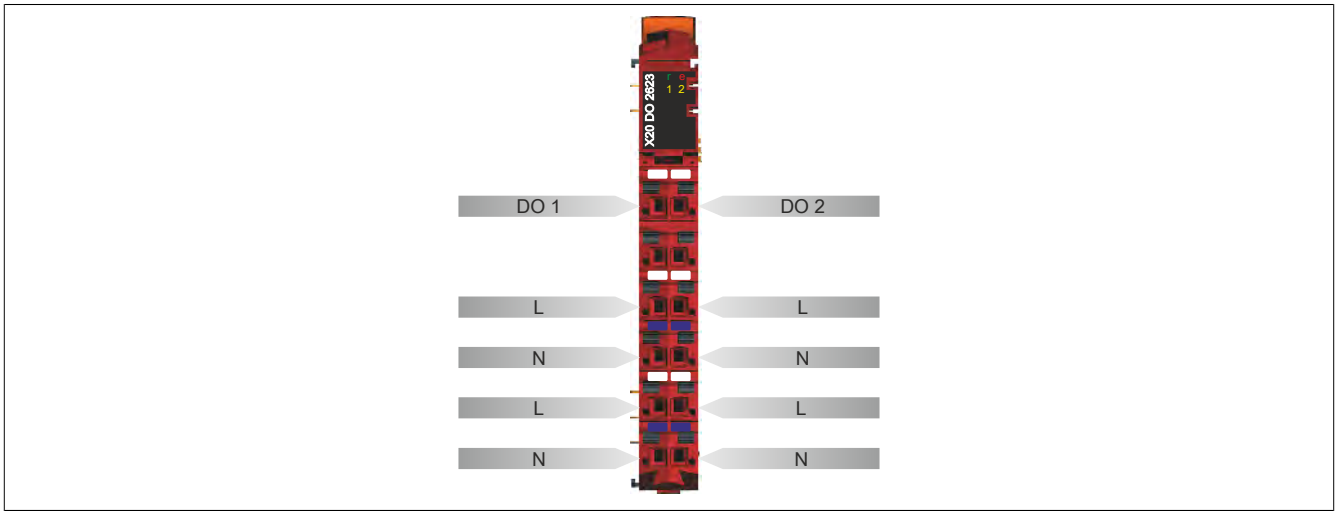
1) Number of outputs x residual voltage (on-state voltage) x nominal output current (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.15.5.4 Status LEDs

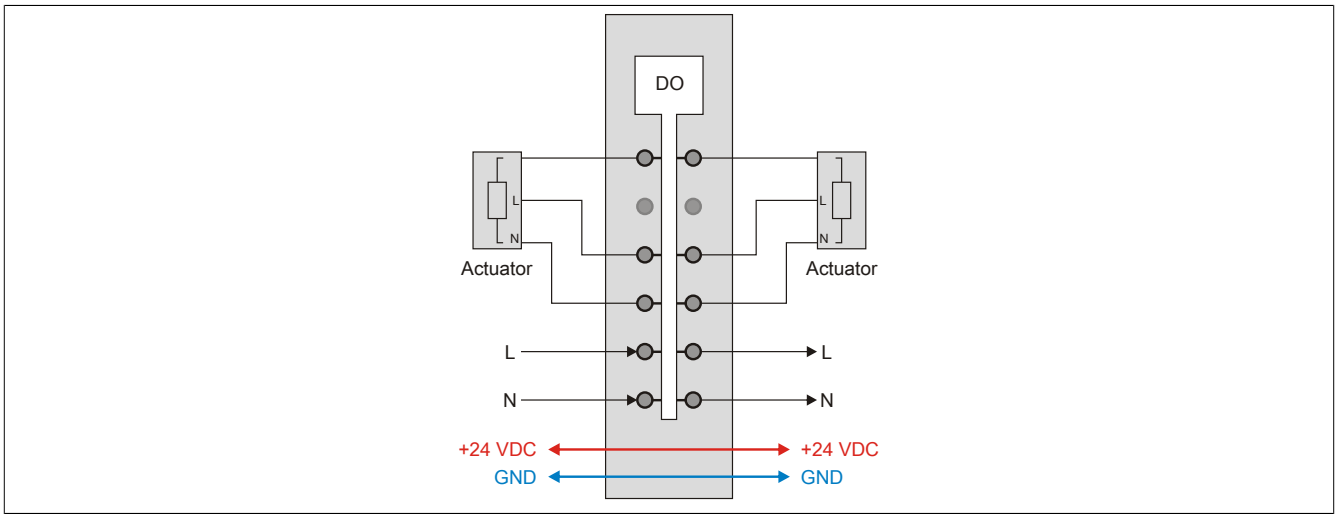
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	Reset mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Zero cross-over signal has dropped out
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Orange		Control status of the corresponding digital output

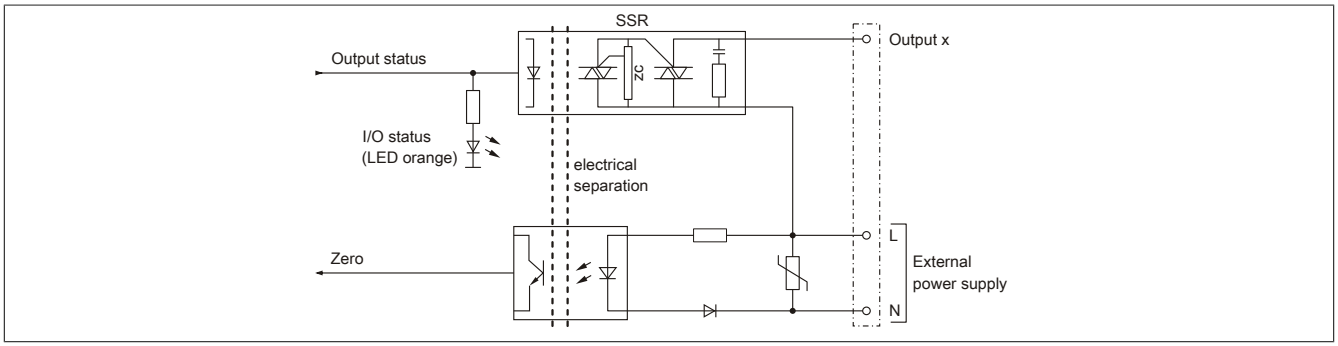
4.15.5.5 Pinout



4.15.5.6 Connection example



4.15.5.7 Output circuit diagram



4.15.5.8 Integrated full-wave control

Full-wave control is used to control power for electrical power consumers that are operated with AC voltage. Temperature control is a typical application

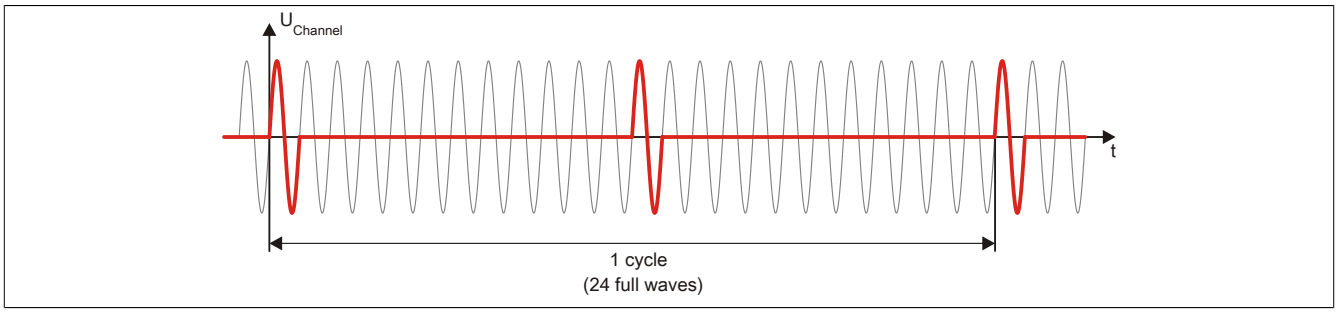
Unlike phase-angle control, the sine wave oscillation form of the mains voltage is not changed during full-wave control. This significantly reduces system perturbation.

The output voltage (channel) is switched on and off at a certain ratio. This switches the multi-cycle packets. A multi-cycle packet consists of a number of complete sine waves throughout a cycle. The relationship between the power-on duration and the cycle duration results in the desired effect of reduced power consumption by the connected power consumer.

With the full-wave control that is integrated in the module, a maximum of 24 full waves can be provided on the outputs per cycle. Control takes place in 4% steps.

Settings		Full waves																						
SW%	%	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
0	0																								
4		•																							
8		•												•											
12		•								•								•							
16		•						•						•						•					
20		•					•					•					•					•			
24	25	•				•				•				•				•				•			
28		•				•			•				•			•				•			•		
32		•			•			•			•			•			•			•			•		
36		•			•			•		•			•			•		•			•			•	
40		•			•		•			•		•		•			•		•			•		•	
44		•			•		•		•		•		•			•		•		•		•		•	
48	50	•		•		•		•		•		•		•		•		•		•		•		•	
52			•	•		•		•		•		•		•	•		•		•		•		•		•
56			•	•		•		•	•		•		•		•	•		•		•	•		•		•
60			•	•		•	•		•		•	•		•	•		•		•	•		•	•		•
64			•	•		•	•		•	•		•	•		•	•		•	•		•	•		•	•
68			•	•	•		•	•		•	•	•		•	•		•	•	•		•	•		•	•
72	75		•	•	•		•	•	•		•	•	•		•	•	•		•	•	•		•	•	•	•
76			•	•	•	•		•	•	•	•		•	•	•	•		•	•	•	•		•	•	•	•
80			•	•	•	•	•		•	•	•	•	•		•	•	•	•	•		•	•	•	•	•	•
84			•	•	•	•	•	•	•		•	•	•	•	•	•	•		•	•	•	•	•	•	•	•
88			•	•	•	•	•	•	•	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•	•
92			•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
96	100	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

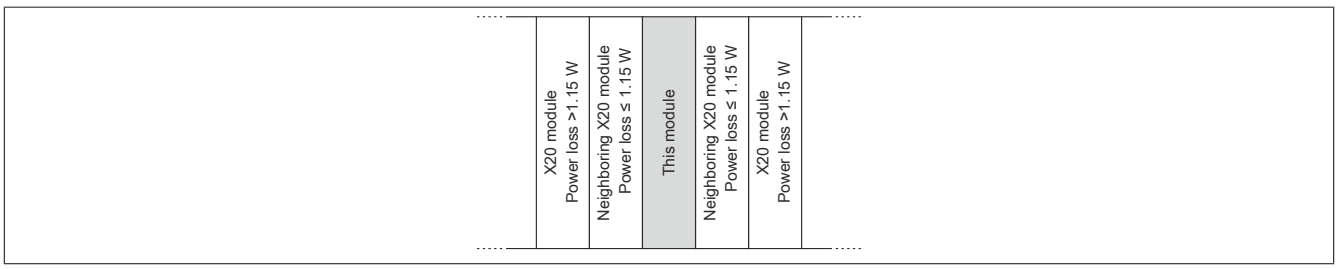
Example of full-wave control (8%):



4.15.5.9 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.15.5.10 Register description

4.15.5.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.5.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
4	1	AnalogOutput01	USINT			•	
6	2	AnalogOutput02	USINT			•	
12	3	ShiftOutput01[1)]	USINT			•	
14	4	ShiftOutput02[1)]	USINT			•	
28	-	Output configuration 1 - 2 ConfigOutput01	USINT				•
30	1	StatusInput01	USINT	•			
		ZeroCrossingInput	Bit 0				
		ZeroCrossingStatus	Bit 4				

1) Firmware version 816 and up.

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.5.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
4	0	AnalogOutput01	USINT			•	
6	2	AnalogOutput02	USINT			•	
12	-	ShiftOutput01[2)]	USINT				•
14	-	ShiftOutput02[2)]	USINT				•
30	0	Zero crossing status	USINT	•			
		ZeroCrossingInput	Bit 0				
		ZeroCrossingStatus	Bit 4				

1) The offset specifies where the register is within the CAN object.
2) Firmware version 816 and up.

4.15.5.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.15.5.10.4 Digital outputs

The output status is transferred to the control switch asynchronously to the connected network. The outputs switch on when the voltage crosses zero and switch off when the current crosses zero.

4.15.5.10.4.1 Switching state of digital outputs 1 to 2

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput02

This register is used to store the switching state of digital outputs 1 to 2.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 3	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
1	DigitalOutput02	0	Digital output 02 reset
		1	Digital output 02 set

Information:

The states in this register are only applied when the channels are set to DIGITAL in "Setting the output configuration ".

When using the setting "packed outputs" ALL channels must be set to DIGITAL. Mixed operation is not possible.

4.15.5.10.5 Analog outputs

The output value is transferred to the control circuit in sync with the connected power mains according to the firing pattern table (see "Integrated full-wave control"). The analog value is output with a resolution of ~4% over a duration of 24 complete waves. Values > 96% result in full control. Changes to the output value within an interval are applied after the next zero crossover.

4.15.5.10.5.1 Setting the output value from the firing pattern table

Name:
AnalogOutput01 to AnalogOutput02

These registers are used to set the output value from the firing pattern table.

Values between 0 and 100 correspond to the output value for the respective channel in percent. Values above 100 correspond to 100%.

Data type	Value
USINT	0 to 100

Information:

The states in these registers are only applied when the channels are set to ANALOG in Setting the output configuration .

4.15.5.10.5.2 Setting the output configuration

Name:
Output configuration 1 - 2 ConfigOutput01

Each channel can be configured for either "digital" or "analog" operation in this register. The corresponding DigitalOutput or AnalogOutput registers must be written depending on the setting.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel 1	0	Digital register is used
		1	Analog register is used
1	Channel 2	0	Digital register is used
		1	Analog register is used
2 - 7	Reserved	0	

4.15.5.10.5.3 Shift switching pattern

Name:
ShiftOutput01 to ShiftOutput02

To prevent load peaks due to simultaneous switching of outputs, this register can be used to shift the switching pattern by a number of full waves. Due to the hardware used, it is not possible to shift by less than a full wave.

Values higher than 23 are limited to 23.

Data type	Value	Information
USINT	0	No shift
	1 to 23	Size of the shift in number of full waves

Example

Set 0 on Channel 1 and 1 on Channel 2. With the same control value (see "Integrated full-wave control") this delays the switching pattern of Channel 2 by one full wave.

4.15.5.10.6 Zero crossing status

Name:
ZeroCrossingInput
ZeroCrossingStatus
StatusInput01

Zero crossing detection uses a fixed filter time of 1 ms and a scanning frequency of 10 kHz. When a missing or too short period is detected, control is switched off until at least 2 periods are detected correctly, and the status flag is set accordingly. Control is offset by 2 ms from the negative half-wave until the next zero crossover is detected correctly or another error occurs. This is normally at least one complete wave.

Monitoring is activated at the first zero crossover after being switched on.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("ZeroCrossingInput" through "ZeroCrossingStatus") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 17	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	ZeroCrossingInput[1)]	0	Signal during the negative half-wave
		1	Signal during the positive half-wave
1 - 3	Reserved	0	
4	ZeroCrossingStatus	0	No error
		1	Zero crossover failed
5 - 7	Reserved	0	

1) Value is valid if no error has occurred (ZeroCrossingStatus= 0)

4.15.5.10.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Digital mode	100 µs
Digital and analog mode	150 µs

4.15.5.10.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Digital mode	100 µs
Digital and analog mode	150 µs

4.15.6 X20(c)DO2633

4.15.6.1 General information

The module is a digital output module with phase-angle control that is equipped with 2 Triac outputs using 3-line connections. The supply (L and N) is fed directly to the module.

- 2 digital outputs
- Outputs with integrated snubber circuit
- Outputs with 12 to 240 VAC
- L switching
- Zero-crossing detection
- Phase-angle control
- Open-circuit detection for each channel
- Negative half-waves can be switched off
- 50 Hz or 60 Hz
- 3-wire connections
- 240 V coding
- OSP mode
- Frequency mode

Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.15.6.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.6.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO2633	X20 digital output module, 2 triac outputs, 12 to 240 VAC, 2 A, L switching, phase angle control, 240 V keyed	
X20cDO2633	X20 digital output module, coated, 2 triac outputs, 12 to 240 VAC, 2 A, L switching, phase angle control, 240 V keyed	
	Required accessories	
	Bus modules	
X20BM32	X20 bus module for double-width modules, 240 VAC keyed, internal I/O supply continuous	
X20cBM32	X20 bus module, coated, for double-width modules, 240 VAC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 302: X20DO2633, X20cDO2633 - Order data

4.15.6.4 Technical data

Product ID	X20DO2633	X20cDO2633
Short description		
I/O module	2 digital outputs 12 to 240 VAC for 3-wire connections	
General information		
B&R ID code	0xAC39	0xE680
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software	
Power consumption		
Bus	0.6 W	
Internal I/O	-	
External I/O	-	
Additional power dissipation caused by the actuators (resistive) [W] [1]	+6 W	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
Digital outputs		
Design	Triac	
Wiring	L switching	
Nominal voltage	12 to 240 VAC	
Max. voltage	264 VAC	
Rated frequency	47 to 63 Hz	
Nominal output current	2 A	
Total nominal current	4 A	
Maximum current		
Output current	2.5 A	
Summation current	5 A	
Connection type	3-wire connections	
Zero-crossing detection	Yes	
Minimum holding current I_H	15 mA	
Leakage current	Max. 2 mA at 240 V and 50 Hz Max. 2.4 mA at 240 V and 60 Hz	
Residual voltage (on-state voltage)	1.5 V	
Phase-angle control		
Area	5 to 95%	
Resolution	1%	
Accuracy (60 to 240 VAC)	<100 µs	
Voltage monitoring L - N	Yes	
Additional functions	Open line detection	
Overvoltage protection between L and N	Yes, Varistor	
Isolation voltage		
Terminal block - Bus	Tested at 2300 VAC (Rev. <E0 1500 VAC)	Tested at 1500 VAC
Terminal block - 24 V	Tested at 2300 VAC (Rev. <E0 2000 VAC)	Tested at 2000 VAC
Terminal block - PE	Tested at 2300 VAC (Rev. <E0 1500 VAC)	Tested at 1500 VAC
Protective circuit		
External	See section "External fuses"	
Internal	Snubber circuit (RC element) and varistor	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 303: X20DO2633, X20cDO2633 - Technical data

Product ID	X20DO2633	X20cDO2633
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM32 bus module separately	Order 1x X20TB32 terminal block separately Order 1x X20cBM32 bus module separately
Spacing	25 $^{+0.2}$ mm	

Table 303: X20DO2633, X20cDO2633 - Technical data

1) Number of outputs x residual voltage (on-state voltage) x nominal output current (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.15.6.5 Status LEDs

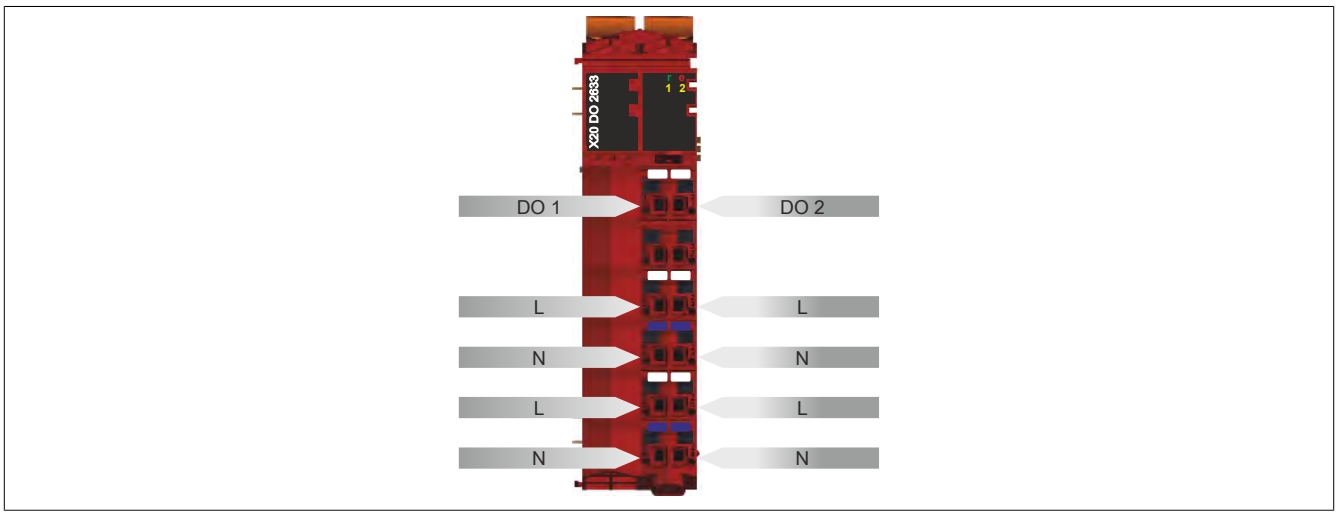
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Zero cross-over signal has dropped out
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Orange		Control status of the corresponding digital output

4.15.6.6 Pinout

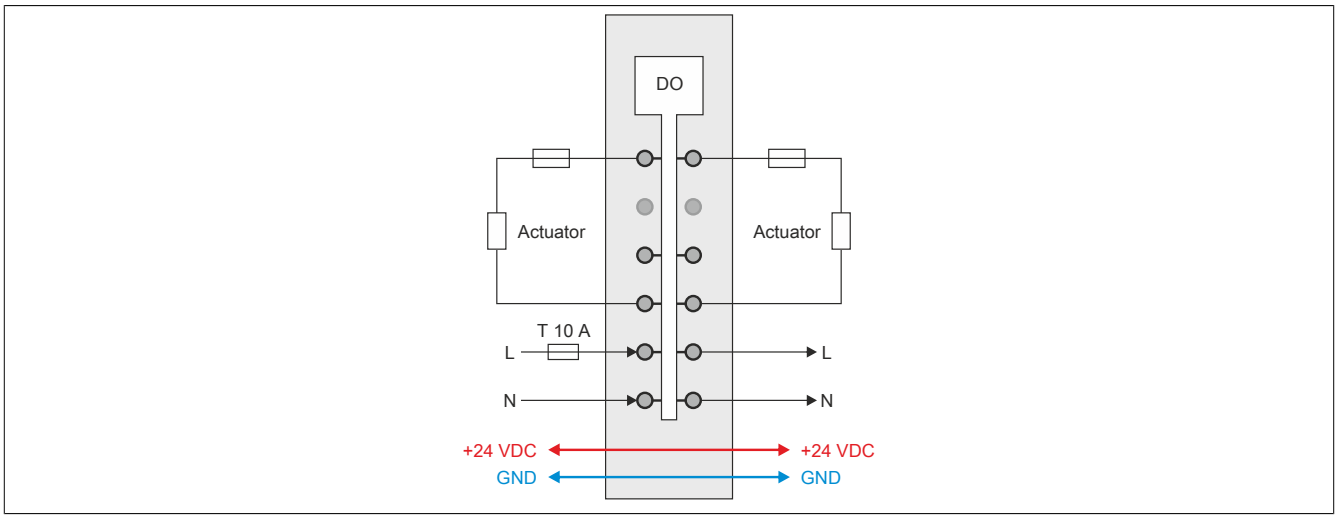
The following points must be taken into consideration when wiring the module:

- For thermal reasons, wires with a cross-section ≥1.5 mm² must be used to wire the module.
- The neutral return lines for the outputs must be wired to the terminal block separately for each channel and must not be bypassed in the field.
- A line filter must be used for the 240 V supply that provides ≥40 dB attenuation at 150 kHz and works up to 5 MHz.

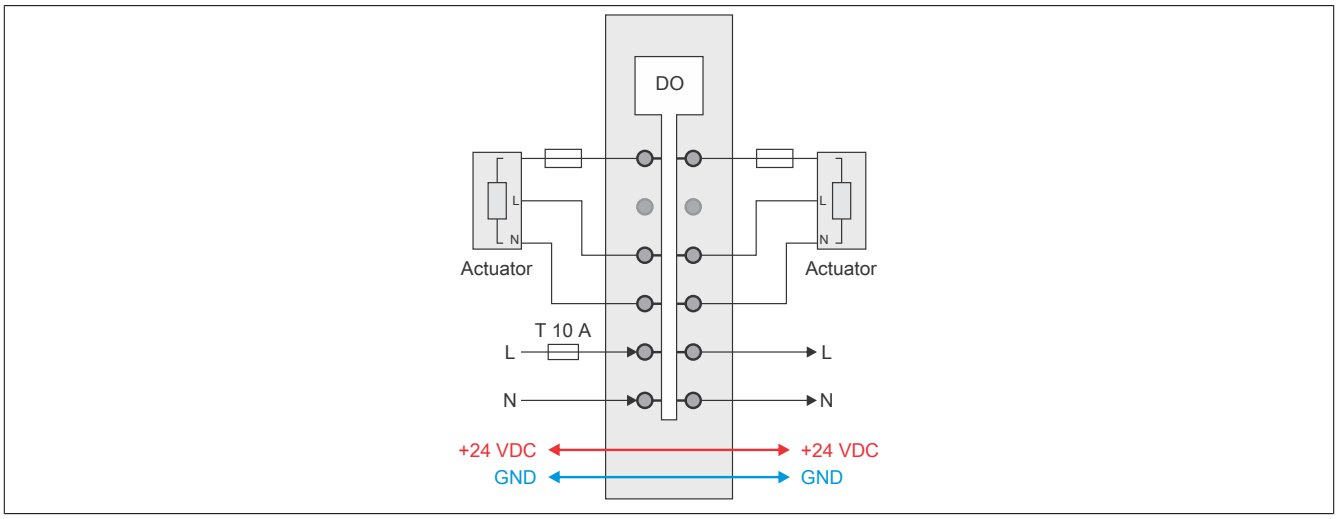


4.15.6.7 Connection example

2-wire connections



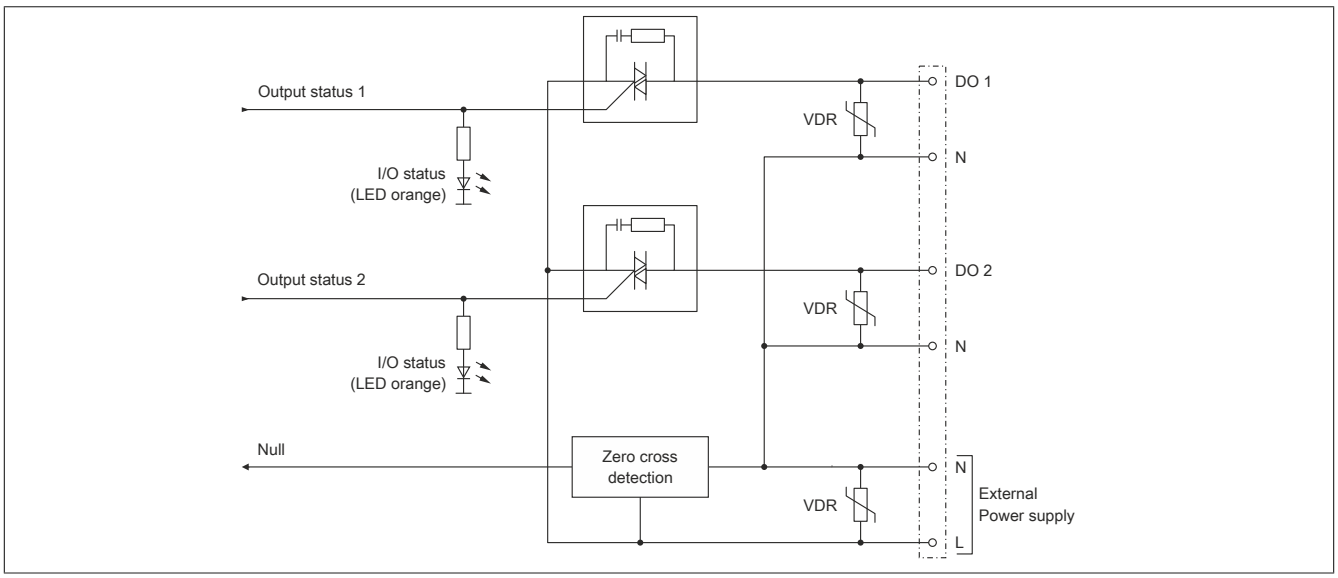
3-wire connections



4.15.6.8 OSP hardware requirements

In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.6.9 Output circuit diagram



4.15.6.10 External fuses

The following protective circuit must be used for safe operation:

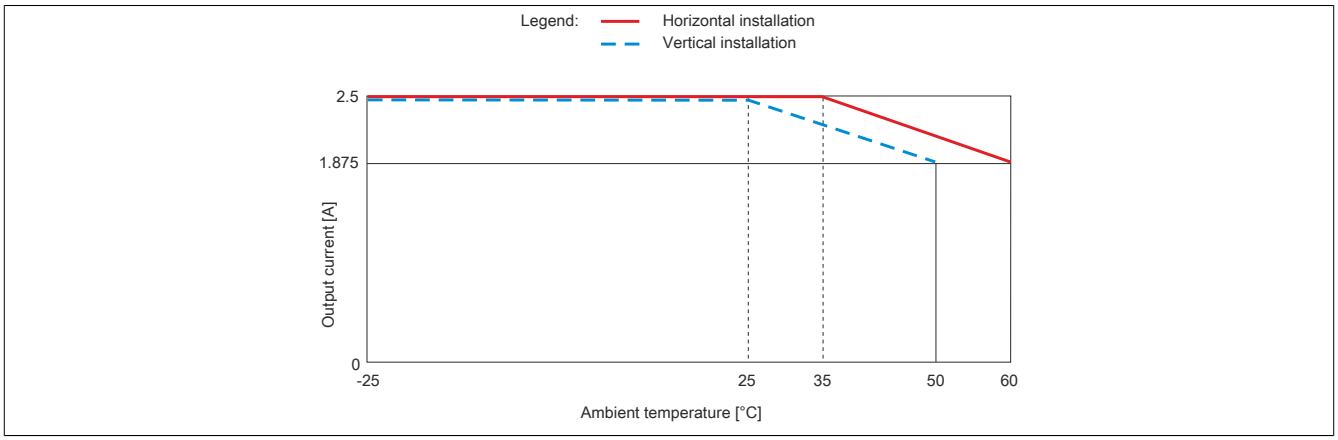
	Protective circuit	Value
For the supply lines	Fuse	T 10 A
For the outputs	Fuse	Melting integral $I^2t \leq 78\ A^2s$ when tp = 10 ms
With an inductive load	Varistor[1)]	e.g. varistor with 275 V_{RMS} at 240 VAC
For the supply voltage	Line filter[2)]	Attenuation ≥40 dB at 150 kHz, effective range up to 5 MHz

1) See also section 4.15.6.14 "Operation with inductive loads" on page 1379

2) Meeting the limit values specified in the standards EN 61131, EN 55011 and EN 55022 (each Class A) requires installation of a line filter in the 240 V supply line. Line filters such as the Schaffner FN 2412-8-44 can be used.
If periodic ground transients occur on the supply lines (as can occur with upstream inverters), it is necessary to use an asymmetric filter that keeps these types of changes in potential below a few volts (e.g. "Sinus Plus" from Schaffner) in addition to the symmetric filter.

4.15.6.11 Derating

The derating listed below must be applied for the current:



4.15.6.12 Operating principle

The digital output module was designed for phase control of resistive and and inductive loads. The triac outputs do not have short circuit protection. The integrated open-circuit detection makes it possible to recognize defects on the load or the cabling (see 4.15.6.13 "Open line detection" on page 1378).

The module is equipped with internal zero-crossing detection. Zero-crossing detection is the basis for a software PLL that generates 200 times the zero-crossing frequency. The output signal of the PLL is the base timer for the PWM outputs in both digital and analog mode.

Upon detection of lost periods or periods that are too short, control to the outputs is cut until the PLL is tuned correctly. The tuning procedure can take several seconds. In addition, the "ZeroCrossingStatus" bit is set and the error LED enabled (valid frequency range for the supply is 45 to 65 Hz).

Information:

The jitter of the output signals generated by the PLL and communication can reach 0.5%.

4.15.6.13 Open line detection

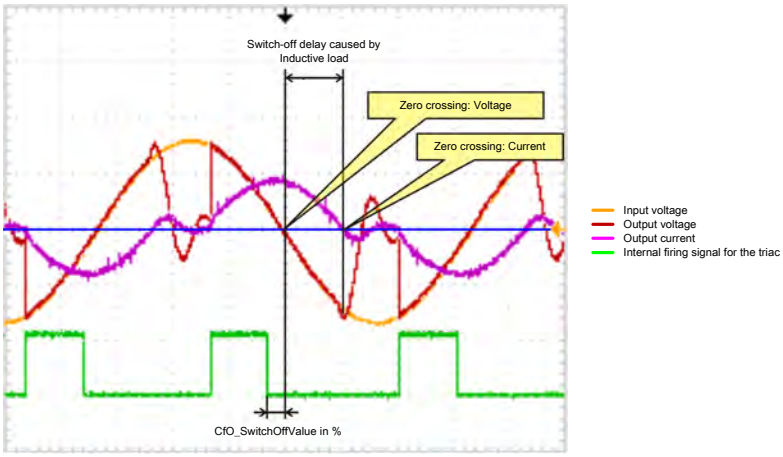
The module is equipped with open-circuit detection. Note that open-circuit detection only works when the output is enabled. An open-circuit will not be detected if the output is turned off.

In addition, open-circuit detection is restricted or doesn't work at all for inductive loads. This depends on the inductance of the load and should be determined beforehand, if necessary.

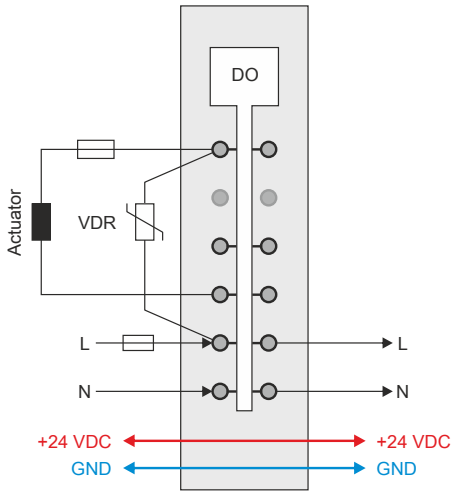
4.15.6.14 Operation with inductive loads

As inherent to its functional principal, the triac output is cleared when the current crosses zero. Because zero crossing for current is delayed with inductive loads, it is possible that the triac will be fired again even though it is not completely cleared at higher output values (between 50 and 100% depending on the inductance of the load). In this case, a full-wave is output. This causes the available control range (0 to 95%) to be changed.

For open line detection (LowCurrentStatus), a pause in control is required where the triac is not permitted to be fired. The full wave that is created with inductive loads causes open line detection to be triggered even though the load on the output is sufficient.
This behavior can be used to detect the full wave and properly adjust the control range (Example: If open line detection is triggered at a control value of 70%, that means that 0 to **70%** corresponds to 0 to **100%** output).



With inductive loads, a suitable varistor must be provided between the output DO x and the phase L (e.g. a varistor with 275 V_{RMS} at 240 VAC).



4.15.6.15 Register description

4.15.6.15.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.6.15.2 Function model 0 - Standard and Function model 2 - Frequency mode

The only difference between function model 2 and function model 0 is the possibility of generating half-wave patterns in various frequencies. Register 18 "CfO_Frequency" is an additional register for this.

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General						
4	AnalogOutput01	USINT			•	
6	AnalogOutput02	USINT			•	
18	CfO-Frequency	UINT				•
20	CfO_SwitchOffValue1	USINT				•
22	CfO_SwitchOffValue2	USINT				•
28	CfO_OutputConfig	USINT				•
29	CfO_OutputTolerance	USINT				•
Communication						
2	DigitalOutput	USINT			•	
	DigitalOutput01	Bit 0				
	DigitalOutput02	Bit 2				
30	StatusInput01	USINT	•			
	LowCurrentStatus1	Bit 0				
	LowCurrentStatus2	Bit 1				
	ZeroCrossingInput	Bit 4				
	ZeroCrossingStatus	Bit 7				

4.15.6.15.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General						
4	AnalogOutput01	USINT			•	
6	AnalogOutput02	USINT			•	
20	CfO_SwitchOffValue1	USINT				•
22	CfO_SwitchOffValue2	USINT				•
28	CfO_OutputConfig	USINT				•
29	CfO_OutputTolerance	USINT				•
Configuration - OSP						
34	Activating the OSP output in the module	USINT			•	
	OSPValid	Bit 0				
32	CfgOSPMode	USINT				•
36	CfgOSPValue	USINT				•
38	CfgOSPValue01	USINT				•
40	CfgOSPValue02	USINT				•
Communication						
2	Switching state of digital outputs 1 to 2	USINT			•	
	DigitalOutput01	Bit 0				
	DigitalOutput02	Bit 1				
30	Status of the outputs	USINT	•			
	LowCurrentStatus1	Bit 0				
	LowCurrentStatus2	Bit 1				
	ZeroCrossingInput	Bit 4				
	ZeroCrossingStatus	Bit 7				

4.15.6.15.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General							
4	0	AnalogOutput01	USINT			•	
6	2	AnalogOutput02	USINT			•	
20	-	CfO_SwitchOffValue1	USINT				•
22	-	CfO_SwitchOffValue2	USINT				•
28	-	CfO_OutputConfig	USINT				•
29	-	CfO_OutputTolerance	USINT				•
Communication							
30	0	Status of the outputs	USINT	•			
		LowCurrentStatus1	Bit 0				
		LowCurrentStatus2	Bit 1				
		ZeroCrossingInput	Bit 4				
		ZeroCrossingStatus	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.15.6.15.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.15.6.15.5 General information

The digital output module was designed for phase control of resistive and inductive loads. The triac outputs do not have short circuit protection, but have open line detection that can be used to find defects in the consumer or the wiring.

The module is equipped with internal zero-crossing detection. Zero crossing detection is the basis for a software PLL that generates 200 times the zero crossing frequency. The output signal of the PLL is the base timer for the 2 PWM outputs in both digital and analog mode.

Upon detection of lost periods or periods that are too short, control of the outputs is cut until the PLL is tuned correctly (can take several seconds). In addition, the "ZeroCrossingStatus" bit is set and the Error LED is enabled (valid frequency range for the supply is 45 to 65 Hz).

Information:

The jitter of the output signals generated by the PLL and communication can reach 0.5%.

4.15.6.15.6 Digital outputs

The output state of the outputs defined as digital is transferred to the output ports of the control switch in sync with the connected power mains. The switch-on state is applied when the voltage crosses zero on the positive half-wave and the switch-off state at the zero crossing for current in each half wave.

4.15.6.15.6.1 Switching state of digital outputs 1 to 2

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput02

This register is used to store the switching state of digital outputs 1 to 2.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 3	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
1	DigitalOutput02	0	Digital output 02 reset
		1	Digital output 02 set

Information:

The states in these registers are only applied when the channels are set to DIGITAL in "Configuration of the output channels".

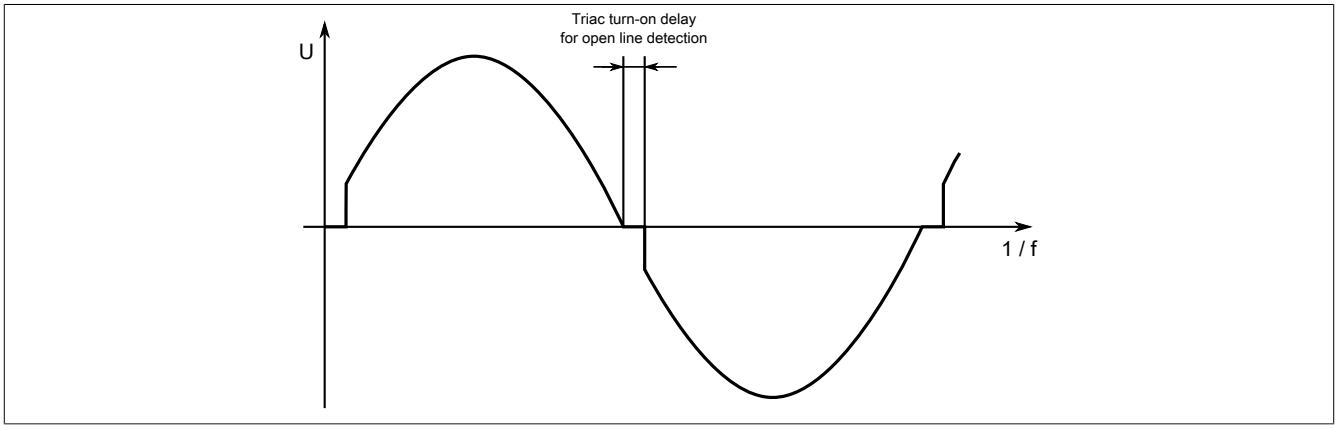
When using the setting "packed outputs" ALL channels must be set to DIGITAL. Mixed operation is not possible.

4.15.6.15.7 Analog outputs

The output value of the outputs defined as analog outputs (unit percent) is switched through to the control ports in sync with power mains. The analog value is output to the TRIAC control port in the range between (output value > SwitchOffValue) and (output value <= 95%) with a resolution of 1%.

A short triac turn-on delay is required for open line detection. Therefore even with output values >= 96%, there is a small pause in control.

Changes to the output value are applied at the next positive half-wave



4.15.6.15.7.1 Commutation angle for analog outputs 1 - 2

Name:
AnalogOutput01 to AnalogOutput02

These registers are used to set the commutation angle for phase angle control.

Values between 0 and 100 correspond to the output value for the respective channel in percent. Values above 100 correspond to 100%.

Data type	Value
USINT	0 to 100

Information:

The commutation angle for phase angle control set in these registers are only applied when the channels are set to ANALOG in "Configuration of the output channels".

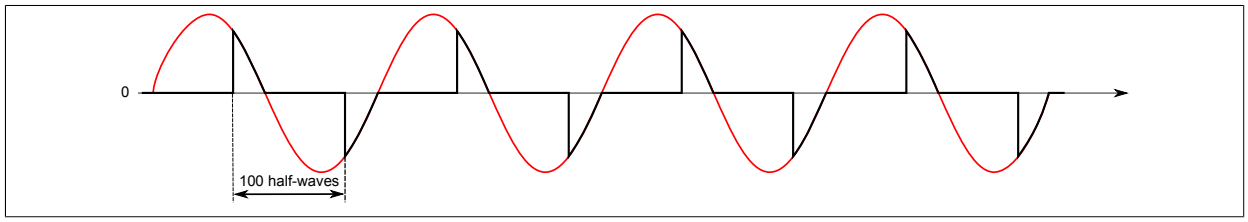
4.15.6.15.8 Output configuration

4.15.6.15.8.1 Configuring the half-wave pattern

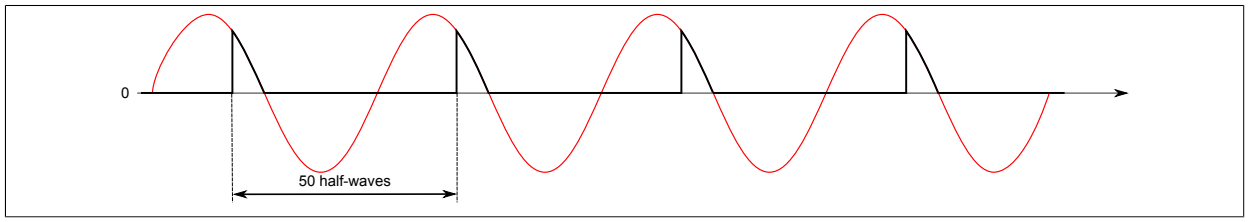
Name:
CfO_Frequency

This register can only be used in function model 2 - Frequency mode and makes it possible to configure the output of half-wave patterns in various frequencies. The commutation angle of the outputs is not affected by this. The following frequency patterns can be configured:

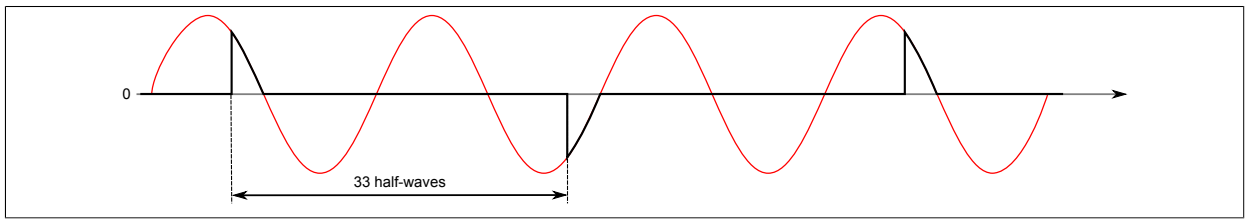
- 100 half-waves



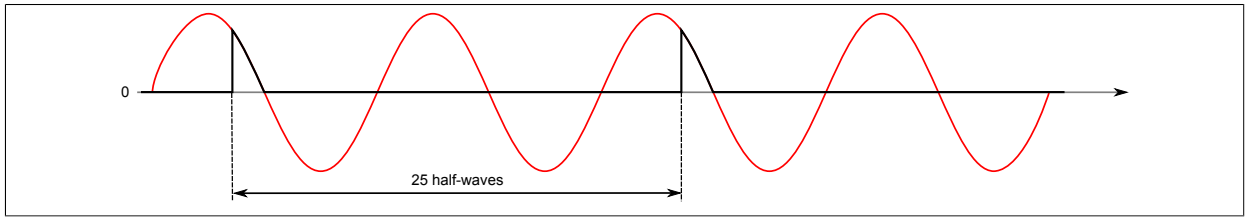
- 50 half-waves



- 33 half-waves



- 25 half-waves



With multichannel operation, the second channels should be operated with delayed half-waves in order to ensure that the load is placed evenly on the module.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Channel 1	0000	100 half-waves/second
		0001	50 half-waves/second
		0010	25 half-waves/second
		0011	33 half-waves/second
		0101	50 half-waves/second delayed by 1 half-wave
		0110	25 half-waves/second delayed by 2 half-waves
		0111	33 half-waves/second delayed by 1 half-wave
4 - 7	Channel 2	0000 to 0111	See channel 1
8 - 15	Reserved	-	

Information:

This function is available beginning with firmware version 940. This can be included beginning with hardware variant 8.

4.15.6.15.8.2 Setting the switch-off time

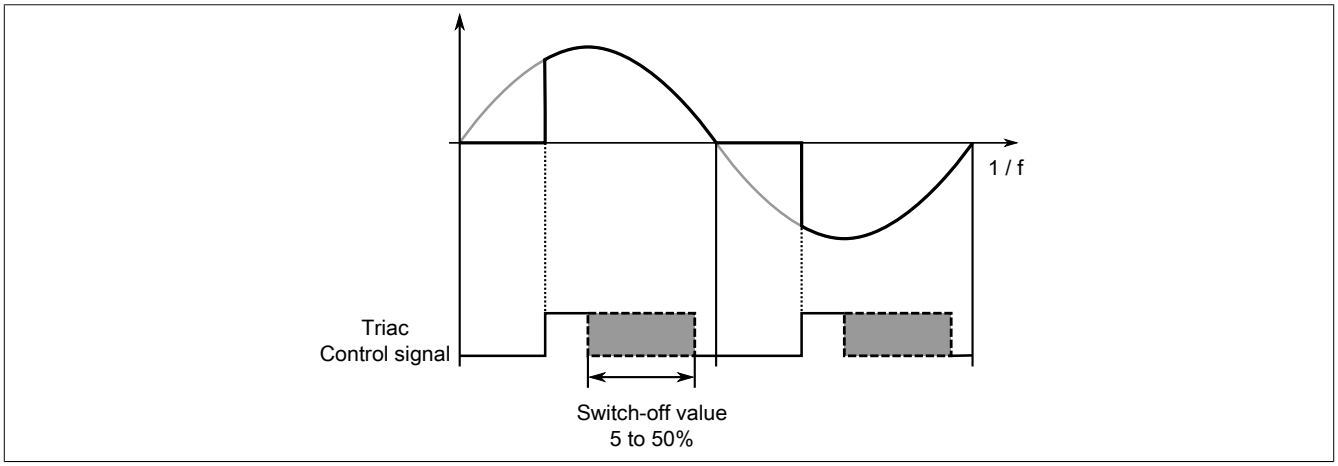
Name:
CfO_SwitchOffValue1 and CfO_SwitchOffValue2

This register defines how far in front of the zero cross-over the internal control signal for the TRIAC is switched off. Increasing this value may be necessary in order to prevent unwanted firing of the TRIAC in the event of a slight disturbance in the mains frequency.

With smaller loads, it is important to ensure that this switch off value is not set to large (too early) to prevent switching off prematurely.

The triac can of course only be fired before the set switch-off time.

"SwitchOffValue" in the AS I/O configuration.



Data type	Value	Description
USINT	5 to 50	Switch-off time in %

4.15.6.15.8.3 Configuration of the output channels

Name:
CfO_OutputConfig

The configuration of the output channels are stored in this register.

"Output type digital/analog" and "Output type full/half wave" in the AS I/O configuration

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel 1: Digital / Analog output	0	Output channel 1 is defined as a digital output. The output status is defined using bit 0 in the DigitalOutput 1 - 2 register.
		1	Output channel 1 is defined as an analog output. The output status is defined using the AnalogOutput01 register.
1	Channel 2: Digital / Analog output	0	Output channel 2 is defined as a digital output. The output status is defined using bit 0 in the DigitalOutput 1 - 2 register.
		1	Output channel 2 is defined as an analog output. The output status is defined using the AnalogOutput02 register.
2 - 3	Reserved	-	
4	Channel 1: Full-wave / half-wave control[1)]	0	Full-wave control on output channel 1
		1	Negative half-wave on output channel 1 is suppressed.
5	Channel 2: Full-wave / half-wave control[1)]	0	Full-wave control on output channel 2
		1	Negative half-wave on output channel 2 is suppressed.
6 - 7	Reserved	-	

1) Not available in function model 2 - Frequency mode.

4.15.6.15.8.4 Switching behavior for zero-crossing errors

Name:
CfO_OutputTolerance

This register can be used to set the switching behavior of the trigger. After the number of zero-crossing errors configured in Bit 0 to 4, the output is switched off for at least 3 periods. This is followed by synchronization with the zero signal according to Bit 7.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 4	Trigger for Resync	0 to 30	Number of zero-crossover errors
5 - 6	Reserved	-	
7	Fast settling	0	Fast synchronization
		1	PLL synchronization

Fast synchronization

With this option, the trigger point is closed-loop controlled after each individual zero-crossover and input jitter.

- **Advantage:** Increased tolerance and faster response to deviations in mains frequency
- **Disadvantage:** Increased switch-on jitter for firing signal by zero cross signal ±100 µSec

PLL synchronization

With this option the intervals between zero cross-overs are measured and the PLL frequency is updated accordingly.

- **Advantage:** Jitter-free firing signal
- **Disadvantage:** When the output is switched off, additional measurement phases are required before it can be switched back on.

Information:

This function is available starting with Firmware version 928. This can be installed with hardware version 8 and hardware revision B4 or higher.

4.15.6.15.9 Status of the outputs

Name:
LowCurrentStatus1 through LowCurrentStatus2
ZeroCrossingInput
ZeroCrossingStatus
StatusInput01

The operating status of the outputs is mapped in this register.

In order to do determine the "LowCurrentStatus", the system checks if there is a neutral connection from the output via the consumer shortly before each triac firing.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("LowCurrentStatus1" through "ZeroCrossingStatus") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	LowCurrentStatus1	0	Current flow on activated output 1
		1	No current flow on activated output 1
1	LowCurrentStatus2	0	Current flow on activated output 2
		1	No current flow on activated output 2
2 - 3	Reserved	-	
4	ZeroCrossingInput	0	Zero cross signal during the negative half-wave
		1	Zero cross signal during the positive half-wave
5 - 6	Reserved	-	
7	ZeroCrossingStatus	0	Zero cross signal OK
		1	Zero cross signal has dropped out

4.15.6.15.10 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.6.15.10.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.6.15.10.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.6.15.10.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.6.15.10.4 Define the OSP analog output value

Name:
CfgOSPValue01 to CfgOSPValue02

This register contains the analog output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	0 to 100

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.6.15.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
All channels	250 µs

4.15.6.15.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
All channels	150 µs

4.15.7 X20DO2649

4.15.7.1 General information

The module has 2 relay outputs.

- 2 digital outputs
- Relay module for 240 VAC / 30 VDC
- 2 change over contacts
- Single-channel isolated outputs

Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.15.7.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO2649	X20 digital output module, 2 relays, changeover contacts, 240 VAC / 5 A, 24 VDC / 5 A	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 304: X20DO2649 - Order data

4.15.7.3 Technical data

Product ID	X20DO2649
Short description	
I/O module	2 digital outputs 30 VDC / 240 VAC, outputs are single-channel isolated
General information	
B&R ID code	0x20DA
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED
Power consumption	
Bus	0.45 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+2.5
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes

Table 305: X20DO2649 - Technical data

Product ID	X20DO2649
Digital outputs	
Design	Relay / Changeover contact Channels are single-channel isolated
Nominal voltage	30 VDC / 240 VAC
Max. voltage	264 VAC
Switching voltage	Max. 110 VDC / 264 VAC
Rated frequency	DC / 45 to 63 Hz
Nominal output current	5 A at 30 VDC / 5 A at 240 VAC
Total nominal current	10 A at 30 VDC / 10 A at 240 VAC
Actuator supply	External
Starting current	Max. 6 A (per channel)
Contact resistance	50 mΩ
Switching delay	
0 -> 1	≤10 ms
1 -> 0	≤10 ms
Isolation voltage	
Contact - Contact	Tested at 1000 VAC
Contact - Coil	Tested at 4000 VAC
Service life	
Electrical [3]	Min. 60 x 10^3 ops. (NC) at 6 A Min. 30 x 30^3 ops. (NO) at 6 A
Mechanical	Min. 10 x 10^6 ops.
Switching capacity	
Minimum	10 mA / 5 VDC
Maximum	180 W / 1500 VA
Protective circuit	
Internal	None
External	
AC	RC combination or VDR
DC	Inverse diode, RC combination or VDR
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 305: X20DO2649 - Technical data

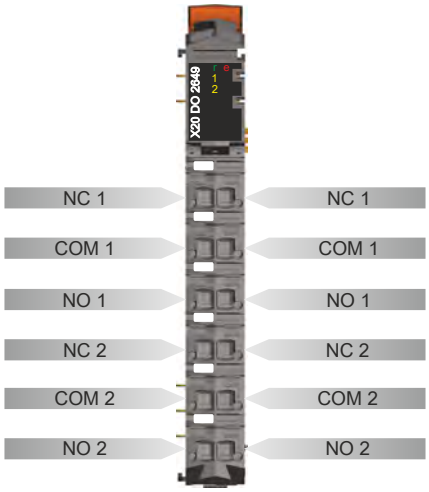
1) Number of outputs x Contact resistance x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) With a resistive load. See also section "Electrical service life"

4.15.7.4 Status LEDs

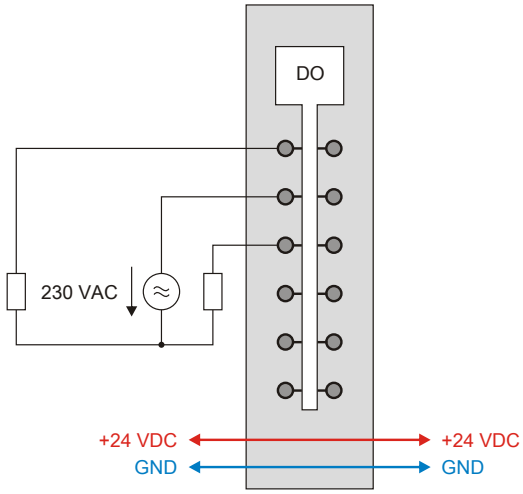
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Orange		Output status of the corresponding digital output

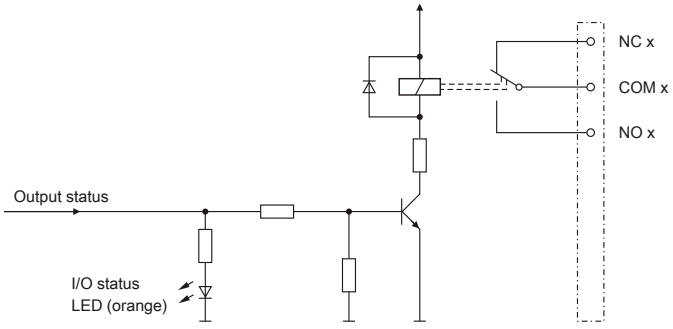
4.15.7.5 Pinout



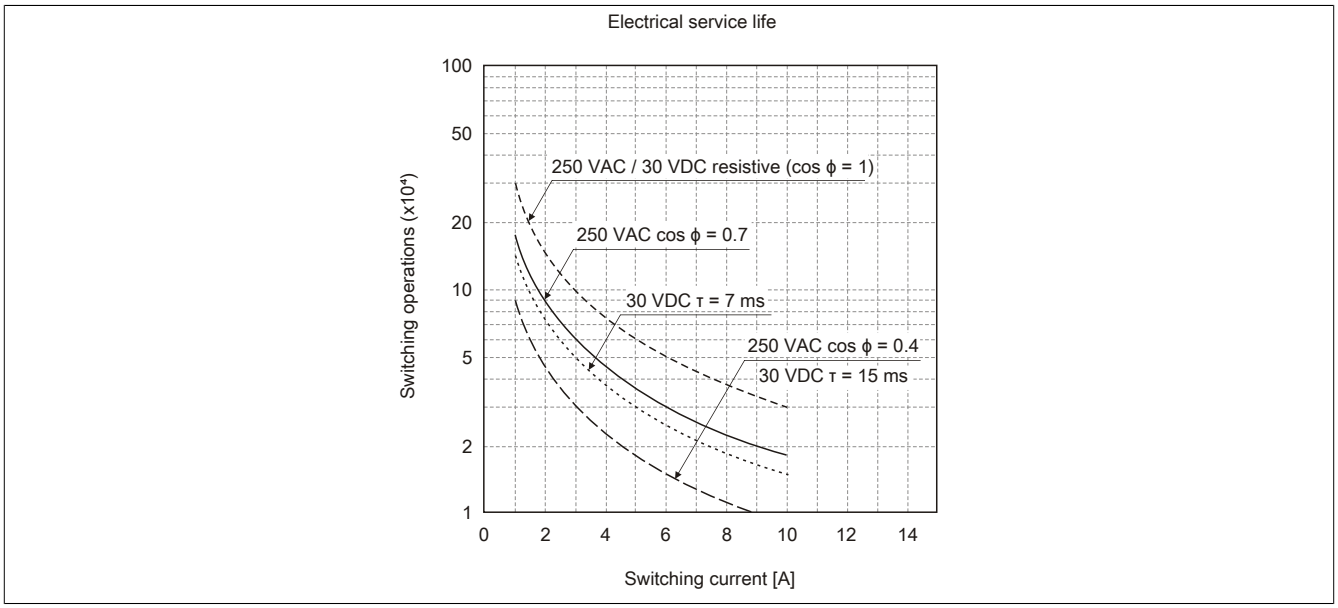
4.15.7.6 Connection example



4.15.7.7 Output circuit diagram



4.15.7.8 Electrical service life



4.15.7.9 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the maximal current per channel is limited to 4 A and maximal total current is limited to 8 A.

4.15.7.10 Register description

4.15.7.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.7.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.7.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				

1) The offset specifies where the register is within the CAN object.

4.15.7.10.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.7.10.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.7.10.4.1 Switching state of digital outputs 1 to 2

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput02

This register is used to store the switching state of digital outputs 1 to 2.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 3	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
1	DigitalOutput02	0	Digital output 02 reset
		1	Digital output 02 set

4.15.7.10.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.7.10.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.8 X20DO4321

4.15.8.1 General information

The module is equipped with 4 outputs for 3-wire connections.

- 4 digital outputs
- Sink connection
- 3-wire connections
- 24 VDC and GND for actuator supply
- Integrated output protection
- OSP mode

4.15.8.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4321	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, sink, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 306: X20DO4321 - Order data

4.15.8.3 Technical data

Product ID	X20DO4321
Short description	
I/O module	4 digital outputs 24 VDC for 3-wire connections
General information	
B&R ID code	0x22B4
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.16 W
Internal I/O	0.49 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+0.12
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Design	FET negative switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	2 A
Connection type	3-wire connections
Output circuit	Sink
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")

Table 307: X20DO4321 - Technical data

Product ID	X20DO4321
Actuator supply	0.5 A in total for output-independent actuator supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	75 µA
$R_{DS(on)}$	120 mΩ
Peak short circuit current	<7 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load	Max. 500 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 50 VDC
Isolation voltage between channel and bus	500 V_{eff}
Actuator supply	
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 V
Short circuit protection	Yes
Power consumption	
Actuator supply	Max. 12 W [3]
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 307: X20DO4321 - Technical data

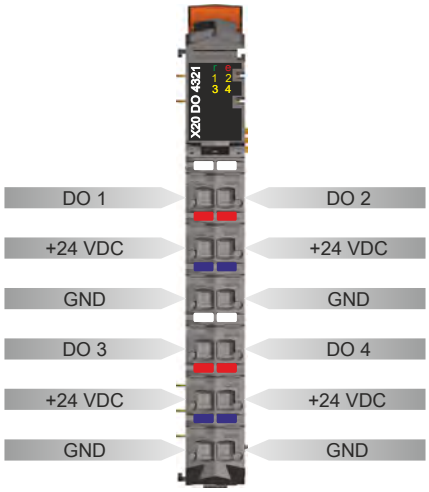
1) Number of outputs x $R_{DS(on)}$ x Nominal output current² (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.15.8.4 Status LEDs

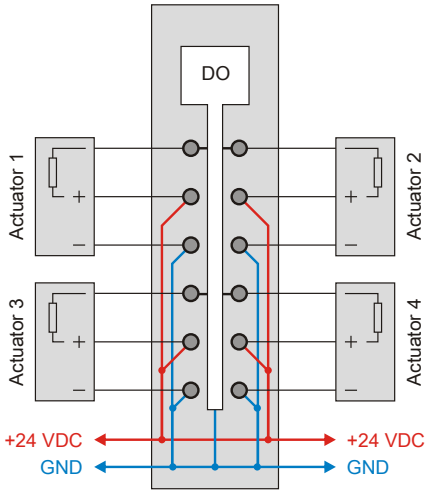
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	Reset mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Output status of the corresponding digital output

4.15.8.5 Pinout



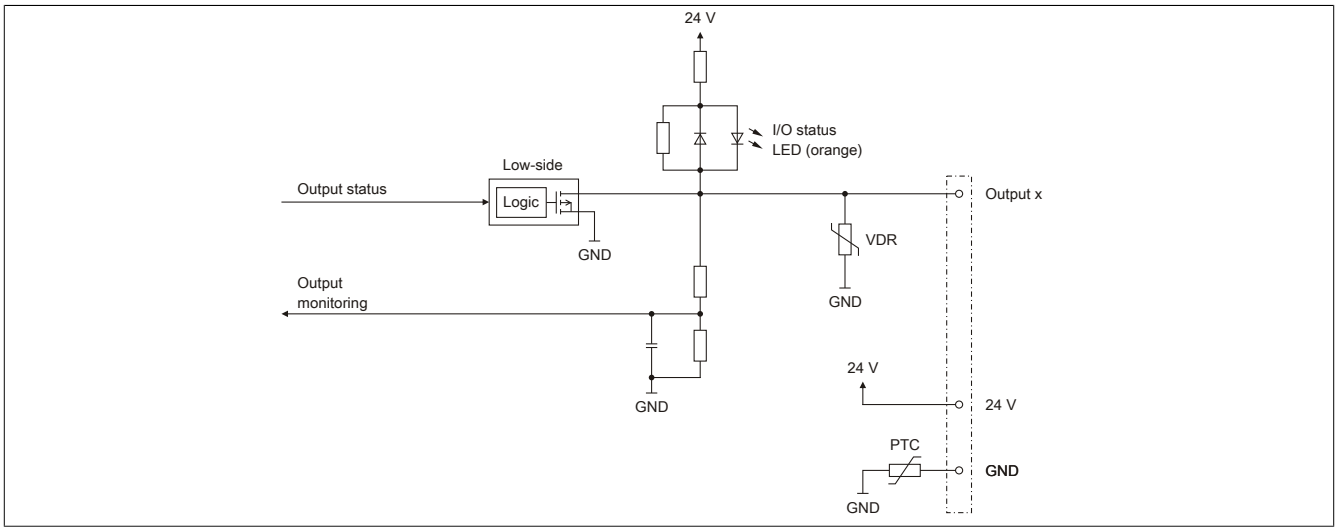
4.15.8.6 Connection example



4.15.8.7 OSP hardware requirements

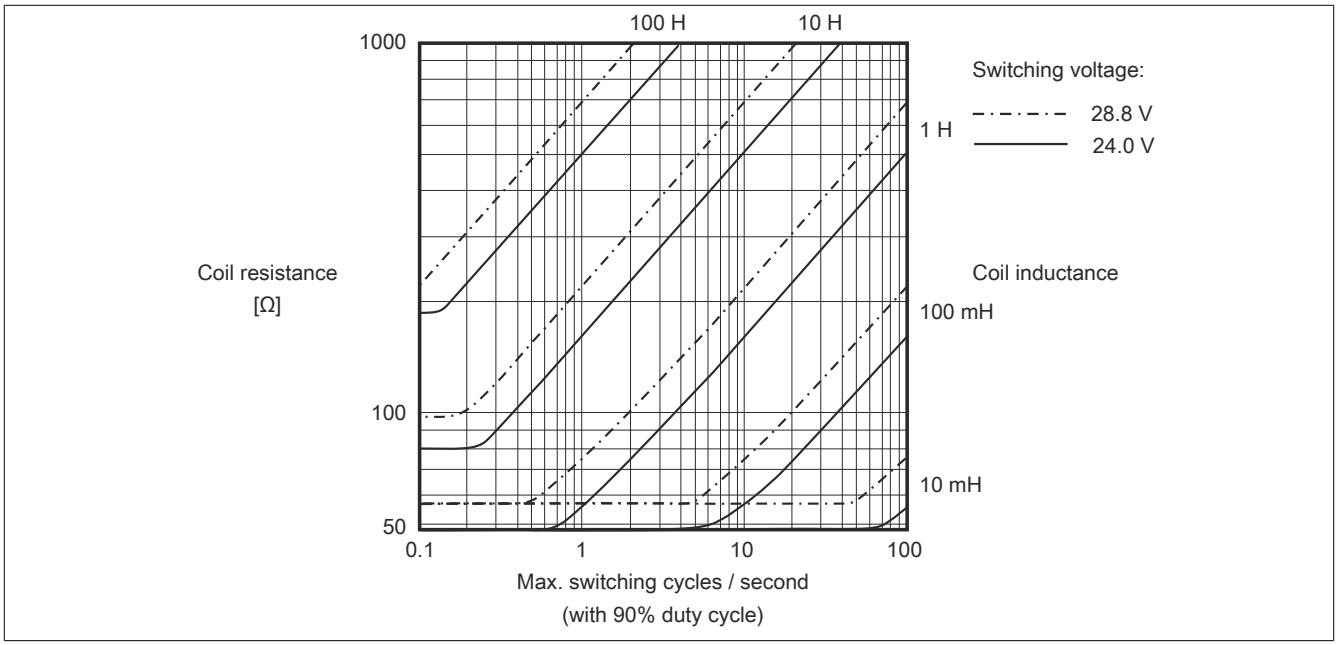
In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.8.8 Output circuit diagram



4.15.8.9 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.8.10 Register description

4.15.8.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.8.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.8.10.3 Function model 1 - OSP

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	1	Status of digital outputs 1 to 4	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				
34	1	Activating the OSP output in the module	USINT			•	
		OSPValid	Bit 0				
32	-	CfgOSPMode	USINT				•
36	-	CfgOSPValue	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.8.10.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	-	Status of digital outputs 1 to 4	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.15.8.10.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.8.10.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.8.10.5.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

4.15.8.10.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.8.10.6.1 Status of digital outputs 1 to 4

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput04

The status of digital outputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit		Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
3	StatusDigitalOutput04	0	Channel 04: No error
		1	Channel 04: Short circuit or overload

4.15.8.10.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.8.10.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.8.10.7.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.8.10.7.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.8.10.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.8.10.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.9 X20(c)DO4322

4.15.9.1 General information

The module is equipped with 4 outputs for 3-wire connections.

- 4 digital outputs
- Source connection
- 3-wire connections
- 24 VDC and GND for actuator supply
- Integrated output protection
- OSP mode

4.15.9.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.9.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4322	X20 digital output module, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections	
X20cDO4322	X20 digital output module, coated, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 308: X20DO4322, X20cDO4322 - Order data

4.15.9.4 Technical data

Product ID	X20DO4322	X20cDO4322
Short description		
I/O module	4 digital outputs 24 VDC for 3-wire connections	
General information		
B&R ID code	0x1B97	0xE226
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	
Power consumption		
Bus	0.16 W	
Internal I/O	0.49 W	
Additional power dissipation caused by the actuators (resistive) [W] 1)	+0.21	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 2)	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Digital outputs		
Design	FET positive switching	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	0.5 A	
Total nominal current	2 A	
Connection type	3-wire connections	
Output circuit	Source	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")	
Actuator supply	0.5 A in total for output-independent actuator supply	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	5 µA	
$R_{DS(on)}$	210 mΩ	
Max. continuous current	6 A	
Peak short circuit current	<12 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay 3)		
0 -> 1	<300 µs	
1 -> 0	<300 µs	
Switching frequency		
Resistive load 3)	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Actuator supply		
Voltage	Module supply minus voltage drop for short circuit protection	
Voltage drop for short circuit protection at 500 mA	Max. 2 V	
Short circuit protection	Yes	
Power consumption		
Actuator supply	Max. 12 W 4)	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 309: X20DO4322, X20cDO4322 - Technical data

Product ID	X20DO4322	X20cDO4322
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 309: X20DO4322, X20cDO4322 - Technical data

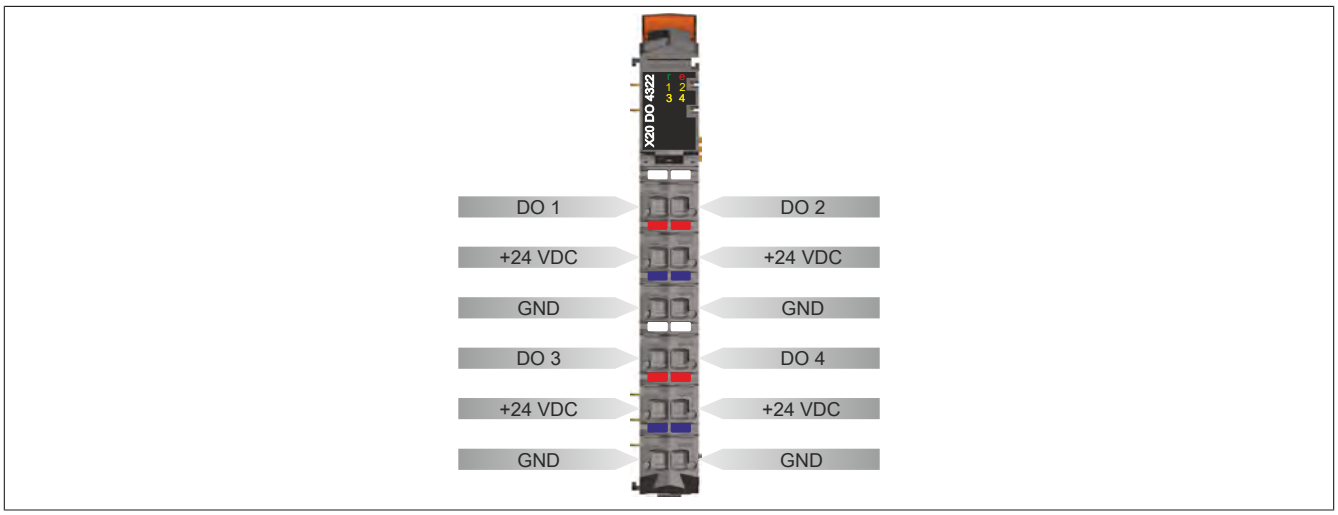
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) At loads ≤ 1 kΩ
4) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.15.9.5 Status LEDs

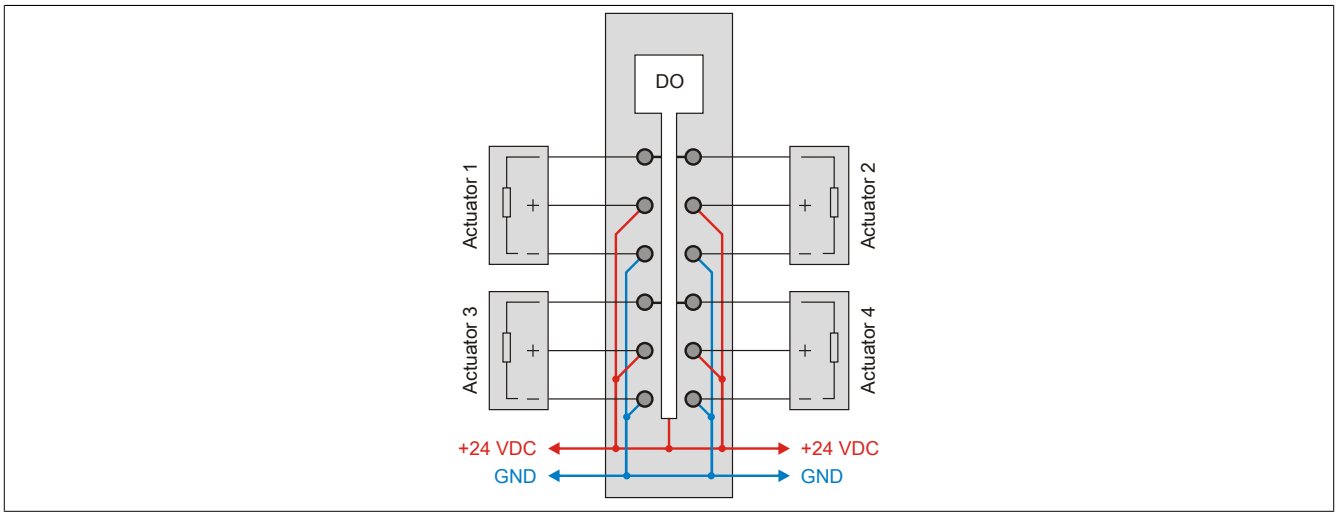
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Output status of the corresponding digital output

4.15.9.6 Pinout



4.15.9.7 Connection example



Caution!

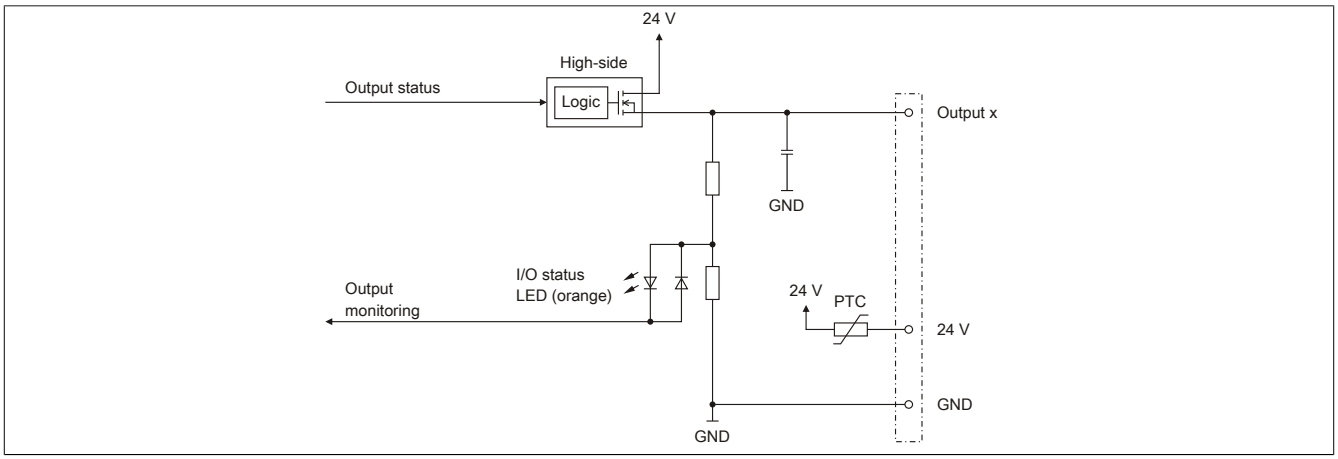
If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

Therefore sufficient cable cross sections or external safety measures must be used.

4.15.9.8 OSP hardware requirements

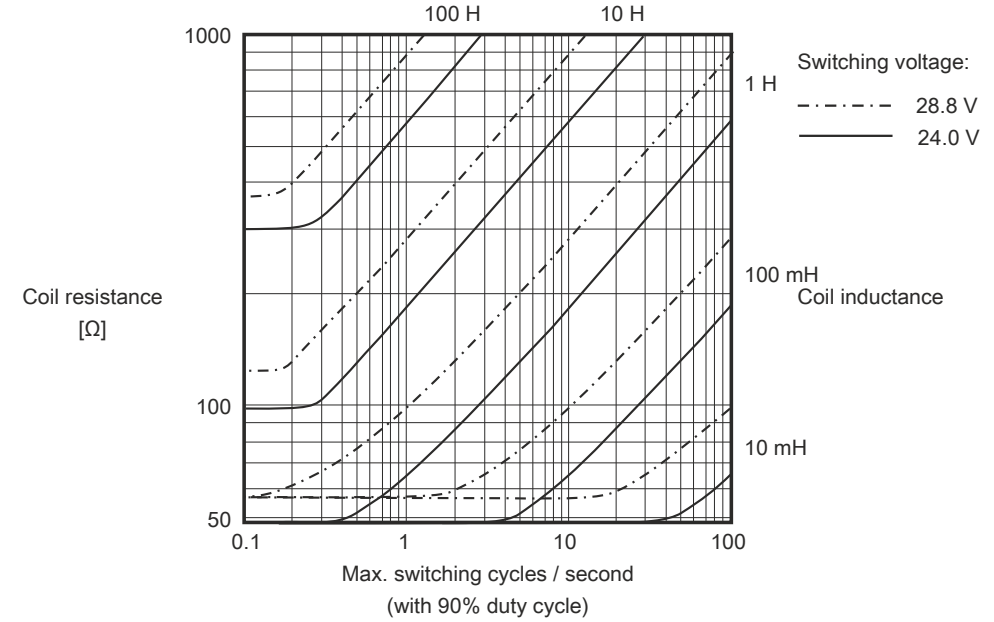
In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.9.9 Output circuit diagram



4.15.9.10 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.9.11 Register description

4.15.9.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.9.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.9.11.3 Function model 1 - OSP

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	1	Status of digital outputs 1 to 4	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				
34	1	Activating the OSP output in the module	USINT			•	
		OSPValid	Bit 0				
32	-	CfgOSPMode	USINT				•
36	-	CfgOSPValue	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.9.11.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	-	Status of digital outputs 1 to 4	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.15.9.11.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.9.11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.9.11.5.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

4.15.9.11.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.9.11.6.1 Status of digital outputs 1 to 4

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput04

The status of digital outputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit		Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
3	StatusDigitalOutput04	0	Channel 04: No error
		1	Channel 04: Short circuit or overload

4.15.9.11.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.9.11.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.9.11.7.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.9.11.7.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.9.11.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.9.11.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.10 X20DO4331

4.15.10.1 General information

The module is equipped with 4 outputs for 3-wire connections. The rated output current is 2 A.

- 4 digital outputs with 2 A
- Sink connection
- 3-wire connections
- 24 VDC and GND for actuator supply
- Integrated output protection
- OSP mode

4.15.10.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4331	X20 digital output module, 4 outputs, 24 VDC, 2 A, sink, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 310: X20DO4331 - Order data

4.15.10.3 Technical data

Product ID	X20DO4331
Short description	
I/O module	4 digital outputs 24 VDC for 3-wire connections
General information	
B&R ID code	0x22B5
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.16 W
Internal I/O	0.49 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+0.56
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Design	FET negative switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	2 A
Total nominal current	8 A
Connection type	3-wire connections
Output circuit	Sink
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")

Table 311: X20DO4331 - Technical data

Product ID	X20DO4331
Actuator supply	0.5 A in total for output-independent actuator supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	75 µA
$R_{DS(on)}$	35 mΩ
Peak short circuit current	<24 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<300 µs
1 -> 0	<500 µs
Switching frequency	
Resistive load	Max. 500 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 50 VDC
Isolation voltage between channel and bus	500 V_{eff}
Additional functions	To increase the output current, outputs can be switched in parallel
Actuator supply	
Voltage	Module supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 500 mA	Max. 2 V
Short circuit protection	Yes
Power consumption	
Actuator supply	Max. 12 W 3)
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 311: X20DO4331 - Technical data

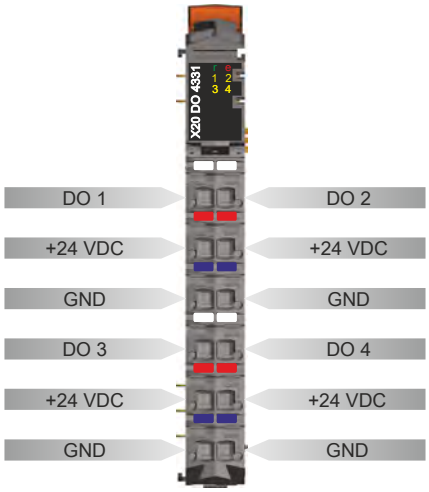
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.15.10.4 Status LEDs

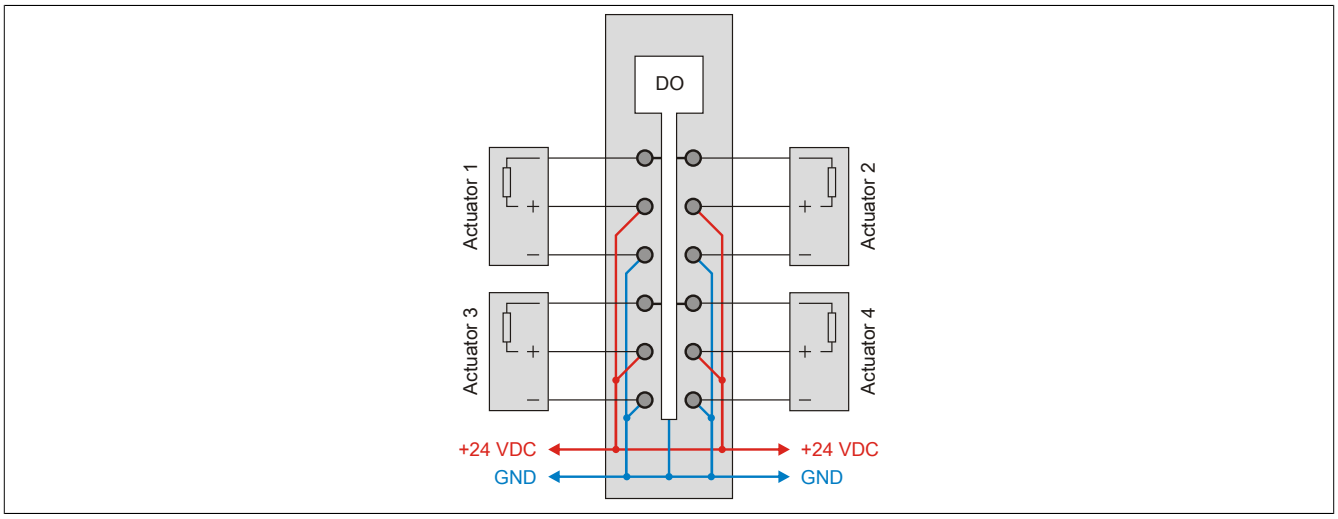
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Output status of the corresponding digital output

4.15.10.5 Pinout



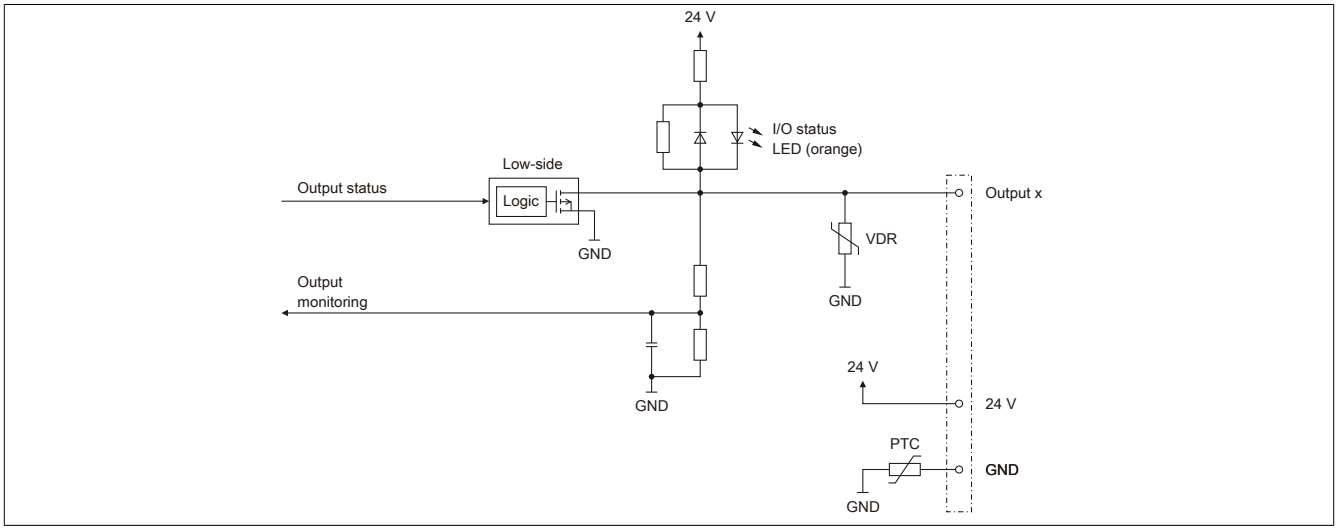
4.15.10.6 Connection example



4.15.10.7 OSP hardware requirements

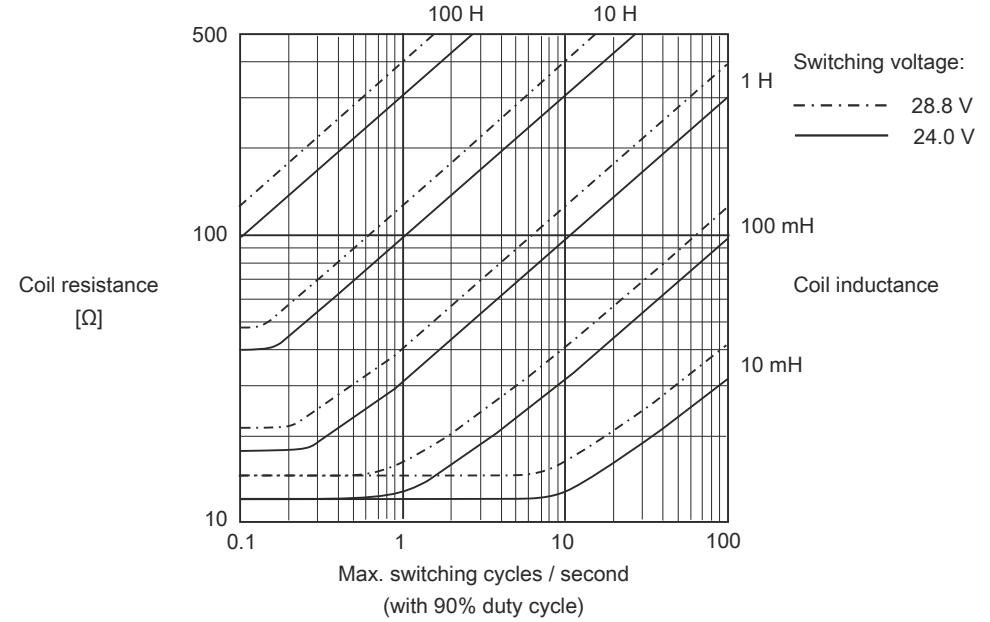
In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.10.8 Output circuit diagram

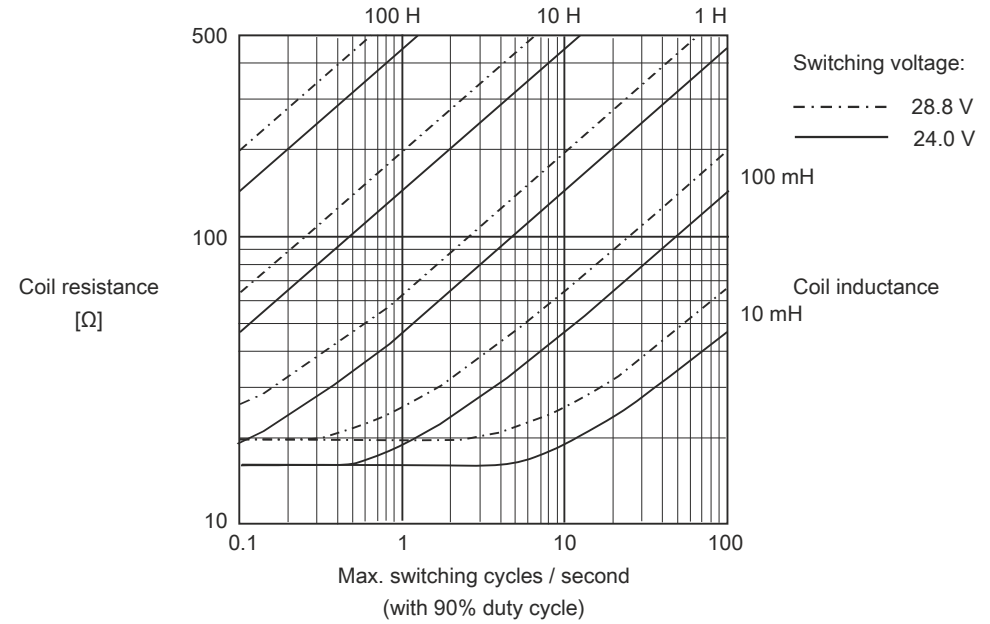


4.15.10.9 Switching inductive loads

Environmental temperature: 40°C, all outputs with the same load.



Environmental temperature: 60°C, all outputs with the same load.



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.10.10 Derating

The outputs of the X20DO4331 can handle up to 2A. To ensure optimal use of the module, it is important to assign the channels properly, and to keep in mind a potential derating.

The following table provides an overview of the number of fully used channels, the resulting best distribution, and a potential derating.

Number of channels using 2A	Division	Derating
1	Any	No
2	Possible divisions: 1, 3 2, 4	No
3	Possible divisions: 1, 2, 4 1, 3, 4	No
4	1 - 4	All channels

Table 312: Operation with 2 A

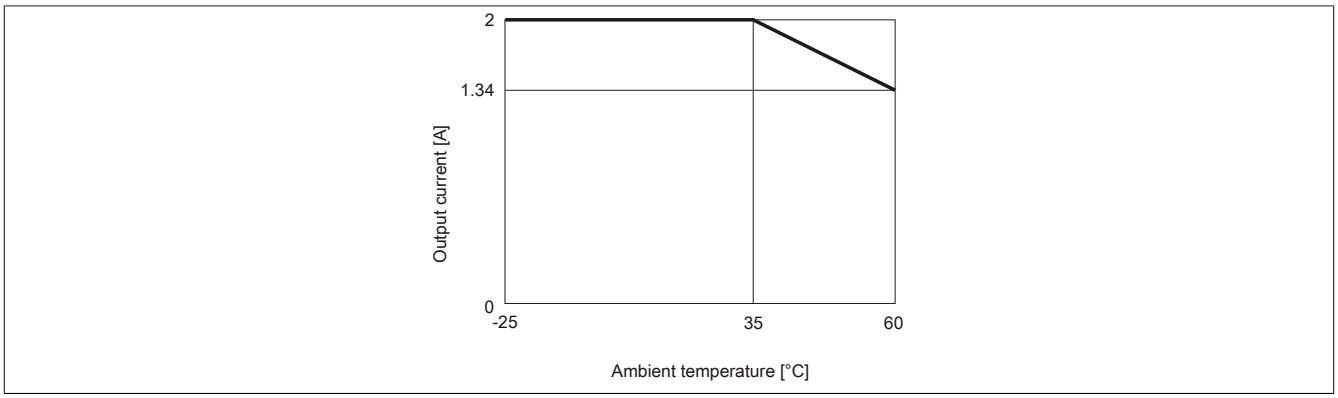


Figure 239: Derating when 4 channels are operated with 2 A

Modules next to the X20DO4331 can have a maximum power consumption of 1.5 W.

4.15.10.11 Register description

4.15.10.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.10.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.10.11.3 Function model 1 - OSP

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	1	Status of digital outputs 1 to 4	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				
34	1	Activating the OSP output in the module	USINT			•	
		OSPValid	Bit 0				
32	-	CfgOSPMode	USINT				•
36	-	CfgOSPValue	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.10.11.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	-	Status of digital outputs 1 to 4	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.15.10.11.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.10.11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.10.11.5.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

4.15.10.11.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.10.11.6.1 Status of digital outputs 1 to 4

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput04

The status of digital outputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit		Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
3	StatusDigitalOutput04	0	Channel 04: No error
		1	Channel 04: Short circuit or overload

4.15.10.11.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.10.11.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.10.11.7.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.10.11.7.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.10.11.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.10.11.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.11 X20(c)DO4332

4.15.11.1 General information

The module is equipped with 4 outputs for 3-wire connections. The rated output current is 2 A.

- 4 digital outputs with 2 A
- Source connection
- 3-wire connections
- 24 VDC and GND for actuator supply
- Integrated output protection
- OSP mode

4.15.11.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.11.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4332	X20 digital output module, 4 outputs, 24 VDC, 2 A, source, 3-wire connections	
X20cDO4332	X20 digital output module, coated, 4 outputs, 24 VDC, 2 A, source, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 313: X20DO4332, X20cDO4332 - Order data

4.15.11.4 Technical data

Product ID	X20DO4332	X20cDO4332
Short description		
I/O module	4 digital outputs 24 VDC for 3-wire connections	
General information		
B&R ID code	0x1B9C	0xE227
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	
Power consumption		
Bus	0.16 W	
Internal I/O	0.49 W	
Additional power dissipation caused by the actuators (resistive) [W] [1]	+1.6 (Rev. <H0: +2.24)	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
Digital outputs		
Design	FET positive switching	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	2 A	
Total nominal current	8 A (Rev. <H0: 4 A)	
Connection type	3-wire connections	
Output circuit	Source	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")	
Actuator supply	0.5 A in total for output-independent actuator supply	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	5 µA	
$R_{DS(on)}$	100 mΩ (Rev. <H0: 140 mΩ)	
Max. continuous current	8 A	
Peak short circuit current	<4 A (Rev. <H0: <12 A)	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay [3]		
0 -> 1	<300 µs	
1 -> 0	<300 µs	
Switching frequency		
Resistive load [3]	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Additional functions	To increase the output current, outputs can be switched in parallel	
Actuator supply		
Voltage	Module supply minus voltage drop for short circuit protection	
Voltage drop for short circuit protection at 500 mA	Max. 2 V	
Short circuit protection	Yes	
Power consumption		
Actuator supply	Max. 12 W [4]	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 314: X20DO4332, X20cDO4332 - Technical data

Product ID	X20DO4332	X20cDO4332
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 314: X20DO4332, X20cDO4332 - Technical data

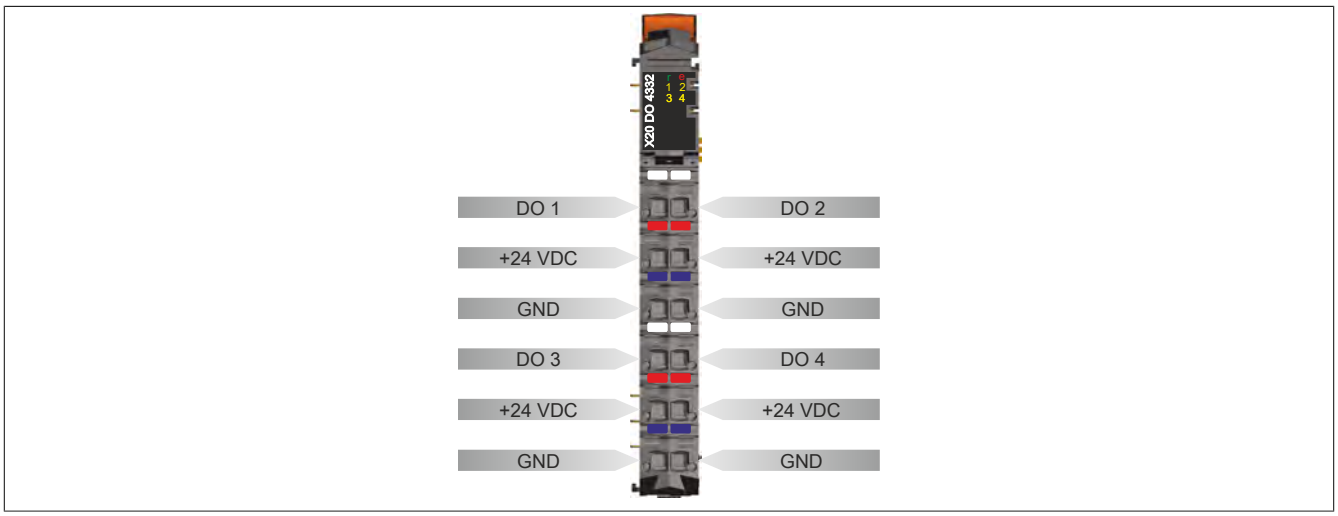
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) At loads ≤ 1 kΩ
4) The power consumption of the sensors connected to the module is not permitted to exceed 12 W.

4.15.11.5 Status LEDs

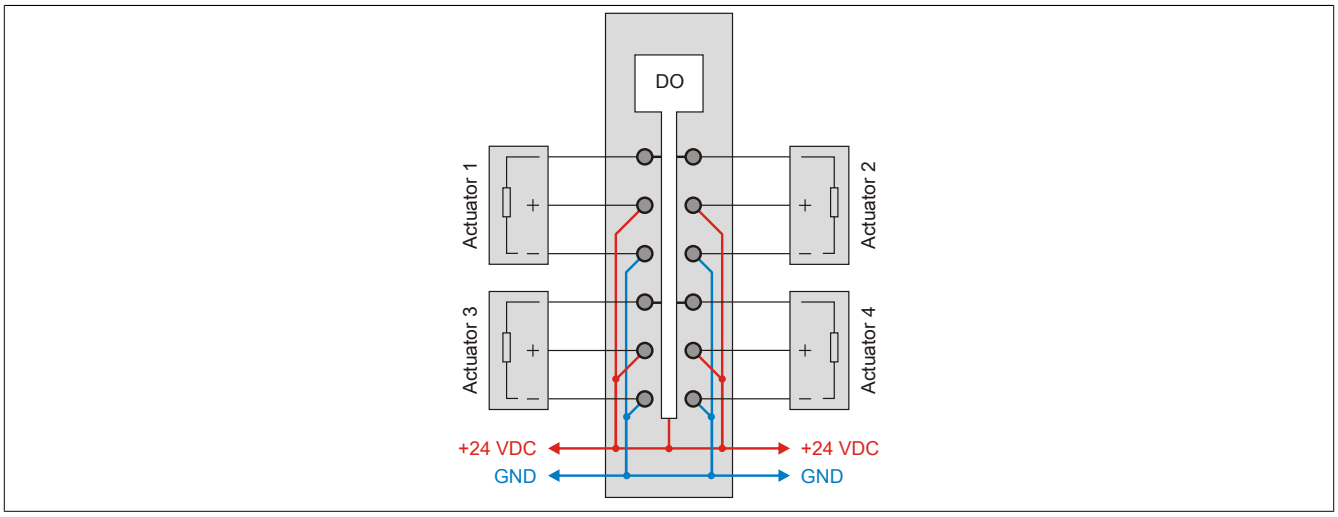
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Output status of the corresponding digital output

4.15.11.6 Pinout



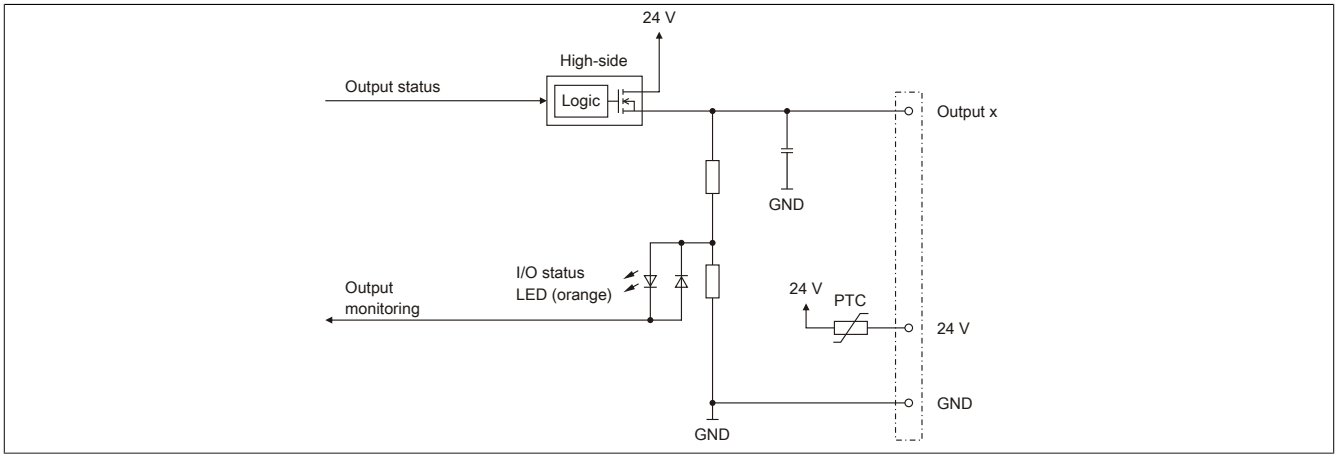
4.15.11.7 Connection example



4.15.11.8 OSP hardware requirements

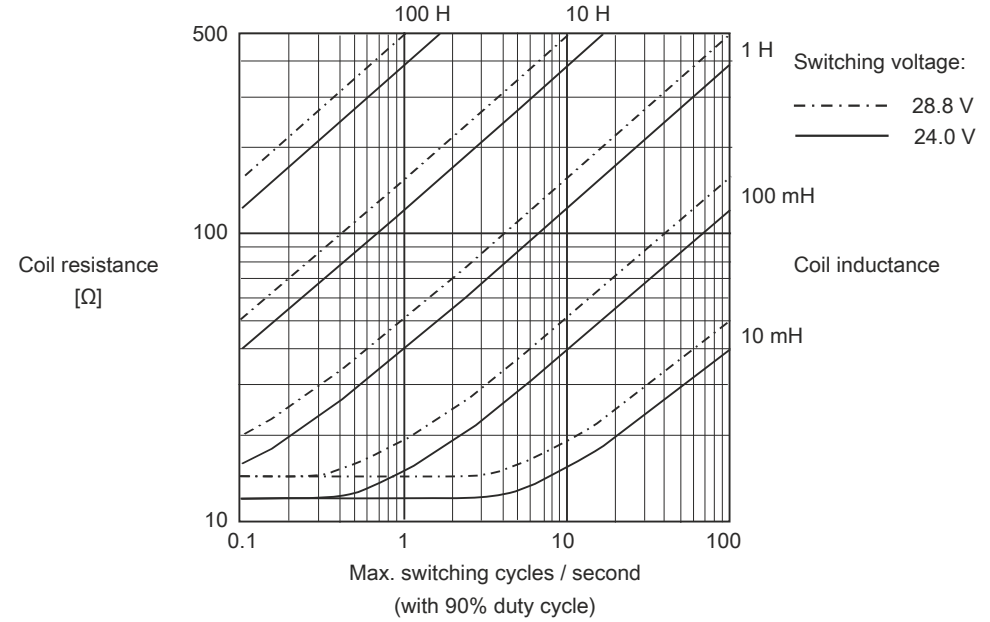
In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.11.9 Output circuit diagram

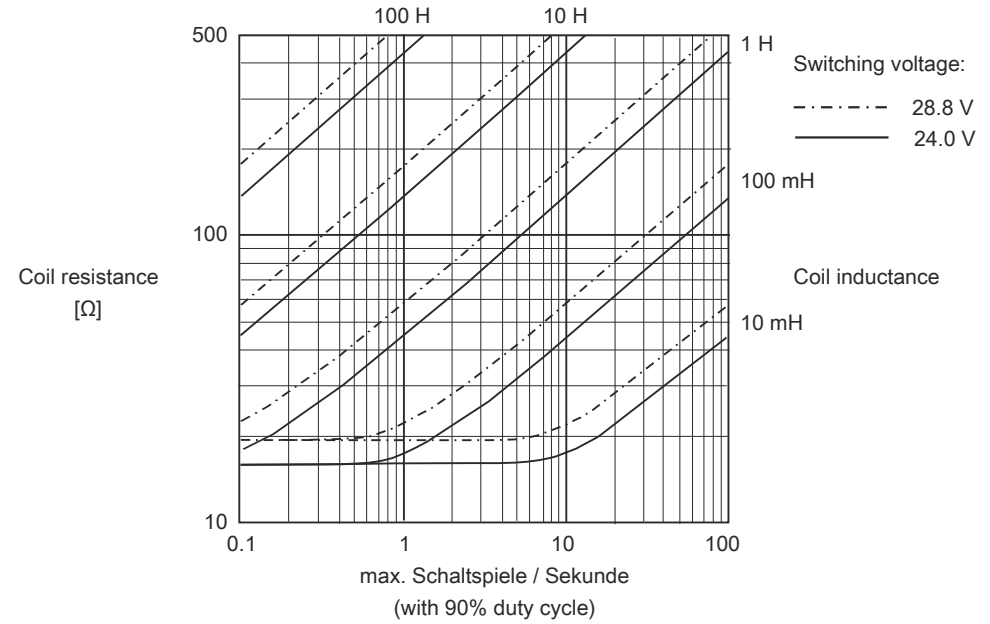


4.15.11.10 Switching inductive loads (Rev. H0 and higher)

Environmental temperature: 50°C, all outputs with the same load.



Environmental temperature: 60°C, all outputs with the same load.



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.11.11 Operation with 2 A

The outputs of the module can handle up to 2 A. With a total current of 4 A, no more than 2 channels are operable at full load. Correct channel assignments are important for achieving optimal use of the module.

The following table provides an overview of the number of fully used channels and the resulting best distribution.

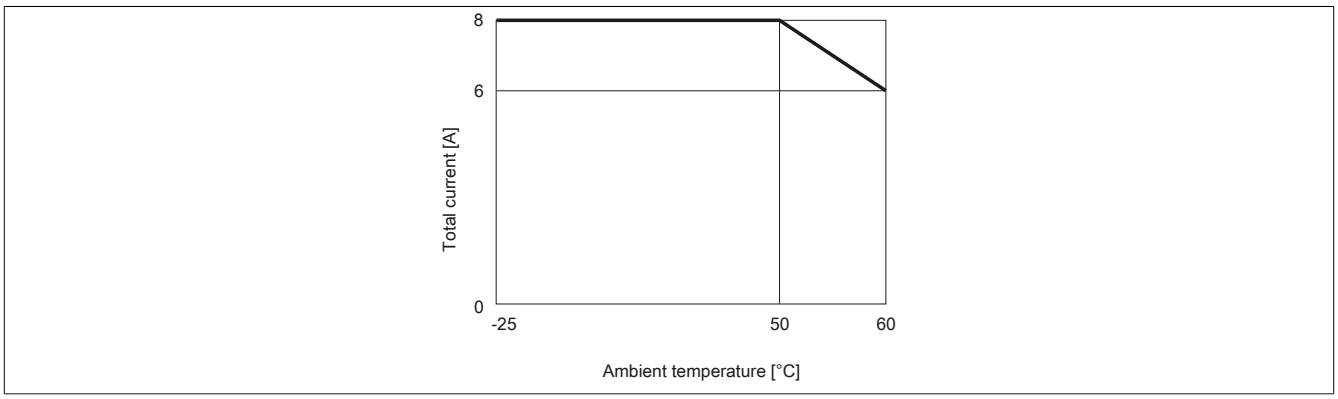
Number of channels using 2A	Division
1	Any
2	The following channel numbers can be assigned: 1, 3 1, 4 2, 4

Information:

This section is only valid up to Rev. H0.

4.15.11.12 Derating

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W.



Information:

This section is only valid for Rev. H0 and higher.

4.15.11.13 Register description

4.15.11.13.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.11.13.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.11.13.3 Function model 1 - OSP

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	1	Status of digital outputs 1 to 4	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				
34	1	Activating the OSP output in the module	USINT			•	
		OSPValid	Bit 0				
32	-	CfgOSPMode	USINT				•
36	-	CfgOSPValue	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.11.13.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
30	-	Status of digital outputs 1 to 4	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput04	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.15.11.13.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.11.13.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.11.13.5.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

4.15.11.13.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.11.13.6.1 Status of digital outputs 1 to 4

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput04

The status of digital outputs 1 to 4 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit		Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
3	StatusDigitalOutput04	0	Channel 04: No error
		1	Channel 04: Short circuit or overload

4.15.11.13.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.11.13.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.11.13.7.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.11.13.7.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.11.13.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.11.13.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.12 X20DO4529

4.15.12.1 General information

The module is equipped with 4 relay outputs.

- 4 digital outputs
- Relay module for 115 VAC
- 4 change over contacts
- Single-channel isolated outputs

Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.15.12.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4529	X20 digital output module, 4 relays, changeover contacts, 115 VAC / 0.5 A, 24 VDC / 1 A	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 315: X20DO4529 - Order data

4.15.12.3 Technical data

Product ID	X20DO4529
Short description	
I/O module	4 digital outputs 30 VDC / 115 VAC, outputs are single-channel isolated
General information	
B&R ID code	0x20D9
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED
Power consumption	
Bus	0.8 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+0.3
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes

Table 316: X20DO4529 - Technical data

Product ID	X20DO4529
Digital outputs	
Design	Relay / Changeover contact Channels are single-channel isolated
Nominal voltage	30 VDC / 115 VAC
Max. voltage	125 VAC
Switching voltage	Max. 110 VDC / 125 VAC
Rated frequency	DC / 45 to 63 Hz
Nominal output current	1 A at 30 VDC / 0.5 A at 115 VAC
Total nominal current	4 A at 30 VDC / 2 A at 115 VAC
Actuator supply	External
Starting current	Max. 2 A (per channel)
Contact resistance	75 mΩ at 6 VDC / 1A
Switching delay	
0 -> 1	≤4 ms
1 -> 0	≤4 ms
Isolation voltage	
Contact - Contact	Tested at 1000 VAC
Contact - Coil	Tested at 1500 VAC
Service life	
Electrical [3]	Min. 100 x 10^3 ops.
Mechanical	Min. 50 x 10^6 ops. (3 Hz)
Switching capacity	
Minimum	0.01 mA / 10 mV DC
Maximum	30 W / 62.5 VA
Protective circuit	
Internal	None
External	
AC	RC combination or VDR
DC	Inverse diode, RC combination or VDR
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 316: X20DO4529 - Technical data

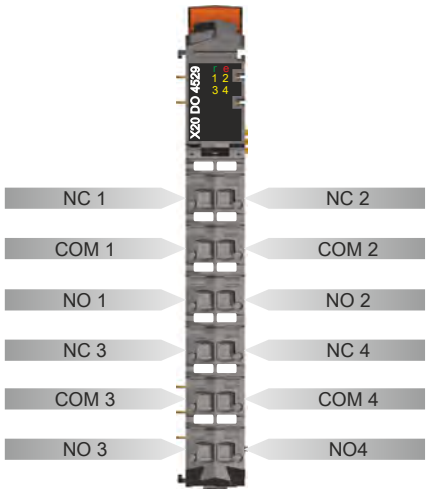
1) Number of outputs x Contact resistance x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) With a resistive load. See also section "Electrical service life"

4.15.12.4 Status LEDs

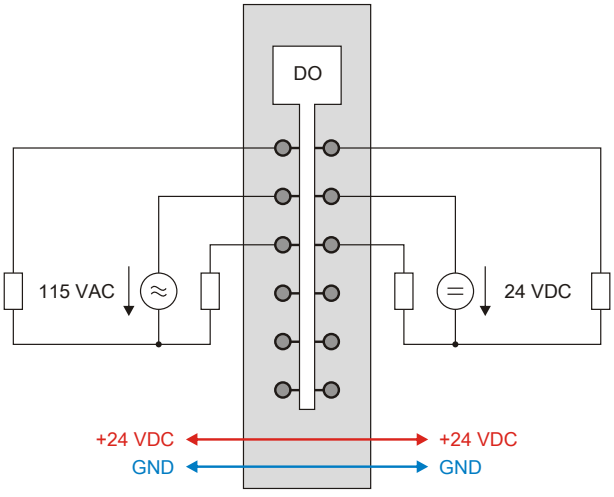
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Output status of the corresponding digital output

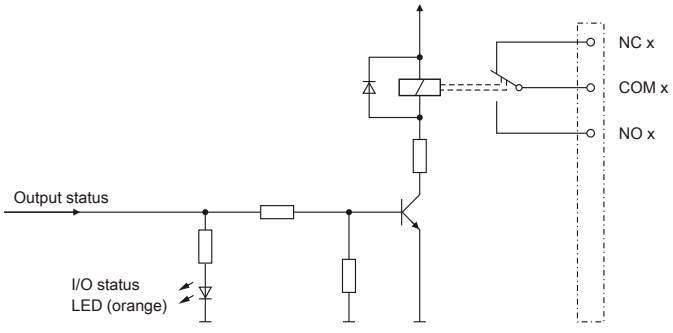
4.15.12.5 Pinout



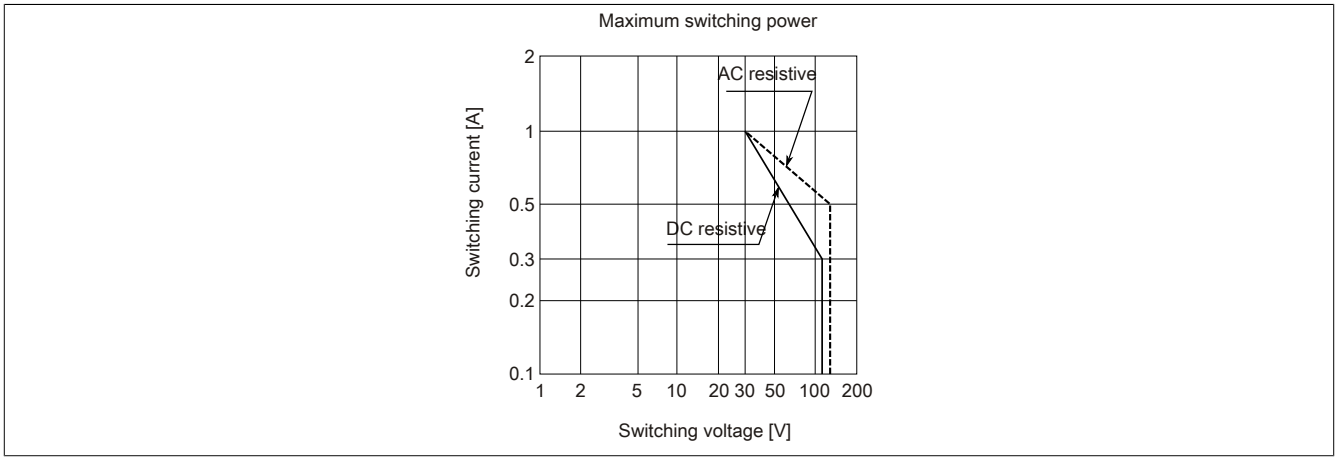
4.15.12.6 Connection example



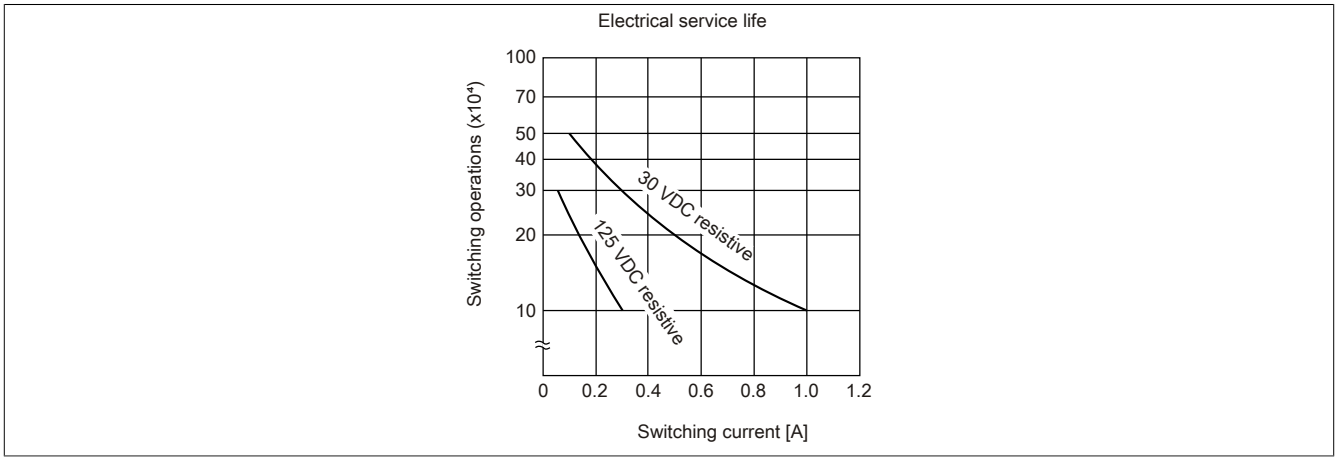
4.15.12.7 Output circuit diagram



4.15.12.8 Maximum switching power



4.15.12.9 Electrical service life



4.15.12.10 Register description

4.15.12.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.12.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.12.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.15.12.10.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.12.10.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.12.10.4.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

4.15.12.10.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.12.10.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.13 X20DO4613

4.15.13.1 General information

The module is a digital output module that is equipped with 4 opto-triac outputs using phase-angle control. L and N are fed to the module for zero-crossing detection.

The 4 outputs are electrically isolated from one another and are used for controlling external power triacs or non-parallel thyristors.

- 4 digital outputs
- Controls external power triacs or non-parallel thyristors
- Outputs with 48 - 240 VAC
- 50 Hz or 60 Hz
- Outputs electrically isolated from one another
- Phase-angle control
- Zero-crossing detection
- Negative half-waves can be switched off
- 2-wire connections
- 240 V coding
- OSP mode
- Frequency mode

Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.15.13.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4613	X20 digital output module, 4 triac coupler outputs, 12 to 240 VAC, 50 mA, zero-crossing detection, 240 V keyed,...	
	Required accessories	
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 317: X20DO4613 - Order data

4.15.13.3 Technical data

Product ID	X20DO4613
Short description	
I/O module	4 digital outputs for controlling external power triacs or non-parallel thyristors
General information	
B&R ID code	0xAD05
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED
Power consumption	
Bus	0.8 W
Internal I/O	-
External I/O	-
Additional power dissipation caused by the actuators (resistive) [W] [1]	+1 W
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Design	Opto-triac
Wiring	N.O. contact
Nominal voltage	48 to 240 VAC
Max. voltage	264 VAC
Rated frequency	47 to 63 Hz
Rated current at 25°C	
Nominal output current	80 mA
Total nominal current	320 mA
Current over entire temperature range	
Output current	50 mA
Summation current	200 mA
Connection type	2-wire connections
Zero-crossing detection	Yes
Holding current	Max. 3.5 mA
Leakage current	Max. 1.5 mA (per channel)
Residual voltage (on-state voltage)	Max. 3 V
Phase-angle control	
Area	5 to 95%
Resolution	1%
Accuracy (60 to 240 VAC)	<100 µs
Voltage monitoring L - N	No
Recommended cabling	Twisted pair cabling to the terminal pairs
Cable length	Max. 10 m
Overvoltage protection between L and N	Yes
Isolation voltage	
Channel - Bus	Tested at 2300 VAC
Channel - Channel	Tested at 2300 VAC
Protective circuit	
External	General protection
Internal	Snubber circuit (RC element) and varistor
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C

Table 318: X20DO4613 - Technical data

Product ID	X20DO4613
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM12 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 318: X20DO4613 - Technical data

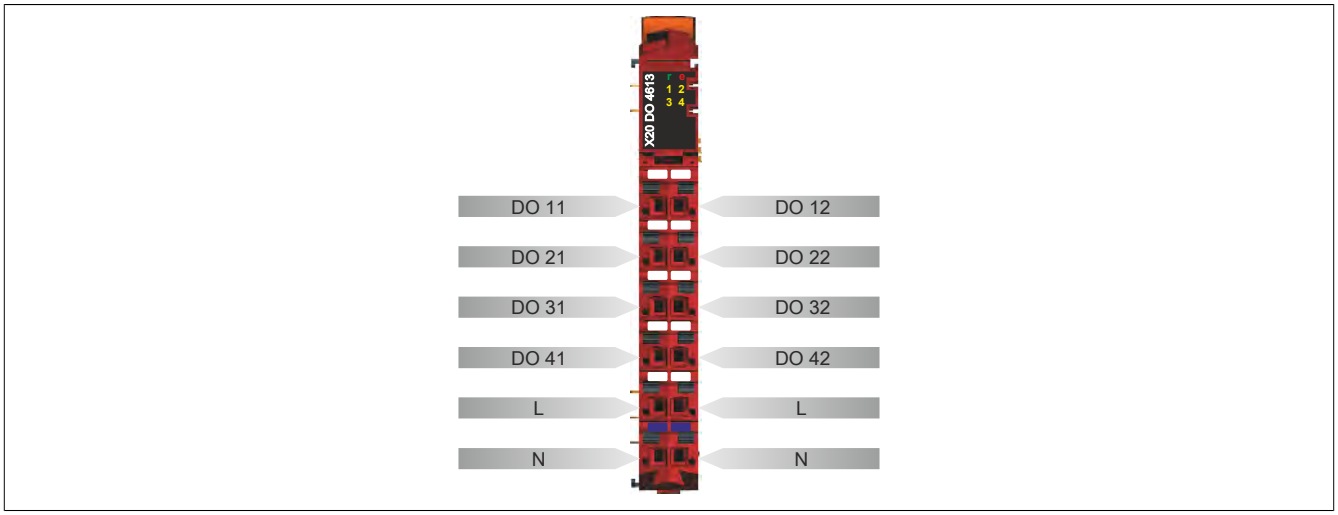
1) Number of outputs x residual voltage (on-state voltage) x nominal output current (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.15.13.4 Status LEDs

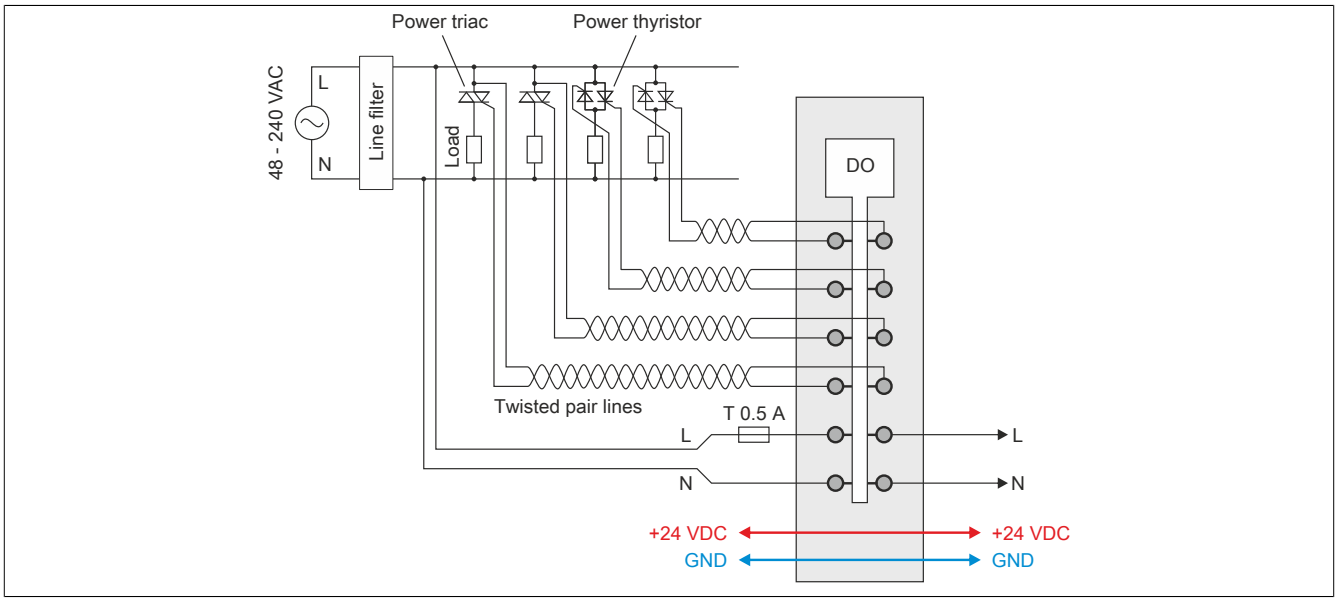
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Loss of zero-crossing signal (input voltage absent or too low)
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Control status of the corresponding digital output

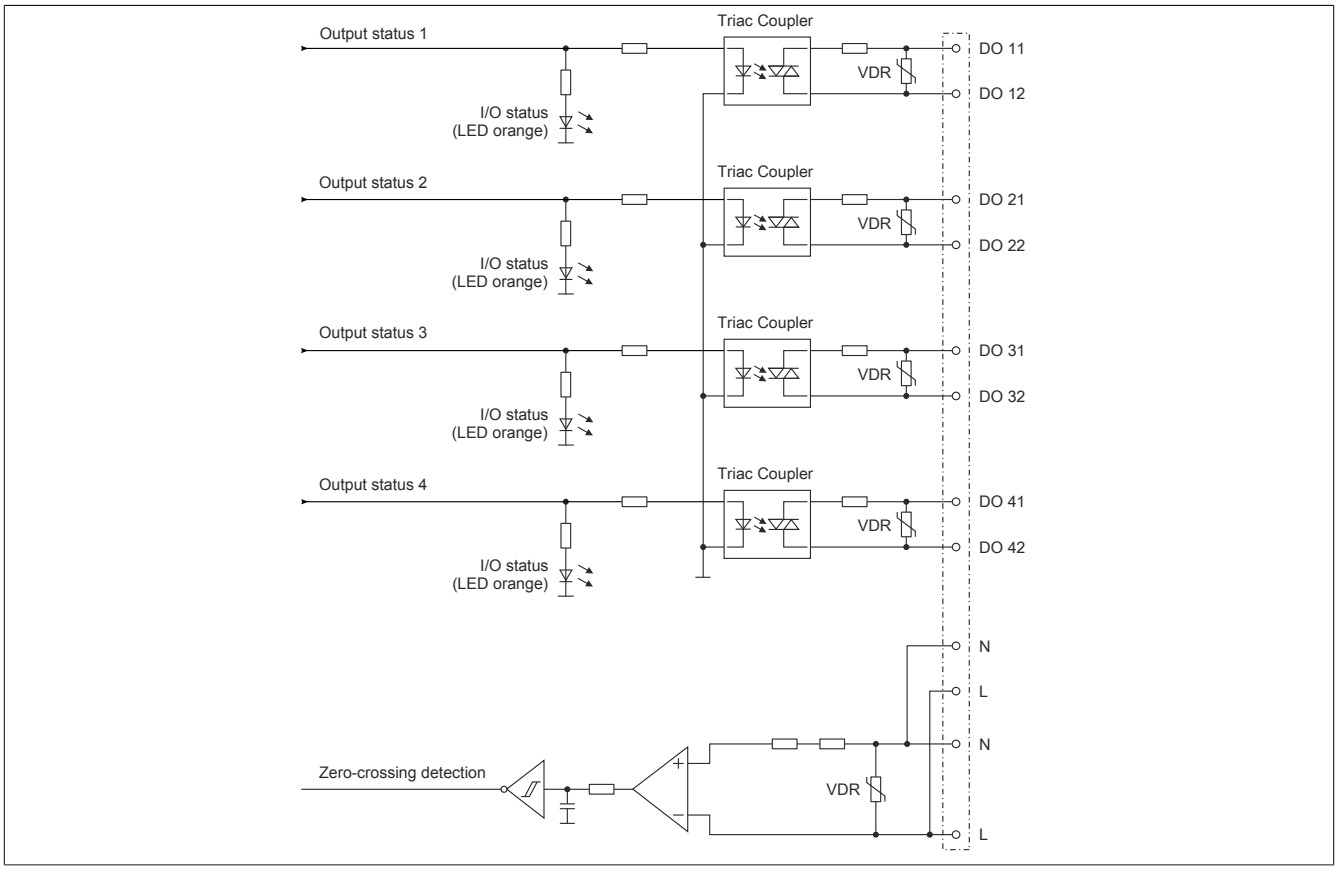
4.15.13.5 Pinout



4.15.13.6 Connection example



4.15.13.7 Output circuit diagram



4.15.13.8 Operating principle

The digital output module DO4613 was designed to control external triacs and thyristors.

The module is equipped with internal zero-crossing detection. Zero-crossing detection is the basis for a software PLL that generates 200 times the zero-crossing frequency. The output signal of the PLL is the base timer for the 4 PWM outputs in both digital and analog mode.

Upon detection of lost periods or periods that are too short, control to the outputs is cut until the PLL is tuned correctly. The tuning procedure can take several seconds. In addition, the "ZeroCrossingStatus" bit is set and the error LED enabled (valid frequency range for the supply is 47 to 63 Hz).

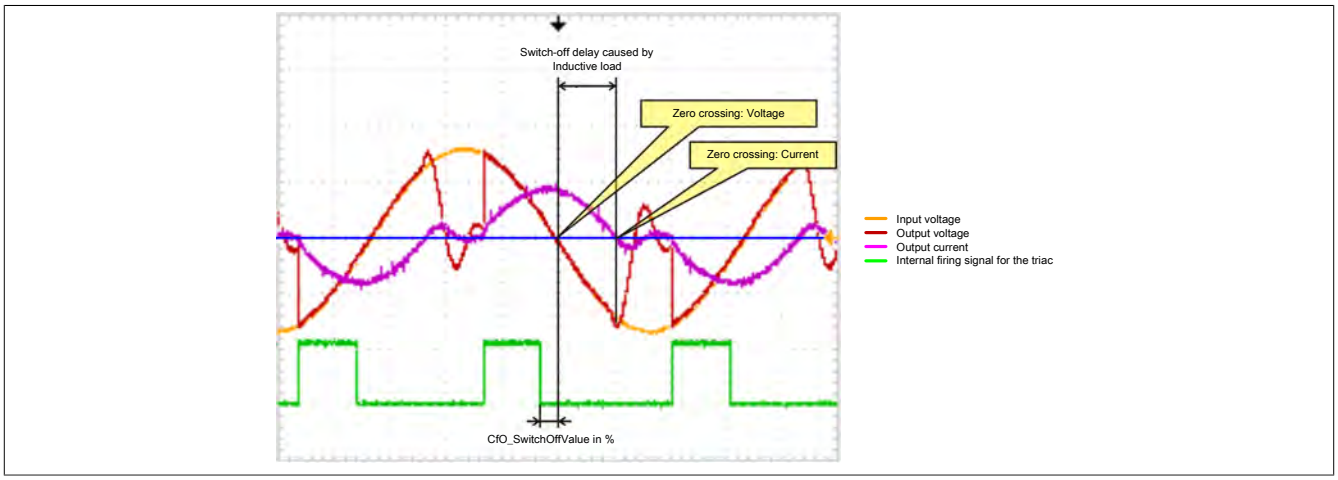
Information:

The jitter of the output signals generated by the PLL and communication can reach 0.5%.

4.15.13.9 Operation with inductive loads

As inherent to its functional principal, the triac output is cleared when the current crosses zero. Because zero crossing for current is delayed with inductive loads, it is possible that the triac will be fired again even though it is not completely cleared at higher output values (between 50 and 100% depending on the inductance of the load). In this case, a full-wave is output. This causes the available control range to be reduced (0 to 100%).

For control beyond the point of full-wave control (up to 100%), the value that is physically output no longer changes. However, this does not cause damage to the module.



4.15.13.10 Register description

4.15.13.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.13.10.2 Function model 0 - Standard and Function model 2 - Frequency mode

The only difference between function model 2 and function model 0 is the possibility of generating half-wave patterns in various frequencies. Register 18 "CfO_Frequency" is an additional register for this.

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General						
2 + N * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18	CfO_Frequency	UINT				•
18 + N * 2	ConfigOutput0N (Index N = 1 to 4)	USINT				•
28	ConfigOutput05	USINT				•
29	CfO_OutputTolerance	USINT				•
Communication						
2	DigitalOutput	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput04	Bit 3				
30	StatusInput01	USINT	•			
	ZeroCrossingInput	Bit 4				
	ZeroCrossingStatus	Bit 7				

4.15.13.10.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General						
2 + N * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18 + N * 2	ConfigOutput0N (Index N = 1 to 4)	USINT				•
28	ConfigOutput05	USINT				•
29	CfO_OutputTolerance	USINT				•
Configuration - OSP						
34	Activating the OSP output in the module	USINT			•	
	OSPValid	Bit 0				
32	CfgOSPMode	USINT				•
36	CfgOSPValue	USINT				•
36 + N * 2	CfgOSPValue0N (Index N = 1 to 4)	USINT				•
Communication						
2	Switching state of digital outputs 1 to 4	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput04	Bit 3				
30	Status of the outputs	USINT	•			
	ZeroCrossingInput	Bit 4				
	ZeroCrossingStatus	Bit 7				

4.15.13.10.4 Function model 254 - Bus controller

Register	Offset	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General							
2 + N * 2	(N-1) * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18 + N * 2	-	ConfigOutput0N (Index N = 1 to 4)	USINT				•
28	-	ConfigOutput05	USINT				•
29	-	CfO_OutputTolerance	USINT				•
Communication							
30	0	Status of the outputs	USINT	•			
		ZeroCrossingInput	Bit 4				
		ZeroCrossingStatus	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.15.13.10.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.15.13.10.5 General information

The digital output module was designed for phase control of resistive and inductive loads.

The module is equipped with internal zero-crossing detection. Zero crossing detection is the basis for a software PLL that generates 200 times the zero crossing frequency. The output signal of the PLL is the base timer for the 2 PWM outputs in both digital and analog mode.

Upon detection of lost periods or periods that are too short, control of the outputs is cut until the PLL is tuned correctly (can take several seconds). In addition, the "ZeroCrossingStatus" bit is set and the Error LED is enabled (valid frequency range for the supply is 45 to 65 Hz).

Information:

The jitter of the output signals generated by the PLL and communication can reach 0.5%.

4.15.13.10.6 Digital outputs

The output state of the outputs defined as digital is transferred to the output ports of the control switch in sync with the connected power mains. The switch-on state is applied when the voltage crosses zero on the positive half-wave and the switch-off state at the zero crossing for current in each half wave.

4.15.13.10.6.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

Information:

The states in these registers are only applied when the channels are set to DIGITAL in register 4.15.13.10.8.3 "ConfigOutput05".

When using the setting "packed outputs" ALL channels must be set to DIGITAL. Mixed operation is not possible.

4.15.13.10.7 Analog outputs

The output value of the outputs defined as analog outputs (unit percent) is switched through to the control ports in sync with power mains. The analog value is output to the TRIAC control port in the range between (output value > SwitchOffValue) and (output value <= 95%) with a resolution of 1%.

Changes to the output value are applied at the next positive half-wave.

4.15.13.10.7.1 Commutation angle for analog outputs 1 - 4

Name:
AnalogOutput01 to AnalogOutput04

These registers are used to set the commutation angle for phase angle control.

Values between 0 and 100 correspond to the output value for the respective channel in percent. Values above 100 correspond to 100%.

Data type	Value
USINT	0 to 100

Information:

The commutation angle for phase angle control set in these registers are only applied when the channels are set to ANALOG in register 4.15.13.10.8.3 "ConfigOutput05".

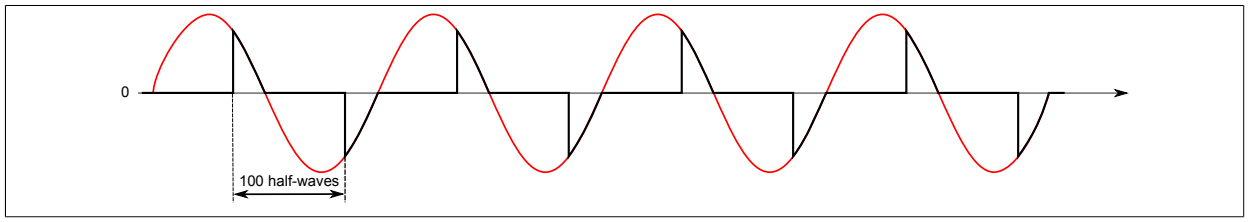
4.15.13.10.8 Output configuration

4.15.13.10.8.1 Configuring the half-wave pattern

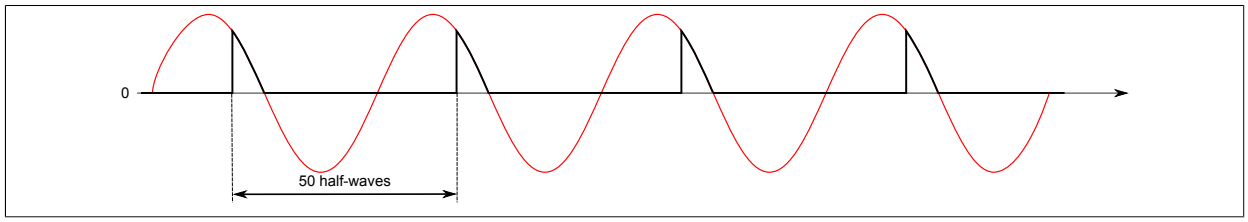
Name:
CfO_Frequency

This register can only be used in function model 2 - Frequency mode and makes it possible to configure the output of half-wave patterns in various frequencies. The commutation angle of the outputs is not affected by this. The following frequency patterns can be configured:

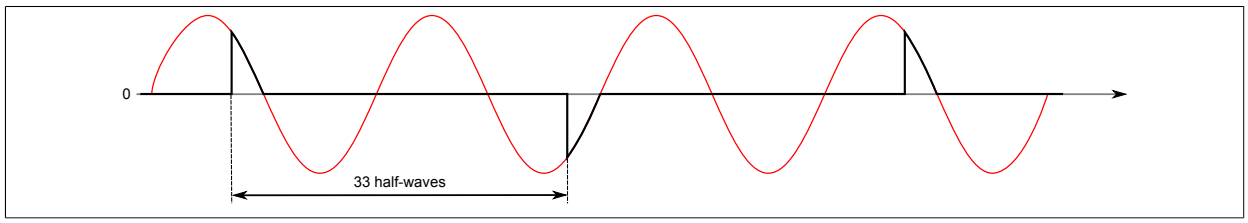
- 100 half-waves



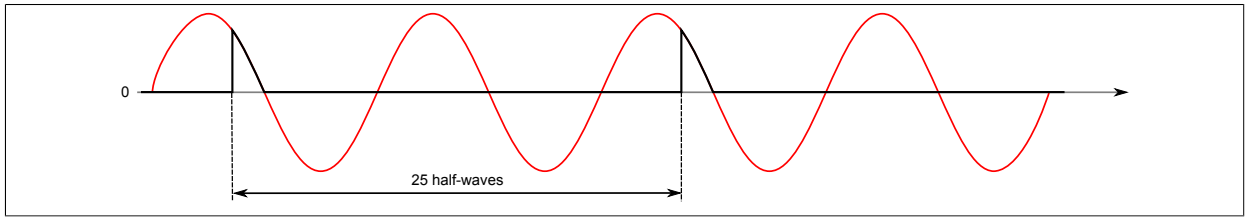
- 50 half-waves



- 33 half-waves



- 25 half-waves



With multichannel operation, the different channels should be operated with delayed half-waves in order to ensure that the load is placed evenly on the module.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Channel 1	0000	100 half-waves/second
		0001	50 half-waves/second
		0010	25 half-waves/second
		0011	33 half-waves/second
		0101	50 half-waves/second delayed by 1 half-wave
		0110	25 half-waves/second delayed by 2 half-waves
		0111	33 half-waves/second delayed by 1 half-wave
4 - 7	Channel 2	0000 to 0111	See channel 1
8 - 11	Channel 3	0000 to 0111	See channel 1
12 - 15	Channel 4	0000 to 0111	See channel 1

Information:

This function is available beginning with firmware version 940. This can be included beginning with hardware variant 8.

4.15.13.10.8.2 Setting the switch-off time

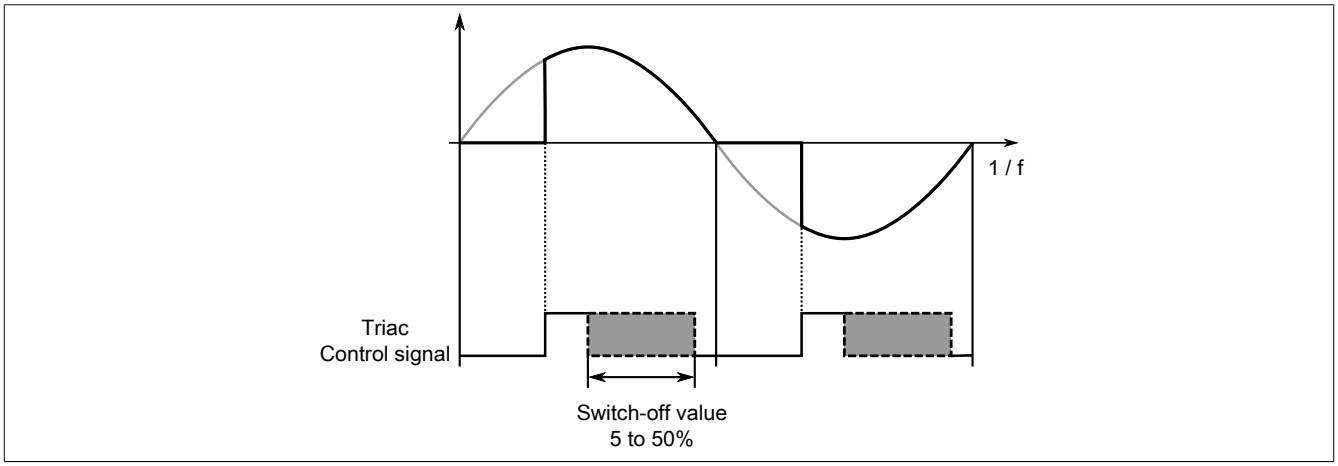
Name:
ConfigOutput01 to ConfigOutput04

This register defines how far in front of the zero cross-over the internal control signal for the TRIAC is switched off. Increasing this value may be necessary in order to prevent unwanted firing of the TRIAC in the event of a slight disturbance in the mains frequency.

With smaller loads, it is important to ensure that this switch off value is not set to large (too early) to prevent switching off prematurely.

The triac can of course only be fired before the set switch-off time.

"SwitchOffValue" in the AS I/O configuration.



Data type	Value	Description
USINT	5 to 50	Switch-off time in %

4.15.13.10.8.3 Configuration of the output channels

Name:
ConfigOutput05

The configuration of the output channels are stored in this register.

"Output type digital/analog" and "Output type full/half wave" in the AS I/O configuration

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel 1: Digital / Analog output	0	Output channel 1 is defined as a digital output. The output status is defined using bit 0 in the register DigitalOutput 1 - 4
		1	Output channel 1 is defined as an analog output. The output status is defined in the register AnalogOutput01
...		...	
3	Channel 4: Digital / Analog output	0	Output channel 4 is defined as a digital output. The output status is defined using bit 1 in the register DigitalOutput 1 - 4
		1	Output channel 2 is defined as an analog output. The output status is defined in the register AnalogOutput04
4	Channel 1: Full-wave / half-wave control[1)]	0	Full-wave control on output channel 1
		1	Negative half-wave on output channel 1 is suppressed.
...		...	
7	Channel 4: Full-wave / half-wave control[1)]	0	Full-wave control on output channel 4
		1	Negative half-wave on output channel 4 is suppressed.

1) Not available in function model 2 - Frequency mode.

4.15.13.10.8.4 Switching behavior for zero-crossing errors

Name:
CfO_OutputTolerance

This register can be used to set the switching behavior of the trigger. After the number of zero-crossing errors configured in Bit 0 to 4, the output is switched off for at least 3 periods. This is followed by synchronization with the zero signal according to Bit 7.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 4	Trigger for Resync	0 to 30	Number of zero-crossover errors
5 - 6	Reserved	-	
7	Fast settling	0	Fast synchronization
		1	PLL synchronization

Fast synchronization

With this option, the trigger point is closed-loop controlled after each individual zero-crossover and input jitter.

- **Advantage:** Increased tolerance and faster response to deviations in mains frequency
- **Disadvantage:** Increased switch-on jitter for firing signal by zero cross signal ±100 µSec

PLL synchronization

With this option the intervals between zero cross-overs are measured and the PLL frequency is updated accordingly.

- **Advantage:** Jitter-free firing signal
- **Disadvantage:** When the output is switched off, additional measurement phases are required before it can be switched back on.

Information:

This function is available starting with Firmware version 928. This can be installed with hardware version 7 and hardware revision B4 or higher.

4.15.13.10.9 Status of the outputs

Name:
ZeroCrossingInput
ZeroCrossingStatus
StatusInput01

The operating status of the outputs is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("ZeroCrossingInput" through "ZeroCrossingStatus") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0 - 3	Reserved	-	
4	ZeroCrossingInput	0	Zero cross signal during the negative half-wave
		1	Zero cross signal during the positive half-wave
5 - 6	Reserved	-	
7	ZeroCrossingStatus	0	Zero cross signal OK
		1	Zero cross signal has dropped out

4.15.13.10.10 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.13.10.10.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.13.10.10.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.13.10.10.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.13.10.10.4 Define the OSP analog output value

Name:
CfgOSPValue01 to CfgOSPValue04

This register contains the analog output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	0 to 100

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.13.10.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
All channels	250 µs

4.15.13.10.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
All channels	150 µs

4.15.14 X20DO4623

4.15.14.1 General information

The module is a digital output module that is equipped with 4 SSR outputs with zero cross-over switches and uses 2-line connections. The module is also equipped with integrated full-wave control. The supply (L and N) is fed directly to the module.

- 4 digital outputs
- Outputs with integrated snubber circuit
- Outputs with 100 to 240 VAC
- L switching
- 50 Hz or 60 Hz
- 2-wire connections
- Integrated full-wave control
- 240 V coding

> **Danger!**
>
> **Risk of electric shock!**
>
> **The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.**

4.15.14.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4623	X20 digital output module, 4 outputs, 100-240 VAC, 0.5 A, source, 240 V keyed, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 319: X20DO4623 - Order data

4.15.14.3 Technical data

Product ID	X20DO4623
Short description	
I/O module	4 digital SSR outputs 100 to 240 VAC for 2-wire connections
General information	
B&R ID code	0x267C
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED
Power consumption	
Bus	0.52 W
Internal I/O	-
External I/O	0.38 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+3.2
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Design	SSR
Wiring	L switching
Nominal voltage	100 to 240 VAC
Max. voltage	264 VAC
Rated frequency	47 to 63 Hz
Nominal output current	0.5 A
Total nominal current	1 A
Surge current	7 A (20 ms), 2 A (1 s)
Connection type	2-wire connections
Zero crossing switches	Yes
Leakage current	Max. 1.5 mA at 240 V
Residual voltage (on-state voltage)	1.6 V
Switching delay	
At 50 Hz	
0 -> 1	≤11 ms
1 -> 0	≤11 ms
At 60 Hz	
0 -> 1	≤9.3 ms
1 -> 0	≤9.3 ms
Isolation voltage between channel and bus	Tested at 2500 VAC
Voltage monitoring L - N	No
Overvoltage protection between L and N	Yes
Output voltage	
Minimum	75 VAC
Protective circuit	
External	Generally a varistor or fuse
Internal	Snubber circuit (RC element)
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C

Table 320: X20DO4623 - Technical data

Product ID	X20DO4623
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM12 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 320: X20DO4623 - Technical data

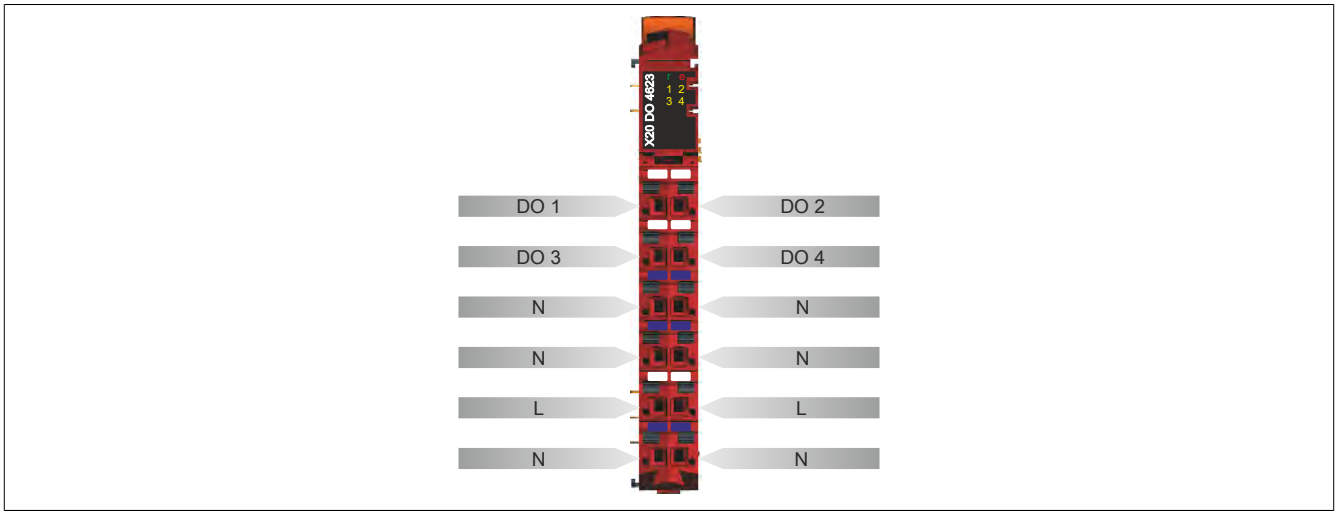
1) Number of outputs x residual voltage (on-state voltage) x nominal output current (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.15.14.4 Status LEDs

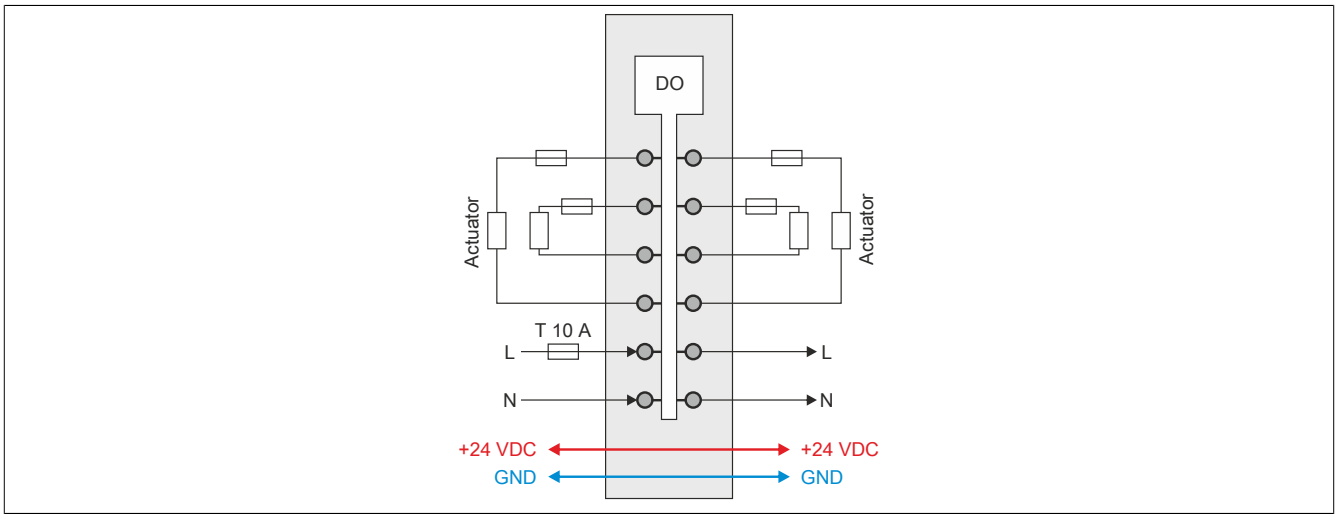
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Zero cross-over signal has dropped out
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Control status of the corresponding digital output

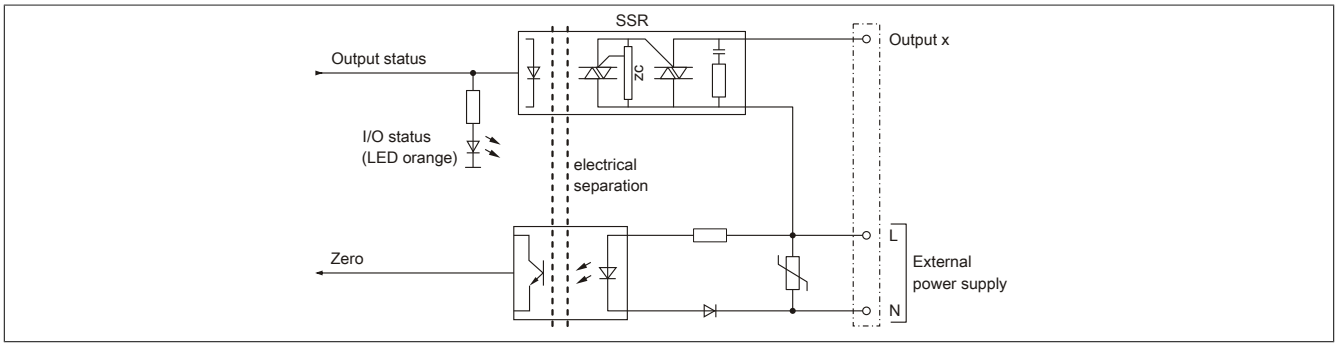
4.15.14.5 Pinout



4.15.14.6 Connection example



4.15.14.7 Output circuit diagram



4.15.14.8 Integrated full-wave control

Full-wave control is used to control power for electrical power consumers that are operated with AC voltage. Temperature control is a typical application

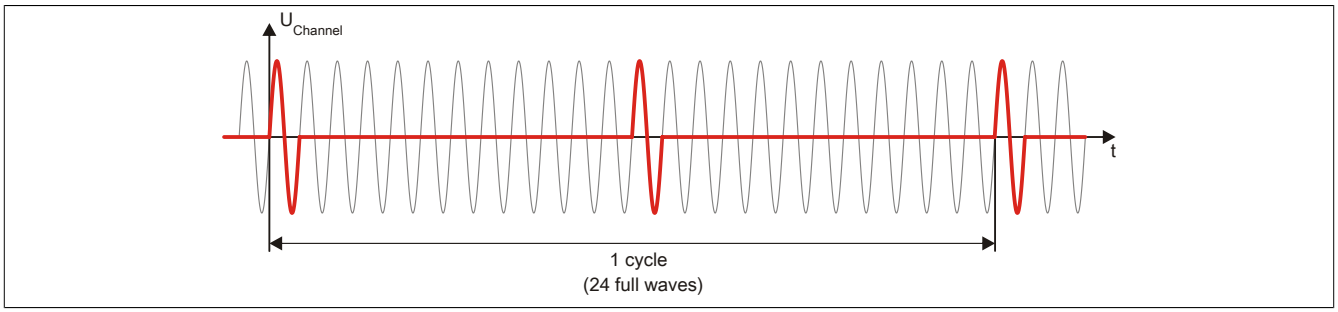
Unlike phase-angle control, the sine wave oscillation form of the mains voltage is not changed during full-wave control. This significantly reduces system perturbation.

The output voltage (channel) is switched on and off at a certain ratio. This switches the multi-cycle packets. A multi-cycle packet consists of a number of complete sine waves throughout a cycle. The relationship between the power-on duration and the cycle duration results in the desired effect of reduced power consumption by the connected power consumer.

With the full-wave control that is integrated in the module, a maximum of 24 full waves can be provided on the outputs per cycle. Control takes place in 4% steps.

Settings		Full waves																						
SW%	%	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
0	0																								
4		•																							
8		•												•											
12		•								•								•							
16		•						•						•						•					
20		•					•					•					•					•			
24	25	•				•				•				•				•				•			
28		•				•			•				•			•				•			•		
32		•			•			•			•			•			•			•			•		
36		•			•			•		•			•			•		•			•			•	
40		•			•		•			•		•		•			•		•			•		•	
44		•			•		•		•		•		•			•		•		•		•		•	
48	50	•		•		•		•		•		•		•		•		•		•		•		•	
52			•	•		•		•		•		•		•	•		•		•		•		•		•
56			•	•		•		•	•		•		•		•	•		•		•	•		•		•
60			•	•		•	•		•		•	•		•	•		•		•	•		•	•		•
64			•	•		•	•		•	•		•	•		•	•		•	•		•	•		•	•
68			•	•	•		•	•		•	•	•		•	•		•	•	•		•	•		•	•
72	75		•	•	•		•	•	•		•	•	•		•	•	•		•	•	•		•	•	•	•
76			•	•	•	•		•	•	•	•		•	•	•	•		•	•	•	•		•	•	•	•
80			•	•	•	•	•		•	•	•	•	•		•	•	•	•	•		•	•	•	•	•	•
84			•	•	•	•	•	•	•		•	•	•	•	•	•	•		•	•	•	•	•	•	•	•
88			•	•	•	•	•	•	•	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•	•
92			•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
96	100	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

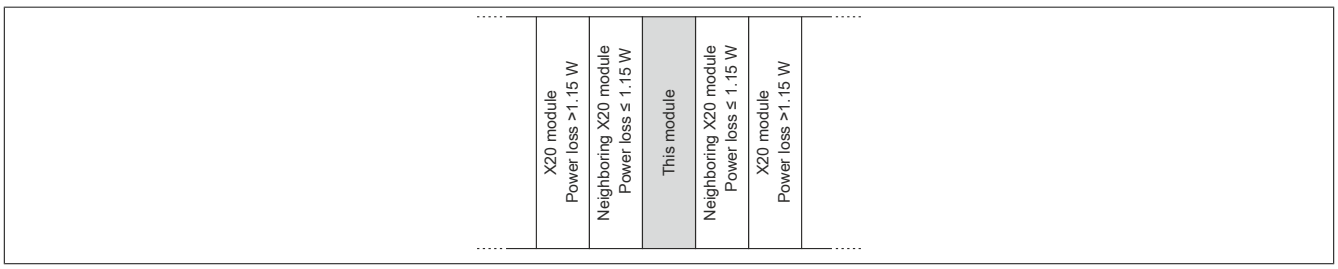
Example of full-wave control (8%):



4.15.14.9 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.15.14.10 Register description

4.15.14.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.14.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
4	1	AnalogOutput01	USINT			•	
6	2	AnalogOutput02	USINT			•	
8	3	AnalogOutput03	USINT			•	
10	4	AnalogOutput04	USINT			•	
28	-	Output configuration 1 - 4 ConfigOutput01	USINT				•
30	1	StatusInput01	USINT	•			
		ZeroCrossingInput	Bit 0				
		ZeroCrossingStatus	Bit 4				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.14.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
4	0	AnalogOutput01	USINT			•	
6	2	AnalogOutput02	USINT			•	
8	4	AnalogOutput03	USINT			•	
10	6	AnalogOutput04	USINT			•	
28	-	Output configuration 1 - 4 ConfigOutput01	USINT				•
30	0	Zero crossing status	USINT	•			
		ZeroCrossingInput	Bit 0				
		ZeroCrossingStatus	Bit 4				

1) The offset specifies where the register is within the CAN object.

4.15.14.10.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.14.10.4 Digital outputs

The output status is transferred to the control switch asynchronously to the connected network. The outputs switch on when the voltage crosses zero and switch off when the current crosses zero.

4.15.14.10.4.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

Information:

The states are only applied when the channels are set to DIGITAL in Setting the output configuration.

When using the setting "packed outputs" ALL channels must be set to DIGITAL. Mixed operation is not possible.

4.15.14.10.5 Analog outputs

The output value is transferred to the control circuit in sync with the connected power mains according to the firing pattern table (see "Integrated full-wave control"). The analog value is output with a resolution of ~4% over a duration of 24 complete waves. Values > 96% result in full control. Changes to the output value within an interval are applied after the next zero crossover.

4.15.14.10.5.1 Setting the output value from the firing pattern table

Name:
AnalogOutput01 to AnalogOutput04

These registers are used to set the output value from the firing pattern table.

Values between 0 and 100 correspond to the output value for the respective channel in percent. Values above 100 correspond to 100%.

Data type	Value
USINT	0 to 100

Information:

The states in these registers are only applied when the channels are set to ANALOG in Setting the output configuration.

4.15.14.10.5.2 Setting the output configuration

Name:
Output configuration 1 - 4
ConfigOutput01

Each channel can be configured for either "digital" or "analog" operation in this register. Depending on the setting, the corresponding DigitalOutput or AnalogOutput registers must be written.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Description
0	Channel 1	0	Digital register is used
1		1	Analog register is used
...		...	
3	Channel 4	0	Digital register is used
		1	Analog register is used
4 - 7	Reserved	0	

4.15.14.10.6 Zero crossing status

Name:
ZeroCrossingInput
ZeroCrossingStatus
StatusInput01

Zero crossing detection uses a fixed filter time of 1 ms and a scanning frequency of 10 kHz. When a missing or too short period is detected, control is switched off until at least 2 periods are detected correctly, and the status flag is set accordingly. Control is offset by 2 ms from the negative half-wave until the next zero crossover is detected correctly or another error occurs. This is normally at least one complete wave.

Monitoring is activated at the first zero crossover after being switched on.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("ZeroCrossingInput" through "ZeroCrossingStatus") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 17	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	ZeroCrossingInput[1)]	0	Signal during the negative half-wave
		1	Signal during the positive half-wave
1 - 3	Reserved	0	
4	ZeroCrossingStatus	0	No error
		1	Zero crossover failed
5 - 7	Reserved	0	

1) Value is valid if no error has occurred (ZeroCrossingStatus= 0)

4.15.14.10.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard function model	100 µs
Bus controller function model	150 µs

4.15.14.10.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Function model 0	Equal to the minimum cycle time
Function model 1	Equal to the minimum cycle time

4.15.15 X20(c)DO4633

4.15.15.1 General information

The module is a digital output module with phase-angle control that is equipped with 4 Triac outputs using 2-line connections. The supply (L and N) is fed directly to the module.

- 4 digital outputs
- Outputs with integrated snubber circuit
- Outputs with 12 to 240 VAC
- L switching
- Zero-crossing detection
- Phase-angle control
- Open-circuit detection for each channel
- Negative half-waves can be switched off
- 50 Hz or 60 Hz
- 2-wire connections
- 240 V coding
- OSP mode
- Frequency mode

Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.15.15.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.15.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4633	X20 digital output module, 4 triac outputs, 12 to 240 VAC, 1 A, L switching, phase angle control, 240 V keyed	
X20cDO4633	X20 digital output module, coated, 4 triac outputs, 12 to 240 VAC, 1 A, L switching, phase angle control, 240 V keyed	
	Required accessories	
	Bus modules	
X20BM32	X20 bus module for double-width modules, 240 VAC keyed, internal I/O supply continuous	
X20cBM32	X20 bus module, coated, for double-width modules, 240 VAC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 321: X20DO4633, X20cDO4633 - Order data

4.15.15.4 Technical data

Product ID	X20DO4633	X20cDO4633
Short description		
I/O module	4 digital outputs 12 to 240 VAC for 2-wire connections	
General information		
B&R ID code	0xAC3A	0xE67D
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED	
Power consumption		
Bus	0.6 W	
Internal I/O	-	
External I/O	-	
Additional power dissipation caused by the actuators (resistive) [W] [1]	+6.4 W	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	-
ATEX Zone 2 [2]	Yes	-
KC	Yes	-
GOST-R	Yes	
Digital outputs		
Design	Triac	
Wiring	L switching	
Nominal voltage	12 to 240 VAC	
Max. voltage	264 VAC	
Rated frequency	47 to 63 Hz	
Nominal output current	1 A	
Total nominal current	4 A	
Maximum current		
Output current	1.25 A	
Summation current	5 A	
Connection type	2-wire connections	
Zero-crossing detection	Yes	
Minimum holding current I_H	15 mA	
Leakage current	Max. 2 mA at 240 V and 50 Hz Max. 2.4 mA at 240 V and 60 Hz	
Residual voltage (on-state voltage)	1.6 V	
Phase-angle control		
Area	5 to 95%	
Resolution	1%	
Accuracy (60 to 240 VAC)	<100 µs	
Voltage monitoring L - N	No	
Additional functions	Open line detection	
Overvoltage protection between L and N	Yes	
Isolation voltage		
Terminal block - Bus	Tested at 2300 VAC (Rev. <E0 1500 VAC)	Tested at 1500 VAC
Terminal block - 24 V	Tested at 2300 VAC (Rev. <E0 2000 VAC)	Tested at 2000 VAC
Terminal block - PE	Tested at 2300 VAC (Rev. <E0 1500 VAC)	Tested at 1500 VAC
Protective circuit		
External	See section "External fuses"	
Internal	Snubber circuit (RC element) and varistor	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 322: X20DO4633, X20cDO4633 - Technical data

Product ID	X20DO4633	X20cDO4633
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB32 terminal block separately Order 1x X20BM32 bus module separately	Order 1x X20TB32 terminal block separately Order 1x X20cBM32 bus module separately
Spacing	25 $^{+0.2}$ mm	

Table 322: X20DO4633, X20cDO4633 - Technical data

1) Number of outputs x residual voltage (on-state voltage) x nominal output current (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.15.15.5 Status LEDs

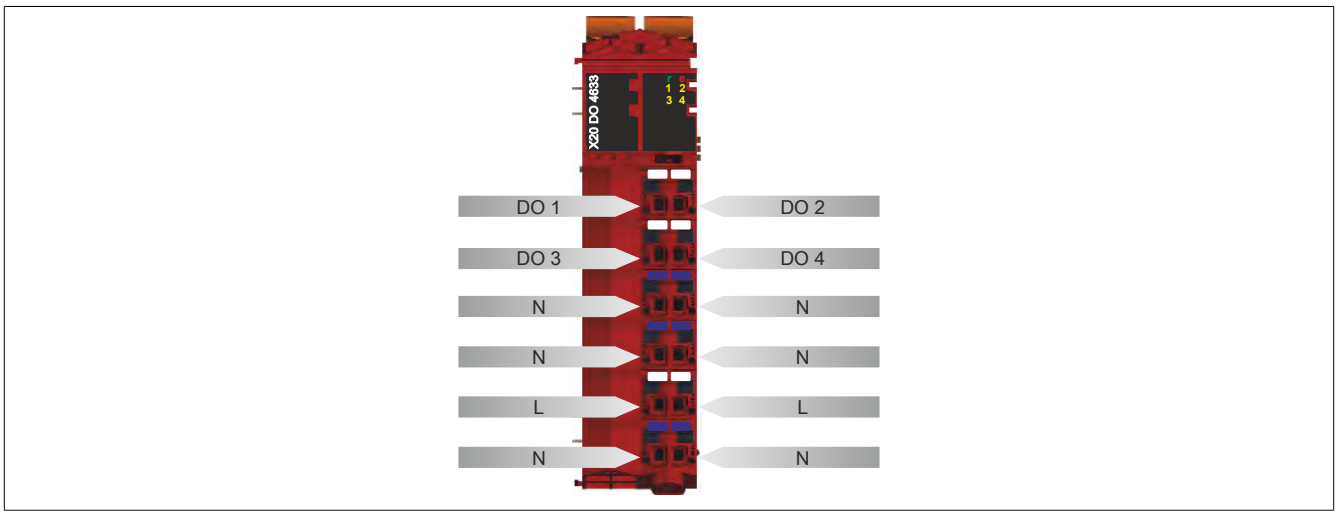
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Loss of zero-crossing signal (I/O supply voltage not applied or too low)
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Control status of the corresponding digital output

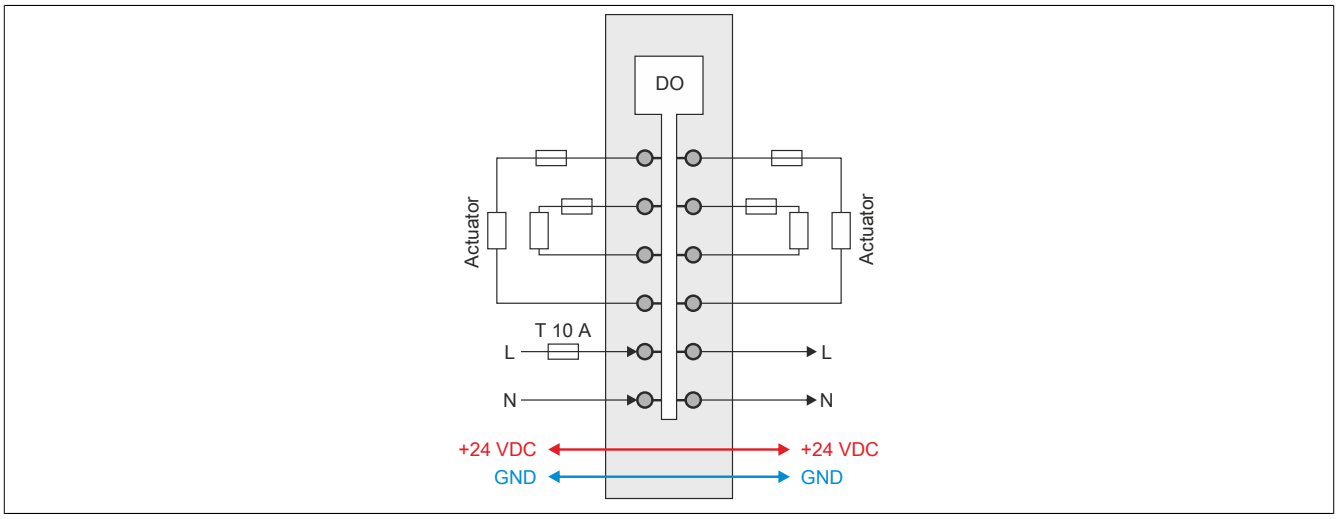
4.15.15.6 Pinout

The following points must be taken into consideration when wiring the module:

- For thermal reasons, wires with a cross-section ≥1.5 mm² must be used to wire the module.
- The neutral return lines for the outputs must be wired to the terminal block separately for each channel and must not be bypassed in the field.
- A line filter must be used for the 240 V supply that provides ≥40 dB attenuation at 150 kHz and works up to 5 MHz.



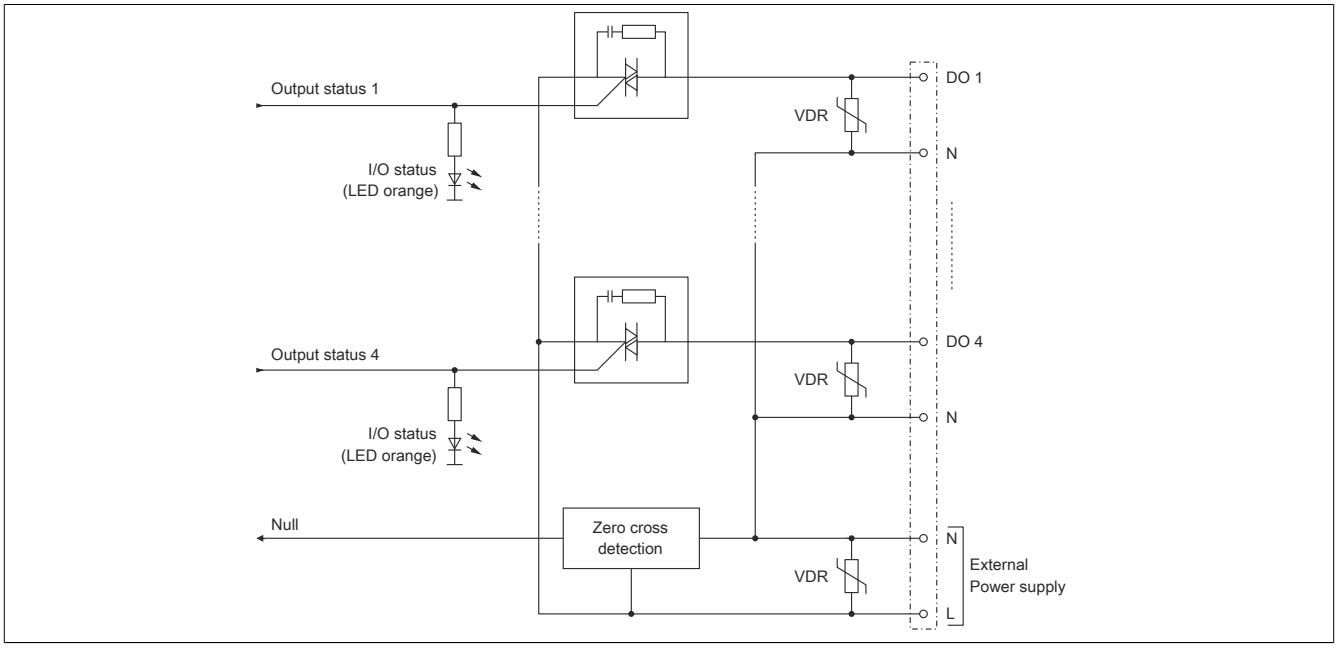
4.15.15.7 Connection example



4.15.15.8 OSP hardware requirements

In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.15.9 Output circuit diagram



4.15.15.10 External fuses

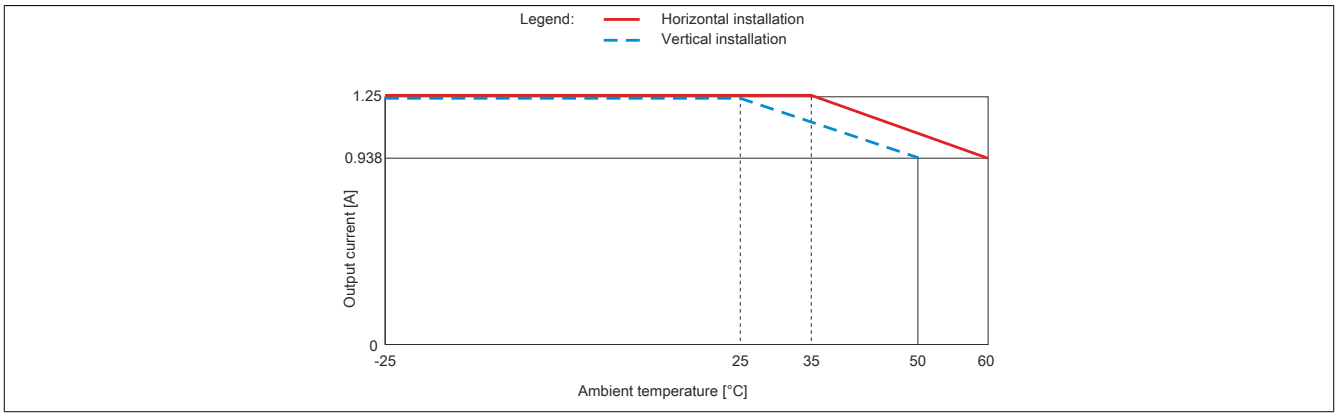
The following protective circuit must be used for safe operation:

	Protective circuit	Value
For the supply lines	Fuse	T 10 A
For the outputs	Fuse	Melting integral $I^2t \leq 36\ A^2s$ when tp = 10 ms
With an inductive load	Varistor[1)]	e.g. varistor with 275 V_{RMS} at 240 VAC
For the supply voltage	Line filter[2)]	Attenuation ≥40 dB at 150 kHz, effective range up to 5 MHz

1) See also section 4.15.6.14 "Operation with inductive loads" on page 1379
2) Meeting the limit values specified in the standards EN 61131, EN 55011 and EN 55022 (each Class A) requires installation of a line filter in the 240 V supply line. Line filters such as the Schaffner FN 2412-8-44 can be used.
If periodic ground transients occur on the supply lines (as can occur with upstream inverters), it is necessary to use an asymmetric filter that keeps these types of changes in potential below a few volts (e.g. "Sinus Plus" from Schaffner) in addition to the symmetric filter.

4.15.15.11 Derating

The derating listed below must be applied for the current:



4.15.15.12 Operating principle

The digital output module was designed for phase control of resistive and and inductive loads. The triac outputs do not have short circuit protection. The integrated open-circuit detection makes it possible to recognize defects on the load or the cabling (see 4.15.6.13 "Open line detection" on page 1378).

The module is equipped with internal zero-crossing detection. Zero-crossing detection is the basis for a software PLL that generates 200 times the zero-crossing frequency. The output signal of the PLL is the base timer for the PWM outputs in both digital and analog mode.

Upon detection of lost periods or periods that are too short, control to the outputs is cut until the PLL is tuned correctly. The tuning procedure can take several seconds. In addition, the "ZeroCrossingStatus" bit is set and the error LED enabled (valid frequency range for the supply is 45 to 65 Hz).

Information:

The jitter of the output signals generated by the PLL and communication can reach 0.5%.

4.15.15.13 Open line detection

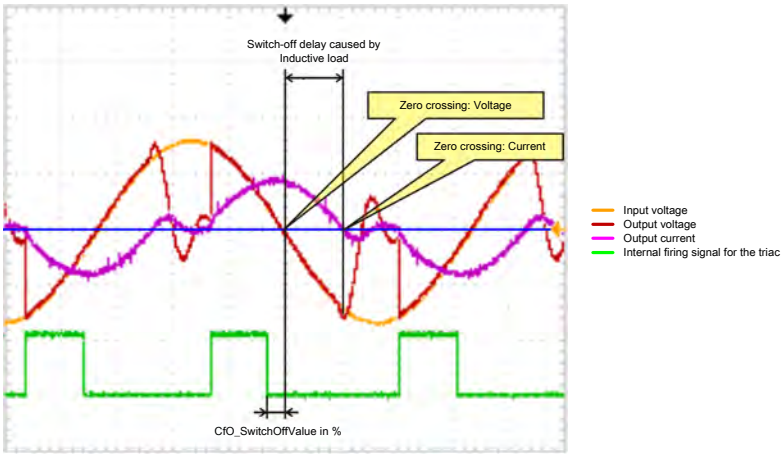
The module is equipped with open-circuit detection. Note that open-circuit detection only works when the output is enabled. An open-circuit will not be detected if the output is turned off.

In addition, open-circuit detection is restricted or doesn't work at all for inductive loads. This depends on the inductance of the load and should be determined beforehand, if necessary.

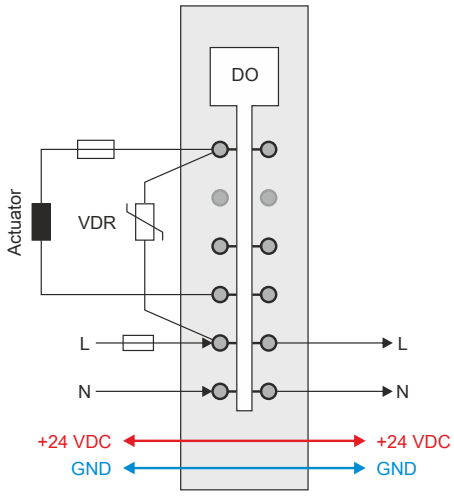
4.15.15.14 Operation with inductive loads

As inherent to its functional principal, the triac output is cleared when the current crosses zero. Because zero crossing for current is delayed with inductive loads, it is possible that the triac will be fired again even though it is not completely cleared at higher output values (between 50 and 100% depending on the inductance of the load). In this case, a full-wave is output. This causes the available control range (0 to 95%) to be changed.

For open line detection (LowCurrentStatus), a pause in control is required where the triac is not permitted to be fired. The full wave that is created with inductive loads causes open line detection to be triggered even though the load on the output is sufficient.
This behavior can be used to detect the full wave and properly adjust the control range (Example: If open line detection is triggered at a control value of 70%, that means that 0 to **70%** corresponds to 0 to **100%** output).



With inductive loads, a suitable varistor must be provided between the output DO x and the phase L (e.g. a varistor with 275 V_{RMS} at 240 VAC).



4.15.15.15 Register description

4.15.15.15.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.15.15.2 Function model 0 - Standard and Function model 2 - Frequency mode

The only difference between function model 2 and function model 0 is the possibility of generating half-wave patterns in various frequencies. Register 18 "CfO_Frequency" is an additional register for this.

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General						
2 + N * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18	CfO_Frequency	UINT				•
18 + N * 2	CfO_SwitchOffValueN (Index N = 1 to 4)	USINT				•
28	CfO_OutputConfig	USINT				•
29	CfO_OutputTolerance	USINT				•
Communication						
2	DigitalOutput	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput04	Bit 3				
30	StatusInput01	USINT	•			
	LowCurrentStatus1	Bit 0				
	...	...				
	LowCurrentStatus4	Bit 3				
	ZeroCrossingInput	Bit 4				
	ZeroCrossingStatus	Bit 7				

4.15.15.15.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General						
2 + N * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18 + N * 2	CfO_SwitchOffValueN (Index N = 1 to 4)	USINT				•
28	CfO_OutputConfig	USINT				•
29	CfO_OutputTolerance	USINT				•
Configuration - OSP						
34	Activating the OSP output in the module	USINT			•	
	OSPValid	Bit 0				
32	Setting the OSP mode	USINT				•
36	CfgOSPValue	USINT				•
36 + N * 2	CfgOSPValue0N (Index N = 1 to 4)	USINT				•
Communication						
2	Switching state of digital outputs 1 to 4	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput04	Bit 3				
30	Status of the outputs	USINT	•			
	LowCurrentStatus1	Bit 0				
	...	...				
	LowCurrentStatus4	Bit 3				
	ZeroCrossingInput	Bit 4				
	ZeroCrossingStatus	Bit 7				

4.15.15.15.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration - General							
2 + N * 2	(N-1) * 2	AnalogOutput0N (Index N = 1 to 4)	USINT			•	
18 + N * 2	-	CfO_SwitchOffValueN (Index N = 1 to 4)	USINT				•
28	-	CfO_OutputConfig	USINT				•
29	-	CfO_OutputTolerance	USINT				•
Communication							
30	0	Status of the outputs	USINT	•			
		LowCurrentStatus1	Bit 0				
		...	...				
		LowCurrentStatus4	Bit 3				
		ZeroCrossingInput	Bit 4				
		ZeroCrossingStatus	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.15.15.15.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.15.15.15.5 General information

The digital output module was designed for phase control of resistive and inductive loads. The triac outputs do not have short circuit protection, but have open line detection that can be used to find defects in the consumer or the wiring.

The module is equipped with internal zero-crossing detection. Zero crossing detection is the basis for a software PLL that generates 200 times the zero crossing frequency. The output signal of the PLL is the base timer for the 2 PWM outputs in both digital and analog mode.

Upon detection of lost periods or periods that are too short, control of the outputs is cut until the PLL is tuned correctly (can take several seconds). In addition, the "ZeroCrossingStatus" bit is set and the Error LED is enabled (valid frequency range for the supply is 45 to 65 Hz).

Information:

The jitter of the output signals generated by the PLL and communication can reach 0.5%.

4.15.15.15.6 Digital outputs

The output state of the outputs defined as digital is transferred to the output ports of the control switch in sync with the connected power mains. The switch-on state is applied when the voltage crosses zero on the positive half-wave and the switch-off state at the zero crossing for current in each half wave.

4.15.15.15.6.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

Information:

The states in these registers are only applied when the channels are set to DIGITAL in register 4.15.15.15.8.3 "CfO_OutputConfig".

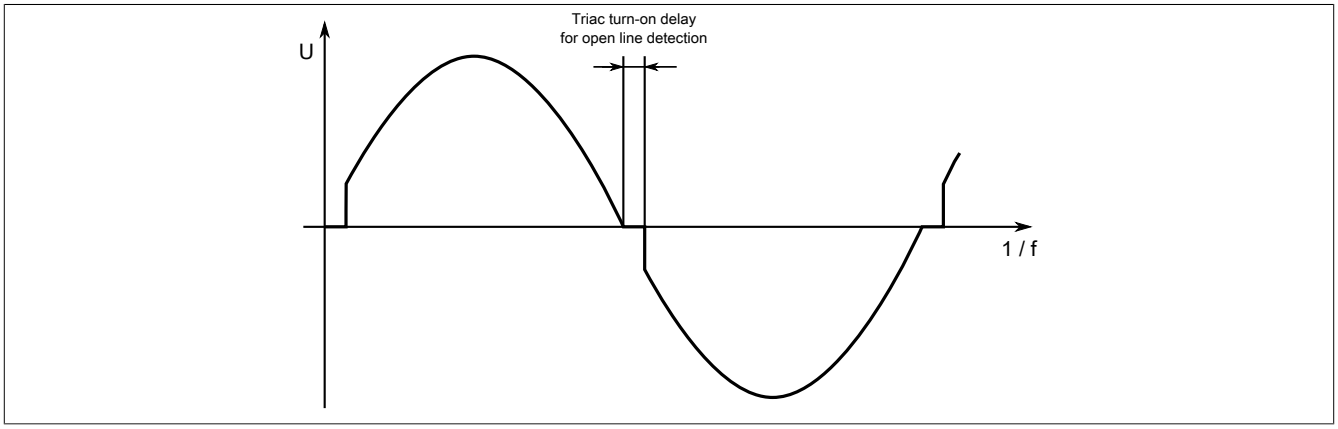
When using the setting "packed outputs" ALL channels must be set to DIGITAL. Mixed operation is not possible.

4.15.15.15.7 Analog outputs

The output value of the outputs defined as analog outputs (unit percent) is switched through to the control ports in sync with power mains. The analog value is output to the TRIAC control port in the range between (output value > SwitchOffValue) and (output value <= 95%) with a resolution of 1%.

A short triac turn-on delay is required for open line detection. Therefore even with output values >= 96%, there is a small pause in control.

Changes to the output value are applied at the next positive half-wave



4.15.15.15.7.1 Commutation angle for analog outputs 1 - 4

Name:
AnalogOutput01 to AnalogOutput04

These registers are used to set the commutation angle for phase angle control.

Values between 0 and 100 correspond to the output value for the respective channel in percent. Values above 100 correspond to 100%.

Data type	Value
USINT	0 to 100

Information:

The commutation angle for phase angle control set in these registers are only applied when the channels are set to ANALOG in register 4.15.15.15.8.3 "CfO_OutputConfig".

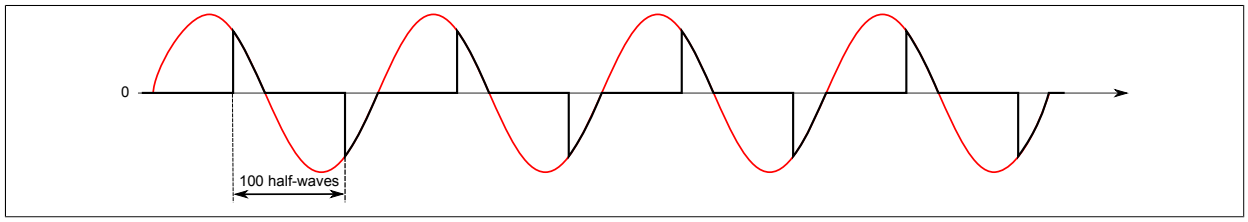
4.15.15.15.8 Output configuration

4.15.15.15.8.1 Configuring the half-wave pattern

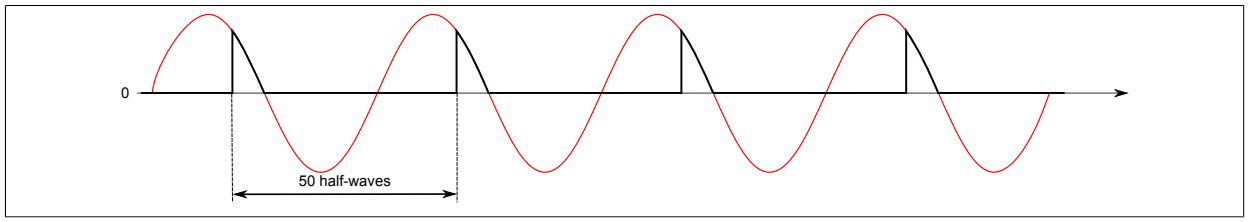
Name:
CfO_Frequency

This register can only be used in function model 2 - Frequency mode and makes it possible to configure the output of half-wave patterns in various frequencies. The commutation angle of the outputs is not affected by this. The following frequency patterns can be configured:

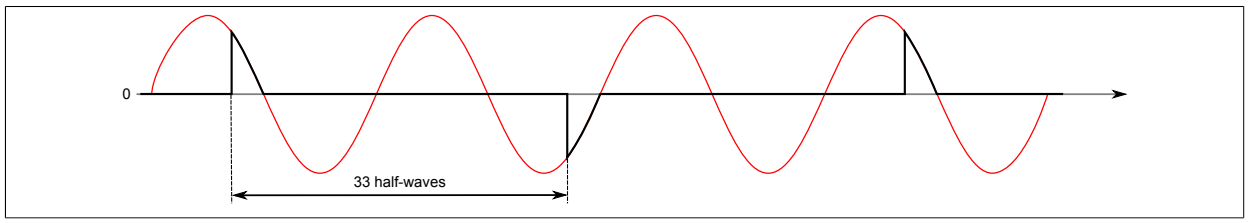
- 100 half-waves



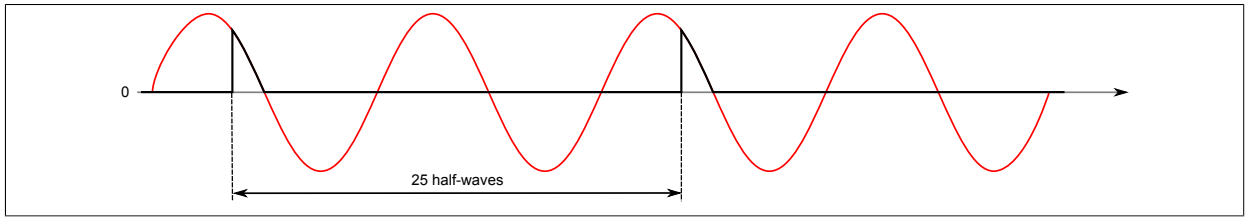
- 50 half-waves



- 33 half-waves



- 25 half-waves



With multichannel operation, the different channels should be operated with delayed half-waves in order to ensure that the load is placed evenly on the module.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Channel 1	0000	100 half-waves/second
		0001	50 half-waves/second
		0010	25 half-waves/second
		0011	33 half-waves/second
		0101	50 half-waves/second delayed by 1 half-wave
		0110	25 half-waves/second delayed by 2 half-waves
		0111	33 half-waves/second delayed by 1 half-wave
4 - 7	Channel 2	0000 to 0111	See channel 1
8 - 11	Channel 3	0000 to 0111	See channel 1
12 - 15	Channel 4	0000 to 0111	See channel 1

Information:

This function is available beginning with firmware version 940. This can be included beginning with hardware variant 8.

4.15.15.15.8.2 Setting the switch-off time

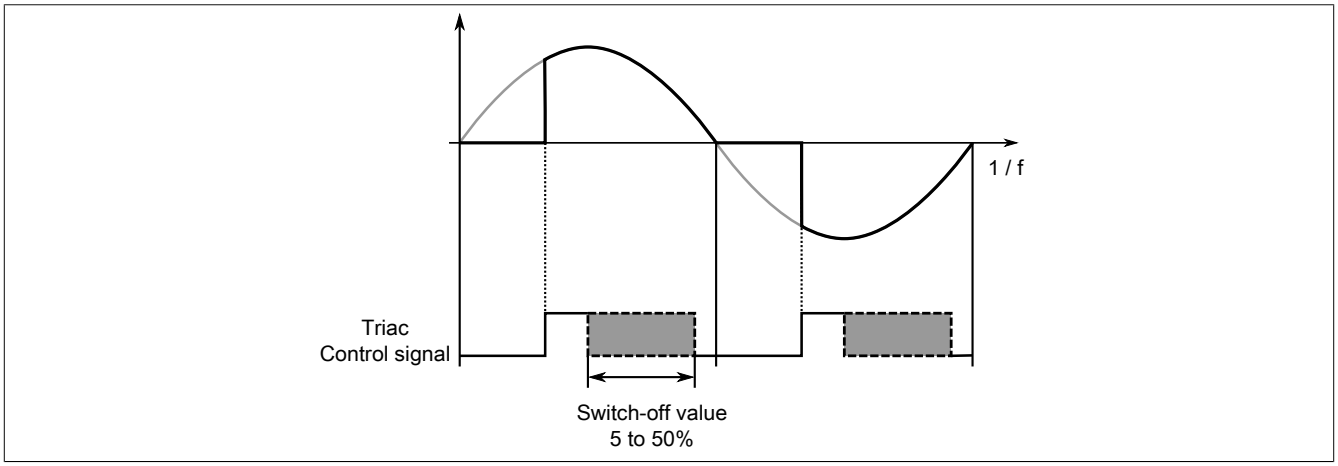
Name:
CfO_SwitchOffValue1 to CfO_SwitchOffValue4

This register defines how far in front of the zero cross-over the internal control signal for the TRIAC is switched off. Increasing this value may be necessary in order to prevent unwanted firing of the TRIAC in the event of a slight disturbance in the mains frequency.

With smaller loads, it is important to ensure that this switch off value is not set to large (too early) to prevent switching off prematurely.

The triac can of course only be fired before the set switch-off time.

"SwitchOffValue" in the AS I/O configuration.



Data type	Value	Description
USINT	5 to 50	Switch-off time in %

4.15.15.15.8.3 Configuration of the output channels

Name:
CfO_OutputConfig

The configuration of the output channels are stored in this register.

"Output type digital/analog" and "Output type full/half wave" in the AS I/O configuration

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel 1: Digital / Analog output	0	Output channel 1 is defined as a digital output. The output status is defined using bit 0 in the register DigitalOutput 1 - 4
		1	Output channel 1 is defined as an analog output. The output status is defined in the register AnalogOutput01
...		...	
3	Channel 4: Digital / Analog output	0	Output channel 4 is defined as a digital output. The output status is defined using bit 1 in the register DigitalOutput 1 - 4
		1	Output channel 2 is defined as an analog output. The output status is defined in the register AnalogOutput04
4	Channel 1: Full-wave / half-wave control[1)]	0	Full-wave control on output channel 1
		1	Negative half-wave on output channel 1 is suppressed.
...		...	
7	Channel 4: Full-wave / half-wave control[1)]	0	Full-wave control on output channel 4
		1	Negative half-wave on output channel 4 is suppressed.

1) Not available in function model 2 - Frequency mode.

4.15.15.15.8.4 Switching behavior for zero-crossing errors

Name:
CfO_OutputTolerance

This register can be used to set the switching behavior of the trigger. After the number of zero-crossing errors configured in Bit 0 to 4, the output is switched off for at least 3 periods. This is followed by synchronization with the zero signal according to Bit 7.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 4	Trigger for Resync	0 to 30	Number of zero-crossover errors
5 - 6	Reserved	-	
7	Fast settling	0	Fast synchronization
		1	PLL synchronization

Fast synchronization

With this option, the trigger point is closed-loop controlled after each individual zero-crossover and input jitter.

- **Advantage:** Increased tolerance and faster response to deviations in mains frequency
- **Disadvantage:** Increased switch-on jitter for firing signal by zero cross signal ±100 µSec

PLL synchronization

With this option the intervals between zero cross-overs are measured and the PLL frequency is updated accordingly.

- **Advantage:** Jitter-free firing signal
- **Disadvantage:** When the output is switched off, additional measurement phases are required before it can be switched back on.

Information:

This function is available starting with Firmware version 928. This can be installed with hardware version 8 and hardware revision B2 or higher.

4.15.15.15.9 Status of the outputs

Name:
LowCurrentStatus1 through LowCurrentStatus4
ZeroCrossingInput
ZeroCrossingStatus
StatusInput01

The operating status of the outputs is mapped in this register.

In order to do determine the "LowCurrentStatus", the system checks if there is a neutral connection from the output via the consumer shortly before each triac firing.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("LowCurrentStatus1" through "ZeroCrossingStatus") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	LowCurrentStatus1	0	0 = No current flow on activated output 1
		1	No current flow on activated output 1
...		...	
3	LowCurrentStatus4	0	Current flow on activated output 4
		1	No current flow on activated output 4
4	ZeroCrossingInput	0	Zero cross signal during the negative half-wave
		1	Zero cross signal during the positive half-wave
5 - 6	Reserved	-	
7	ZeroCrossingStatus	0	Zero cross signal OK
		1	Zero cross signal has dropped out

4.15.15.15.10 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.15.15.10.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.15.15.10.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.15.15.10.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.15.15.10.4 Define the OSP analog output value

Name:
CfgOSPValue01 to CfgOSPValue04

This register contains the analog output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	0 to 100

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.15.15.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
All channels	250 µs

4.15.15.15.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
All channels	150 µs

4.15.16 X20(c)DO4649

4.15.16.1 General information

The module is equipped with 4 relay outputs.

- 4 digital outputs
- Relay module for 240 VAC / 30 VDC
- 4 normally open contacts
- Single-channel isolated outputs

Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

4.15.16.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.16.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO4649	X20 digital output module, 4 relays, N.O. contacts, 240 VAC / 5 A	
X20cDO4649	X20 digital output module, coated, 4 relays, N.O. contacts, 240 VAC / 5 A	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 323: X20DO4649, X20cDO4649 - Order data

4.15.16.4 Technical data

Product ID	X20DO4649	X20cDO4649
Short description		
I/O module	4 digital outputs 30 VDC / 240 VAC, outputs are single-channel isolated	
General information		
B&R ID code	0xA704	0xE67E
Status indicators	I/O function per channel, operating state, module status	

Table 324: X20DO4649, X20cDO4649 - Technical data

Product ID	X20DO4649	X20cDO4649
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED	
Power consumption		
Bus	0.8 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W] 1)	+1.5	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 2)	Yes	
KC	Yes	-
GL	Yes	-
GOST-R	Yes	
Digital outputs		
Design	Relay / Normally open contact Channels are single-channel isolated	
Nominal voltage	30 VDC / 240 VAC	
Max. voltage	264 VAC	
Switching voltage	Max. 110 VDC / 264 VAC	
Rated frequency	DC / 45 to 63 Hz	
Nominal output current	5 A at 30 VDC / 5 A at 240 VAC	
Total nominal current	10 A at 30 VDC / 10 A at 240 VAC	
Actuator supply	External	
Contact resistance	Max. 100 mΩ	
Switching delay		
0 -> 1	≤10 ms	
1 -> 0	≤10 ms	
Isolation voltage		
Contact - Contact	Tested at 750 VAC	
Contact - Coil	Tested at 2300 VAC	
Service life		
Electrical 3)	Min. 5 x 10^4 ops. (NO) at 5 A	
Mechanical	Min. 2 x 10^7 ops.	
Switching capacity		
Minimum	0.05 W / 2.4 VA	
Maximum	150 W / 1250 VA	
Protective circuit		
Internal	None	
External		
AC	RC combination or VDR	
DC	Inverse diode, RC combination or VDR	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 324: X20DO4649, X20cDO4649 - Technical data

Product ID	X20DO4649	X20cDO4649
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 324: X20DO4649, X20cDO4649 - Technical data

1) Number of outputs x Contact resistance x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) With a resistive load. See also section "Electrical service life"

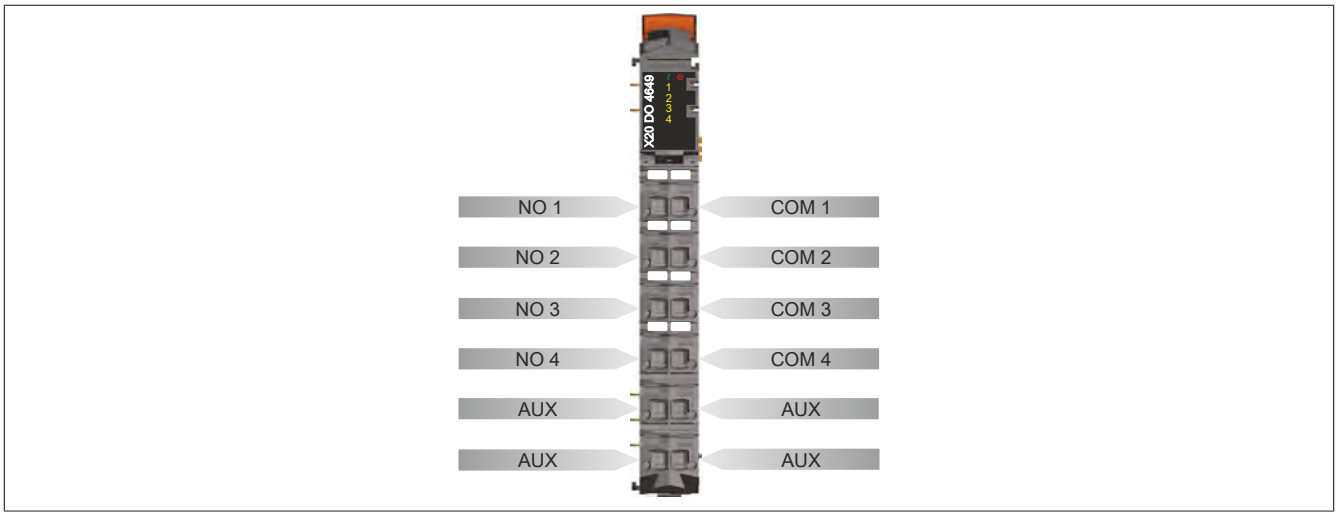
4.15.16.5 Status LEDs

For a description of the various operating modes, see section 2.11.1 "re LEDs".

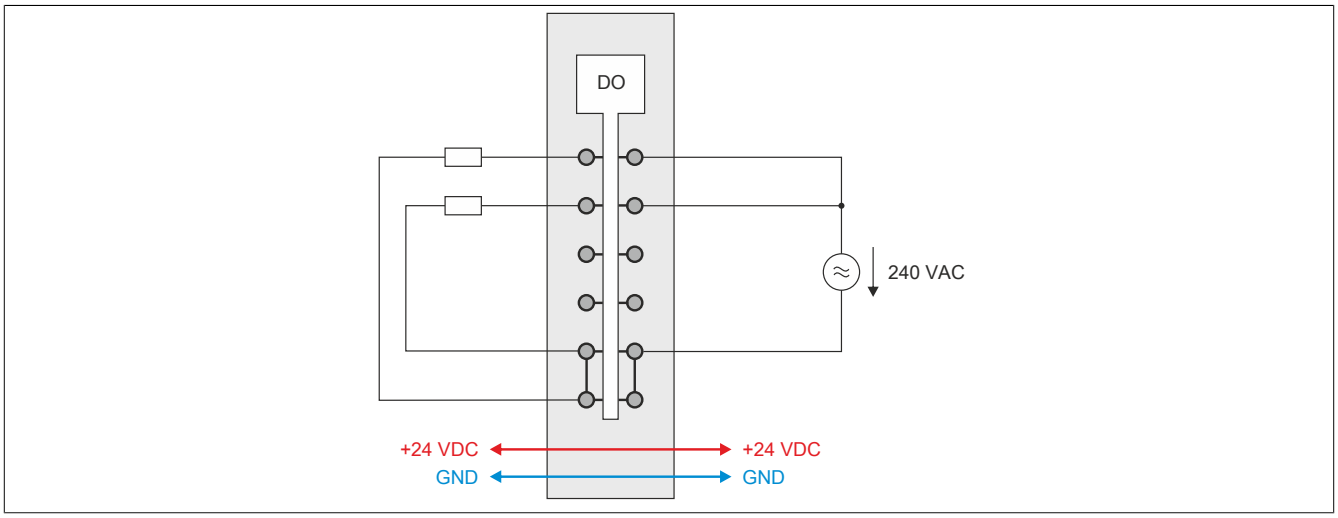
Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange		Output status of the corresponding digital output

4.15.16.6 Pinout

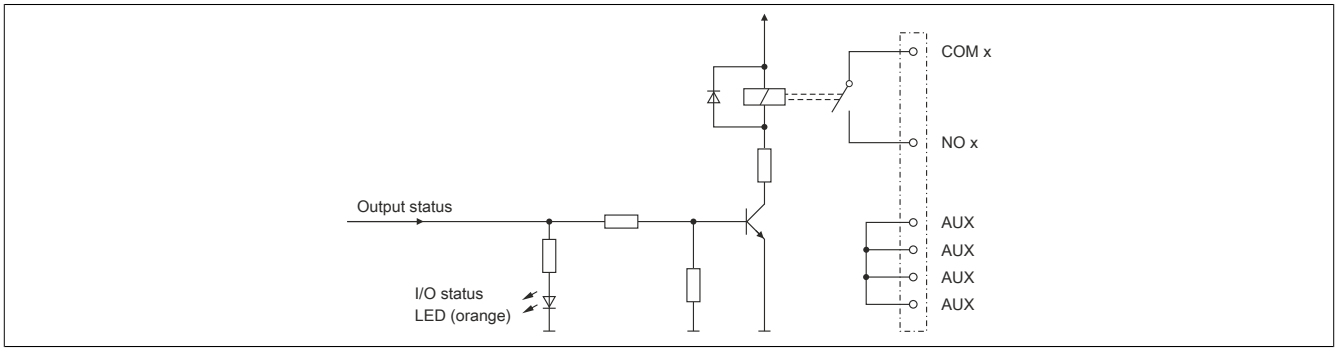
For easy wiring, 4 auxiliary contacts are available on the module starting with revision E0. They are connected together internally and can be loaded with a total of 10 A (see also section "Connection example").



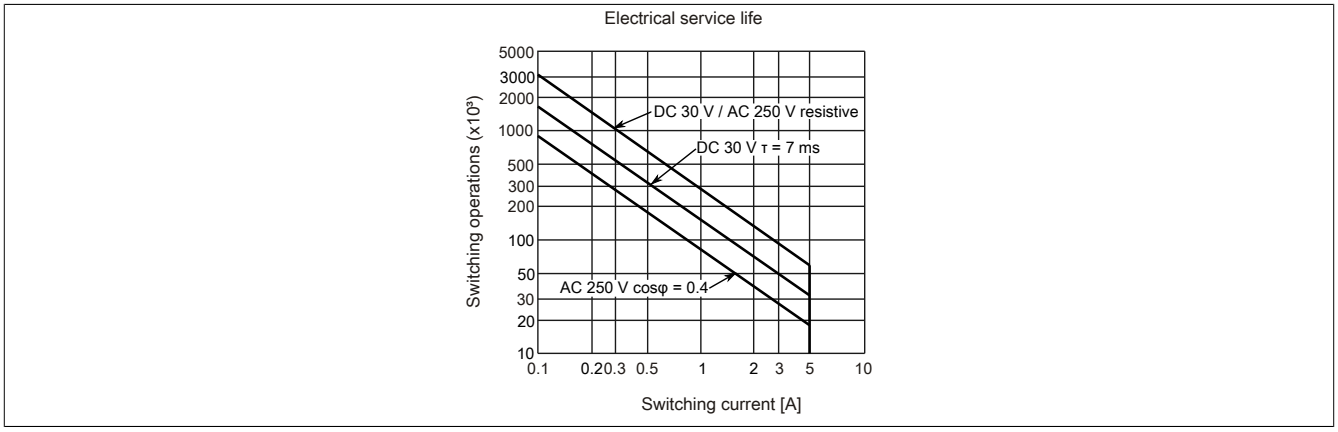
4.15.16.7 Connection example



4.15.16.8 Output circuit diagram



4.15.16.9 Electrical service life



4.15.16.10 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the maximal current per channel is limited to 4 A and maximal total current is limited to 8 A.

4.15.16.11 Register description

4.15.16.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.16.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.16.11.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 4	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.15.16.11.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.16.11.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.16.11.4.1 Switching state of digital outputs 1 to 4

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput04

The switching state of digital outputs 1 to 4 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 15	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
3	DigitalOutput04	0	Digital output 04 reset
		1	Digital output 04 set

4.15.16.11.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.16.11.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.17 X20(c)DO6321

4.15.17.1 General information

The module is equipped with 6 outputs for 1 or 2-wire connections. The X20 6-pin terminal block can be used for universal 1-line wiring. 2-line wiring can be implemented using the 12-pin terminal block. The X20DO6321 is designed for sink output wiring.

- 6 digital outputs
- Sink connection
- 2-wire connections
- 24 VDC for signal supply
- Integrated output protection
- 1-wire connection type with 6-pin terminal block

4.15.17.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.17.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO6321	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections	
X20cDO6321	X20 digital output module, coated, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 325: X20DO6321, X20cDO6321 - Order data

4.15.17.4 Technical data

Product ID	X20DO6321	X20cDO6321
Short description		
I/O module	6 digital outputs 24 VDC for 1- or 2-wire connections	
General information		
B&R ID code	0x1B99	0xE228
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	
Power consumption		
Bus	0.2 W	
Internal I/O	0.59 W	

Table 326: X20DO6321, X20cDO6321 - Technical data

Product ID	X20DO6321	X20cDO6321
Additional power dissipation caused by the actuators (resistive) [W] 1)	+0.18	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 2)	Yes	
KC	Yes	-
GOST-R	Yes	
Digital outputs		
Design	FET negative switching	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	0.5 A	
Total nominal current	3 A	
Connection type	1- or 2-wire connections	
Output circuit	Sink	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	75 µA	
$R_{DS(on)}$	120 mΩ	
Peak short circuit current	<7 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay		
0 -> 1	<300 µs	
1 -> 0	<300 µs	
Switching frequency		
Resistive load	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 326: X20DO6321, X20cDO6321 - Technical data

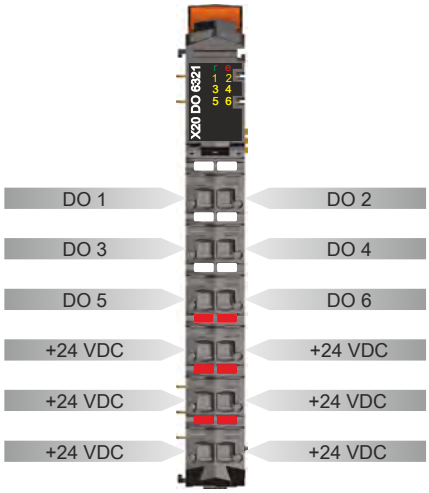
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.15.17.5 Status LEDs

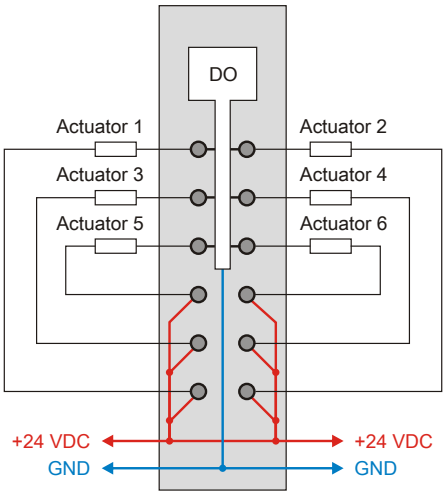
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Orange		Output status of the corresponding digital output

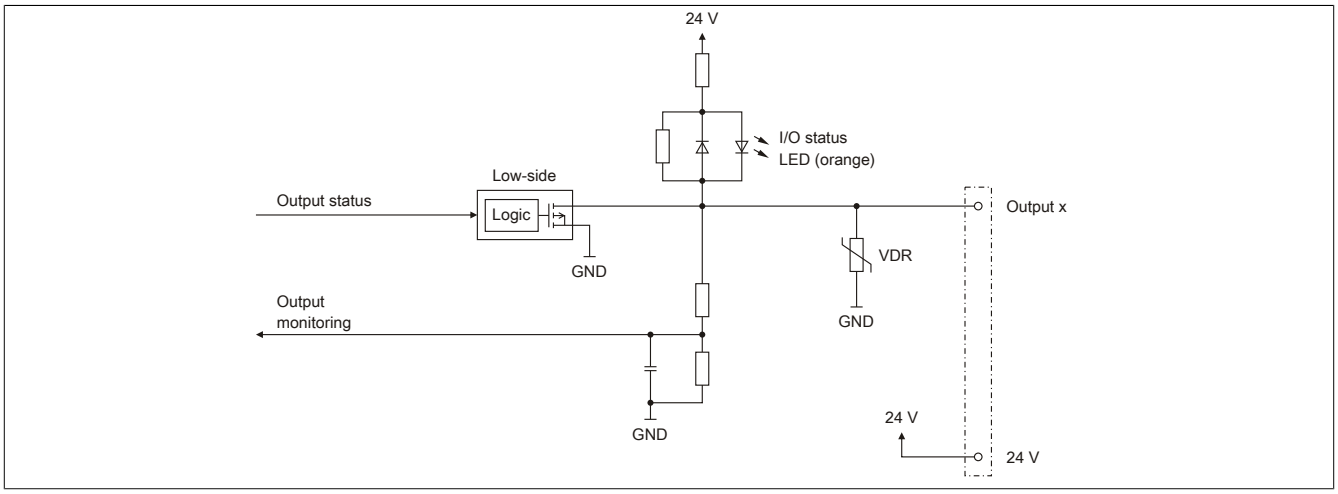
4.15.17.6 Pinout



4.15.17.7 Connection example

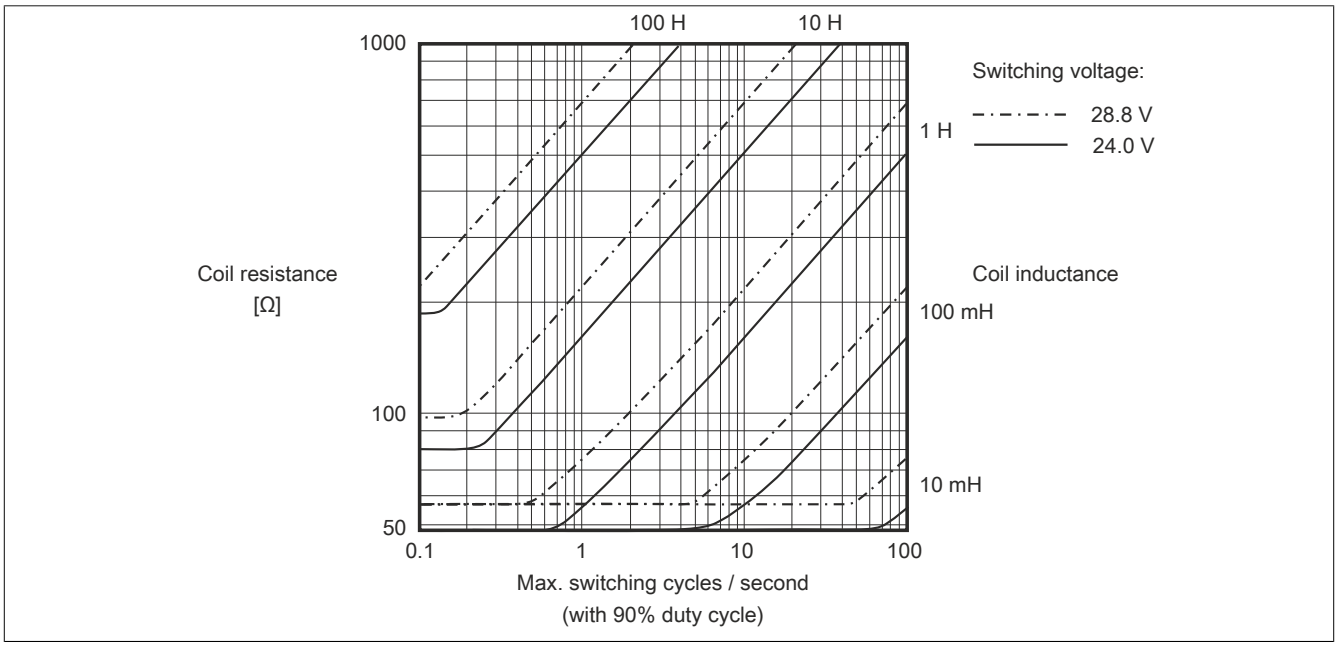


4.15.17.8 Output circuit diagram



4.15.17.9 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.17.10 Register description

4.15.17.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.17.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput06	Bit 5				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.17.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 6	USINT			•	
		DigitalOutput01	Bit 0				
			...				
		DigitalOutput06	Bit 5				
30	-	Status of digital outputs 1 to 6	USINT		•		
		StatusDigitalOutput01	Bit 0				
			...				
		StatusDigitalOutput06	Bit 5				

1) The offset specifies where the register is within the CAN object.

4.15.17.10.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.17.10.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.17.10.4.1 Switching state of digital outputs 1 to 6

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput06

The switching state of digital outputs 1 to 6 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
5	DigitalOutput06	0	Digital output 06 reset
		1	Digital output 06 set

4.15.17.10.5 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.17.10.5.1 Status of digital outputs 1 to 6

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput06

The status of digital outputs 1 to 6 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
5	StatusDigitalOutput06	0	Channel 06: No error
		1	Channel 06: Short circuit or overload

4.15.17.10.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.17.10.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.18 X20(c)DO6322

4.15.18.1 General information

The module is equipped with 6 outputs for 1 or 2-wire connections. The X20 6-pin terminal block can be used for universal 1-line wiring. 2-line wiring can be implemented using the 12-pin terminal block. The module is designed for source output wiring.

- 6 digital outputs
- Source connection
- 2-wire connections
- GND for signal supply
- Integrated output protection
- 1-wire connection type with 6-pin terminal block
- OSP mode

4.15.18.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.18.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO6322	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections	
X20cDO6322	X20 digital output module, coated, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 327: X20DO6322, X20cDO6322 - Order data

4.15.18.4 Technical data

Product ID	X20DO6322	X20cDO6322
Short description		
I/O module	6 digital outputs 24 VDC for 1- or 2-wire connections	
General information		
B&R ID code	0x1B98	0xE229
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	

Table 328: X20DO6322, X20cDO6322 - Technical data

Product ID	X20DO6322	X20cDO6322
Power consumption		
Bus	0.18 W	
Internal I/O	0.71 W	
Additional power dissipation caused by the actuators (resistive) [W] 1)	+0.31	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 2)	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Digital outputs		
Design	FET positive switching	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15% / +20%	
Nominal output current	0.5 A	
Total nominal current	3 A	
Connection type	1- or 2-wire connections	
Output circuit	Source	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	5 µA	
$R_{DS(on)}$	210 mΩ	
Max. continuous current	3 A	
Peak short circuit current	<12 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay 3)		
0 -> 1	<300 µs	
1 -> 0	<300 µs	
Switching frequency		
Resistive load 3)	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 328: X20DO6322, X20cDO6322 - Technical data

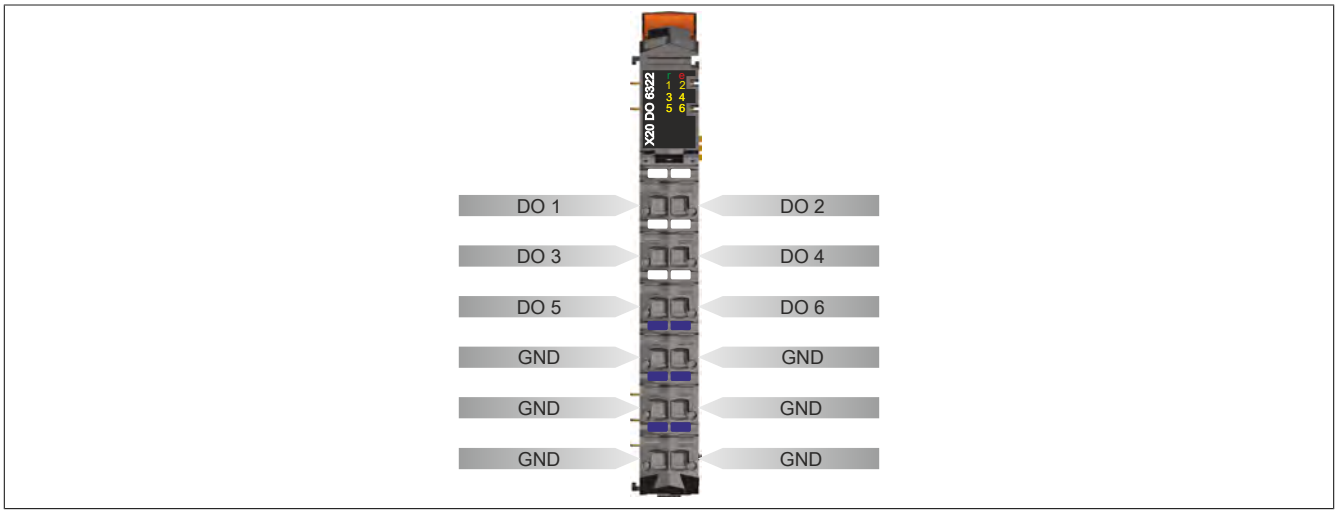
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) At loads ≤ 1 kΩ

4.15.18.5 Status LEDs

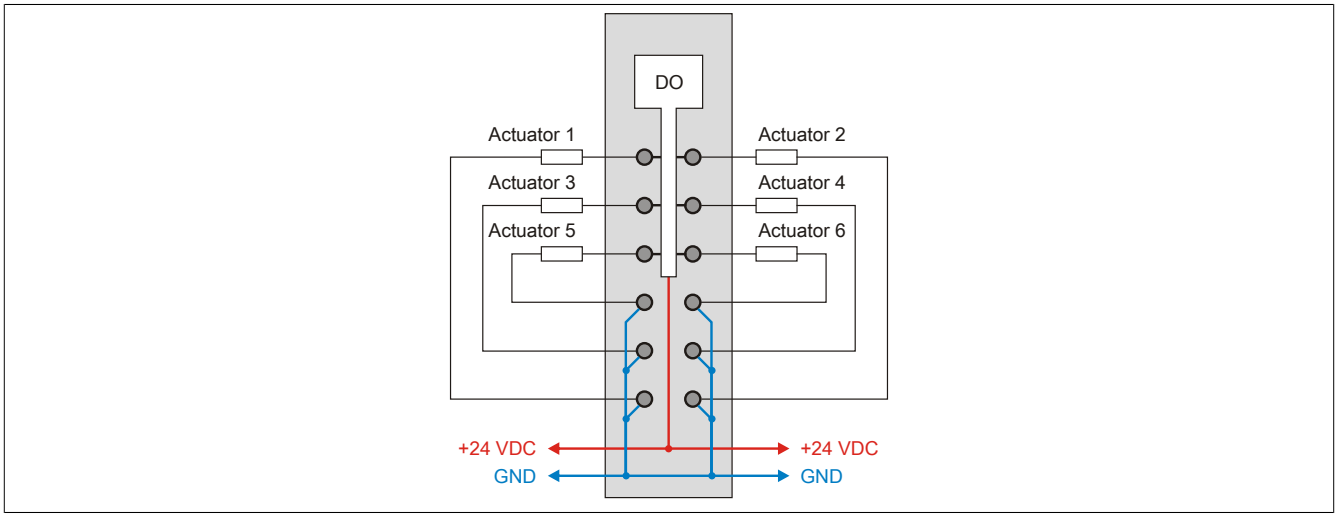
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP state
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Orange		Output status of the corresponding digital output

4.15.18.6 Pinout



4.15.18.7 Connection example



Caution!

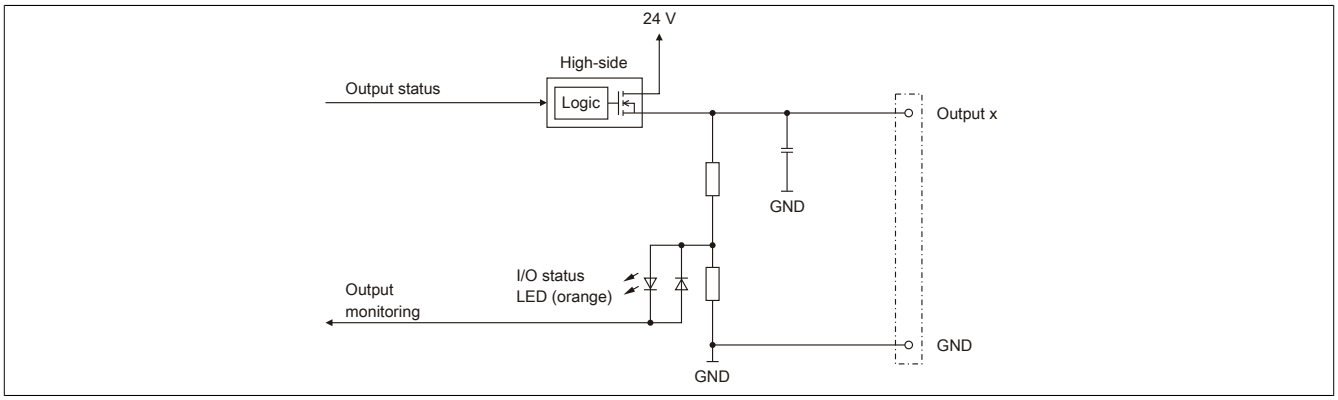
If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

Therefore sufficient cable cross sections or external safety measures must be used.

4.15.18.8 OSP hardware requirements

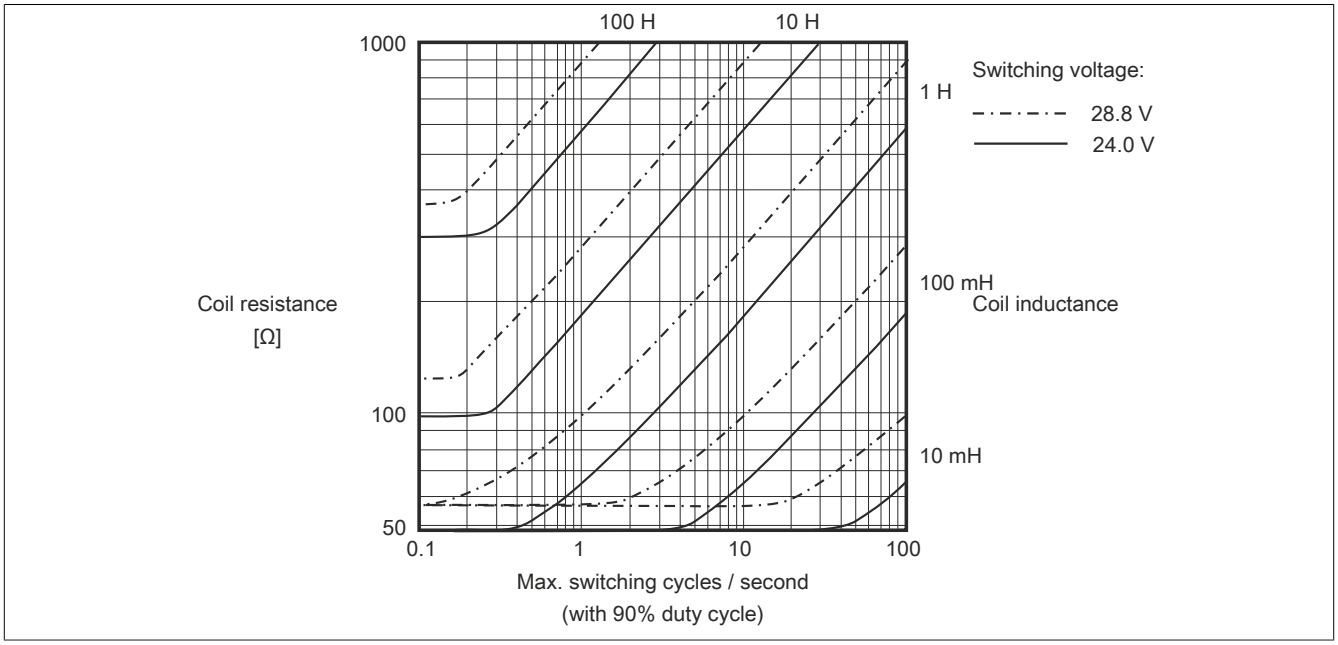
In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.18.9 Output circuit diagram



4.15.18.10 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.18.11 Register description

4.15.18.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.18.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput06	Bit 5				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.18.11.3 Function model 1 - OSP

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 6	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				
30	1	Status of digital outputs 1 to 6	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput06	Bit 5				
34	1	Activating the OSP output in the module	USINT			•	
		OSPValid	Bit 0				
32	-	CfgOSPMode	USINT				•
36	-	CfgOSPValue	USINT				•

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.18.11.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 6	USINT			•	
		DigitalOutput01	Bit 0				
			...				
		DigitalOutput06	Bit 5				
30	-	Status of digital outputs 1 to 6	USINT		•		
		StatusDigitalOutput01	Bit 0				
			...				
		StatusDigitalOutput06	Bit 5				

1) The offset specifies where the register is within the CAN object.

4.15.18.11.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.18.11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.18.11.5.1 Switching state of digital outputs 1 to 6

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput06

The switching state of digital outputs 1 to 6 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
5	DigitalOutput06	0	Digital output 06 reset
		1	Digital output 06 set

4.15.18.11.6 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.18.11.6.1 Status of digital outputs 1 to 6

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput06

The status of digital outputs 1 to 6 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
5	StatusDigitalOutput06	0	Channel 06: No error
		1	Channel 06: Short circuit or overload

4.15.18.11.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.18.11.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.18.11.7.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.18.11.7.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.18.11.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.18.11.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.19 X20DO6325

4.15.19.1 General information

The module is equipped with six outputs for 1 or 2-wire connections with diagnostic functions. The X20 6-pin terminal block can be used for universal 1-line wiring. Two-line wiring can be implemented using the 12-pin terminal block. The outputs on the module are designed for source connections.

- 6 digital outputs
- Source connection
- 2-wire connections
- GND for signal supply
- Integrated output protection
- 1-wire connection type with 6-pin terminal block
- Diagnostic functions (open line, short circuit and overload/overtemperature)
- OSP mode

4.15.19.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO6325	X20 digital output module, 6 outputs, 24 VDC, 0.5 A, source, open line and overload detection, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 329: X20DO6325 - Order data

4.15.19.3 Technical data

Product ID	X20DO6325
Short description	
I/O module	6 digital outputs 24 VDC for 1- or 2-wire connections with a diagnostics function
General information	
B&R ID code	0xE284
Status indicators	I/O function by channel, diagnostics by channel, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Status outputs	Yes, using status LED and software
Diagnostic outputs	Yes, using status LED and software
Power consumption	
Bus	0.15 W
Internal I/O	0.4 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	Max. 0.225 W
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2)]	Yes
GOST-R	Yes
Digital outputs	
Design	FET positive switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	3 A

Table 330: X20DO6325 - Technical data

Product ID	X20DO6325
Connection type	1- or 2-wire connections
Output circuit	Source
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")
Diagnostic status	
Open line	Current is <1 mA (typ.): Detected if the output is OFF, delay approx. 10 ms
Short circuit to 24 VDC	Detected if the output is OFF, delay approx. 10 ms
Short circuit to GND	Detected if the output is ON, delay approx. 10 ms
Overload/overtemperature	Detected if the output is ON, delay approx. 10 ms
Leakage current when switched off	<160 µA
$R_{DS(on)}$	150 mΩ
Peak short circuit current	<40 A
Switching on after overload or short circuit cutoff	Depends on the module temperature
Switching delay [3]	
0 -> 1	<100 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load [3]	Max. 2000 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	45 to 52 VDC
Isolation voltage between channel and bus	510 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 330: X20DO6325 - Technical data

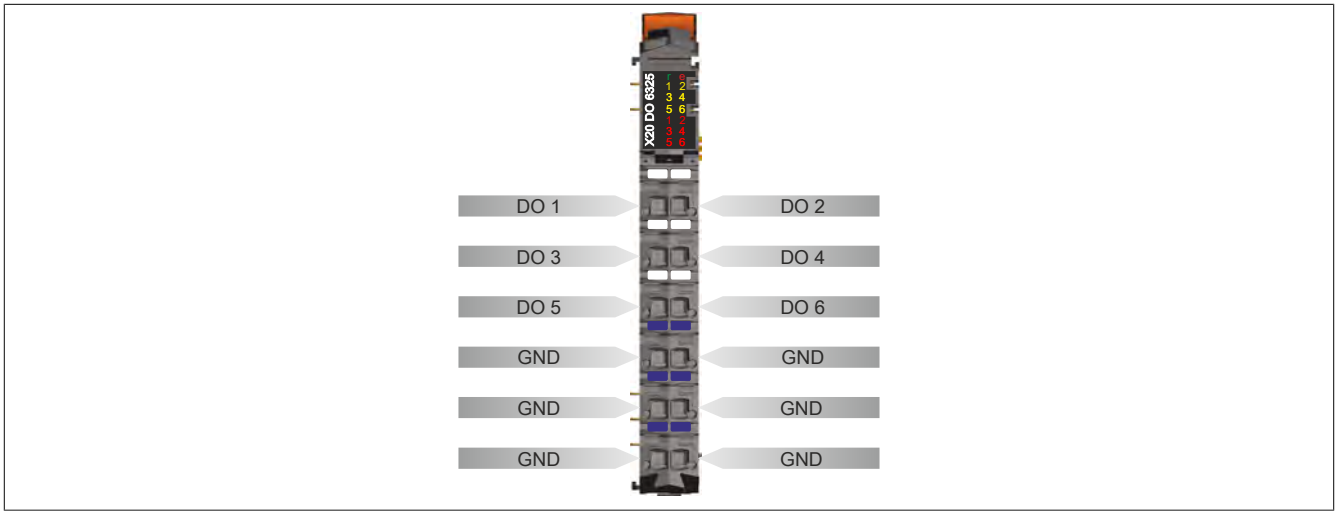
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) At loads ≤ 1 kΩ

4.15.19.4 LED status indicators

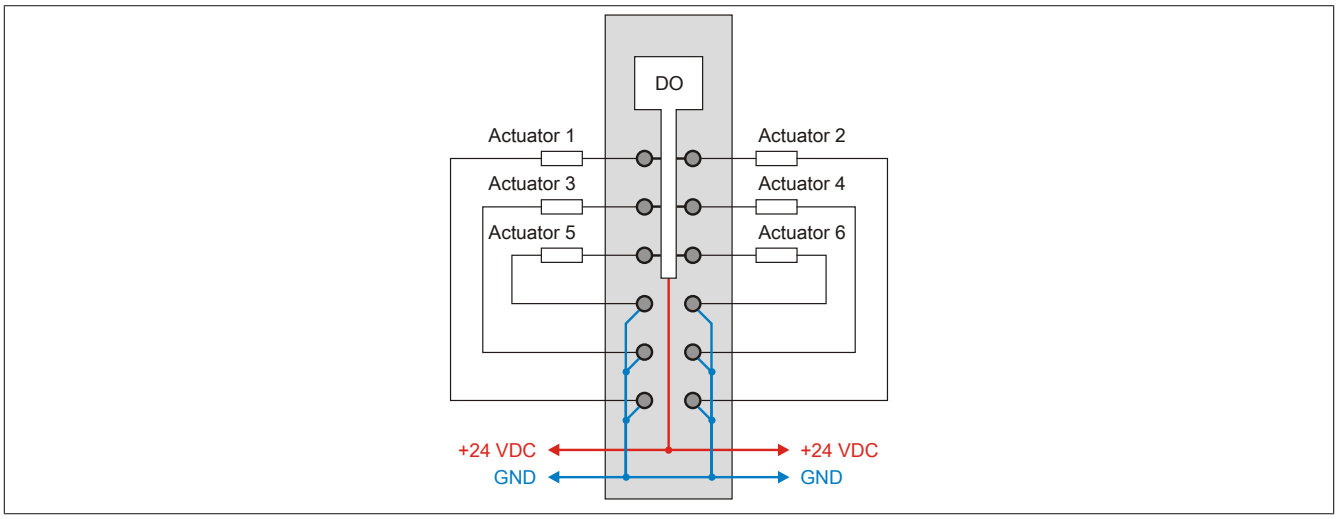
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP mode
	e	Red	Off	No power to module or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	I/O supply is outside valid range.
	e + r	Red on / Green single flash		Invalid firmware
	Channel 1 - 6	Orange		Output status of the corresponding digital output
	Diagnostics 1 - 6	Red		Monitoring of the corresponding digital output was tripped (short circuit, open line or overload)

4.15.19.5 Pinout



4.15.19.6 Connection example



Caution!

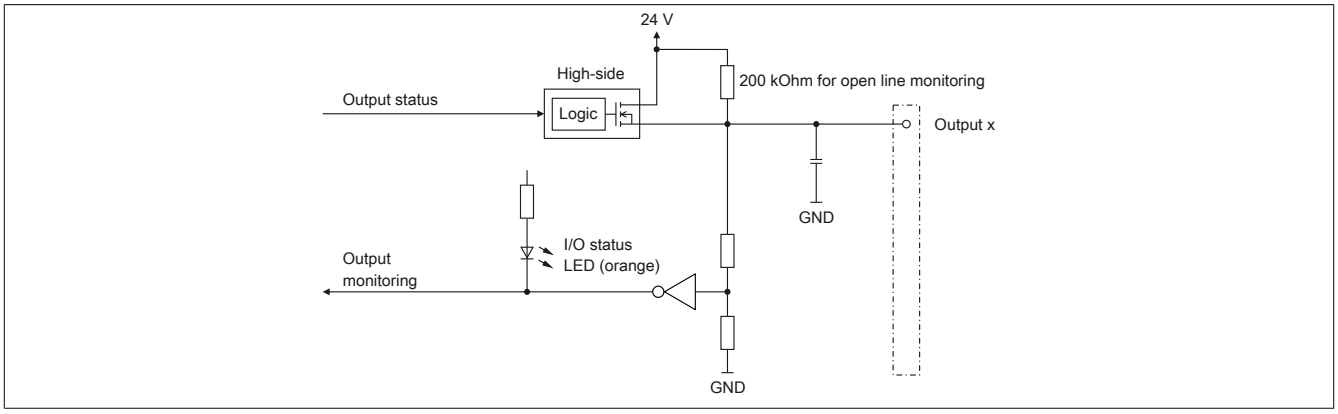
If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

Therefore sufficient cable cross sections or external safety measures must be used.

4.15.19.7 OSP hardware requirements

In order to best use OSP mode, make sure when creating the application that the output module and CPU have separate power supplies.

4.15.19.8 Output circuit diagram



4.15.19.9 Open line detection

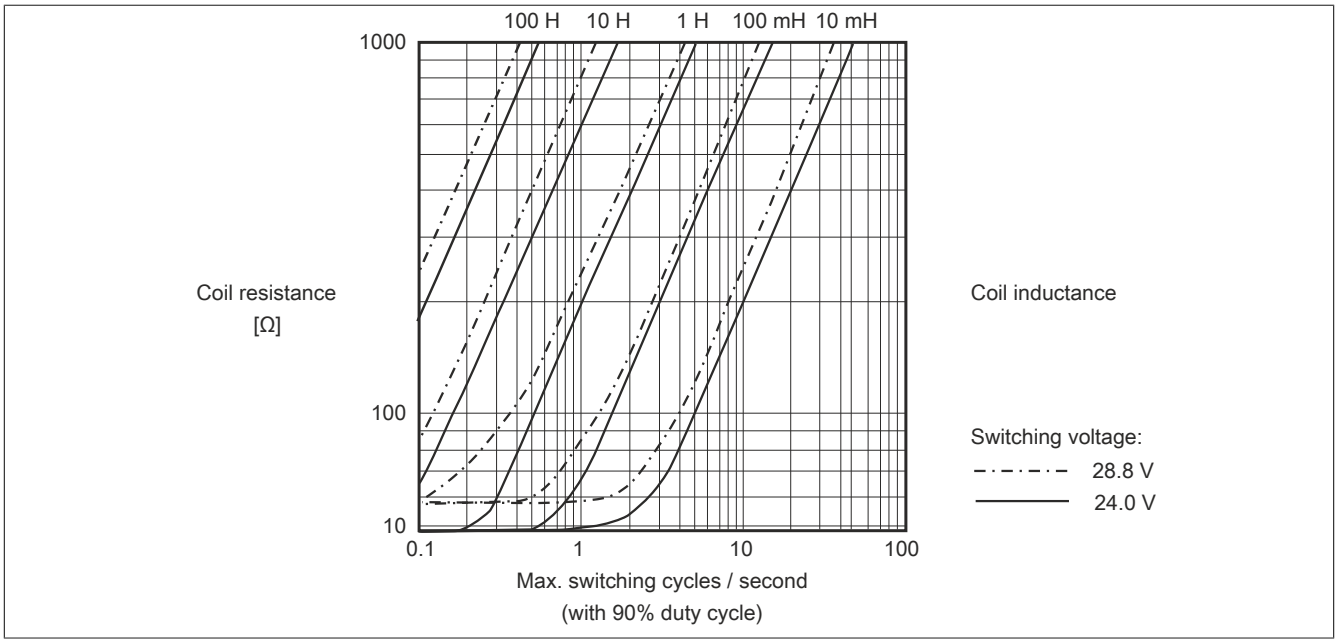
Each output is equipped with an internal 200 kOhm resistor to 24 V for open line detection.

If the charging resistance at the terminal is greater than 25 to 100 kOhm (tolerance range) an open line is therefore detected at 24 V. When switched on, this corresponds to a current of 0.2 to 1 mA with all tolerances taken into consideration.

Supply voltage	Min. load	Max. load	Corresponds to load current when ON
24 V	100 kOhm	25 kOhm	0.2 to 1 mA

4.15.19.10 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.19.11 Register description

4.15.19.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.19.11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
2	DigitalOutput	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput06	Bit 5				
4	CfgBwStatus	USINT				•
28	StatusInput01	USINT	•			
	DigitalStatusGnd01	Bit 0				
	...	...				
	DigitalStatusGnd06	Bit 5				
29	StatusInput02	USINT	•			
	DigitalStatusVcc01	Bit 0				
	...	...				
	DigitalStatusVcc06	Bit 5				
30	StatusInput03	USINT	•			
	DigitalStatusBw01	Bit 0				
	...	...				
	DigitalStatusBw06	Bit 5				
31	StatusInput04	USINT	•			
	DigitalStatusSum01	Bit 0				
	...	...				
	DigitalStatusSum06	Bit 5				
	PowerSupply01	Bit 7				

4.15.19.11.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
2	Switching state of digital outputs 1 to 6	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput06	Bit 5				
4	CfgBwStatus	USINT				•
28	Short circuit to GND and overtemperature	USINT	•			
	DigitalStatusGnd01	Bit 0				
	...	...				
	DigitalStatusGnd06	Bit 5				
29	Short circuit to voltage	USINT	•			
	DigitalStatusVcc01	Bit 0				
	...	...				
	DigitalStatusVcc06	Bit 5				
30	Open line	USINT	•			
	DigitalStatusBw01	Bit 0				
	...	...				
	DigitalStatusBw06	Bit 5				
31	Cumulative status	USINT	•			
	DigitalStatusSum01	Bit 0				
	...	...				
	DigitalStatusSum06	Bit 5				
	PowerSupply01	Bit 7				
34	Activating the OSP output in the module	USINT			•	
	OSPValid	Bit 0				
32	CfgOSPMode	USINT				•
36	CfgOSPValue	USINT			•	

4.15.19.11.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
2	2	Switching state of digital outputs 1 to 6	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				
4	4	CfgBwStatus	USINT				•
28	28	Short circuit to GND and overtemperature	USINT	•			
		DigitalStatusGnd01	Bit 0				
		...	...				
		DigitalStatusGnd06	Bit 5				
29	29	Short circuit to voltage	USINT	•			
		DigitalStatusVcc01	Bit 0				
		...	...				
		DigitalStatusVcc06	Bit 5				
30	30	Open line	USINT	•			
		DigitalStatusBw01	Bit 0				
		...	...				
		DigitalStatusBw06	Bit 5				
31	31	Cumulative status	USINT	•			
		DigitalStatusSum01	Bit 0				
		...	...				
		DigitalStatusSum06	Bit 5				
		PowerSupply01	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.15.19.11.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.19.11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.19.11.5.1 Switching state of digital outputs 1 to 6

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput06

The switching state of digital outputs 1 to 6 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
5	DigitalOutput06	0	Digital output 06 reset
		1	Digital output 06 set

4.15.19.11.6 Digital output status

The status of the outputs is checked every 4 ms. To suppress disturbances on the feedback inputs, two readings are compared.

The hardware diagnostics recognize the following states:

- Short circuit to ground GND (when output is ON)
- Short circuit to 24 VDC (when output is OFF)
- Open line (when output is OFF)
- Overtemperature / overload

The error is logged in the corresponding status registers and in the cumulative status register.

An open line error is also indicated by the corresponding LED. The LED indicator can be disabled so that an open (unused) channel does not constantly indicate an error.

4.15.19.11.6.1 Enabling the status LED

Name:
CfgBwStatus

For each output there is a corresponding enable bit. In this register, the bit can be set to define whether or not the status LED should be used to indicate an open line error. This allows the LED to be disabled for unused channels. In the bus controller function model the default value is 0xBF.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel 01	0	Open line indicator 01 disabled
		1	Open line indicator 01 enabled
...		...	
5	Channel 06	0	Open line indicator 06 disabled
		1	Open line indicator 06 enabled
6	Reserved	0	
7	PowerSupply01	0	No error status indicators
		1	Monitor supply voltage

4.15.19.11.6.2 Short circuit to GND and overtemperature

Name:
StatusInput01
DigitalStatusGnd01 to DigitalStatusGnd06

In this register, a short circuit or overtemperature error can be indicated by setting the corresponding channel bit. It is not possible to differentiate between short circuit to GND and overload/overtemperature.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalStatusGnd01" through "DigitalStatusGnd06") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalStatusGnd01	0	No error
		1	Channel 1: Short circuit or overload
...		...	
5	DigitalStatusGnd06	0	No error
		1	Channel 6: Short circuit or overload
6 - 7	Reserved	0	

4.15.19.11.6.3 Short circuit to voltage

Name:
StatusInput02
DigitalStatusVcc01 to DigitalStatusVcc06

In this register, a short circuit can be indicated by setting the corresponding channel bit.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalStatusVcc01" through "DigitalStatusVcc06") or whether this register should be displayed as an individual USINT data point ("StatusInput02").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalStatusVcc01	0	No error
		1	Channel 1: Short circuit to voltage
...		...	
5	DigitalStatusVcc06	0	No error
		1	Channel 6: Short circuit to voltage
6 - 7	Reserved	0	

4.15.19.11.6.4 Open line

Name:
StatusInput03
DigitalStatusBw01 to DigitalStatusBw06

In this register, an open line can be indicated by setting the corresponding channel bit.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalStatusBw01" through "DigitalStatusBw06") or whether this register should be displayed as an individual USINT data point ("StatusInput03").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalStatusBw01	0	No error
		1	Channel 1: Open line
...		...	
5	DigitalStatusBw06	0	No error
		1	Channel 6: Open line
6 - 7	Reserved	0	

4.15.19.11.6.5 Cumulative status

Name:
StatusInput04
DigitalStatusSum01 to DigitalStatusSum06
PowerSupply01

Every error found in the other status registers is also shown in this register. This provides an easy way to check whether any errors have occurred.
If the I/O supply fails, Bit 7 is set and all status bits in the other status registers are reset to 0.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points ("DigitalStatusSum01 through DigitalStatusSum06","PowerSupply01") in the AS I/O mapping or whether this register should be displayed as an individual USINT data point ("StatusInput04").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalStatusSum01	0	No error
		1	Channel 1: Error occurred
...		...	
5	DigitalStatusSum06	0	No error
		1	Channel 6: Error occurred
6	Reserved	0	
7	PowerSupply01	0	No error
		1	Pending supply voltage error

4.15.19.11.7 "OSP" function model

In the "OSP" function model (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as communication between the module and master is interrupted.

Functionality

The user can choose between two OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value as validly recognized output state.

When selecting the mode, "Replace with static value" a plausible output value must be entered in the corresponding value register. If an OSP event occurs, this value will be output instead of the value currently requested by the task.

4.15.19.11.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the responsible task in the master CPU. However, output still occurs according to the configuration of the OSP replacement value.

4.15.19.11.7.2 Setting the OSP mode

Name:
CfgOSPMode

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

4.15.19.11.7.3 Define the OSP digital output value

Name:
CfgOSPValue

This register contains the digital output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0		0 or 1	OSP output value for channel DigitalOutput00
...		...	
x		0 or 1	OSP output value for channel DigitalOutput0x

Warning!

The "OSPValue" is not accepted by the module until the "OSPValid" bit has been set in the module.

4.15.19.11.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.15.19.11.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.20 X20DO6529

4.15.20.1 General information

The module is equipped with 6 relay outputs.

- 6 digital outputs
- Relay module for 115 VAC
- 6 normally open contacts
- Single-channel isolated outputs

> **Danger!**
>
> **Risk of electric shock!**
>
> **The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.**

4.15.20.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO6529	X20 digital output module, 6 relays, normally open contacts, 115 VAC / 0.5 A, 30 VDC / 1 A	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 331: X20DO6529 - Order data

4.15.20.3 Technical data

Product ID	X20DO6529
Short description	
I/O module	6 digital outputs 30 VDC / 115 VAC, outputs are single-channel isolated
General information	
B&R ID code	0x2019
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED
Power consumption	
Bus	1.1 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+0.45
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes

Table 332: X20DO6529 - Technical data

Product ID	X20DO6529
Digital outputs	
Design	Relay / Normally open contact Channels are single-channel isolated
Nominal voltage	30 VDC / 115 VAC
Max. voltage	125 VAC
Switching voltage	Max. 110 VDC / 125 VAC
Rated frequency	DC / 45 to 63 Hz
Nominal output current	1 A at 30 VDC / 0.5 A at 115 VAC
Total nominal current	6 A at 30 VDC / 3 A at 115 VAC
Actuator supply	External
Starting current	Max. 2 A (per channel)
Contact resistance	75 mΩ at 6 VDC / 1A
Switching delay	
0 -> 1	≤4 ms
1 -> 0	≤4 ms
Isolation voltage	
Contact - Contact	Tested at 1000 VAC
Contact - Coil	Tested at 1500 VAC
Service life	
Electrical [3]	Min. 100 x 10^3 ops.
Mechanical	Min. 50 x 10^6 ops. (3 Hz)
Switching capacity	
Minimum	0.01 mA / 10 mV DC
Maximum	30 W / 62.5 VA
Protective circuit	
Internal	None
External	
AC	RC combination or VDR
DC	Inverse diode, RC combination or VDR
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 332: X20DO6529 - Technical data

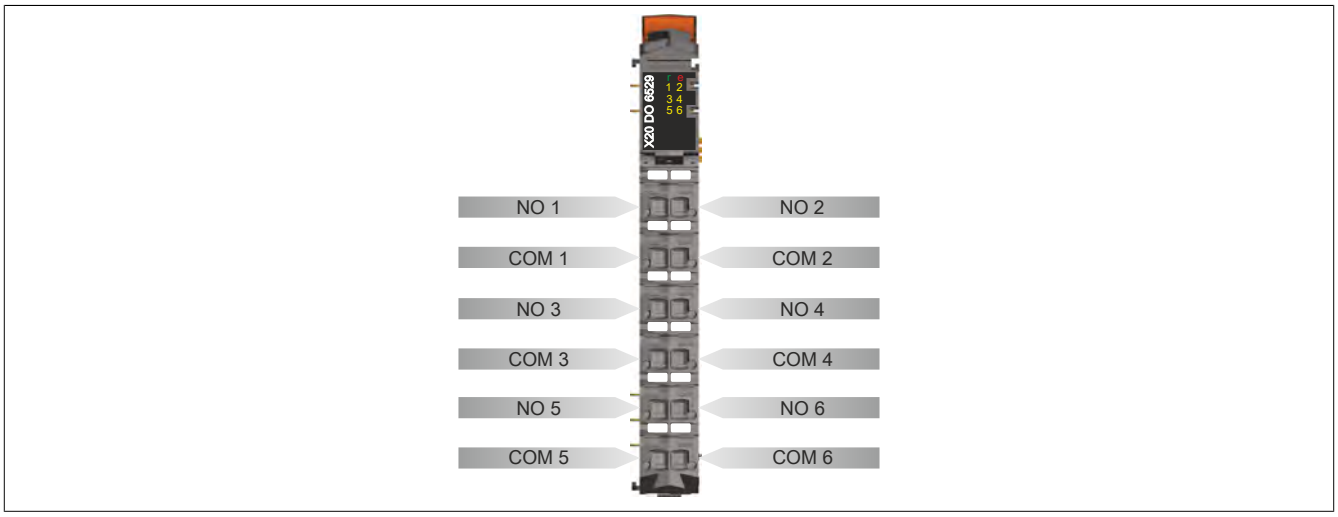
1) Number of outputs x Contact resistance x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
Ta max.: See environmental conditions
3) With a resistive load. See also section "Electrical service life"

4.15.20.4 Status LEDs

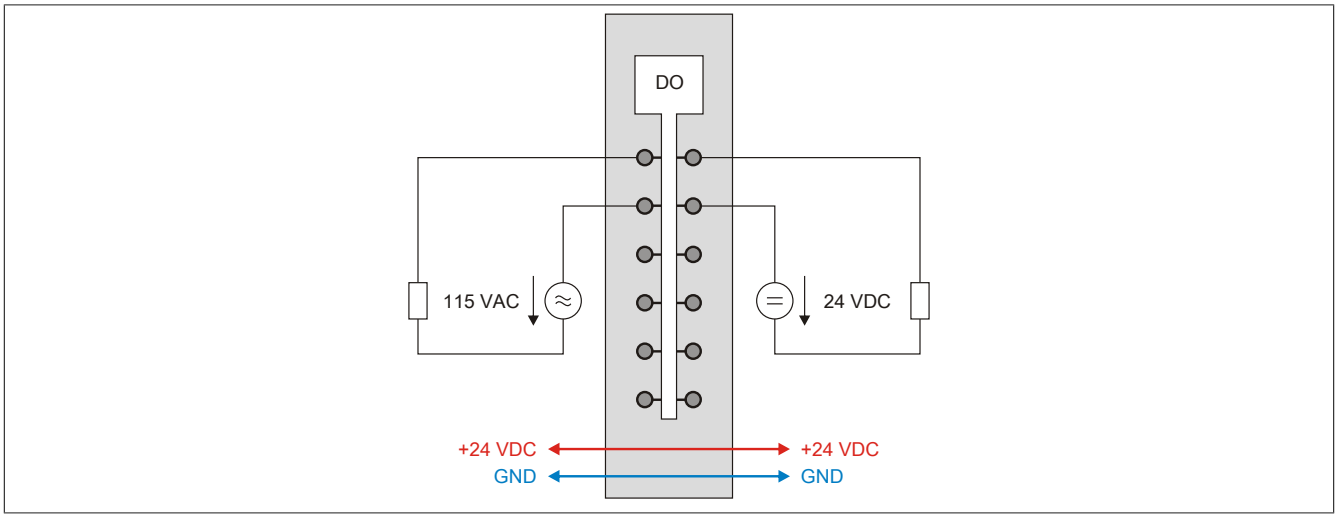
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Orange		Output status of the corresponding digital output

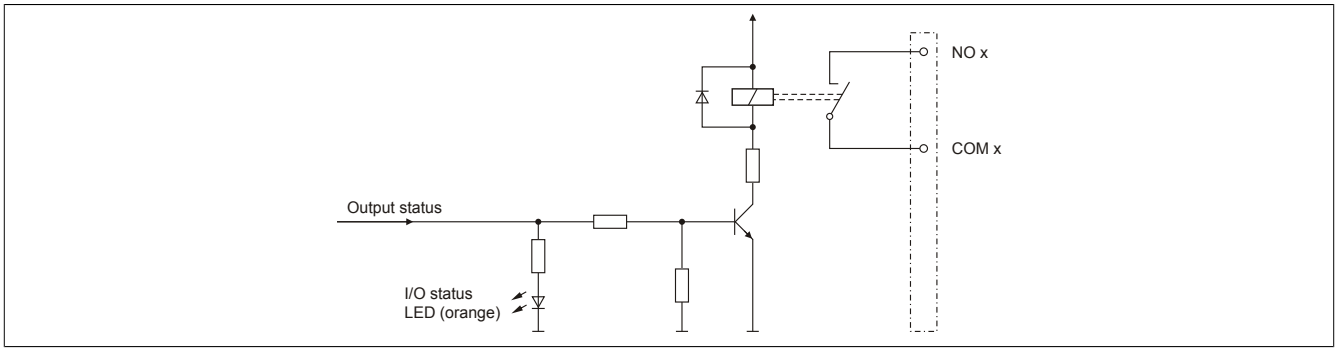
4.15.20.5 Pinout



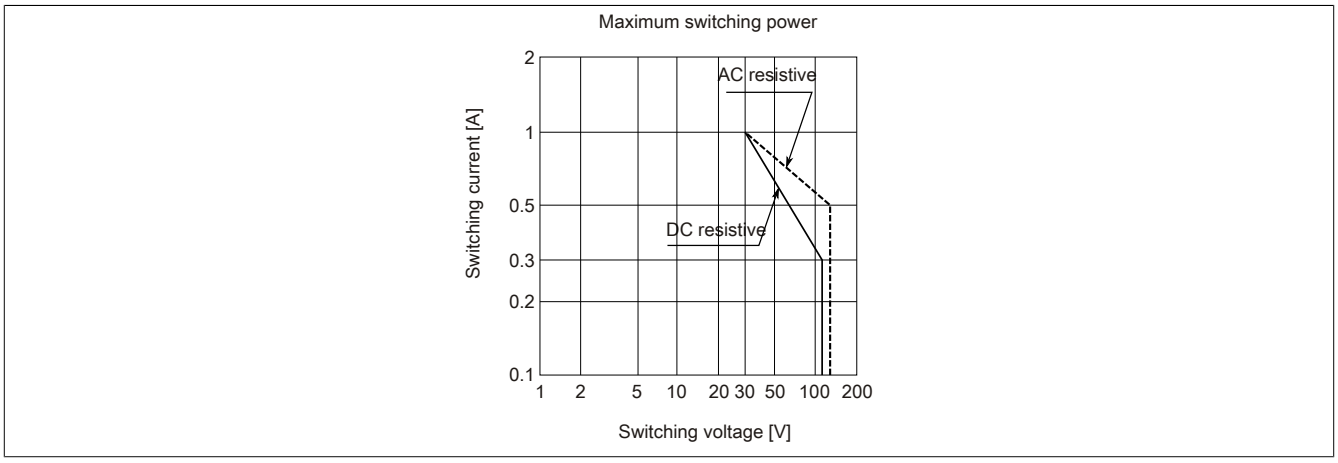
4.15.20.6 Connection example



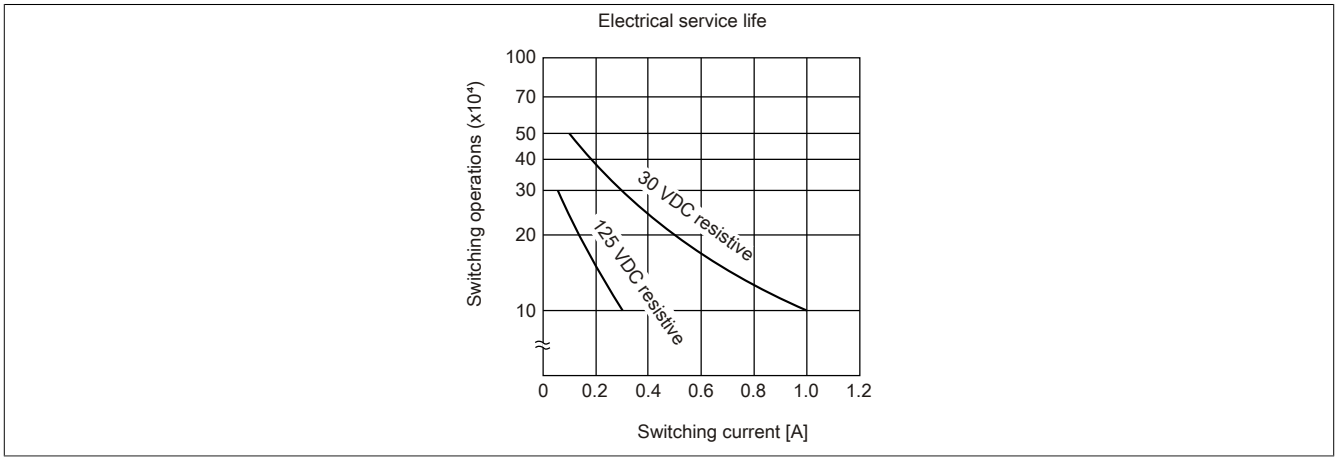
4.15.20.7 Output circuit diagram



4.15.20.8 Maximum switching power



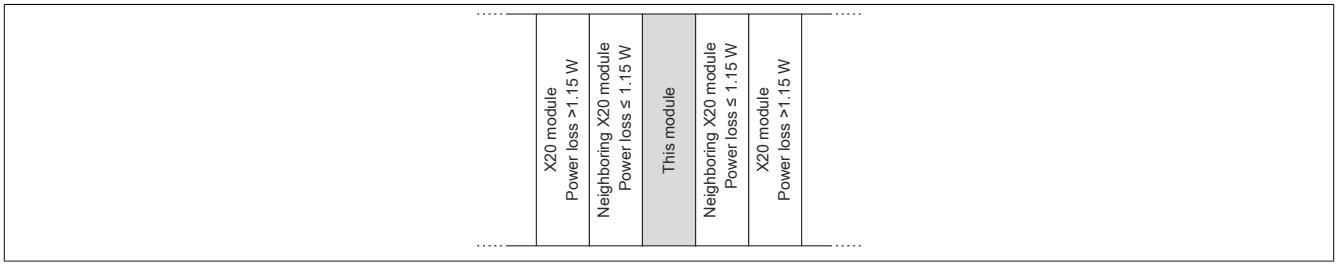
4.15.20.9 Electrical service life



4.15.20.10 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.15.20.11 Register description

4.15.20.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.20.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.20.11.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 6	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				

1) The offset specifies where the register is within the CAN object.

4.15.20.11.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.20.11.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.20.11.4.1 Switching state of digital outputs 1 to 6

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput06

The switching state of digital outputs 1 to 6 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
5	DigitalOutput06	0	Digital output 06 reset
		1	Digital output 06 set

4.15.20.11.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.20.11.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.21 X20(c)DO6639

4.15.21.1 General information

The module is equipped with 6 relay outputs.

- 6 digital outputs
- Relay module for 240 VAC / 30 VDC
- Switching current 2 A
- 6 normally open contacts
- Single-channel isolated outputs

> **Danger!**
>
> **Risk of electric shock!**
>
> **The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.**

4.15.21.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

> **For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.**

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.21.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO6639	X20 digital output module, 6 relays, normally open contacts, 240 VAC / 2 A, 30 VDC / 2 A	
X20cDO6639	X20 digital output module, coated, 6 relays, normally open contacts, 240 VAC / 2 A, 30 VDC / 2 A	
	Required accessories	
	Bus modules	
X20BM12	X20 bus module, 240 VDC keyed, internal I/O supply continuous	
X20cBM12	X20 bus module, coated, 240 VAC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 333: X20DO6639, X20cDO6639 - Order data

4.15.21.4 Technical data

Product ID	X20DO6639	X20cDO6639
Short description		
I/O module	6 digital outputs 30 VDC / 240 VAC, outputs are single-channel isolated	
General information		
B&R ID code	0xDF50	0xE22A
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED	
Outputs	Yes, using status LED	
Power consumption		
Bus	1 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W] 1)	+0.36	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	-	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 2)	Yes	
GL	Yes	
GOST-R	Yes	
Digital outputs		
Design	Relay / Normally open contact Channels are single-channel isolated	
Nominal voltage	30 VDC / 240 VAC	
Max. voltage	264 VAC	
Switching voltage	Max. 110 VDC / 264 VAC	
Rated frequency	DC / 45 to 63 Hz	
Nominal output current	2 A at 30 VDC / 2 A at 240 VAC	
Total nominal current	10 A at 30 VDC / 10 A at 240 VAC	
Actuator supply	External	
Contact resistance	Max. 100 mΩ	
Switching delay		
0 -> 1	≤10 ms	
1 -> 0	≤10 ms	
Isolation voltage		
Contact - Contact	Tested at 750 VAC	
Contact - Coil	Tested at 2300 VAC	
Service life		
Electrical 3)	Min. 120 x 10^3 ops. (at 2 A / 240 VAC)	
Mechanical	Min. 2 x 10^7 ops.	
Switching capacity		
Minimum	0.05 W DC / 2.4 W AC	
Maximum	60 W DC / 480 W AC	
Total power of all channels		
AC	3000 W	
DC	360 W	
Protective circuit		
Internal	None	
External		
AC	RC combination or VDR	
DC	Inverse diode, RC combination or VDR	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 334: X20DO6639, X20cDO6639 - Technical data

Product ID	X20DO6639	X20cDO6639
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB32 terminal block separately, Order 1x X20BM12 bus module separately	Order 1x X20TB32 terminal block separately, Order 1x X20cBM12 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 334: X20DO6639, X20cDO6639 - Technical data

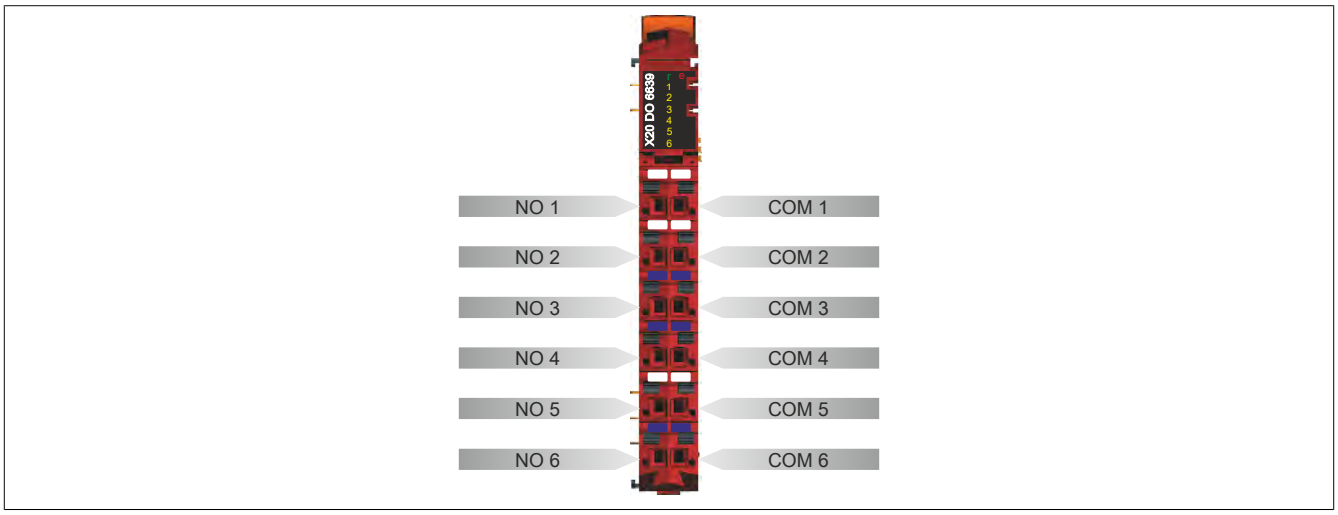
1) Number of outputs x Contact resistance x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) With a resistive load. See also section "Electrical service life"

4.15.21.5 Status LEDs

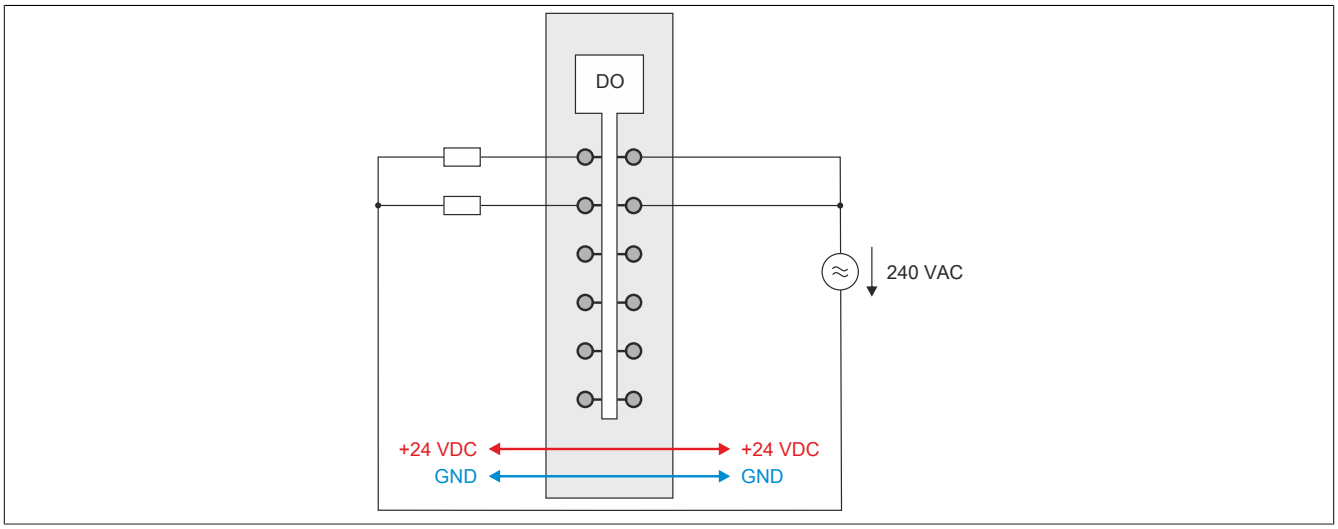
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Orange		Output status of the corresponding digital output

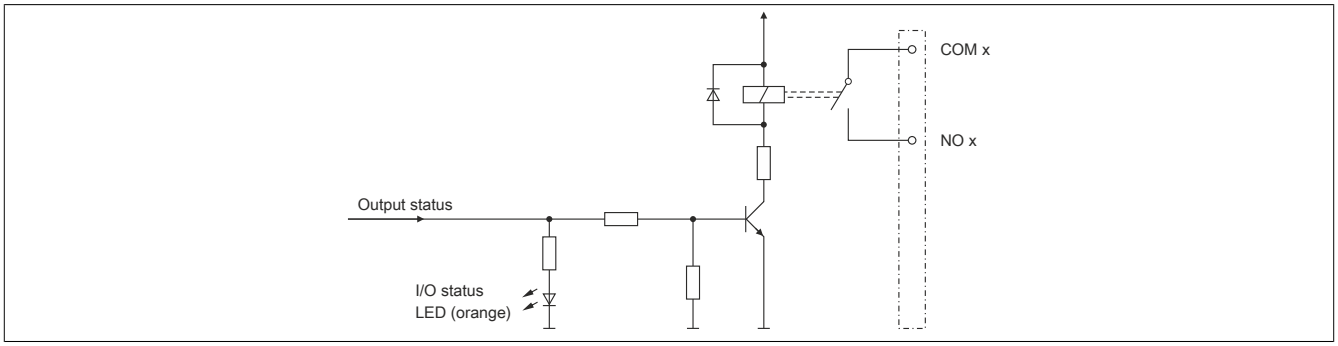
4.15.21.6 Pinout



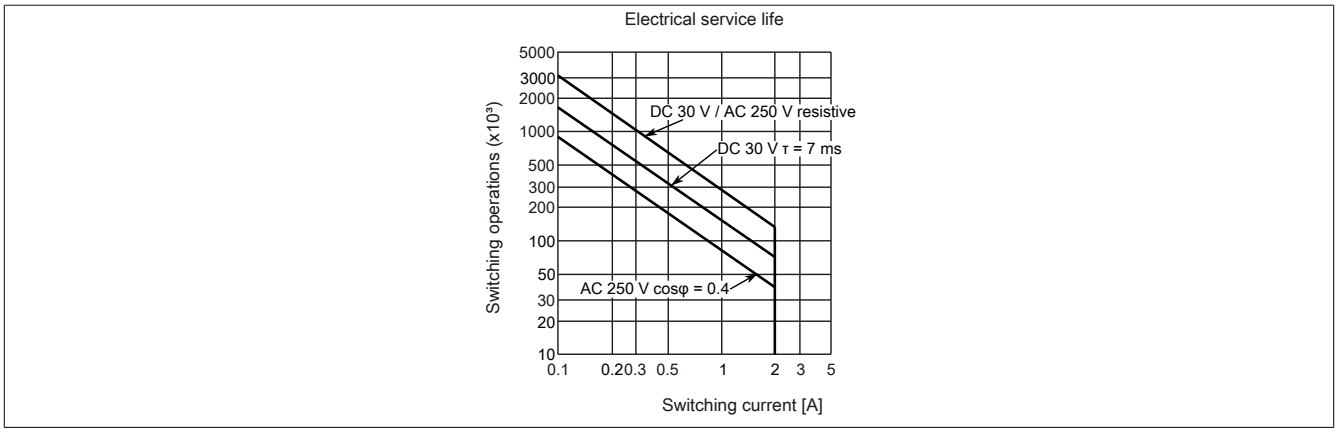
4.15.21.7 Connection example



4.15.21.8 Output circuit diagram



4.15.21.9 Electrical service life



4.15.21.10 Register description

4.15.21.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.21.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.21.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 6	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput06	Bit 5				

1) The offset specifies where the register is within the CAN object.

4.15.21.10.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.21.10.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.21.10.4.1 Switching state of digital outputs 1 to 6

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput06

The switching state of digital outputs 1 to 6 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 63	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
5	DigitalOutput06	0	Digital output 06 reset
		1	Digital output 06 set

4.15.21.10.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.21.10.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.22 X20DO8232

4.15.22.1 General information

The module is equipped with 8 outputs for 1-wire connections. The nominal output current is 2 A and the nominal voltage is 12 VDC.

The output supply is fed directly to the module. An additional supply module is not needed. There is no connection between the module and the I/O supply potential on the bus module.

- 8 digital outputs with 2 A
- Rated voltage 12 VDC
- Source connection
- 1-wire connection
- Power feed integrated in the module
- Integrated output protection

4.15.22.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO8232	X20 digital output module, 8 outputs, 12 VDC, 2 A, source, supply directly on module, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 335: X20DO8232 - Order data

4.15.22.3 Technical data

Product ID	X20DO8232
Short description	
I/O module	Eight 12 VDC digital outputs for 1-wire connections
General information	
B&R ID code	0xA4AD
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Supply voltage monitoring	Yes, using software
Power consumption	
Bus	0.22 W
Internal I/O	-
External I/O	0.82 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+4.48
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital outputs	
Design	FET positive switching

Table 336: X20DO8232 - Technical data

Product ID	X20DO8232
Nominal voltage	12 VDC
Switching voltage	12 VDC (-15% / +20%)
Nominal output current	2 A
Total nominal current	8 A
Connection type	1-wire connections
Output circuit	Source
Output protection	Thermal cutoff for overcurrent or short circuit (see value "Peak short circuit current") Internal inverse diode for switching ind. loads (see section "Switching inductive loads") Reverse polarity protection for supply voltage
Actuator supply	
Supply	External
Fuse	Required line fuse max. 10 A (slow blow)
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
$R_{DS(on)}$	140 mΩ
Max. continuous current	8.0 A
Peak short circuit current	<12 A
Switching on after overload or short circuit cutoff	Ca. 10 ms (depends on the module temperature)
Switching delay 3)	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load 3)	Max. 500 Hz; 600 Hz with max. 250 mA load
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Type 50 VDC
Isolation voltage between channel and bus	500 V_{eff}
Additional functions	To increase the output current, outputs can be switched in parallel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0,5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 336: X20DO8232 - Technical data

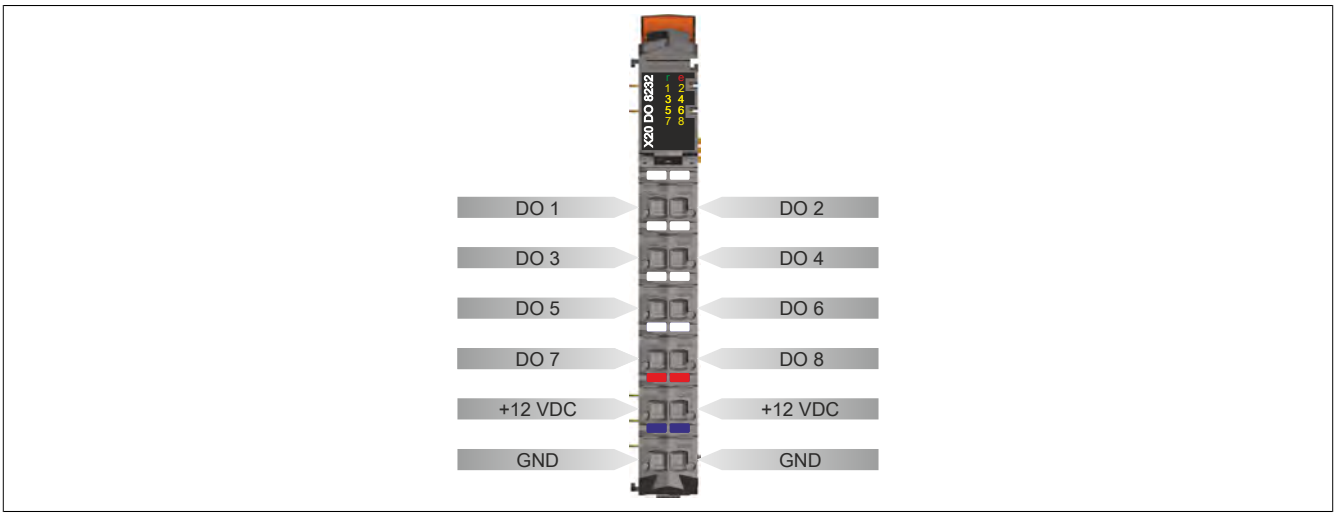
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) At loads ≤ 1 kΩ

4.15.22.4 Status LEDs

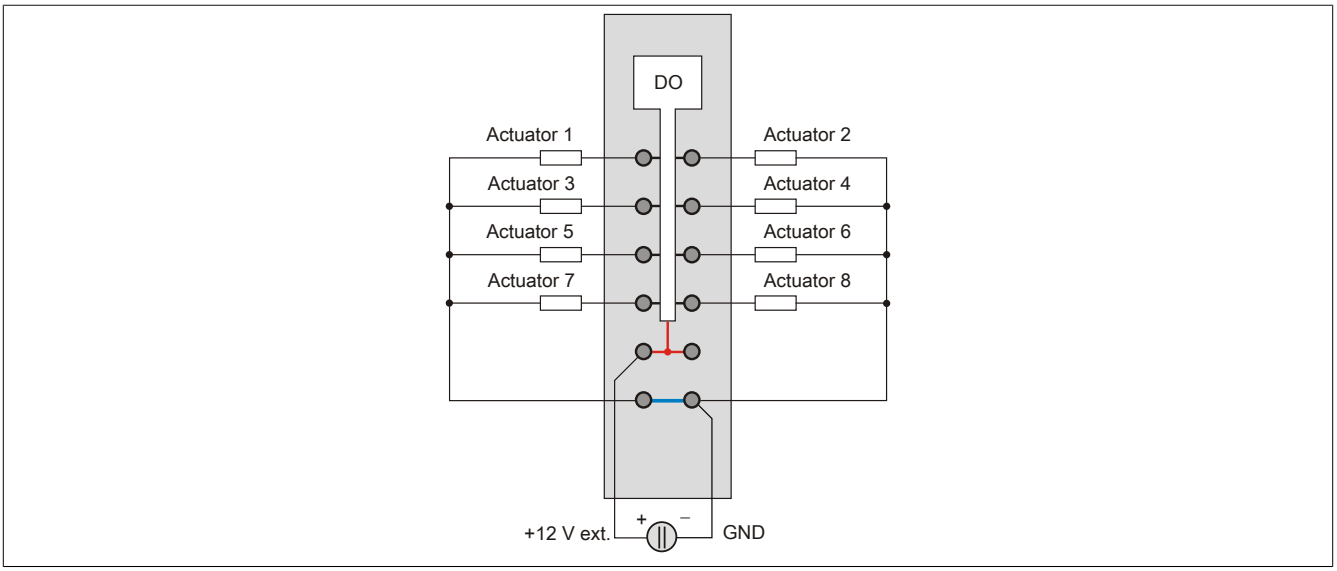
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	External I/O supply is outside the valid range: 12 VDC (-15% / +20%)
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Orange		Output status of the corresponding digital output

4.15.22.5 Pinout



4.15.22.6 Connection example

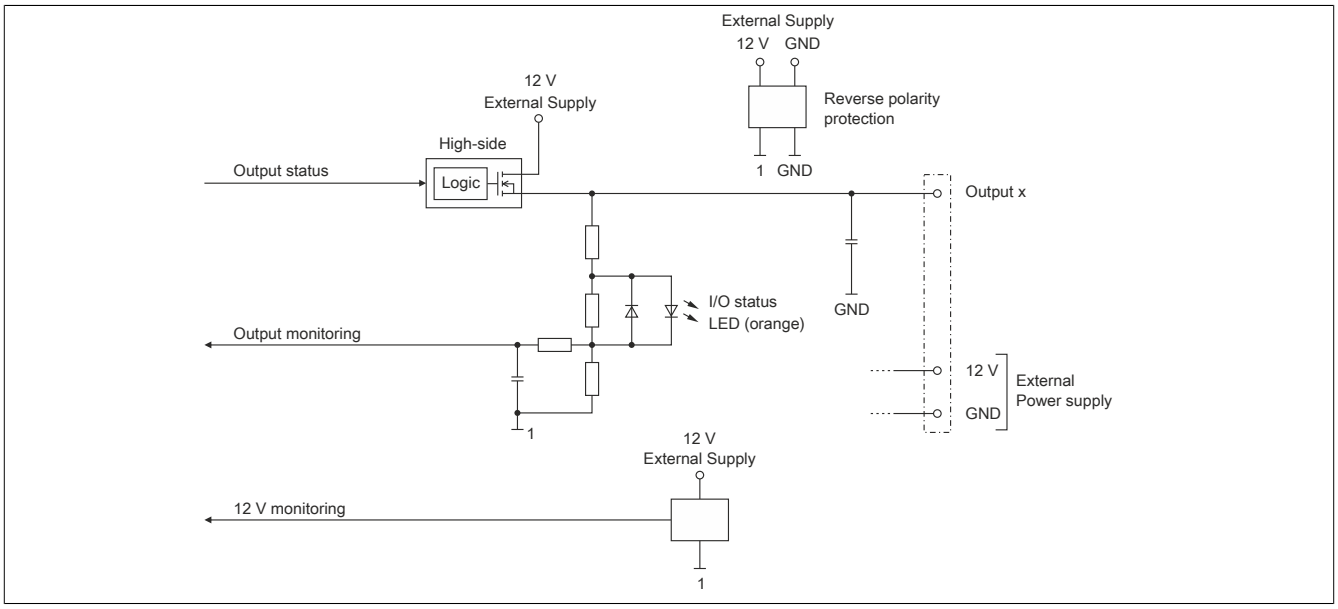


Caution!

If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

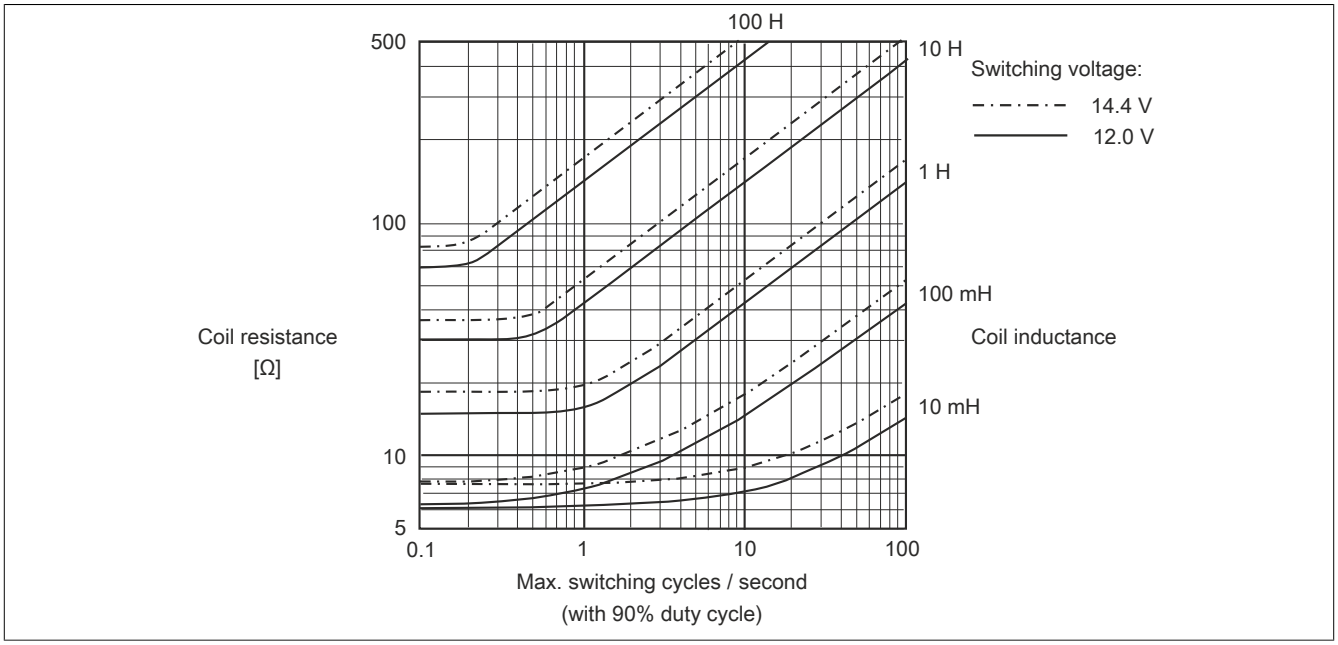
Therefore sufficient cable cross sections or external safety measures must be used.

4.15.22.7 Output circuit diagram

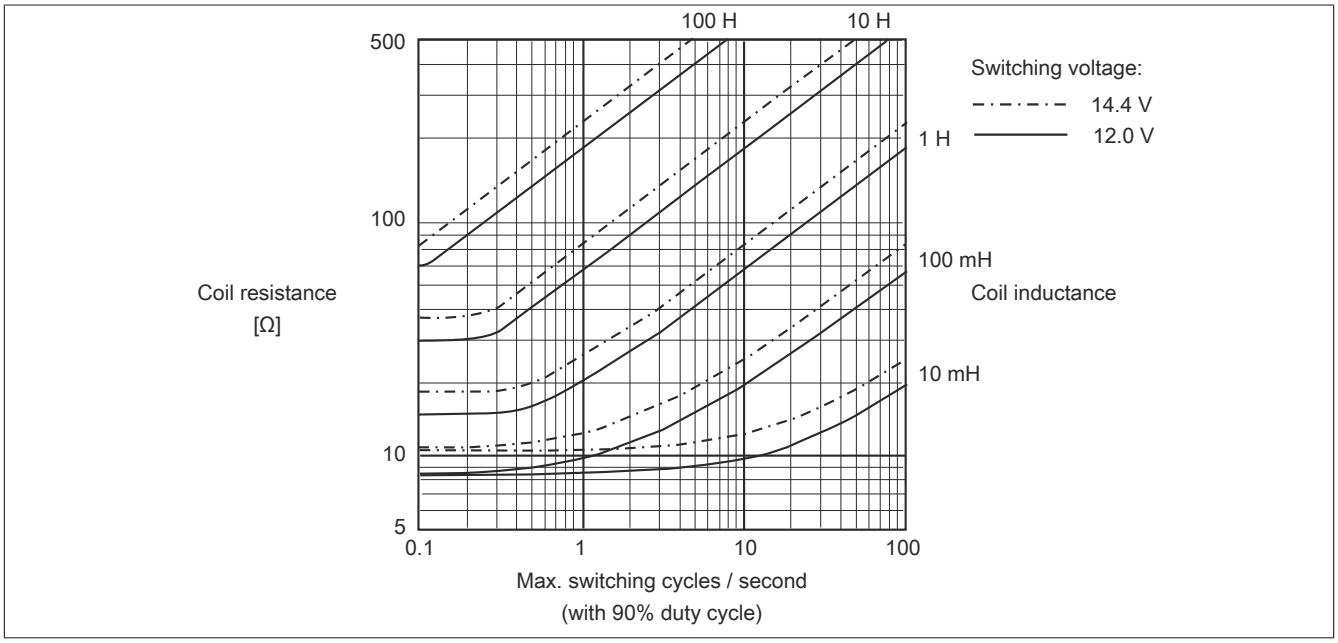


4.15.22.8 Switching inductive loads

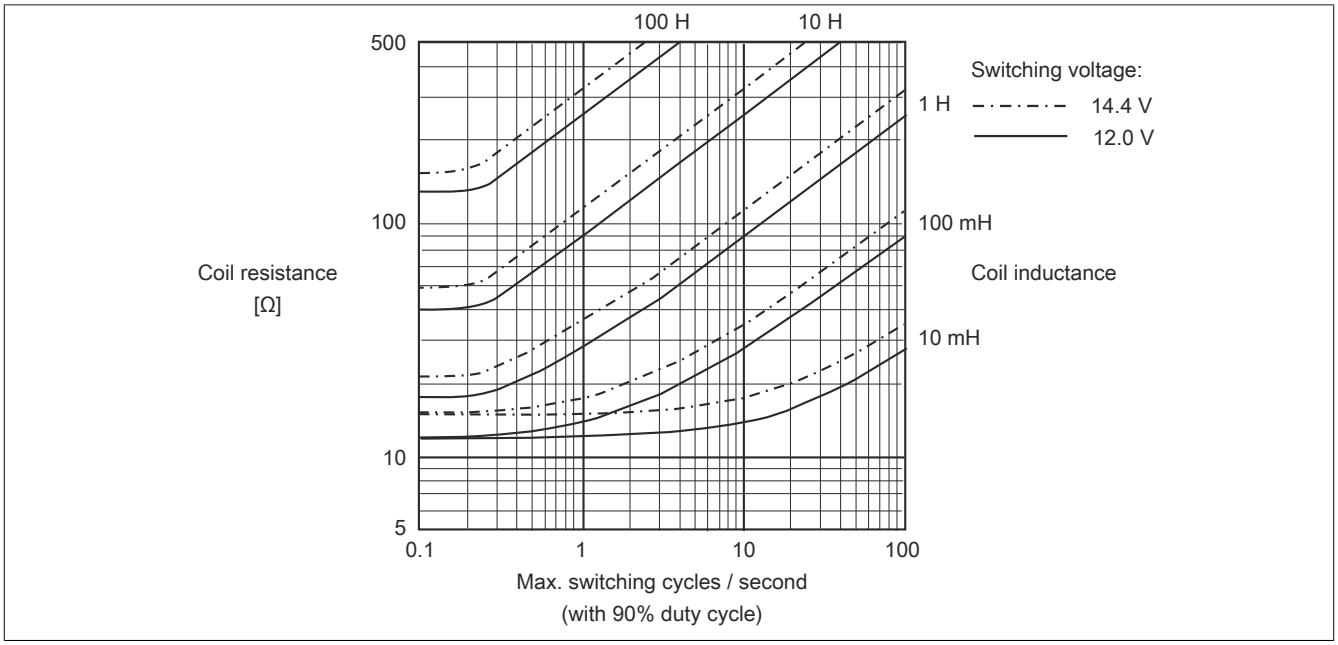
Environmental temperature: 35°C, 4 outputs (1,3,5,7 or 2,4,6,8) with the same load.



Environmental temperature: 60°C, 4 outputs (1,3,5,7 or 2,4,6,8) with the same load.



Environmental temperature: 60°C, all outputs with the same load.



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.22.9 Derating

The outputs of the module can handle up to 2 A. With a total current of 8 A, no more than 4 channels are operable at full load. To ensure optimal use of the module, it is important to assign the channels properly, and to keep in mind a potential derating.

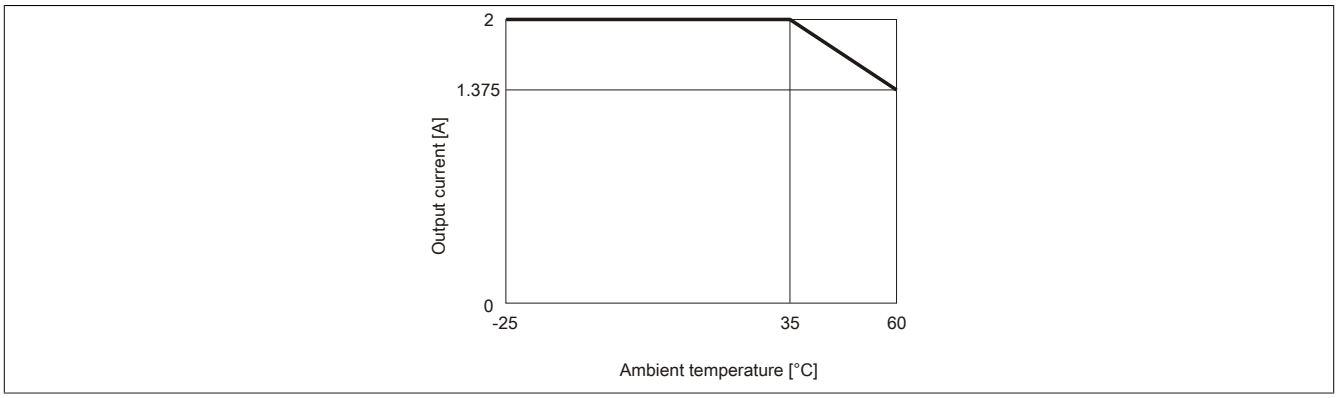
Correct channel assignment is important, since the eight outputs are divided between two output drivers. The channels operated with 2A must therefore be evenly divided between both output drivers.

Output driver 1: Channels 1 - 4
Output driver 2: Channels 5 - 8

The following table provides an overview of the number of fully used channels, the resulting best distribution, and a potential derating.

Number of channels using 2A	Division	Derating
1	Any	No
2	1st channel with 2 A ... channel no. 1 - 4 2nd channel with 2 A ... channel no. 5 - 8	No
3	Assign all even or all odd channel numbers. Examples: 1, 3, 5 2, 4, 6 3, 5, 7 4, 6, 8	 Channels 1 and 3 Channels 2 and 4 Channels 5 and 7 Channels 6 and 8
4	Assign all even or all odd channel numbers. Possible distributions: 1, 3, 5, 7 2, 4, 6, 8	 All channels All channels

Derating when 3 or 4 channels are operated with 2 A:



Information:

Modules next to this module can have a maximum power consumption of 1.0 W.

4.15.22.10 Register description

4.15.22.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.22.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		PowerSupply01	Bit 2	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.22.10.3 Function model 1 - Output switching

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
4	1	Switching state of delayed digital outputs 1 to 8	USINT			•	
		DigitalOutput01Delayed	Bit 0				
		...	...				
		DigitalOutput08Delayed	Bit 7				
6	2	Switching mask after the delay time has expired	USINT			•	
		DigitalOutput01DelayEnable	Bit 0				
		...	...				
		DigitalOutput08DelayEnable	Bit 7				
8	3	Setting the delay (OutputDelayTime)	USINT			•	
30	1	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		PowerSupply01	Bit 2	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.22.10.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	-	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		PowerSupply01	Bit 2		•		

1) The offset specifies where the register is within the CAN object.

4.15.22.10.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.22.10.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.22.10.5.1 Switching state of digital outputs 1 to 8

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput08

The switching state of digital outputs 1 to 8 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

4.15.22.10.6 Reading the module ID

Name:
asy_ModulID

This register offers another possibility for reading the module ID.

Data type	Value
UINT	Module ID

4.15.22.10.7 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.22.10.7.1 Status of digital outputs 1 to 8

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput08

This register is used to indicate the status of digital outputs 1 to 8.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
8	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

4.15.22.10.8 Operating limit monitoring

The module's output supply is monitored. An I/O supply voltage of <10.2 V is displayed as a warning.

4.15.22.10.8.1 Status of the supply voltage

Name:
asy_SupplyStatus

The status of the I/O supply voltage is mapped in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	0
2	PowerSupply01	0	I/O supply above the warning level of 10.2 V
		1	I/O supply below the warning level of 10.2 V
3 - 7	Reserved	0	0

4.15.22.10.9 Additional function - switch digital outputs w/ delay using switching mask

In function model 1 - Output switching, it is possible to control the digital outputs with a delay.

The OutputDelay mask can be used to activate the delay for each channel individually. The module is controlled here using a 100 µs-based timer and the Output or OutputDelayed register.

Behavior of function model 1 - Output switching

With a timer delay of 0:

Output: DigitalOutput0x bits

When the delay is changed:

The bit string for DigitalOutput0x bits is output. The timer restarts.

Output: DigitalOutput0x bits

After delay time has expired:

The channels with bits set in the OutputDelay mask are adapted to the respective OutputDelayed bits.

Output: DigitalOutput0x bits (if Enable bit = FALSE)
OutputDelayed bits (if Enable bit = TRUE)

Information:

Adjusting the output and restarting the timer take place immediately after transferring the new delay, even if the previous time has not yet passed.

4.15.22.10.9.1 Switching state of delayed digital outputs 1 to 8

Name:
DigitalOutput01Delayed to Digital08Delayed

According to the corresponding bit in the OutputDelay mask, the switching state of all digital outputs 1 to 8 are stored in the OutputDelayed bits after the delay time has expired.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01Delayed	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08Delayed	0	Digital output 08 reset
		1	Digital output 08 set

Information:

After the delay time has expired, only the channels with a bit set in the OutputDelay mask are adjusted to the OutputDelayed bits.

4.15.22.10.9.2 Switching mask after the delay time has expired

Name:
DigitalOutput01DelayEnable to DigitalOutput08DelayEnable

These registers create the mask for OutputDelay. They define which outputs are switched to the bit string for the OutputDelayed register after the delay time has expired.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01DelayEnable	0	Digital output 01 remains unchanged
		1	Digital output 01 is toggled
...		...	
7	DigitalOutput08DelayEnable	0	Digital output 08 remains unchanged
		1	Digital output 08 is toggled

4.15.22.10.9.3 Setting the delay

Name:
OutputDelayTime

This register can be used to set the delay in 100 µs steps.

After the delay time has expired, the digital outputs are adjusted according to the switching mask (register 6) and the delayed output pattern (register 4).

Data type	Value
USINT	0 to 255 (in 100 µs steps)[1)]

1) The value 0 disables processing

4.15.22.10.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard function model	100 µs
Bus controller function model	150 µs

4.15.22.10.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Function model 0	Equal to the minimum cycle time
Function model 1	Equal to the minimum cycle time

4.15.23 X20DO8322

4.15.23.1 General information

The module is equipped with 8 outputs for 1-wire connections and designed for source output wiring.

- 8 digital outputs
- Source connection
- 1-wire connections
- Integrated output protection

4.15.23.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO8322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 337: X20DO8322 - Order data

4.15.23.3 Technical data

Product ID	X20DO8322
Short description	
I/O module	8 digital outputs 24 VDC for 1-wire connections
General information	
B&R ID code	0xA4AC
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.26 W
Internal I/O	0.8 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+0.42
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital outputs	
Design	FET positive switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	4 A
Connection type	1-wire connections
Output circuit	Source
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")
Diagnostic status	Output monitoring with 10 ms delay

Table 338: X20DO8322 - Technical data

Product ID	X20DO8322
Leakage current when switched off	5 µA
$R_{DS(on)}$	210 mΩ
Max. continuous current	6 A
Peak short circuit current	<12 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load	Max. 500 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 50 VDC
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 338: X20DO8322 - Technical data

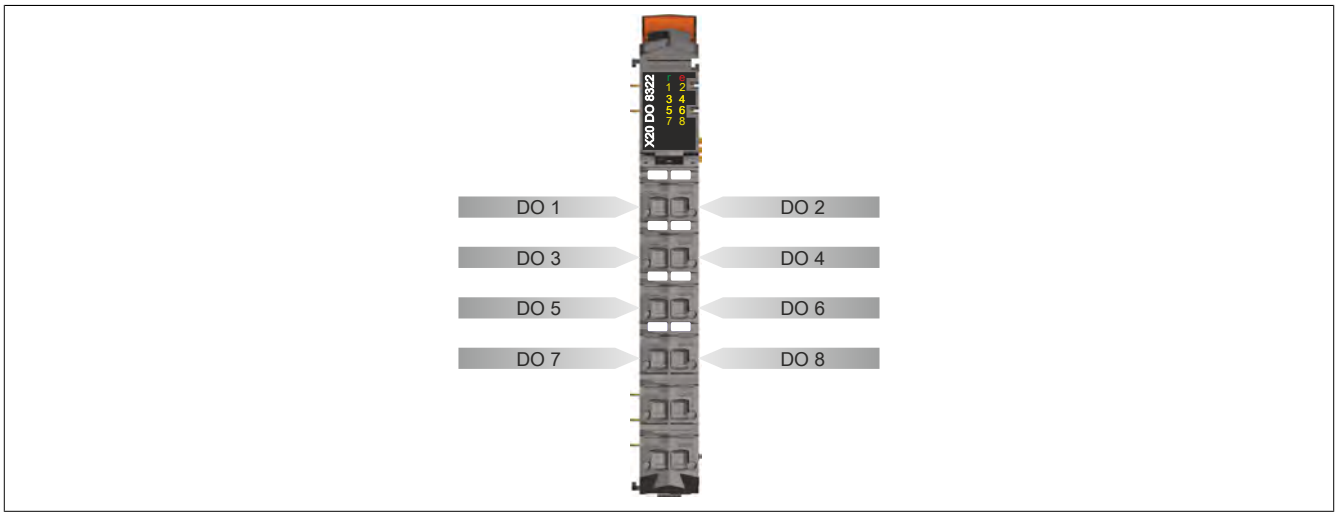
1) Number of outputs x $R_{DS(on)}$ x nominal output current^2
2) Ta min.: 0°C
   Ta max.: See environmental conditions

4.15.23.4 Status LEDs

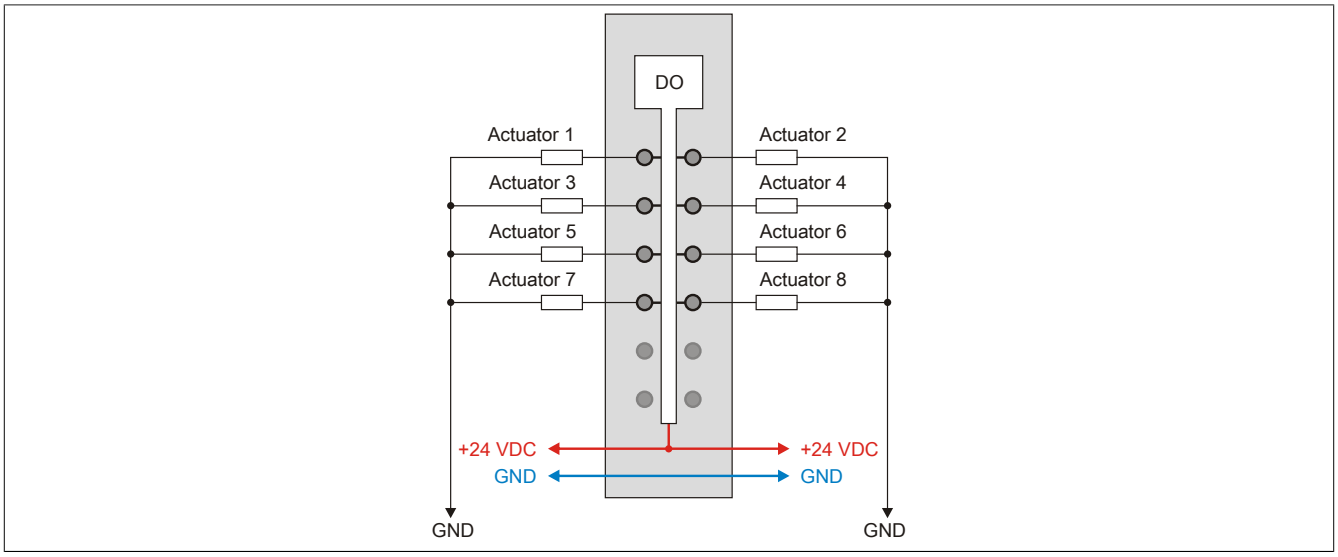
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Orange		Output status of the corresponding digital output

4.15.23.5 Pinout



4.15.23.6 Connection example

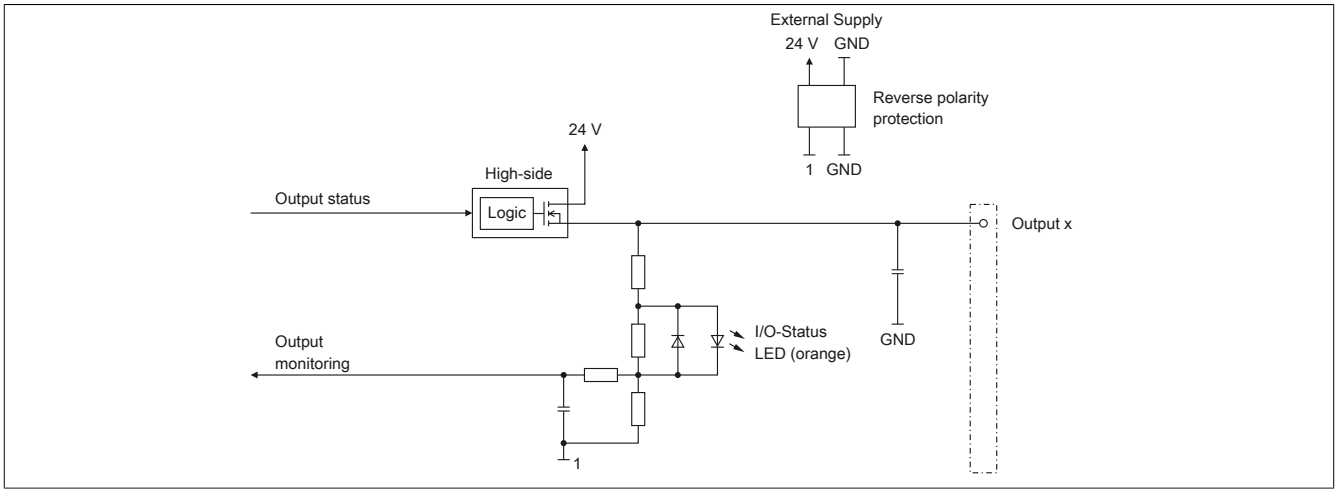


Caution!

If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

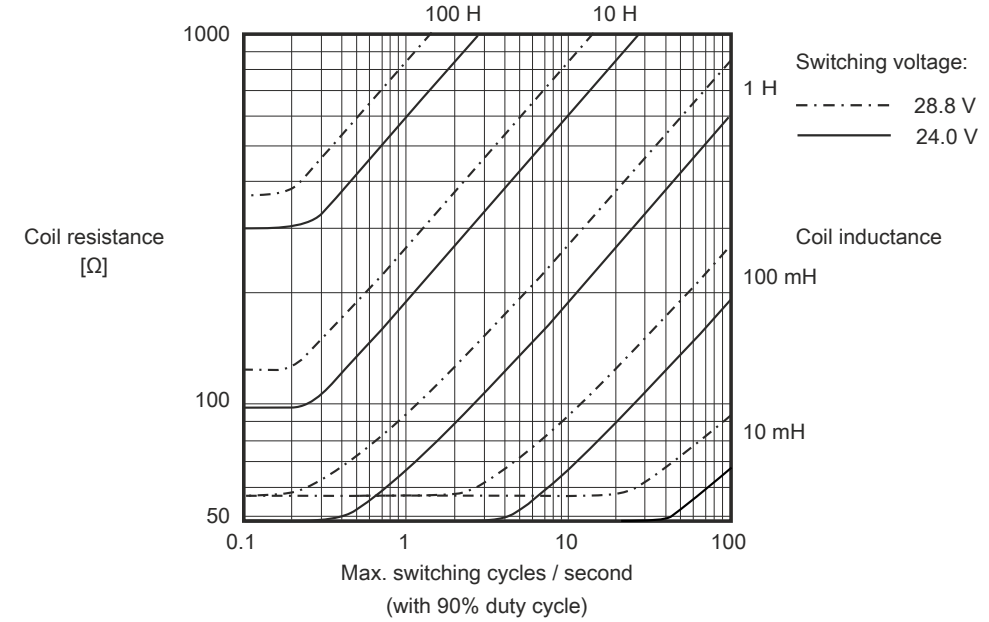
Therefore sufficient cable cross sections or external safety measures must be used.

4.15.23.7 Output circuit diagram

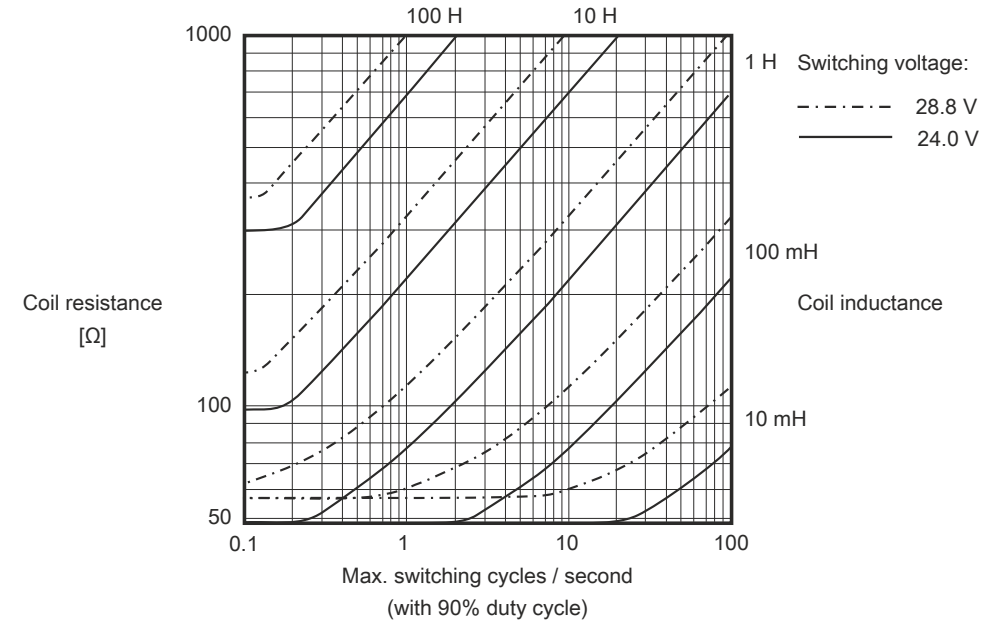


4.15.23.8 Switching inductive loads

Environmental temperature: 55°C, all outputs with the same load



Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.23.9 Register description

4.15.23.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.23.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	1	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.23.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				

1) The offset specifies where the register is within the CAN object.

4.15.23.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.23.9.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.23.9.4.1 Switching state of digital outputs 1 to 8

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput08

The switching state of digital outputs 1 to 8 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

4.15.23.9.5 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.23.9.5.1 Status of digital outputs 1 to 8

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput08

This register is used to indicate the status of digital outputs 1 to 8.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
8	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

4.15.23.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.23.9.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.24 X20DO8323

4.15.24.1 General Information

The module is an electrically isolated 8-channel digital output module. It can be configured as high-side or low-side or as a push/pull output for controlling 12 to 24 VDC DC motors.

- 8 digital outputs
- High-side or low-side connection
- Push/pull outputs
- 1-wire connections
- Integrated output protection

4.15.24.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO8323	X20 digital output module, 8 outputs, 12 to 24 V, 0.5 A, sink/source, 1-wire connections, full bridge, half bridge, thermal overload protection	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 339: X20DO8323 - Order data

4.15.24.3 Technical data

Product ID	X20DO8323
Short description	
I/O module	8 digital outputs 11.5 to 30 V for 1-wire connections
General information	
B&R ID code	0xDF4E
Status indicators	Operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using software
Power consumption	
Bus	160 mW
Internal I/O	200 mW (without load)
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
GOST-R	Yes
Digital outputs	
Design	FET push/pull (high resistance)
Nominal voltage	11.5 to 30 V
Nominal output current	0.5 A
Total nominal current	4 A
Connection type	1-wire connections
Output circuit	Sink / source
Diagnostic status	
Voltage monitoring [2)]	11.5 V < supply voltage < 30 V
Output monitoring	Output OK
Leakage current when switched off	5 µA per channel
$R_{DS(on)}$	120 mΩ (low-side), 140 mΩ (high-side)
Switching delay	
0 -> 1	Max. 450 µs
1 -> 0	Max. 450 µs
Switching frequency	
Resistive load	Max. 100 Hz
Isolation voltage between channel and bus	500 V
Reverse polarity protection	Yes
Switching voltage	
Minimum	11.5 VDC
Nominal	12 to 24 VDC
Maximum	30 VDC
Protective circuit	
External	24 VDC voltage supply – Maximum current 5A (blow-out fuse)
Internal	Thermal cutoff, integrated protection for switching inductances
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C

Table 340: X20DO8323 - Technical data

Product ID	X20DO8323
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 340: X20DO8323 - Technical data

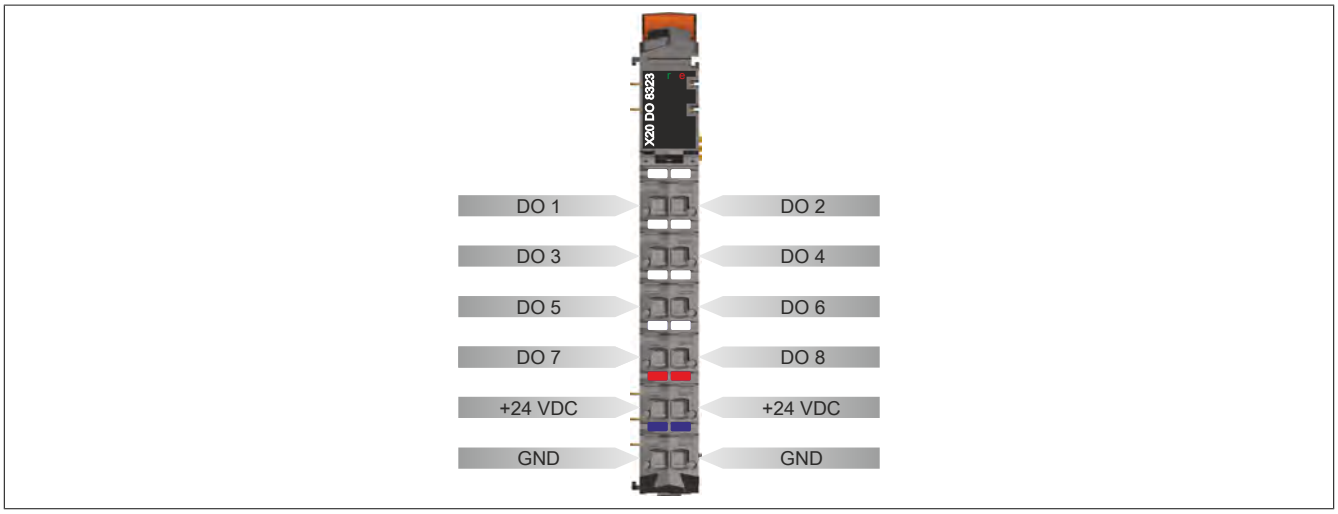
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) If the voltage is too low, the outputs are switched off.

4.15.24.4 Status LEDs

For a description of the various operating modes, see section 2.11.1 "re LEDs".

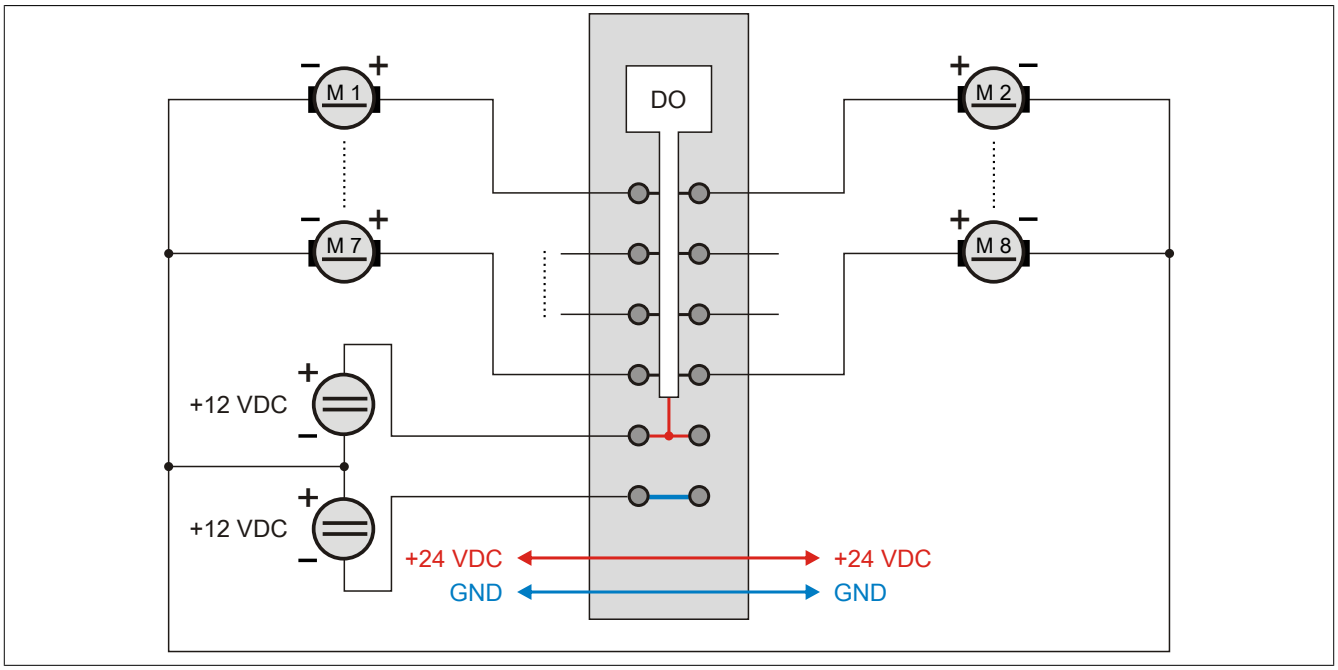
Image	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	I/O supply too low

4.15.24.5 Pinout

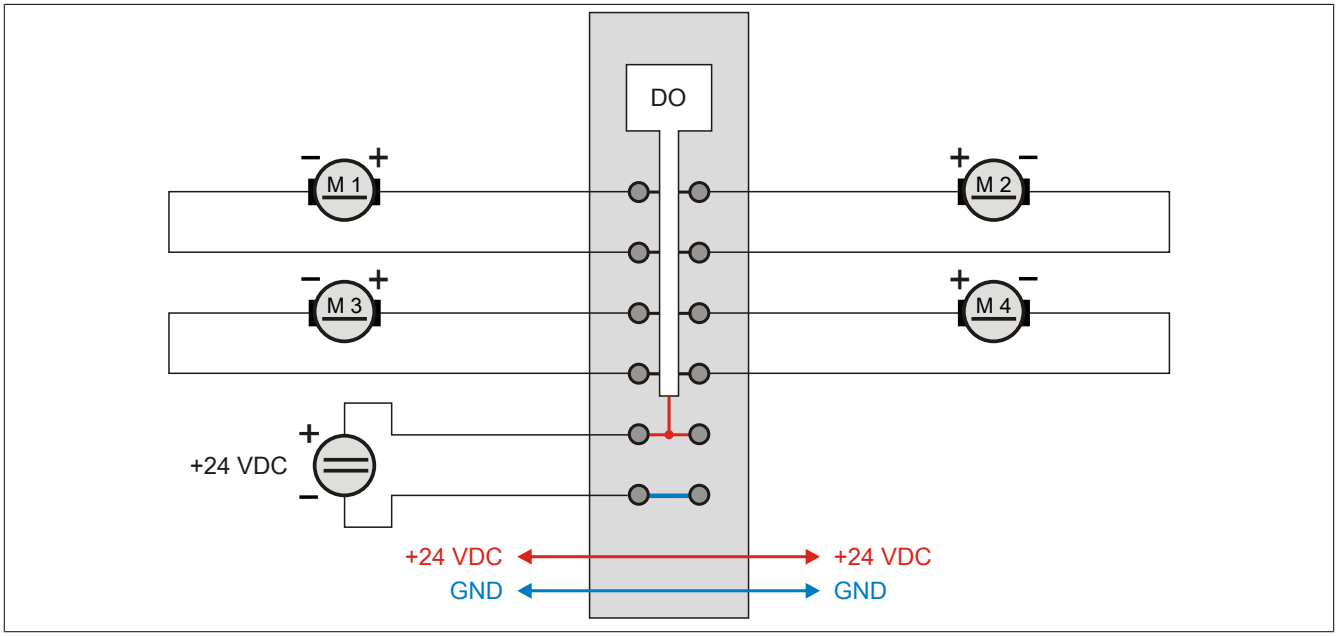


4.15.24.6 Connection example

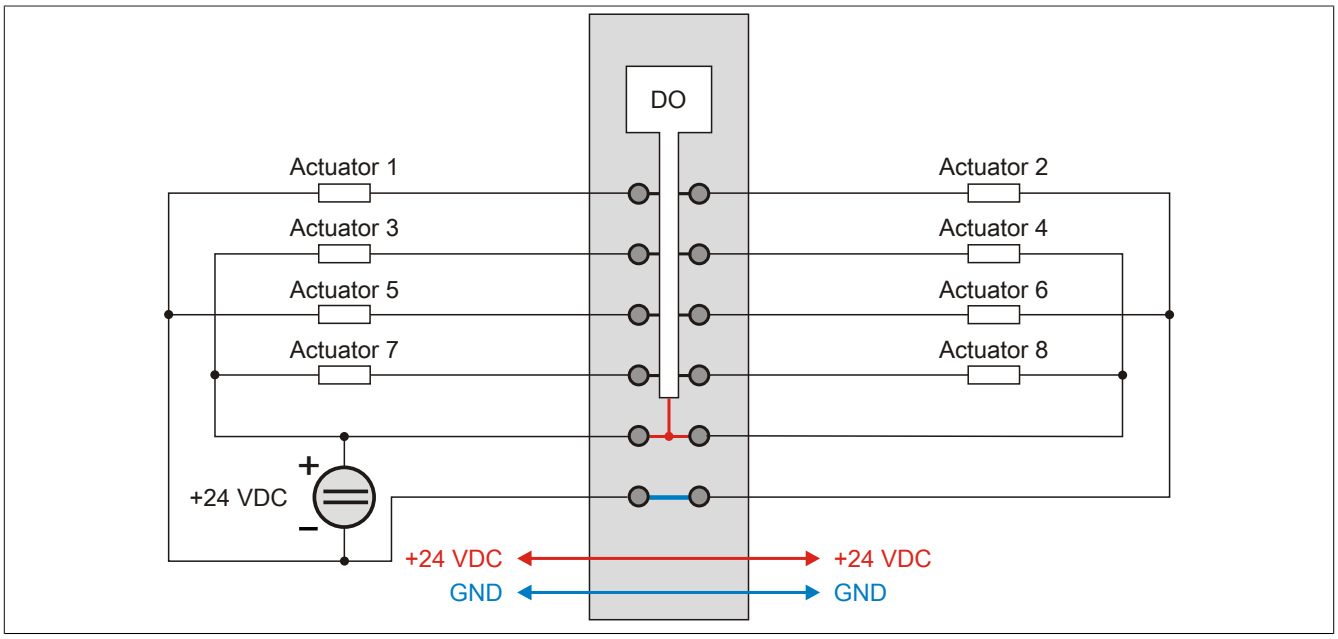
Half bridge connection:



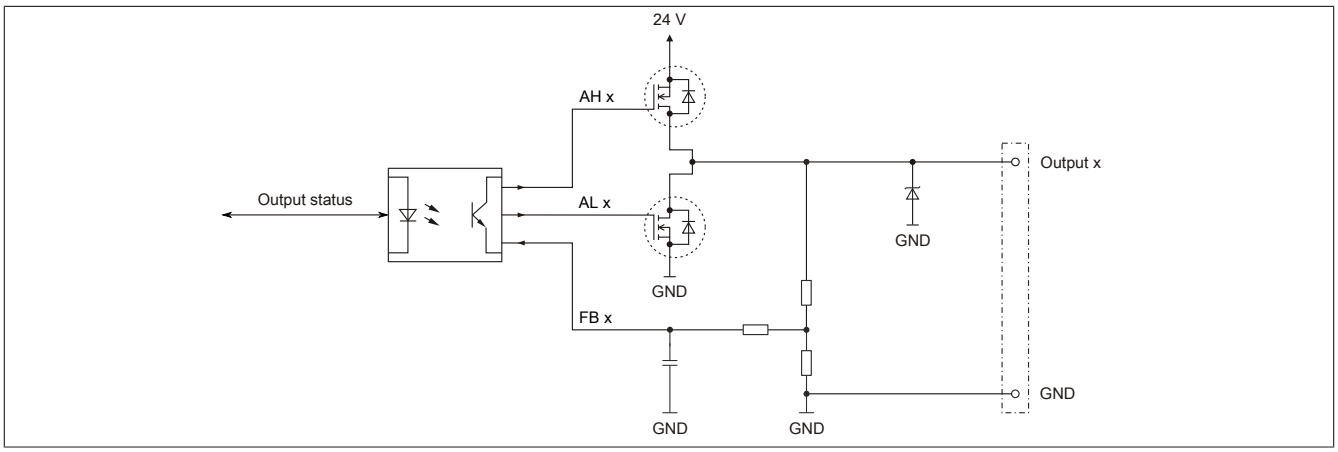
Full bridge connection:



Use as high-side or low-side:



4.15.24.7 Output circuit diagram



4.15.24.8 Register description

4.15.24.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.24.8.2 Function model 0 - Default

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	1	DigitalInput	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
4	1	EnableDigitalOutput	USINT			•	
		EnabDigitalOutput01	Bit 0				
		...	...				
		EnabDigitalOutput08	Bit 7				
30	2	StatusInput01	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
31	3	Cumulative status	USINT	•			
		StatusDigitalOutputs	Bit 0				
		StatusSupplyLO	Bit 4				
		StatusSupplyHI	Bit 5				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.24.8.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Digital inputs	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
4	-	Switching between inputs and outputs	USINT				•
		EnabDigitalOutput01	Bit 0				
		...	...				
		EnabDigitalOutput08	Bit 7				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
31	-	Cumulative status	USINT		•		
		StatusDigitalOutputs	Bit 0				
		StatusSupplyLO	Bit 4				
		StatusSupplyHI	Bit 5				

1) The offset specifies where the register is within the CAN object.

4.15.24.8.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.24.8.4 Digital outputs

The output state is sent to the output ports acyclically to the network in the system timer (100 µsec). (max. switch off jitter: 50 µsec, max. switch on jitter: 150 µsec)

The output state must be switched with at least a 300 µsec delay in order to prevent the high-side and low-side drivers from switching together.

4.15.24.8.4.1 Switching state of digital outputs 1 to 8

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput08

The switching state of digital outputs 1 to 8 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

4.15.24.8.4.2 Status of digital outputs 1 to 8

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput08

This register is used to indicate the status of digital outputs 1 to 8.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
8	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

4.15.24.8.4.3 Switching between inputs and outputs

Name:
EnableDigitalOutput
EnabDigitalOutput01 through EnabDigitalOutput08

In this register, all channels can be connected as inputs or outputs. For each output there is a corresponding switching bit. Clearing this bit switches to tristate mode.

In function model 254 the initial value is 255.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("EnabDigitalOutput01" through "EnabDigitalOutput08") or whether this register should be displayed as an individual USINT data point ("EnableDigitalOutput").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	EnabDigitalOutput01	0	Channel 1 used as input
		1	Channel 1 used as output
...		...	
7	EnabDigitalOutput08	0	Channel 8 used as input
		1	Channel 8 used as output

4.15.24.8.5 Digital inputs

Name:
DigitalInput
DigitalInput01 through DigitalInput08

The status of digital inputs 1 to 8 is mapped in this register.

The status of the digital inputs is read with a minimum update rate of 5 to 8 msec. according to the digital output status sample rate.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalInput01" through "DigitalInput0x") or whether this register should be displayed as an individual USINT data point ("DigitalInput").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input status - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input status - Digital input 8

4.15.24.8.6 Cumulative status

Name:
StatusDigitalOutputs
StatusSupplyLO
StatusSupplyHI

The state of output monitoring and the supply voltage for all outputs are collected and mapped to this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutputs	0	No output monitoring
		1	Output monitoring active for at least one channel
1 - 3	Reserved	0	
4	StatusSupplyLO	0	No error
		1	Supply voltage too low (<= 11.5 VDC)
5	StatusSupplyHI	0	No error
		1	Supply voltage too high (> 30 VDC)
6 - 7	Reserved	0	

4.15.24.8.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.24.8.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
All channels	400 µs

4.15.25 X20(c)DO8331

4.15.25.1 General information

The module is equipped with 8 outputs for 1-wire connections. The rated output current is 2 A.

The output supply is fed directly to the module. An additional supply module is not needed. There is no connection between the module and the I/O supply potential on the bus module.

- 8 digital outputs with 2 A
- Sink connection
- 1-wire connections
- Power feed integrated in the module
- Integrated output protection

4.15.25.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.25.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO8331	X20 digital output module, 8 outputs, 24 VDC, 2 A, sink, supply directly on module, 1-wire connections	
X20cDO8331	X20 digital output module, coated, 8 outputs, 24 VDC, 2 A, sink, supply directly on module, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 341: X20DO8331, X20cDO8331 - Order data

4.15.25.4 Technical data

Product ID	X20DO8331	X20cDO8331
Short description		
I/O module	8 digital outputs 24 VDC for 1-wire connections	
General information		
B&R ID code	0x22EB	0xE22B
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	
Supply voltage monitoring	Yes, using software	
Power consumption		
Bus	0.22 W	
Internal I/O	-	
External I/O	0.9 W	
Additional power dissipation caused by the actuators (resistive) [W] [1]	+0.56	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
Digital outputs		
Design	FET negative switching	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	2 A	
Total nominal current	8 A	
Connection type	1-wire connections	
Output circuit	Sink	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads") Reverse polarity protection for supply voltage	
Actuator supply		
Supply	External	
Fuse	Required line fuse: Max. 10 A, slow-blow	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	75 µA	
$R_{DS(on)}$	35 mΩ	
Peak short circuit current	<24 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay		
0 -> 1	<300 µs	
1 -> 0	<500 µs	
Switching frequency		
Resistive load	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Additional functions	To increase the output current, outputs can be switched in parallel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 342: X20DO8331, X20cDO8331 - Technical data

Product ID	X20DO8331	X20cDO8331
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 342: X20DO8331, X20cDO8331 - Technical data

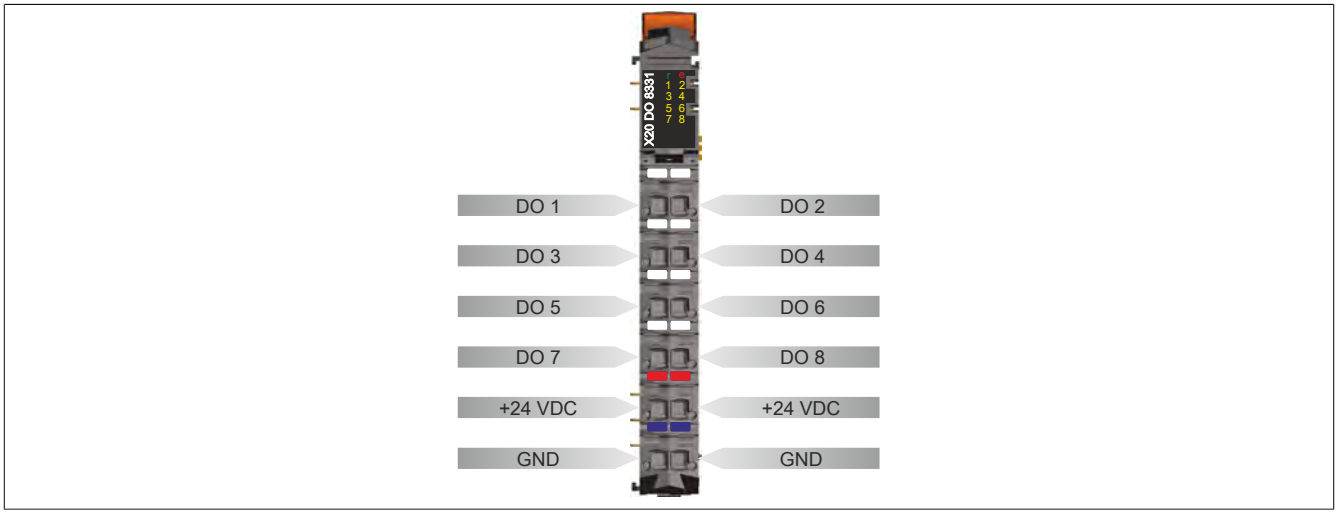
1) Number of outputs x $R_{DS(on)}$ x nominal output current^2
2) Ta min.: 0°C
   Ta max.: See environmental conditions

4.15.25.5 Status LEDs

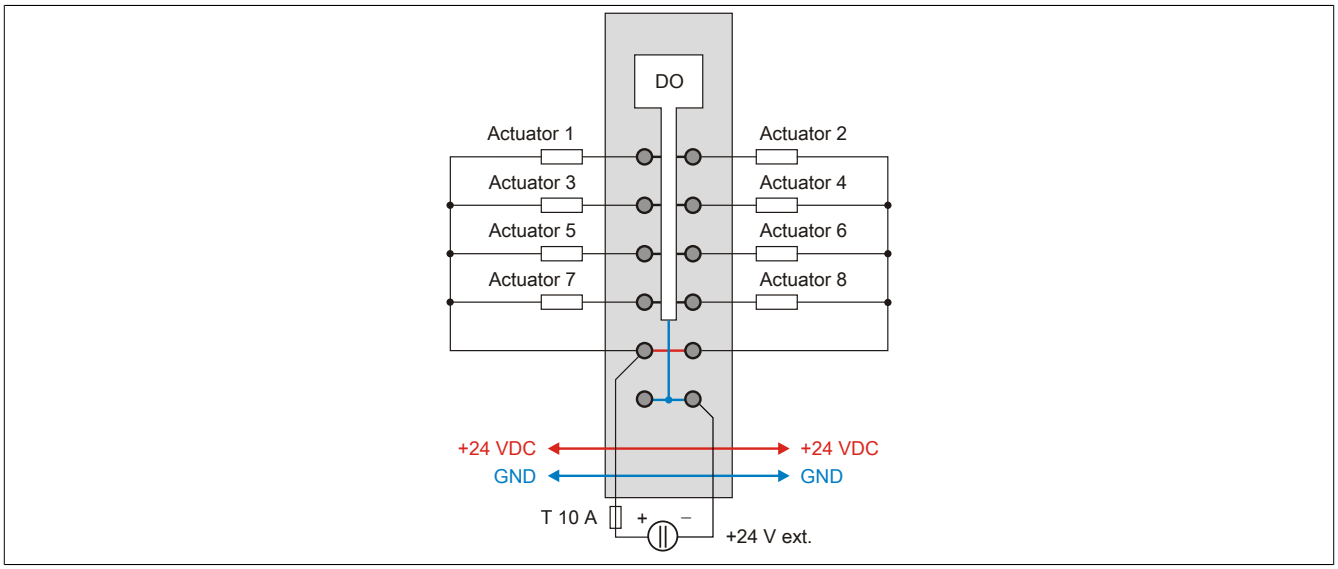
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	I/O supply too low
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Orange		Output status of the corresponding digital output

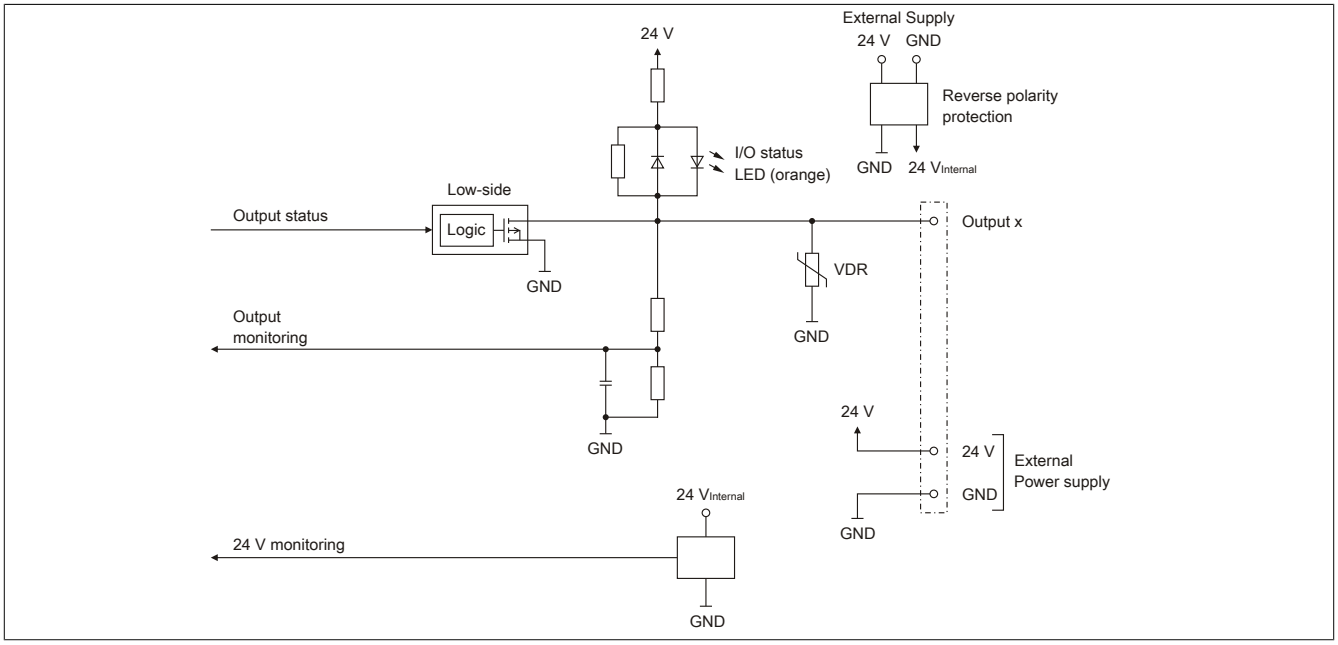
4.15.25.6 Pinout



4.15.25.7 Connection example

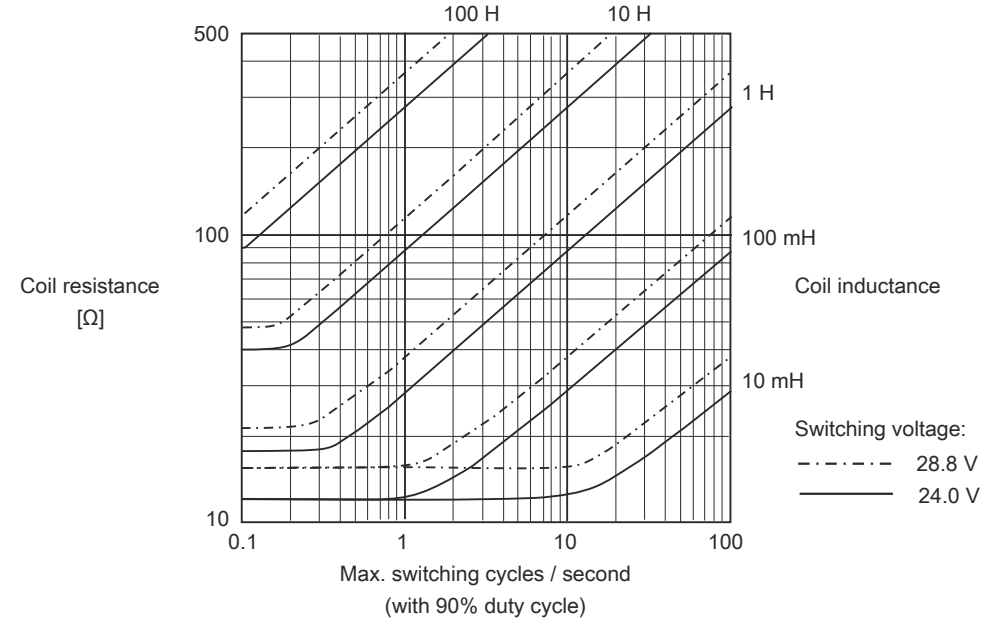


4.15.25.8 Output circuit diagram

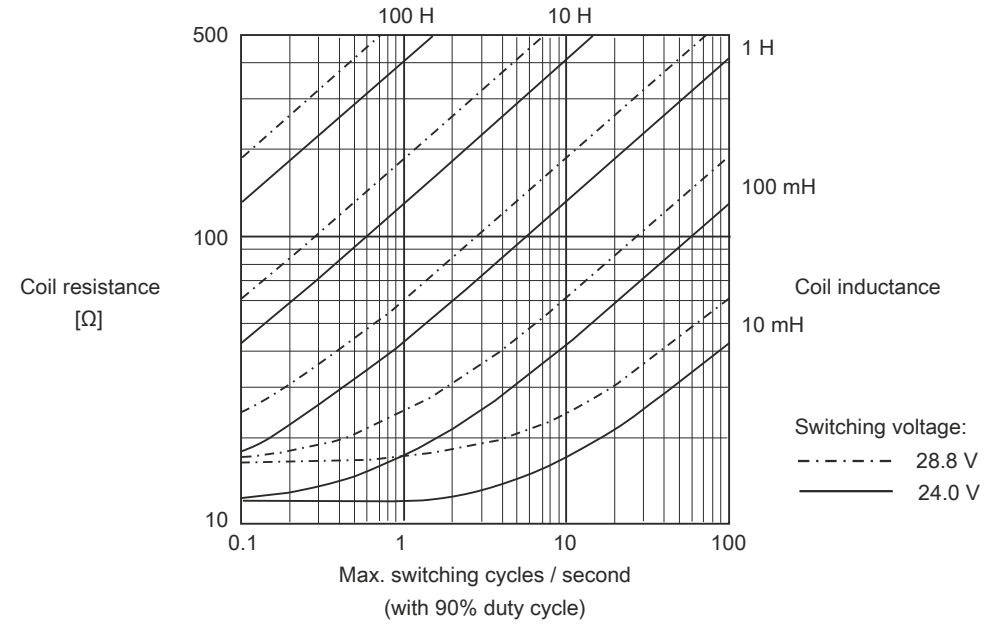


4.15.25.9 Switching inductive loads

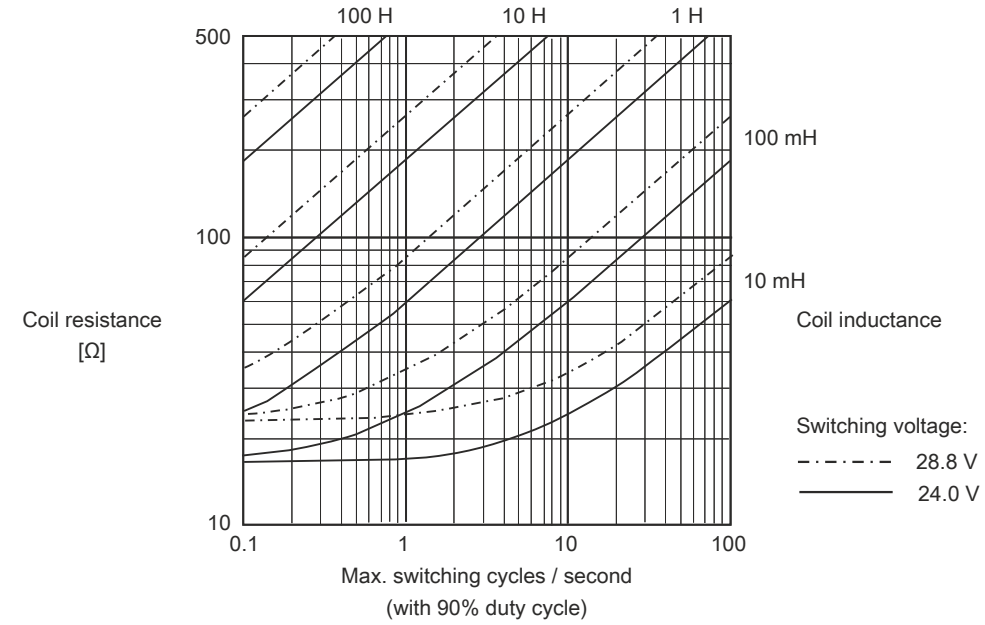
Environmental temperature: 35°C, 4 outputs (1,3,5,7 or 2,4,6,8) with the same load.



Environmental temperature: 60°C, 4 outputs (1,3,5,7 or 2,4,6,8) with the same load.



Environmental temperature: 60°C, all outputs with the same load.



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.25.10 Derating

The outputs of the module can handle up to 2 A. With a total current of 8 A, no more than 4 channels are operable at full load. To ensure optimal use of the module, it is important to assign the channels properly, and to keep in mind a potential derating.

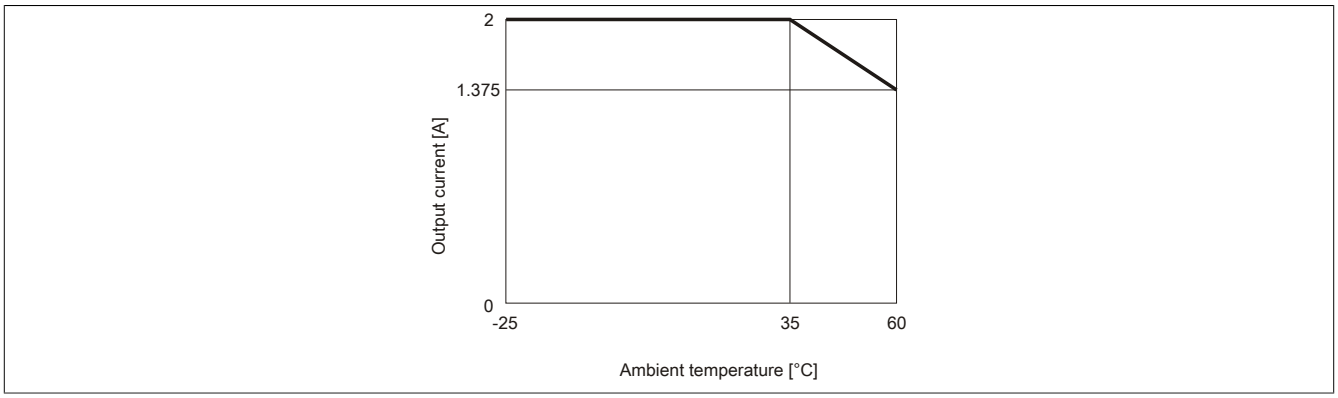
Correct channel assignment is important, since the eight outputs are divided between two output drivers. The channels operated with 2A must therefore be evenly divided between both output drivers.

Output driver 1: Channels 1 - 4
Output driver 2: Channels 5 - 8

The following table provides an overview of the number of fully used channels, the resulting best distribution, and a potential derating.

Number of channels using 2A	Division	Derating
1	Any	No
2	1st channel with 2 A ... channel no. 1 - 4 2nd channel with 2 A ... channel no. 5 - 8	No
3	Assign all even or all odd channel numbers. Examples: 1, 3, 5 2, 4, 6 3, 5, 7 4, 6, 8	 Channels 1 and 3 Channels 2 and 4 Channels 5 and 7 Channels 6 and 8
4	Assign all even or all odd channel numbers. Possible distributions: 1, 3, 5, 7 2, 4, 6, 8	 All channels All channels

Derating when 3 or 4 channels are operated with 2 A:



Information:

Modules next to this module can have a maximum power consumption of 1.5 W.

4.15.25.11 Register description

4.15.25.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.25.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	1	StatusInput01	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		PowerSupply01	Bit 2	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.25.11.3 Function model 1 - Output switching

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
4	1	Switching state of delayed digital outputs 1 to 8	USINT			•	
		DigitalOutput01Delayed	Bit 0				
		...	...				
		DigitalOutput08Delayed	Bit 7				
6	2	Switching mask after the delay time has expired	USINT			•	
		DigitalOutput01DelayEnable	Bit 0				
		...	...				
		DigitalOutput08DelayEnable	Bit 7				
8	3	Setting the delay (OutputDelayTime)	USINT			•	
30	1	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		PowerSupply01	Bit 2	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.25.11.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		Power Supply01	Bit 2		•		

1) The offset specifies where the register is within the CAN object.

4.15.25.11.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.25.11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.25.11.5.1 Switching state of digital outputs 1 to 8

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput08

The switching state of digital outputs 1 to 8 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

4.15.25.11.6 Reading the module ID

Name:
asy_ModulID

This register offers another possibility for reading the module ID.

Data type	Value
UINT	Module ID

4.15.25.11.7 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.25.11.7.1 Status of digital outputs 1 to 8

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput08

This register is used to indicate the status of digital outputs 1 to 8.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
8	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

4.15.25.11.8 Operating limit monitoring

The module's output supply is monitored. An I/O supply voltage of <20.4 V is displayed as a warning.

4.15.25.11.8.1 Status of the supply voltage

Name:
asy_SupplyStatus

The status of the I/O supply voltage is mapped in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	PowerSupply01	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - 7	Reserved	0	

4.15.25.11.9 Additional function - switch digital outputs w/ delay using switching mask

In function model 1 - Output switching, it is possible to control the digital outputs with a delay.

The OutputDelay mask can be used to activate the delay for each channel individually. The module is controlled here using a 100 µs-based timer and the Output or OutputDelayed register.

Behavior of function model 1 - Output switching

With a timer delay of 0:

Output: DigitalOutput0x bits

When the delay is changed:

The bit string for DigitalOutput0x bits is output. The timer restarts.

Output: DigitalOutput0x bits

After delay time has expired:

The channels with bits set in the OutputDelay mask are adapted to the respective OutputDelayed bits.

Output: DigitalOutput0x bits (if Enable bit = FALSE)
OutputDelayed bits (if Enable bit = TRUE)

Information:

Adjusting the output and restarting the timer take place immediately after transferring the new delay, even if the previous time has not yet passed.

4.15.25.11.9.1 Switching state of delayed digital outputs 1 to 8

Name:
DigitalOutput01Delayed to Digital08Delayed

According to the corresponding bit in the OutputDelay mask, the switching state of all digital outputs 1 to 8 are stored in the OutputDelayed bits after the delay time has expired.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01Delayed	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08Delayed	0	Digital output 08 reset
		1	Digital output 08 set

Information:

After the delay time has expired, only the channels with a bit set in the OutputDelay mask are adjusted to the OutputDelayed bits.

4.15.25.11.9.2 Switching mask after the delay time has expired

Name:
DigitalOutput01DelayEnable to DigitalOutput08DelayEnable

These registers create the mask for OutputDelay. They define which outputs are switched to the bit string for the OutputDelayed register after the delay time has expired.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01DelayEnable	0	Digital output 01 remains unchanged
		1	Digital output 01 is toggled
...		...	
7	DigitalOutput08DelayEnable	0	Digital output 08 remains unchanged
		1	Digital output 08 is toggled

4.15.25.11.9.3 Setting the delay

Name:
OutputDelayTime

This register can be used to set the delay in 100 µs steps.

After the delay time has expired, the digital outputs are adjusted according to the switching mask (register 6) and the delayed output pattern (register 4).

Data type	Value
USINT	0 to 255 (in 100 µs steps)[1)]

1) The value 0 disables processing

4.15.25.11.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard function model	100 µs
Bus controller function model	150 µs

4.15.25.11.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Function model 0	Equal to the minimum cycle time
Function model 1	Equal to the minimum cycle time

4.15.26 X20(c)DO8332

4.15.26.1 General information

The module is equipped with 8 outputs for 1-wire connections. The rated output current is 2 A.

The output supply is fed directly to the module. An additional supply module is not needed. There is no connection between the module and the I/O supply potential on the bus module.

- 8 digital outputs with 2 A
- Source connection
- 1-wire connections
- Power feed integrated in the module
- Integrated output protection

4.15.26.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.26.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO8332	X20 digital output module, 8 outputs, 24 VDC, 2 A, source, supply directly on module, 1-wire connections	
X20cDO8332	X20 digital output module, coated, 8 outputs, 24 VDC, 2 A, source, supply directly on module, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 343: X20DO8332, X20cDO8332 - Order data

4.15.26.4 Technical data

Product ID	X20DO8332	X20cDO8332
Short description		
I/O module	8 digital outputs 24 VDC for 1-wire connections	
General information		
B&R ID code	0x1B9D	0xE22C
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	
Supply voltage monitoring	Yes, using software	
Power consumption		
Bus	0.22 W	
Internal I/O	-	
External I/O	0.92 W	
Additional power dissipation caused by the actuators (resistive) [W] [1]	+2.24	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Digital outputs		
Design	FET positive switching	
Number of output groups	2	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	2 A	
Total nominal current		
Per group	4 A	
Per module	8 A [3]	
Connection type	1-wire connections	
Output circuit	Source	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads") Reverse polarity protection for supply voltage	
Actuator supply		
Supply	External	
Fuse	Required line fuse: Max. 10 A, slow-blow	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	5 µA	
$R_{DS(on)}$	140 mΩ	
Max. continuous current	8 A	
Peak short circuit current	<12 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay		
0 -> 1	<300 µs	
1 -> 0	<300 µs	
Switching frequency		
Resistive load	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Additional functions	To increase the output current, outputs can be switched in parallel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	

Table 344: X20DO8332, X20cDO8332 - Technical data

Product ID	X20DO8332	X20cDO8332
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 344: X20DO8332, X20cDO8332 - Technical data

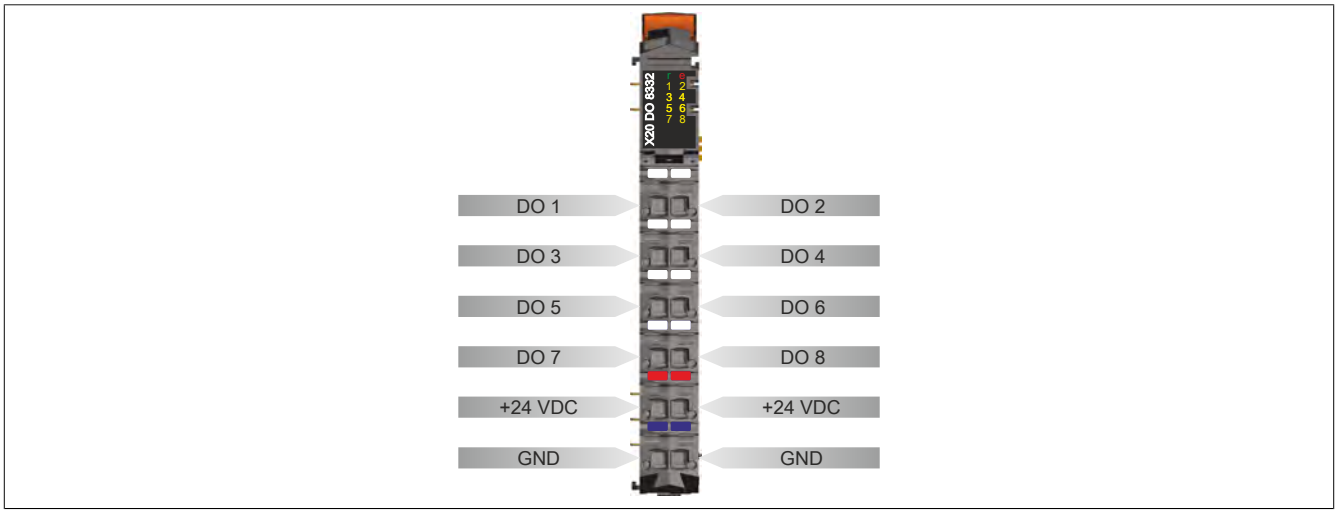
1) Number of outputs x $R_{DS(on)}$ x nominal output current[2]
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) Derating may be necessary with more than 6 A summation current.

4.15.26.5 Status LEDs

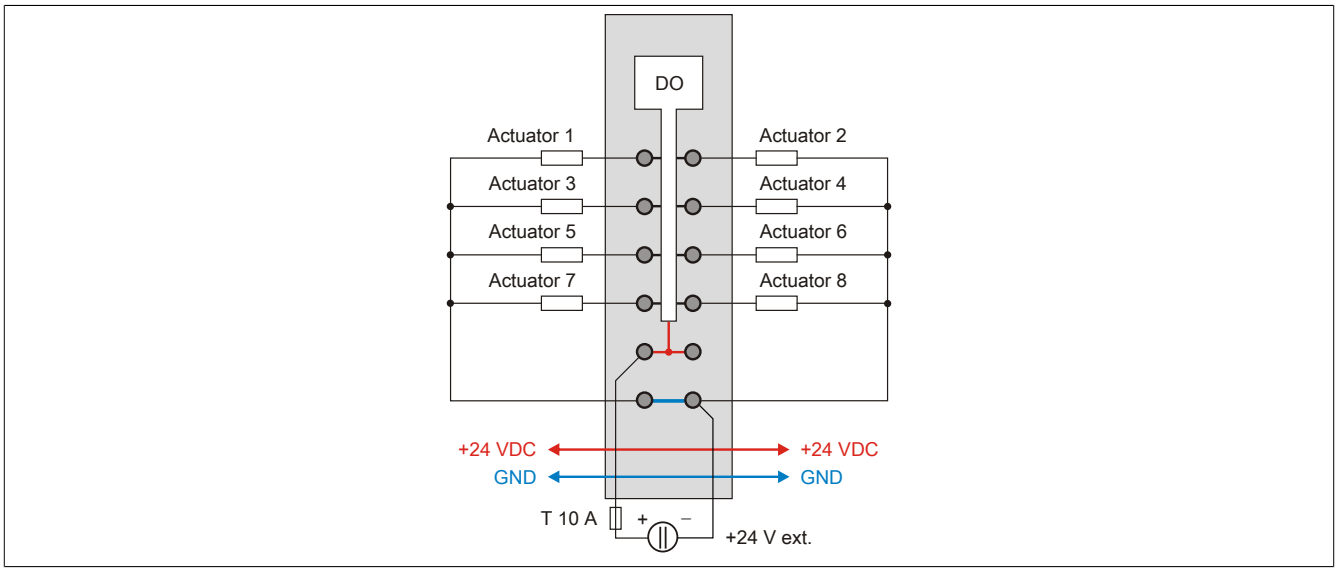
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	I/O supply too low
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Orange		Output status of the corresponding digital output

4.15.26.6 Pinout



4.15.26.7 Connection example

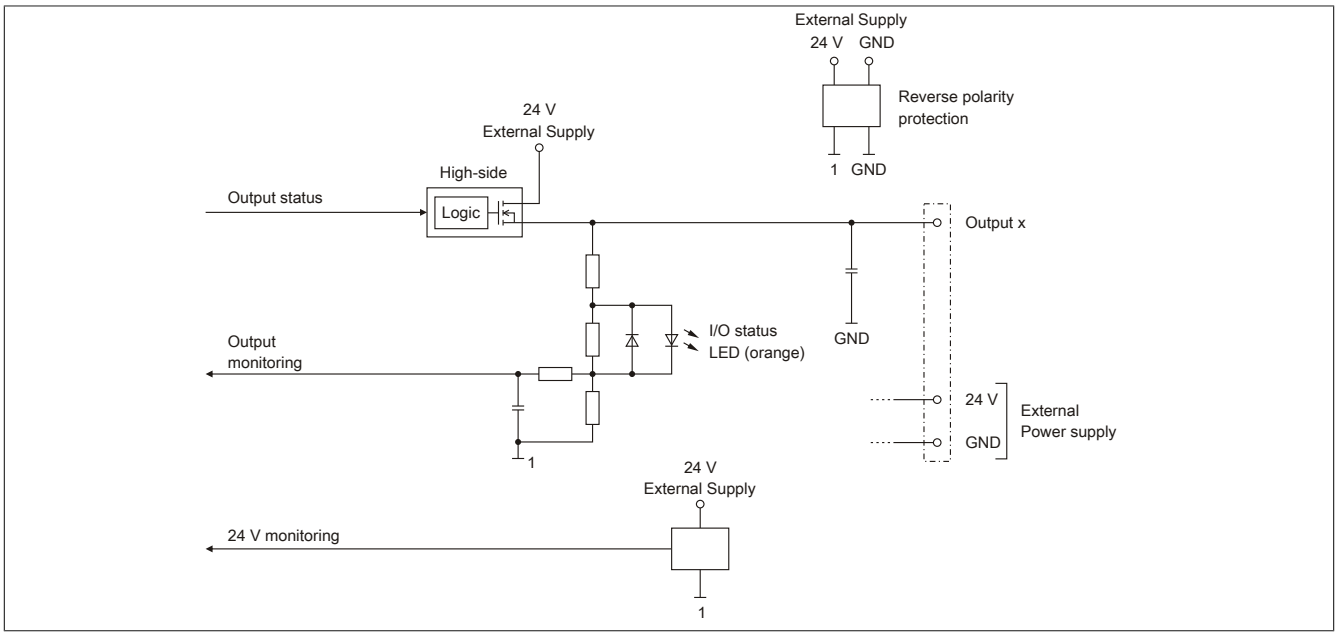


Caution!

If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

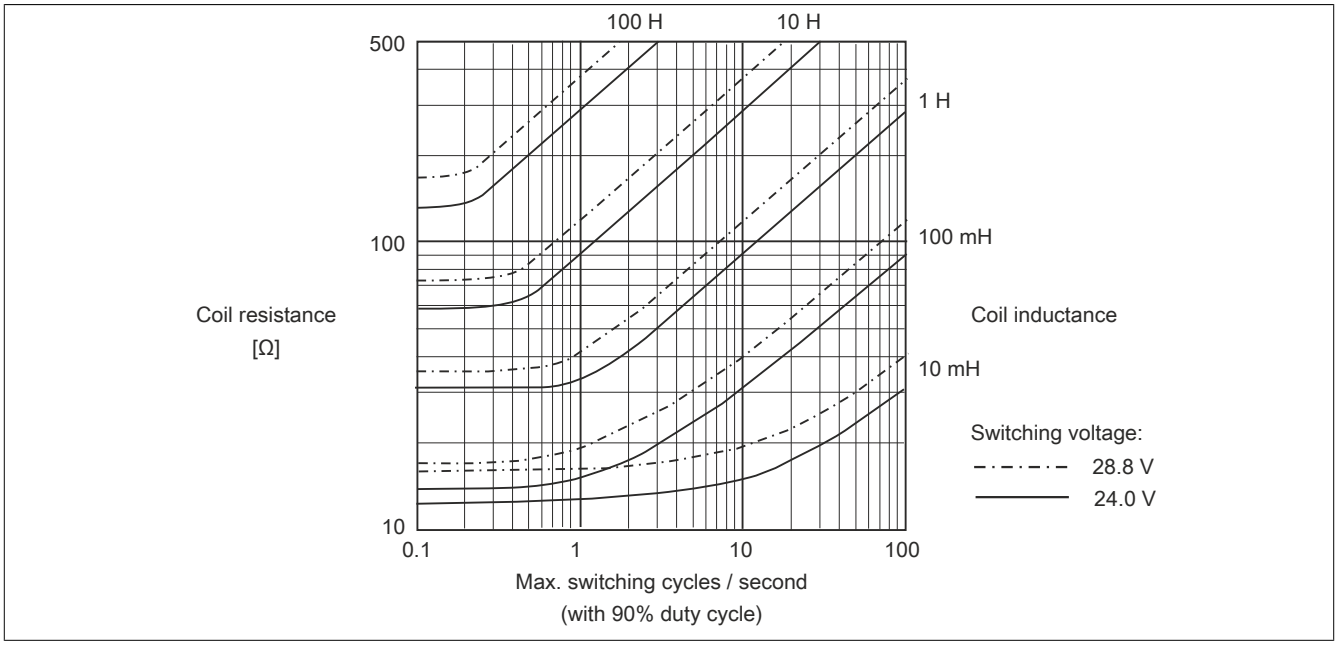
Therefore sufficient cable cross sections or external safety measures must be used.

4.15.26.8 Output circuit diagram

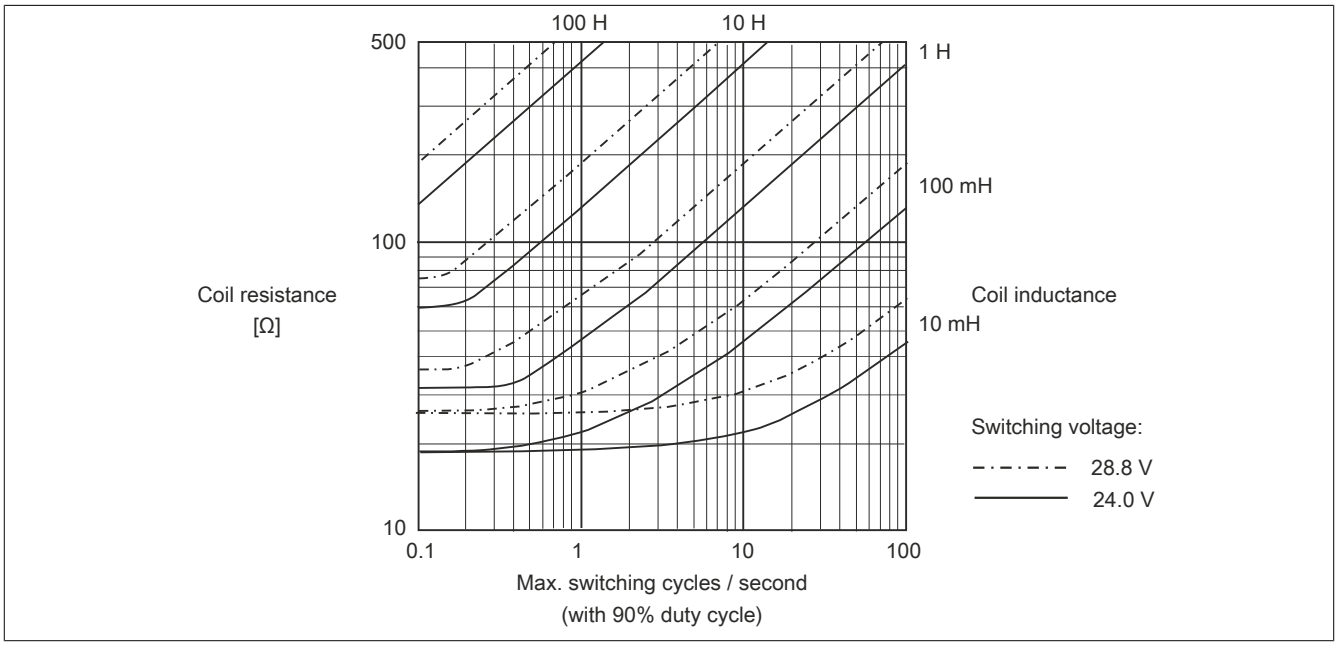


4.15.26.9 Switching inductive loads

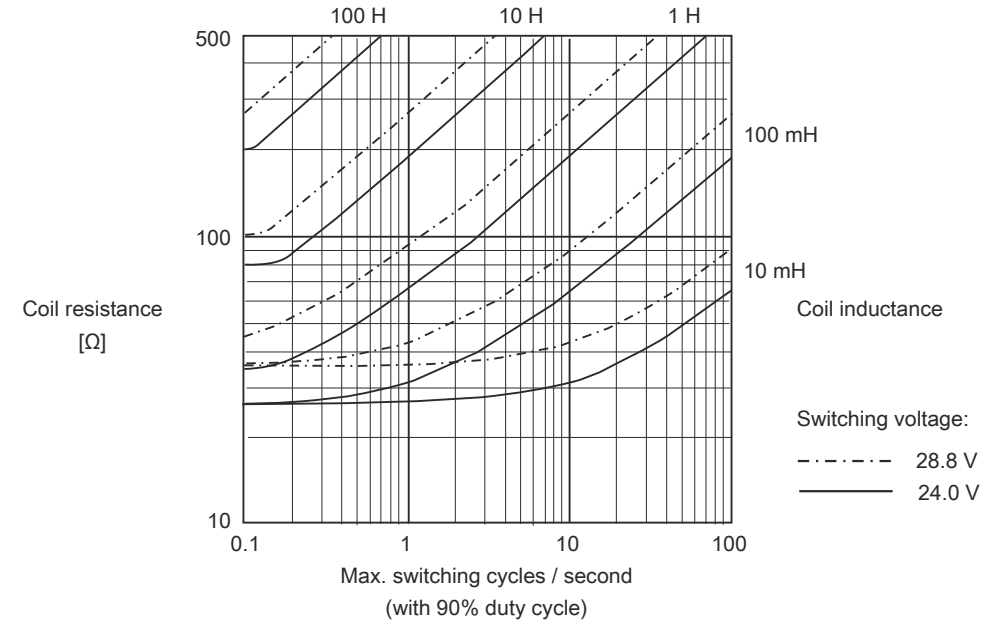
Environmental temperature: 35°C, 4 outputs (1,3,5,7 or 2,4,6,8) with the same load.



Environmental temperature: 60°C, 4 outputs (1,3,5,7 or 2,4,6,8) with the same load.



Environmental temperature: 60°C, all outputs with the same load.



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.26.10 Derating

The outputs of the module can handle up to 2 A. With a total current of 8 A, no more than 4 channels are operable at full load. To ensure optimal use of the module, it is important to assign the channels properly, and to keep in mind a potential derating.

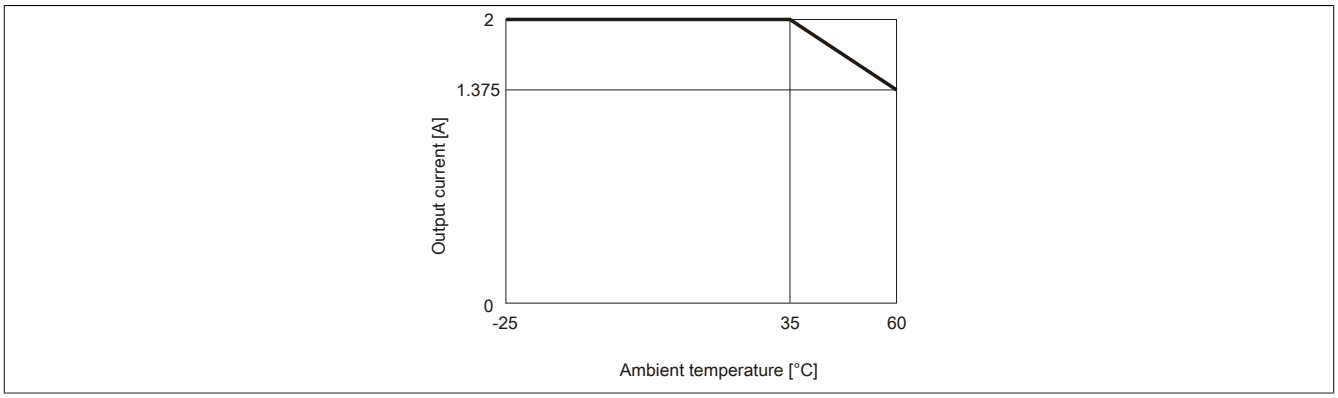
Correct channel assignment is important, since the eight outputs are divided between two output drivers. The channels operated with 2A must therefore be evenly divided between both output drivers.

Output driver 1: Channels 1 - 4
Output driver 2: Channels 5 - 8

The following table provides an overview of the number of fully used channels, the resulting best distribution, and a potential derating.

Number of channels using 2A	Division	Derating
1	Any	No
2	1st channel with 2 A ... channel no. 1 - 4 2nd channel with 2 A ... channel no. 5 - 8	No
3	Assign all even or all odd channel numbers. Examples: 1, 3, 5 2, 4, 6 3, 5, 7 4, 6, 8	 Channels 1 and 3 Channels 2 and 4 Channels 5 and 7 Channels 6 and 8
4	Assign all even or all odd channel numbers. Possible distributions: 1, 3, 5, 7 2, 4, 6, 8	 All channels All channels

Derating when 3 or 4 channels are operated with 2 A:



Information:

Modules next to this module can have a maximum power consumption of 1.5 W.

4.15.26.11 Register description

4.15.26.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.26.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	1	StatusInput01	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		PowerSupply01	Bit 2	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.26.11.3 Function model 1 - Output switching

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
4	1	Switching state of delayed digital outputs 1 to 8	USINT			•	
		DigitalOutput01Delayed	Bit 0				
		...	...				
		DigitalOutput08Delayed	Bit 7				
6	2	Switching mask after the delay time has expired	USINT			•	
		DigitalOutput01DelayEnable	Bit 0				
		...	...				
		DigitalOutput08DelayEnable	Bit 7				
8	3	Setting the delay (OutputDelayTime)	USINT			•	
30	1	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		PowerSupply01	Bit 2	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.26.11.4 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
8192	-	Reading the module ID	UINT		•		
8196	-	Status of the supply voltage	USINT		•		
		Power Supply01	Bit 2		•		

1) The offset specifies where the register is within the CAN object.

4.15.26.11.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.26.11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.26.11.5.1 Switching state of digital outputs 1 to 8

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput08

The switching state of digital outputs 1 to 8 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("DigitalOutput").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

4.15.26.11.6 Reading the module ID

Name:
asy_ModulID

This register offers another possibility for reading the module ID.

Data type	Value
UINT	Module ID

4.15.26.11.7 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.26.11.7.1 Status of digital outputs 1 to 8

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput08

This register is used to indicate the status of digital outputs 1 to 8.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of this registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput0x") or whether this register should be displayed as an individual USINT data point ("StatusInput01").

Data type	Value	Information
USINT	0 to 255	Packed outputs = on
	See bit structure	Packed outputs = off or function model <> 0 - Standard

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
8	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

4.15.26.11.8 Operating limit monitoring

The module's output supply is monitored. An I/O supply voltage of <20.4 V is displayed as a warning.

4.15.26.11.8.1 Status of the supply voltage

Name:
asy_SupplyStatus

The status of the I/O supply voltage is mapped in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	PowerSupply01	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - 7	Reserved	0	

4.15.26.11.9 Additional function - switch digital outputs w/ delay using switching mask

In function model 1 - Output switching, it is possible to control the digital outputs with a delay.

The OutputDelay mask can be used to activate the delay for each channel individually. The module is controlled here using a 100 µs-based timer and the Output or OutputDelayed register.

Behavior of function model 1 - Output switching

With a timer delay of 0:

Output: DigitalOutput0x bits

When the delay is changed:

The bit string for DigitalOutput0x bits is output. The timer restarts.

Output: DigitalOutput0x bits

After delay time has expired:

The channels with bits set in the OutputDelay mask are adapted to the respective OutputDelayed bits.

Output: DigitalOutput0x bits (if Enable bit = FALSE)
OutputDelayed bits (if Enable bit = TRUE)

Information:

Adjusting the output and restarting the timer take place immediately after transferring the new delay, even if the previous time has not yet passed.

4.15.26.11.9.1 Switching state of delayed digital outputs 1 to 8

Name:
DigitalOutput01Delayed to Digital08Delayed

According to the corresponding bit in the OutputDelay mask, the switching state of all digital outputs 1 to 8 are stored in the OutputDelayed bits after the delay time has expired.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01Delayed	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08Delayed	0	Digital output 08 reset
		1	Digital output 08 set

Information:

After the delay time has expired, only the channels with a bit set in the OutputDelay mask are adjusted to the OutputDelayed bits.

4.15.26.11.9.2 Switching mask after the delay time has expired

Name:
DigitalOutput01DelayEnable to DigitalOutput08DelayEnable

These registers create the mask for OutputDelay. They define which outputs are switched to the bit string for the OutputDelayed register after the delay time has expired.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01DelayEnable	0	Digital output 01 remains unchanged
		1	Digital output 01 is toggled
...		...	
7	DigitalOutput08DelayEnable	0	Digital output 08 remains unchanged
		1	Digital output 08 is toggled

4.15.26.11.9.3 Setting the delay

Name:
OutputDelayTime

This register can be used to set the delay in 100 µs steps.

After the delay time has expired, the digital outputs are adjusted according to the switching mask (register 6) and the delayed output pattern (register 4).

Data type	Value
USINT	0 to 255 (in 100 µs steps)[1)]

1) The value 0 disables processing

4.15.26.11.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard function model	100 µs
Bus controller function model	150 µs

4.15.26.11.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Function model 0	Equal to the minimum cycle time
Function model 1	Equal to the minimum cycle time

4.15.27 X20(c)DO9321

4.15.27.1 General information

The module is equipped with 12 outputs for 1-wire connections. The module is designed for sink output wiring.

- 12 digital outputs
- Sink connection
- 1-wire connections
- Integrated output protection

4.15.27.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.27.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO9321	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections	
X20cDO9321	X20 digital output module, coated, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 345: X20DO9321, X20cDO9321 - Order data

4.15.27.4 Technical data

Product ID	X20DO9321	X20cDO9321
Short description		
I/O module	12 digital outputs 24 VDC for 1-wire connections	
General information		
B&R ID code	0x1B9B	0xE22D
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	
Power consumption		
Bus	0.26 W	
Internal I/O	0.99 W	
Additional power dissipation caused by the actuators (resistive) [W] [1]	+0.36	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
Digital outputs		
Design	FET negative switching	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	0.5 A	
Total nominal current	6 A	
Connection type	1-wire connections	
Output circuit	Sink	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	75 µA	
$R_{DS(on)}$	120 mΩ	
Peak short circuit current	<7 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay		
0 -> 1	<300 µs	
1 -> 0	<300 µs	
Switching frequency		
Resistive load	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 346: X20DO9321, X20cDO9321 - Technical data

Product ID	X20DO9321	X20cDO9321
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 346: X20DO9321, X20cDO9321 - Technical data

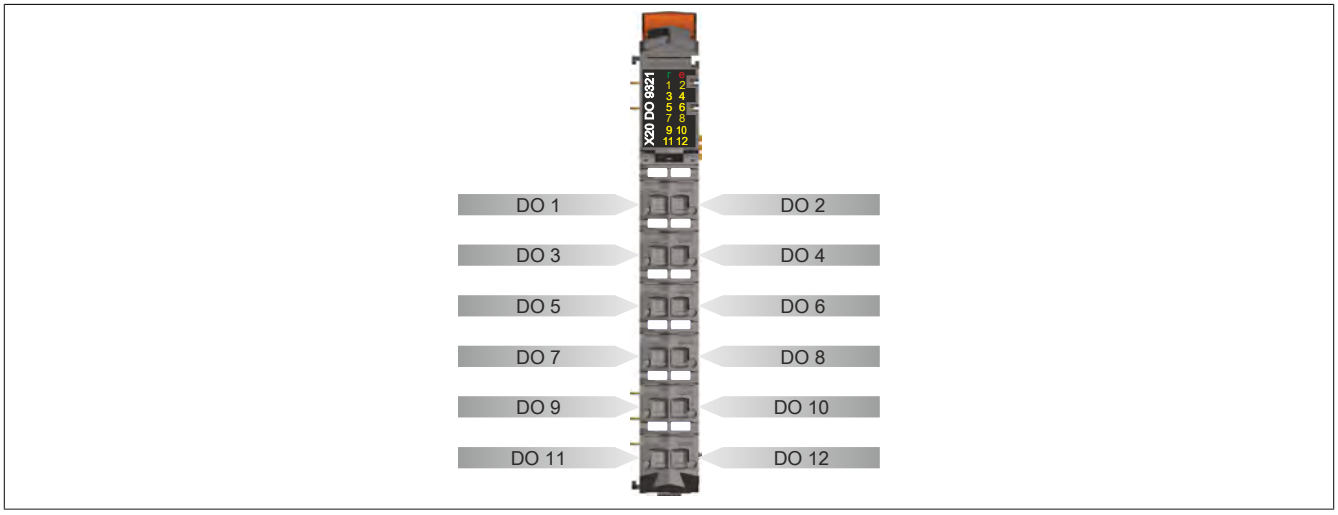
1) Number of outputs x $R_{DS(on)}$ x nominal output current^2
2) Ta min.: 0°C
   Ta max.: See environmental conditions

4.15.27.5 Status LEDs

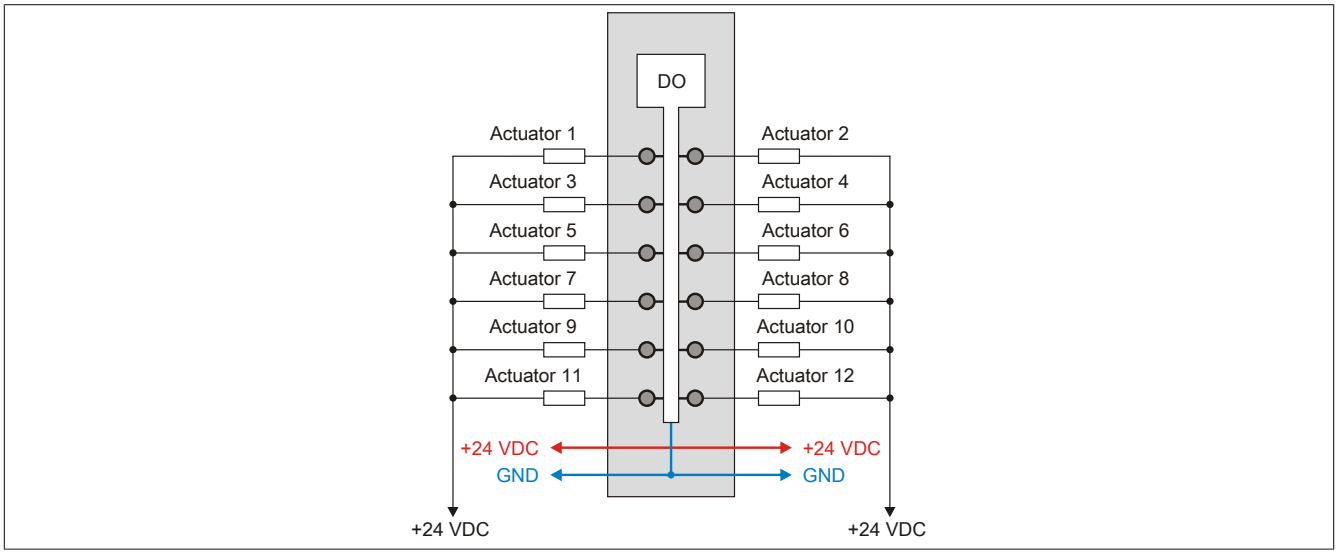
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 12	Orange		Output status of the corresponding digital output

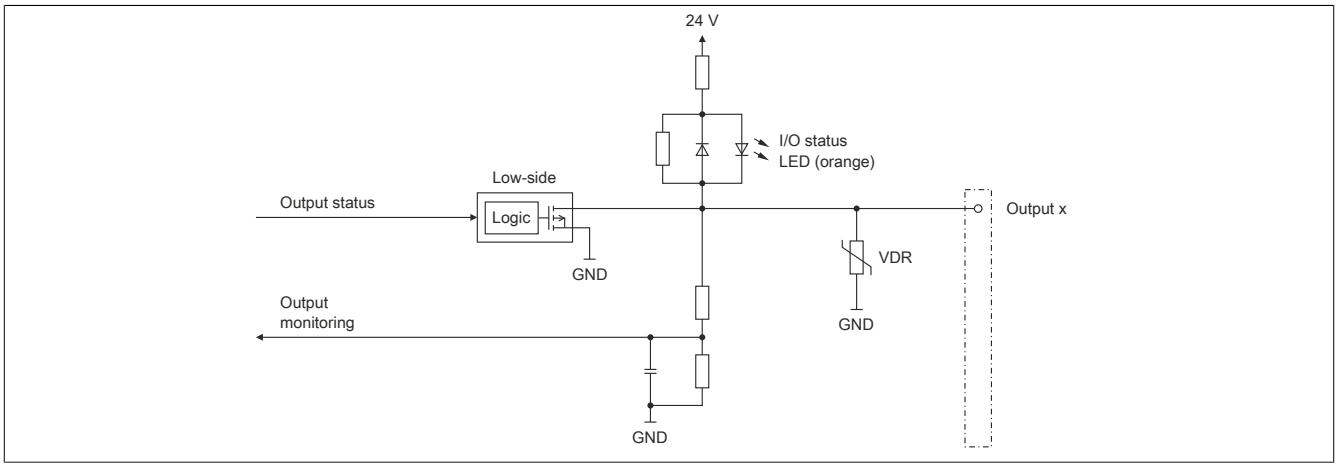
4.15.27.6 Pinout



4.15.27.7 Connection example



4.15.27.8 Output circuit diagram



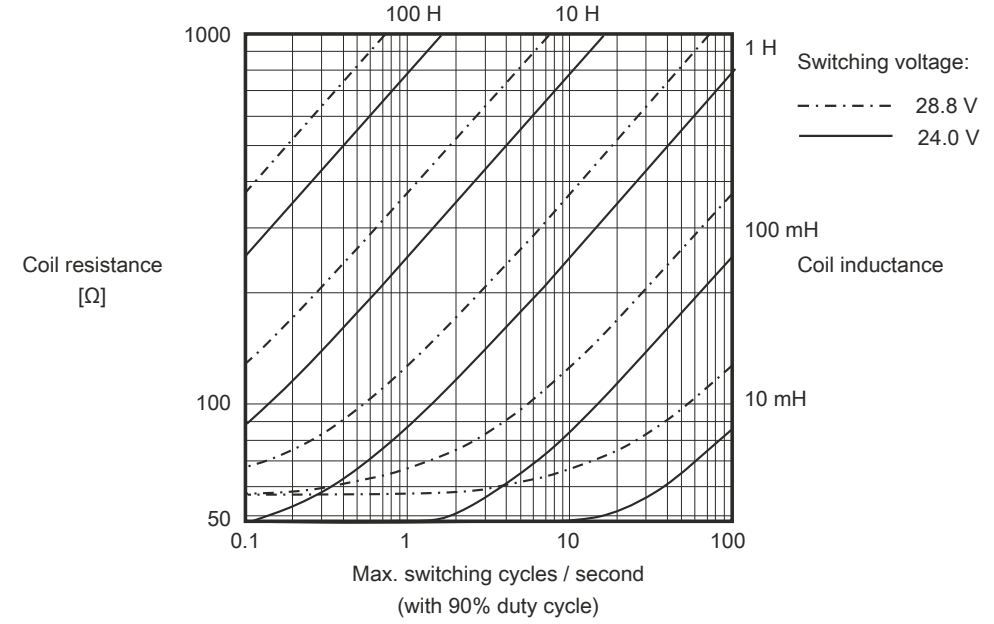
4.15.27.9 Derating

There is no derating when operated below 55°C.

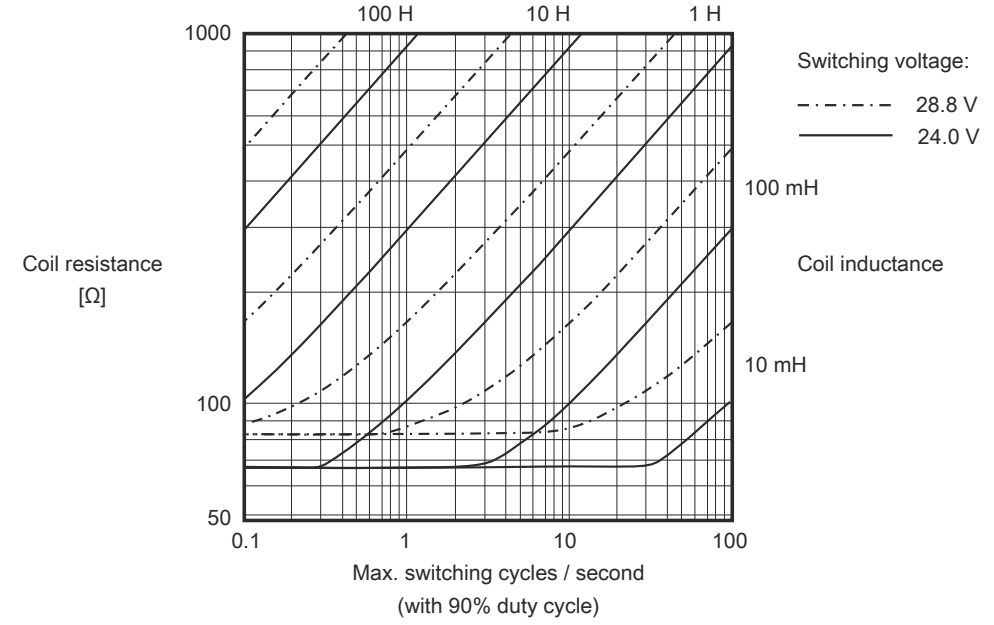
When operated at temperatures above 55°C, the maximal total current per channel is limited to 0,35 A

4.15.27.10 Switching inductive loads

Environmental temperature: 55°C, all outputs with the same load



Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.27.11 Register description

4.15.27.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.27.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
	1	DigitalOutput	UINT			•	
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
3	1	Switching state of digital outputs 9 to 12	USINT			•	
		DigitalOutput09	Bit 0				
		...	...				
		DigitalOutput12	Bit 3				
	1	StatusInput01	UINT	•			
30	1	Status of digital outputs 1 to 8	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
31	2	Status of digital outputs 9 to 12	USINT	•			
		StatusDigitalOutput09	Bit 0				
		...	...				
		StatusDigitalOutput12	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.27.11.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
3	1	Switching state of digital outputs 9 to 12	USINT			•	
		DigitalOutput09	Bit 0				
		...	...				
		DigitalOutput12	Bit 3				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
31	-	Status of digital outputs 9 to 12	USINT		•		
		StatusDigitalOutput09	Bit 0				
		...	...				
		StatusDigitalOutput12	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.15.27.11.3.1 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN-I/O.

4.15.27.11.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.27.11.4.1 Switching state of digital outputs 1 to 12

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput12

The switching state of digital outputs 1 to 12 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of these registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput12") or whether these registers should be displayed as an individual UINT data point ("DigitalOutput").

Data type	Value
UINT	Packed "DigitalOutput" values
USINT	See bit structure

Bit structure:

Register 2, Offset 0:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

Register 3, Offset 1:

Bit	Name	Value	Information
0	DigitalOutput09	0	Digital output 09 reset
		1	Digital output 09 set
...		...	
3	DigitalOutput12	0	Digital output 12 reset
		1	Digital output 12 set

4.15.27.11.5 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.27.11.5.1 Status of digital outputs 1 to 12

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput12

The status of digital outputs 1 to 12 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of these registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput12") or whether these registers should be displayed as an individual UINT data point ("StatusDigitalOutput").

Data type	Value
UINT	Packed "StatusDigitalOutput" values
USINT	See bit structure

Bit structure:

Register 30, (Offset 1):

Bit	Name	Value	Description
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
7	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

Register 31, (Offset 2):

Bit	Name	Value	Information
0	StatusDigitalOutput09	0	Channel 09: No error
		1	Channel 09: Short circuit or overload
...		...	
3	StatusDigitalOutput12	0	Channel 12: No error
		1	Channel 12: Short circuit or overload

4.15.27.11.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.27.11.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.28 X20(c)DO9322

4.15.28.1 General information

The module is equipped with 12 outputs for 1-wire connections. The module is designed for source output wiring.

- 12 digital outputs
- Source connection
- 1-wire connections
- Integrated output protection

4.15.28.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.15.28.3 Order data

Model number	Short description	Figure
	Digital outputs	
X20DO9322	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections	
X20cDO9322	X20 digital output module, coated, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 347: X20DO9322, X20cDO9322 - Order data

4.15.28.4 Technical data

Product ID	X20DO9322	X20cDO9322
Short description		
I/O module	12 digital outputs 24 VDC for 1-wire connections	
General information		
B&R ID code	0x1B9A	0xD578
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software (output error status)	
Power consumption		
Bus	0.26 W	
Internal I/O	1.15 W	
Additional power dissipation caused by the actuators (resistive) [W] 1)	+0.63	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 2)	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Digital outputs		
Design	FET positive switching	
Nominal voltage	24 VDC	
Switching voltage	24 VDC -15 % / +20 %	
Nominal output current	0.5 A	
Total nominal current	6 A	
Connection type	1-wire connections	
Output circuit	Source	
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	5 µA	
$R_{DS(on)}$	210 mΩ	
Max. continuous current	6 A	
Peak short circuit current	<12 A	
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)	
Switching delay 3)		
0 -> 1	<300 µs	
1 -> 0	<300 µs	
Switching frequency		
Resistive load 3)	Max. 500 Hz	
Inductive load	See section "Switching inductive loads"	
Braking voltage when switching off inductive loads	Typ. 50 VDC	
Isolation voltage between channel and bus	500 V_{eff}	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 348: X20DO9322, X20cDO9322 - Technical data

Product ID	X20DO9322	X20cDO9322
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 348: X20DO9322, X20cDO9322 - Technical data

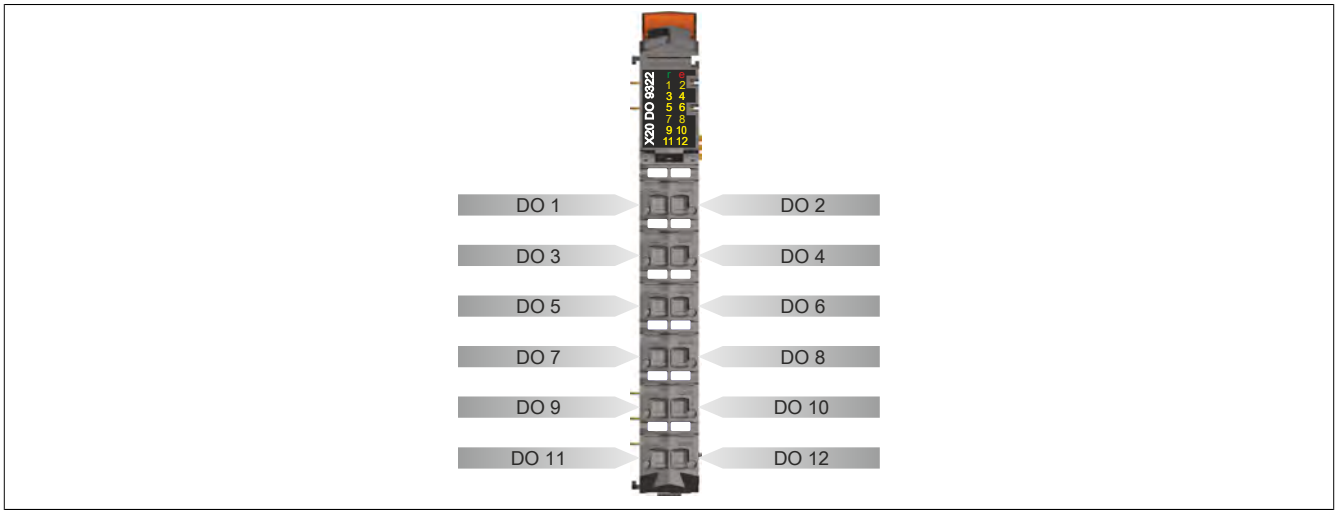
1) Number of outputs x $R_{DS(on)}$ x nominal output current^2
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) @ ≤ 1 kΩ

4.15.28.5 Status LEDs

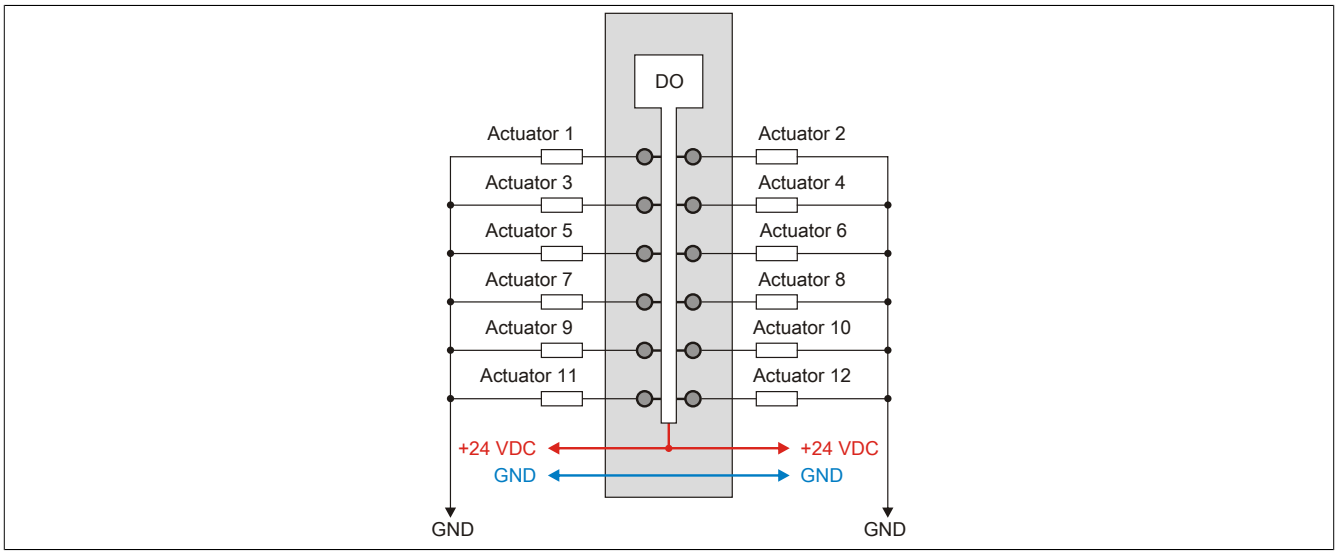
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 12	Orange		Output status of the corresponding digital output

4.15.28.6 Pinout



4.15.28.7 Connection example

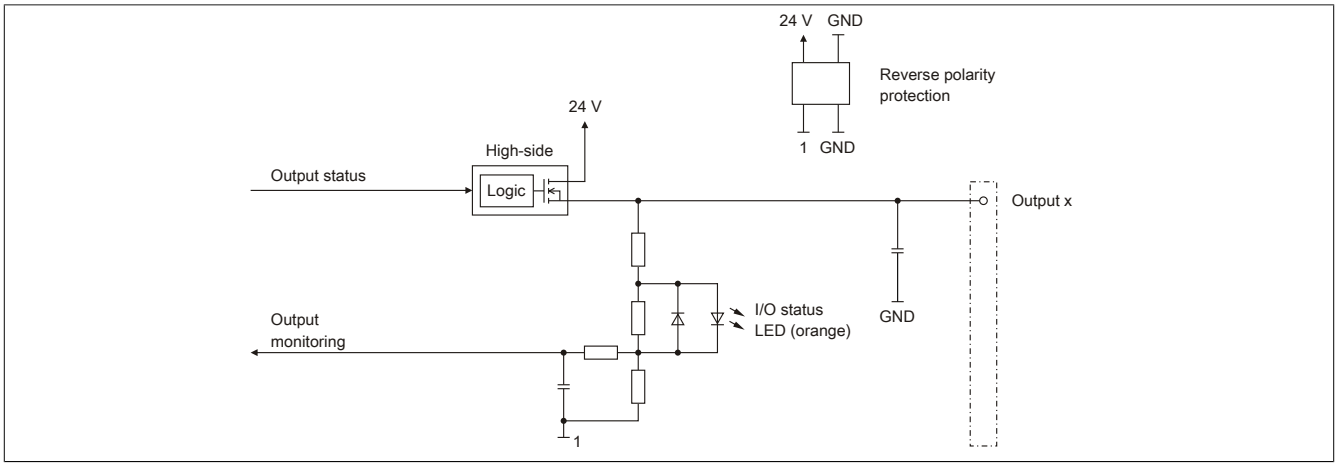


Caution!

If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

Therefore sufficient cable cross sections or external safety measures must be used.

4.15.28.8 Output circuit diagram



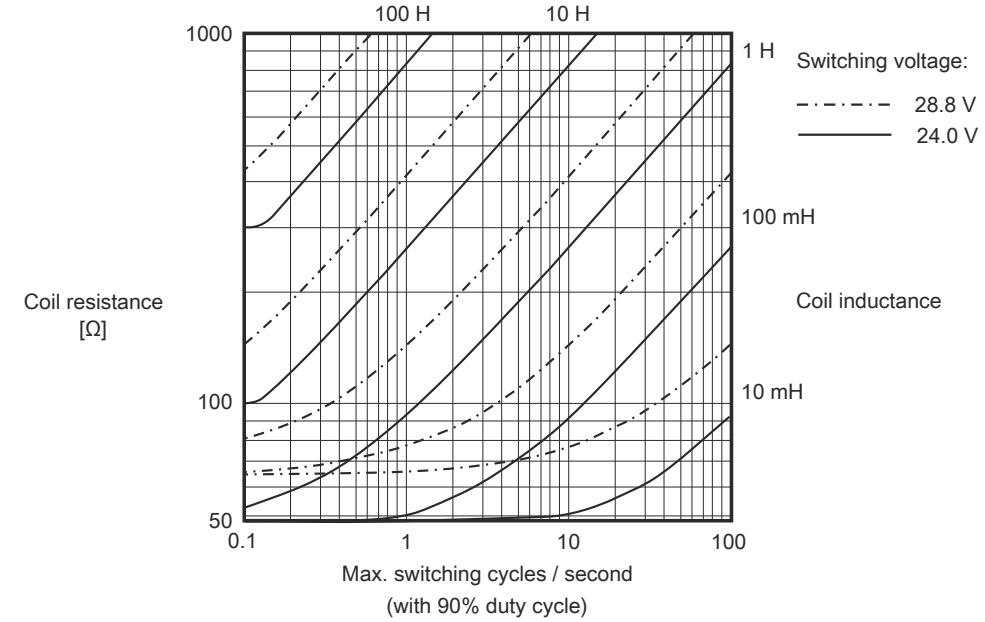
4.15.28.9 Derating

There is no derating when operated below 55°C.

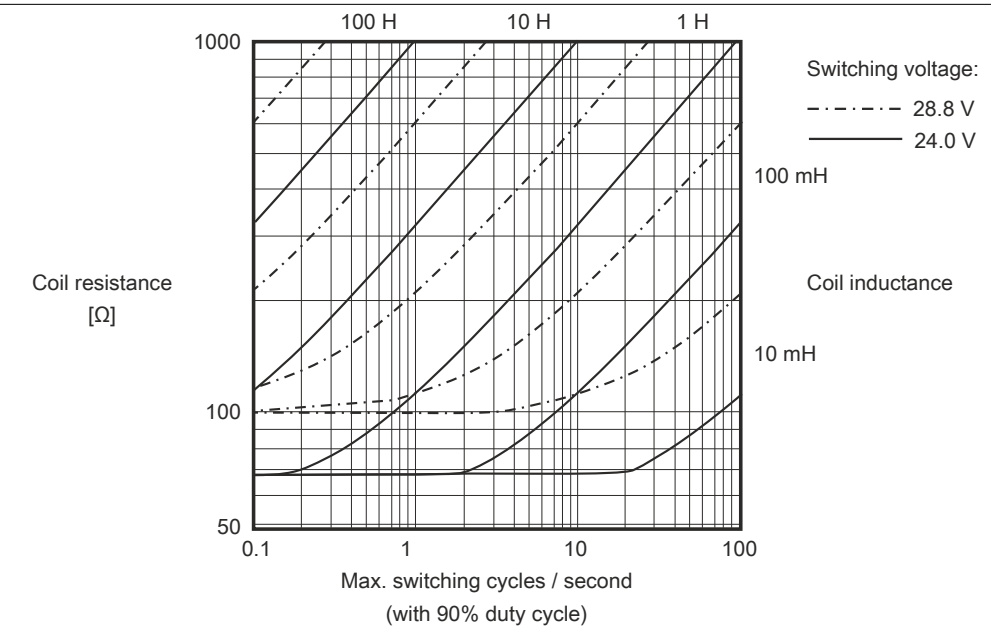
When operated at temperatures above 55°C, the maximal total current per channel is limited to 0,35 A

4.15.28.10 Switching inductive loads

Environmental temperature: 55°C, all outputs with the same load



Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.28.11 Register description

4.15.28.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.28.11.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
	1	DigitalOutput	UINT			•	
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
3	1	Switching state of digital outputs 9 to 12	USINT			•	
		DigitalOutput09	Bit 0				
		...	...				
		DigitalOutput12	Bit 3				
	1	StatusInput01	UINT	•			
30	1	Status of digital outputs 1 to 8	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
31	2	Status of digital outputs 9 to 12	USINT	•			
		StatusDigitalOutput09	Bit 0				
		...	...				
		StatusDigitalOutput12	Bit 3				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.28.11.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
3	1	Switching state of digital outputs 9 to 12	USINT			•	
		DigitalOutput09	Bit 0				
		...	...				
		DigitalOutput12	Bit 3				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
31	-	Status of digital outputs 9 to 12	USINT		•		
		StatusDigitalOutput09	Bit 0				
		...	...				
		StatusDigitalOutput12	Bit 3				

1) The offset specifies where the register is within the CAN object.

4.15.28.11.3.1 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN-I/O.

4.15.28.11.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.28.11.4.1 Switching state of digital outputs 1 to 12

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput12

The switching state of digital outputs 1 to 12 are stored in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of these registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput12") or whether these registers should be displayed as an individual UINT data point ("DigitalOutput").

Data type	Value
UINT	Packed "DigitalOutput" values
USINT	See bit structure

Bit structure:

Register 2, Offset 0:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

Register 3, Offset 1:

Bit	Name	Value	Information
0	DigitalOutput09	0	Digital output 09 reset
		1	Digital output 09 set
...		...	
3	DigitalOutput12	0	Digital output 12 reset
		1	Digital output 12 set

4.15.28.11.5 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.28.11.5.1 Status of digital outputs 1 to 12

Name:
StatusInput01
StatusDigitalOutput01 to StatusDigitalOutput12

The status of digital outputs 1 to 12 is mapped in this register.

Function model 0 - Standard only:

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of these registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput12") or whether these registers should be displayed as an individual UINT data point ("StatusDigitalOutput").

Data type	Value
UINT	Packed "StatusDigitalOutput" values
USINT	See bit structure

Bit structure:

Register 30, (Offset 1):

Bit	Name	Value	Description
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
7	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

Register 31, (Offset 2):

Bit	Name	Value	Information
0	StatusDigitalOutput09	0	Channel 09: No error
		1	Channel 09: Short circuit or overload
...		...	
3	StatusDigitalOutput12	0	Channel 12: No error
		1	Channel 12: Short circuit or overload

4.15.28.11.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.28.11.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.29 X20DOD322

4.15.29.1 General information

The X20DOD322 module is equipped with eight outputs for 1-wire or 2-wire connections. The X20DOD322 is designed for source output wiring.

- 8 digital outputs
- Source connection
- 2-wire connections
- GND for signal supply
- Integrated output protection

4.15.29.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DOD322	X20 digital output module, 8 outputs, 24 VDC, 0.5 A, source, 2-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 349: X20DOD322 - Order data

4.15.29.3 Technical data

Product ID	X20DOD322
Short description	
I/O module	8 digital outputs 24 VDC for 1- or 2-wire connections
General information	
B&R ID code	0xC0E9
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.19 W
Internal I/O	0.8 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+0.28 W
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital outputs	
Design	FET positive switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	4 A
Connection type	1- or 2-wire connections
Output circuit	Source

Table 350: X20DOD322 - Technical data

Product ID	X20DOD322
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
$R_{DS(on)}$	140 mΩ
Max. continuous current	6 A
Peak short circuit current	<3 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay 3)	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load 3)	Max. 500 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 45 VDC
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 350: X20DOD322 - Technical data

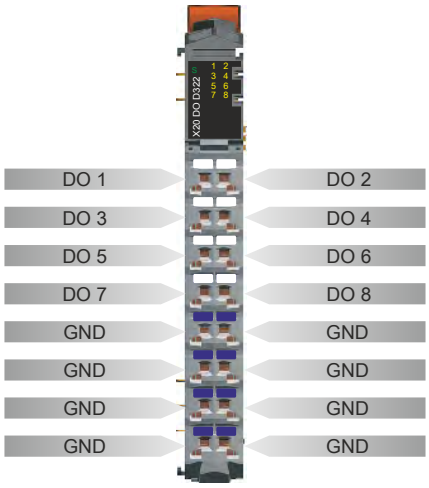
1) Number of outputs x $R_{DS(on)}$ x Nominal output current² (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) At loads ≤ 1 kΩ

4.15.29.4 Status LEDs

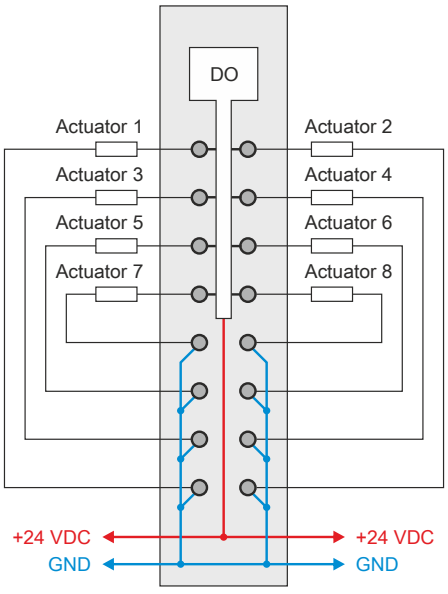
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	S	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
		Red on / Green single flash		Invalid firmware
	1 - 8	Orange		Output status of the corresponding digital output

4.15.29.5 Pinout



4.15.29.6 Connection example

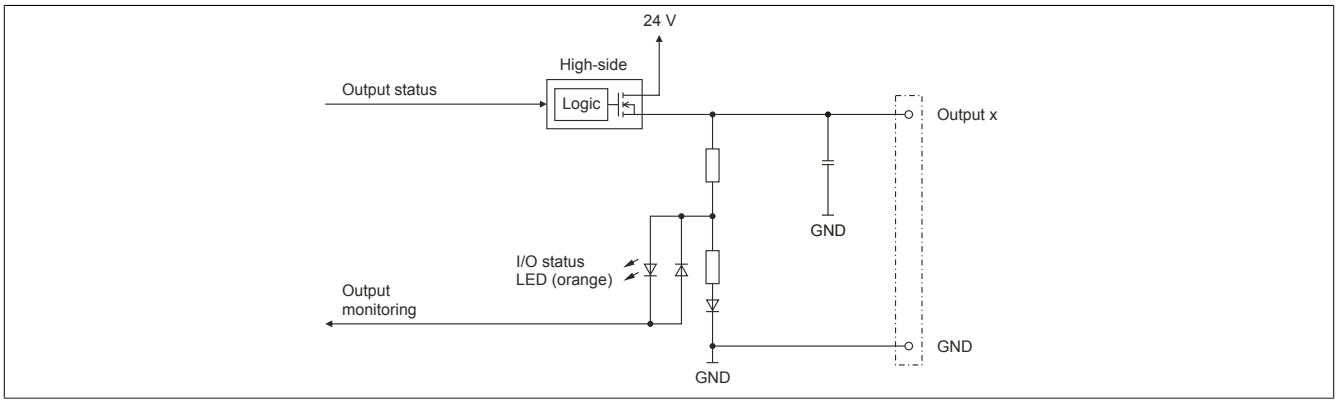


Caution!

If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

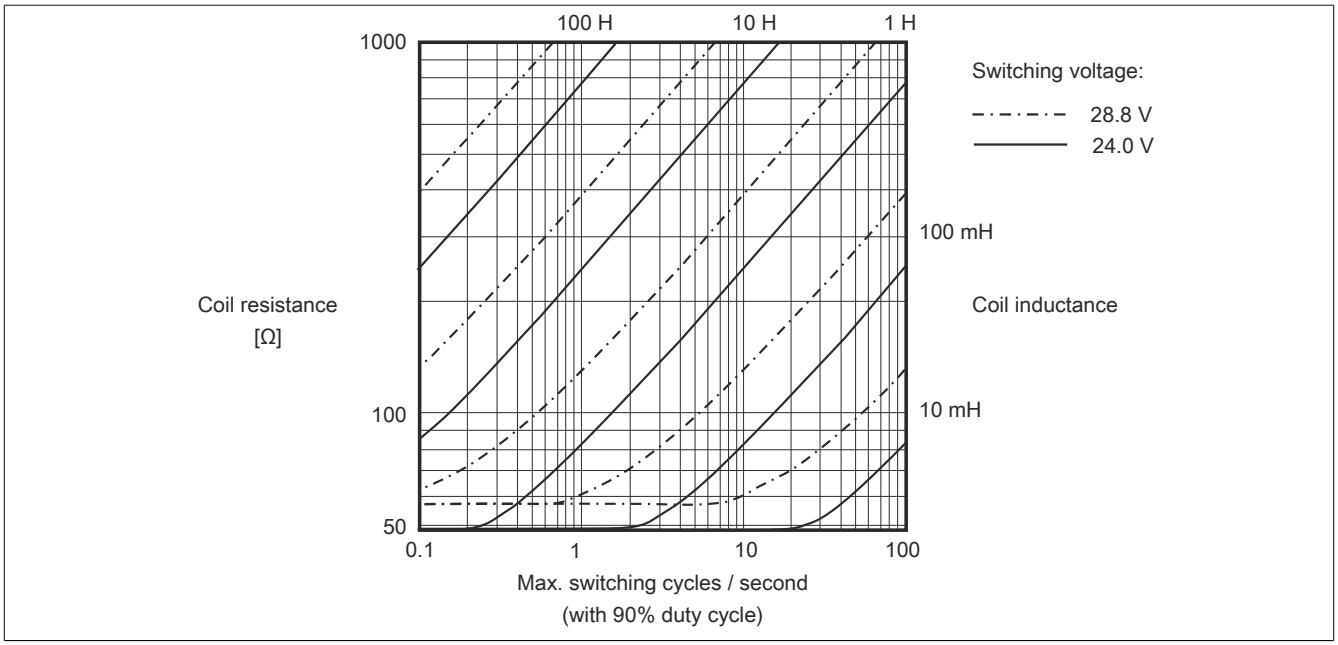
Therefore sufficient cable cross sections or external safety measures must be used.

4.15.29.7 Output circuit diagram



4.15.29.8 Switching inductive loads

Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.29.9 Register description

4.15.29.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.29.9.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	DigitalOutput	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	1	StatusDigitalOutput	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.29.9.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				

1) The offset specifies where the register is within the CAN object.

4.15.29.9.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.15.29.9.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.29.9.4.1 Switching state of digital outputs 1 to 8

Name:
DigitalOutput or
DigitalOutput01 to DigitalOutput08

The switching state of digital outputs 1 to 8 are stored in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of these registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput16") or whether these registers should be displayed as an individual UINT data point ("DigitalOutput").

4.15.29.9.5 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.29.9.5.1 Status of digital outputs 1 to 8

Name:
StatusDigitalOutput or
StatusDigitalOutput01 to StatusDigitalOutput08

The status of digital outputs 1 to 8 is mapped in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
8	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of these registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput16") or whether these registers should be displayed as an individual UINT data point ("StatusDigitalOutput").

4.15.29.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.29.9.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.15.30 X20DOF322

4.15.30.1 General information

The X20DOF322 module is equipped with 16 outputs for 1-wire connections. The X20DOF322 is designed for source output wiring.

- 16 digital outputs
- Source connection
- 1-wire connections
- Integrated output protection

4.15.30.2 Order data

Model number	Short description	Figure
	Digital outputs	
X20DOF322	X20 digital output module, 16 outputs, 24 VDC, 0.5 A, source, 1-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 351: X20DOF322 - Order data

4.15.30.3 Technical data

Product ID	X20DOF322
Short description	
I/O module	16 digital outputs 24 VDC for 1-wire connections
General information	
B&R ID code	0xC0EA
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.28 W
Internal I/O	0.95 W
Additional power dissipation caused by the actuators (resistive) [W] [1)]	+0.56 W
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital outputs	
Design	FET positive switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	8 A
Connection type	1-wire connections
Output circuit	Source
Output protection	Thermal cutoff if overcurrent or short circuit occurs (see value "Peak short circuit current") Internal inverse diode for switching inductive loads (see section "Switching inductive loads")
Diagnostic status	Output monitoring with 10 ms delay

Table 352: X20DOF322 - Technical data

Product ID	X20DOF322
Leakage current when switched off	5 µA
$R_{DS(on)}$	140 mΩ
Max. continuous current	6 A
Peak short circuit current	<3 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay 3)	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load 3)	Max. 500 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 45 VDC
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 352: X20DOF322 - Technical data

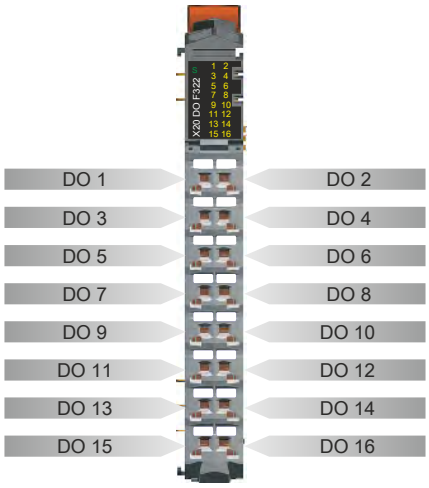
1) Number of outputs x $R_{DS(on)}$ x Nominal output current^2 (A calculation example can be found on the B&R website in the download area for the module.)
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) At loads ≤ 1 kΩ

4.15.30.4 Status LEDs

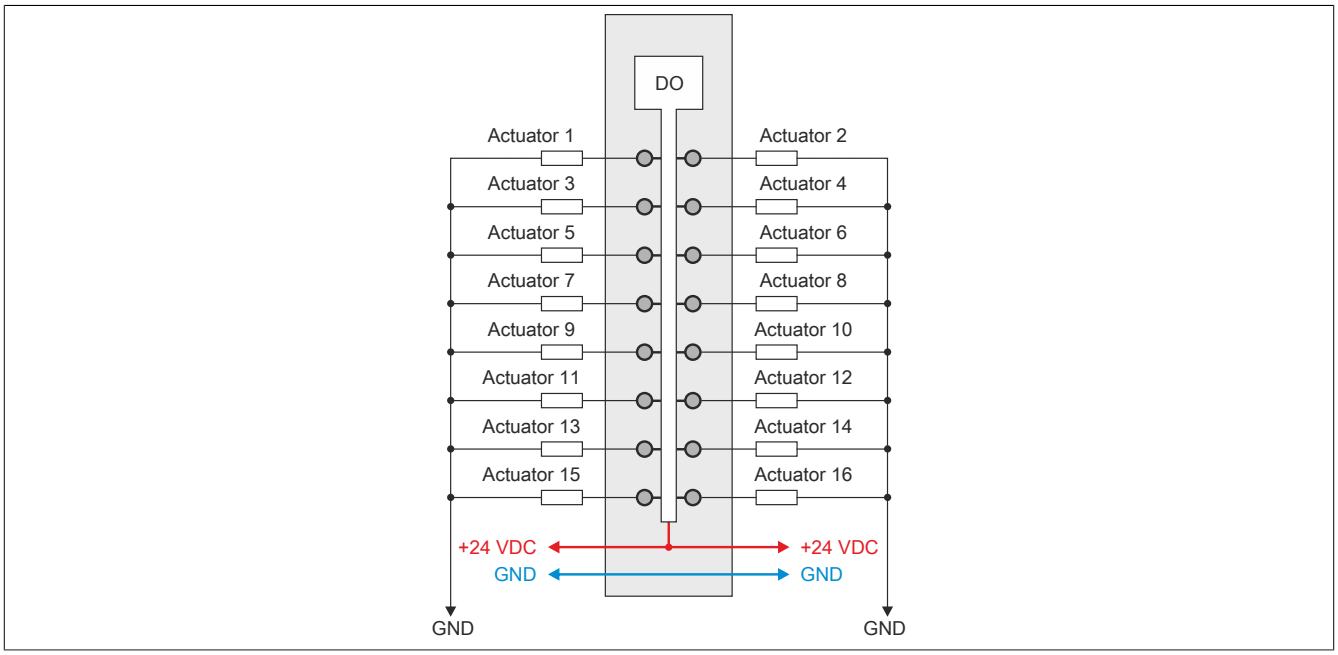
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	S	Green	Off	Module supply not connected
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	Module supply not connected or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
		Red on / Green single flash		Invalid firmware
	1 - 16	Orange		Output status of the corresponding digital output

4.15.30.5 Pinout



4.15.30.6 Connection example

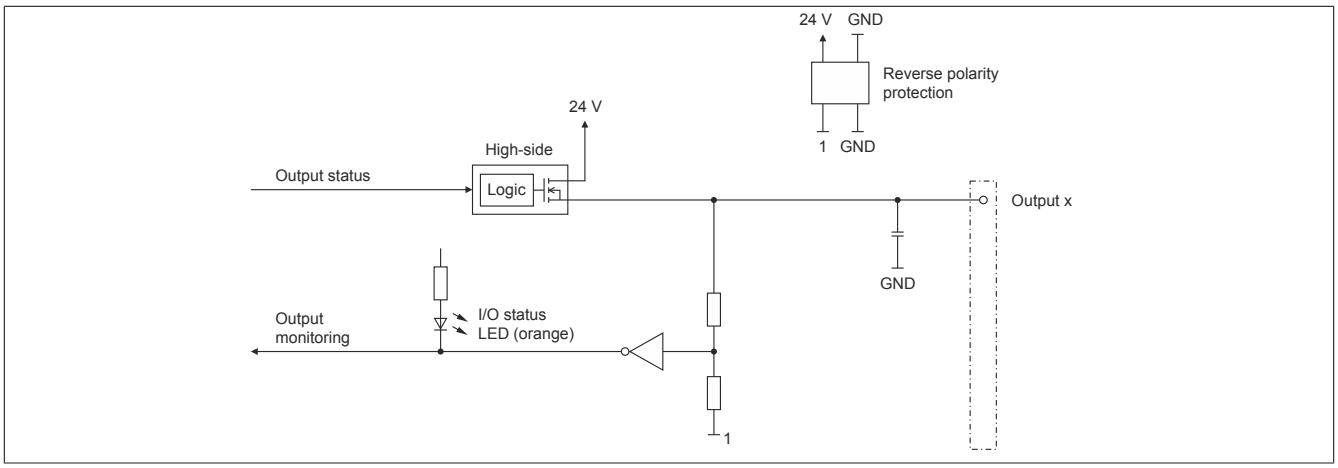


Caution!

If the module is operated outside of specifications, the output current can increase above the maximum permissible nominal current. This applies to individual channels and also to the summation current for the module.

Therefore sufficient cable cross sections or external safety measures must be used.

4.15.30.7 Output circuit diagram



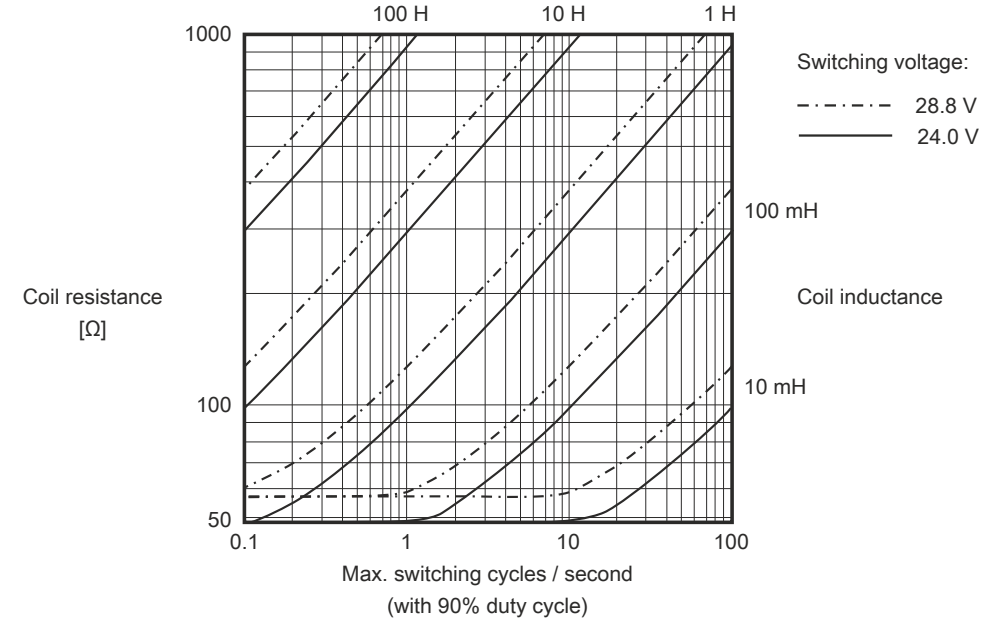
4.15.30.8 Derating

There is no derating when operated below 55°C.

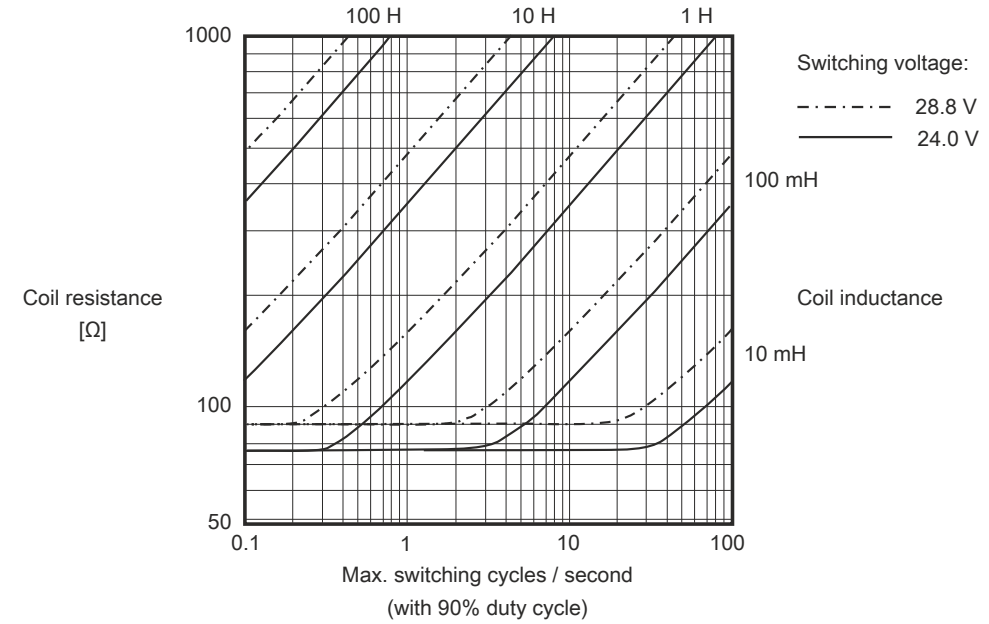
When operated at temperatures above 55°C, the maximal total current per channel is limited to 0,35 A

4.15.30.9 Switching inductive loads

Environmental temperature: 55°C, all outputs with the same load



Environmental temperature: 60°C, all outputs with the same load



Information:

If the maximum number of operating cycles per second is exceeded, an external inverse diode must be used.

Operating conditions outside of the area in the diagram are not permitted!

4.15.30.10 Register description

4.15.30.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.15.30.10.2 Function model 0 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
	0	DigitalOutput	UINT			•	
2	0	Switching state of digital outputs 1 to 8	USINT				
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
3	1	Switching state of digital outputs 9 to 16	USINT				
		DigitalOutput09	Bit 0				
		...	...				
		DigitalOutput16	Bit 7				
	2	StatusDigitalOutput	UINT		•		
30	2	Status of digital outputs 1 to 8	USINT				
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
31	3	Status of digital outputs 9 to 16	USINT				
		StatusDigitalOutput09	Bit 0				
		...	...				
		StatusDigitalOutput16	Bit 7				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Acyclic access continues to be based on the register numbers.

4.15.30.10.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
3	1	Switching state of digital outputs 9 to 16	USINT				
		DigitalOutput09	Bit 0				
		...	...				
		DigitalOutput16	Bit 7				
30	-	Status of digital outputs 1 to 8	USINT		•		
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
31	-	Status of digital outputs 9 to 16	USINT				
		StatusDigitalOutput09	Bit 0				
		...	...				
		StatusDigitalOutput16	Bit 7				

1) The offset specifies where the register is within the CAN object.

4.15.30.10.3.1 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN-I/O.

4.15.30.10.4 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.15.30.10.4.1 Switching state of digital outputs 1 to 16

Name:
DigitalOutput or
DigitalOutput01 to DigitalOutput16

The switching state of digital outputs 1 to 16 are stored in this register.

Data type	Value
UINT	Packed "DigitalOutput" values
USINT	See bit structure

Bit structure:

Register 2, Offset 0:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

Register 3, Offset 1:

Bit	Name	Value	Information
0	DigitalOutput09	0	Digital output 09 reset
		1	Digital output 09 set
...		...	
7	DigitalOutput16	0	Digital output 16 reset
		1	Digital output 16 set

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of these registers' bits should be set up individually as data points in the AS I/O mapping ("DigitalOutput01" through "DigitalOutput16") or whether these registers should be displayed as an individual UINT data point ("DigitalOutput").

4.15.30.10.5 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the setpoint states. The control of the output driver is used for the setpoint states.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

4.15.30.10.5.1 Status of digital outputs 1 to 16

Name:
StatusDigitalOutput or
StatusDigitalOutput01 to StatusDigitalOutput16

The status of digital outputs 1 to 16 is mapped in this register.

Data type	Value
UINT	Packed "StatusDigitalOutput" values
USINT	See bit structure

Bit structure:

Register 30, Offset 1:

Bit	Name	Value	Description
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
7	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

Register 31, Offset 2:

Bit	Name	Value	Information
0	StatusDigitalOutput09	0	Channel 09: No error
		1	Channel 09: Short circuit or overload
...		...	
7	StatusDigitalOutput16	0	Channel 16: No error
		1	Channel 16: Short circuit or overload

The "packed outputs" setting in the AS I/O configuration is used to determine whether all of these registers' bits should be set up individually as data points in the AS I/O mapping ("StatusDigitalOutput01" through "StatusDigitalOutput16") or whether these registers should be displayed as an individual UINT data point ("StatusDigitalOutput").

4.15.30.10.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.15.30.10.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
Equal to the minimum cycle time

4.16 Digital signal processing modules

The highly flexible digital signal processor modules can be implemented for a wide range of tasks involving the creation or processing of digital signals.

4.16.1 Brief information

Product ID	Short description	on page
X20CM1201	X20 combination module, 1 AB incremental encoder, 24 V, 4 digital inputs 24 V, 4 channels 24 V configurable as inputs or outputs, flexible digital controller logic	1603
X20DC1073	X20 digital counter module, 1x SinCos, 1 Vss, 400 kHz input frequency, encoder monitoring, NetTime module	1623
X20DS1119	X20 multifunctional digital signal processor, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module	1637
X20DS1319	X20 multifunctional digital signal processor, 4 digital input channels, 4 digital channels configurable as inputs or outputs, 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 2 reference pulses, SSI absolute encoder, NetTime module	1678
X20DS1828	X20 digital signal module, 1 HIPERFACE interface, NetTime module	1720
X20DS1928	X20 digital signal module, 1 EnDat 2.1/2.2 interface, NetTime module	1780
X20DS4389	X20 digital signal module, 4 digital inputs, 24 VDC, 4 digital outputs, 24 VDC, 0.1 A, oversampling I/O functions, time-triggered I/O functions, NetTime module	1833
X20cDS1119	X20 multifunctional digital signal processor, coated, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module	1637

4.16.2 X20CM1201

4.16.2.1 General information

The module can be used to configure and carry out simple movements. For this purpose, the module has one AB encoder input and a total of 8 digital channels. Four of them are inputs, and the other 4 can be set as either an input or an output. Various output bit patterns are stored directly in the module.

The module is perfectly suited for easy to create drive control tasks for program and event controlled motor movements. Feed movements using drives with 2 speeds and forward/reverse movement are created easily and efficiently.

- Command-dependent digital pattern output
- Counter-dependent output circuit
- Event-controlled abort criteria
- 4 digital inputs
- 4 digital channels, configurable as inputs or outputs

4.16.2.2 Order data

Model number	Short description	Figure
	Digital signal processing and preparation	
X20CM1201	X20 combination module, 1 AB incremental encoder, 24 V, 4 digital inputs 24 V, 4 channels 24 V configurable as inputs or outputs, flexible digital controller logic	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 353: X20CM1201 - Order data

4.16.2.3 Technical data

Product ID	X20CM1201
Short description	
I/O module	1 AB incremental encoder, 24 V, 4 digital inputs, 4 channels configurable as inputs or outputs
General information	
Input voltage	24 VDC -15 % / +20 %
B&R ID code	0x21EF
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using the status LED and software (output error status)
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines.
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Digital inputs	
Quantity	4 + 4 additional channels, configurable as inputs or outputs
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Approx. 1.3 mA
Input filter	
Hardware	≤2 µs
Software	-
Connection type	1-wire connections
Input circuit	Sink
Input resistance	18.4 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
AB incremental encoder	
Quantity	1
Encoder inputs	24 V, asymmetrical
Counter size	32-bit
Input frequency	Max. 100 kHz
Evaluation	4x
Encoder supply	Module-internal, max. 600 mA
Overload behavior of the encoder supply	Short circuit protection, overload protection
Digital outputs	
Design	Push / Pull / Push-Pull
Quantity	Up to 4, configurable as inputs or outputs using software
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.1 A
Total nominal current	0.4 A
Connection type	1-wire connections
Output circuit	Sink or source
Output protection	Thermal cutoff if overcurrent or short circuit occurs, integrated protection for switching inductances
Actuator supply	Module-internal, max. 600 mA
Diagnostic status	Output monitoring
Leakage current when switched off	Max. 25 µA
Residual voltage	<0.9 V at 0.1 A rated current
Peak short circuit current	<10 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<2 µs
1 -> 0	<2 µs
Switching frequency	
Resistive load	Max. 24 kHz
Inductive load	See section "Switching inductive loads" (at 90% duty cycle).
Braking voltage when switching off inductive loads	Switching voltage + 0.6 VDC

Table 354: X20CM1201 - Technical data

Product ID	X20CM1201
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 354: X20CM1201 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.16.2.4 LED status indicators

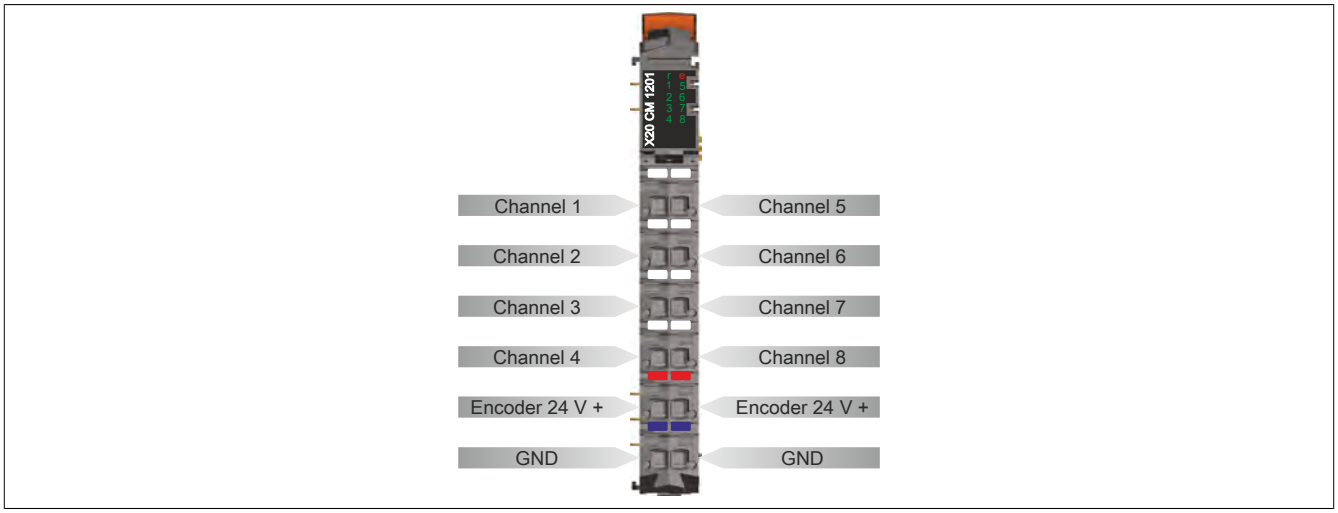
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 8	Green		Status of the corresponding digital signal

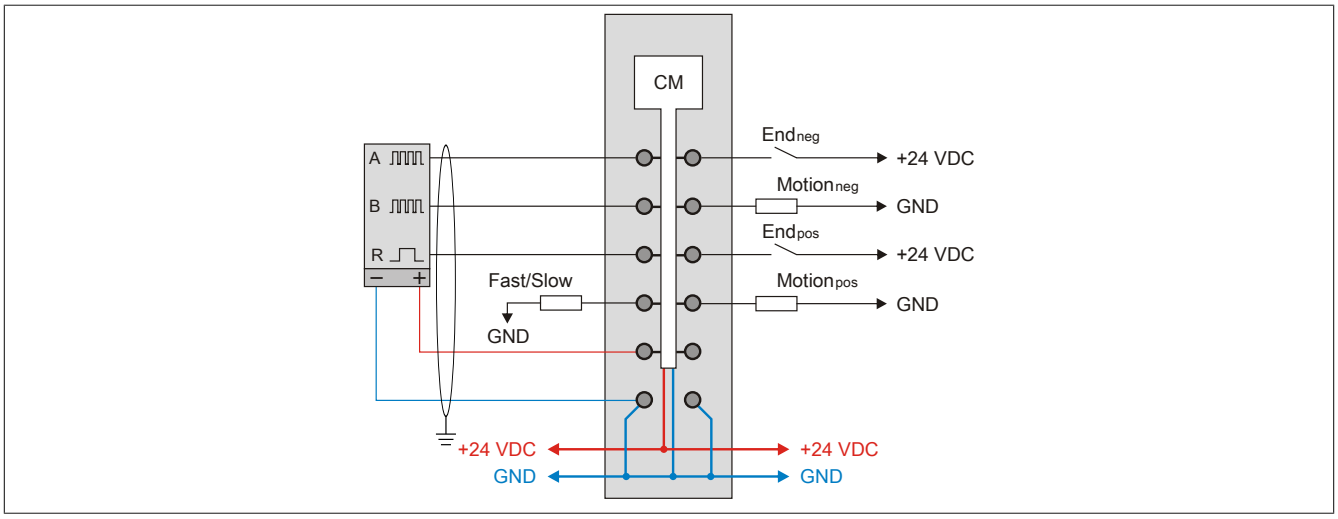
1) Depending on the configuration, a firmware update can take up to several minutes.

4.16.2.5 Pinout

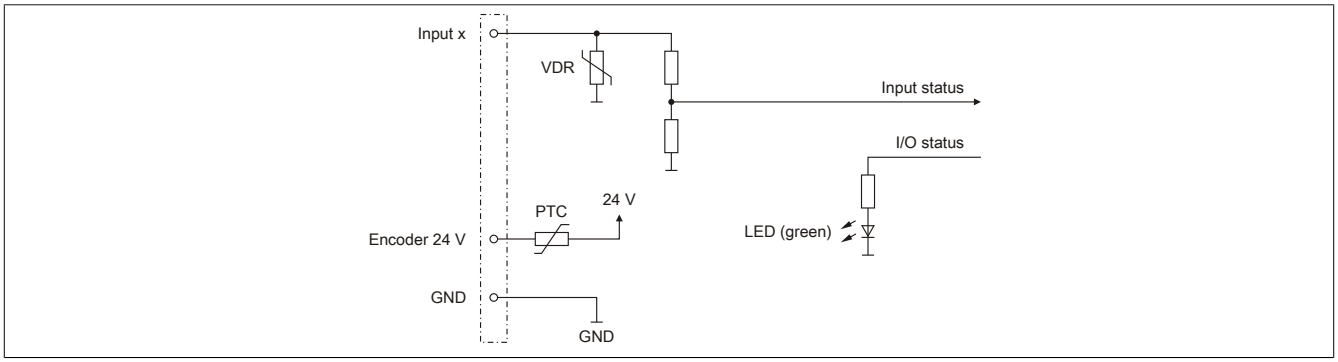
Shielded cables must be used for all signal lines.



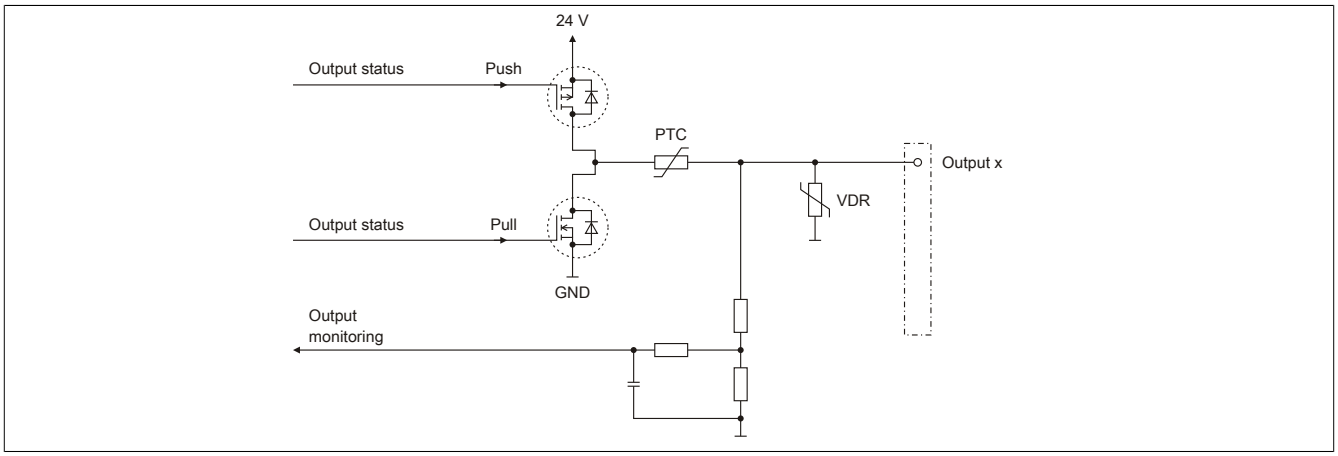
4.16.2.6 Connection example



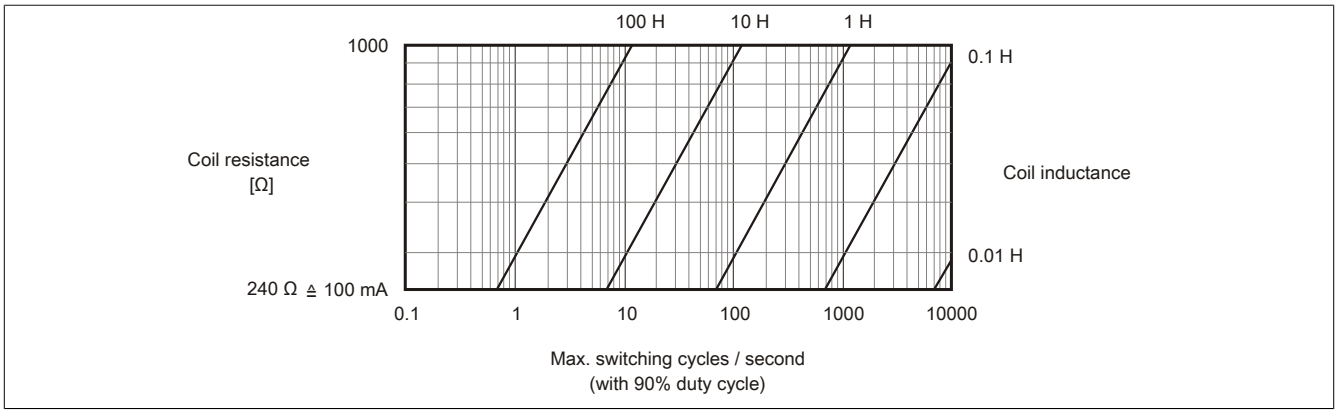
4.16.2.7 Input circuit diagram



4.16.2.8 Output circuit diagram



4.16.2.9 Switching inductive loads



4.16.2.10 Register description

4.16.2.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.16.2.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
130	CycleTimeCff					•
Communication - Command interface						
1	SendCommand	USINT			•	
3	SendCommandParam	USINT			•	
12	SendData	DINT			•	
1	ReadStatus	USINT	•			
3	ReadIndex	USINT	•			
12	ReadData	DINT	•			
Communication - Display register						
20	ABRposition	DINT	•			
28	TargetARBposition	DINT	•			
36	ErrorInfo	UDINT	•			
47	Status of the digital inputs	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
55	Status of encoder supply	USINT	•			
	PowerSupply01	Bit 0				

4.16.2.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
130	-	CycleTimeCff					•
Communication - Command interface							
1	1	SendCommand	USINT			•	
3	0	SendCommandParam	USINT			•	
12	4	SendData	DINT			•	
1	1	ReadStatus	USINT	•			
3	0	ReadIndex	USINT	•			
12	4	ReadData	DINT	•			
Communication - Display register							
20	-	ABRposition	DINT		•		
28	-	TargetABRposition	DINT		•		
36	-	ErrorInfo	UDINT		•		
47	-	Status of the digital inputs	USINT		•		
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
55	-	Status of encoder supply	USINT		•		
		PowerSupply01	Bit 0				

1) The offset specifies the position of the register within the CAN object.

4.16.2.10.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.16.2.10.4 General

This is a low-end positioning module that supports 2 speed movements in positive and negative directions. No active position check is performed. The movements are started using a command interface and stopped by the position comparator (target position) or user-defined trigger conditions (input edge/ comparison). Every movement step is time-monitored. Up to 8 movement steps can be linked to form one continuous movement.

Position, input states and timeout periods are checked during each system cycle.

4.16.2.10.4.1 Types of movement

The module supports the following types of movement:

- Negative direction - fast
- Negative direction - slow
- Stop
- Positive direction - slow
- Positive direction - fast

The initial state of each type of movement is defined by the user. In order to avoid false input levels on the motor (caused by signal runtimes), and ensure timing (e.g. during direction change), there are additional command parameters to describe a operating mode change:

- 0x93 Negative directional setup state
- 0x88 Negative directional setup time
- 0x8A Negative directional stop time
- 0x95 Positive direction setup state
- 0x89 Positive direction setup time
- 0x8B Positive direction stop time
- 0x94 Stop state

Information:

No directional stop state is defined. To allow error handling, the directional stop state must be the same as STOP. Speed changes in the same direction of movement are not evaluated as changes in the operating mode of the movement.

4.16.2.10.4.2 Movement blocks

The module supports 4 movement blocks: Each movement block contains up to 8 movement steps. Each step is comprised of the following parameters:

- Target position - relative or absolute
- Timeout or delay
- Trigger condition - edge or comparator value (signal level)

A block's movement steps can be executed as one continuous movement. The following parameters must be configured before the movement start command is issued:

- Step activation
- Step target position interpolation - relative or absolute
- Step speed - slow or fast
- Trigger mode - off or "Comparator value = true" or "Comparator value = false"

4.16.2.10.4.3 Movement generator

When a movement start command is issued, the mode of the active movement step is calculated based on the preceding target position. Step parameters may also be changed after the start as long as the step direction is not changed. Otherwise a movement error occurs. To ensure correct directional interpretation, the movement step position/range is limited to ±1073741824.

The target position of a step configured with a trigger is evaluated as the end position (error position). This means the position at the time of the trigger condition becomes the effective target position. Because this position is unknown when the calculation is made by the movement generator, the set end position is used for calculating the next absolute movement step. As a result, it is recommended to proceed with a relative movement step following a triggered step. A successive absolute movement step must be outside the positioning range of the triggered step.

If a movement step is configured as a standstill, i.e. relative position = 0, or the new absolute position = previous target position, a delay has occurred. If no trigger is configured, the parameter step timeout is evaluated as a simple delay time and not as an error state.

4.16.2.10.4.4 Tolerance monitoring

The module constantly monitors the position tolerance, even when no movements are active. Jitter and overshoot tolerances must be configured for both directions. Depending on the previous movement direction, a tolerance window is calculated based on the current target position. Because the movement generator uses the last target position, movements within the tolerance window must be avoided to prevent errors from occurring.

4.16.2.10.4.5 Homing

Homing is not implemented in this module as a movement function. The target position of a completed movement can be applied as the home position via command.

4.16.2.10.4.6 Safety monitoring

A safe input status (masks and comparator values) for positive and negative movements must be configured. Software end positions – minimum and maximum positions – can also be configured for both directions.

The module monitors these two positions from the time the parameter 0x93 or 0x95 "Positive directional setup state" is set. Monitoring is ended when the parameter 0x94 "Stop state" is set.

Because a trigger condition aborts the movement step before a safety check, a hardware limit switch can also be used as a trigger condition without generating an error.

4.16.2.10.5 Command description

4.16.2.10.5.1 No action

This command can be used as a placeholder during development or to separate 2 identical commands.

Code	0x00
Parameter	0
Data 0 to 3	0

4.16.2.10.5.2 Configure display mode

This command can be used to configure how the values in the 4.16.2.10.6.6 "Read parameter number" and 4.16.2.10.6.7 "Read parameter data" registers are displayed. Up to 4 display values can be displayed simultaneously. Possible selections include the command parameters 0xC0 = current position, to 0xC3 = I/O states.

Code	0x01
Parameter	Display control: 0 Scheduler off; Data 0 used for display 1 Scheduler cycle = X2X cycle; The next display cycle starts with each X2X cycle 2 Scheduler cycle = Command cycle; The next display cycle starts with each completed command
Data 0	Parameter number of display cycle 1 (Default: 0xC0 = current position)
...	...
Data 3	Parameter number of display cycle 4 (Default: 0xC0 = current position)

4.16.2.10.5.3 Enables the interface

This command activates the movement interface. The status of the interface is displayed in the 4.16.2.10.6.5 "Read status" register (bit 5). The interface is disabled following a reset. This is necessary to ensure a consistent parameter field.

Code	0x02
Parameter	0
Data 0 to 3	0

4.16.2.10.5.4 Configure parameters

Code	0x03
Parameter	See parameter list
Data 0 to 3	Parameter data

Parameter list

Parameter	Description	Parameter format
Movement blocks		
Calculating the address: Addr = (BlockN - 1) * 32 + (StepN - 1) * 4 BlockN = 1 to 4 StepN = 1 to 8		
Addr	Movement BlockN StepN: Position (relative or absolute)	DINT value
Addr + 1	Movement BlockN StepN: Timeout or delay	Time format
Addr + 2	Movement BlockN StepN: Trigger condition (edge or comparator value)	Trigger condition
Addr + 3	Movement BlockN StepN: Debug information (read only)	0
Configuration		
0x80	Jitter tolerance negative (must be a negative value)	Time format
0x81	Jitter tolerance positive (must be a positive value)	Time format
0x82	Overshoot tolerance negative (must be a negative value)	Time format
0x83	Overshoot tolerance positive (must be a positive value)	Time format
0x84 - 0x87	Reserved	
0x88	Setup time - negative direction	Time format
0x89	Setup time - positive direction	Time format
0x8a	Stop time - negative direction	Time format
0x8b	Stop time - positive direction	Time format
0x8C - 0x8F	Reserved	
0x90	Output configuration (push/pull)	Output configuration
0x91	Output state - negative direction, high speed	Output states
0x92	Output state - negative direction, low speed	Output states
0x93	Output state, negative direction - setup	Output states
0x94	Output state - stop	Output states
0x95	Output state, positive direction - setup	Output states
0x96	Output state - positive direction, low speed	Output states
0x97	Output state - positive direction, high speed	Output states
0x98	Safe input state - negative direction	Safe input states
0x99	Safe input state - positive direction	Safe input states
0x9A - 0x9B	Reserved	
0x9C	Safe minimum position - negative direction	DINT value
0x9D	Safe maximum position - negative direction	DINT value
0x9E	Safe minimum position - positive direction	DINT value
0x9F	Safe maximum position - positive direction	DINT value
0xA0 - 0xBF	Reserved	
Status indicators		
0xC0	Current position	0
0xC1	Target position	0
0xC2	Error information	0; Error information
0xC3	I/O states	0; I/O states
0xC4 - 0xFF	Reserved	

Parameter formats used

DINT value

The possible values depend on the respective command.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Time format

Time in microseconds. System resolution is a result of the system cycle time (default: 50 µs).

Trigger condition

Depending on bits 2 and 3 in the data structure of each movement block, either the "edge" or "comparator value" structure is selected as the trigger condition.

Edge

Bit	Description	Value	Information
0	Falling edge - channel 01	0	Disabled
		1	Enabled
...		...	
7	Falling edge - channel 08	0	Disabled
		1	Enabled
8 - 15	Reserved	0	
16	Rising edge - channel 01	0	Disabled
		1	Enabled
..		...	
23	Rising edge - channel 08	0	Disabled
		1	Enabled
24 - 31	Reserved	0	

Comparator value

Bit	Description	Value	Information
0	Activation mask - channel 01	0	Disabled
		1	Enabled
...		...	
7	Activation mask - channel 08	0	Disabled
		1	Enabled
8 - 15	Reserved	0	
15	Comparative state - channel 01	0 or 1	
...			
23	Comparative state - channel 08	0 or 1	
24 - 31	Reserved	0	

Output configuration

Bit	Description	Value	Information
0 - 1	Reserved	0	
2	Push driver - channel 02	0	Disabled
		1	Enabled
3	Push driver - channel 02	0	Disabled
		1	Enabled
4 - 5	Reserved	0	
6	Push driver - channel 04	0	Disabled
		1	Enabled
7	Pull driver - channel 04	0	Disabled
		1	Enabled
8 - 9	Reserved	0	
10	Push driver - channel 06	0	Disabled
		1	Enabled
11	Pull driver - channel 06	0	Disabled
		1	Enabled
12 - 13	Reserved	0	
14	Push driver - channel 08	0	Disabled
		1	Enabled
15	Pull driver - channel 08	0	Disabled
		1	Enabled
16 - 31	Reserved	0	

Output states

Bit	Description	Value	Information
0	Reserved	0	
1	Channel 02	0	No action
		1	Clear channel
2	Reserved	0	
3	Channel 04	0	No action
		1	Clear channel
4	Reserved	0	
5	Channel 06	0	No action
		1	Clear channel
6	Reserved	0	
7	Channel 08	0	No action
		1	Clear channel
8 - 16	Reserved	0	
17	Channel 02	0	No action
		1	Set channel
18	Reserved	0	
19	Channel 04	0	No action
		1	Set channel
20	Reserved	0	
21	Channel 06	0	No action
		1	Set channel
22	Reserved	0	
23	Channel 08	0	No action
		1	Set channel
24 - 31	Reserved	0	

Safe input states

Bit	Description	Value	Information
0	Activation mask - channel 01	0	Disabled
		1	Enabled
...		...	
7	Activation mask - channel 08	0	Disabled
		1	Enabled
8 - 15	Reserved	0	
15	Comparative state - channel 01	0 or 1	
...			
23	Comparative state - channel 08	0 or 1	
24 - 31	Reserved	0	

Error information

This table shows the read display value. The parameter for the display command is 0.

Bit	Description	Value	Information
0	Tolerance error - negative	0	No error
		1	Error occurred
1	Tolerance error - positive	0	No error
		1	Error occurred
2	Timeout	0	No timeout
		1	Timeout
3 - 7	Reserved	0	
8	Safety monitoring error Inputs (hardwire limit switch)	0	No error
		1	Error occurred
9	Safety monitoring error Position (software end position)	0	No error
		1	Error occurred
10 - 15	Reserved	0	
16 - 18	Error status information	000	Reserved
		001	Negative directional stop state
		010	Negative movement
		011	Negative directional setup state
		100	Stop state
		101	Positive directional setup state
		110	Positive movement
		111	Positive directional stop state
19	Reserved	0	
20 - 24	Invalid step number	000 to 111	Number of the step that does not contain any movement information.
		1000	Inactive movement step (tolerance check)
25 - 31	Reserved	0	

I/O states

This table shows the read display value. The parameter for the display command is 0.

Bit	Description	Value	Information
0	Input state - channel 01	0 or 1	
...		...	
7	Input state - channel 08	0 or 1	
8 - 16	Reserved	0	
17	Output state - channel 02	0 or 1	
18	Reserved	0	
19	Output state - channel 04	0 or 1	
20	Reserved	0	
21	Output state - channel 06	0 or 1	
22	Reserved	0	
23	Output state - channel 08	0 or 1	
24 - 31	Reserved	0	

4.16.2.10.5.5 Configure counters

This command can be used to assign the hardware channels to the AB counter. With an ABR counter, the R input can be connected to any hardware channel as the trigger signal.

Code	0x04
Parameter	See parameter structure
Data 0	See data structure
Data 1 to 3	0

Parameter structure:

Bit	Description	Value	Information
0 - 1	Counter connection pair	00	Pair 1 (A: channel 01, B: channel 02)
		01	Pair 2 (A: channel 03, B: channel 04)
		10	Pair 3 (A: channel 05, B: channel 06)
		11	Pair 4 (A: channel 07, B: channel 08)
2 - 7	Reserved	0	

Data structure:

Bit	Description	Value	Information
0 - 1	Counter mode	00	AB encoder
		01	Up/down counter (A: timing, B: up/down signal)
		10	Edge counter - channel A
		11	Edge counter - channel B
2	Counting direction	0	Positive
		1	Negative
3 - 7	Reserved	0	

4.16.2.10.5.6 Homing

Assumes the target position of the last successful movement step as a reference position.

Code	0x05
Parameter	0
Data 0 to 3	Home position

4.16.2.10.5.7 Stops the movement.

The movement step in progress is stopped. This command always results in a movement error.

Code	0x06
Parameter	0
Data 0 to 3	0

4.16.2.10.5.8 Acknowledge movement error

The movement error is is cleared. If this command is executed when the error is still present, the current position is assumed as the target position. The basis of the relative position becomes unclear.

Code	0x07
Parameter	0
Data 0 to 3	0

4.16.2.10.5.9 Start a movement block

This command starts a movement block consisting of up to 8 steps.

Code	0x08 (Block 1) 0x09 (Block 2) 0x0A (Block 3) 0x0B (Block 4)
Parameter	See parameter structure
Data 0 to 3	See data structure

Parameter structure:

Bit	Description	Value	Information
0	Step 1	0	No movement.
		1	Perform movement step.
...		...	
7	Step 8	0	No movement.
		1	Perform movement step.

Data structure:

Bit	Description	Value	Information
0	Step 1 position setting:	0	Relative
		1	Absolute
1	Step 1 speed:	0	Slow
		1	Fast
2 - 3	Step 1 trigger mode:	00	No trigger
		01	Edge trigger
		10	Comparator value "true"
		11	Comparator value "false"
4 - 7	Step 2	x	Like step 1 / Bits 0 to 2
...			
28 - 31	Step 8	x	Like step 1 / Bits 0 to 2

4.16.2.10.5.10 Selecting the debug information

At the end of each movement step, the command parameter "Addr + 3" (see 4.16.2.10.5.4 "Movement blocks - Calculating the address" can be used to read the debug information selected in this register. This debug information is shown in the 4.16.2.10.6.6 "Read parameter number" and 4.16.2.10.6.7 "Read parameter data" registers.

Code	0x00
Parameter	0 Error information (default) 1 Timestamp 2 Current position 3 Target position
Data 0 to 3	0

4.16.2.10.6 Command interface

A command interface is available to the user. A command consists of:

- 4.16.2.10.6.2 "Command" (in the command description: code)
- 4.16.2.10.6.3 "Command parameter" (in the command description: parameters)
- 4.16.2.10.6.4 "Command data" (in the command description: Data 0 to 3)

The following commands can be executed:

- 4.16.2.10.5.1 "No action"
- 4.16.2.10.5.2 "Configure display mode"
- 4.16.2.10.5.3 "Enable the interface"
- 4.16.2.10.5.4 "Configure parameters"
- 4.16.2.10.5.5 "Configure counters"
- 4.16.2.10.5.6 "Perform homing"
- 4.16.2.10.5.7 "Stop the movement"
- 4.16.2.10.5.8 "Acknowledge movement error"
- 4.16.2.10.5.9 "Start a movement block"
- 4.16.2.10.5.10 "Select debug information"

The module returns:

- 4.16.2.10.6.5 "System status"
- 4.16.2.10.6.6 "Displays parameter number"
- 4.16.2.10.6.7 "Displays data content"

The module detects a new command through a change in the command register. The toggle bit must be changed in order to detect when the command issued in the 4.16.2.10.6.5 "System status" register is applied. Identical commands can be executed immediately following one another simply by changing the toggle bit.

4.16.2.10.6.1 Execution of a command

Commands must be sent by the application using the command interface. Due to the simple structure of the command interface, it is also possible to send them via CAN.

All commands are executed as follows:

1 Write command parameters and command data to the respective register.
2 Write command with changed toggle bit.
When bit 7 in the command register is toggled, the module executes the comand with the command parameters and command data.
3 Wait until bit 7 in the response register (System Status) matches bit 7 in the command register.
4 Read additional status information from the response register if necessary.
5 If additional commands should be sent, proceed with step 1.

4.16.2.10.6.2 Send command

Name:
SendCommand

The commands described under 4.16.2.10.5 "Command description" can be sent from this register. Bit 7 must be toggled to apply the commands.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 6	Command code	x	
7	Toggle bit for applying a new command	x	

4.16.2.10.6.3 Send command parameters

Name:
SendCommandParam

Specific parameters for the command to be sent must be entered in this register. The required parameters are listed under 4.16.2.10.5 "Command description" for the respective commands.

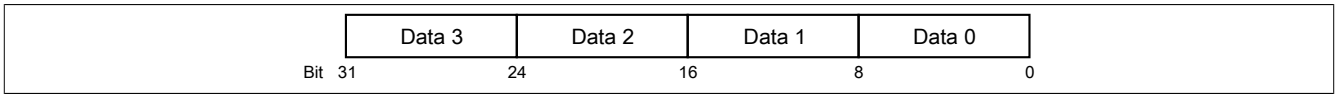
Data type	Value	Information
USINT	x	Command parameter

4.16.2.10.6.4 Send command data

Name:
SendData

Specific parameters for the command to be sent must be entered in this register. The required data is listed under 4.16.2.10.5 "Command description" for the respective commands.

Data 0 to 3 are sent as a single DINT value. The following structure is used:



Data type	Value	Information
DINT	x	Command data 0 to 3

4.16.2.10.6.5 Read status

Name:
ReadStatus

The commands and the current status can be checked in this register. Bit 7 can be used to check whether an issued command has been applied.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	0	
2	Position	0	Not yet reached
		1	Reached
3	Motion	0	In motion
		1	completed
4	Numerator	0	Not yet configured
		1	Configured
5	Interface	0	Not enabled
		1	Enabled
6	Command	0	No error
		1	Error occurred
7	Command toggle bit	x	Value that was read

4.16.2.10.6.6 Read parameter number

Name:
ReadIndex

The parameter number returned for a display command is shown in this register. See 4.16.2.10.5.2 "Configure display mode" and 4.16.2.10.5.10 "Selecting the debug information"

Data type	Value	Information
USINT	x	Parameter numbers

4.16.2.10.6.7 Read parameter data

Name:
ReadData

The parameter data returned for a display command is shown in this register. See 4.16.2.10.5.2 "Configure display mode" and 4.16.2.10.5.10 "Selecting the debug information"

Data type	Value	Information
DINT	x	Parameter data

4.16.2.10.6.8 Special display parameters

The following 4 registers correspond to display parameters 0xC0 to 0xC3 in the command description 4.16.2.10.5.4 "Configure parameters". This frees up the 4.16.2.10.6.7 "ReadData" register for other data.

Indicates the current position.

Name:
ABRPosition

This register shows the current position in the current step. It corresponds with the parameter 0xC0 in section 4.16.2.10.5.4 "Configure parameters".

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Indicates the current target position

Name:
TargetABRposition

This register shows the target position of the current step. It corresponds with the parameter 0xC1 in section 4.16.2.10.5.4 "Configure parameters".

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Displays the error information

Name:
ErrorInfo

The error information is shown in this register. It corresponds with the parameter 0xC2 in section 4.16.2.10.5.4 "Configure parameters".

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Tolerance error - negative	0	No error
		1	Error occurred
1	Tolerance error - positive	0	No error
		1	Error occurred
2	Timeout	0	No timeout
		1	Timeout
3 - 7	Reserved	0	
8	Safety monitoring error Inputs (hardwire limit switch)	0	No error
		1	Error occurred
9	Safety monitoring error Position (software end position)	0	No error
		1	Error occurred
10 - 15	Reserved	0	
16 - 18	Error status information	000	Reserved
		001	Negative directional stop state
		010	Negative movement
		011	Negative directional setup state
		100	Stop state
		101	Positive directional setup state
		110	Positive movement
		111	Positive directional stop state
19	Reserved	0	
20 - 24	Invalid step number	000 to 111	Number of the step that does not contain any movement information.
		1000	Inactive movement step (tolerance check)
25 - 31	Reserved	0	

Status of the digital inputs

Name:
DigitalInput01 to DigitalInput08

The status of the digital inputs or read outputs are shown in this register. It corresponds with the parameter 0xC3 in section 4.16.2.10.5.4 "Configure parameters".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalInput01	0 or 1	Input status - channel 1
...		...	
7	DigitalInput08	0 or 1	Input status - channel 8

4.16.2.10.7 Sample configurations

4.16.2.10.7.1 Movement example

The channels have been set as follows for this example:

Hardware channel	Direction	Function assignment
1	Input	ABR encoder - signal A
2	Input	ABR encoder - signal B
3	Input	ABR encoder - signal R
4	Output	Fast speed
5	Input	Negative limit switch
6	Output	Negative direction
7	Input	Positive limit switch
8	Output	Positive direction

Enable interface

	Value	Description
Code	0x02	
Parameter	0	
Data 0 to 3	0	

Configure parameters

	Value
Code	0x03
Parameter	Parameter numbers
Data 0 to 3	Parameter data

The following parameters must be configured:

Parameter	Data	Description
0x80	APPL	Negative jitter tolerance [µs] (application-specific)
0x81	APPL	Positive jitter tolerance [µs] (application-specific)
0x82	APPL	Negative overshoot tolerance [µs] (application-specific)
0x83	APPL	Positive overshoot tolerance [µs] (application-specific)
0x88	APPL	Negative setup time [µs] (application-specific)
0x89	APPL	Positive setup time [µs] (application-specific)
0x8A	APPL	Negative stop time [µs] (application-specific)
0x8B	APPL	Positive stop time [µs] (application-specific)
0x90	0x0000CCC0	Output configuration: Channel 04, channel 06, channel 08 as push/pull outputs
0x91	0x00280080	Output states - fast negative movement: Set channels 04 and 06, clear channel 08
0x92	0x00200088	Output states - slow negative movement: Set channel 06, clear channels 04 and 08
0x93	0x000000A8	Output states - negative setup: Clear channels 04, 06 and 08
0x94	0x000000A8	Output states - stop: Clear channels 04, 06 and 08
0x95	0x000000A8	Output states - positive setup: Clear channels 04, 06 and 08
0x96	0x00800028	Output states - slow positive movement: Set channel 08, clear channels 04 and 06
0x97	0x00880020	Output states - fast positive movement: Set channels 04 and 08, clear channel 06
0x98	0x00100010	Safe input state - negative: Channel 05 active, status of channel 05 (level) = 1
0x99	0x00400040	Safe input state - positive: Channel 07 active, status of channel 05 (level) = 1 Code 0x04

Configure counters

	Value	Description
Code	0x04	
Parameter	0x00	Counter pair 1
Data 0	0	AB encoder, positive direction
Data 1 to 3	0	

4.16.2.10.7.2 Homing example

Configure parameters

	Value
Code	0x03
Parameter	Parameter numbers
Data 0 to 3	Parameter data

The following parameters must be configured:

Parameter	Data	Description
0x00	0x3FFFFFFF	Relative positive position maximum
0x02	0x00000040	Trigger on input state of channel 07 = 0
0x04	0xC0000001	Relative negative position maximum
0x06	0x00400040	Trigger on input state of channel 07 == 1
0x08	0xC0000001	Relative negative position maximum
0x0A	0x00000004	Trigger on falling edge of channel 03

Start movement

	Value	Description
Code	0x08	Block 1
Parameter	0x07	Activate steps 1 to 3
Data 0 to 3	0x00000**411**	Step 1: absolute, slow, trigger off Step 2: absolute, slow, trigger off Step 3: relative, slow, trigger on edge

Wait until the movement is complete.

Homing

	Value	Description
Code	0x05	
Parameter	0	
Data 0 to 3	x	Home position

4.16.2.10.7.3 Standard positioning example

Configure parameters

	Value
Code	0x03
Parameter	Parameter numbers
Data 0 to 3	Parameter data

The following parameters must be configured:

Parameter	Data	Description
0x00	X1	Pre-stop position
0x04	X2	Stop position

Start movement

	Value	Description
Code	0x08	Block 1
Parameter	0x03	Activate steps 1 and 2
Data 0 to 3	0x0000000**11**	Step 1: absolute, slow, trigger off Step 2: absolute, slow, trigger off

4.16.2.10.7.4 Standard positioning example with stop

Configure parameters

	Value
Code	0x03
Parameter	Parameter numbers
Data 0 to 3	Parameter data

The following parameters must be configured:

Parameter	Data	Description
0x00	X1	Pre-stop position
0x04	X2	Stop position
0x08	0	Relative movement
0x09	T_STOP	Stop delay [µs]

Start movement

	Value	Description
Code	0x08	Block 1
Parameter	0x07	Activate steps 1 to 3
Data 0 to 3	0x00000**011**	Step 1: absolute, slow, trigger off Step 2: absolute, slow, trigger off Step 3: relative, trigger off

4.16.2.10.8 General module register

4.16.2.10.8.1 Configures the system cycle time

Name:
CycleTimeCff

This register configures the module's system cycle time.

Data type	Value	Information
UINT	25 to 255	System cycle time in µs (default = 50 µs)

4.16.2.10.8.2 Status of encoder supply

Name:
PowerSupply01

This register shows the status of the integrated encoder supply. A faulty encoder power supply is displayed as a warning.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

4.16.2.10.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
100 µs

4.16.2.10.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.16.3 X20DC1073

4.16.3.1 General information

The module is equipped with a SinCos encoder interface. The input signals are monitored. This makes it possible to detect open or shorted lines as well as encoder supply failures.

- SinCos encoder interface
- Encoder input monitoring
- 5 VDC and GND for encoder supply
- NetTime function: Timestamp for position

SinCos encoders

SinCos encoders with 1 V_{ss} are mostly used in linear drives and systems with high-resolution optical or magnetic position measurement systems. The module can process input signals with a frequency of up to 400 kHz.

NetTime position timestamp

Highly dynamic positioning tasks require not only the position value, but also the exact time at which the position was determined. The module has a NetTime function for this, which adds a timestamp to the recorded position with microsecond accuracy.

The module provides the PLC with the position value and timestamp as absolute time value. The NetTime mechanisms ensure that the PLC NetTime clock and the local NetTime clock on the module have exactly the same absolute time at all times.

4.16.3.2 Order data

Model number	Short description	Figure
	Digital signal processing and preparation	
X20DC1073	X20 digital counter module, 1x SinCos, 1 Vss, 400 kHz input frequency, encoder monitoring, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 355: X20DC1073 - Order data

4.16.3.3 Technical data

Product ID	X20DC1073
Short description	
I/O module	1x SinCos input
General information	
B&R ID code	0xAEC6
Status indicators	Counting direction, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Counting direction	Yes, using status LED
Power consumption	
Bus	0.01 W
Internal I/O	1.3 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Encoder inputs	
Type	SinCos
Angular position resolution	13-bit, with a 1 V_{SS} signal
Encoder monitoring	Yes
Max. encoder cable length	Max. 20 m, see "Calculation of the maximum encoder cable length"
Sine/Cosine inputs	
Signal transmission	Differential signals, symmetrical
Signal frequency	DC up to 400 kHz
Differential voltage	1 V_{SS}
Common-mode voltage	Max. ±10 V
Terminating resistor	120 Ω
Encoder supply	
Output voltage	5 V
Min. output voltage at 300 mA	4.86 V
Load capability	300 mA
Protective measures	
Overload protection	Yes
Short circuit protection	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 356: X20DC1073 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.16.3.4 LED status indicators

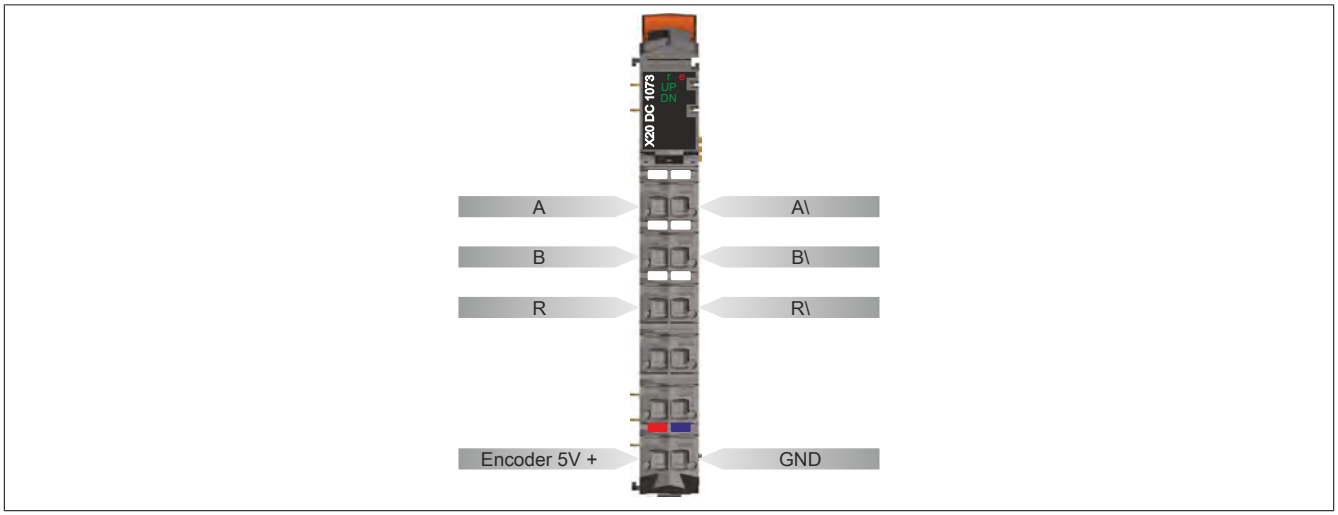
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset state. Possible cause: • Encoder supply error
			Single flash	I/O error. Possible cause: • Sine/Cosine relative position error (open line)
			Single flash, inverted	Error or reset state and I/O error
	UP	Green	On	The "UP/DN" LEDs are lit depending on the rotational direction and the speed of the connected encoder. The "UP" LED indicates when the encoder position changes in the positive direction.
	DN	Green	On	The "DN" LED indicates when the encoder position changes in the negative direction.

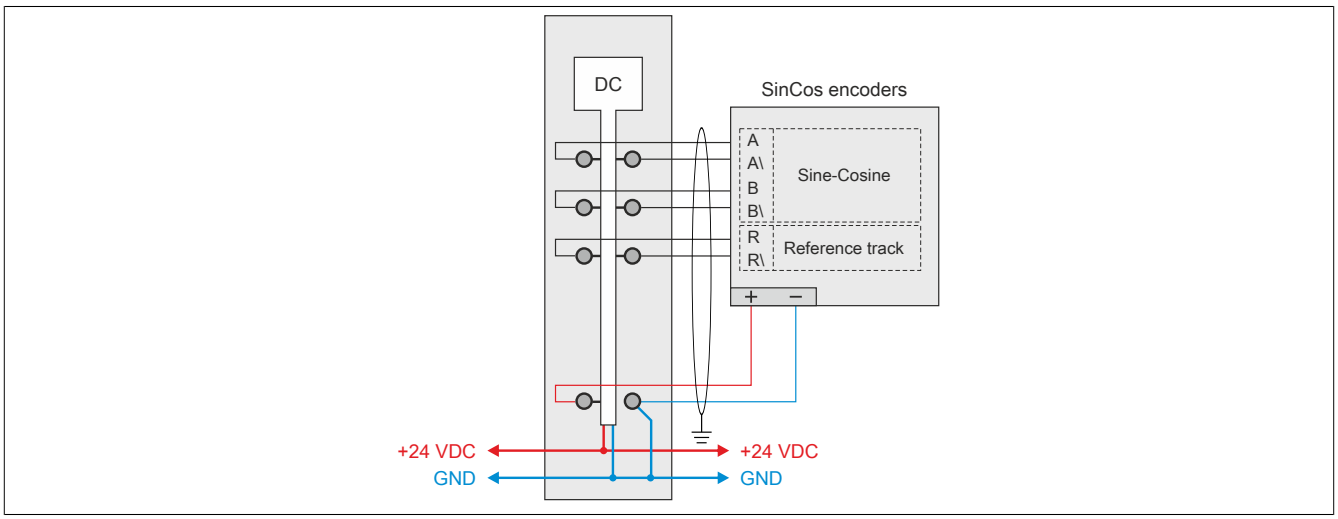
1) Depending on the configuration, a firmware update can take up to several minutes.

4.16.3.5 Pinout

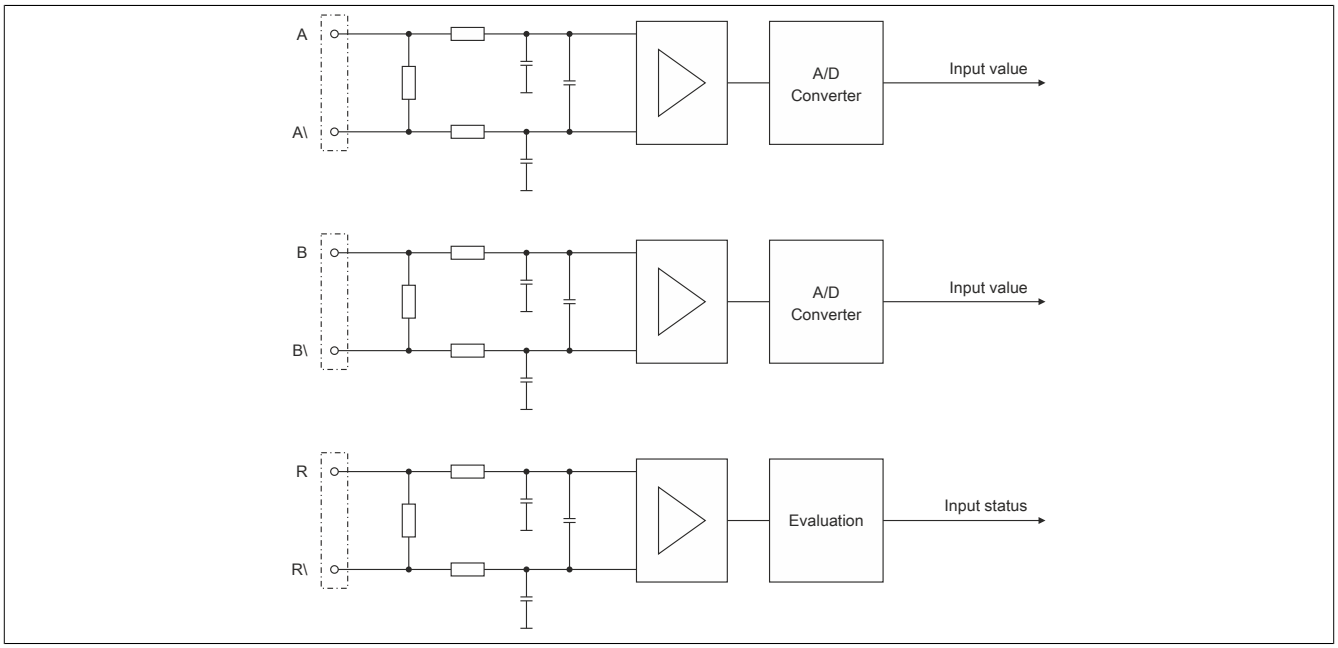
Shielded cables must be used for all signal lines.



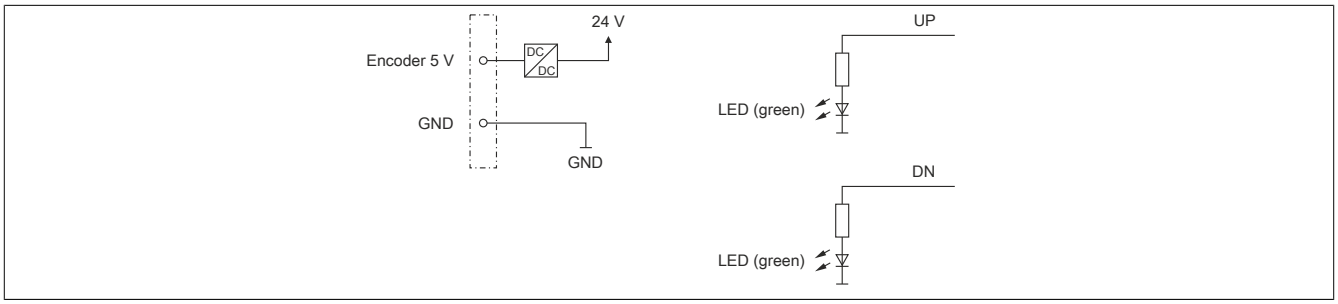
4.16.3.6 Connection example



4.16.3.7 Analog inputs - Input circuit diagram



4.16.3.8 Circuit diagram for the encoder supply and LEDs



4.16.3.9 Calculating the maximum encoder cable length

The following encoder data is assumed for this sample calculation:

Encoder data	
Input voltage	4.75 V – 5.25 V
Max. input current	0.12 A
Module encoder output	
Min. output voltage at 300 mA	4.86 V

Calculation of the maximum voltage drop for the cable

The maximum permitted voltage drop is calculated using the minimum encoder output voltage for the module ($U_{ModuleMin}$) and the minimum encoder input voltage ($U_{EncoderMin}$) of the encoder being used.

$$U_{CableMax} = (U_{ModuleMin} - U_{EncoderMin}) / 2$$

Example: $U_{CableMax} = (4.86\ V - 4.75\ V) / 2 = 0.055\ V$

Calculation of the maximum cable length

$$\text{Cable length}_{Max} = U_{CableMax} * \text{Wire cross section } (mm^2) / (0.01786 * I_{Encoder})$$

This means:

$I_{Encoder}$ Current consumption of encoder in amps

$U_{CableMax}$ Maximum permitted voltage drop in volts

Example with resolver cable "8BCR0xxxx.1111A-0"

Encoder with 120 mA max. current consumption

Resolver cable cross section = 0.25 mm^2

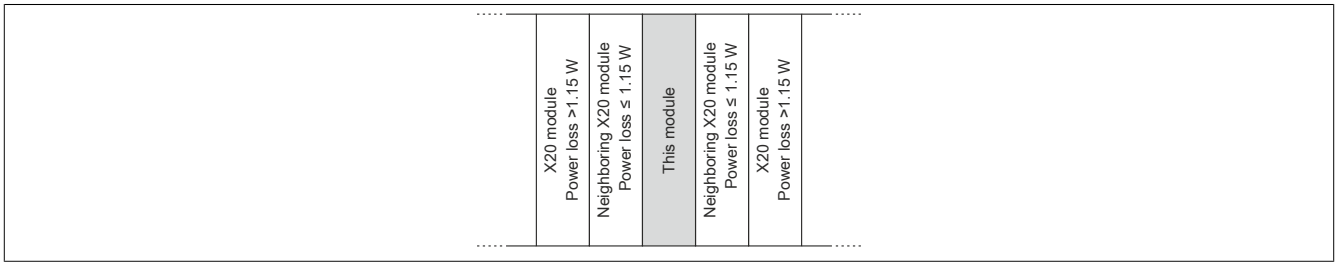
Results in a total cable length of:

$$\text{Cable length}_{Max} = 0.055\ V * 0.25\ mm^2 / 0.01786 * 0.12\ A) = 6.41\ m$$

4.16.3.10 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.16.3.11 Register description

4.16.3.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.16.3.11.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module configuration						
513	CfO_SIframeGenID	USINT				•
Basic functions						
683	SDCLifeCount	SINT	•			
1172	PositionHW	UDINT	•			
1180	PositionLW	UDINT	•			
	Position	DINT				
1164	PosTime	DINT	•			
1166	PosTime	INT	•			
1155	PosCycle	SINT	•			
Error management						
389	ErrorEnableID_1710	USINT				•
261	ErrorStateID_1710	USINT	•			
	EncoderSupplyError	Bit 0				
	VssCheckError	Bit 2				
325	ErrorQuitID_1710	USINT			•	
	AckEncoderSupplyError	Bit 0				
	AckVssCheckError	Bit 2				
Sin/Cos - Analog interface configuration						
1025	SinCosEnable	USINT				•
1027	SinCosRefSource	USINT				•
1034	SinCosVssMin	UINT				•
1038	SinCosVssMax	UINT				•
1044	SinCosQuitTime	UDINT				•
Additional encoder position						
1029	SinCosCompMode	USINT				•
1204	ReferenceHW	UDINT	•			
1212	ReferenceLW	UDINT	•			
	Reference	DINT				
1187	RefCycle	SINT	•			

4.16.3.11.3 Function model 254 - Bus controller

Register	Object[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Module configuration							
513	-	CfO_SIframeGenID	USINT				•
Basic functions							
1180	0	Position	DINT	•			
1155	4	PosCycle	SINT	•			
Error management							
389	-	ErrorEnableID_1710	USINT				•
325	15	ErrorStateID_1710	USINT	•			
		EncoderSupplyError	Bit 0				
		VssCheckError	Bit 2				
261	6	ErrorQuitID_1710	USINT			•	
		AckEncoderSupplyError	Bit 0				
		AckVssCheckError	Bit 2				
Sin/Cos - Analog interface configuration							
1025	-	SinCosEnable	USINT				•
1027	-	SinCosRefSource	USINT				•
1034	-	SinCosVssMin	UINT				•
1038	-	SinCosVssMax	UINT				•
1044	-	SinCosQuitTime	UDINT				•
Additional encoder position							
1029	-	SinCosCompMode	USINT				•
1212	8	Reference	DINT	•			
1187	12	RefCycle	SINT	•			

1) The offset specifies the position of the register within the CAN object.

4.16.3.11.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.16.3.11.4 Module configuration

The following configuration register can be used to configure different module settings. They can be used, for example, to modify the module's behavior on an X2X Link network. One configuration register is available for the user.

4.16.3.11.4.1 Data query

Name:
CfO_SIframeGenID

This register can be used to define when the synchronous/cyclic input data is generated. "X2X cycle optimized" should be set for jitter-free data acquisition. "Fast reaction" can be set for the best performance.

Data type	Value	Information
USINT	9	Fast reaction
	14	X2X cycle optimized (bus controller default setting)

4.16.3.11.5 Basic functions

This module can import the position of a motor shaft when used together with a sin/cos encoder. The received position data is prepared in 2 different formats and given a time stamp. 5 registers are available for further processing. This allows the user to select the format that best fits the application at hand.

4.16.3.11.5.1 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.16.3.11.5.2 Absolute position values

Name:
PositionHW
PositionLW

The absolute position of the encoder is defined using 64-bit resolution. The position value is stored in the PositionHW and PositionLW registers. The upper 32 bits are stored the PositionHW register, while the lower 32 bits are stored in the PositionLW register.

For SinCos signal evaluation, see 4.16.3.11.7.1 "Format of the SinCos signal" for information regarding the data format.

Data type	Value
2x UDINT	0 to 4,294,967,295

4.16.3.11.5.3 SDC position value

Name:
Position

The SDC library requires a signed 32-bit position value. The position's low word can be accessed separately for this. The value can also be used as default position value, however.

For SinCos signal evaluation, see 4.16.3.11.7.1 "Format of the SinCos signal" for information regarding the data format.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.16.3.11.5.4 NetTime of the position values

Name:
PosTime

This register is used to assign each recorded position of the current NetTime value. The NetTime is recorded with µs accuracy.
The SDC library requires a 16 bit value. The NetTime value is therefore also generated in this format.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	NetTime in µs
INT	-32,768 to 32,767	

4.16.3.11.5.5 Counter for position values

Name:
PosCycle

PosCycle is an integer counter that is incremented as soon as the module has saved a new valid position value.

Data type	Value
SINT	-128 to 127

4.16.3.11.6 Error management

Module-based diagnostics

This module can detect errors on its own and differentiates between 2 different types of error.

- **Encoder supply:**
  The encoder voltage supply is below the permitted limit.
- **V_{ss} Sin/Cos:**
  The voltage value for the Sin/Cos track violates the configured limit values.
  → See register 4.16.3.11.7.4 "SinCosVssMin" or 4.16.3.11.7.5 "SinCosVssMax"

4.16.3.11.6.1 Enabling/disabling error messages

Name:
ErrorEnableID_1710
The individual diagnostics can be separately enabled or disabled in this register.

Data type	Value
USINT	See bit structure.

Bit structure

Bit	Name	Value	Information
0	Error detection - Encoder supply	0	Disabled
		1	Enabled (bus controller default setting)
1	Reserved	-	
2	Error detection - V_{ss} Sin/Cos	0	Disabled
		1	Enabled (bus controller default setting)
3 - 7	Reserved	-	

4.16.3.11.6.2 Show error messages

Name:
ErrorStateID_1710

EncoderSupplyError
VssCheckError

This register indicates which error or warning is currently active. For the meaning of individual error messages, see 4.16.3.11.6 "Error management".

Data type	Value
USINT	See bit structure.

Bit structure

Bit	Name	Value	Information
0	EncoderSupplyError	0	No error
		1	Encoder supply error
1	Reserved	-	
2	VssCheckError	0	No error
		1	V_{ss} error on the Sin/Cos track
3 - 7	Reserved	-	

4.16.3.11.6.3 Acknowledge error messages

Name:
ErrorQuitID_1710

AckEncoderSupplyError
AckVssCheckError

This register is used to acknowledge an error message that occurred in the 4.16.3.11.6.2 "Show error messages" register. For the meaning of individual error messages, see 4.16.3.11.6 "Error management".

Data type	Value
USINT	See bit structure.

Bit structure

Bit	Name	Value	Information
0	AckEncoderSupplyError	0	No error acknowledgment
		1	Error acknowledgment
1	Reserved	-	
2	AckVssCheckError	0	No error acknowledgment
		1	Error acknowledgment
3 - 7	Reserved	-	

4.16.3.11.7 Sin/Cos - Analog interface configuration

The module is equipped with an analog interface for detecting a differential sine-, cosine- and reference signal.

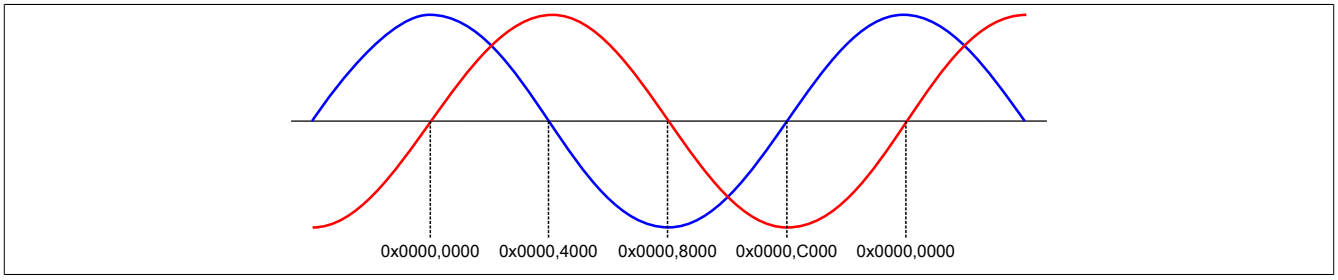
4.16.3.11.7.1 Format of the SinCos signal

The SinCos signal is represented as a position value in the 4.16.3.11.5.2 "Absolute position values" and 4.16.3.11.5.3 "SDC position value" registers. The following relationships apply:

- PositionLW and Position are identical in the function.
- PositionHW extends the integer range of PositionLW by adding multi-turn functionality.

<table>
<tr><td>64-bit register</td><td>PositionHW
(unsigned)</td><td colspan="2">PositionLW
(unsigned)</td></tr>
<tr><td>32-bit register</td><td>-</td><td colspan="2">Position (signed)</td></tr>
<tr><td>Format</td><td>Integer extension
(to 48-bit)</td><td>Integer
(16-bit)</td><td>Decimal places:
(with 13-bit resolution)</td></tr>
<tr><td>Information</td><td></td><td>A full sine wave corresponds to an increment of the integer.</td><td>
<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>0</td><td>0</td></tr>
</table>
Important: The lower 3 bits always contain the value 0.
</td></tr>
<tr><td>Word/DWord</td><td>DWord</td><td>Word 1</td><td>Word 0</td></tr>
</table>

Relationship between sine curve (red) and decimal places:



4.16.3.11.7.2 Enabling SinCos

Name:
SinCosEnable

This register must always have the value 1 for configuration reasons.

Data type	Value	Information
USINT	1	Bus controller default: 1

4.16.3.11.7.3 Enabling SinCos reference source

Name:
SinCosRefSource

This register must always have the value 0 for configuration reasons.

Data type	Value	Information
USINT	0	Bus controller default: 0

4.16.3.11.7.4 Configuring the lower Vss value

Name:
SinCosVssMin

This register specifies the lower limit value for the peak-to-peak voltage of the sine/cosine track. The incoming signal is monitored in this way. If the incoming value falls below this specified limit, then the module reports the corresponding error.

Data type	Value	Information
UINT	0 to 1500	Values in mV, bus controller default setting: 800

4.16.3.11.7.5 Configuring the upper Vss value

Name:
SinCosVssMax

This register specifies the upper limit value for the peak-to-peak voltage of the sine/cosine track. The incoming signal is monitored in this way. If the incoming value exceeds this specified limit, then the module reports the corresponding error.

Data type	Value	Information
UINT	0 to 1500	Values in mV, bus controller default setting: 1200

4.16.3.11.7.6 Configuring the delay time after errors

Name:
SinCosQuitTime

If an error is detected on the analog interface, the last correctly read values remain valid. An interval can be defined in this register at which the module begins receiving correct values again after the error state without processing them further internally. Only then will newly sampled correct analog values be recognized as valid.

Data type	Value	Information
UDINT	0 to 20000000	Values in µs, bus controller default setting: 100000

4.16.3.11.8 Additional encoder position

In addition to the basic function, importing position values, the module can also copy an imported position to the reference register. The copy procedure is triggered by a configurable event.

4.16.3.11.8.1 Configuration

The position of the axis being measured is determined by 3 signals. The Z-signal is triggered exactly once during a single full rotation of the axis, which defines the reference point. The sine and cosine values are offset by 90° and undergo twofold evaluation by the module hardware. During "rough interpolation" the analog sine and cosine values are handled like digital signals. This works in the same way as a conventional ABR module. Fine interpolation takes place simultaneously in another part of the module. This is done using module-specific algorithms.

4.16.3.11.8.2 Configuring the copy procedure

Name:
SinCosCompMode

This register is used to determine when the current position should be copied to the reference register. The register is divided into 2 halves. The upper 4 bits determine which of the signal tracks are relevant for the trigger. The lower 4 bits determine which roughly interpolated states the individual signal tracks must demonstrate in order for the copying procedure to take place.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Latch - Sine track	0	Copy when sine is negative
		1	Copy when sine is positive (bus controller default setting)
1	Latch - Cosine track	0	Copy when cosine is negative
		1	Copy when cosine is positive (bus controller default setting)
2	Latch - Reference track (Z-track)	0	Copy when reference is negative
		1	Copy when reference is positive (bus controller default setting)
3	Reserved	-	
4	Sine track	0	Irrelevant for latch
		1	Relevant for latch (bus controller default setting)
5	Cosine track	0	Irrelevant for latch
		1	Relevant for latch (bus controller default setting)
6	Reference track (Z-track)	0	Irrelevant for latch
		1	Relevant for latch (bus controller default setting)
7	Reserved	-	

Call

The reference registers can be called the same way as the registers for the current position.

4.16.3.11.8.3 Reference position (to 64-bit)

Name:
ReferenceHW
ReferenceLW

This register prepares the value of the encoder position at the time a specific event occurred.

The 64-bit position value is placed in the registers ReferenceHW and ReferenceLW. The upper 32 bits are in the ReferenceHW register and the lower 32 bits in the ReferenceLW register.

Data type	Value
UDINT	0 to 4,294,967,295

4.16.3.11.8.4 Reference position (to 32-bit)

Name:
Reference
Reference

Just like the position registers, the lower 32 bits of the reference position can also be addressed separately. The result if interpreted as a signed value.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.16.3.11.8.5 Counter for reference values

Name:
RefCycle

This register acts as an integer counter that is incremented as soon as the module has determined a new valid reference value.

Data type	Value
SINT	-128 to 127

4.16.3.11.9 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.16.3.11.10 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
100 µs

4.16.4 X20(c)DS1119

4.16.4.1 General information

The module being used is a multifunctional digital signal processor module. It's flexibility allows it to be implemented for a wide range of tasks involving the creation or processing of digital signals. For example, two main uses include encoder emulation and controlling stepper output stages with pulse and direction signals. When used for encoder emulation, frequency inverters or servo axes with the speed follow function can follow a real or virtual master axis.

A further important feature is the timestamp function, which is integrated in the module. It can be used, for example, to create ramp curves for the counter in the encoder emulation virtually independent of bus cycle times. It's only necessary to enter the target counter value and the time at which it should be reached. The module generates the appropriate counter values, precisely in microsecond resolution and independently of the bus clock.

- 3 digital 5 V channels, configurable as inputs or outputs
- 2 digital 24 V input channels
- 1 universal counter pair (2 event counters, AB counter or up/down counter)
- Linear movement generator (A/B; direction/frequency) with one reference pulse
- SSI absolute encoder

4.16.4.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.16.4.3 Order data

Model number	Short description	Figure
	Digital signal processing and preparation	
X20DS1119	X20 multifunctional digital signal processor, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module	
X20cDS1119	X20 multifunctional digital signal processor, coated, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 357: X20DS1119, X20cDS1119 - Order data

4.16.4.4 Technical data

Product ID	X20DS1119	X20cDS1119
Short description		
I/O module	3 digital 5 V (symmetrical) channels configurable as inputs or outputs, 2 digital 24 V (asymmetrical) input channels, 1 universal counter pair (2 event counters, AB counter or up/down counter), linear movement generator (A/B; direction/frequency) with one reference pulse, SSI absolute encoder, relative or absolute times of input edges in µs resolution, time-triggered I/O, I/O oversampling	
General information		
B&R ID code	0xA067	0xE20D
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Inputs/Outputs	Yes, using status LED	
Power consumption		
Bus	0.01 W	
Internal I/O	1.5 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Type of signal lines	Shielded cables must be used for all signal lines.	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Linear movement generator		
Quantity	1	
Encoder outputs	5 V, symmetrical (A/B; direction/frequency)	
Counter size	16/32-bit	
SSI absolute encoder		
Quantity	1	
Counter size	Encoder-dependent up to 32-bit	
Max. transfer rate	1 Mbit/s	
Encoder signal	5 V, symmetrical	
Encoder supply		
5 VDC	±5%, module-internal, max. 300 mA	
24 VDC	Module-internal, max. 300 mA	
Digital inputs 5 VDC		
Quantity	Up to 3, configurable as inputs or outputs using software	
Nominal voltage	5 VDC differential signal, EiA RS485 standard	
Input frequency	600 kHz	
Common-mode range	$-7\ V \leq V_{CM} \leq +12\ V$	
Isolation voltage between encoder and bus	500 V_{eff}	
Overload behavior of the encoder supply	Short circuit protection, overload protection	

Table 358: X20DS1119, X20cDS1119 - Technical data

Product ID	X20DS1119	X20cDS1119
Input filter		
Hardware	≤200 ns	
Software	-	
Additional functions	SSI absolute encoder, universal counter pair	
Digital inputs 24 VDC		
Quantity	2	
Nominal voltage	24 VDC	
Input frequency	100 kHz	
Input circuit	Sink	
Input voltage	24 VDC -15 % / +20 %	
Input current at 24 VDC	Approx. 3.4 mA	
Input resistance	Approx. 7.19 kΩ	
Isolation voltage between channel and bus	500 V_{eff}	
Input filter		
Hardware	≤2 µs	
Software	-	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Additional functions	Latch function for universal counter pair	
Universal counter pair		
Quantity	1	
Operating modes	2x event counter, up/down counter, AB counter	
Encoder inputs	5 V, symmetrical	
Counter size	16/32-bit	
Input frequency	Max. 600 kHz	
Evaluation		
AB counter	4x	
Event counter	2x	
Up/Down counter	2x	
Encoder supply		
5 VDC	±5%, module-internal, max. 300 mA	
24 VDC	Module-internal, max. 300 mA	
Digital outputs 5 VDC		
Quantity	Up to 3, configurable as inputs or outputs using software	
Type	5 VDC differential signal, EiA RS485 standard	
Output circuit	Sink and/or source	
Output protection	Short circuit protection	
Design	Push/Pull/Push-Pull	
Diagnostic status	Readable output	
Isolation voltage between channel and bus	500 V_{eff}	
Switching voltage	5 VDC differential signal, EiA RS485 standard	
Additional functions	SSI absolute encoder, linear movement generator	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 358: X20DS1119, X20cDS1119 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.16.4.5 LED status indicators

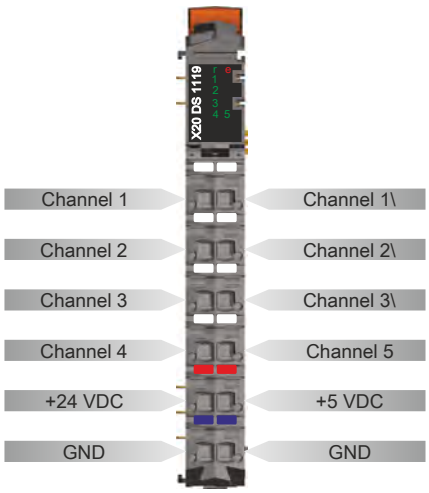
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	I/O error. Possible causes: • SSI error[2]
			Double flash	System error. Possible causes: • Motion function error[3] • I/O oversampling error[4] • Edge detection error[4]
			Triple flash	I/O error and system error occur together
			On	Error or reset status
	1 - 8	Green		Status of the corresponding digital signal

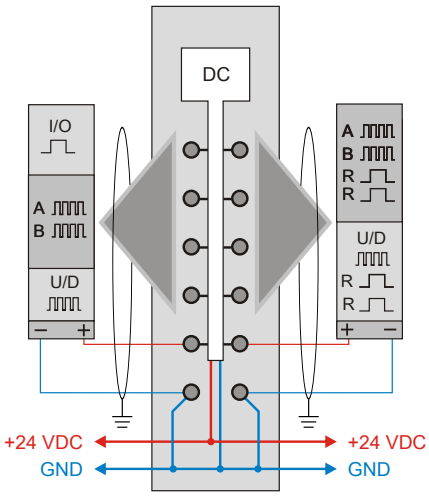
1) Depending on the configuration, a firmware update can take up to several minutes.
2) See 4.16.4.11.6.2 "Error state - SSI" register for the exact error description.
3) See 4.16.4.11.6.3 "Error state - Motion functions" register for the exact error description.
4) See 4.16.4.11.6.1 "Error state - Output data and edge detection" register for the exact error description.

4.16.4.6 Pinout

Shielded cables must be used for all signal lines.

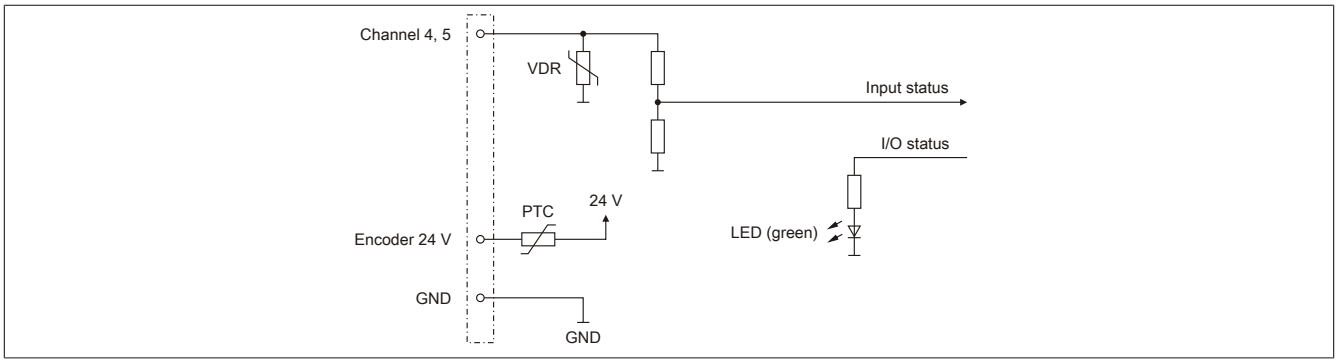


4.16.4.7 Connection example

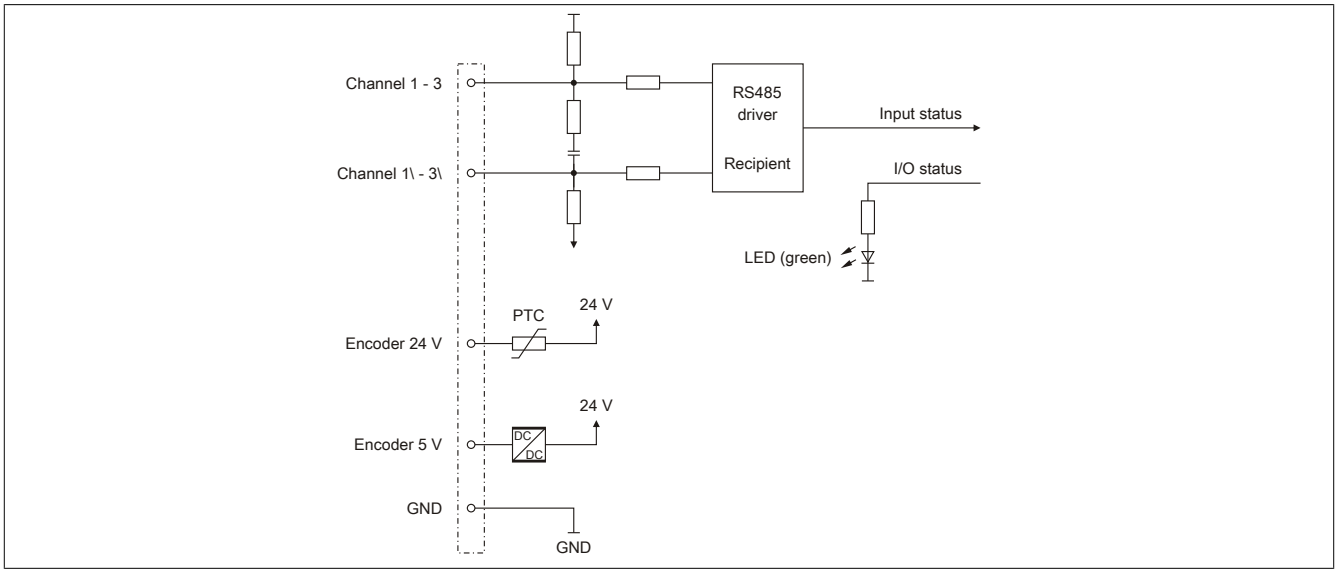


4.16.4.8 Input circuit diagram

Asymmetrical +24 VDC

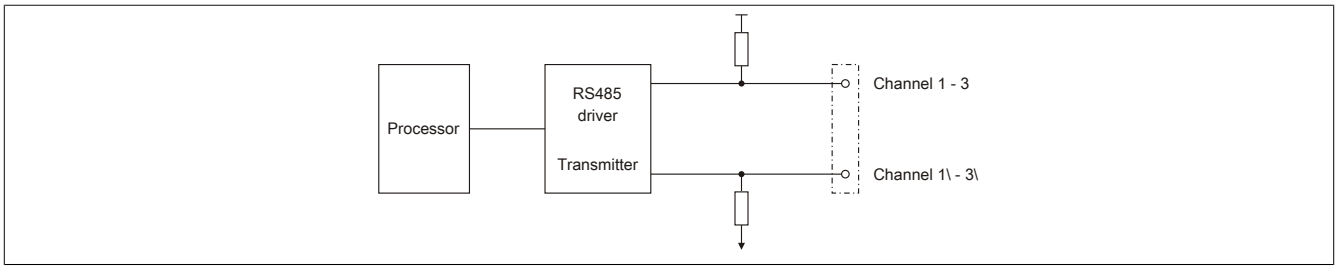


Symmetrical +5 VDC



4.16.4.9 Output circuit diagram

Symmetrical +5 VDC



4.16.4.10 Connection options

Digital input/output

Channel	Function
1	Input / Output (5 V symmetrical)
2	Input / Output (5 V symmetrical)
3	Input / Output (5 V symmetrical)
4	Input (24 V asymmetrical)
5	Input (24 V asymmetrical)

Wiring of the SSI absolute encoder

Channel	Function
1 (input)	Data
2 (output)	Clock

Wiring of the linear movement generator

Channel	Up-Down	AB
1 (output)	Direction	A
2 (output)	Frequency	B
3 (output)	Reference	

Wiring of the universal counter pair

Channel	Edge counters	Up/Down counter	Incremental
1 (input)	Input 1	Direction	A
2 (input)	Input 2	Frequency	B
3 (input)	Latch input 1 (R)		
5 (input)	Latch input 2 (E)		

4.16.4.11 Register description

4.16.4.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.16.4.11.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - General						
513	CfO_SIframeGenID	USINT				•
Configuration - System timer						
642	CfO_SystemCycleTime	UINT				•
646	CfO_SystemCycleOffset	INT				•
650	CfO_SystemCyclePrescaler	UINT				•
Configuration - Physical I/O						
769 + (N-1) * 2	CfO_PhyIOConfigCh0N (Index N = 1 to 5)	USINT				•
Configuration - Direct I/O						
899	CfO_DirectIOClearMask0_7	USINT				•
903	CfO_DirectIOSetMask0_7	USINT				•
905	CfO_OutputUpdateCycle	USINT				•
Configuration - Oversampled I/O						
1025	CfO_OversampleMode	USINT				•
1027	CfO_OversampleSampleCycleID	USINT				•
1029	CfO_OversampleRelativeCycleID	USINT				•
1031	CfO_OversampleConsumeCycleID	USINT				•
1033	CfO_OversampleOutputBits	USINT				•
1035	CfO_OversampleInputBits	USINT				•
1037	CfO_OversampleOutputWindow	USINT				•
1039	CfO_OversampleInputWindow	USINT				•
1041 + (N*2)	CfO_OversampleConfigInputN (Index N = 0 to 3)	USINT				•
1049 + (N*2)	CfO_OversampleConfigOutputN (Index N = 0 to 3)	USINT				•
Configuration - Edge detection						
1537	CfO_EdgeDetectPollCycleID	USINT				•
1548	CfO_EdgeDetectEventEnable	UDINT				•
1665 + (N-1) * 16	CfO_EdgeDetectUnit0NMode (Index N = 1 to 4)	USINT				•
1667 + (N-1) * 16	CfO_EdgeDetectUnit0NLeading (Index N = 1 to 4)	USINT				•
1669 + (N-1) * 16	CfO_EdgeDetectUnit0NMaster (Index N = 1 to 4)	USINT				•
1671 + (N-1) * 16	CfO_EdgeDetectUnit0NSlave (Index N = 1 to 4)	USINT				•
Configuration - Movement functions						
4097	CfO_FifoSize	USINT				•
4099	CfO_Mode	SINT				•
4101	CfO_SpeedLimit	USINT				•
4103	CfO_FormatAdjust	USINT				•
4105	CfO_TimeStampRange	SINT				•
4107	CfO_PositionRange	SINT				•
4109	CfO_Reference0Range	SINT				•
4111	CfO_Reference1Range	SINT				•
4116	CfO_TimeStampDelay	DINT				•
4124	CfO_SpeedCycleTime_32bit	UDINT				•
4129	CfO_ResolPosition	SINT				•
4131	CfO_ResolSpeed	SINT				•
4220	CfO_AccelDataInit	UDINT				•
4260	CfO_Reference0Start	DINT				•
4268	CfO_Reference0StopMargin	DINT				•
4276	CfO_Reference1Start	DINT				•
4284	CfO_Reference1StopMargin	DINT				•
Configuration - SSI						
2049	CfO_CycleSelect	USINT				•
2051	CfO_PhysicalMode	USINT				•
2053	CfO_DataBits	USINT				•
2055	CfO_NullBits	USINT				•
Configuration - Universal counter						
6145	CfO_CounterCycleSelect	USINT				•
6147	CfO_CounterMode	USINT				•

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
6149	CfO_LatchMode	USINT				●
6151	CfO_LatchComparator	USINT				●
6153	CounterControl	USINT			●	
	CounterReset	Bit 0				
	LatchEnable	Bit 1				
Communication - General						
546	ProtocolError (16-bit)	USINT	●			
547	ProtocolError (8-bit)	UINT	●			
550	ProtocolSequenceViolation (16-bit)	UINT	●			
551	ProtocolSequenceViolation (8-bit)	USINT	●			
Communication - Error register						
257	Error state register - Output data and edge detection	USINT	●			
	OutputControlError	Bit 4				
	OutputCopyError	Bit 5				
	EdgeDetectError	Bit 6				
259	Error state register - SSI	USINT	●			
	SSICycleTimeViolation	Bit 0				
	SSIParityError	Bit 1				
261	Error state register - Movement functions	USINT	●			
	MovFifoEmpty	Bit 0				
	MovFifoFull	Bit 1				
	MovTargetTimeViolation	Bit 2				
	MovMaxFrequencyViolation	Bit 3				
321	Acknowledge error message register - Output data and edge detection	USINT			●	
	QuitOutputControlError	Bit 4				
	QuitOutputCopyError	Bit 5				
	QuitEdgeDetectError	Bit 6				
323	Acknowledge error message register - SSI	USINT			●	
	SSIQuitCycleTimeViolation	Bit 0				
	SSIQuitParityError	Bit 1				
325	Acknowledge error message register - Movement functions	USINT			●	
	MovQuitFifoEmpty	Bit 0				
	MovQuitFifoFull	Bit 1				
	MovQuitTargetTimeViolation	Bit 2				
	MovQuitMaxFrequencyViolation	Bit 3				
Communication - System timer						
683	SDCLifeCount	SINT	●			
Communication - Direct I/O						
915	"DigitalOutput" register	USINT			●	
	DigitalOutput03	Bit 2				
	DigitalOutput04	Bit 3				
	DigitalOutput07	Bit 6				
	DigitalOutput08	Bit 7				
927	"DigitalInput" register	USINT	●			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
Communication - Oversampled I/O (output)						
1059	Oversample register - Configuration	USINT			●	
	OversampleEnable	Bit 0				
	OversampleOutputValidate	Bit 1				
1063	OversampleOutputCycle	USINT			●	
	OversampleSampleOffset	USINT			●	
1088 + N	OversampleOutput0NSample1_8 (Index N = 1 to 4)	USINT			●	
1092 + N	OversampleOutput0NSample9_16 (Index N = 1 to 4)	USINT			●	
1096 + N	OversampleOutput0NSample17_24 (Index N = 1 to 4)	USINT			●	
1100 + N	OversampleOutput0NSample25_32 (Index N = 1 to 4)	USINT			●	
1104 + N	OversampleOutput0NSample33_40 (Index N = 1 to 4)	USINT			●	
1108 + N	OversampleOutput0NSample41_48 (Index N = 1 to 4)	USINT			●	
1112 + N	OversampleOutput0NSample49_56 (Index N = 1 to 4)	USINT			●	
1116 + N	OversampleOutput0NSample57_64 (Index N = 1 to 4)	USINT			●	
Communication - Oversampled I/O (input)						
1074	OversampleInputTime	INT	●			
1079	OversampleInputCycle	USINT	●			
1120 + N	OversampleInput0NSample64_57 (Index N = 1 to 4)	USINT	●			
1124 + N	OversampleInput0NSample56_49 (Index N = 1 to 4)	USINT	●			
1128 + N	OversampleInput0NSample48_41 (Index N = 1 to 4)	USINT	●			
1132 + N	OversampleInput0NSample40_33 (Index N = 1 to 4)	USINT	●			
1136 + N	OversampleInput0NSample32_25 (Index N = 1 to 4)	USINT	●			
1140 + N	OversampleInput0NSample24_17 (Index N = 1 to 4)	USINT	●			
1144 + N	OversampleInput0NSample16_9 (Index N = 1 to 4)	USINT	●			
1148 + N	OversampleInput0NSample8_1 (Index N = 1 to 4)	USINT	●			
Communication - Edge detection						

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
1794 + (N-1) * 32	EdgeDetect0NMastercount (16-bit) (Index N = 1 to 4)	INT	●			
1795 + (N-1) * 32	EdgeDetect0NMastercount (8-bit) (Index N = 1 to 4)	SINT	●			
1798 + (N-1) * 32	EdgeDetect0NSlavecount (16-bit) (Index N = 1 to 4)	INT	●			
1799 + (N-1) * 32	EdgeDetect0NSlavecount (8-bit) (Index N = 1 to 4)	SINT	●			
1804 + (N-1) * 32	EdgeDetect0NDifference (32-bit) (Index N = 1 to 4)	DINT	●			
1806 + (N-1) * 32	EdgeDetect0NDifference (16-bit) (Index N = 1 to 4)	INT	●			
1812 + (N-1) * 32	EdgeDetect0NMastertime (32-bit) (Index N = 1 to 4)	DINT	●			
1814 + (N-1) * 32	EdgeDetect0NMastertime (16-bit) (Index N = 1 to 4)	INT	●			
1820 + (N-1) * 32	EdgeDetect0NSlavetime (32-bit) (Index N = 1 to 4)	DINT	●			
1822 + (N-1) * 32	EdgeDetect0NSlavetime (16-bit) (Index N = 1 to 4)	INT	●			
Communication - Movement functions						
4225	MovementControl	USINT			●	
	MovPosEnable	Bit 0				
	MovSpeedEnable	Bit 1				
4244	MovTargetTime (32-bit)	DINT			●	
4246	MovTargetTime (16-bit)	INT			●	
4252	MovTargetPosition (32-bit)	DINT			●	
4254	MovTargetPosition (16-bit)	INT			●	
4260	MovReference1Start (32-bit)	DINT			●	
4262	MovReference1Start (16-bit)	INT			●	
4268	MovReference1StopMargin (32-bit)	DINT			●	
4270	MovReference1StopMargin (16-bit)	INT			●	
4276	MovReference2Start (32-bit)	DINT			●	
4278	MovReference2Start (16-bit)	INT			●	
4284	MovReference2StopMargin (32-bit)	DINT			●	
4286	MovReference2StopMargin (16-bit)	INT			●	
4212	MovSpeed (32-bit)	DINT			●	
4210	MovSpeed (16-bit)	INT			●	
4220	MovAcceleration (32-bit)	UDINT			●	
4218	MovAcceleration (16-bit)	UINT			●	
4292	MovTimeValid (32-bit)	DINT	●			
4294	MovTimeValid (16-bit)	INT	●			
4300	MovPosition (32-bit)	DINT	●			
4302	MovPosition (16-bit)	INT	●			
Communication - SSI						
2084	SSITimeValid (32-bit)	DINT	●			
2086	SSITimeValid (16-bit)	INT	●			
2092	SSITimeChanged (32-bit)	DINT	●			
2094	SSITimeChanged (16-bit)	INT	●			
2100	SSIPosition (32-bit)	(U)DINT	●			
2102	SSIPosition (16-bit)	UINT	●			
Communication - Universal counter						
6303	LatchCount	SINT	●			
6308	CounterTimeValid (32-bit)	DINT	●			
6310	CounterTimeValid (16-bit)	INT	●			
6324	Counter01TimeChanged (32-bit)	DINT	●			
6326	Counter01TimeChanged (16-bit)	INT	●			
6332	Counter02TimeChanged (32-bit)	DINT	●			
6334	Counter02TimeChanged (16-bit)	INT	●			
6340	CounterValue01 (32-bit)	DINT	●			
6342	CounterValue01 (16-bit)	INT	●			
6348	CounterValue02 (32-bit)	DINT	●			
6350	CounterValue02 (16-bit)	INT	●			
6356	CounterLatch01 (32-bit)	DINT	●			
6358	CounterLatch01 (16-bit)	INT	●			
6364	CounterLatch02 (32-bit)	DINT	●			
6366	CounterLatch02 (16-bit)	INT	●			
6372	CounterRel01 (32-bit)	DINT	●			
6374	CounterRel01 (16-bit)	INT	●			
6380	CounterRel02 (32-bit)	DINT	●			
6382	CounterRel02 (16-bit)	INT	●			

4.16.4.11.3 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.16.4.11.4 General

4.16.4.11.4.1 Use with Automation Studio

The module is supported via X2X Link and POWERLINK.

X2X Link supports a up to 28 bytes of synchronous data per module. To optimize use and to prevent needless data transfer, the data points can be adjusted as needed in Automation Studio. Data points that are not needed can be disabled, and the bit width of the data points can be defined.

4.16.4.11.4.2 Timestamp function

The timestamp function is based on synchronized timers. When a timestamp event occurs, the module immediately saves the current net time. After the respective data is transmitted to the CPU, including this precise time, the CPU can then evaluate the data using its own net time (or system time).

Conversely, the CPU can predefine output events, apply a timestamp and transfer them to the module. The module then executes the predefined action at the precise time defined by the CPU.

The resolution of the timestamp is up to 1/8 µs in both directions.

4.16.4.11.4.3 Synchronization jitter

Because the CPU – which determines the X2X net time – and the module have different clocks, the module's internal X2X net time must be synchronized with the CPU's net time. Due to this synchronization, the module's internal X2X net time is corrected by a maximum of 1/8 µs per system cycle if necessary. This synchronization jitter becomes noticeable when using the net time with 1/8 µs resolution (max. ±1/8 µs).

If a 100% exact 1/8 µs resolution without jitter is required, then the "localtime 1/8 µs" must be used (see the 4.16.4.11.11.3 "CfO_EdgeDetectUnitMode" register).

4.16.4.11.5 General registers

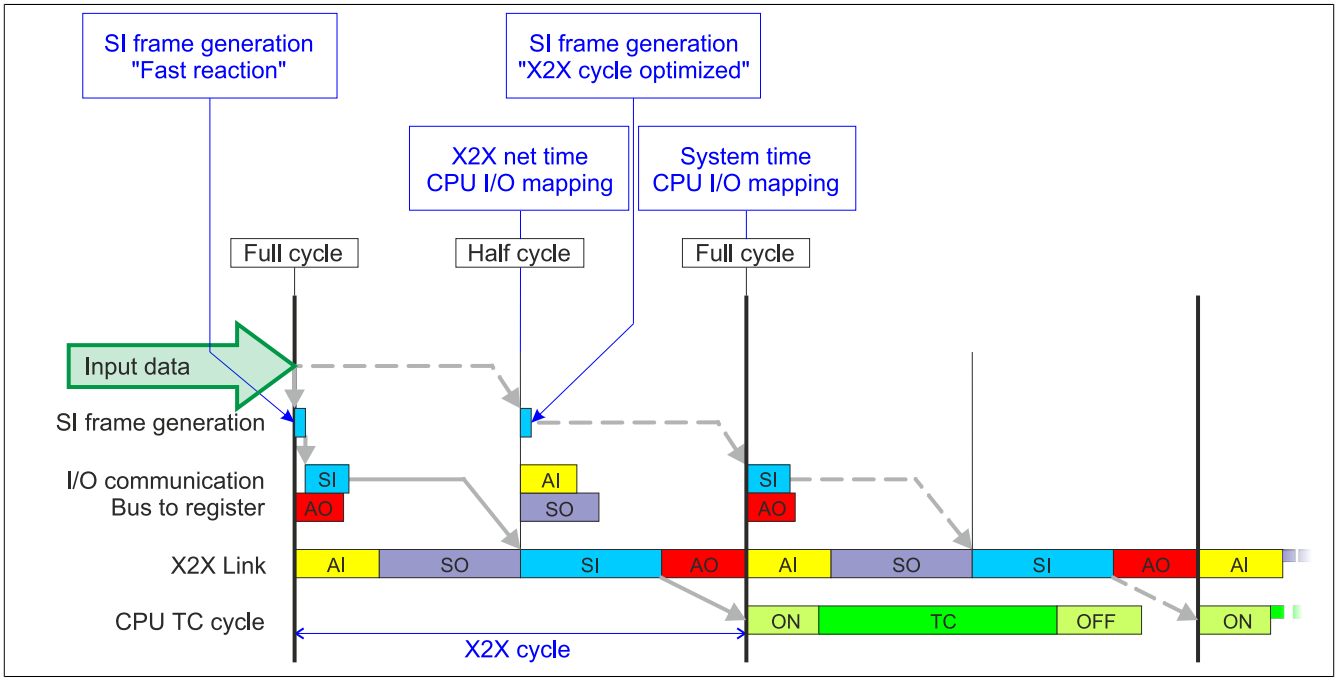
4.16.4.11.5.1 "CfO_SIframeGenID" register

Name:
CfO_SIframeGenID
"SI-frame generation" in the AS I/O configuration.

This register determines when the synchronous input data is generated for transfer. This has a decisive effect on the timing of the input data.

The setting "Fast reaction" causes the input data to be available one X2X cycle sooner in the CPU. However, this setting also has a negative effect on the minimum X2X cycle time.

Data type	Value	Information
USINT	9	X2X cycle optimized
	14	Fast reaction



4.16.4.11.5.2 "ProtocolError" register

Name:
ProtocolError

This register contains an error counter that specifies the number of X2X protocol errors. In the I/O configuration, the "Network information" parameter can be used to help configure a data point for this register with a bit width of 8 or 16 bits in the I/O mapping.

Data type	Value	Information
USINT	0 to 255	Error counter (8-bit)
UINT	0 to 65,535	Error counter (16-bit)

4.16.4.11.5.3 "ProtocolSequenceViolation" register

Name:
ProtocolSequenceViolation

This register contains an error counter that specifies the number of X2X sequence violations. In the I/O configuration, the "Network information" parameter can be used to help configure a data point with a bit width of 8 or 16 bits in the I/O mapping.

Data type	Value	Information
USINT	0 to 255	Error counter (8-bit)
UINT	0 to 65,535	Error counter (16-bit)

4.16.4.11.5.4 "SDCLifeCount" register

Name:
SDCLifeCount

Counter that is incremented with each system timer cycle. The "SDC information" setting in the AS I/O configuration can be used to activate this register in the I/O mapping as the data point, "SDCLifeCount".

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.16.4.11.6 Error handling

If one of the functions detects an error, then an error bit is set in one of the error state registers. The application is now able to react accordingly and acknowledge the errors by setting a respective bit in the "Acknowledge error message" registers. This causes the bit to be reset in the error state register. If the source of the error persists, then the error bit is set again as soon as the error is detected again (i.e. cannot be reset).

Acknowledging the error does not affect the module's functionality. If possible, the module automatically resumes processing as soon as the source of the error has been corrected.

If an error occurs (not a warning), this is indicated by the red "e" LED on the module (double flash). This signal is automatically acknowledged as soon as the source of the error has been corrected.

4.16.4.11.6.1 Error state register - Output data and edge detection

Name:
OutputControlError
OutputCopyError
EdgeDetectError

Errors in the output data and cycle time settings are indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	OutputControlError	0	No error
		1	The module did not receive new data in time while in the mode "Output control mode = single", meaning that a bit that has already been output would have been output again by the output control buffer.
5	OutputCopyError	0	No error
		1	Oversampling output data could not be copied to the output control buffer. (e.g. an attempt was made to write oversampling output data to an address outside of the OversampleOutputWindow).
6	EdgeDetectError	0	No error
		1	Cycle time violation edge detection: The "EdgeDetectPollCycle" must be smaller than or equal to 255 µs. This error is caused if the cycle defined in the 4.16.4.11.11.1 "CfO_EdgeDetectPollCycleID" register is > 255 µs.
7	Reserved	-	

4.16.4.11.6.2 Error state register - SSI

Name:
SSICycleTimeViolation
SSIParityError

SSI interface errors are indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	SSICycleTimeViolation	0	No error
		1	Error occurred, possible causes: • SSI transfer takes longer than the defined "Update cycle". • Monoflop check is enabled and the SSI data line does not assume the defined level after the transfer is complete.
1	SSIParityError	0	No error
		1	SSI parity error
2 - 7	Reserved	-	

4.16.4.11.6.3 Error state register - Movement functions

Name:
MovFifoEmpty
MovFifoFull
MovTargetTimeViolation
MovMaxFrequencyViolation

Movement function errors are indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	MovFifoEmpty	0	No error
		1	The position/timestamp FIFO is empty.
1	MovFifoFull	0	No error
		1	The position/timestamp FIFO has exceeded the size defined in the 4.16.4.11.12.3 "FifoSize" register.
2	MovTargetTimeViolation	0	No error
		1	This only occurs when the 4.16.4.11.12.18 "MovTargetTime" is in the past.
3	MovMaxFrequencyViolation	0	No error
		1	The maximum output frequency setpoint has exceeded the maximum frequency configured in the 4.16.4.11.12.4 "CfO_SpeedLimit" register.
4 - 7	Reserved	-	

4.16.4.11.6.4 Acknowledge error message register - Output data and edge detection

Name:
QuitOutputControlError
QuitOutputCopyError
QuitEdgeDetectError

Error messages from the 4.16.4.11.6.1 "Error state - Output data and edge detection" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	QuitOutputControlError	0	No change
		1	Acknowledge error
5	QuitOutputCopyError	0	No change
		1	Acknowledge error
6	QuitEdgeDetectError	0	No change
		1	Acknowledge error
7	Reserved	-	

4.16.4.11.6.5 Acknowledge error message register - SSI

Name:
SSIQuitCycleTimeViolation
SSIQuitParityError

Error messages from the 4.16.4.11.6.2 "Error state - SSI" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	SSIQuitCycleTimeViolation	0	No change
		1	Acknowledge error
1	SSIQuitParityError	0	No change
		1	Acknowledge error
2 - 7	Reserved	-	

4.16.4.11.6.6 Acknowledge error message register - Movement functions

Name:
MovQuitFifoEmpty
MovQuitFifoFull
MovQuitTargetTimeViolation
MovQuitMaxFrequencyViolation

Error messages from the 4.16.4.11.6.3 "Error state - Movement functions" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	MovQuitFifoEmpty	0	No change
		1	Acknowledge error
1	MovQuitFifoFull	0	No change
		1	Acknowledge error
2	MovQuitTargetTimeViolation	0	No change
		1	Acknowledge error
3	MovQuitMaxFrequencyViolation	0	No change
		1	Acknowledge error
4 - 7	Reserved	-	

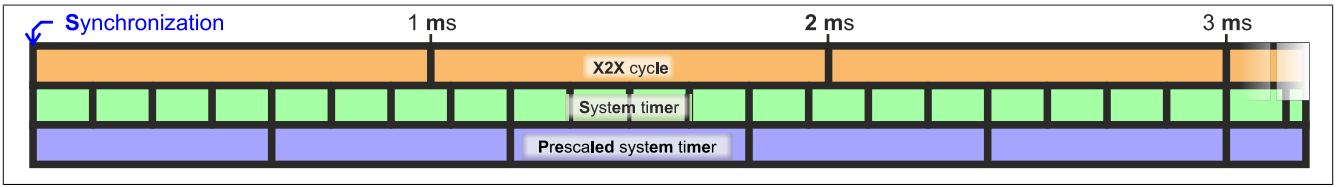
4.16.4.11.7 System timer

The module's individual functions all depend on a system timer. This internal "system cycle time" can be defined from 25 to 255 µs. The functions can also be run with the help of a configurable "prescaled system timer" to minimize the load on the module, thereby making it possible to use the shortest possible X2X cycle time.

The cycle of the "prescaled system timer" (and system timer) is referenced with the X2X Link as soon as the module has been started up and the X2X Link has been initialized. Since the system timer and the module's internal X2X net time use the same clock, the two run synchronously from that point on. An X2X cycle time that is not a multiple of the system cycle time results in an offset, which can be calculated.

The following values apply to the following example:

X2X cycle	1 ms
System timer	150 µs
Prescaled system timer	4



4.16.4.11.7.1 "CfO_SystemCycleTime" register

Name:
CfO_SystemCycleTime
"Cycle time" in the AS I/O configuration.

The cycle time of the system timer can be set in this register in steps of 1/8 µs. The value entered in the AS I/O configuration is automatically multiplied by 8.

Information:

A setting < 50 µs has a negative effect on the minimum X2X cycle time!

Data type	Value	Information
UINT	200 to 2047	System timer cycle time in steps of 1/8 µs (25 to 255,875 µs)

4.16.4.11.7.2 "CfO_SystemCycleOffset" register

Name:
CfO_SystemCycleOffset
"Cycle offset" in the AS I/O configuration.

The synchronization time for the system cycle can be offset in this register in steps of 1/8 µs. The value entered in the AS I/O configuration is automatically multiplied by 8.

Data type	Value	Information
INT	-32,768 to 32,767	Cycle offset in steps of 1/8 µs (-4096 to 4095.875 µs)

4.16.4.11.7.3 "CfO_SystemCyclePrescaler" register

Name:
CfO_SystemCyclePrescaler
"Cycle prescaler" in the AS I/O configuration.

The prescaler for setting the "Prescaled system timer" can be configured in this register. The cycle time of the specified system timer is a product of the system timer multiple set in this register.

The "prescaled system timer" can be used as alternative time source for the individual functions. This is useful if a function requires a very short system cycle. To reduce the load on the module in such a situation, other functions can be processed in a slow cycle.

Data type	Value	Information
UINT	2 to 128	Multiple of the system timer

4.16.4.11.8 Physical I/O configuration

4.16.4.11.8.1 "CfO_PhyIOConfigCh" registers

Name:
CfO_PhyIOConfigCh01 to CfO_PhyIOConfigCh05

The physical I/O channels can each be configured individually in these registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Push driver[1)]	0	Disabled
		1	Enabled
1	Pull driver[1)]	0	Disabled
		1	Enabled
2	Input inverted	0	Not inverted
		1	Inverse
3	Output inverted[1)]	0	Not inverted
		1	Inverse
4 - 7	Output function[1)]	0 to 15	See: Overview of output channel functions

1) Only available for I/O channels 1 to 3

Overview of output channel functions

Values of bits 4 to 7	Output channel 1	Output channel 2	Output channel 3
0	Direct I/O	Direct I/O	Direct I/O
1		SSI clock output	
2	ABR emulation (A)	ABR emulation (B)	ABR emulation (reference)
3	Up/down emulation (direction)	Up/down emulation (frequency)	Up/down emulation (reference)
4 - 15	Reserved		

4.16.4.11.9 Direct I/O

Direct I/O makes it possible to use the physical I/Os like normal I/Os. Additionally, the application can only set or reset I/Os (e.g. an output channel is set by the edge generator and manually reset by the application).

4.16.4.11.9.1 "CfO_DirectIOClearMask0_7" register

Name:
CfO_DirectIOClearMask0_7
"Direct control of output channel 01" to "Direct control of output channel 03" in the AS I/O configuration.

If the bit for the respective channel is set in this register, then the output is reset as soon as its direct I/O output channel is reset (4.16.4.11.9.3 "output control channel 7_0" or "DigitalOutput0x" register in the AS I/O mapping).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Output channel 0	0	No change
		1	Reset channel
1	Output channel 1	0	No change
		1	Reset channel
2	Output channel 2	0	No change
		1	Reset channel
3 - 7	Reserved	-	

4.16.4.11.9.2 "CfO_DirectIOSetMask0_7" register

Name:
CfO_DirectIOSetMask0_7
"Direct control of output channel 01" to "Direct control of output channel 03" in the AS I/O configuration.

If the bit for the respective channel is set in this register, then the output is set as soon as its direct I/O output channel is set (4.16.4.11.9.3 "output control channel 7_0" or "DigitalOutput0x" register in the AS I/O mapping).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Output channel 0	0	No change
		1	Set channel
1	Output channel 1	0	No change
		1	Set channel
2	Output channel 2	0	No change
		1	Set channel
3 - 7	Reserved	-	

4.16.4.11.9.3 "DigitalOutput" register

Name:
DigitalOutput01 to DigitalOutput03

The register contains the bits for controlling the direct I/O output channels. Depending on how the 4.16.4.11.9.1 "CfO_DirectIOClearMask0_7" and 4.16.4.11.9.2 "CfO_DirectIOSetMask0_7" registers are configured, the digital outputs are set to the status of the respective bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput01	0 or 1	Output status of the channel
1	DigitalOutput02	0 or 1	Output status of the channel
2	DigitalOutput03	0 or 1	Output status of the channel
3 - 7	Reserved	-	

4.16.4.11.9.4 "DigitalInput" register

Name:
DigitalInput01 to DigitalInput05

This register displays the status of the digital input channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalInput01	0 or 1	Input status of channel 1
1	DigitalInput02	0 or 1	Input status of channel 2
2	DigitalInput03	0 or 1	Input status of channel 3
3	Reserved	-	
4	DigitalInput04	0 or 1	Input status of channel 4
5	DigitalInput05	0 or 1	Input status of channel 5
6 - 7	Reserved	-	

4.16.4.11.10 Oversampled I/O

"Oversampled I/O" is based on input status buffers and output control buffers. Input data acquisition and output control occur in one sample cycle (one sample cycle equals one bit in the buffer). The precise time of an input buffer entry is indicated by its position in the buffer and the net time assigned to the buffer.

In "Output control mode = single" every output buffer entry is marked as invalid once it has been executed. This ensures that the outputs are not supplied with invalid data. In this mode, the application needs to ensure that the module is always supplied with valid data.

When using "Output control mode = continuous" the contents of the buffer are output again if the module is not supplied with new oversample output data.

4.16.4.11.10.1 Addressing the output control buffer

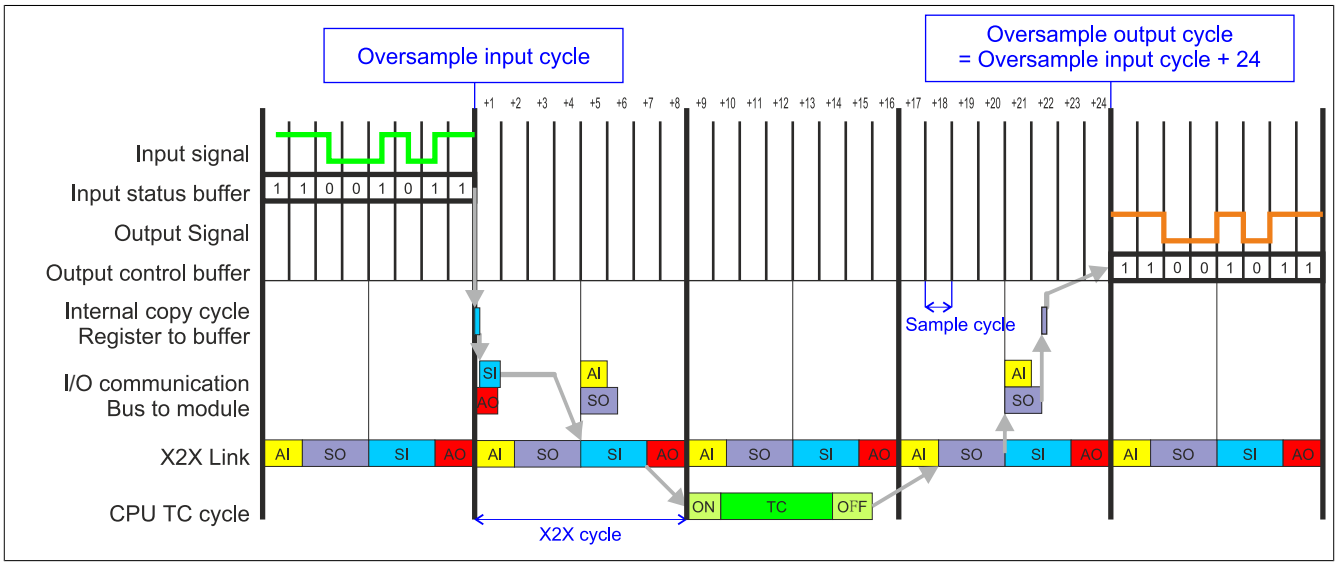
The module has one cyclic 256-bit output control buffer for each oversample channel. One bit is output from these buffers to the configured physical output channels in each "sample cycle". When new data is transferred to one of these buffers, the application must define where in the respective buffer the data should be written to. There are 2 possibilities (absolute or relative "Output mode" in the AS I/O configuration).

Absolute addressing of the output control buffer

With absolute addressing, in each cycle where "OversampleOutputValidate = True", in addition to the oversample output sample data (in the 4.16.4.11.10.15 "OversampleOutput0NSample" registers) an address must also be transferred in the 4.16.4.11.10.13 "OversampleOutputCycle" register. This address determines where in the output control buffer the new data should be copied to. In order to calculate this address, you must account for the contents of the 4.16.4.11.10.17 "OversampleInputCycle" register, which contains the address of the most recently output data, and the transfer time to the module. To help avoid incorrect addressing of the output control buffer, the buffer section that is capable of being written to can be limited using the 4.16.4.11.10.8 "OversampleOutputWindow" register. This window will always be shifted relative to the current sample address. An "OutputCopyError" will be triggered if an attempt is made to write to an address that is outside of this window.

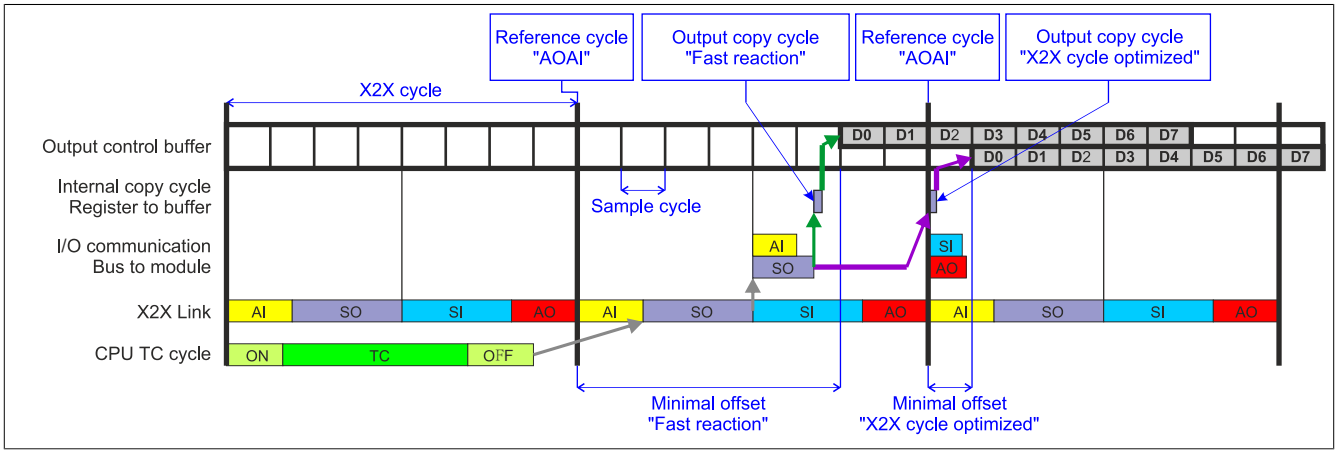
Example

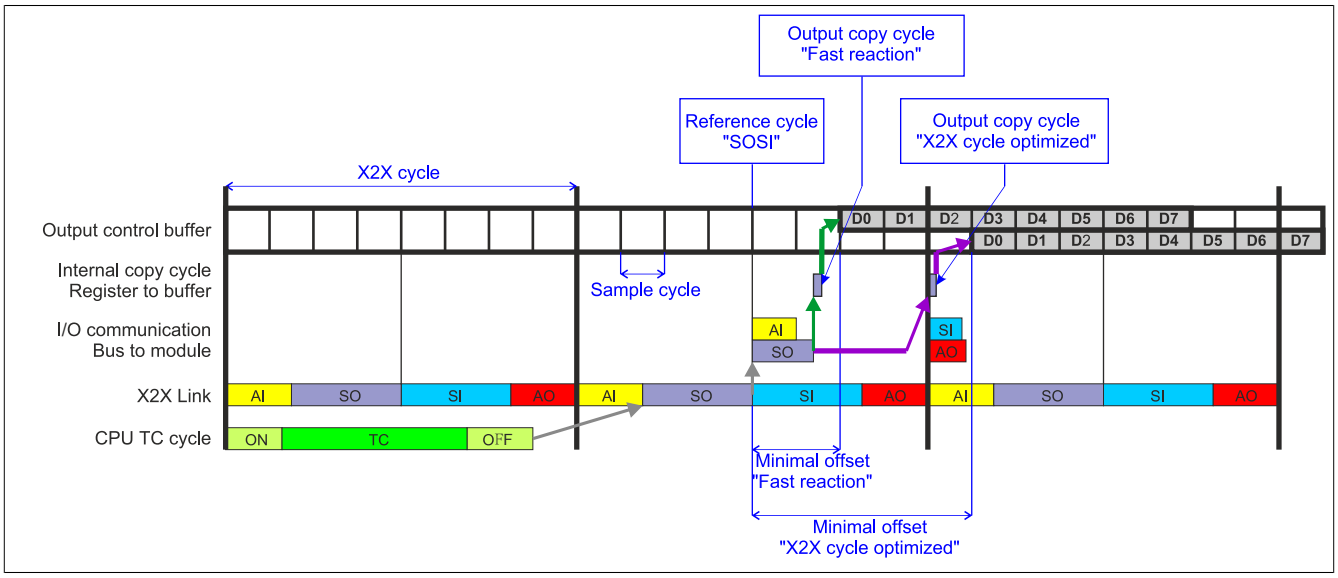
Timing from oversample input cycle to oversample output cycle in absolute output mode ("SI-frame generation = Fast reaction", "Output copy cycle = Fast reaction", 8 samples per X2X cycle):



Relative addressing of the output control buffer

When "OversampleOutputValidate = True", then the oversample output sample data is automatically copied to an address relative to the last referenced address at the defined "output copy cycle" time. The 4.16.4.11.10.14 "OversampleSampleOffset" register serves as the offset. The new data cannot start being output immediately at the "output copy cycle" time because it takes time to copy the data from the registers to the buffer. This means that an offset of 0 is not allowed. The relative output control buffer address + offset must point to an address within the "oversample output window". The "oversample output window" is always offset relative to the current sample address. An "OutputCopyError" is triggered if an attempt is made to write to an address that is outside of this window.





4.16.4.11.10.2 "CfO_OversampleMode" register

Name:
CfO_OversampleMode
"Output mode" in the AS I/O configuration
"Output control mode" in the AS I/O configuration.

The output control buffer can be configured globally for all channels in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Addressing the output control buffer "Output mode" in the AS I/O configuration.	0	Absolute addressing of the output control buffer
		1	Relative addressing of the output control buffer
1	Cyclic output control "Output control mode" in the AS I/O configuration.	0	Single Output control buffer entry is marked invalid after execution.
		1	Continuous Output control buffer entry is not changed.
2 - 7	Reserved	-	

Cyclic output control

If cyclic output control is enabled, then all data in the output control buffer is marked invalid as soon as it is output ("Output control mode = single"). An OutputControlError is generated if the module does not receive data in time, thereby causing a situation in which a bit that has already been output would be output in the buffer again. In such a situation, the output assumes the "Output default state" configured in the 4.16.4.11.10.10 "CfO_OversampleConfigOutput" register.

If cyclic output control is disabled, then the data is output again if the output control buffer overflows ("Output control mode = continuous").

Information:

All 256 bits of the output control buffer are always output.

4.16.4.11.10.3 "CfO_OversampleSampleCycleID" register

Name:
CfO_OversampleSampleCycleID
"Sample cycle" in the AS I/O configuration.

The source of the sample cycle can be configured in this register. During each sample cycle, one bit from the output control buffers of the oversampled I/O channels is output to the configured physical output, and the status of the configured inputs is entered in one bit of the respective input status buffer.

Data type	Value	Information
USINT	2	System timer The value configured in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used as the sample cycle.
	3	Prescaled system timer The "prescaled system timer" is used as sample cycle.
	10	AOAI The sample cycle is clocked with the AOAI interrupt of the X2X cycle.
	14	SOSI The sample cycle is clocked with the SOSI interrupt of the X2X cycle.

4.16.4.11.10.4 "CfO_OversampleRelativeCycleID" register

Name:
CfO_OversampleRelativeCycleID
"Reference cycle" in the AS I/O configuration.

The source of the user interface reference cycle can be configured in this register.

- The input data is referenced at the time of the "reference cycle". The referenced data is then copied to the "oversample input sample register" at the time of "SI frame generation", while taking the "OversampleInputWindow" into account.
- With relative addressing of the output control buffer, the new sample data is copied to an address relative to the output control buffer address current to the "reference cycle".
- The reference cycle is also used to reference the sample cycle, and with it also the output data production and input data acquisition (e.g. to the X2X cycle).

Data type	Value	Information
USINT	2	System timer The value configured in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used as the reference cycle.
	3	Prescaled system timer The "prescaled system timer" is used as sample cycle.
	10	AOAI The sample cycle is referenced with the AOAI interrupt of the X2X cycle.
	14	SOSI The sample cycle is referenced with the SOSI interrupt of the X2X cycle.

4.16.4.11.10.5 "CfO_OversampleConsumeCycleID" register

Name:
CfO_OversampleConsumeCycleID
"Output copy cycle" in the AS I/O configuration.

At the time of the output copy cycle, data is copied from the 4.16.4.11.10.15 "OversampleOutput0NSample" registers into the output control buffer.

When "Output copy cycle = Fast reaction", it is not possible to determine when the data is copied to the output control buffer in either of the two addressing modes. The copy cycles will experience a certain degree of jitter depending on the module load. However, this only affects the moment of the internal copy procedures and therefore the moment of the earliest possible output sample. This will not affect the quality of the output signal. However, "Output copy cycle = Fast reaction" also has a negative effect on the minimum X2X cycle time.

When using the setting "Output copy cycle = X2X cycle optimized", be aware that the sample data cannot start being output immediately at the "Output copy cycle" time due to the internal copy cycle to the output control buffers.

Data type	Value	Information
USINT	10	X2X cycle optimized The output data is copied to the output control buffer with the AOAI interrupt of the X2X cycle.
	15	Fast reaction The output data is copied to the output control buffer immediately after being received.

4.16.4.11.10.6 "CfO_OversampleOutputBits" register

Name:
CfO_OversampleOutputBits
"User interface size" in the AS I/O configuration.

Specifies how many bits are transferred from the 4.16.4.11.10.15 "OversampleOutputONSample" registers to the output control buffers at the time of the "output copy cycle".

Data type	Value	Information
USINT	1 to 64	Output bits

4.16.4.11.10.7 "CfO_OversampleInputBits" register

Name:
CfO_OversampleInputBits
"User interface size" in the AS I/O configuration.

Specifies how many bits are transferred from the input status buffer to the 4.16.4.11.10.18 "OversampleInput0NSample" register during "SI frame generation".

Data type	Value	Information
USINT	1 to 64	Input bits

4.16.4.11.10.8 "CfO_OversampleOutputWindow" register

Name:
CfO_OversampleOutputWindow
"Output control mode" in the AS I/O configuration.

Determines the area in the output control buffer in which data can be written. The window is always offset relative to the current sample position. (a value of 128, for example, means that the 128 bits following the current sample cycle can be written to). An "OutputCopyError" is triggered if an attempt is made to write output sample data to a location outside of this window.
In AS, with the setting "Output control mode = Single", this register is set to 128 bits and with the setting "Output control mode = Continuous" it is set to 255 bits.

Data type	Value	Information
USINT	0 to 255	Output window

4.16.4.11.10.9 "CfO_OversampleInputWindow" register

Name:
CfO_OversampleInputWindow
"Input mode" in the AS I/O configuration.

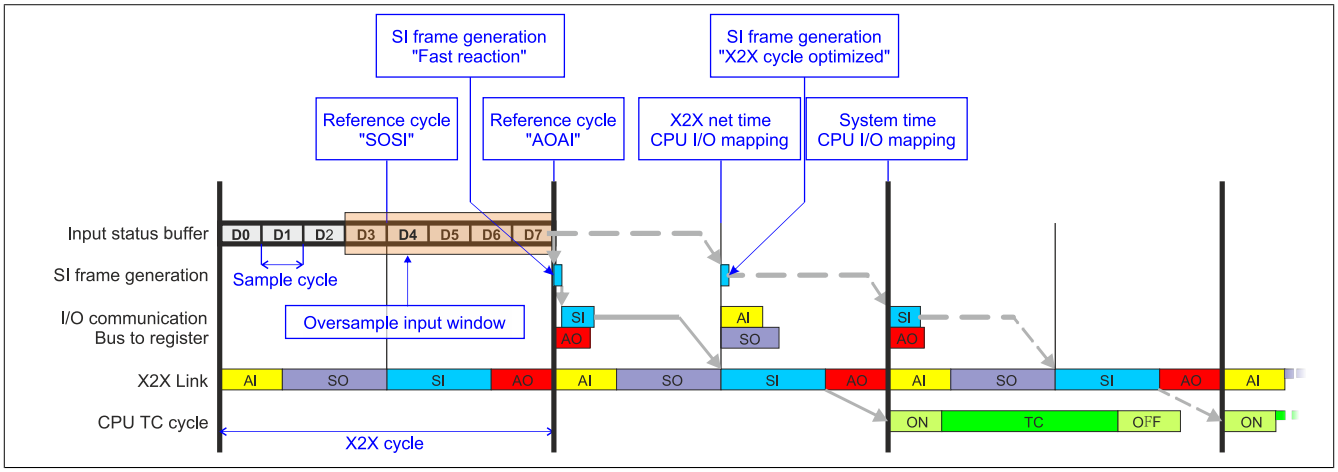
The "OversampleInputWindow" determines when the input data is referenced. It is located chronologically before "SI frame generation". If the reference time ("reference cycle") is within this window, then the referenced data is copied from the input status buffer to the OversampleInput0NSample register. If the time at which the reference occurs is outside the "OversampleInputWindow" then the data that is most recent at the time of "SI frame generation" is copied from the input status buffer to the 4.16.4.11.10.18 "OversampleInput0NSample" register.
This register is limited internally with to the value set in the 4.16.4.11.10.7 "CfO_OversampleInputBits" register.

Information:

As a result, the "OversampleInputTime" and the "OversampleInputCycle" are set either at the reference time or at the time of "SI frame generation".

In Automation Studio, this register is set to 63 when "Input mode = Referenced values" and to 0 when "Input mode = Most recent values".

Data type	Value	Information
USINT	0 to 63	Input window



4.16.4.11.10.10 "CfO_OversampleConfigOutput" register

Name:
CfO_OversampleConfigOutput
"Oversample I/O 01 →Output" to "Oversample I/O 04 →Output" in the AS I/O configuration
"Oversample I/O 01 →Output control" to "Oversample I/O 04 →Output control" in the AS I/O configuration
"Oversample I/O 01 →Output default state" to "Oversample I/O 04 →Output default state" in the AS I/O configuration

This register helps configure the outputs of the individual oversample channels.

The "Output default state" bits determine which level the respective output assumes before oversampling is started. Furthermore, the output is set to the defined "Output default state" in the event of an error.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Number of the physical output channel "Oversample I/O 0x →Output" in the AS I/O configuration	0	Output channel 1
		1	Output channel 2
		2	Output channel 3
4	Output: Clear "Oversample I/O 0x →Output control" in the AS I/O configuration	0	Output cannot be reset by the oversample channel.
		1	Output can be reset by the oversample channel.
5	Output: Set "Oversample I/O 0x →Output control" in the AS I/O configuration	0	Output cannot be set by the oversample channel.
		1	Output can be set by the oversample channel.
6	Output default state: Clear "Oversample I/O 0x →Output default state" in the AS I/O configuration	0	Output not cleared by default
		1	Output cleared by default
7	Output default state: Set "Oversample I/O 0x →Output default state" in the AS I/O configuration	0	Output not set by default
		1	Output set by default

4.16.4.11.10.11 "CfO_OversampleConfigInput" register

Name:
CfO_OversampleConfigInput
"Oversample I/O 01 →input" to "Oversample I/O 04 →input" in the AS I/O configuration

This register determines which physical input channel an oversample I/O input should be linked to.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Number of the physical input channel	0	Input channel 1
		1	Input channel 2
		2	Input channel 3
		3	Reserved
		4	Input channel 4
		5	Input channel 5
4 - 7	Reserved	-	

4.16.4.11.10.12 Oversample register - Configuration

Name:
OversampleEnable
OversampleOutputValidate

This register can be used to configure oversampling and the copy procedure for the output buffer.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	OversampleEnable	0	Disables oversampling (with the next reference cycle)
		1	Enables oversampling (with the next reference cycle)
1	OversampleOutputValidate	0	Disable the copy procedure to the output control buffer.
		1	Enables the copy procedure to the output control buffer. • Used to synchronize the oversampling procedure at startup. • This makes it possible to prevent new data from being transferred to the 4.16.4.11.10.15 "OversampleOutput0NSample" registers in each X2X cycle.
2 - 7	Reserved	-	

4.16.4.11.10.13 "OversampleOutputCycle" register

Name:
OversampleOutputCycle

When absolute addressing of the output control buffer is being used, this register specifies the address from which the new output sample data should be copied to the output control buffer.

Data type	Value	Information
USINT	0 to 255	Address of the output control buffer

4.16.4.11.10.14 "OversampleSampleOffset" register

Name:
OversampleSampleOffset

When relative addressing of the output control buffer is being used, this register serves as the offset for the new output sample data. (Sample address at the time of the "reference cycle" + Offset = address to which the new output sample data is copied in the output control buffer).

Data type	Value	Information
USINT	0 to 255	Offset of output sample data

4.16.4.11.10.15 "OversampleOutputSample" register

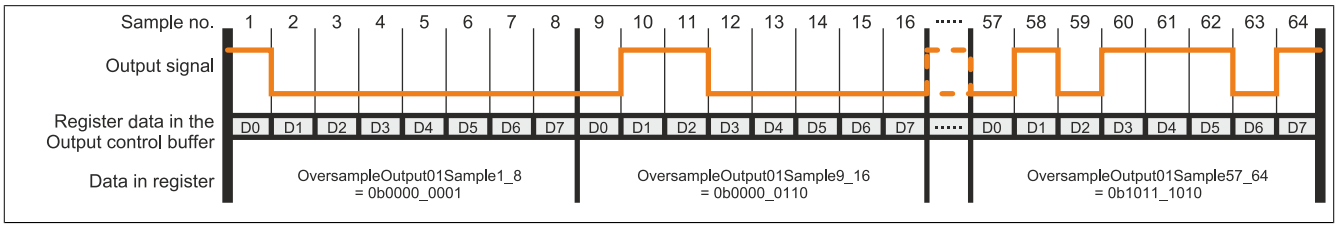
Name:
OversampleOutput01Sample1_8 to OversampleOutput04Sample1_8
OversampleOutput01Sample9_16 to OversampleOutput04Sample9_16
OversampleOutput01Sample17_24 to OversampleOutput04Sample17_24
OversampleOutput01Sample25_32 to OversampleOutput04Sample25_32
OversampleOutput01Sample33_40 to OversampleOutput04Sample33_40
OversampleOutput01Sample41_48 to OversampleOutput04Sample41_48
OversampleOutput01Sample49_56 to OversampleOutput04Sample49_56
OversampleOutput01Sample57_64 to OversampleOutput04Sample57_64

Contains the oversample output sample data. Up to 64 samples (8 bytes) for each oversample I/O channel can be synchronously transferred with a X2X cycle. This data is copied to the specified address (absolute or relative) in the output control buffer during the "output copy cycle". 1 bit of this data is then output during each "sample cycle" to the physical output that is assigned to the oversample I/O channel.
Bit 0 of "OversampleOutputSample8_1" is copied to the output control buffer first, meaning that it is the first bit that is output. "OversampleOutputSample64_57" bit 7 is the last bit to be output.

Data type	Value	Information
USINT	0 to 255	Output sample data

Example

Assignment of "OversampleOutputSample" register data to output signal



4.16.4.11.10.16 "OversampleInputTime" register

Name:
OversampleInputTime

This register contains the 2 low-order bytes of the X2X net time from the moment at which the oversample input data was referenced. This provides an easy way to accurately calculate the time of each individual input sample.

Data type	Value	Information
INT	-32,768 to 32,767	X2X net time of the input data

4.16.4.11.10.17 "OversampleInputCycle" register

Name:
OversampleInputCycle

This register provides the width of the input status buffer address for the input sample data.
Furthermore, the value in this register can be used for referencing an absolute addressing of the output control buffer.

Data type	Value	Information
USINT	0 to 255	Input status buffer address

4.16.4.11.10.18 "OversampleInputSample" register

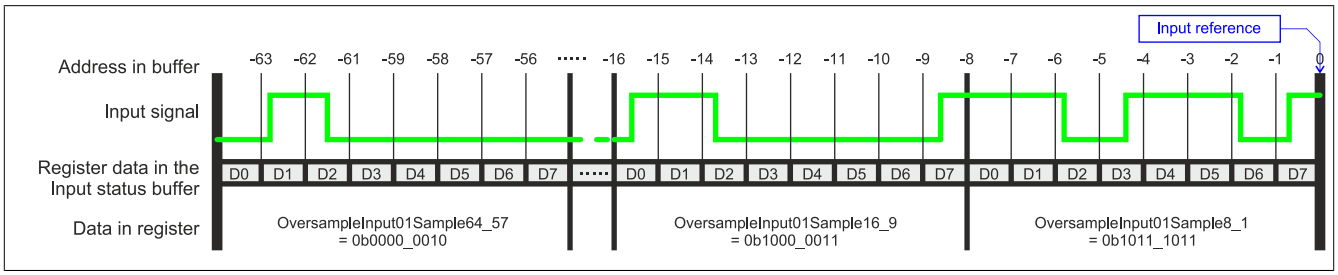
Name:
OversampleInput01Sample8_1 to OversampleInput04Sample8_1
OversampleInput01Sample16_9 to OversampleInput04Sample16_9
OversampleInput01Sample24_17 to OversampleInput04Sample24_17
OversampleInput01Sample32_25 to OversampleInput04Sample32_25
OversampleInput01Sample40_33 to OversampleInput04Sample40_33
OversampleInput01Sample48_41 to OversampleInput04Sample48_41
OversampleInput01Sample56_49 to OversampleInput04Sample56_49
OversampleInput01Sample64_57 to OversampleInput04Sample64_57

The data of the four oversample input status buffers are copied to this register at the time of "SI frame generation". A maximum of 64 samples (8 bytes) per oversample I/O channel can be synchronously retrieved from the oversample input status buffer with each X2X cycle.
The most recent input sample bit is stored in "OversampleInputSample8_1" bit 7. The oldest input sample is stored in "OversampleInputSample64_57" bit 0.

Data type	Value	Information
USINT	0 to 255	Input sample data

Example

Input signal and resulting data in "OversampleInputSample"



4.16.4.11.11 Edge detection

The module's edge detection function identifies edges with µs precision. The concept is based on a maximum of 4 units. A master and a slave edge can be configured for each unit.

At each master edge, the net time of the master edge and the net time of a previous slave edge (if present) are logged. A "master counter" and a "slave counter" can always be used to determine how many edges have been detected since the last X2X cycle.

4.16.4.11.11.1 "CfO_EdgeDetectPollCycleID" register

Name:
CfO_EdgeDetectPollCycleID
"Polling cycle" in the AS I/O configuration.

The source of the polling cycle can be configured in this register.

Information:

The polling cycle must be less than or equal to 255 µs. Setting the cycle > 255 µs causes an EdgeDetectError.

Data type	Value	Information
USINT	2	System timer The time set in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used for the polling cycle.
	3	Prescaled system timer The time set in the 4.16.4.11.7.3 "CfO_SystemCyclePrescaler" register is used for the polling cycle.

4.16.4.11.11.2 "CfO_EdgeDetectEventEnable" register

Name:
CfO_EdgeDetectEventEnable
"Edge detection mode" in the AS I/O configuration.

The bits in this register determine at which edges on the individual input channels an interrupt should be triggered for the edge detection.

In the AS IO configuration, this register is initialized with 0x00000000 when "Edge detection mode = polling" and with 0xFFFFFFFF when "Edge detection mode = event triggered".

In "event triggered" mode, the net time of each edge is recorded immediately at interrupt. However, an extremely large amount of interrupts within a short amount of time can prevent the module from being able to process any other operations in time!

In "polling" mode, only the net time of the first edge that occurs within a polling cycle is recorded. This ensures that the module is not overloaded by too many edges.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Physical input 1	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
1	Physical input 2	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
2	Physical input 3	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
3	Reserved	-	
4	Physical input 4	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
5	Physical input 5	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
6 - 15	Reserved	-	
16	Physical input 1	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
17	Physical input 2	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
18	Physical input 3	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
19	Reserved	-	
20	Physical input 4	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
21	Physical input 5	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
22 - 31	Reserved	-	

4.16.4.11.11.3 "CfO_EdgeDetectUnitMode" register

Name:
CfO_EdgeDetectUnit01Mode to CfO_EdgeDetectUnit04Mode
"Time base" in the AS I/O configuration.
"Slave edge" in the AS I/O configuration.
"Master edge" in the AS I/O configuration.

When using a "time base" with 1/8 µs resolution, keep in mind that the timestamps produced also have a resolution of exactly 1/8 µs. The respective conversions must be made for calculating in combination with the CPU system time or X2X net time.

Furthermore, synchronization jitter also plays a role when using the setting "time base = net time resolution 1/8 µs" (see: 4.16.4.11.4.3 "Synchronization jitter"). This means that exactly identical input edges can cause slight differences in the results. If a 100% exact 1/8 µs resolution is required, then the "local resolution 1/8 µs" must be used.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	"Time base" in the AS I/O configuration.	0	Local time 1/8 µs (AS: Local resolution 1/8 µs)
		1	Local time 1 µs (AS: Local resolution 1 µs)
		2	Net time 1/8 µs (AS: Net time resolution 1/8 µs)
		3	Net time 1 µs (AS: Net time resolution 1 µs)
2 - 5	Reserved	-	
6	"Slave edge" in the AS I/O configuration.	0	Disabled
		1	Enabled
7	"Master edge" in the AS I/O configuration.	0	Disabled
		1	Enabled

4.16.4.11.11.4 "CfO_EdgeDetectUnitLeading" register

Name:
CfO_EdgeDetectUnit01Leading to CfO_EdgeDetectUnit04Leading
"Slave leading" in the AS I/O configuration.

When a slave edge occurs, the current net time is always saved within the module. A FIFO is provided inside the module which always stores the last 256 slave stamps (even when a master edge occurs).

This value determines from which position the slave time should be retrieved from the FIFO when a master edge occurs. This can be used to measure average periodic signals over multiple cycles.

Data type	Value	Information
USINT	0 to 255	Position in the slave edge FIFO

4.16.4.11.11.5 "CfO_EdgeDetectUnitMaster" register

Name:
CfO_EdgeDetectUnit01Master to CfO_EdgeDetectUnit01Master
"Master edge" in the AS I/O configuration.

Determines the source of the master edge for the respective "Edge detection unit".

Data type	Value	Information
USINT	0	Rising edge on physical input 1
	1	Rising edge on physical input 2
	2	Rising edge on physical input 3
	4	Rising edge on physical input 4
	5	Rising edge on physical input 5
	16	Falling edge on physical input 1
	17	Falling edge on physical input 2
	18	Falling edge on physical input 3
	20	Falling edge on physical input 4
	21	Falling edge on physical input 5

4.16.4.11.11.6 "CfO_EdgeDetectUnitSlave" register

Name:
CfO_EdgeDetectUnit01Slave to CfO_EdgeDetectUnit04Slave
"Slave edge" in the AS I/O configuration.

Determines the source of the slave edge for the respective "Edge detection unit".

Data type	Value	Information
USINT	0	Rising edge on physical input 1
	1	Rising edge on physical input 2
	2	Rising edge on physical input 3
	4	Rising edge on physical input 4
	5	Rising edge on physical input 5
	16	Falling edge on physical input 1
	17	Falling edge on physical input 2
	18	Falling edge on physical input 3
	20	Falling edge on physical input 4
	21	Falling edge on physical input 5

4.16.4.11.11.7 "EdgeDetectMastercount" register

Name:
EdgeDetect01Mastercount to EdgeDetect04Mastercount

The reference pulses of the detected master edges are counted in this register.

Data type	Value	Information
SINT	-128 to 127	Number of detected master edges (8-bit)
INT	-32,768 to 32,767	Number of detected master edges (16-bit)

4.16.4.11.11.8 "EdgeDetectSlavecount" register

Name:
EdgeDetect01Slavecount to EdgeDetect04Slavecount

Counts the number of detected slave edges consecutively. The contents of this register are only updated when a master edge occurs. These counters can detect if multiple slave edges occur before a master edge.

Data type	Value	Information
SINT	-128 to 127	Number of detected slave edges (8-bit)
INT	-32,768 to 32,767	Number of detected slave edges (16-bit)

4.16.4.11.11.9 "EdgeDetectDifference" register

Name:
EdgeDetect01Difference to EdgeDetect04Difference

Contains the time difference between a master edge and the last slave edge addressed via "Slave leading".

Data type	Value	Information
INT	-32,768 to 32,767	Time difference between master/slave edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Time difference between master/slave edge (32-bit)

4.16.4.11.11.10 "EdgeDetectMastertime" register

Name:
EdgeDetect01Mastertime to EdgeDetect04Mastertime

The exact net time is copied in this register when a master edge occurs.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of master edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of master edge (32-bit)

4.16.4.11.11.11 "EdgeDetectSlavetime" register

Name:
EdgeDetect01Slavetime to EdgeDetect04Slavetime

When a master edge occurs, the exact net time of any slave edge that may have occurred prior to the master edge and addressed by "Slave leading" is copied in this register. If multiple slave edges occur before a master edge, then only the net time of the last edge that was not ignored by "Slave leading" is stored. The 4.16.4.11.11.8 "EdgeDetectSlavecount" register can be used to detect multiple edges.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the slave edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the slave edge (32-bit)

4.16.4.11.12 Movement functions

Encoder emulation can be used to generate up/down counters (direction/frequency) and ABR encoder signals. The movement function can be operated in 2 different modes:

- Position control mode
- Speed control mode

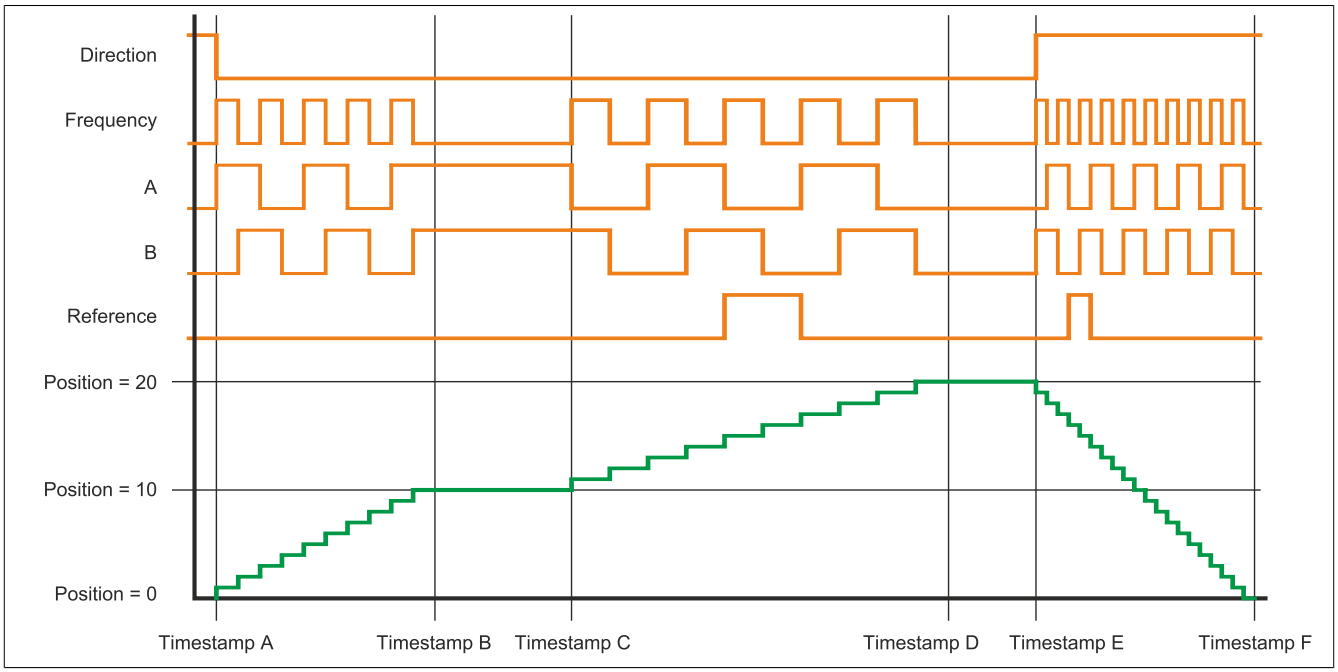
4.16.4.11.12.1 Position control mode

Each time the 4.16.4.11.12.18 "MovTargetTime" register changes, a new position setpoint is transferred from the 4.16.4.11.12.19 "MovPosition" register to the FIFO. The time/position data in the FIFO is then processed in such a manner that the positions are always reached at the time of the respective timestamps. This means that the module internally ensures that the positions are reached by the defined timestamps (number/frequency of the pulses is calculated automatically). The timestamps can be based on the X2X net time, the CPU's system time or the 4.16.4.11.12.21 "MovCurrentTime" register. Timestamps that are set in a manner that does not allow the required position change to be reached before the timestamp (output frequency of the pulse would exceed 4.16.4.11.12.4 "CfO_SpeedLimit") cause a MovMaxFrequencyViolation error.

Selected values for the example "Timing of movement":

Timestamp A = MovTimeValid + 40,000	Position for timestamp A = 0
Timestamp B = Timestamp A + 40.000	Position for timestamp B = 10
Timestamp C = Timestamp B + 25.000	Position for timestamp C = 10
Timestamp D = Timestamp C + 70,000	Position for timestamp D = 20
Timestamp E = Timestamp D + 15,000	Position for timestamp E = 20
Timestamp F = Timestamp E + 40,000	Position for timestamp F = 0

Configuration: Reference pulse = Start and end position, Start position = 15, End position = 17



4.16.4.11.12.2 Speed control mode

In speed control mode, the application only specifies the speed setpoint. The module returns the current position in the 4.16.4.11.12.22 "MovPosition (32-bit)" register.

The internal timing is designed so that the value 16,777,216 (0x01000000) in the 4.16.4.11.12.20 "MovSpeed" register results in exactly one increment per "control period".

This creates the following relationship for 32-bit speed setpoints ("Data format of speed values = 32-bit):

$$MovSpeed = vOut * 2^{resol} * period$$

Unlike other registers, the 2 higher-value bytes of "MovSpeed (32-bit)" are set when the "MovSpeed (32-bit)" register is written. This creates the following relationship for the direct calculation with "MovSpeed (16-bit)"

$$MovSpeed = \frac{vOut * 2^{resol} * period}{2^{16}}$$

Variable	Description	Unit
MovSpeed	Value for "MovSpeed" register (16 or 32-bit)	
vOut	Desired output speed Each edge represents one increment (rising or falling).	Inc/s
resol	Value configured for the 4.16.4.11.12.13 "CfO_ResolSpeed" register	Bits
period	Value configured for the 4.16.4.11.12.11 "CfO_SpeedCycleTime_32Bit" register **Information:** **Must be set in µs in Automation Studio. The calculation is performed in s, however.**	s

4.16.4.11.12.3 "FifoSize" register

Name:
FifoSize
"Number of Fifo entries" in the AS I/O configuration.

Determines the size of the FIFO for MovTargetTime and MovTargetPosition. One timestamp and one position that should be reached by the timestamp can be transferred to the FIFO per X2X cycle.

Data type	Value	Information
USINT	0	FIFO disabled
	3	8 entries (2^3)
	4	16 entries (2^4)
	5	32 entries (2^5)
	6	64 entries (2^6)
	7	128 entries (2^7)
	8	256 entries (2^8)

4.16.4.11.12.4 "CfO_SpeedLimit" register

Name:
CfO_SpeedLimit
"Max. movement frequency" in the AS I/O configuration.

Configures the maximum permitted output frequency and the maximum internal computing frequency. The higher internal computing frequencies of 2, 4, 8, 16, 32 and 64 MHz can only be achieved by configuring n bits as decimal places (see 4.16.4.11.12.12 "CfO_ResolPosition" register).

Data type	Value	Max. increment frequency	Max. frequency for frequency output channel	Max. frequency for A/B output channel
USINT	253	64 MHz	500 kHz	250 kHz
	254	32 MHz		
	255	16 MHz		
	0	8 MHz		
	1	4 MHz		
	2	2 MHz		
	3	1 MHz (default)		
	4	500 kHz	250 kHz	125 kHz
	5	250 kHz (default)	125 kHz	625 kHz
	6	125 kHz	625 kHz	3125 kHz

Information:

In Position control mode, the increment frequencies 16, 32 and 64 MHz are not permitted to be used when a 29-bit timestamp is set (see 4.16.4.11.12.7 "CfO_TimeStampRange" register) due to an internal range violation.

4.16.4.11.12.5 "CfO_Mode" register

Name:
CfO_Mode

This register can be used to configure the mode of the movement functions.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Must be enabled when working without timestamps. Enabled in AS if: • Movement = "speed control" • Movement = "position control and "data format / mode of preset time = local time"	0	Disabled
		1	Enabled
1	If this function is enabled, then a new positioning movement is triggered as soon as the value changes in the 4.16.4.11.12.19 "MovPosition" register. Enabled in AS if: • Movement = "position control and "data format / mode of preset time = local time"	0	No position control (speed control)
		1	Position control enabled (position control)
2	Reference mode "Configuration reference pulse 1" in the AS I/O configuration.	0	Start/end position
		1	Start position and span
3 - 7	Reserved	-	

4.16.4.11.12.6 "CfO_FormatAdjust" register

Name:
CfO_FormatAdjust

This register determines the number of absolute bits that can be output on the signal output (With a direction/frequency signal, the bit with the lowest value can be output directly on the frequency output. With an AB signal, 2 bits are possible.)

Data type	Value	Information
USINT	1 to 2	Number of absolute bits (AS default = 1)

4.16.4.11.12.7 "CfO_TimeStampRange" register

Name:
CfO_TimeStampRange
"Data format/mode of target time" in the AS I/O configuration.

The width of the transferred timestamp data in the module is configured in this register.

Information:

Because the module uses an internal resolution of 1/8 µs, timestamp data is processed internally at a maximum width of 29 bits.

Data type	Value	Information
SINT	16	16-bit timestamp ("16-bit" selected in the AS I/O configuration)
	24	24-bit timestamp ("local time" or "speed control" movement selected in the AS I/O configuration)
	29	29-bit timestamp ("29-bit" selected in the AS I/O configuration)

4.16.4.11.12.8 "CfO_PositionsRange" register

Name:
CfO_PositionsRange
"Target position range" in the AS I/O configuration.

The number of bits for position control are configured in this register. The "PositionRange" must be reduced if, for example, the movement function should follow the absolute value of a 12-bit SSI encoder. In this case, the bit width of the movement position also has to be limited to the number of bits of the encoder, or else the movement position would not also overrun if the encoder were to overrun. In this case, the module would attempt (in the opposite direction) to reach the position of an encoder that had just overrun.

Example

The 12-bit SSI encoder overruns from 2047 to -2048. The module would generate 4096 negative increments if more than 12 bits were defined for "CfO_PositionRange" in order to reach position -2048 from the position 2047.

Information:

If the 16-bit value of the 4.16.4.11.12.22 "MovPosition" register is used, then the bit width of the position must also be limited to ≤16 bits or else this would also result in incorrect overrun behavior.

Data type	Value	Information
SINT	8 to 32	Number of bits for position control

4.16.4.11.12.9 "CfO_TimeStampDelay" register

Name:
CfO_TimeStampDelay

All timestamps are delayed by the value defined in this register.

Data type	Value	Information
DINT	0 to 1000000	Timestamp delay in µs

4.16.4.11.12.10 "CfO_ReferenceRange" register

Name:
CfO_ReferenceRange
"Reference range" in the AS I/O configuration.

This register determines the number of bits that can be used for the reference position comparison. This makes it possible to generate a reference pulse every 2^n increments.

Information:

The number of bits set in this register must not be higher than the number of bits set for MovReferenceStart and MovReferenceStopMargin.

Data type	Value	Information
SINT	4 to 32	Number of bits for position comparison

4.16.4.11.12.11 "CfO_SpeedCycleTime_32Bit" register

Name:
CfO_SpeedCycleTime_32Bit
"Control period" in the AS I/O configuration.

The control period for "speed control" mode can be set in this register in steps of 1/8 µs.

Information:

The value defined in the AS I/O configuration under "Control period" is automatically multiplied by 8 and then used as CfO_SpeedCycleTime_32bit.

Data type	Value	Information
UDINT	400 to 40000	Control period for "speed control" mode

4.16.4.11.12.12 "CfO_ResolPosition" register

Name:
CfO_ResolPosition
"Position resolution" in the AS I/O configuration.

This register contains the number of bits as decimal place for jitter reduction. Internally, the module adds 2^n (n = number of decimal places) to the frequency, which results in edge switching times with a higher resolution. The output switching frequency is not increased from a hardware perspective, but the edge timing is more precise.

Data type	Value	Information
SINT	0	Default, no decimal places
	1 to 14	Selection of bits as decimal places

Information:

Keep in mind that each configured decimal place also limits the maximum number range by that number of bits.

For example: 0 decimal places →maximum position range = 29 bits

3 decimal places →maximum position range = 26 bits

Also keep in mind that the CfO_SpeedLimit parameter must be adjusted for these higher computing frequencies based on the number of configured decimal places.

4.16.4.11.12.13 "CfO_ResolSpeed" register

Name:
CfO_ResolSpeed
"Speed resolution" in the AS I/O configuration.

This register contains the number of bits as decimal place for jitter reduction of the speed value. Internally, the module adds 2^n (n = number of decimal places) to the frequency, which results in edge speed values with a higher resolution.

Due to the bit limitation, a 16 or 32-bit speed value is set in the AS I/O configuration. Since the internal calculation is always based on 32-bit, when configured to 16-bit an offset of 16 must always be added to the desired number of decimal places.

Data type	Value	Information
SINT	0 to 31	Selection of bits as decimal places
	24	Standard

Information:

Keep in mind that each configured decimal place also limits the maximum number range by that number of bits.

4.16.4.11.12.14 "CfO_ReferenceStart / MovReferenceStart" register

Name:
CfO_Reference0Start
MovReferenceStart
"Start position" in the AS I/O configuration.

The start position for the reference pulse is shown in these registers.

In the positive direction, the output (R) is set when the start position is reached. In negative direction, the output is reset as soon as the value falls below the start position value.

Data type	Value	Information
INT	-32,768 to 32,767	Start position (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Start position (32-bit)

4.16.4.11.12.15 "CfO_ReferenceStopMargin / MovReferenceStopMargin" register

Name:
CfO_Reference0StopMargin
MovReferenceStopMargin
"End position or margin" in the AS I/O configuration.

The end position or the margin in which the reference pulse is output is configured in these registers.

If "Reference mode = Start/end position" is used in the 4.16.4.11.12.5 "CfO_Mode" register, then the output (R) is reset when the end position is reached in the positive direction. In the negative direction, the output is set as soon as the value falls below the end position value.

When "Reference mode = Start position and span", the content of this register is added to the start position and the resulting sum is used as the end position.

Data type	Value	Information
INT	-32,768 to 32,767	End position (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	End position (32-bit)

4.16.4.11.12.16 "CfO_AccelDataInit / MovAcceleration" register

Name:
CfO_AccelDataInit
MovAcceleration
"Acceleration value" in the AS I/O configuration.

This register shows the acceleration value in increments per control period².

- 32-bit: 16777216 (0x01000000) corresponds to 1 increment per control period²
- 16-bit: 256 (0x0100) corresponds to 1 increment per control period²

Data type	Value	Information
UINT	0 to 65,535	Acceleration value (16-bit)
UDINT	0 to 4,294,967,296	Acceleration value (32-bit)

4.16.4.11.12.17 "MovementControl" register

Name:
MovPosEnable
MovSpeedEnable

This register can be used to enable position and speed control.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	MovPosEnable	0	Position control disabled
		1	Position control enabled
1	MovSpeedEnable	0	Speed control disabled
		1	Speed control enabled
2 - 6	Reserved	-	
7	Movement reset (immediate stop)	0	Passive reset
		1	Active reset

4.16.4.11.12.18 "MovTargetTime" register

Name:
MovTargetTime

Timestamp data is shown in this register.Each time this register changes, the new position data (MovTargetPosition) and timestamp data are transferred to the FIFO. When "MovSpeedEnable = True", the module calculates the output speed (frequency) so that the "MovTargetPosition" is reached at "MovTargetTime".

Data type	Value	Information
INT	-32,768 to 32,767	Timestamp (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Timestamp (32-bit)

Information:

Only 29 bits of this register are processed internally.

4.16.4.11.12.19 "MovTargetPosition" register

Name:
MovTargetPosition

Position data is shown in this register.

Data type	Value	Information
INT	-32,768 to 32,767	Position (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Position (32-bit)

4.16.4.11.12.20 "MovSpeed" register

Name:
MovSpeed

This register shows the speed setpoint for "speed control" mode in increments per control period.

- 32-bit: 16,777,216 (0x01000000) corresponds to 1 increment per control period
- 16-bit: 256 (0x0100) corresponds to 1 increment per control period

Data type	Value	Information
INT	-32,768 to 32,767	Speed setpoint (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Speed setpoint (32-bit)

4.16.4.11.12.21 "MovTimeValid" register

Name:
MovTimeValid

This register displays the net time of the current position.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the current position (16-bit).
DINT	-2,147,483,648 to 2,147,483,647	Net time of the current position (32-bit)

4.16.4.11.12.22 "MovPosition" register

Name:
MovPosition

This register shows the current position.

Data type	Value	Information
INT	-32,768 to 32,767	Current position (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Current position (32-bit)

4.16.4.11.13 Synchronous serial interface (SSI)

The synchronous serial interface makes it possible to receive data from SSI absolute encoders.

Two lines are needed for data exchange:

SSI clock:	Generated by the module on output 2 (if configured).
SSI data:	A data bit is transferred from the encoder to the module with each clock pulse (input 1 can be used as the SSI input).

4.16.4.11.13.1 SSI transfer process

When the first edge occurs on the SSI clock, a monoflop is triggered in the encoder and the current parallel pending value is latched to the offset register (the low level of the monoflop prevents other values from being added to the offset register during data transfer).

The highest value bit is then transferred to the module when the next edge occurs.

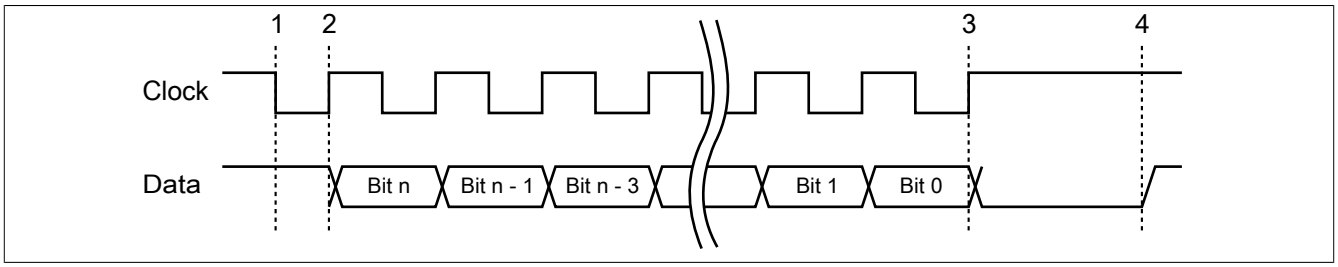
With each subsequent cycle, the next lowest bit is transferred. The cycles re-trigger the monoflop constantly so that its output prevents new data from being accepted.

The sequence of cycles stops once the number of data bits defined in the 4.16.4.11.13.4 "CfO_DataBits" register has been received.

The monoflop is no longer triggered. After a certain amount of time has passed (depending on the encoder), the monoflop's output re-assumes the output level, thereby enabling parallel data to be accepted once again in the encoder's offset register.

When the "Monoflop check" is run, the data line is queried for the configured level before a new transfer is started. This makes it possible to ensure that the monoflop really has reset before a new transfer is started.

Transfer to synchronous serial interface



Measurement value processing

1 Starting bit ... Stores the measurement value
2 Output of first data bit
3 All data bits are transferred, monostable multivibrator time starts counting down.
4 Monostable multivibrator returns to its initial state. A new transfer can be started.

4.16.4.11.13.2 "CfO_CycleSelect" register

Name:
CfO_CycleSelect
"Update cycle" in the AS I/O configuration.

SSI transfer is started at the update cycle. The clock sequence is generated on the SSI clock output. The first edge of the clock signal triggers the monoflop in the encoder and latches the current position. At the same time, the current net time is also recorded in the 4.16.4.11.13.6 "SSITimeValid" register. As soon as all bits have been transferred via the SSI, the position is passed on with the next "SIframeGenCycle" via the X2X Link. A SSICycleTimeViolation error is reported if the SSI transfer is not completed within the SSI update cycle (e.g. system timer as update cycle). The SSI transfer is still fully completed and then started again with the next update cycle.

Data type	Value	Information
USINT	2	System timer
	3	Prescaled system timer
	10	AOAI
	14	SOSI

4.16.4.11.13.3 "CfO_PhysicalMode" register

Name:
CfO_PhysicalMode
"Parity bit" in the AS I/O configuration
"Monoflop check" in the AS I/O configuration
"Data format" in the AS I/O configuration
"Clock frequency" in the AS I/O configuration

The SSI interface is configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	"Parity bit" in the AS I/O configuration.[1)]	00	Disabled
		01	Even parity
		10	Uneven parity
		11	Ignored (the parity bit is transferred, but not evaluated).
2 - 3	"Monoflop check" in the AS I/O configuration.[2)]	00	Disabled
		01	Low level (data signal is checked for low level after the monoflop has reset).
		10	High level (data signal is checked for high level after the monoflop has reset).
		11	Ignored (the necessary cycle is triggered, but not evaluated).
4	"Data format" in the AS I/O configuration.	0	Encoder with binary output
		1	Encoder with Gray Code. The module converts the position data into binary format.
5	Reserved	-	
6 - 7	"Clock frequency" in the AS I/O configuration.	00	1 MHz
		01	500 kHz
		10	250 kHz
		11	125 kHz

1) If the parity bit does not match, then a SSIParityError is generated and the position data is not accepted in the "SSIPosition" register.
2) A new SSI transfer is not started until the data signal has assumed the level defined for the "monoflop check" after the transfer. This then triggers the error SSICycleTimeViolation.

4.16.4.11.13.4 "CfO_DataBits" register

Name:
CfO_DataBits
"Valid SSI bit length" in the AS I/O configuration.

Determines the number of valid data bits to be transferred via the SSI. The valid data bits are used for the SSI-Position.

Data type	Value	Information
USINT	1 to 32	Number of valid data bits

4.16.4.11.13.5 "CfO_NullBits" register

Name:
CfO_NullBits
"Leading zero bits" in the AS I/O configuration.

This register can be used to configure the number of leading zero bits. The leading zero bits can be required before the valid data bits.

Data type	Value	Information
USINT	0 to 31	Number of leading zero bits

4.16.4.11.13.6 "SSITimeValid" register

Name:
SSITimeValid

This register displays the net time of the current position.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the current position (16-bit).
DINT	-2,147,483,648 to 2,147,483,647	Net time of the current position (32-bit)

4.16.4.11.13.7 "SSITimeChanged" register

Name:
SSITimeChanged

The net time of the last position change is shown in this register.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the last position change (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the last position change (32-bit)

4.16.4.11.13.8 "SSIPosition" register

Name:
SSIPosition

This register shows the current position sent via the SSI interface.

Data type	Value	Information
INT	-32,768 to 32,767	Current position (16-bit)
UDINT	0 to 4,294,967,295	Current position (32-bit)
DINT	-2,147,483,648 to 2,147,483,647	

4.16.4.11.14 Counter

The universal counter pair can be used in 3 different modes. Signals up to 600 kHz, depending on the system timer, are reliably measured. Up to 4 latch inputs can be configured in all modes. Enabled latch inputs are negated if necessary and connected with a logical AND operation for a latch condition. If the latch condition is met, the current counter value is stored in a separate register.

Inputs

The physical inputs have fixed assignments based on the respective mode.

Mode	Input 1	Input 2	Input 3	Input 4
Edge counters	Counter input for counter 1 Latch input 1	Counter input for counter 2 Latch input 2	- Latch input 3	- Latch input 4
Up/down counter	Counting direction Latch input 1	Counter frequency Latch input 2	- Latch input 3	- Latch input 4
Incremental encoder	A Latch input 1	B Latch input 2	- Latch input 3	- Latch input 4

Latch function

As latch inputs, inputs 1 to 4 can each be polled to determine if they have a high or low level.

In "Latch mode = continuous", the counters are latched once as soon as "LatchEnable = TRUE" and the configured latch condition is met. If the latch condition is met again, then the counter value is also latched again. (i.e. One latch event is triggered with each rising edge on the output of the AND operation of all latch inputs).

In "Latch mode = single", the counters are latched once as soon as "LatchEnable = TRUE" and the configured latch condition is met. If the latch condition is met again, then the counter value is not automatically copied again. Another latch event can only be processed after "LatchEnable = False" and then "LatchEnable = True" again.

4.16.4.11.14.1 "CfO_CounterCycleSelect" register

Name:
CfO_CounterCycleSelect
"Update cycle" in the AS I/O configuration.

The update cycle for the counter values is configured in this register.

Information:

The maximum counting frequency depends on the cycle. The module can process a maximum of 200 increments (edges) within a counter cycle.

Data type	Value	Information
USINT	2	System timer
	3	Prescaled system timer
	10	AOAI time of X2X cycle
	14	SOSI time of X2X cycle

4.16.4.11.14.2 "CfO_CounterMode" register

Name:
CfO_CounterMode
"Counter mode" in the AS I/O configuration.

The counter mode is configured in this register.

Data type	Value	Information
USINT	0	Edge counters In this mode, the two counters are used as edge counters. The counter input of counter 1 is linked permanently to input 1 and the counter input of the second counter is linked permanently to input 2. Both rising as well as falling edges are counted.
	2	Up/down counter The up/down counter works according to the direction/frequency principle. Input 1 determines the counting direction (LOW = positive, HIGH = negative), input 2 serves as the counting frequency input. Both rising as well as falling edges on the counting frequency input are counted.
	3	Incremental encoder (AB counter) When configured as an AB counter, input 1 serves as the A channel and input 2 as the B channel. All edges are evaluated (4x evaluation).

4.16.4.11.14.3 "CfO_LatchMode" register

Name:
CfO_LatchMode
"Latch mode" in the AS I/O configuration.

The latch mode is configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	LatchMode	0	Single shot
		1	Continuous
1 - 7	Reserved	-	

4.16.4.11.14.4 "CfO_LatchComparator" register

Name:
CfO_LatchComparator
"Latch level channel 01" to "Latch level channel 04" in the AS I/O configuration.

The latch comparators for the counter inputs are configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparison level for latch comparator on input 1	0	Low
		1	High
...		...	
3	Comparison level for latch comparator on input 4	0	Low
		1	High
4	Enable latch comparator on input 1	0	Disabled
		1	Enabled
...		...	
7	Enable latch comparator on input 4	0	Disabled
		1	Enabled

4.16.4.11.14.5 "CounterControl" register

Name:
CounterReset
LatchEnable

This register can be used to clear counter values or enable the latch.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	CounterReset	0	No action
		1	Delete counter
1	LatchEnable	0	Disabled
		1	Enabled
2 - 7	Reserved	-	

4.16.4.11.14.6 "LatchCount" register

Name:
LatchCount

Latch events are counted in this register. This counter can be used to detect whether a new value has been latched.

Data type	Value	Information
SINT	-128 to 127	Latch counter

4.16.4.11.14.7 "CounterTimeValid" register

Name:
CounterTimeValid

This register displays the X2X net time of the current counter value.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the current counter value (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the current counter value (32-bit)

4.16.4.11.14.8 "CounterTimeChanged" register

Name:
Counter01TimeChanged to Counter02TimeChanged

The net time of the last change to the respective counter is shown in this register.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the last change to the respective counter (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the last change to the respective counter (32-bit)

4.16.4.11.14.9 "CounterValue" register

Name:
CounterValue01 to CounterValue02

This register shows the current value of the respective counter.

Data type	Value	Information
INT	-32,768 to 32,767	Value of the respective counter (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Value of the respective counter (32-bit)

4.16.4.11.14.10 "CounterLatch" register

Name:
CounterLatch01 to CounterLatch02

As soon as the latch conditions defined in the 4.16.4.11.14.4 "CfO_LatchComparator" register have been met, the contents of the respective CounterValue register are copied to this register.

Data type	Value	Information
INT	-32,768 to 32,767	Latch counter (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Latch counter (32-bit)

4.16.4.11.14.11 "CounterRel" register

Name:
CounterRel01 to CounterRel02

The value of the respective counter, relative to the last latch of the respective counter is calculated in this register.

Data type	Value	Information
INT	-32,768 to 32,767	Counter value relative to the last latch (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Counter value relative to the last latch (32-bit)

4.16.4.11.15 Minimum X2X cycle time

The minimum X2X cycle time is strongly dependent on the configured functions and the resulting load on the module. In general, a "Fast reaction" setting and a very short system cycle (50 µs) have a negative influence on the minimum X2X cycle time. This can lead to errors when the X2X cycle time is short.

4.16.5 X20DS1319

4.16.5.1 General information

The module being used is a multifunctional digital signal processor module. It's flexibility allows it to be implemented for a wide range of tasks involving the creation or processing of digital signals. For example, two main uses include encoder emulation and controlling stepper output stages with pulse and direction signals. When used for encoder emulation, frequency inverters or servo axes with the speed follow function can follow a real or virtual master axis.

A further important feature is the timestamp function, which is integrated in the module. It can be used, for example, to create ramp curves for the counter in the encoder emulation virtually independent of bus cycle times. It's only necessary to enter the target counter value and the time at which it should be reached. The module generates the appropriate counter values, precisely in microsecond resolution and independently of the bus clock.

- 4 digital input channels
- 4 digital channels, configurable as inputs or outputs
- 1 universal counter pair (2 event counters, AB counter or up/down counter)
- Linear movement generator (A/B; direction/frequency) with up to 2 reference pulses
- SSI absolute encoder

4.16.5.2 Order data

Model number	Short description	Figure
	Digital signal processing and preparation	
X20DS1319	X20 multifunctional digital signal processor, 4 digital input channels, 4 digital channels configurable as inputs or outputs, 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 2 reference pulses, SSI absolute encoder, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 359: X20DS1319 - Order data

4.16.5.3 Technical data

Product ID	X20DS1319
Short description	
I/O module	4 digital input channels, 4 digital channels configurable as inputs or outputs, 1 universal counter pair (2 event counters, AB counter or up/down counter), linear movement generator (A/B; direction/frequency) with up to two reference pulses, SSI absolute encoder, relative or absolute times of input edges in µs resolution, time-triggered I/O, I/O oversampling
General information	
B&R ID code	0x2547
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs/Outputs	Yes, using status LED
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines.
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Linear movement generator	
Quantity	1
Encoder outputs	24 V, asymmetrical (A/B; direction/frequency)
Counter size	16/32-bit
Digital inputs	
Quantity	4 + 4, configurable as inputs or outputs using software
Nominal voltage	24 VDC
Input voltage	24 VDC -15% / +20%
Input current at 24 VDC	Approx. 1.3 mA
Input filter	
Hardware	≤2 µs
Software	-
Input circuit	Sink
Additional functions	SSI absolute encoder, universal counter pair, latch function for universal counter pair
Input resistance	18.4 kΩ
Input frequency	100 kHz
Switching threshold	
Low	<5 VDC
High	>15 VDC
Overload behavior of the encoder supply	Short circuit protection, overload protection
Isolation voltage between channel and bus	500 V_{eff}
SSI absolute encoder	
Quantity	1
Counter size	Encoder-dependent up to 32-bit
Max. transfer rate	125 kbit/s
Encoder supply	Module-internal, max. 600 mA
Nominal voltage	24 V, asymmetrical
Universal counter pair	
Quantity	1
Operating modes	2x event counter, up/down counter, AB counter
Encoder inputs	24 V, asymmetrical
Counter size	16/32-bit
Input frequency	Max. 100 kHz
Evaluation	
AB counter	4x
Event counter	2x
Up/Down counter	2x
Signal form	Square wave pulse
Encoder supply	Module-internal, max. 600 mA
Digital outputs	
Design	Push / Pull / Push-Pull
Quantity	Up to 4, configurable as inputs or outputs using software
Nominal voltage	24 VDC
Switching voltage	24 VDC -15% / +20%

Table 360: X20DS1319 - Technical data

Product ID	X20DS1319
Nominal output current	0.1 A
Total nominal current	0.4 A
Output circuit	Sink and/or source
Output protection	Thermal cutoff if overcurrent or short circuit occurs, integrated protection for switching inductances
Diagnostic status	Output monitoring
Leakage current when switched off	Max. 25 µA
Residual voltage	<0.9 V at 0.1 A rated current
Peak short circuit current	<10 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<2 µs
1 -> 0	<2 µs
Switching frequency	
Resistive load	Max. 125 kHz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Switching voltage + 0.6 VDC
Additional functions	Timing for SSI absolute encoder, linear movement generator
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 360: X20DS1319 - Technical data

4.16.5.4 LED status indicators

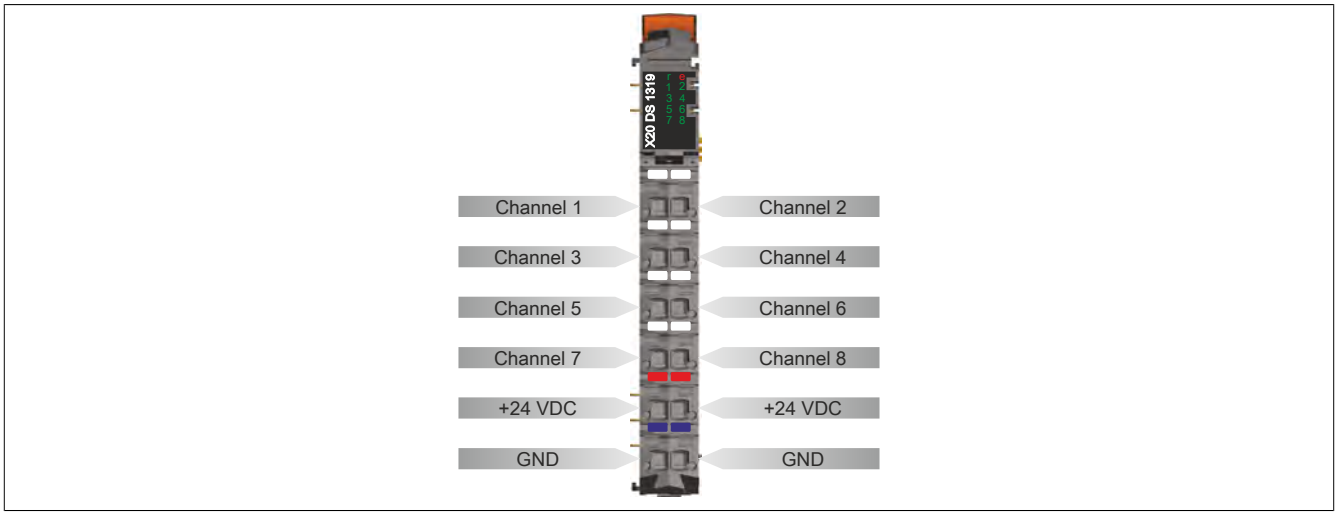
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	I/O error. Possible causes: • SSI error[2]
			Double flash	System error. Possible causes: • Motion function error[3] • I/O oversampling error[4] • Edge detection error[4]
			Triple flash	I/O error and system error occur together
			On	Error or reset status
	1 - 8	Green		Status of the corresponding digital signal

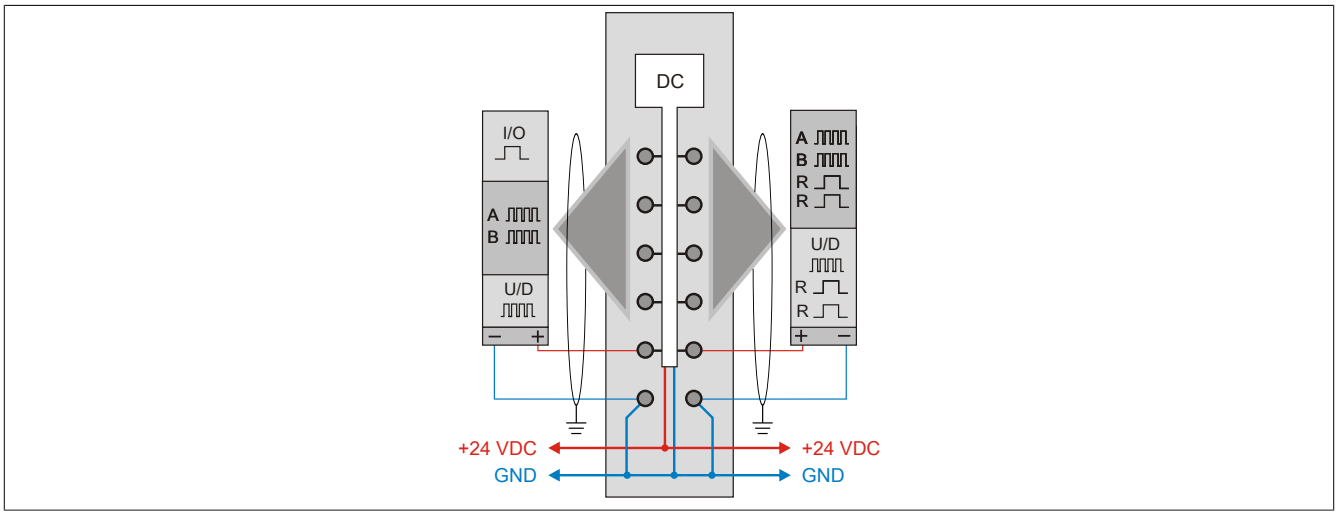
1) Depending on the configuration, a firmware update can take up to several minutes.
2) See 4.16.4.11.6.2 "Error state - SSI" register for the exact error description.
3) See 4.16.5.11.6.3 "Error state - Motion functions" register for the exact error description.
4) See 4.16.4.11.6.1 "Error state - Output data and edge detection" register for the exact error description.

4.16.5.5 Pinout

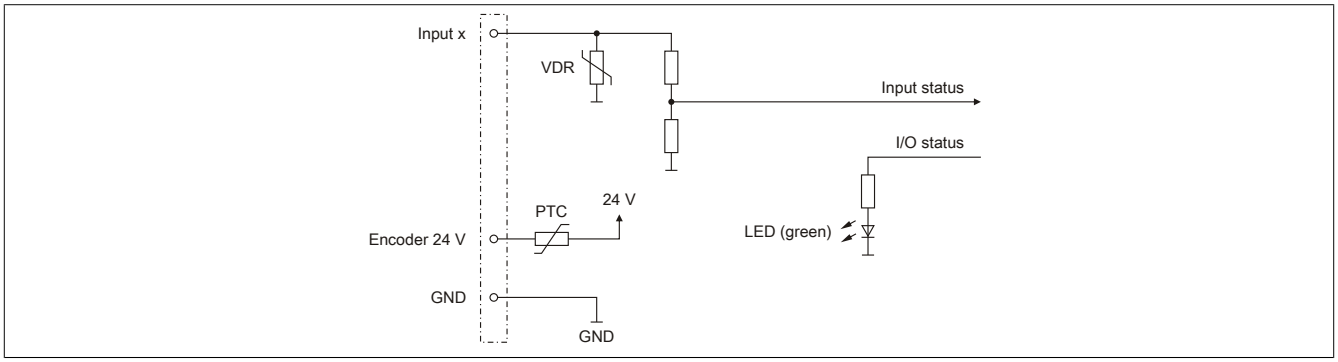
Shielded cables must be used for all signal lines.



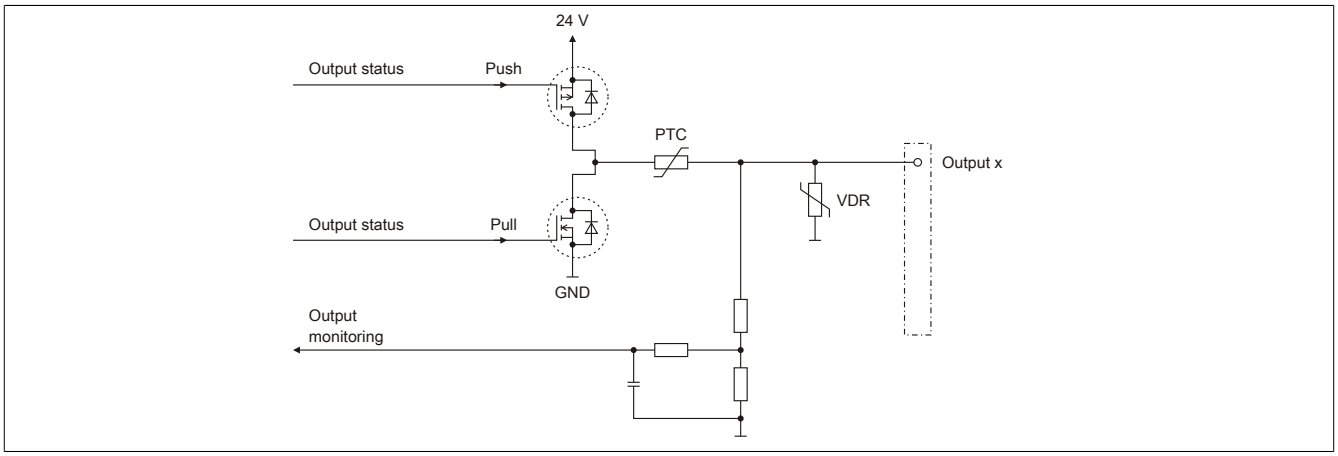
4.16.5.6 Connection example



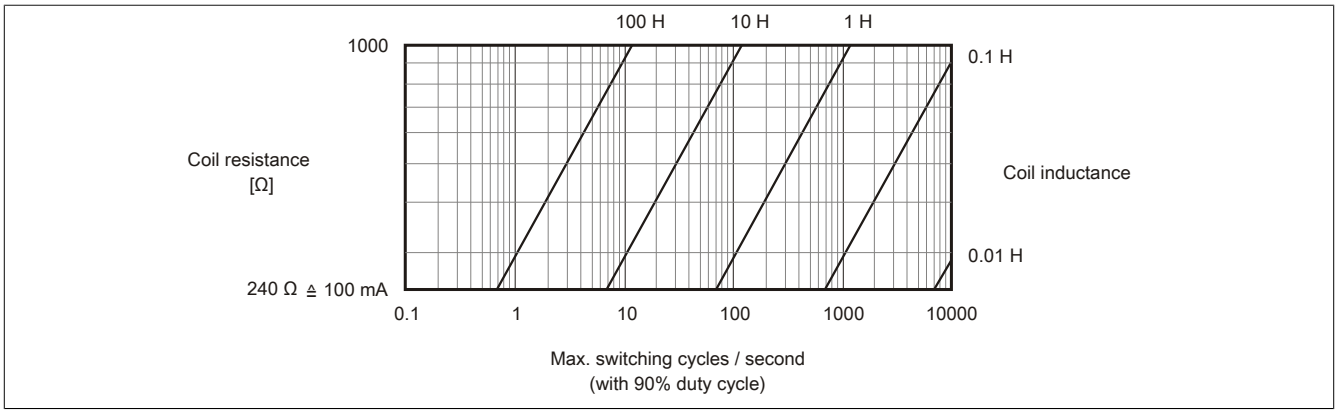
4.16.5.7 Input circuit diagram



4.16.5.8 Output circuit diagram



4.16.5.9 Switching inductive loads



4.16.5.10 Connection options

Digital input/output

Channel	Function
1	Input
2	Input
3	Input / Output
4	Input / Output
5	Input
6	Input
7	Input / Output
8	Input / Output

Wiring of the SSI absolute encoder

Channel	Function
5 (input)	Data
7 (output)	Clock

Wiring of the linear movement generator

Channel	Up-Down	AB
3 (output)	Direction	A
4 (output)	Frequency	B
7 (output)	Reference 1	
8 (output)	Reference 2	

Wiring of the universal counter pair

Channel	Edge counters	Up/Down counter	Incremental
1 (input)	Input 1	Direction	A
2 (input)	Input 2	Frequency	B
5 (input)		Latch input 1 (R)	
6 (input)		Latch input 2 (E)	

4.16.5.11 Register description

4.16.5.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.16.5.11.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - General						
513	CfO_SIframeGenID	USINT				•
Configuration - System timer						
642	CfO_SystemCycleTime	UINT				•
646	CfO_SystemCycleOffset	INT				•
650	CfO_SystemCyclePrescaler	UINT				•
Configuration - Physical I/O						
769 + (N-1) * 2	CfO_PhyIOConfigCh0N (Index N = 1 to 8)	USINT				•
Configuration - Direct I/O						
899	CfO_DirectIOClearMask0_7	USINT				•
903	CfO_DirectIOSetMask0_7	USINT				•
905	CfO_OutputUpdateCycle	USINT				•
Configuration - Oversampled I/O						
1025	CfO_OversampleMode	USINT				•
1027	CfO_OversampleSampleCycleID	USINT				•
1029	CfO_OversampleRelativeCycleID	USINT				•
1031	CfO_OversampleConsumeCycleID	USINT				•
1033	CfO_OversampleOutputBits	USINT				•
1035	CfO_OversampleInputBits	USINT				•
1037	CfO_OversampleOutputWindow	USINT				•
1039	CfO_OversampleInputWindow	USINT				•
1041 + (N*2)	CfO_OversampleConfigInputN (Index N = 0 to 3)	USINT				•
1049 + (N*2)	CfO_OversampleConfigOutputN (Index N = 0 to 3)	USINT				•
Configuration - Edge detection						
1537	CfO_EdgeDetectPollCycleID	USINT				•
1548	CfO_EdgeDetectEventEnable	UDINT				•
1665 + (N-1) * 16	CfO_EdgeDetectUnit0NMode (Index N = 1 to 4)	USINT				•
1667 + (N-1) * 16	CfO_EdgeDetectUnit0NLeading (Index N = 1 to 4)	USINT				•
1669 + (N-1) * 16	CfO_EdgeDetectUnit0NMaster (Index N = 1 to 4)	USINT				•
1671 + (N-1) * 16	CfO_EdgeDetectUnit0NSlave (Index N = 1 to 4)	USINT				•
Configuration - Movement functions						
4097	CfO_FifoSize	USINT				•
4099	CfO_Mode	SINT				•
4101	CfO_SpeedLimit	USINT				•
4103	CfO_FormatAdjust	USINT				•
4105	CfO_TimeStampRange	SINT				•
4107	CfO_PositionRange	SINT				•
4109	CfO_Reference0Range	SINT				•
4111	CfO_Reference1Range	SINT				•
4116	CfO_TimeStampDelay	DINT				•
4124	CfO_SpeedCycleTime_32bit	UDINT				•
4129	CfO_ResolPosition	SINT				•
4131	CfO_ResolSpeed	SINT				•
4220	CfO_AccelDataInit	UDINT				•
4260	CfO_Reference0Start	DINT				•
4268	CfO_Reference0StopMargin	DINT				•
4276	CfO_Reference1Start	DINT				•
4284	CfO_Reference1StopMargin	DINT				•
Configuration - SSI						
2049	CfO_CycleSelect	USINT				•
2051	CfO_PhysicalMode	USINT				•
2053	CfO_DataBits	USINT				•
2055	CfO_NullBits	USINT				•
Configuration - Universal counter						
6145	CfO_CounterCycleSelect	USINT				•
6147	CfO_CounterMode	USINT				•

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
6149	CfO_LatchMode	USINT				●
6151	CfO_LatchComparator	USINT				●
6153	CounterControl	USINT			●	
	CounterReset	Bit 0				
	LatchEnable	Bit 1				
Communication - General						
546	ProtocolError (16-bit)	USINT	●			
547	ProtocolError (8-bit)	UINT	●			
550	ProtocolSequenceViolation (16-bit)	UINT	●			
551	ProtocolSequenceViolation (8-bit)	USINT	●			
Communication - Error register						
257	Error state - Output data and edge detection	USINT	●			
	OutputControlError	Bit 4				
	OutputCopyError	Bit 5				
	EdgeDetectError	Bit 6				
259	Error state - SSI	USINT	●			
	SSICycleTimeViolation	Bit 0				
	SSIParityError	Bit 1				
261	Error state - Movement functions	USINT	●			
	MovFifoEmpty	Bit 0				
	MovFifoFull	Bit 1				
	MovTargetTimeViolation	Bit 2				
	MovMaxFrequencyViolation	Bit 3				
321	Acknowledge error messages - Output data and edge detection	USINT			●	
	QuitOutputControlError	Bit 4				
	QuitOutputCopyError	Bit 5				
	QuitEdgeDetectError	Bit 6				
323	Acknowledge error messages - SSI	USINT			●	
	SSIQuitCycleTimeViolation	Bit 0				
	SSIQuitParityError	Bit 1				
325	Acknowledge error messages - Movement functions	USINT			●	
	MovQuitFifoEmpty	Bit 0				
	MovQuitFifoFull	Bit 1				
	MovQuitTargetTimeViolation	Bit 2				
	MovQuitMaxFrequencyViolation	Bit 3				
Communication - System timer						
683	SDCLifeCount	SINT	●			
Communication - Direct I/O						
915	"DigitalOutput" register	USINT			●	
	DigitalOutput03	Bit 2				
	DigitalOutput04	Bit 3				
	DigitalOutput07	Bit 6				
	DigitalOutput08	Bit 7				
927	"DigitalInput" register	USINT	●			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
Communication - Oversampled I/O (output)						
1059	Oversample register - Configuration	USINT			●	
	OversampleEnable	Bit 0				
	OversampleOutputValidate	Bit 1				
1063	OversampleOutputCycle	USINT			●	
	OversampleSampleOffset	USINT			●	
1088 + N	OversampleOutput0NSample1_8 (Index N = 1 to 4)	USINT			●	
1092 + N	OversampleOutput0NSample9_16 (Index N = 1 to 4)	USINT			●	
1096 + N	OversampleOutput0NSample17_24 (Index N = 1 to 4)	USINT			●	
1100 + N	OversampleOutput0NSample25_32 (Index N = 1 to 4)	USINT			●	
1104 + N	OversampleOutput0NSample33_40 (Index N = 1 to 4)	USINT			●	
1108 + N	OversampleOutput0NSample41_48 (Index N = 1 to 4)	USINT			●	
1112 + N	OversampleOutput0NSample49_56 (Index N = 1 to 4)	USINT			●	
1116 + N	OversampleOutput0NSample57_64 (Index N = 1 to 4)	USINT			●	
Communication - Oversampled I/O (input)						
1074	OversampleInputTime	INT	●			
1079	OversampleInputCycle	USINT	●			
1120 + N	OversampleInput0NSample64_57 (Index N = 1 to 4)	USINT	●			
1124 + N	OversampleInput0NSample56_49 (Index N = 1 to 4)	USINT	●			
1128 + N	OversampleInput0NSample48_41 (Index N = 1 to 4)	USINT	●			
1132 + N	OversampleInput0NSample40_33 (Index N = 1 to 4)	USINT	●			
1136 + N	OversampleInput0NSample32_25 (Index N = 1 to 4)	USINT	●			
1140 + N	OversampleInput0NSample24_17 (Index N = 1 to 4)	USINT	●			
1144 + N	OversampleInput0NSample16_9 (Index N = 1 to 4)	USINT	●			
1148 + N	OversampleInput0NSample8_1 (Index N = 1 to 4)	USINT	●			
Communication - Edge detection						

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
1794 + (N-1) * 32	EdgeDetect0NMastercount (16-bit) (Index N = 1 to 4)	INT	●			
1795 + (N-1) * 32	EdgeDetect0NMastercount (8-bit) (Index N = 1 to 4)	SINT	●			
1798 + (N-1) * 32	EdgeDetect0NSlavecount (16-bit) (Index N = 1 to 4)	INT	●			
1799 + (N-1) * 32	EdgeDetect0NSlavecount (8-bit) (Index N = 1 to 4)	SINT	●			
1804 + (N-1) * 32	EdgeDetect0NDifference (32-bit) (Index N = 1 to 4)	DINT	●			
1806 + (N-1) * 32	EdgeDetect0NDifference (16-bit) (Index N = 1 to 4)	INT	●			
1812 + (N-1) * 32	EdgeDetect0NMastertime (32-bit) (Index N = 1 to 4)	DINT	●			
1814 + (N-1) * 32	EdgeDetect0NMastertime (16-bit) (Index N = 1 to 4)	INT	●			
1820 + (N-1) * 32	EdgeDetect0NSlavetime (32-bit) (Index N = 1 to 4)	DINT	●			
1822 + (N-1) * 32	EdgeDetect0NSlavetime (16-bit) (Index N = 1 to 4)	INT	●			
Communication - Movement functions						
4225	MovementControl	USINT			●	
	MovPosEnable	Bit 0				
	MovSpeedEnable	Bit 1				
4244	MovTargetTime (32-bit)	DINT			●	
4246	MovTargetTime (16-bit)	INT			●	
4252	MovTargetPosition (32-bit)	DINT			●	
4254	MovTargetPosition (16-bit)	INT			●	
4260	MovReference1Start (32-bit)	DINT			●	
4262	MovReference1Start (16-bit)	INT			●	
4268	MovReference1StopMargin (32-bit)	DINT			●	
4270	MovReference1StopMargin (16-bit)	INT			●	
4276	MovReference2Start (32-bit)	DINT			●	
4278	MovReference2Start (16-bit)	INT			●	
4284	MovReference2StopMargin (32-bit)	DINT			●	
4286	MovReference2StopMargin (16-bit)	INT			●	
4212	MovSpeed (32-bit)	DINT			●	
4210	MovSpeed (16-bit)	INT			●	
4220	MovAcceleration (32-bit)	UDINT			●	
4218	MovAcceleration (16-bit)	UINT			●	
4292	MovTimeValid (32-bit)	DINT	●			
4294	MovTimeValid (16-bit)	INT	●			
4300	MovPosition (32-bit)	DINT	●			
4302	MovPosition (16-bit)	INT	●			
Communication - SSI						
2084	SSITimeValid (32-bit)	DINT	●			
2086	SSITimeValid (16-bit)	INT	●			
2092	SSITimeChanged (32-bit)	DINT	●			
2094	SSITimeChanged (16-bit)	INT	●			
2100	SSIPosition (32-bit)	(U)DINT	●			
2102	SSIPosition (16-bit)	UINT	●			
Communication - Universal counter						
6303	LatchCount	SINT	●			
6308	CounterTimeValid (32-bit)	DINT	●			
6310	CounterTimeValid (16-bit)	INT	●			
6324	Counter01TimeChanged (32-bit)	DINT	●			
6326	Counter01TimeChanged (16-bit)	INT	●			
6332	Counter02TimeChanged (32-bit)	DINT	●			
6334	Counter02TimeChanged (16-bit)	INT	●			
6340	CounterValue01 (32-bit)	DINT	●			
6342	CounterValue01 (16-bit)	INT	●			
6348	CounterValue02 (32-bit)	DINT	●			
6350	CounterValue02 (16-bit)	INT	●			
6356	CounterLatch01 (32-bit)	DINT	●			
6358	CounterLatch01 (16-bit)	INT	●			
6364	CounterLatch02 (32-bit)	DINT	●			
6366	CounterLatch02 (16-bit)	INT	●			
6372	CounterRel01 (32-bit)	DINT	●			
6374	CounterRel01 (16-bit)	INT	●			
6380	CounterRel02 (32-bit)	DINT	●			
6382	CounterRel02 (16-bit)	INT	●			

4.16.5.11.3 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.16.5.11.4 General

4.16.5.11.4.1 Use with Automation Studio

The module is supported via X2X Link and POWERLINK.

X2X Link supports a up to 28 bytes of synchronous data per module. To optimize use and to prevent needless data transfer, the data points can be adjusted as needed in Automation Studio. Data points that are not needed can be disabled, and the bit width of the data points can be defined.

4.16.5.11.4.2 Timestamp function

The timestamp function is based on synchronized timers. When a timestamp event occurs, the module immediately saves the current net time. After the respective data is transmitted to the CPU, including this precise time, the CPU can then evaluate the data using its own net time (or system time).

Conversely, the CPU can predefine output events, apply a timestamp and transfer them to the module. The module then executes the predefined action at the precise time defined by the CPU.

The resolution of the timestamp is up to 1/8 µs in both directions.

4.16.5.11.4.3 Synchronization jitter

Because the CPU – which determines the X2X net time – and the module have different clocks, the module's internal X2X net time must be synchronized with the CPU's net time. Due to this synchronization, the module's internal X2X net time is corrected by a maximum of 1/8 µs per system cycle if necessary. This synchronization jitter becomes noticeable when using the net time with 1/8 µs resolution (max. ±1/8 µs).

If a 100% exact 1/8 µs resolution without jitter is required, then the "localtime 1/8 µs" must be used (see the 4.16.4.11.11.3 "CfO_EdgeDetectUnitMode" register).

4.16.5.11.5 General registers

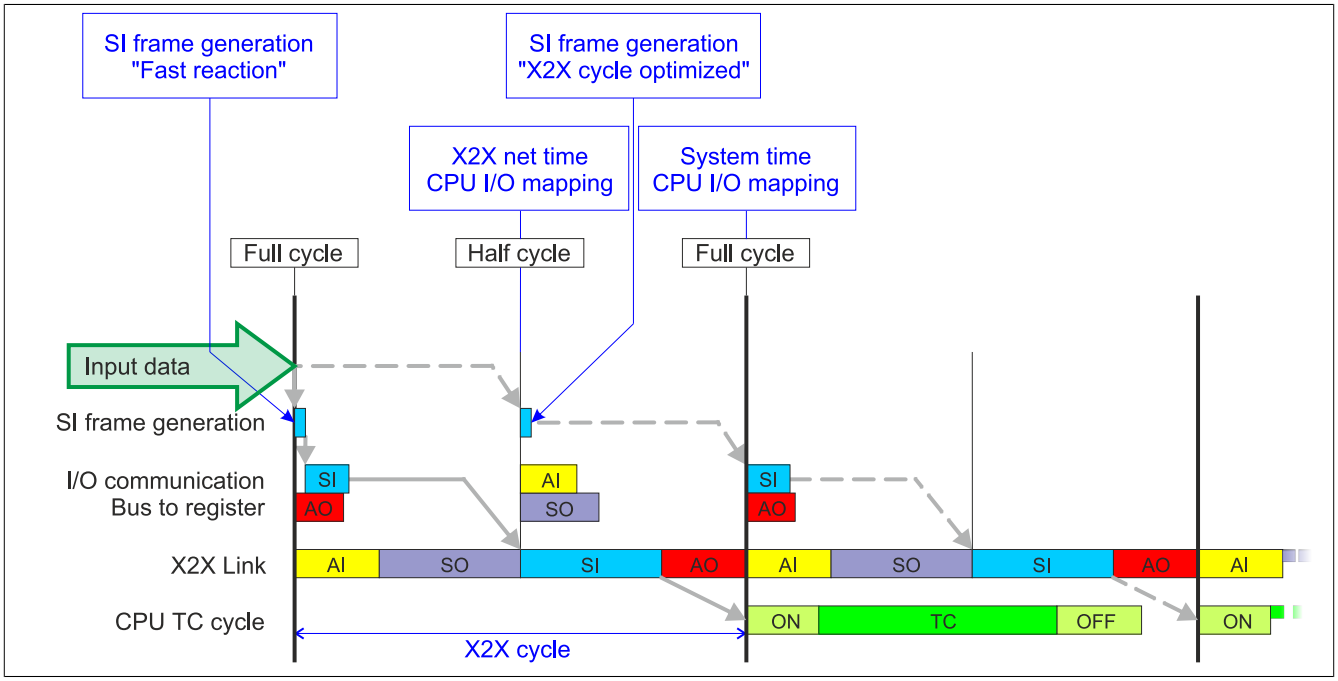
4.16.5.11.5.1 "CfO_SIframeGenID" register

Name:
CfO_SIframeGenID
"SI-frame generation" in the AS I/O configuration.

This register determines when the synchronous input data is generated for transfer. This has a decisive effect on the timing of the input data.

The setting "Fast reaction" causes the input data to be available one X2X cycle sooner in the CPU. However, this setting also has a negative effect on the minimum X2X cycle time.

Data type	Value	Information
USINT	9	X2X cycle optimized
	14	Fast reaction



4.16.5.11.5.2 "ProtocolError" register

Name:
ProtocolError

This register contains an error counter that specifies the number of X2X protocol errors. In the I/O configuration, the "Network information" parameter can be used to help configure a data point for this register with a bit width of 8 or 16 bits in the I/O mapping.

Data type	Value	Information
USINT	0 to 255	Error counter (8-bit)
UINT	0 to 65,535	Error counter (16-bit)

4.16.5.11.5.3 "ProtocolSequenceViolation" register

Name:
ProtocolSequenceViolation

This register contains an error counter that specifies the number of X2X sequence violations. In the I/O configuration, the "Network information" parameter can be used to help configure a data point with a bit width of 8 or 16 bits in the I/O mapping.

Data type	Value	Information
USINT	0 to 255	Error counter (8-bit)
UINT	0 to 65,535	Error counter (16-bit)

4.16.5.11.5.4 "SDCLifeCount" register

Name:
SDCLifeCount

Counter that is incremented with each system timer cycle. The "SDC information" setting in the AS I/O configuration can be used to activate this register in the I/O mapping as the data point, "SDCLifeCount".

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.16.5.11.6 Error handling

If one of the functions detects an error, then an error bit is set in one of the error state registers. The application is now able to react accordingly and acknowledge the errors by setting a respective bit in the "Acknowledge error message" registers. This causes the bit to be reset in the error state register. If the source of the error persists, then the error bit is set again as soon as the error is detected again (i.e. cannot be reset).

Acknowledging the error does not affect the module's functionality. If possible, the module automatically resumes processing as soon as the source of the error has been corrected.

If an error occurs (not a warning), this is indicated by the red "e" LED on the module (double flash). This signal is automatically acknowledged as soon as the source of the error has been corrected.

4.16.5.11.6.1 Error state register - Output data and edge detection

Name:
OutputControlError
OutputCopyError
EdgeDetectError

Errors in the output data and cycle time settings are indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	OutputControlError	0	No error
		1	The module did not receive new data in time while in the mode "Output control mode = single", meaning that a bit that has already been output would have been output again by the output control buffer.
5	OutputCopyError	0	No error
		1	Oversampling output data could not be copied to the output control buffer. (e.g. an attempt was made to write oversampling output data to an address outside of the OversampleOutputWindow).
6	EdgeDetectError	0	No error
		1	Cycle time violation edge detection: The "EdgeDetectPollCycle" must be smaller than or equal to 255 µs. This error is caused if the cycle defined in the 4.16.4.11.11.1 "CfO_EdgeDetectPollCycleID" register is > 255 µs.
7	Reserved	-	

4.16.5.11.6.2 Error state register - SSI

Name:
SSICycleTimeViolation
SSIParityError

SSI interface errors are indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	SSICycleTimeViolation	0	No error
		1	Error occurred, possible causes: • SSI transfer takes longer than the defined "Update cycle". • Monoflop check is enabled and the SSI data line does not assume the defined level after the transfer is complete.
1	SSIParityError	0	No error
		1	SSI parity error
2 - 7	Reserved	-	

4.16.5.11.6.3 Error state register - Movement functions

Name:
MovFifoEmpty
MovFifoFull
MovTargetTimeViolation
MovMaxFrequencyViolation

Movement function errors are indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	MovFifoEmpty	0	No error
		1	The position/timestamp FIFO is empty.
1	MovFifoFull	0	No error
		1	The position/timestamp FIFO has exceeded the size defined in the 4.16.4.11.12.3 "FifoSize" register.
2	MovTargetTimeViolation	0	No error
		1	This only occurs when the 4.16.4.11.12.18 "MovTargetTime" is in the past.
3	MovMaxFrequencyViolation	0	No error
		1	The maximum output frequency setpoint has exceeded the maximum frequency configured in the 4.16.5.11.12.5 "CfO_SpeedLimit" register.
4 - 7	Reserved	-	

4.16.5.11.6.4 Acknowledge error message register - Output data and edge detection

Name:
QuitOutputControlError
QuitOutputCopyError
QuitEdgeDetectError

Error messages from the 4.16.4.11.6.1 "Error state - Output data and edge detection" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	QuitOutputControlError	0	No change
		1	Acknowledge error
5	QuitOutputCopyError	0	No change
		1	Acknowledge error
6	QuitEdgeDetectError	0	No change
		1	Acknowledge error
7	Reserved	-	

4.16.5.11.6.5 Acknowledge error message register - SSI

Name:
SSIQuitCycleTimeViolation
SSIQuitParityError

Error messages from the 4.16.4.11.6.2 "Error state - SSI" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	SSIQuitCycleTimeViolation	0	No change
		1	Acknowledge error
1	SSIQuitParityError	0	No change
		1	Acknowledge error
2 - 7	Reserved	-	

4.16.5.11.6.6 Acknowledge error message register - Movement functions

Name:
MovQuitFifoEmpty
MovQuitFifoFull
MovQuitTargetTimeViolation
MovQuitMaxFrequencyViolation

Error messages from the 4.16.5.11.6.3 "Error state register - Movement functions"register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	MovQuitFifoEmpty	0	No change
		1	Acknowledge error
1	MovQuitFifoFull	0	No change
		1	Acknowledge error
2	MovQuitTargetTimeViolation	0	No change
		1	Acknowledge error
3	MovQuitMaxFrequencyViolation	0	No change
		1	Acknowledge error
4 - 7	Reserved	-	

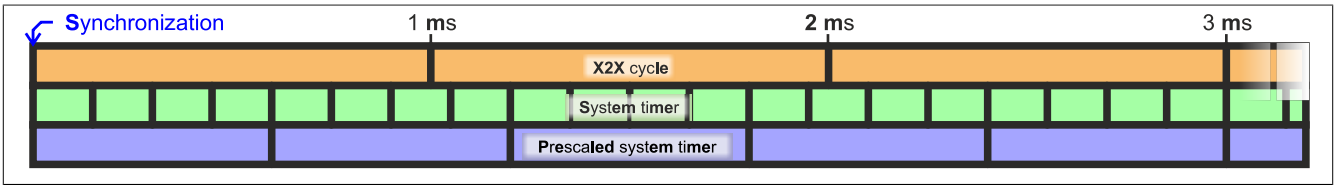
4.16.5.11.7 System timer

The module's individual functions all depend on a system timer. This internal "system cycle time" can be defined from 25 to 255 µs. The functions can also be run with the help of a configurable "prescaled system timer" to minimize the load on the module, thereby making it possible to use the shortest possible X2X cycle time.

The cycle of the "prescaled system timer" (and system timer) is referenced with the X2X Link as soon as the module has been started up and the X2X Link has been initialized. Since the system timer and the module's internal X2X net time use the same clock, the two run synchronously from that point on. An X2X cycle time that is not a multiple of the system cycle time results in an offset, which can be calculated.

The following values apply to the following example:

X2X cycle	1 ms
System timer	150 µs
Prescaled system timer	4



4.16.5.11.7.1 "CfO_SystemCycleTime" register

Name:
CfO_SystemCycleTime
"Cycle time" in the AS I/O configuration.

The cycle time of the system timer can be set in this register in steps of 1/8 µs. The value entered in the AS I/O configuration is automatically multiplied by 8.

Information:

A setting < 50 µs has a negative effect on the minimum X2X cycle time!

Data type	Value	Information
UINT	200 to 2047	System timer cycle time in steps of 1/8 µs (25 to 255,875 µs)

4.16.5.11.7.2 "CfO_SystemCycleOffset" register

Name:
CfO_SystemCycleOffset
"Cycle offset" in the AS I/O configuration.

The synchronization time for the system cycle can be offset in this register in steps of 1/8 µs. The value entered in the AS I/O configuration is automatically multiplied by 8.

Data type	Value	Information
INT	-32,768 to 32,767	Cycle offset in steps of 1/8 µs (-4096 to 4095.875 µs)

4.16.5.11.7.3 "CfO_SystemCyclePrescaler" register

Name:
CfO_SystemCyclePrescaler
"Cycle prescaler" in the AS I/O configuration.

The prescaler for setting the "Prescaled system timer" can be configured in this register. The cycle time of the specified system timer is a product of the system timer multiple set in this register.

The "prescaled system timer" can be used as alternative time source for the individual functions. This is useful if a function requires a very short system cycle. To reduce the load on the module in such a situation, other functions can be processed in a slow cycle.

Data type	Value	Information
UINT	2 to 128	Multiple of the system timer

4.16.5.11.8 Physical I/O configuration

4.16.5.11.8.1 "CfO_PhyIOConfigCh" registers

Name:
CfO_PhyIOConfigCh01 to CfO_PhyIOConfigCh08

The physical I/O channels can each be configured individually in these registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Push driver[1)]	0	Disabled
		1	Enabled
1	Pull driver[1)]	0	Disabled
		1	Enabled
2	Input inverted	0	Not inverted
		1	Inverse
3	Output inverted[1)]	0	Not inverted
		1	Inverse
4 - 7	Output function[1)]	0 to 15	See: Overview of output channel functions

1) Only available for the I/O channels 3, 4, 7 and 8.

Overview of output channel functions

Values of bits 4 to 7	Output channel 3	Output channel 4	Output channel 7	Output channel 8
0	Direct I/O			
1				SSI clock output
2	ABR emulation (A)	ABR emulation (B)	ABR emulation (reference 1)	ABR emulation (reference 2)
3	Up/down emulation (direction)	Up/down emulation (frequency)	Up/down emulation (reference 1)	Up/down emulation (reference 2)
4 - 15	Reserved			

4.16.5.11.9 Direct I/O

Direct I/O makes it possible to use the physical I/Os like normal I/Os. Additionally, the application can only set or reset I/Os (e.g. an output channel is set by the edge generator and manually reset by the application).

4.16.5.11.9.1 "EdgeGenTimestamp" register

Name:
CfO_DirectIOClearMask0_7
"Direct control of output channel 03" to "Direct control of output channel 08" in the AS I/O configuration.

If the bit for the respective channel is set in this register, then the output is reset as soon as its direct I/O output channel is reset (4.16.5.11.9.3 "output control channel 7_0" or "DigitalOutput0x" register in the AS I/O mapping).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	-	
2	Output channel 3	0	No change
		1	Reset channel
3	Output channel 4	0	No change
		1	Reset channel
4 - 5	Reserved	-	
6	Output channel 7	0	No change
		1	Reset channel
7	Output channel 8	0	No change
		1	Reset channel

4.16.5.11.9.2 "CfO_DirectIOSetMask0_7" register

Name:
CfO_DirectIOSetMask0_7
"Direct control of output channel 03" to "Direct control of output channel 08" in the AS I/O configuration.

If the bit for the respective channel is set in this register, then the output is set as soon as its direct I/O output channel is set (4.16.5.11.9.3 "output control channel 7_0" or "DigitalOutput0x" register in the AS I/O mapping).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	-	
2	Output channel 3	0	No change
		1	Set channel
3	Output channel 4	0	No change
		1	Set channel
4 - 5	Reserved	-	
6	Output channel 7	0	No change
		1	Set channel
7	Output channel 8	0	No change
		1	Set channel

4.16.5.11.9.3 "DigitalOutput" register

Name:
DigitalOutput03 and DigitalOutput04, DigitalOutput07 and DigitalOutput08

This register contains the bits for controlling the direct I/O output channels. Depending on how the 4.16.5.11.9.1 "CfO_DirectIOClearMask0_7" and 4.16.5.11.9.2 "CfO_DirectIOSetMask0_7" registers are configured, the digital outputs are set to the status of the respective bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	-	
2	DigitalOutput03	0 or 1	Output status of channel 3
3	DigitalOutput04	0 or 1	Output status of channel 4
4 - 5	Reserved	-	
6	DigitalOutput07	0 or 1	Output status of channel 7
7	DigitalOutput08	0 or 1	Output status of channel 8

4.16.5.11.9.4 "DigitalInput" register

Name:
DigitalInput01 to DigitalInput08

This register displays the status of the digital input channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalInput01	0 or 1	Input status of channel 1
...	...	...	
7	DigitalInput08	0 or 1	Input status of channel 8

4.16.5.11.10 Oversampled I/O

"Oversampled I/O" is based on input status buffers and output control buffers. Input data acquisition and output control occur in one sample cycle (one sample cycle equals one bit in the buffer). The precise time of an input buffer entry is indicated by its position in the buffer and the net time assigned to the buffer.

In "Output control mode = single" every output buffer entry is marked as invalid once it has been executed. This ensures that the outputs are not supplied with invalid data. In this mode, the application needs to ensure that the module is always supplied with valid data.

When using "Output control mode = continuous" the contents of the buffer are output again if the module is not supplied with new oversample output data.

4.16.5.11.10.1 Addressing the output control buffer

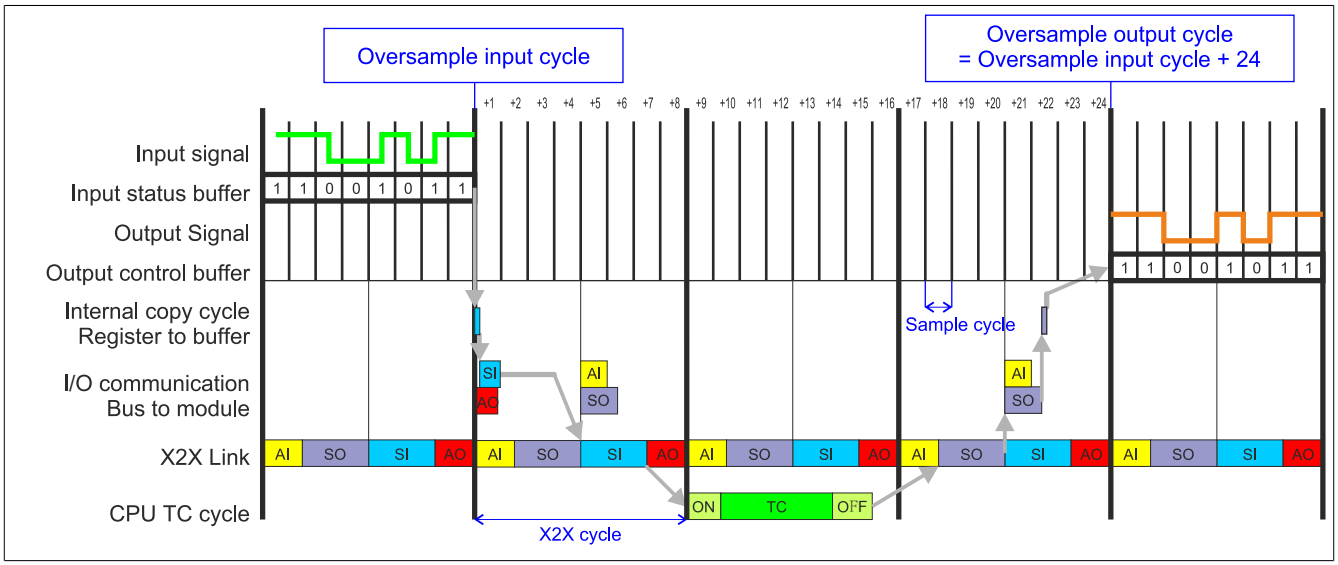
The module has one cyclic 256-bit output control buffer for each oversample channel. One bit is output from these buffers to the configured physical output channels in each "sample cycle". When new data is transferred to one of these buffers, the application must define where in the respective buffer the data should be written to. There are 2 possibilities (absolute or relative "Output mode" in the AS I/O configuration).

Absolute addressing of the output control buffer

With absolute addressing, in each cycle where "OversampleOutputValidate = True", in addition to the oversample output sample data (in the 4.16.4.11.10.15 "OversampleOutput0NSample" registers) an address must also be transferred in the 4.16.4.11.10.13 "OversampleOutputCycle" register. This address determines where in the output control buffer the new data should be copied to. In order to calculate this address, you must account for the contents of the 4.16.4.11.10.17 "OversampleInputCycle" register, which contains the address of the most recently output data, and the transfer time to the module. To help avoid incorrect addressing of the output control buffer, the buffer section that is capable of being written to can be limited using the 4.16.4.11.10.8 "OversampleOutputWindow" register. This window will always be shifted relative to the current sample address. An "OutputCopyError" will be triggered if an attempt is made to write to an address that is outside of this window.

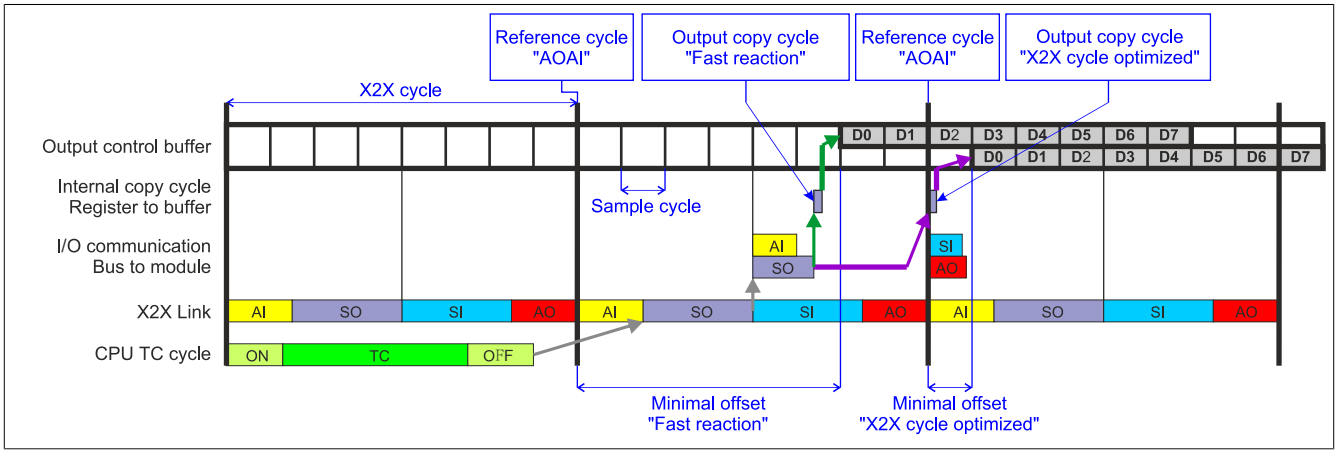
Example

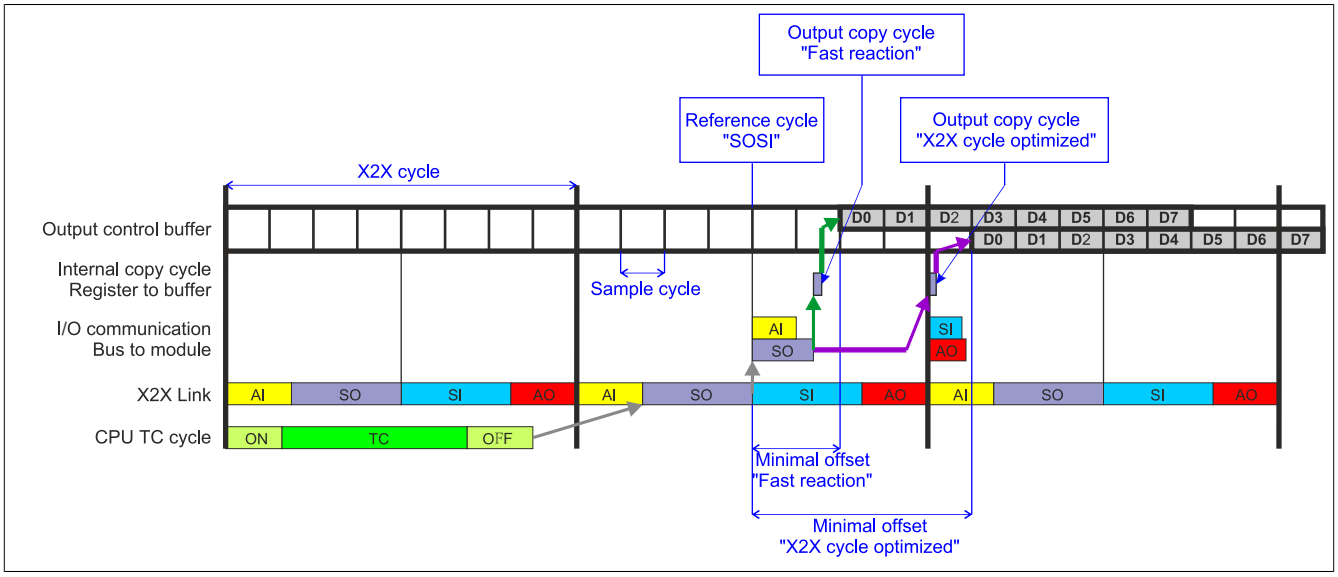
Timing from oversample input cycle to oversample output cycle in absolute output mode ("SI-frame generation = Fast reaction", "Output copy cycle = Fast reaction", 8 samples per X2X cycle):



Relative addressing of the output control buffer

When "OversampleOutputValidate = True", then the oversample output sample data is automatically copied to an address relative to the last referenced address at the defined "output copy cycle" time. The 4.16.4.11.10.14 "OversampleSampleOffset" register serves as the offset. The new data cannot start being output immediately at the "output copy cycle" time because it takes time to copy the data from the registers to the buffer. This means that an offset of 0 is not allowed. The relative output control buffer address + offset must point to an address within the "oversample output window". The "oversample output window" is always offset relative to the current sample address. An "OutputCopyError" is triggered if an attempt is made to write to an address that is outside of this window.





4.16.5.11.10.2 "CfO_OversampleMode" register

Name:
CfO_OversampleMode
"Output mode" in the AS I/O configuration
"Output control mode" in the AS I/O configuration.

The output control buffer can be configured globally for all channels in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Addressing the output control buffer "Output mode" in the AS I/O configuration.	0	Absolute addressing of the output control buffer
		1	Relative addressing of the output control buffer
1	Cyclic output control "Output control mode" in the AS I/O configuration.	0	Single - Output control buffer entry is marked invalid after execution.
		1	Continuous - Output control buffer entry is not changed.
2 - 7	Reserved	-	

Cyclic output control

If cyclic output control is enabled, then all data in the output control buffer is marked invalid as soon as it is output ("Output control mode = single"). An OutputControlError is generated if the module does not receive data in time, thereby causing a situation in which a bit that has already been output would be output in the buffer again. In such a situation, the output assumes the "Output default state" configured in the CfO_OversampleConfigOutput register.

If cyclic output control is disabled, then the data is output again if the output control buffer overflows ("Output control mode = continuous").

Information:

All 256 bits of the output control buffer are always output.

4.16.5.11.10.3 "CfO_OversampleSampleCycleID" register

Name:
CfO_OversampleSampleCycleID
"Sample cycle" in the AS I/O configuration.

The source of the sample cycle can be configured in this register. During each sample cycle, one bit from the output control buffers of the oversampled I/O channels is output to the configured physical output, and the status of the configured inputs is entered in one bit of the respective input status buffer.

Data type	Value	Information
USINT	2	System timer The value configured in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used as the sample cycle.
	3	Prescaled system timer The "prescaled system timer" is used as sample cycle.
	10	AOAI The sample cycle is clocked with the AOAI interrupt of the X2X cycle.
	14	SOSI The sample cycle is clocked with the SOSI interrupt of the X2X cycle.

4.16.5.11.10.4 "CfO_OversampleRelativeCycleID" register

Name:
CfO_OversampleRelativeCycleID
"Reference cycle" in the AS I/O configuration.

The source of the user interface reference cycle can be configured in this register.

- The input data is referenced at the time of the "reference cycle". The referenced data is then copied to the "oversample input sample register" at the time of "SI frame generation", while taking the "OversampleInputWindow" into account.
- With relative addressing of the output control buffer, the new sample data is copied to an address relative to the output control buffer address current to the "reference cycle".
- The reference cycle is also used to reference the sample cycle, and with it also the output data production and input data acquisition (e.g. to the X2X cycle).

Data type	Value	Information
USINT	2	System timer The value configured in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used as the reference cycle.
	3	Prescaled system timer The "prescaled system timer" is used as sample cycle.
	10	AOAI The sample cycle is referenced with the AOAI interrupt of the X2X cycle.
	14	SOSI The sample cycle is referenced with the SOSI interrupt of the X2X cycle.

4.16.5.11.10.5 "CfO_OversampleConsumeCycleID" register

Name:
CfO_OversampleConsumeCycleID
"Output copy cycle" in the AS I/O configuration.

At the time of the output copy cycle, data is copied from the 4.16.4.11.10.15 "OversampleOutput0NSample" registers into the output control buffer.

When "Output copy cycle = Fast reaction", it is not possible to determine when the data is copied to the output control buffer in either of the two addressing modes. The copy cycles will experience a certain degree of jitter depending on the module load. However, this only affects the moment of the internal copy procedures and therefore the moment of the earliest possible output sample. This will not affect the quality of the output signal. However, "Output copy cycle = Fast reaction" also has a negative effect on the minimum X2X cycle time.

When using the setting "Output copy cycle = X2X cycle optimized", be aware that the sample data cannot start being output immediately at the "Output copy cycle" time due to the internal copy cycle to the output control buffers.

Data type	Value	Information
USINT	10	X2X cycle optimized The output data is copied to the output control buffer with the AOAI interrupt of the X2X cycle.
	15	Fast reaction The output data is copied to the output control buffer immediately after being received.

4.16.5.11.10.6 "CfO_OversampleOutputBits" register

Name:
CfO_OversampleOutputBits
"User interface size" in the AS I/O configuration.

Specifies how many bits are transferred from the 4.16.4.11.10.15 "OversampleOutputONSample" registers to the output control buffers at the time of the "output copy cycle".

Data type	Value	Information
USINT	1 to 64	Output bits

4.16.5.11.10.7 "CfO_OversampleInputBits" register

Name:
CfO_OversampleInputBits
"User interface size" in the AS I/O configuration.

Specifies how many bits are transferred from the input status buffer to the 4.16.4.11.10.18 "OversampleInput0NSample" register during "SI frame generation".

Data type	Value	Information
USINT	1 to 64	Input bits

4.16.5.11.10.8 "CfO_OversampleOutputWindow" register

Name:
CfO_OversampleOutputWindow
"Output control mode" in the AS I/O configuration.

Determines the area in the output control buffer in which data can be written. The window is always offset relative to the current sample position. (a value of 128, for example, means that the 128 bits following the current sample cycle can be written to). An "OutputCopyError" is triggered if an attempt is made to write output sample data to a location outside of this window.
In AS, with the setting "Output control mode = Single", this register is set to 128 bits and with the setting "Output control mode = Continuous" it is set to 255 bits.

Data type	Value	Information
USINT	0 to 255	Output window

4.16.5.11.10.9 "CfO_OversampleInputWindow" register

Name:
CfO_OversampleInputWindow
"Input mode" in the AS I/O configuration.

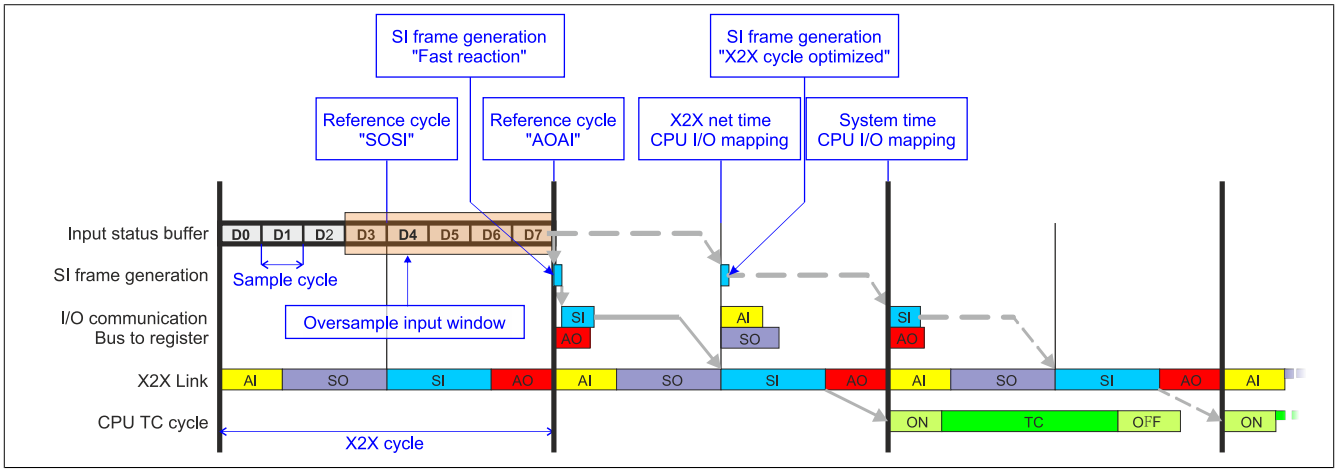
The "OversampleInputWindow" determines when the input data is referenced. It is located chronologically before "SI frame generation". If the reference time ("reference cycle") is within this window, then the referenced data is copied from the input status buffer to the OversampleInput0NSample register. If the time at which the reference occurs is outside the "OversampleInputWindow" then the data that is most recent at the time of "SI frame generation" is copied from the input status buffer to the 4.16.4.11.10.18 "OversampleInput0NSample" register.
This register is limited internally with to the value set in the 4.16.4.11.10.7 "CfO_OversampleInputBits" register.

Information:

As a result, the "OversampleInputTime" and the "OversampleInputCycle" are set either at the reference time or at the time of "SI frame generation".

In Automation Studio, this register is set to 63 when "Input mode = Referenced values" and to 0 when "Input mode = Most recent values".

Data type	Value	Information
USINT	0 to 63	Input window



4.16.5.11.10.10 "CfO_OversampleConfigInput" register

Name:
CfO_OversampleConfigInput
"Oversample I/O 01 →Input" to "Oversample I/O 04 → Input" in the AS I/O configuration

This register determines which physical input channel an oversample I/O input should be linked to.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Number of the physical input channel	0	Input channel 1
		..	
		7	Input channel 8
4 - 7	Reserved	-	

4.16.5.11.10.11 "CfO_OversampleConfigOutput" register

Name:
CfO_OversampleConfigOutput
"Oversample I/O 01 → Output" to "Oversample I/O 04 → Output" in the AS I/O configuration
"Oversample I/O 01 → Output control" to "Oversample I/O 04 → Output control" in the AS I/O configuration
"Oversample I/O 01 → Output default state" to "Oversample I/O 04 → Output default state" in the AS I/O configuration

This register helps configure the outputs of the individual oversample channels.

The "Output default state" bits determine which level the respective output assumes before oversampling is started. Furthermore, the output is set to the defined "Output default state" in the event of an error.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Number of the physical output channel "Oversample I/O 0x →Output" in the AS I/O configuration	2	Output channel 3
		3	Output channel 4
		6	Output channel 7
		7	Output channel 8
4	Output: Clear "Oversample I/O 0x →Output control" in the AS I/O configuration	0	Output cannot be reset by the oversample channel.
		1	Output can be reset by the oversample channel.
5	Output: Set "Oversample I/O 0x →Output control" in the AS I/O configuration	0	Output cannot be set by the oversample channel.
		1	Output can be set by the oversample channel.
6	Output default state: Clear "Oversample I/O 0x →Output default state" in the AS I/O configuration	0	Output not cleared by default
		1	Output cleared by default
7	Output default state: Set "Oversample I/O 0x →Output default state" in the AS I/O configuration	0	Output not set by default
		1	Output set by default

4.16.5.11.10.12 Oversample register - Configuration

Name:
OversampleEnable
OversampleOutputValidate

This register can be used to configure oversampling and the copy procedure for the output buffer.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	OversampleEnable	0	Disables oversampling (with the next reference cycle)
		1	Enables oversampling (with the next reference cycle)
1	OversampleOutputValidate	0	Disable the copy procedure to the output control buffer.
		1	Enables the copy procedure to the output control buffer. • Used to synchronize the oversampling procedure at startup. • This makes it possible to prevent new data from being transferred to the 4.16.4.11.10.15 "OversampleOutput0NSample" registers in each X2X cycle.
2 - 7	Reserved	-	

4.16.5.11.10.13 "OversampleOutputCycle" register

Name:
OversampleOutputCycle

When absolute addressing of the output control buffer is being used, this register specifies the address from which the new output sample data should be copied to the output control buffer.

Data type	Value	Information
USINT	0 to 255	Address of the output control buffer

4.16.5.11.10.14 "OversampleSampleOffset" register

Name:
OversampleSampleOffset

When relative addressing of the output control buffer is being used, this register serves as the offset for the new output sample data. (Sample address at the time of the "reference cycle" + Offset = address to which the new output sample data is copied in the output control buffer).

Data type	Value	Information
USINT	0 to 255	Offset of output sample data

4.16.5.11.10.15 "OversampleOutputSample" register

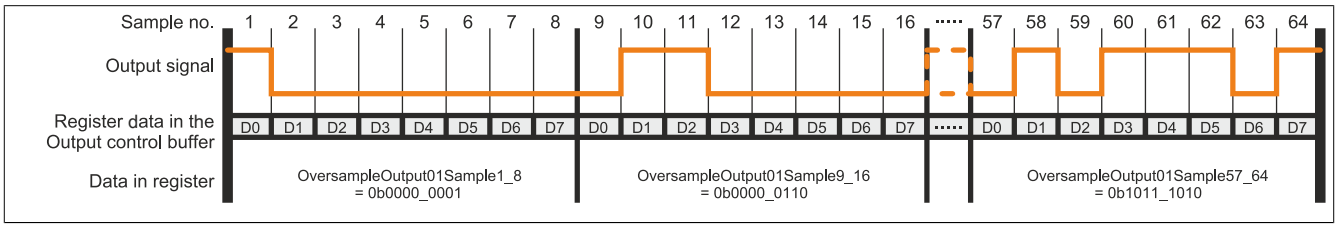
Name:
OversampleOutput01Sample1_8 to OversampleOutput04Sample1_8
OversampleOutput01Sample9_16 to OversampleOutput04Sample9_16
OversampleOutput01Sample17_24 to OversampleOutput04Sample17_24
OversampleOutput01Sample25_32 to OversampleOutput04Sample25_32
OversampleOutput01Sample33_40 to OversampleOutput04Sample33_40
OversampleOutput01Sample41_48 to OversampleOutput04Sample41_48
OversampleOutput01Sample49_56 to OversampleOutput04Sample49_56
OversampleOutput01Sample57_64 to OversampleOutput04Sample57_64

Contains the oversample output sample data. Up to 64 samples (8 bytes) for each oversample I/O channel can be synchronously transferred with a X2X cycle. This data is copied to the specified address (absolute or relative) in the output control buffer during the "output copy cycle". 1 bit of this data is then output during each "sample cycle" to the physical output that is assigned to the oversample I/O channel.
Bit 0 of "OversampleOutputSample8_1" is copied to the output control buffer first, meaning that it is the first bit that is output. "OversampleOutputSample64_57" bit 7 is the last bit to be output.

Data type	Value	Information
USINT	0 to 255	Output sample data

Example

Assignment of "OversampleOutputSample" register data to output signal



4.16.5.11.10.16 "OversampleInputTime" register

Name:
OversampleInputTime

This register contains the 2 low-order bytes of the X2X net time from the moment at which the oversample input data was referenced. This provides an easy way to accurately calculate the time of each individual input sample.

Data type	Value	Information
INT	-32,768 to 32,767	X2X net time of the input data

4.16.5.11.10.17 "OversampleInputCycle" register

Name:
OversampleInputCycle

This register provides the width of the input status buffer address for the input sample data.
Furthermore, the value in this register can be used for referencing an absolute addressing of the output control buffer.

Data type	Value	Information
USINT	0 to 255	Input status buffer address

4.16.5.11.10.18 "OversampleInputSample" register

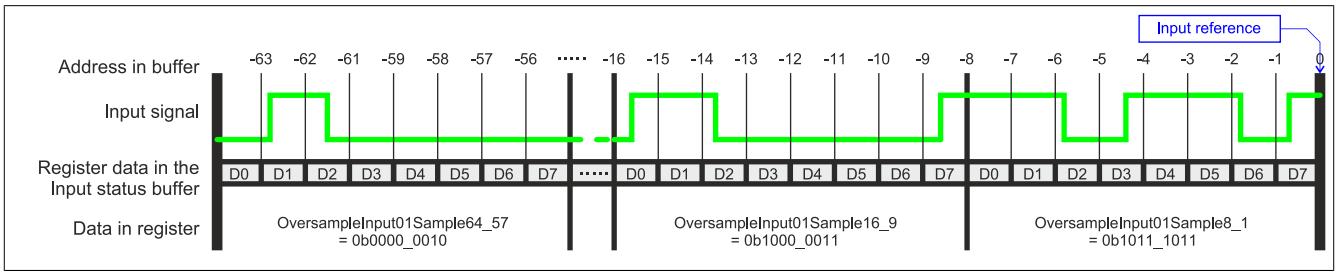
Name:
OversampleInput01Sample8_1 to OversampleInput04Sample8_1
OversampleInput01Sample16_9 to OversampleInput04Sample16_9
OversampleInput01Sample24_17 to OversampleInput04Sample24_17
OversampleInput01Sample32_25 to OversampleInput04Sample32_25
OversampleInput01Sample40_33 to OversampleInput04Sample40_33
OversampleInput01Sample48_41 to OversampleInput04Sample48_41
OversampleInput01Sample56_49 to OversampleInput04Sample56_49
OversampleInput01Sample64_57 to OversampleInput04Sample64_57

The data of the four oversample input status buffers are copied to this register at the time of "SI frame generation". A maximum of 64 samples (8 bytes) per oversample I/O channel can be synchronously retrieved from the oversample input status buffer with each X2X cycle.
The most recent input sample bit is stored in "OversampleInputSample8_1" bit 7. The oldest input sample is stored in "OversampleInputSample64_57" bit 0.

Data type	Value	Information
USINT	0 to 255	Input sample data

Example

Input signal and resulting data in "OversampleInputSample"



4.16.5.11.11 Edge detection

The module's edge detection function identifies edges with µs precision. The concept is based on a maximum of 4 units. A master and a slave edge can be configured for each unit.

At each master edge, the net time of the master edge and the net time of a previous slave edge (if present) are logged. A "master counter" and a "slave counter" can always be used to determine how many edges have been detected since the last X2X cycle.

4.16.5.11.11.1 "CfO_EdgeDetectPollCycleID" register

Name:
CfO_EdgeDetectPollCycleID
"Polling cycle" in the AS I/O configuration.

The source of the polling cycle can be configured in this register.

Information:

The polling cycle must be less than or equal to 255 µs. Setting the cycle > 255 µs causes an EdgeDetectError.

Data type	Value	Information
USINT	2	System timer The time set in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used for the polling cycle.
	3	Prescaled system timer The time set in the 4.16.4.11.7.3 "CfO_SystemCyclePrescaler" register is used for the polling cycle.

4.16.5.11.11.2 "CfO_EdgeDetectEventEnable" register

Name:
CfO_EdgeDetectEventEnable
"Edge detection mode" in the AS I/O configuration.

The bits in this register determine at which edges on the individual input channels an interrupt should be triggered for the edge detection.

In "event triggered" mode, the net time of each edge is recorded immediately an interrupt. However, an extremely large amount of interrupts within a short amount of time can prevent the module from being able to process any other operations in time!

In "polling" mode, only the net time of the first edge that occurs within a polling cycle is recorded. This ensures that the module is not overloaded by too many edges.

In the AS IO configuration, this register is initialized with 0x00000000 when "Edge detection mode = polling" and with 0xFFFFFFFF when "Edge detection mode = event triggered".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Physical input 1	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
...		...	
7	Physical input 8	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
8 - 15	Reserved	-	
16	Physical input 1	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
...		...	
23	Physical input 8	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
24 - 31	Reserved	-	

4.16.5.11.11.3 "CfO_EdgeDetectUnitMode" register

Name:
CfO_EdgeDetectUnit01Mode to CfO_EdgeDetectUnit04Mode
"Time base" in the AS I/O configuration.
"Slave edge" in the AS I/O configuration.
"Master edge" in the AS I/O configuration.

When using a "time base" with 1/8 µs resolution, keep in mind that the timestamps produced also have a resolution of exactly 1/8 µs. The respective conversions must be made for calculating in combination with the CPU system time or X2X net time.

Furthermore, synchronization jitter also plays a role when using the setting "time base = net time resolution 1/8 µs" (see: 4.16.4.11.4.3 "Synchronization jitter"). This means that exactly identical input edges can cause slight differences in the results. If a 100% exact 1/8 µs resolution is required, then the "local resolution 1/8 µs" must be used.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	"Time base" in the AS I/O configuration.	0	Local time 1/8 µs (AS: Local resolution 1/8 µs)
		1	Local time 1 µs (AS: Local resolution 1 µs)
		2	Net time 1/8 µs (AS: Net time resolution 1/8 µs)
		3	Net time 1 µs (AS: Net time resolution 1 µs)
2 - 5	Reserved	-	
6	"Slave edge" in the AS I/O configuration.	0	Disabled
		1	Enabled
7	"Master edge" in the AS I/O configuration.	0	Disabled
		1	Enabled

4.16.5.11.11.4 "CfO_EdgeDetectUnitLeading" register

Name:
CfO_EdgeDetectUnit01Leading to CfO_EdgeDetectUnit04Leading
"Slave leading" in the AS I/O configuration.

When a slave edge occurs, the current net time is always saved within the module. A FIFO is provided inside the module which always stores the last 256 slave stamps (even when a master edge occurs).

This value determines from which position the slave time should be retrieved from the FIFO when a master edge occurs. This can be used to measure average periodic signals over multiple cycles.

Data type	Value	Information
USINT	0 to 255	Position in the slave edge FIFO

4.16.5.11.11.5 "CfO_EdgeDetectUnitMaster" register

Name:
CfO_EdgeDetectUnit01Master to CfO_EdgeDetectUnit01Master
"Master edge" in the AS I/O configuration.

This register is used to select the source of the master edge for the respective "edge detection unit".

Data type	Value	Information
USINT	0	Rising edge on physical input 1
	...	...
	7	Rising edge on physical input 8
	16	Falling edge on physical input 1
	...	...
	23	Falling edge on physical input 8

4.16.5.11.11.6 "CfO_EdgeDetectUnitSlave" register

Name:
CfO_EdgeDetectUnit01Slave to CfO_EdgeDetectUnit04Slave
"Slave edge" in the AS I/O configuration.

This register is used to select the source of the slave edge for the respective "edge detection unit".

Data type	Value	Information
USINT	0	Rising edge on physical input 1
	...	...
	7	Rising edge on physical input 8
	16	Falling edge on physical input 1
	...	...
	23	Falling edge on physical input 8

4.16.5.11.11.7 "EdgeDetectMastercount" register

Name:
EdgeDetect01Mastercount to EdgeDetect04Mastercount

The reference pulses of the detected master edges are counted in this register.

Data type	Value	Information
SINT	-128 to 127	Number of detected master edges (8-bit)
INT	-32,768 to 32,767	Number of detected master edges (16-bit)

4.16.5.11.11.8 "EdgeDetectSlavecount" register

Name:
EdgeDetect01Slavecount to EdgeDetect04Slavecount

Counts the number of detected slave edges consecutively. The contents of this register are only updated when a master edge occurs. These counters can detect if multiple slave edges occur before a master edge.

Data type	Value	Information
SINT	-128 to 127	Number of detected slave edges (8-bit)
INT	-32,768 to 32,767	Number of detected slave edges (16-bit)

4.16.5.11.11.9 "EdgeDetectDifference" register

Name:
EdgeDetect01Difference to EdgeDetect04Difference

Contains the time difference between a master edge and the last slave edge addressed via "Slave leading".

Data type	Value	Information
INT	-32,768 to 32,767	Time difference between master/slave edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Time difference between master/slave edge (32-bit)

4.16.5.11.11.10 "EdgeDetectMastertime" register

Name:
EdgeDetect01Mastertime to EdgeDetect04Mastertime

The exact net time is copied in this register when a master edge occurs.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of master edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of master edge (32-bit)

4.16.5.11.11.11 "EdgeDetectSlavetime" register

Name:
EdgeDetect01Slavetime to EdgeDetect04Slavetime

When a master edge occurs, the exact net time of any slave edge that may have occurred prior to the master edge and addressed by "Slave leading" is copied in this register. If multiple slave edges occur before a master edge, then only the net time of the last edge that was not ignored by "Slave leading" is stored. The 4.16.4.11.11.8 "EdgeDetectSlavecount" register can be used to detect multiple edges.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the slave edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the slave edge (32-bit)

4.16.5.11.12 Movement functions

Encoder emulation can be used to generate up/down counters (direction/frequency) and ABR encoder signals. The movement function can be operated in 2 different modes:

- Position control mode
- Speed control mode

4.16.5.11.12.1 Position control mode

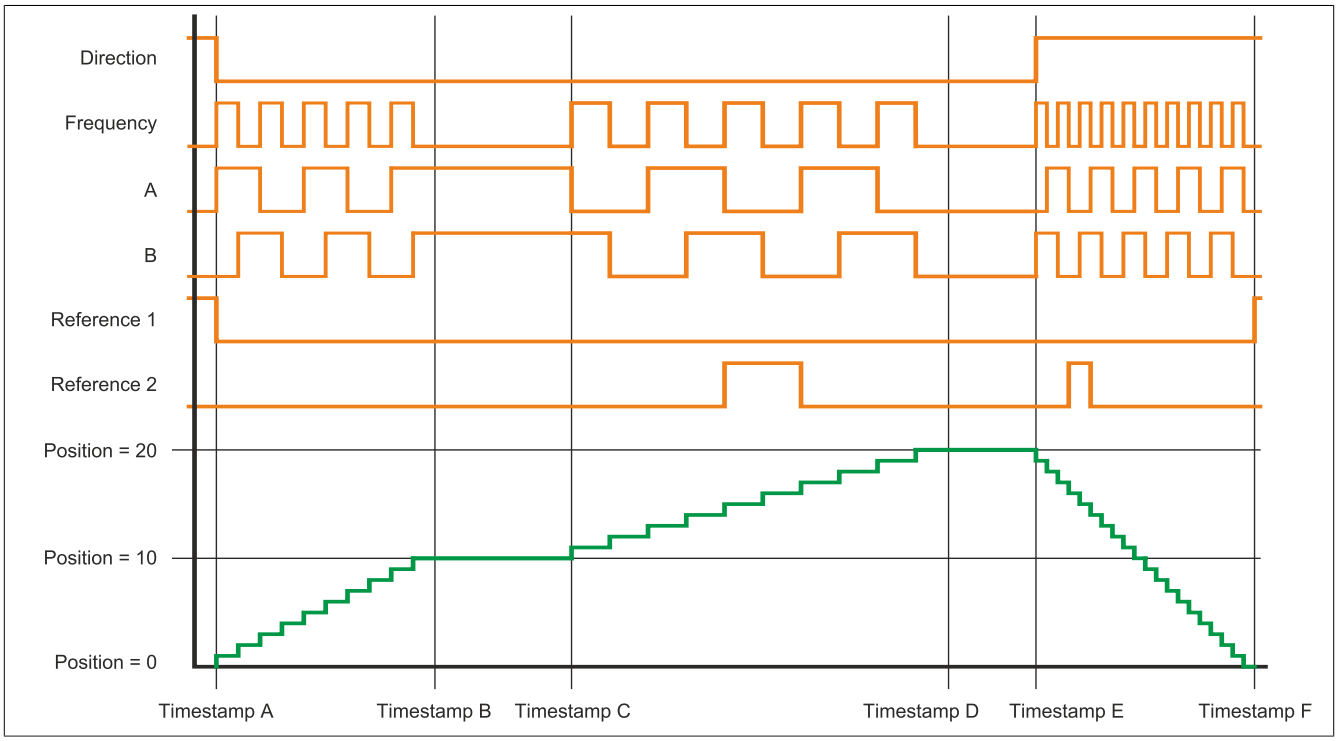
Each time the 4.16.4.11.12.18 "MovTargetTime" register changes, a new position setpoint is transferred from the 4.16.4.11.12.19 "MovPosition" register to the FIFO. The time/position data in the FIFO is then processed in such a manner that the positions are always reached at the time of the respective timestamps. This means that the module internally ensures that the positions are reached by the defined timestamps (number/frequency of the pulses is calculated automatically). The timestamps can be based on the X2X net time, the CPU's system time or the 4.16.4.11.12.21 "MovCurrentTime" register. Timestamps that are set in a manner that does not allow the required position change to be reached before the timestamp (output frequency of the pulse would exceed 4.16.5.11.12.5 "CfO_SpeedLimit") cause a MovMaxFrequencyViolation error.

Selected values for the example "Timing of movement":

Timestamp A = MovTimeValid + 40,000	Position for timestamp A = 0
Timestamp B = Timestamp A + 40.000	Position for timestamp B = 10
Timestamp C = Timestamp B + 25.000	Position for timestamp C = 10
Timestamp D = Timestamp C + 70,000	Position for timestamp D = 20
Timestamp E = Timestamp D + 15,000	Position for timestamp E = 20
Timestamp F = Timestamp E + 40,000	Position for timestamp F = 0

Configuration: Reference pulse 1 = Start position and margin, Start position = 0, Margin = 1

Configuration: Reference pulse 2 = Start and end position, Start position = 15, End position = 17



4.16.5.11.12.2 Speed control mode

In speed control mode, the application only specifies the speed setpoint. The module returns the current position in the 4.16.4.11.12.22 "MovPosition (32-bit)" register.

The internal timing is designed so that the value 16,777,216 (0x01000000) in the 4.16.4.11.12.20 "MovSpeed" register results in exactly one increment per "control period".

This creates the following relationship for 32-bit speed setpoints ("Data format of speed values = 32-bit):

$$MovSpeed = vOut * 2^{resol} * period$$

Unlike other registers, the 2 higher-value bytes of "MovSpeed (32-bit)" are set when the "MovSpeed (32-bit)" register is written. This creates the following relationship for the direct calculation with "MovSpeed (16-bit)"

$$MovSpeed = \frac{vOut * 2^{resol} * period}{2^{16}}$$

Variable	Description	Unit
MovSpeed	Value for "MovSpeed" register (16 or 32-bit)	
vOut	Desired output speed Each edge represents one increment (rising or falling).	Inc/s
resol	Value configured for the 4.16.4.11.12.13 "CfO_ResolSpeed" register	Bits
period	Value configured for the 4.16.4.11.12.11 "CfO_SpeedCycleTime_32Bit" register **Information:** **Must be set in µs in Automation Studio. The calculation is performed in s, however.**	s

4.16.5.11.12.3 "FifoSize" register

Name:
FifoSize
"Number of Fifo entries" in the AS I/O configuration.

Determines the size of the FIFO for MovTargetTime and MovTargetPosition. One timestamp and one position that should be reached by the timestamp can be transferred to the FIFO per X2X cycle.

Data type	Value	Information
USINT	0	FIFO disabled
	3	8 entries (2^3)
	4	16 entries (2^4)
	5	32 entries (2^5)
	6	64 entries (2^6)
	7	128 entries (2^7)
	8	256 entries (2^8)

4.16.5.11.12.4 "CfO_Mode" register

Name:
CfO_Mode

This register can be used to configure the mode of the movement functions.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Must be enabled when working without timestamps. Enabled in AS if: • Movement = "speed control" • Movement = "position control and "data format / mode of preset time = local time"	0	Disabled
		1	Enabled
1	If this function is enabled, then a new positioning movement is triggered as soon as the value changes in the 4.16.4.11.12.19 "MovPosition" register. Enabled in AS if: • Movement = "position control and "data format / mode of preset time = local time"	0	No position control (speed control)
		1	Position control enabled (position control)
2	Reference mode 1 "Configuration reference pulse 1" in the AS I/O configuration.	0	Start/end position
		1	Start position and span
3	Reference mode 2 "Configuration reference pulse 1" in the AS I/O configuration.	0	Start/end position
		1	Start position and span
4 - 7	Reserved	-	

4.16.5.11.12.5 "CfO_SpeedLimit" register

Name:
CfO_SpeedLimit
"Max. movement frequency" in the AS I/O configuration.

Configures the maximum permitted output frequency and the maximum internal computing frequency. The higher internal computing frequencies of 500 kHz and 2, 4, 8, 16, 32 and 64 MHz can only be achieved by configuring n bits as decimal places (see "CfO_ResolPosition" register).

Data type	Value	Max. increment frequency	Max. frequency for frequency output channel	Max. frequency for A/B output channel
USINT	253	64 MHz	125 kHz	625 kHz
	254	32 MHz		
	255	16 MHz		
	0	8 MHz		
	1	4 MHz		
	2	2 MHz		
	3	1 MHz		
	4	500 kHz		
	5	250 kHz (default)		
	6	125 kHz	625 kHz	3125 kHz

Information:

In "position control" mode, the increment frequencies 16, 32 and 64 MHz are not permitted to be used when a 29-bit timestamp is set (see 4.16.4.11.12.7 "CfO_TimeStampRange" register) due to an internal range violation.

4.16.5.11.12.6 "CfO_FormatAdjust" register

Name:
CfO_FormatAdjust

This register determines the number of absolute bits that can be output on the signal output (With a direction/frequency signal, the bit with the lowest value can be output directly on the frequency output. With an AB signal, 2 bits are possible.)

Data type	Value	Information
USINT	1 to 2	Number of absolute bits (AS default = 1)

4.16.5.11.12.7 "CfO_TimeStampRange" register

Name:
CfO_TimeStampRange
"Data format/mode of target time" in the AS I/O configuration.

The width of the transferred timestamp data in the module is configured in this register.

Information:

Because the module uses an internal resolution of 1/8 µs, timestamp data is processed internally at a maximum width of 29 bits.

Data type	Value	Information
SINT	16	16-bit timestamp ("16-bit" selected in the AS I/O configuration)
	24	24-bit timestamp ("local time" or "speed control" movement selected in the AS I/O configuration)
	29	29-bit timestamp ("29-bit" selected in the AS I/O configuration)

4.16.5.11.12.8 "CfO_PositionsRange" register

Name:
CfO_PositionsRange
"Target position range" in the AS I/O configuration.

The number of bits for position control are configured in this register. The "PositionRange" must be reduced if, for example, the movement function should follow the absolute value of a 12-bit SSI encoder. In this case, the bit width of the movement position also has to be limited to the number of bits of the encoder, or else the movement position would not also overrun if the encoder were to overrun. In this case, the module would attempt (in the opposite direction) to reach the position of an encoder that had just overrun.

Example

The 12-bit SSI encoder overruns from 2047 to -2048. The module would generate 4096 negative increments if more than 12 bits were defined for "CfO_PositionRange" in order to reach position -2048 from the position 2047.

Information:

If the 16-bit value of the 4.16.4.11.12.22 "MovPosition" register is used, then the bit width of the position must also be limited to ≤16 bits or else this would also result in incorrect overrun behavior.

Data type	Value	Information
SINT	8 to 32	Number of bits for position control

4.16.5.11.12.9 "CfO_ReferenceRange" register

Name:
CfO_Reference0Range to CfO_Reference1Range
"Reference#1 range" to "Reference#2 range" in the AS I/O configuration.

This register determines the number of bits that can be used for the reference position comparison. This makes it possible to generate a reference pulse every 2^n increments.

Information:

The number of bits set in this register must not be higher than the number of bits set for 4.16.5.11.12.14 "MovReferenceStart" and 4.16.5.11.12.15 "MovReferenceStopMargin".

Data type	Value	Information
SINT	4 to 32	Number of bits for position comparison

4.16.5.11.12.10 "CfO_TimeStampDelay" register

Name:
CfO_TimeStampDelay

All timestamps are delayed by the value defined in this register.

Data type	Value	Information
DINT	0 to 1000000	Timestamp delay in µs

4.16.5.11.12.11 "CfO_SpeedCycleTime_32Bit" register

Name:
CfO_SpeedCycleTime_32Bit
"Control period" in the AS I/O configuration.

The control period for "speed control" mode can be set in this register in steps of 1/8 µs.

Information:

The value defined in the AS I/O configuration under "Control period" is automatically multiplied by 8 and then used as CfO_SpeedCycleTime_32bit.

Data type	Value	Information
UDINT	400 to 40000	Control period for "speed control" mode

4.16.5.11.12.12 "CfO_ResolPosition" register

Name:
CfO_ResolPosition
"Position resolution" in the AS I/O configuration.

This register contains the number of bits as decimal place for jitter reduction. Internally, the module adds 2^n (n = number of decimal places) to the frequency, which results in edge switching times with a higher resolution. The output switching frequency is not increased from a hardware perspective, but the edge timing is more precise.

Data type	Value	Information
SINT	0	Default, no decimal places
	1 to 14	Selection of bits as decimal places

Information:

Keep in mind that each configured decimal place also limits the maximum number range by that number of bits.

For example: 0 decimal places →maximum position range = 29 bits

3 decimal places →maximum position range = 26 bits

Also keep in mind that the 4.16.5.11.12.5 "CfO_SpeedLimit" register must be adjusted for these higher computing frequencies based on the number of configured decimal places.

4.16.5.11.12.13 "CfO_ResolSpeed" register

Name:
CfO_ResolSpeed
"Speed resolution" in the AS I/O configuration.

This register contains the number of bits as decimal place for jitter reduction of the speed value. Internally, the module adds 2^n (n = number of decimal places) to the frequency, which results in edge speed values with a higher resolution.

Due to the bit limitation, a 16 or 32-bit speed value is set in the AS I/O configuration. Since the internal calculation is always based on 32-bit, when configured to 16-bit an offset of 16 must always be added to the desired number of decimal places.

Data type	Value	Information
SINT	0 to 31	Selection of bits as decimal places
	24	Standard

Information:

Keep in mind that each configured decimal place also limits the maximum number range by that number of bits.

4.16.5.11.12.14 "CfO_ReferenceStart / MovReferenceStart" register

Name:
CfO_Reference0Start to CfO_Reference1Start
MovReference1Start to MovReference2Start
"Start position" in the AS I/O configuration

The start position for the reference pulse is shown in these registers.

In the positive direction, the output (R) is set when the start position is reached. In negative direction, the output is reset as soon as the value falls below the start position value.

Data type	Value	Information
INT	-32,768 to 32,767	Start position (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Start position (32-bit)

4.16.5.11.12.15 "CfO_ReferenceStopMargin / MovReferenceStopMargin" register

Name:
CfO_Reference0StopMargin to CfO_Reference1StopMargin
MovReference1StopMargin to MovReference2StopMargin
"End position or margin" in the AS I/O configuration

The end position or the margin in which the reference pulse is output is configured in these registers.

If "Reference mode x = Start/end position" is used in the 4.16.5.11.12.4 "CfO_Mode" register, then the output (R) is reset when the end position is reached in the positive direction. In the negative direction, the output is set as soon as the value falls below the end position value.

When "Reference mode x = Start position and span", the content of this register is added to the start position and the resulting sum is used as the end position.

Data type	Value	Information
INT	-32,768 to 32,767	End position (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	End position (32-bit)

4.16.5.11.12.16 "CfO_AccelDataInit / MovAcceleration" register

Name:
CfO_AccelDataInit
MovAcceleration
"Acceleration value" in the AS I/O configuration.

This register shows the acceleration value in increments per control period².

- 32-bit: 16777216 (0x01000000) corresponds to 1 increment per control period²
- 16-bit: 256 (0x0100) corresponds to 1 increment per control period²

Data type	Value	Information
UINT	0 to 65,535	Acceleration value (16-bit)
UDINT	0 to 4,294,967,296	Acceleration value (32-bit)

4.16.5.11.12.17 "MovementControl" register

Name:
MovPosEnable
MovSpeedEnable

This register can be used to enable position and speed control.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	MovPosEnable	0	Position control disabled
		1	Position control enabled
1	MovSpeedEnable	0	Speed control disabled
		1	Speed control enabled
2 - 6	Reserved	-	
7	Movement reset (immediate stop)	0	Passive reset
		1	Active reset

4.16.5.11.12.18 "MovTargetTime" register

Name:
MovTargetTime

Timestamp data is shown in this register.Each time this register changes, the new position data (MovTargetPosition) and timestamp data are transferred to the FIFO. When "MovSpeedEnable = True", the module calculates the output speed (frequency) so that the "MovTargetPosition" is reached at "MovTargetTime".

Data type	Value	Information
INT	-32,768 to 32,767	Timestamp (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Timestamp (32-bit)

Information:

Only 29 bits of this register are processed internally.

4.16.5.11.12.19 "MovTargetPosition" register

Name:
MovTargetPosition

Position data is shown in this register.

Data type	Value	Information
INT	-32,768 to 32,767	Position (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Position (32-bit)

4.16.5.11.12.20 "MovSpeed" register

Name:
MovSpeed

This register shows the speed setpoint for "speed control" mode in increments per control period.

- 32-bit: 16,777,216 (0x01000000) corresponds to 1 increment per control period
- 16-bit: 256 (0x0100) corresponds to 1 increment per control period

Data type	Value	Information
INT	-32,768 to 32,767	Speed setpoint (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Speed setpoint (32-bit)

4.16.5.11.12.21 "MovTimeValid" register

Name:
MovTimeValid

This register displays the net time of the current position.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the current position (16-bit).
DINT	-2,147,483,648 to 2,147,483,647	Net time of the current position (32-bit)

4.16.5.11.12.22 "MovPosition" register

Name:
MovPosition

This register shows the current position.

Data type	Value	Information
INT	-32,768 to 32,767	Current position (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Current position (32-bit)

4.16.5.11.13 Synchronous serial interface (SSI)

The synchronous serial interface makes it possible to receive data from SSI absolute encoders.

Two lines are needed for data exchange:

SSI clock:	Generated by the module on output 7 (if configured).
SSI data:	A data bit is transferred from the encoder to the module with each clock pulse (input 5 can be used as the SSI input).

4.16.5.11.13.1 SSI transfer process

When the first edge occurs on the SSI clock, a monoflop is triggered in the encoder and the current parallel pending value is latched to the offset register (the low level of the monoflop prevents other values from being added to the offset register during data transfer).

The highest value bit is then transferred to the module when the next edge occurs.

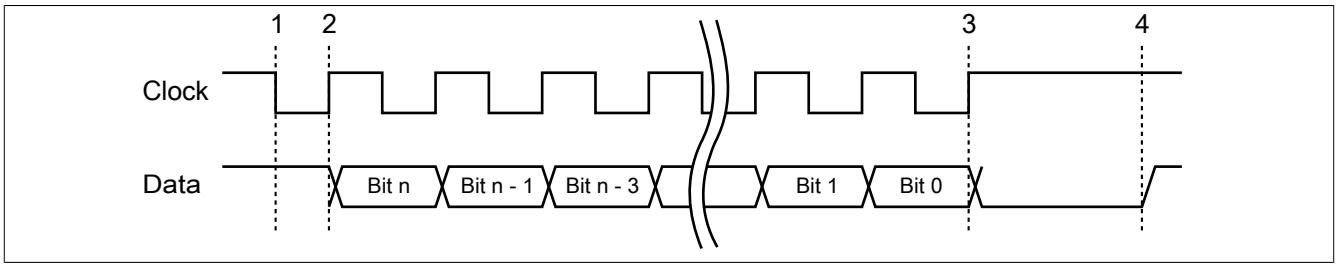
With each subsequent cycle, the next lowest bit is transferred. The cycles re-trigger the monoflop constantly so that its output prevents new data from being accepted.

The sequence of cycles stops once the number of data bits defined in the 4.16.4.11.13.4 "CfO_DataBits" register has been received.

The monoflop is no longer triggered. After a certain amount of time has passed (depending on the encoder), the monoflop's output re-assumes the output level, thereby enabling parallel data to be accepted once again in the encoder's offset register.

When the "Monoflop check" is run, the data line is queried for the configured level before a new transfer is started. This makes it possible to ensure that the monoflop really has reset before a new transfer is started.

Transfer to synchronous serial interface



Measurement value processing

1 Starting bit ... Stores the measurement value
2 Output of first data bit
3 All data bits are transferred, monostable multivibrator time starts counting down.
4 Monostable multivibrator returns to its initial state. A new transfer can be started.

4.16.5.11.13.2 "CfO_CycleSelect" register

Name:
CfO_CycleSelect
"Update cycle" in the AS I/O configuration.

SSI transfer is started at the update cycle. The clock sequence is generated on the SSI clock output. The first edge of the clock signal triggers the monoflop in the encoder and latches the current position. At the same time, the current net time is also recorded in the 4.16.4.11.13.6 "SSITimeValid" register. As soon as all bits have been transferred via the SSI, the position is passed on with the next "SIframeGenCycle" via the X2X Link. A SSICycleTimeViolation error is reported if the SSI transfer is not completed within the SSI update cycle (e.g. system timer as update cycle). The SSI transfer is still fully completed and then started again with the next update cycle.

Data type	Value	Information
USINT	2	System timer
	3	Prescaled system timer
	10	AOAI
	14	SOSI

4.16.5.11.13.3 "CfO_PhysicalMode" register

Name:
CfO_PhysicalMode
"Parity bit" in the AS I/O configuration
"Monoflop check" in the AS I/O configuration
"Data format" in the AS I/O configuration
"Clock frequency" in the AS I/O configuration

The SSI interface is configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	"Parity bit" in the AS I/O configuration.[1)]	00	Disabled
		01	Even parity
		10	Uneven parity
		11	Ignored (the parity bit is transferred, but not evaluated).
2 - 3	"Monoflop check" in the AS I/O configuration.[2)]	00	Disabled
		01	Low level (data signal is checked for low level after the monoflop has reset).
		10	High level (data signal is checked for high level after the monoflop has reset).
		11	Ignored (the necessary cycle is triggered, but not evaluated).
4	"Data format" in the AS I/O configuration.	0	Encoder with binary output
		1	Encoder with Gray Code. The module converts the position data into binary format.
5	Reserved	-	
6 - 7	"Clock frequency" in the AS I/O configuration.	00 to 10	Not permitted
		11	125 kHz

1) If the parity bit does not match, then a SSIParityError is generated and the position data is not accepted in the "SSIPosition" register.
2) A new SSI transfer is not started until the data signal has assumed the level defined for the "monoflop check" after the transfer. This then triggers the error SSICycleTimeViolation.

4.16.5.11.13.4 "CfO_DataBits" register

Name:
CfO_DataBits
"Valid SSI bit length" in the AS I/O configuration.

Determines the number of valid data bits to be transferred via the SSI. The valid data bits are used for the SSI-Position.

Data type	Value	Information
USINT	1 to 32	Number of valid data bits

4.16.5.11.13.5 "CfO_NullBits" register

Name:
CfO_NullBits
"Leading zero bits" in the AS I/O configuration.

This register can be used to configure the number of leading zero bits. The leading zero bits can be required before the valid data bits.

Data type	Value	Information
USINT	0 to 31	Number of leading zero bits

4.16.5.11.13.6 "SSITimeValid" register

Name:
SSITimeValid

This register displays the net time of the current position.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the current position (16-bit).
DINT	-2,147,483,648 to 2,147,483,647	Net time of the current position (32-bit)

4.16.5.11.13.7 "SSITimeChanged" register

Name:
SSITimeChanged

The net time of the last position change is shown in this register.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the last position change (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the last position change (32-bit)

4.16.5.11.13.8 "SSIPosition" register

Name:
SSIPosition

This register shows the current position sent via the SSI interface.

Data type	Value	Information
INT	-32,768 to 32,767	Current position (16-bit)
UDINT	0 to 4,294,967,295	Current position (32-bit)
DINT	-2,147,483,648 to 2,147,483,647	

4.16.5.11.14 Counter

The universal counter pair can be used in 3 different modes. Here, signals up to 100kHz are reliably measured. Up to 4 latch inputs can be configured in all modes. Enabled latch inputs are negated if necessary and connected with a logical AND operation for a latch condition. If the latch condition is met, the current counter value is stored in a separate register.

Inputs

The physical inputs have fixed assignments based on the respective mode.

Mode	Input 1	Input 2	Input 5	Input 6
Edge counters	Counter input for counter 1 Latch input 1	Counter input for counter 2 Latch input 2	- Latch input 3	- Latch input 4
Up/down counter	Counting direction Latch input 1	Counter frequency Latch input 2	- Latch input 3	- Latch input 4
Incremental encoder	A Latch input 1	B Latch input 2	- Latch input 3	- Latch input 4

Latch function

As latch inputs, inputs 1, 2, 5, and 6 can each be polled to determine if they have a HIGH or LOW level.

In "Latch mode = continuous", the counters are latched once as soon as "LatchEnable = TRUE" and the configured latch condition is met. If the latch condition is met again, then the counter value is also latched again. (i.e. One latch event is triggered with each rising edge on the output of the AND operation of all latch inputs).

In "Latch mode = single", the counters are latched once as soon as "LatchEnable = TRUE" and the configured latch condition is met. If the latch condition is met again, then the counter value is not automatically copied again. Another latch event can only be processed after "LatchEnable = False" and then "LatchEnable = True" again.

4.16.5.11.14.1 "CfO_CounterCycleSelect" register

Name:
CfO_CounterCycleSelect
"Update cycle" in the AS I/O configuration.

The update cycle for the counter values is configured in this register.

Information:

The maximum counting frequency depends on the cycle. The module can process a maximum of 200 increments (edges) within a counter cycle.

Data type	Value	Information
USINT	2	System timer
	3	Prescaled system timer
	10	AOAI time of X2X cycle
	14	SOSI time of X2X cycle

4.16.5.11.14.2 "CfO_CounterMode" register

Name:
CfO_CounterMode
"Counter mode" in the AS I/O configuration.

The counter mode is configured in this register.

Data type	Value	Information
USINT	0	Edge counters In this mode, the two counters are used as edge counters. The counter input of counter 1 is linked permanently to input 1 and the counter input of the second counter is linked permanently to input 2. Both rising as well as falling edges are counted.
	2	Up/down counter The up/down counter works according to the direction/frequency principle. Input 1 determines the counting direction (LOW = positive, HIGH = negative), input 2 serves as the counting frequency input. Both rising as well as falling edges on the counting frequency input are counted.
	3	Incremental encoder (AB counter) When configured as an AB counter, input 1 serves as the A channel and input 2 as the B channel. All edges are evaluated (4x evaluation).

4.16.5.11.14.3 "CfO_LatchMode" register

Name:
CfO_LatchMode
"Latch mode" in the AS I/O configuration.

The latch mode is configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	LatchMode	0	Single shot
		1	Continuous
1 - 7	Reserved	-	

4.16.5.11.14.4 "CfO_LatchComparator" register

Name:
CfO_LatchComparator

"Latch level channel 0x" in the AS I/O configuration.

The latch comparators for the counter inputs are configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparison level for latch comparator on input 1	0	LOW
		1	HIGH
1	Comparison level for latch comparator on input 2	0	LOW
		1	HIGH
2	Comparison level for latch comparator on input 5	0	LOW
		1	HIGH
3	Comparison level for latch comparator on input 6	0	LOW
		1	HIGH
4	Enable latch comparator on input 1	0	Disabled
		1	Enabled
5	Enable latch comparator on input 2	0	Disabled
		1	Enabled
6	Enable latch comparator on input 5	0	Disabled
		1	Enabled
7	Enable latch comparator on input 6	0	Disabled
		1	Enabled

4.16.5.11.14.5 "CounterControl" register

Name:
CounterReset
LatchEnable

This register can be used to clear counter values or enable the latch.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	CounterReset	0	No action
		1	Delete counter
1	LatchEnable	0	Disabled
		1	Enabled
2 - 7	Reserved	-	

4.16.5.11.14.6 "LatchCount" register

Name:
LatchCount

Latch events are counted in this register. This counter can be used to detect whether a new value has been latched.

Data type	Value	Information
SINT	-128 to 127	Latch counter

4.16.5.11.14.7 "CounterTimeValid" register

Name:
CounterTimeValid

This register displays the X2X net time of the current counter value.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the current counter value (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the current counter value (32-bit)

4.16.5.11.14.8 "CounterTimeChanged" register

Name:
Counter01TimeChanged to Counter02TimeChanged

The net time of the last change to the respective counter is shown in this register.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the last change to the respective counter (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the last change to the respective counter (32-bit)

4.16.5.11.14.9 "CounterValue" register

Name:
CounterValue01 to CounterValue02

This register shows the current value of the respective counter.

Data type	Value	Information
INT	-32,768 to 32,767	Value of the respective counter (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Value of the respective counter (32-bit)

4.16.5.11.14.10 "CounterLatch" register

Name:
CounterLatch01 to CounterLatch02

As soon as the latch conditions defined in the 4.16.5.11.14.4 "CfO_LatchComparator" register have been met, the contents of the respective CounterValue register are copied to this register.

Data type	Value	Information
INT	-32,768 to 32,767	Latch counter (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Latch counter (32-bit)

4.16.5.11.14.11 "CounterRel" register

Name:
CounterRel01 to CounterRel02

The value of the respective counter, relative to the last latch of the respective counter is calculated in this register.

Data type	Value	Information
INT	-32,768 to 32,767	Counter value relative to the last latch (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Counter value relative to the last latch (32-bit)

4.16.5.11.15 Minimum X2X cycle time

The minimum X2X cycle time is strongly dependent on the configured functions and the resulting load on the module. In general, a "Fast reaction" setting and a very short system cycle (50 µs) have a negative influence on the minimum X2X cycle time. This can lead to errors when the X2X cycle time is short.

4.16.6 X20DS1828

4.16.6.1 General information

The module is equipped with 1 HIPERFACE encoder interface. This module can be used to evaluate encoders installed in motors from other manufacturers as well as encoders for external axes (encoders that sample any machine movement). The input signals are monitored. This makes it possible to detect open or shorted lines as well as encoder supply failures.

- HIPERFACE encoder interface
- Encoder input monitoring
- 11 VDC and GND for encoder supply
- NetTime function: Timestamp for position

HIPERFACE

HIPERFACE is a standard developed by Max Stegmann GmbH (www.stegmann.de), which like EnDat incorporates the advantages of absolute and incremental position measurement while also offering a read/write parameter memory in the encoder. With absolute position measurement (the absolute position is sampled serially), a homing procedure for referencing is usually not required. Where necessary, a multi-turn encoder should be installed. To reduce costs, a single-turn encoder and a reference switch can also be used. In this case, a homing procedure must be carried out.

The incremental process allows the short deceleration periods necessary for position measurement when using drives with highly dynamic characteristics. With the sinusoidal incremental signal and the fine resolution in the HIPERFACE module, a very high positioning resolution is achieved in spite of the moderate signal frequencies used.

NetTime position timestamp

Highly dynamic positioning tasks require not only the position value, but also the exact time at which the position was determined. The module has a NetTime function for this, which adds a timestamp to the recorded position with microsecond accuracy.

The module provides the PLC with the position value and timestamp as absolute time value. The NetTime mechanisms ensure that the PLC NetTime clock and the local NetTime clock on the module have exactly the same absolute time at all times.

4.16.6.2 Order data

Model number	Short description	Figure
	Digital signal processing and preparation	
X20DS1828	X20 digital signal module, 1 HIPERFACE interface, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 361: X20DS1828 - Order data

4.16.6.3 Technical data

Product ID	X20DS1828
Short description	
I/O module	1x HIPERFACE interface
General information	
B&R ID code	0xAEC7
Status indicators	Counting direction, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Counting direction	Yes, using status LED
Power consumption	
Bus	0.01 W
Internal I/O	1.3 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Encoder inputs	
Angular position resolution	13-bit, with a 1 V_{SS} signal
Encoder monitoring	Yes
Max. encoder cable length	10 m
Sine/Cosine inputs	
Signal transmission	Differential signals, symmetrical
Signal frequency	DC up to 200 kHz
Differential voltage	1 V_{SS}
Common-mode voltage	Max. ±10 V
Terminating resistor	120 Ω
Encoder supply	
Output voltage	11 V
Load capability	150 mA
Protective measures	
Overload protection	Yes
Short circuit protection	Yes
Parameter channel (RS485)	
Signal transmission	5 VDC differential signal, EiA RS-485 standard
Transmission status	See HIPERFACE specification
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 362: X20DS1828 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.16.6.4 LED status indicators

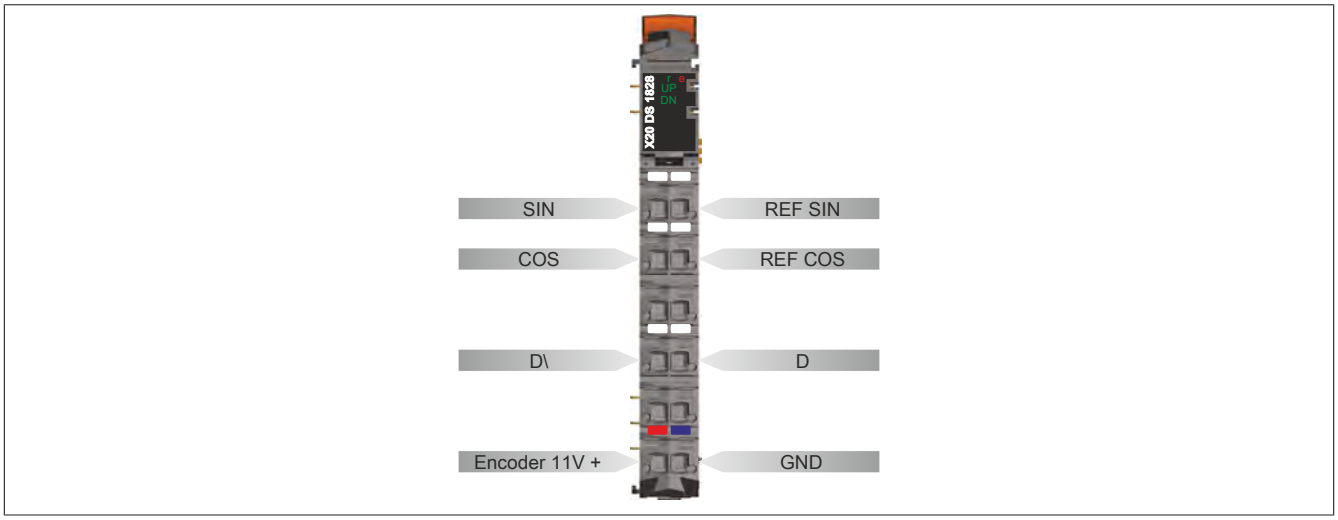
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset state. Possible cause: • Encoder supply error
			Single flash	I/O error - Possible causes: • Sine/Cosine relative position error (open line) • Sine/Cosine absolute position error (reference)
			Double flash	System error. Possible causes: • HIPERFACE communication error
			Triple flash	I/O error and system error
			Single flash, inverted	Error or reset state and I/O error
			Double flash, inverted	Error or reset state and system error
			Triple flash, inverted	Error or reset state, I/O error and system error
	UP	Green	On	The "UP/DN" LEDs are lit depending on the rotational direction and the speed of the connected encoder. The "UP" LED indicates when the encoder position changes in the positive direction.
	DN	Green	On	The "DN" LED indicates when the encoder position changes in the negative direction.

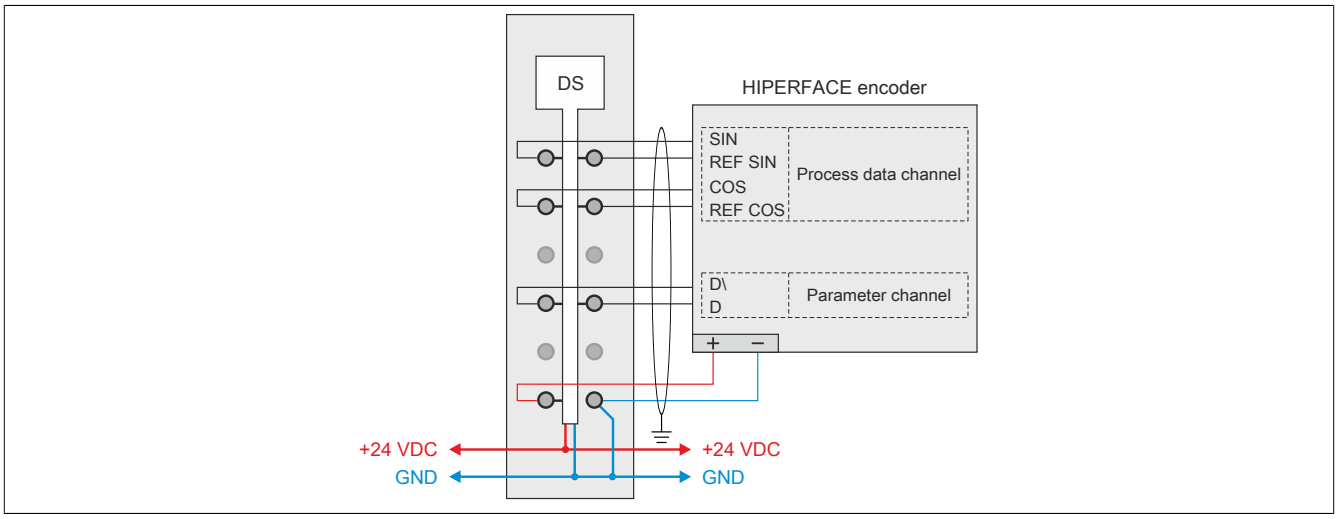
1) Depending on the configuration, a firmware update can take up to several minutes.

4.16.6.5 Pinout

Shielded cables must be used for all signal lines.

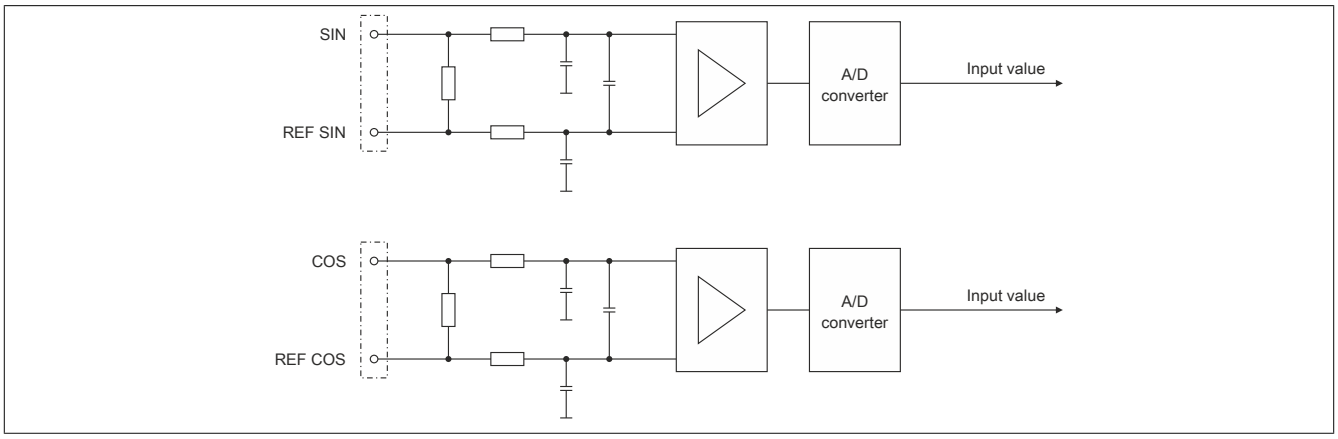


4.16.6.6 Connection example

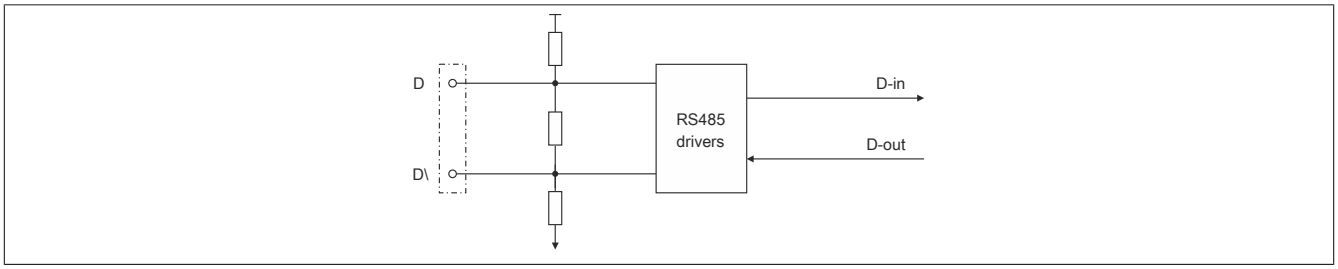


4.16.6.7 Input circuit diagram

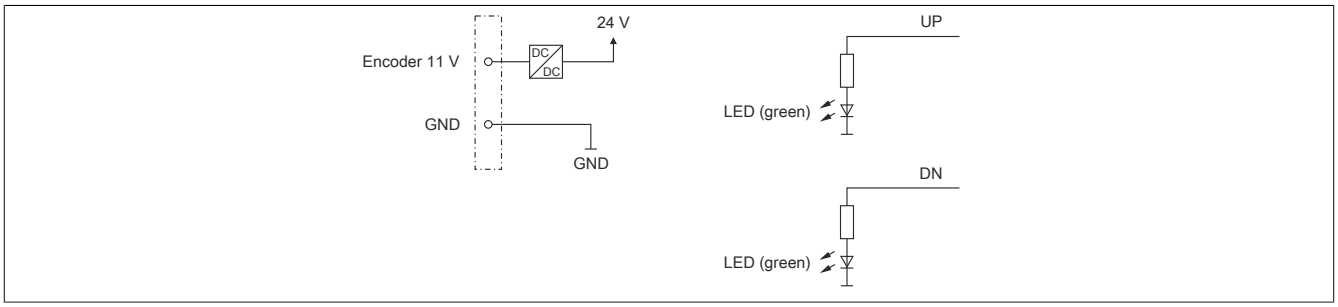
4.16.6.7.1 Diagram for the process data channel (sine-cosine track)



4.16.6.7.2 Circuit diagram for the parameter channel (RS485 interface)



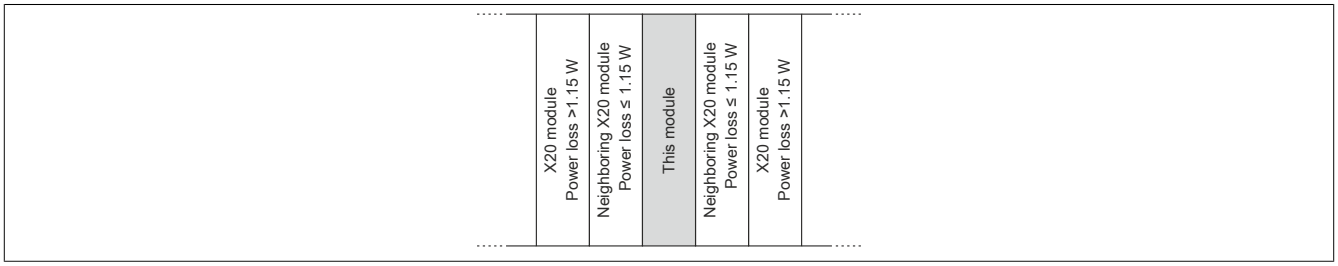
4.16.6.7.3 Circuit diagram for the encoder supply and LEDs



4.16.6.8 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.16.6.9 Register description

4.16.6.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.16.6.9.2 Register overview - Function model 0 (standard)

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module configuration						
513	CfO_SIframeGenID	USINT				•
Basic functions						
683	SDCLifeCount	SINT	•			
1236	PositionHW	UDINT	•			
1244	PositionLW	UDINT	•			
	Position	DINT				
1228	PosTime (32-bit)	DINT	•			
1230	PosTime (16-bit)	INT	•			
1219	PosCycle	SINT	•			
Error management						
387	ErrorEnableID_0F08	USINT				•
259	ErrorInfo	USINT	•			
	EncoderSupplyError	Bit 0				
	VssCheckError	Bit 2				
	PositionError	Bit 3				
	HfComError	Bit 4				
	HfRefWarning	Bit 5				
323	AckErrorInfo	USINT			•	
	AckEncoderSupplyError	Bit 0				
	AckVssCheckError	Bit 2				
	AckPositionError	Bit 3				
	AckHfComError	Bit 4				
	AckHfRefWarning	Bit 5				
2116	HfErrorCode	UDINT	•			
Sin/Cos - Configuration						
1025	SinCosEnable	USINT				•
1027	SinCosRefSource	USINT				•
1034	SinCosVssMin	UINT				•
1038	SinCosVssMax	UINT				•
1044	SinCosQuitTime	UDINT				•
HIPERFACE - Configuration						
2049	HfMode	USINT				•
2053	HfParity	USINT				•
2055	HfCharTimeout	USINT				•
2060	HfBaud	UDINT				•
2068	HfRepressErrTime	UDINT				•
2073	HfRefAdr	USINT				•
2075	HfRefWidth	USINT				•
HIPERFACE - Identification						
2561	HfAdrIdent	USINT				•
2563	HfSelectionIdent	USINT				•
2631	HfIdentOk	USINT		•		
2688	HfRs485Settings	USINT		•		
2689	HfEncoderType	USINT		•		
2690	HfEepromSize	USINT		•		
2691	HfOptionFlags	USINT		•		
2692	HfFreeMemory	USINT		•		
2693	HfDataFields	USINT		•		
2693 + N	HfExtByte0N (index N = 1 to 10)	USINT		•		
HIPERFACE - Additional positions						
2817	AddPosAdr01	USINT				•
2887	AddPosOk (byte)	USINT	•			
	AddPosOk01	Bit 0				
	AddPosOk02	Bit 1				
2956	AddPosition01	DINT	•			
2958	AddPosition01	INT	•			
2948	AddPosTime01	DINT	•			
2950	AddPosTime01	INT	•			
2825	AddPosAdr02	USINT				•

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2972	AddPosition02	DINT	●			
2974	AddPosition02	INT	●			
2964	AddPosTime02	DINT	●			
2966	AddPosTime02	INT	●			
HIPERFACE - Additional analog values						
3065 + N * 8	AnalogAdrCh0N (index N = 1 to 4)	USINT				●
3067 + N * 8	AnalogCh0N (index N = 1 to 4)	USINT				●
3143	AnalogChOk (byte)	USINT	●			
	AnalogChOk01	Bit 0				
	...	...				
	AnalogChOk04	Bit 3				
3194 + N * 16	AnalogChValue0N (index N = 1 to 4)	(U)INT	●			
3188 + N * 16	AnalogChTime0N (index N = 1 to 4) (32-bit)	DINT	●			
3190 + N * 16	AnalogChTime0N (index N = 1 to 4) (16-bit)	INT	●			
Flatstream mode						
2305	OutputMTU	USINT				●
2307	InputMTU	USINT				●
2309	FlatStreamMode	USINT				●
2311	Forward	USINT				●
2316	ForwardDelay	UINT				●
2368	InputSequence	USINT	●			
2368 + N	RxByteN (index N = 1 to 15)	USINT	●			
2400	OutputSequence	USINT			●	
2400 + N	TxByteN (index N = 1 to 15)	USINT			●	

4.16.6.9.3 Register overview - Function model 254 (bus controller)

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Module configuration							
513	-	CfO_SIframeGenID	USINT				●
Basic functions							
1236	0	PositionHW	UDINT	●			
1244	4	PositionLW	UDINT	●			
1219	15	PosCycle	SINT	●			
Error management							
387	-	ErrorEnableID_0F08	USINT				●
259	14	ErrorInfo	USINT	●			
		EncoderSupplyError	Bit 0				
		VssCheckError	Bit 2				
		PositionError	Bit 3				
		HfComError	Bit 4				
		HfRefWarning	Bit 5				
323	6	AckErrorInfo	USINT			●	
		AckEncoderSupplyError	Bit 0				
		AckVssCheckError	Bit 2				
		AckPositionError	Bit 3				
		AckHfComError	Bit 4				
		AckHfRefWarning	Bit 5				
2116	-	HfErrorCode	UDINT	●			
Sin/Cos - Configuration							
1025	-	SinCosEnable	USINT				●
1027	-	SinCosRefSource	USINT				●
1034	-	SinCosVssMin	UINT				●
1038	-	SinCosVssMax	UINT				●
1044	-	SinCosQuitTime	UDINT				●
HIPERFACE - Configuration							
2049	-	HfMode	USINT				●
2053	-	HfParity	USINT				●
2055	-	HfCharTimeout	USINT				●
2060	-	HfBaud	UDINT				●
2068	-	HfRepressErrTime	UDINT				●
2073	-	HfRefAdr	USINT				●
2075	-	HfRefWidth	USINT				●
HIPERFACE - Identification							
2561	-	HfAdrIdent	USINT				●
2563	-	HfSelectionIdent	USINT				●
2631	-	HfIdentOk	USINT		●		
2688	-	HfRs485Settings	USINT		●		
2689	-	HfEncoderType	USINT		●		
2690	-	HfEepromSize	USINT		●		
2691	-	HfOptionFlags	USINT		●		
2692	-	HfFreeMemory	USINT		●		
2693	-	HfDataFields	USINT		●		
2693 + N	-	HfExtByte0N (index N = 1 to 10)	USINT		●		
HIPERFACE - Additional positions							
2817	-	AddPosAdr01	USINT				●
2887	-	AddPosOk (byte)	USINT	●			
		AddPosOk01	Bit 0				
		AddPosOk02	Bit 1				
2956	-	AddPosition01	DINT	●			
2958	-	AddPosition01	INT	●			
2825	-	AddPosAdr02	USINT				●
2972	-	AddPosition02	DINT	●			
2974	-	AddPosition02	INT	●			
HIPERFACE - Additional analog values							
3065 + N * 8	-	AnalogAdrCh0N (index N = 1 to 4)	USINT				●
3067 + N * 8	-	AnalogCh0N (index N = 1 to 4)	USINT				●
3143	-	AnalogChOk (byte)	USINT	●			
		AnalogChOk01	Bit 0				
		...	...				
		AnalogChOk04	Bit 3				
3194 + N * 16	-	AnalogChValue0N (index N = 1 to 4)	(U)INT	●			
Flatstream mode							
2305	-	OutputMTU	USINT				●
2307	-	InputMTU	USINT				●
2309	-	FlatStreamMode	USINT				●
2311	-	Forward	USINT				●
2316	-	ForwardDelay	UINT				●

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2368	8	InputSequence	USINT	●			
2368 + N	9 to 13	RxByteN (index N = 1 to 5)	USINT	●			
2400	0	OutputSequence	USINT			●	
2400 + N	1 to 5	TxByteN (index N = 1 to 5)	USINT			●	

1) The offset specifies the position of the register within the CAN object.

4.16.6.9.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.16.6.9.4 Module configuration

The following configuration register can be used to configure different module settings. They can be used, for example, to modify the module's behavior on an X2X Link network.

4.16.6.9.4.1 Data query

Name:
CfO_SIframeGenID

This register can be used to define when the synchronous/cyclic input data is generated. "X2X cycle optimized" should be set for jitter-free data acquisition. "Fast reaction" can be set for the best performance.

Data type	Value	Information
USINT	9	Fast reaction
	14	X2X cycle optimized (bus controller default setting)

4.16.6.9.5 Basic functions

This module can read a position when used together with a HIPERFACE encoder. The received position data is prepared in 2 different formats and given a time stamp. 6 registers are available for further processing. This allows the user to select the format that best fits the application at hand.

4.16.6.9.5.1 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.16.6.9.5.2 Absolute position values

Name:
PositionHW
PositionLW

The absolute position of the encoder is defined using 64-bit resolution. The position value is stored in the PositionHW and PositionLW registers. The upper 32 bits are stored the PositionHW register, while the lower 32 bits are stored in the PositionLW register.

For SinCos signal evaluation, see 4.16.3.11.7.1 "Format of the SinCos signal" for information regarding the data format.

Data type	Value
2x UDINT	0 to 4,294,967,295

4.16.6.9.5.3 SDC position value

Name:
Position

The SDC library requires a signed 32-bit position value. The position's low word can be accessed separately for this. The value can also be used as default position value, however.

For SinCos signal evaluation, see 4.16.3.11.7.1 "Format of the SinCos signal" for information regarding the data format.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.16.6.9.5.4 NetTime of the position values

Name:
PosTime

This register is used to assign each recorded position of the current NetTime value. The NetTime is recorded with µs accuracy.
The SDC library requires a 16 bit value. The NetTime value is therefore also generated in this format.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	NetTime in µs
INT	-32,768 to 32,767	

4.16.6.9.5.5 Counter for position values

Name:
PosCycle

PosCycle is an integer counter that is incremented as soon as the module has saved a new valid position value.

Data type	Value
SINT	-128 to 127

4.16.6.9.6 Error management

This module can be used to diagnose error states. There are 2 ways this module performs error diagnostics:

- Module-based diagnostics
- HIPERFACE-based diagnostics

4.16.6.9.6.1 Module-based diagnostics

Like most B&R modules, this module is also able to detect errors on its own. It diagnoses 5 different errors or warnings. The error bits can be retrieved individually or grouped together.

Enabling/disabling error messages

Name:
ErrorEnableID_0F08

The implemented diagnostic algorithms can be enabled or disabled in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder supply	0	Error detection disabled
		1	Error detection enabled (bus controller default)
1	Reserved	-	
2	Vss Sin/Cos	0	Error detection disabled
		1	Error detection enabled (bus controller default)
3	Position error	0	Error detection disabled
		1	Error detection enabled (bus controller default)
4	HIPERFACE communication	0	Error detection disabled
		1	Error detection enabled (bus controller default)
5	HIPERFACE reference warning	0	Warning disabled
		1	Warning enabled (bus controller default)
6 - 7	Reserved	-	

Encoder supply

The encoder voltage supply is below the permitted limit.

Vss Sin/Cos

The voltage value for the Sin/Cos track violates the configured limit values.
→ See register "SinCosVssMin" or "SinCosVssMax"

Position error

The position value determined violates internal requirements.

HIPERFACE communication

Communication error on the HIPERFACE interface (RS485)
→ See register "HfErrorCode"

HIPERFACE reference warning

The digital interface provides an absolute position value that can be used to accurately describe the axis position. The position value is homed to this absolute value at the beginning of a measurement. The analog interface can be used to incrementally sample changes that occur very rapidly. This enables the module to continue sampling the position value at a high resolution. Both the analog and the digital signal are sampled cyclically. If the value read incrementally deviates from the absolute value during operation, then the warning is generated and the position must be homed again.

Show error messages

Name:
ErrorInfo
EncoderSupplyError
VssCheckError
PositionError
HfComError
HfRefWarning

This register indicates any errors or warnings that have not yet been acknowledged. For the meaning of individual error messages, see register "Enabling/disabling error messages".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EncoderSupplyError	0	No error
		1	Encoder supply error
1	Reserved	-	
2	VssCheckError	0	No error
		1	Vss error on the Sin/Cos track
3	PositionError	0	No error
		1	Position error
4	HfComError	0	No error
		1	HIPERFACE communication error
5	HfRefWarning	0	No warning
		1	HIPERFACE reference warning
6 - 7	Reserved	-	

Acknowledge error messages

Name:
AckErrorInfo
AckEncoderSupplyError
AckVssCheckError
AckPositionError
AckHfComError
AckHfRefWarning

This register is used to acknowledge an error or warning message that occurred in the "Show error messages" register. For the meaning of individual error messages, see register "Enabling/disabling error messages".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	AckEncoderSupplyError	0	No error acknowledgment
		1	Error acknowledgment
1	Reserved	-	
2	AckVssCheckError	0	No error acknowledgment
		1	Error acknowledgment
3	AckPositionError	0	No error acknowledgment
		1	Error acknowledgment
4	AckHfComError	0	No error acknowledgment
		1	Error acknowledgment
5	AckHfRefWarning	0	No acknowledgment
		1	Acknowledgment
6 - 7	Reserved	-	

4.16.6.9.6.2 HIPERFACE-based diagnostics

Memory areas are provided in the HIPERFACE standard for error diagnostics. Error management has been adjusted in order to use error detection in accordance with the HIPERFACE standard. An additional register has been implemented in the module to provide this area in the encoder's memory. This error memory is mirrored in the module's registers and can be interpreted by the user. Detailed information regarding the errors that can be detected in this way can be found in the encoder's manual.

HfErrorCode

Name:
HfErrorCode

This register is used to store the error code that identifies the current problem with the HIPERFACE interface.

Data type	Value
UDINT	See bit structure.

Internally, the register consists of 4 pieces of information.

Bit structure:

Bit	Name	Information
00 - 07	Error ID	See below
08 - 15	Last command	Command that caused the error on the slave
16 - 23	Station address	Address of the faulty HIPERFACE slave
24 - 31	Error counter	Counts the number of errors that have occurred

Bit 00-07 (error ID)
These 8 bits of this register specify the error that has occurred. The error ID is not a standard value, however, and must be looked up in the manual for the HIPERFACE slave. The module also diagnoses a timeout on the HIPERFACE interface. This triggers error ID 255.

4.16.6.9.7 Sin/Cos - Analog interface configuration

In addition to the digital HIPERFACE interface, this module is also equipped with an analog interface for sampling a differential sine-cosine signal. To increase the resolution, the EnDat standard supports cooperation between the analog and digital data. This enables a highly dynamic representation of the position while maintaining high resolution.

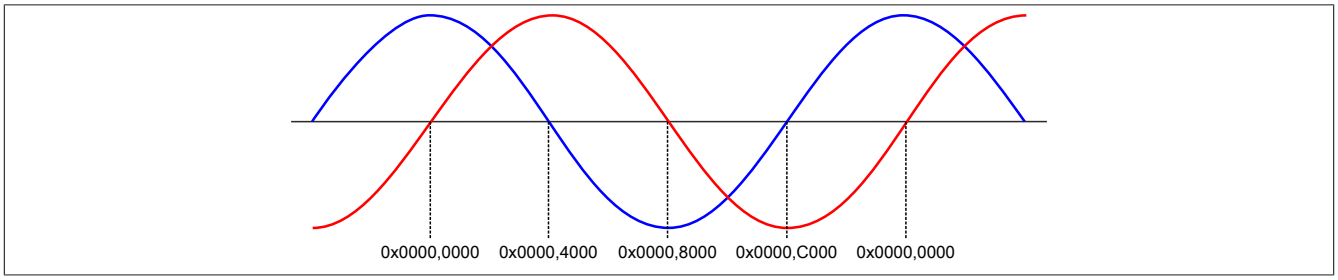
4.16.6.9.7.1 Format of the SinCos signal

The SinCos signal is represented as a position value in the 4.16.3.11.5.2 "Absolute position values" and 4.16.3.11.5.3 "SDC position value" registers. The following relationships apply:

- PositionLW and Position are identical in the function.
- PositionHW extends the integer range of PositionLW by adding multi-turn functionality.

64-bit register	PositionHW (unsigned)	PositionLW (unsigned)	
32-bit register	-	Position (signed)	
Format	Integer extension (to 48-bit)	Integer (16-bit)	Decimal places: (with 13-bit resolution)
Information		A full sine wave corresponds to an increment of the integer.	**15** **14** **13** **12** **11** **10** **9** **8** **7** **6** **5** **4** **3** **2** **1** **0** x x x x x x x x x x x x x 0 0 0 **Important:** The lower 3 bits always contain the value 0.
Word/DWord	DWord	Word 1	Word 0

Relationship between sine curve (red) and decimal places:



4.16.6.9.7.2 Enabling SinCos

Name:
SinCosEnable

This register must always have the value 1 for configuration reasons.

Data type	Value	Information
USINT	1	Bus controller default: 1

4.16.6.9.7.3 SinCosRefSource

Name:
SinCosRefSource

This register must always have the value 3 for configuration reasons.

Data type	Value	Information
USINT	3	Bus controller default: 3

4.16.6.9.7.4 Configuring the lower Vss value

Name:
SinCosVssMin

This register specifies the lower limit value for the peak-to-peak voltage of the sine/cosine track. The incoming signal is monitored in this way. If the incoming value falls below this specified limit, then the module reports the corresponding error.

Data type	Value	Information
UINT	0 to 1500	Values in mV, bus controller default setting: 800

4.16.6.9.7.5 Configuring the upper Vss value

Name:
SinCosVssMax

This register specifies the upper limit value for the peak-to-peak voltage of the sine/cosine track. The incoming signal is monitored in this way. If the incoming value exceeds this specified limit, then the module reports the corresponding error.

Data type	Value	Information
UINT	0 to 1500	Values in mV, bus controller default setting: 1200

4.16.6.9.7.6 Configuring the delay time after errors

Name:
SinCosQuitTime

If an error is detected on the analog interface, the last correctly read values remain valid. An interval can be defined in this register at which the module begins receiving correct values again after the error state without processing them further internally. Only then will newly sampled correct analog values be recognized as valid.

Data type	Value	Information
UDINT	0 to 20000000	Values in µs, bus controller default setting: 100000

4.16.6.9.8 HIPERFACE

4.16.6.9.8.1 HIPERFACE - Digital interface configuration

HIPERFACE builds upon the RS-485 (EIA-485) specification and permits communication with multiple HIPERFACE slaves.

There are 2 methods available to use the slave data in a PLC program. One is to store the necessary slave values temporarily in the module, where they can then be provided to the CPU. The other is to use the module's FlatStream mode, which supports the full range of commands defined in the HIPERFACE specification.

Additional information regarding the HIPERFACE specification is provided in the "Description of HIPERFACE" document.

HfMode

Name:
HfMode

This register is used to enable the HIPERFACE interface and must always be set to the value 1 for configuration reasons.

Data type	Value	Value
USINT	1	Bus controller default: 1

HfParity

Name:
HfParity

This register configures the parity bit for the interface.

Data type	Value	Information
USINT	69	E → even parity bit; bus controller default
	78	N → no parity bit
	79	O → odd parity bit

HfCharTimeout

Name:
HfCharTimeout

This register configures the time that the module waits after receiving the last data block to add additional data to the current data packet (frame). When this time expires, the data received thus far is saved in a frame. The transfer is complete and the data can be evaluated.

Information:

Time is specified as a char value in order to ensure identical behavior regardless of the baud rate setting.

Data type	Value	Information
USINT	1 to 255	Char; bus controller default: 55

HfBaud

Name:
HfBaud

This register configures the baud rate (transfer rate) of the interface.
The module does not allow a transfer rate of 600 baud.

Data type	Value	Information
UDINT	1200, 2400, 4800, 9600, 19200, 38400	Baud; bus controller default: 9600

HfRepressErrTime

Name:
HfRepressErrTime

This register configures the minimum time that an error code remains in the "HfErrorCode" register. This makes it possible to ensure that the CPU registers every error that occurs.

Data type	Value	Information
UDINT	1 to 20000000	Time in µs, bus controller default setting: 100000

HfRefAdr

Name:
HfRefAdr

This module can manage up to 32 HIPERFACE slaves via its digital interface. High-resolution position sampling, however, requires information from both the digital and analog interfaces. The HIPERFACE address of the station whose sine/cosine track is being read by the module is entered in this register. If there is only one slave on the network, the broadcast address (255) can also be used.

Data type	Value	Information
USINT	0	Operation without sine/cosine track
	64 to 95	Open address range for max. 32 HIPERFACE slaves
	255	Broadcast address; bus controller default

HfRefWidth

Name:
HfRefWidth

This register is used to set the absolute width for the sampled position. The number of bits must be taken from the data provided by the encoder manufacturer and usually consists of three values:

- 5 bits: Resolution of the digital absolute position
- x bits: HIPERFACE data format, number of bits per revolution
- 2^y bits: Number of sine/cosine periods per revolution

The sum of the sampled values results in the HfRefWidth (HfRefWidth = 5+x+y).

Data type	Value	Information
USINT	8 to 32	Bus controller default: 32

4.16.6.9.8.2 HIPERFACE - Read ID

The digital interface provides the option of assigning a HIPERFACE slave a specific ID. Its parameter data can be queried when booting the PLC, for example. Any deviations from the previous hardware constellation can then be handled accordingly in the program.

Configuration

The parameter to be read is specified by 2 registers. One of the registers contains the address of the desired HIPERFACE slave; the other contains a code for the value to be read.

HfAdrIdent

Name:
HfAdrIdent

This register is used to specify the address of the HIPERFACE slave whose parameter should be read by the module.

Data type	Value	Information
USINT	0	Identification disabled; bus controller default: 0
	64 to 95	Open address range for max. 32 HIPERFACE slaves
	255	Broadcast address (when operating with one slave)

HfSelectionIdent

Name:
HfSelectionIdent

This register defines the parameters that should be provided in the slave response and buffered in the module's "HfExtByte" register.

Data type	Value	Value
USINT	0	Serial number; bus controller default
	1	Firmware date
	2	High part of firmware version
	3	Low part of firmware version

Call

After being configured correctly, the selected parameter is transmitted cyclically to the module. There are 8 registers that serve as temporary storage. The module confirms successful receipt by setting the HfIdentOkByte.

HfIdentOk

Name:
HfIdentOk

This register's bits provide information about the validity of the latest ID values in temporary storage.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	HfIdentOk01	0	Parameter 01 invalid
		1	Parameter 01 valid
1 - 7	Reserved	-	

HfRs485Settings

Name:
HfRs485Settings

This register is used to temporarily store the current network configuration expected by the slave. The register value is specifically structured for HIPERFACE.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	Speed code	001	1200 baud
		010	2400 baud
		011	4800 baud
		100	9600 baud; bus controller default
		101	19200 baud
		110	38400 baud
3	Reserved	-	
4	Number of parity bits	0	No parity bit
		1	One parity bit (default)
5	Type of parity bit	0	Even (default)
		1	Odd
6	Behavior if a timeout occurs	0	Timeout 11/baudrate
		1	Timeout 4*11/baud rate (default)
7	Network behavior	0	Bus
		1	Direct connection (default)

HfEncoderType

Name:
HfEncoderType

This register is used to temporarily store the ID of the current encoder. The register value is structured specifically for each slave and must be looked up in the encoder's data sheet.

Data type	Value
USINT	0 to 255

HfEepromSize

Name:
HfEepromSize

This register is used to store the size of the EEPROM being used. The number of 16-byte blocks is specified.

Data type	Value	Value
USINT	0 to 255	16-byte blocks

HfOptionFlags

Name:
HfOptionFlags

This register is used to store slave-specific hardware and software settings.

Data type	Value
USINT	0 to 255

HfFreeMemory

Name:
HfFreeMemory

This register is used to indicate the number of free 16-byte blocks remaining on the HIPERFACE slave.

Data type	Value	Information
USINT	0 to 255	16-byte blocks

HfDataFields

Name:
HfDataFields

This register is used to indicate the number of data fields that have been written thus far.

Data type	Value
USINT	0 to 255

HfExtByte

Name:
HfExtByte01 to HfExtByte10

These registers provide the respective parameters according to how the "HfSelectionIdent" register is configured.

Data type	Value
USINT	0 to 255

4.16.6.9.8.3 HIPERFACE - Reading additional encoder positions

This module can read up to 2 additional position values via the HIPERFACE interface and provide them to the PLC. Each position value is accompanied by a timestamp.

Configuration

The address must be specified in order to read the position value from the respective HIPERFACE interface. One address register is provided for each position value.

AddPosAdr

Name:
AddPosAdr01 to AddPosAdr02

These registers specify the addresses of the HIPERFACE slaves whose position values should be processed in the module.

Data type	Value	Information
USINT	0	Additional encoder position disabled; bus controller default
	64 to 95	Open address range for max. 32 HIPERFACE slaves
	255	Broadcast address (when operating with one slave)

Call

After being configured correctly, the position value is transmitted cyclically to the module. Each slave has five registers that serve as temporary storage. The module automatically generates the timestamp and confirms successful transmission by setting the corresponding AddPosOk0x bit. The HIPERFACE specification does not specify in which format the parameters must be received. The module therefore provides the position value and time in two formats. Which of the position registers should be used for further processing depends on the HIPERFACE slave. The user is free to define the format of the timestamp.

AddPosOk (byte)

Name:
AddPosOk01 to AddPosOk02

This register's bits provide information about the validity of the last position values in temporary storage.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	AddPosOk01	0	Position value 01 invalid
		1	Position value 01 valid
1	AddPosOk02	0	Position value 02 invalid
		1	Position value 02 valid
2 - 7	Reserved	-	

AddPosition

Name:
AddPosition01 to AddPosition02

These registers provide the current position values, depending on the register address, as signed 2-byte or 4-byte values.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647
INT	-32,768 to 32,767

AddPosTime

Name:
AddPosTime01 to AddPosTime02

These registers provide the time stamp of the most recently received position values, depending on the register address, as signed 2-byte or 4-byte values.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	NetTime in µs
INT	-32,768 to 32,767	

4.16.6.9.8.4 HIPERFACE - Reading additional analog values

This module can read up to 4 analog values (16-bit) via the HIPERFACE interface and provide them to the PLC. Each analog value is accompanied by a timestamp.

Configuration

The analog value to be read is specified by 2 registers. One of them contains the address of the desired station, and the other the channel of the parameter to be read. An overview of analog values that can be read is provided in the data sheet for the respective slave.

AnalogAdrCh

Name:
AnalogAdrCh01 to AnalogAdrCh04

These registers specify the addresses of the HIPERFACE slaves whose analog values should be processed in the module. To query multiple values from one HIPERFACE slave, it may make sense to write the same address to different AnalogAdrCh registers.

Data type	Value	Information
USINT	0	Additional analog values disabled; bus controller default
	64 to 95	Open address range for max. 32 HIPERFACE slaves
	255	Broadcast address (when operating with one slave)

AnalogCh

Name:
AnalogCh01 to AnalogCh04

These registers define the channel to be read that is written by the bus station to the module's temporary storage.

Data type	Value
USINT	See encoder data sheet Bus controller default: 0

Call

After being configured correctly, the analog value is transmitted cyclically to the module. There are 5 registers that serve as temporary storage. The module automatically generates the timestamp and confirms successful transmission by setting the corresponding AnalogChOk0x bit. The HIPERFACE specification does not specify in which format the parameters must be received. The module therefore provides the value and time in two formats. Which of the value registers should be used for further processing depends on the peripheral equipment. The user is free to define the format of the timestamp.

AnalogChOk (byte)

Name:
AnalogChOk01 to AnalogChOk04

This register's bits provide information about the validity of the values in temporary storage.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	AnalogChOk01	0	Analog value 01 invalid
		1	Analog value 01 valid
...		...	
3	AnalogChOk04	0	Analog value 04 invalid
		1	Analog value 04 valid
4 - 7	Reserved	-	

AnalogChValue

Name:
AnalogChValue01 to AnalogChValue04

These registers provide the current analog values, depending on the register address, as signed or unsigned 2-byte values.

Data type	Value
UINT	0 to 65,535
INT	-32,768 to 32,767

AnalogChTime

Name:
AnalogChTime01 to AnalogChTime04

These registers provide the time stamp of the most recently received analog values, depending on the register address, as signed 2-byte or 4-byte values.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Time in µs
INT	-32,768 to 32,767	

4.16.6.9.9 FlatStream communication

4.16.6.9.9.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

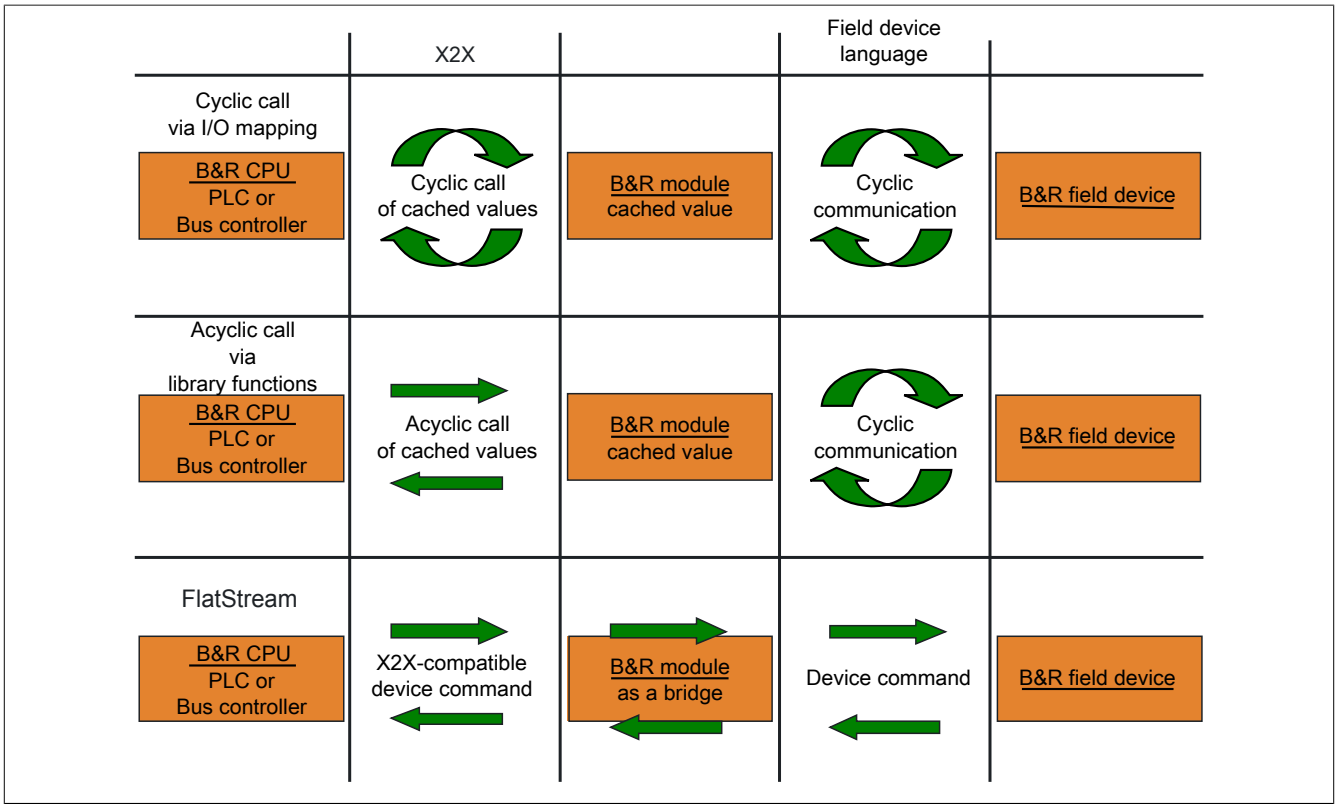


Figure 240: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.16.6.9.9.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.16.6.9.9.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

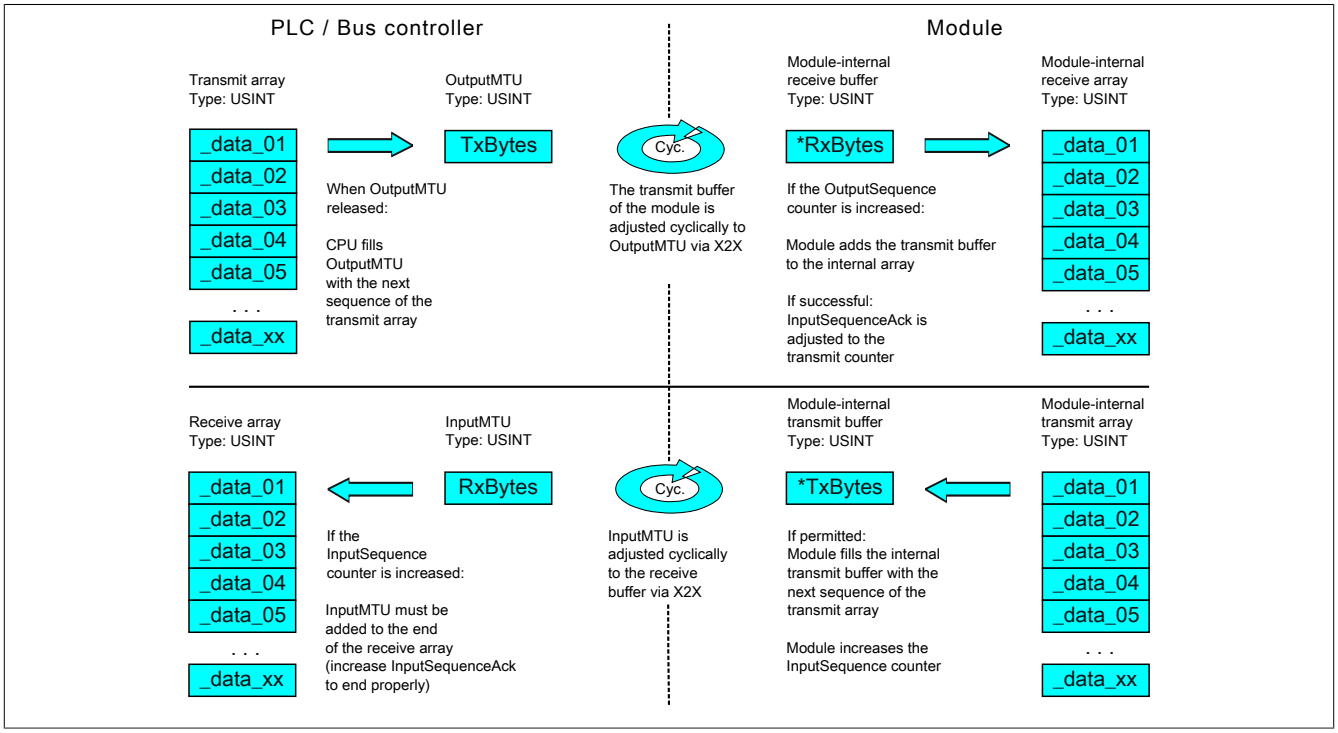


Figure 241: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.16.6.9.9.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

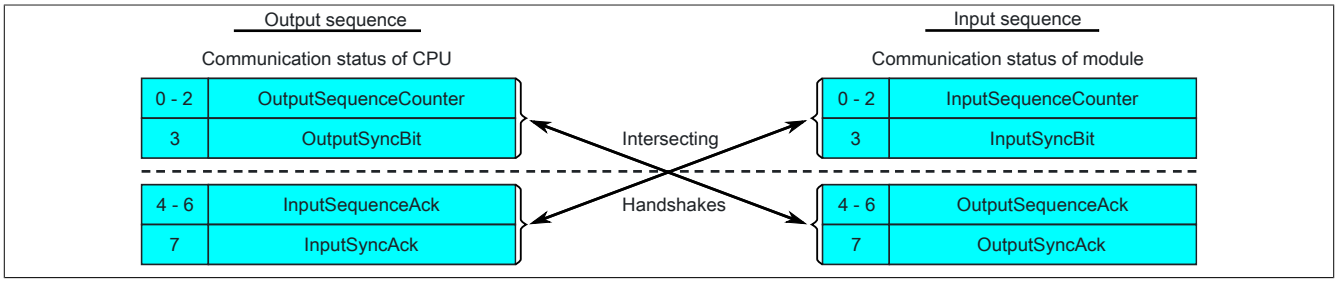


Figure 242: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

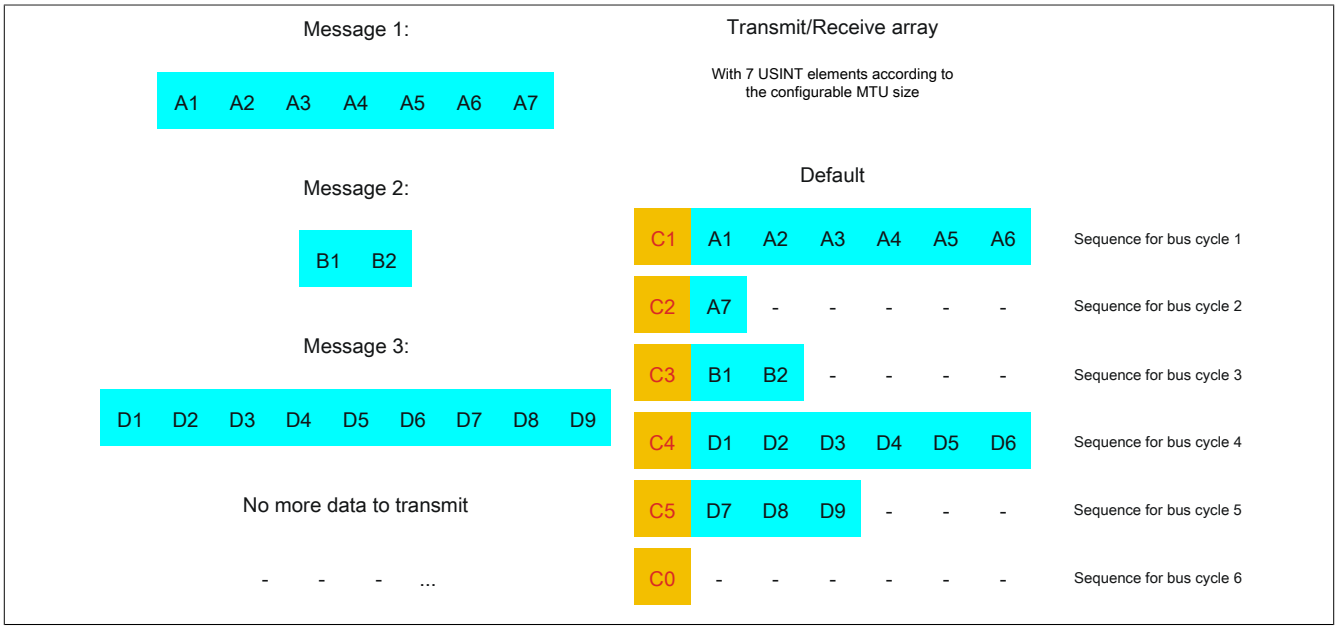


Figure 243: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 363: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 364: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

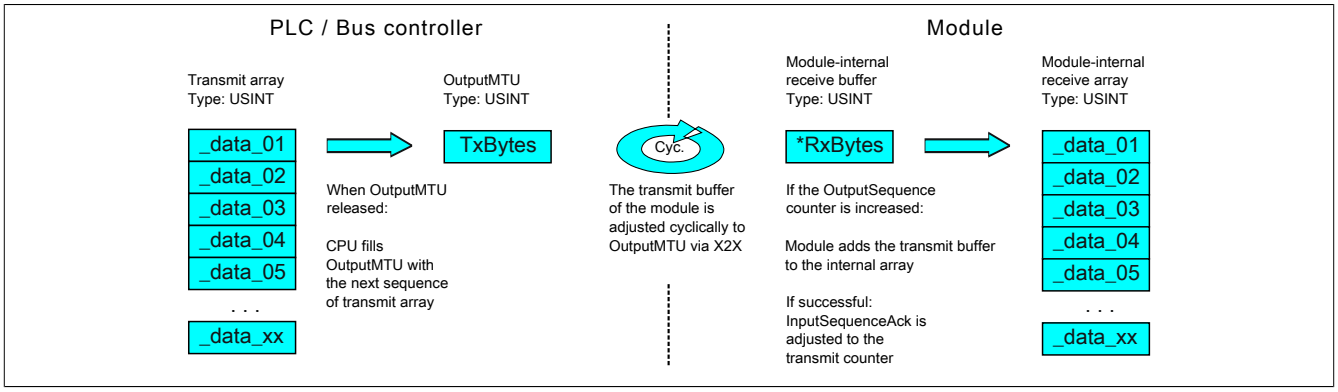


Figure 244: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

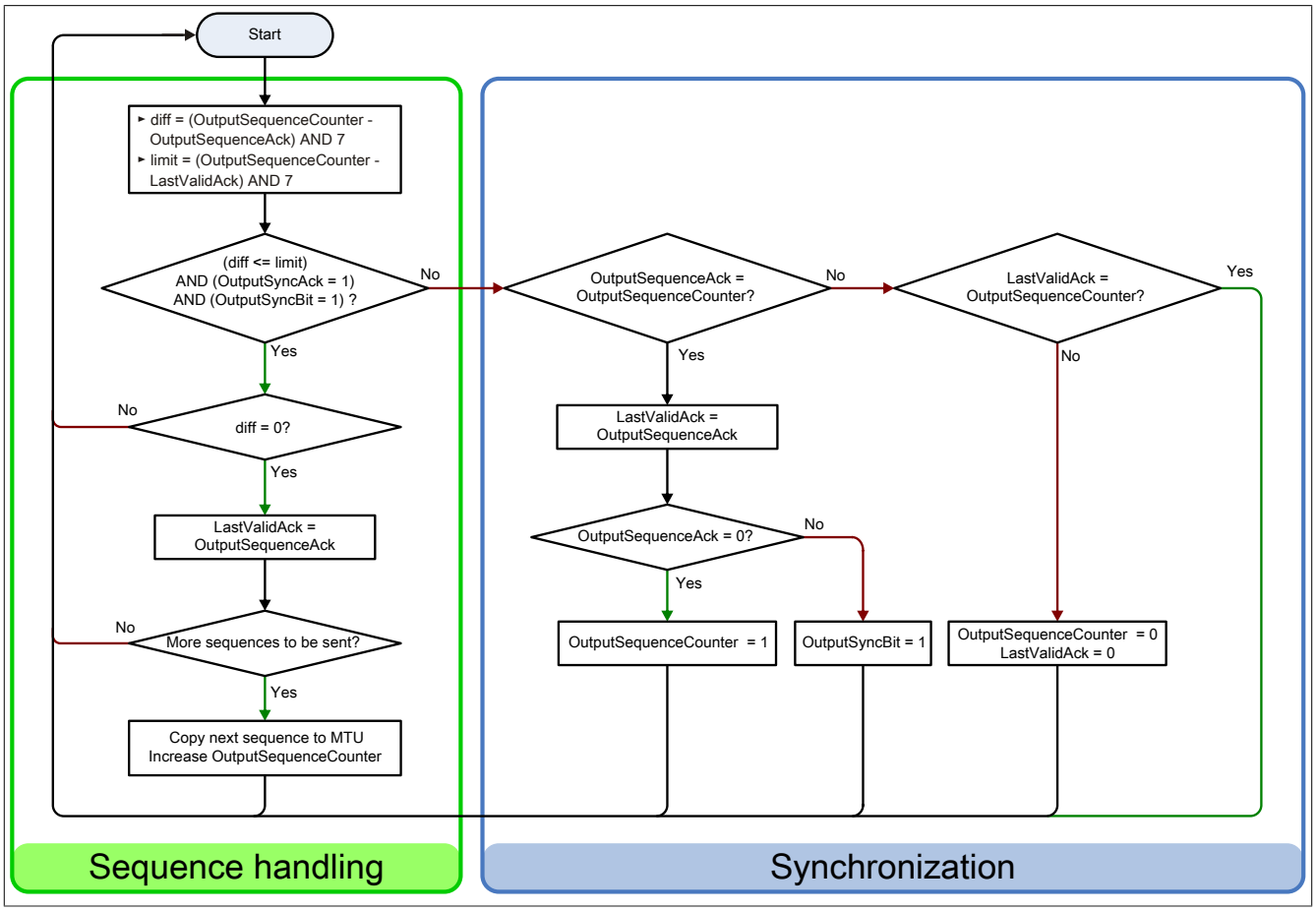


Figure 245: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

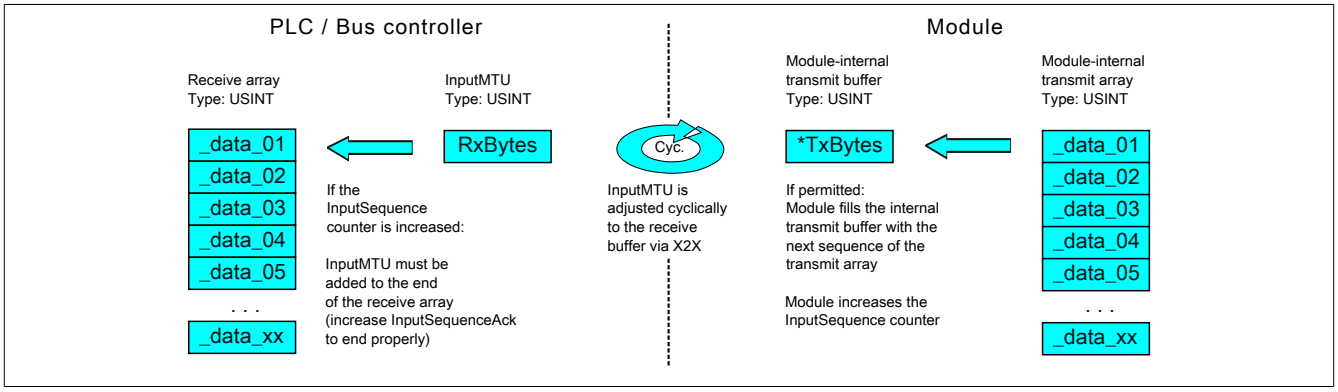


Figure 246: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

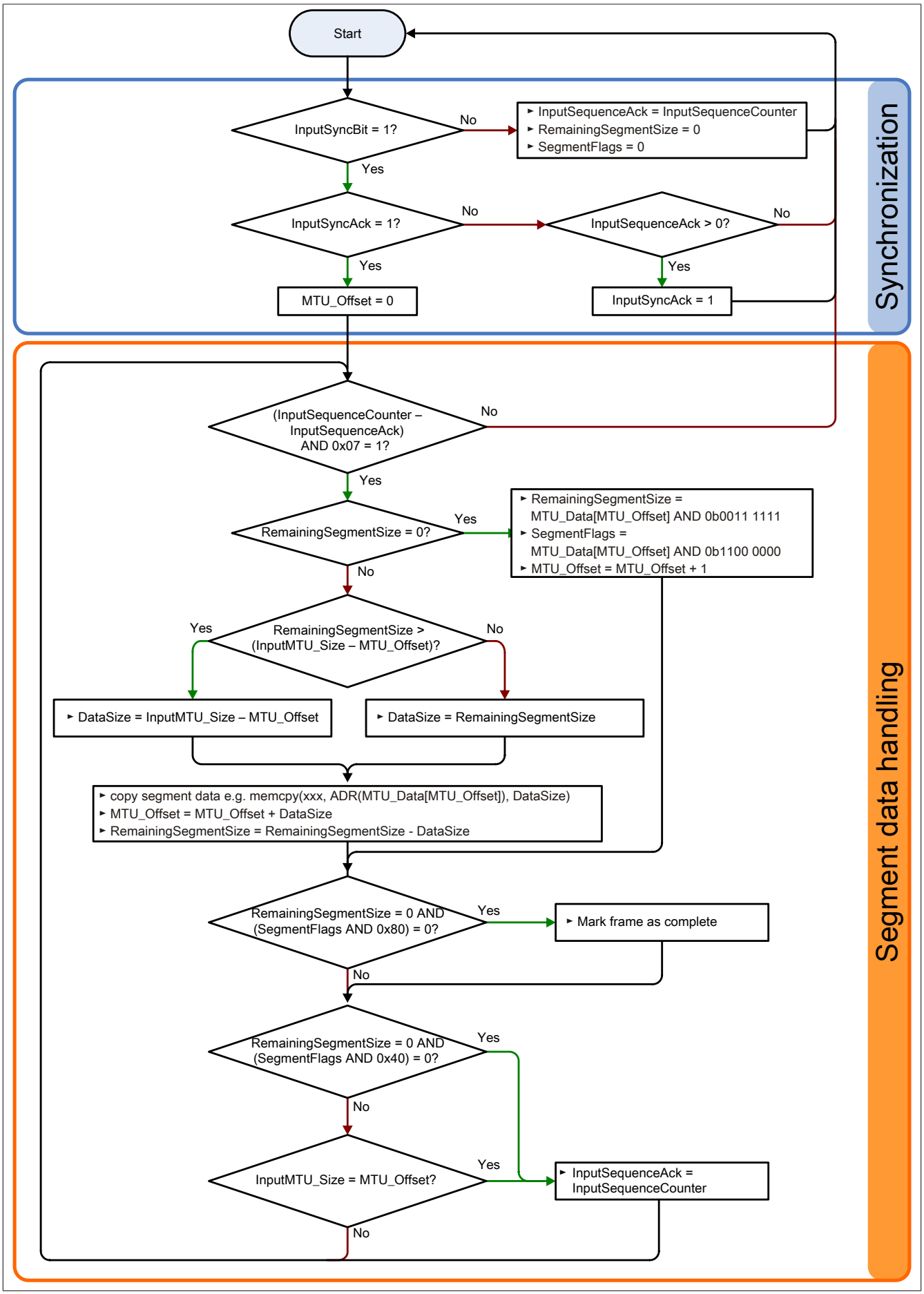


Figure 247: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

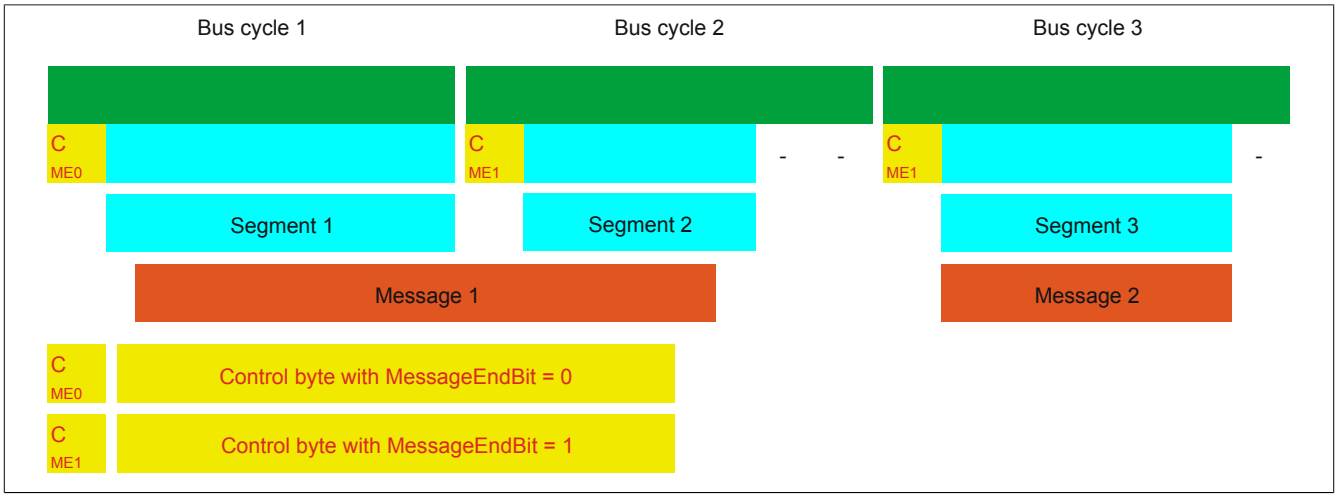


Figure 248: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

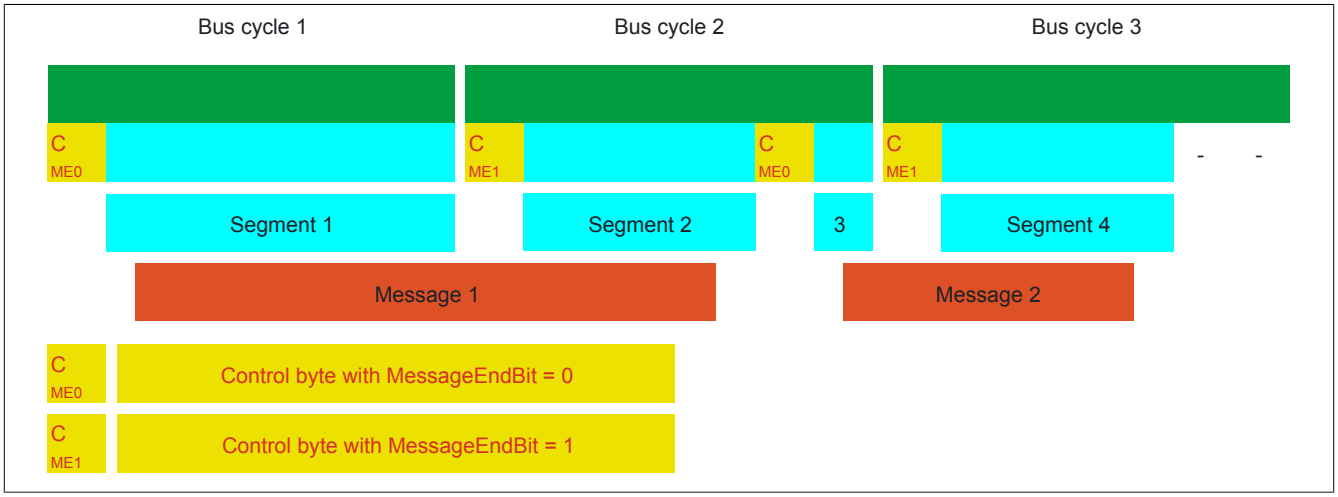


Figure 249: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

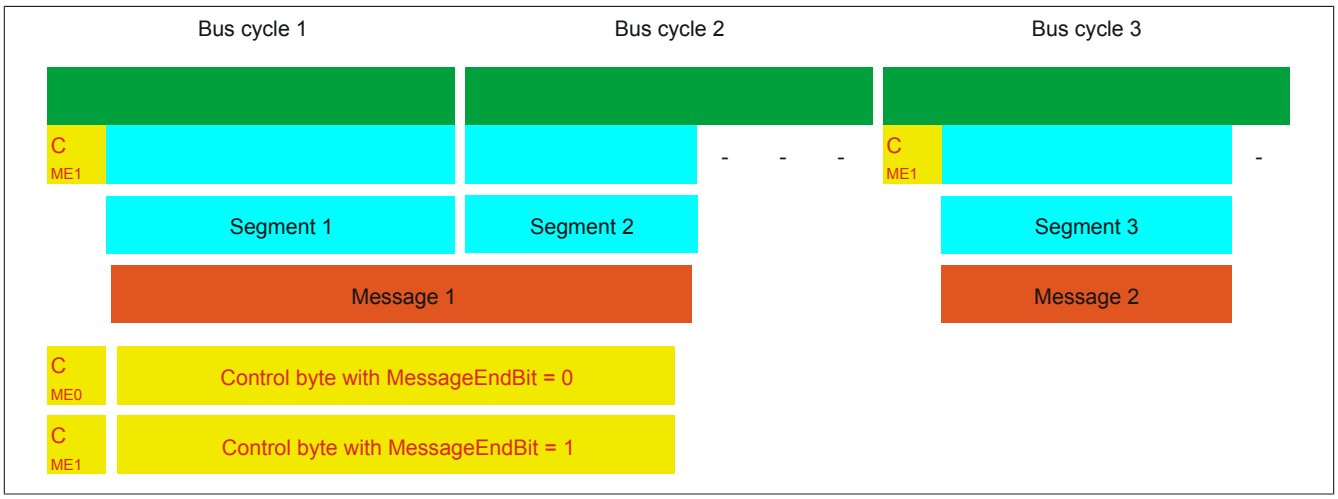


Figure 250: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

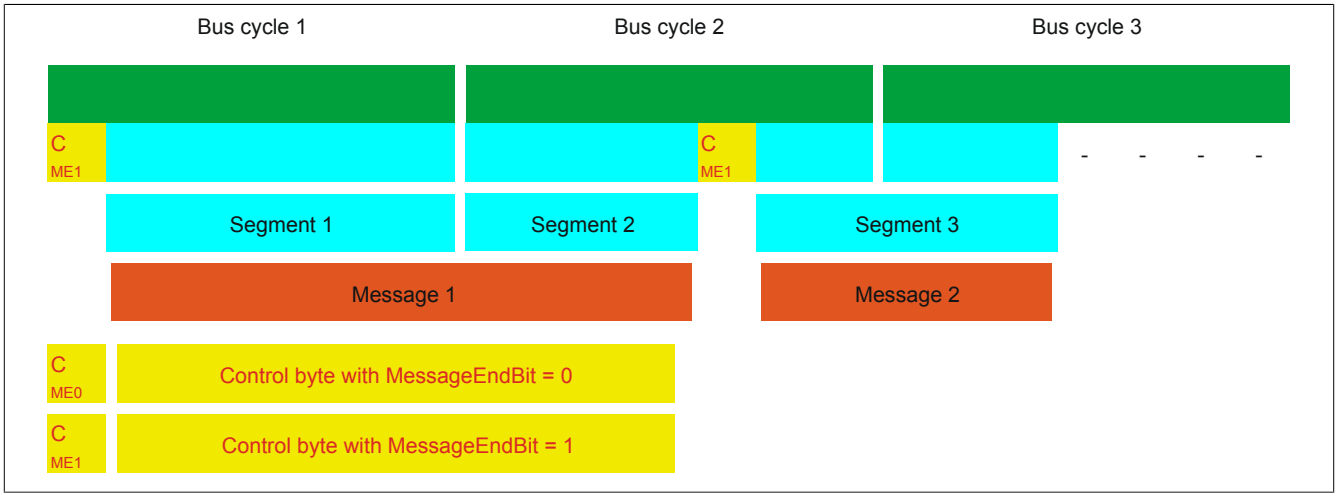


Figure 251: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

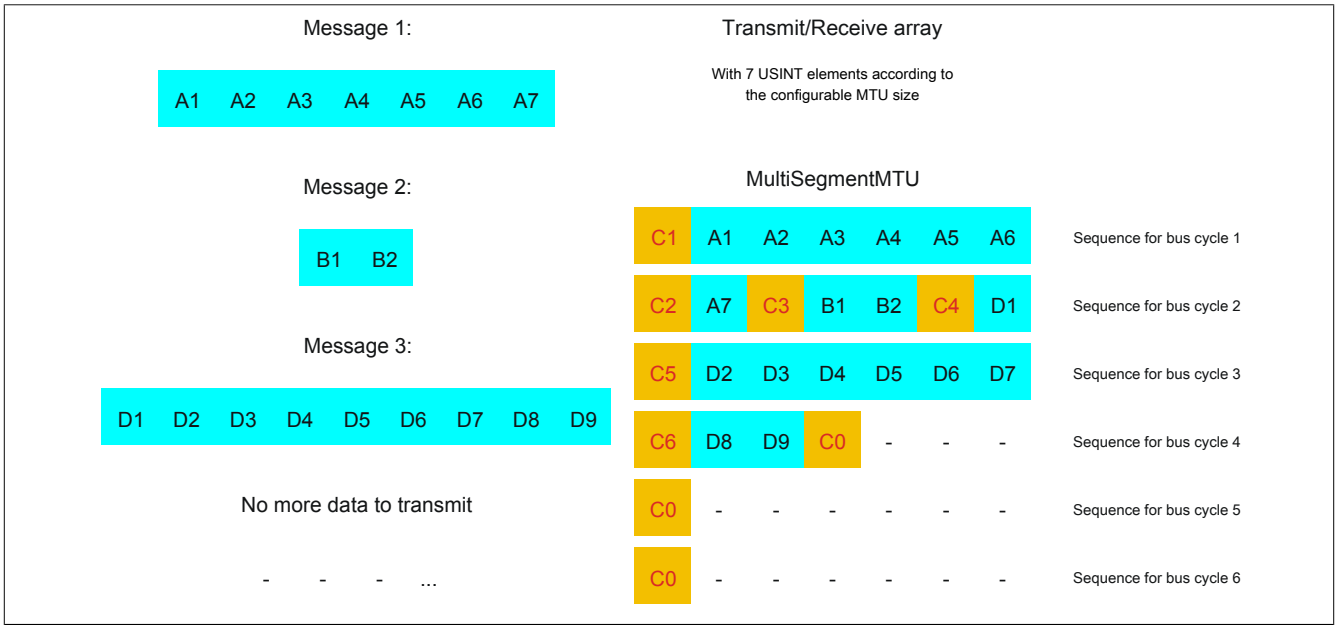


Figure 252: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 365: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 366: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

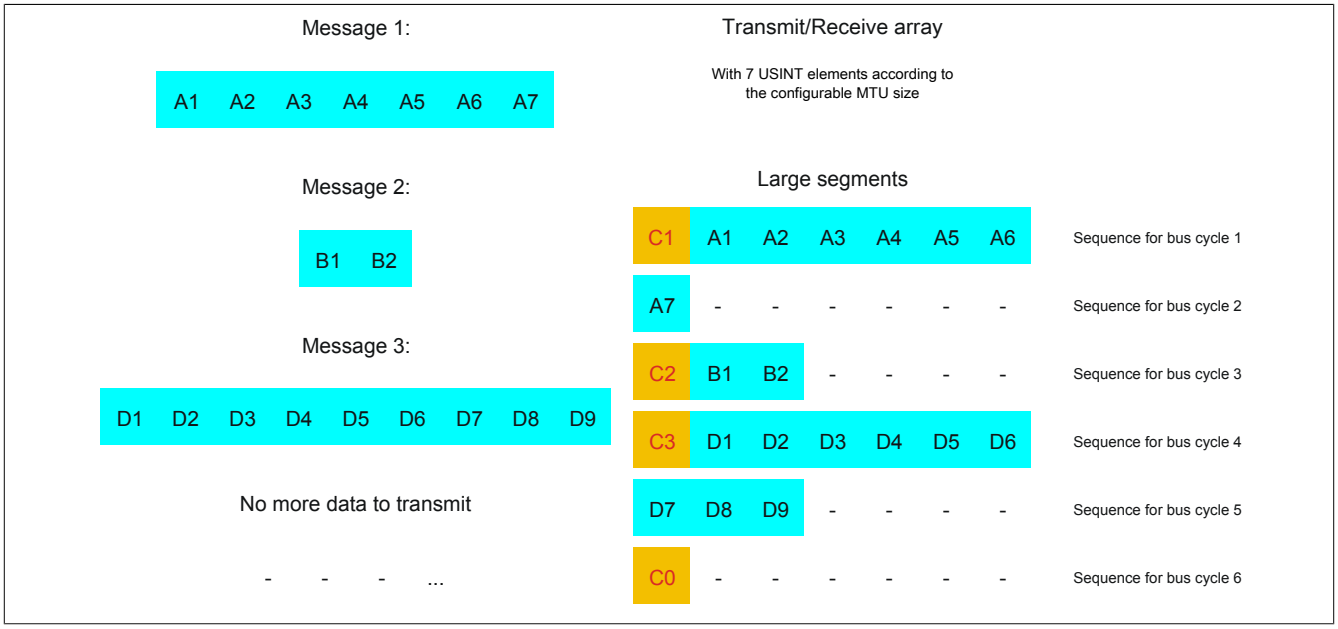


Figure 253: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 367: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

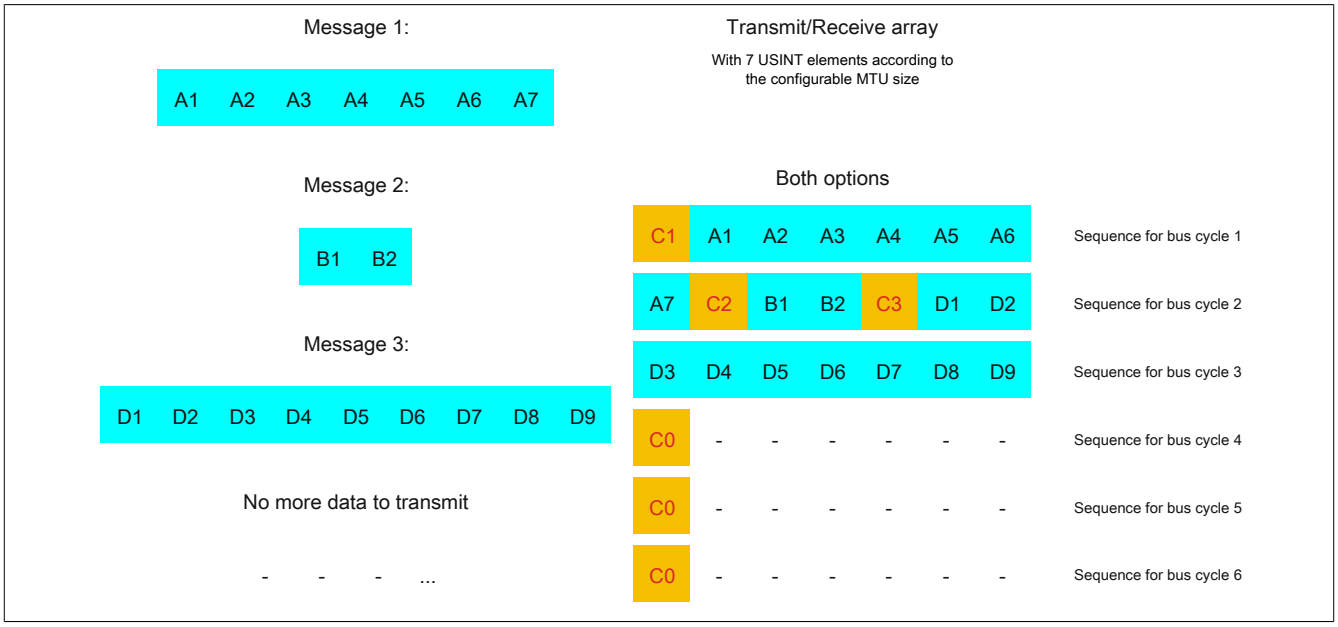


Figure 254: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 368: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.16.6.9.9.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

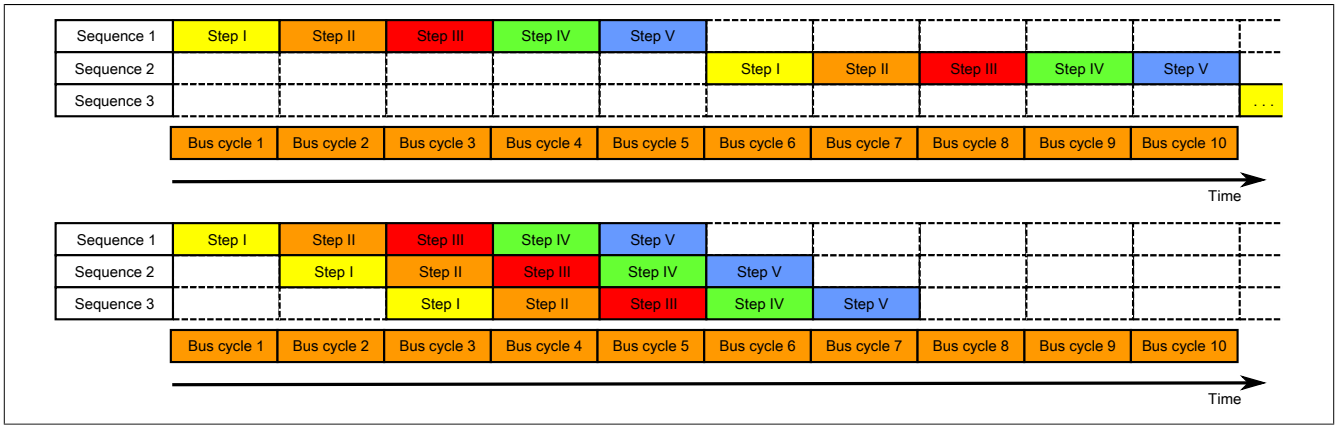


Figure 255: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

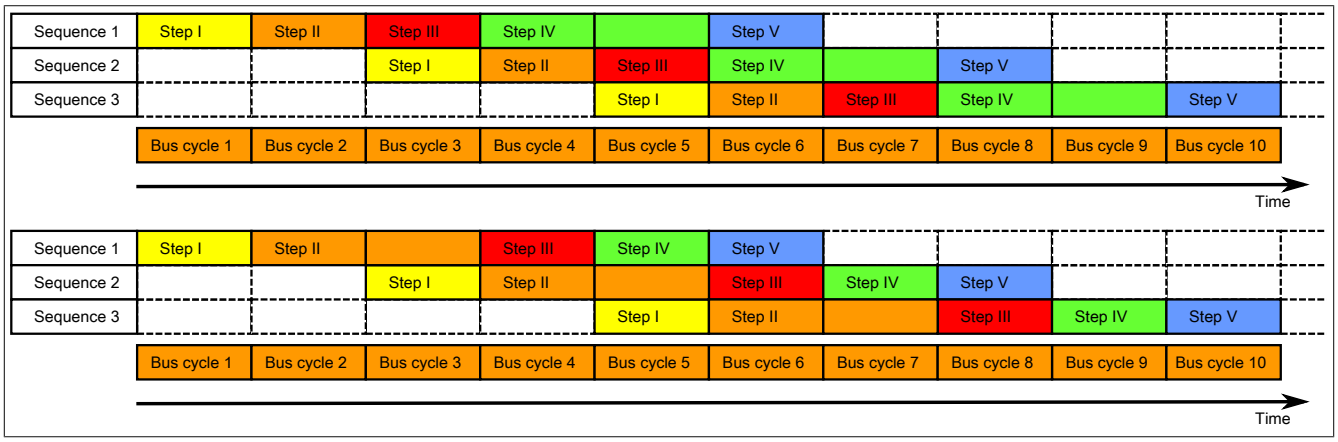


Figure 256: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

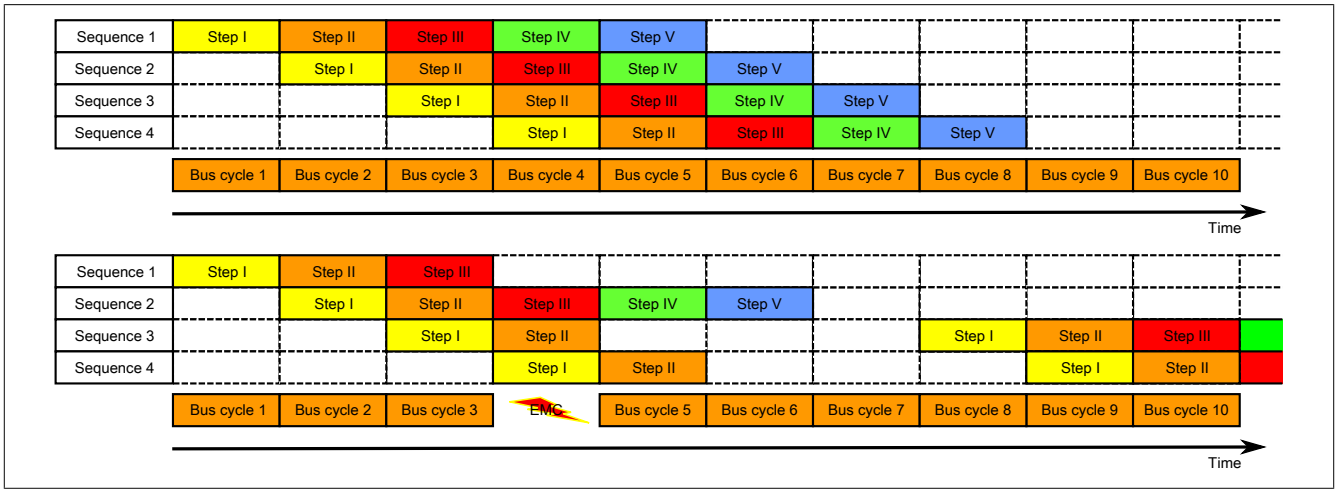


Figure 257: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.16.6.9.10 HIPERFACE with FlatStream

HIPERFACE is an asynchronous interface capable of half-duplex communication. Various features have been included to ensure that signals are transmitted without errors.

- The user can choose to have a parity bit added when transmitting a data block.
- A checksum is sent together with a signal and evaluated by the receiver.
- The command to which the encoder is responding is repeated at the start of a response.

In FlatStream mode, the module acts as a bridge between the CPU and the HIPERFACE slave. HIPERFACE-specific algorithms have been implemented to monitor timeouts and handle checksums. During normal operation, the user does not have access to these details.

Additional information is provided in the "Description of HIPERFACE" document.

4.16.6.9.10.1 Overview of conventional HIPERFACE commands for FlatStream mode

Command byte [hex]	Command	Code0
0x42	Read position	
0x43	Set position	•
0x44	Read analog value	
0x46	Read counter	
0x47	Increment counter	
0x49	Delete counter	•
0x4A	Read data	
0x4B	Save data	
0x4C	Read status of a data field	
0x4D	Create data field	
0x4E	Read available memory area	
0x4F	Change access key	
0x50	Read encoder status	
0x52	Read nameplate	
0x53	Reset encoder	
0x55	Allocate encoder address	•
0x56	Read serial number and program version	
0x57	Configure serial interface	•

Code0 is a byte that was added to the transfer protocol for safety reasons. It protects important system parameters from being overwritten by mistake (default: Code0 = 0x55).

4.16.6.9.10.2 Read position (0x42)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x42	Command byte (read position)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x42	
3	Pos_HH	Response (data bytes)
4	Pos_HL	
5	Pos_LH	
6	Pos_LL	
Master		

4.16.6.9.10.3 Set position (0x43)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x43	Command byte (set position)
3	Pos_HH	New position (data bytes)
4	Pos_HL	
5	Pos_LH	
6	Pos_LL	
7	Code0	Safety byte in accordance with the HIPERFACE specification
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x43	
Master		

4.16.6.9.10.4 Read analog value (0x44)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x44	Command byte (read analog value)
3	channel	Channel byte (selects desired analog value)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address, command byte and channel byte (safety)
2	0x44	
3	channel	
4	Value_H	Value read
5	Value_L	
Master		

4.16.6.9.10.5 Read counter (0x46)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x46	Command byte (read counter)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x46	
3	Ctr_H	Counter value
4	Ctr_M	
5	Ctr_L	
Master		

4.16.6.9.10.6 Increment counter (0x47)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x47	Command byte (increment counter)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x47	
Master		

4.16.6.9.10.7 Clear counter (0x49)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x49	Command byte (clear counter)
3	Code0	Safety byte in accordance with the HIPERFACE specification
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x49	
Master		

4.16.6.9.10.8 Read data (0x4A)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x4A	Command byte (read data)
3	Data field	ID of data to be read: Number of the data field, start byte within the data field and number of bytes to be read
4	Byte address	
5	Count	
6	Access code	Access code in accordance with the HIPERFACE specification
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address, command byte and ID of data to be read (safety)
2	0x4A	
3	Data field	
4	Byte address	
5	Count	
6...n	Data1...n	Data to be read
Master		

4.16.6.9.10.9 Save data (0x4B)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x4B	Command byte (save data)
3	Data field	ID of data to be saved:
4	Byte address	Number of the data field, start byte within the data field and number of bytes to be read
5	Count	
6	Access code	Access code in accordance with the HIPERFACE specification
7...x	Data1...n	Data to be saved
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address, command byte and ID of data to be saved (safety)
2	0x4B	
3	Data field	
4	Byte address	
5	Count	
Master		

4.16.6.9.10.10 Read status of a data field (0x4C)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x4C	Command byte (determine status of a data field)
3	Data field	Number of the data field
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address, command byte and number of the data field (safety)
2	0x4C	
3	Data field	
4	Status	Access mode for queried data field
Master		

4.16.6.9.10.11 Create data field (0x4D)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x4D	Command byte (create data field)
3	Data field	Number of the data field
4	Status	Access mode for the data field
5	Access code	Access code in accordance with the HIPERFACE specification
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address, command byte, number of the data field and access mode of the data field (safety)
2	0x4D	
3	Data field	
4	Status	
Master		

4.16.6.9.10.12 Read available memory area (0x4E)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x4E	Command byte (read available memory area)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x4E	
3	Free memory	Number of available 16-byte blocks
4	Number of data fields	Number of data fields
Master		

4.16.6.9.10.13 Change access key (0x4F)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x4F	Command byte (change access key)
3	Code number	Safety code from the slave manufacturer
4	Old code	
5	New code	
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address, command byte and code number (safety)
2	0x4F	
3	Code number	
Master		

4.16.6.9.10.14 Read encoder status (0x50)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x50	Command byte (read encoder status)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x50	
3	Encoder status	Status byte as specified by the slave manufacturer
Master		

4.16.6.9.10.15 Read nameplate (0x52)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x52	Command byte (read nameplate)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x52	
3	RS485 settings	Nameplate in accordance with HIPERFACE specification: HIPERFACE configuration, type of encoder, size of memory and other options
4	Encoder type	
5	Size of EEPROM	
6	Options	
Master		

4.16.6.9.10.16 Encoder reset (0x53)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x53	Command byte (encoder reset)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
-	-	No response
Master		

4.16.6.9.10.17 Allocate encoder address (0x55)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x55	Command byte (allocate encoder address)
3	New address	New HIPERFACE address
4	Code0	Safety byte in accordance with the HIPERFACE specification
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x55	
Master		

4.16.6.9.10.18 Read serial number and program version (0x56)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x56	Command byte (read serial number and program version)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address and command byte (safety)
2	0x56	
3...11	Serial number	9 characters
12...n	Firmware version	Max. 20 characters
...n+8	Firmware date	8 characters (format: DD.MM.YY)
Master		

4.16.6.9.10.19 Configure serial interface (0x57)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	Address	Address of the HIPERFACE slave
2	0x57	Command byte (configure serial interface)
3	RS485 settings	New baud rate in accordance with the HIPERFACE specification
4	Code0	Safety byte in accordance with the HIPERFACE specification
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	Address	Repeated address, command byte and new baud rate (safety)
2	0x57	
3	RS485 settings	
Master		

4.16.6.9.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
100 µs

4.16.6.9.12 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.16.7 X20DS1928

4.16.7.1 General information

The module is equipped with an EnDat encoder interface. The module automatically detects whether an encoder is connected with EnDat 2.1 or EnDat 2.2. This module can be used to evaluate encoders installed in B&R servo motors as well as encoders for external axes (encoders that scan any machine movement). The input signals are monitored. This makes it possible to detect open or shorted lines as well as encoder supply failures.

- EnDat 2.1 and EnDat 2.2 encoder interface
- Encoder input monitoring
- 5 VDC and GND for encoder supply
- NetTime function: Time stamp for position

EnDat encoders

EnDat is a standard developed by Johannes Heidenhain GmbH (www.heidenhain.de) that incorporates the advantages of absolute and incremental position measurement and also offers a read/write parameter memory in the encoder. With absolute position measurement, the homing procedure is generally not required. Where necessary a multi-turn encoder should be installed. To save costs, a single-turn encoder and a reference switch can also be used. In this case, a homing procedure must be carried out.

NetTime position timestamp

Highly dynamic positioning tasks require not only the position value, but also the exact time at which the position was determined. The module has a NetTime function for this, which adds a timestamp to the recorded position with microsecond accuracy.

The module provides the PLC with the position value and timestamp as absolute time value. The NetTime mechanisms ensure that the PLC NetTime clock and the local NetTime clock on the module have exactly the same absolute time at all times.

4.16.7.2 Order data

Model number	Short description	Figure
	Digital signal processing and preparation	
X20DS1928	X20 digital signal module, 1 EnDat 2.1/2.2 interface, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 369: X20DS1928 - Order data

4.16.7.3 Technical data

Product ID	X20DS1928
Short description	
I/O module	1x EnDat interface
General information	
B&R ID code	0xA912
Status indicators	Counting direction, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Counting direction	Yes, using status LED
Power consumption	
Bus	0.01 W
Internal I/O	1.3 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Encoder inputs	
Type	EnDat 2.1/2.2
Angular position resolution	13-bit, with a 1 V_{SS} signal
Encoder monitoring	Yes
Max. encoder cable length	10 m, with a line cross-section 4x 2x 0.14 mm² and 1x 2x 0.5 mm²
Sine/Cosine inputs	
Signal transmission	Differential signals, symmetrical
Signal frequency	DC up to 400 kHz
Differential voltage	1 V_{SS}
Common-mode voltage	Max. ±10 V
Terminating resistor	120 Ω
Encoder supply	
Output voltage	5 V (±5%)
Load capability	300 mA
Protective measures	
Overload protection	Yes
Short circuit protection	Yes
Serial EnDat interface	
Signal transmission	5 VDC differential signal, EiA RS-485 standard
Transmission status	See EnDat specification
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 370: X20DS1928 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.16.7.4 Status LEDs

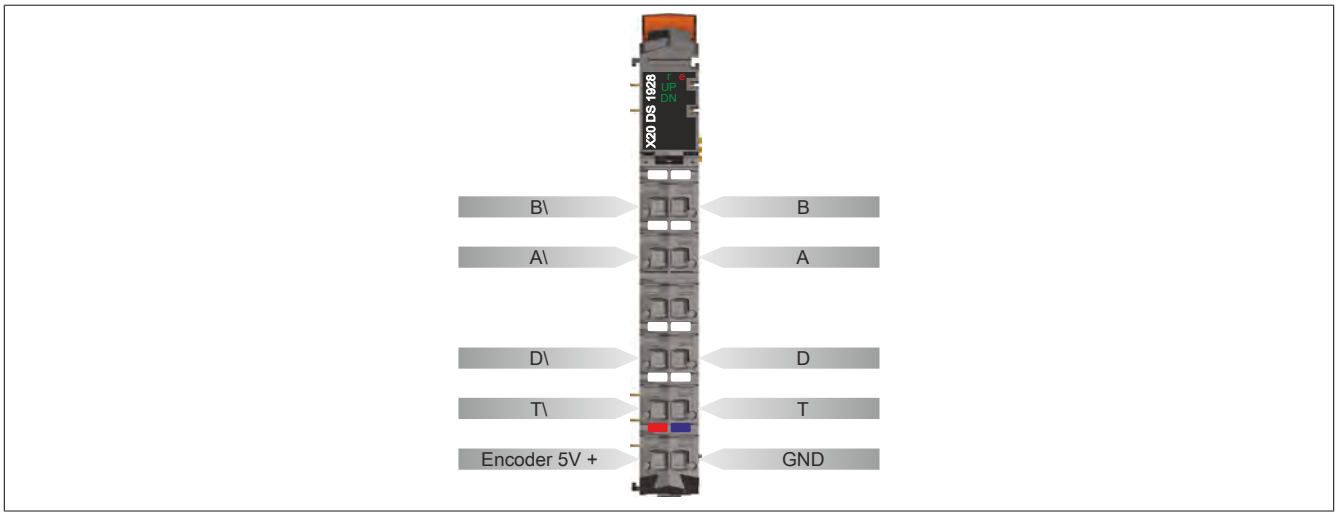
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Image	LED	Color	Status	Description
	r	Green	Off	Module supply not connected
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything is OK
			On	Error or reset state - Possible cause: • Encoder supply error
			Single flash	I/O error - Possible causes: • Sine/Cosine relative position error (open line) • Sine/Cosine absolute position error (reference)
			Double flash	System error - Possible causes: • EnDat communication error • EnDat position error • EnDat error defining parameters
			Tripple flash	I/O error and system error
			Single flash, inverted	Error or reset state and I/O error
			Double flash, inverted	Error or reset state and system error
			Triple flash, inverted	Error or reset state, I/O error and system error
	UP	Green	On	The "UP/DN" LEDs are lit depending on the rotational direction and the speed of the connected encoder. The "UP" LED indicates when the encoder position changes in the positive direction.
	DN	Green	On	The "DN" LED indicates when the encoder position changes in the negative direction.

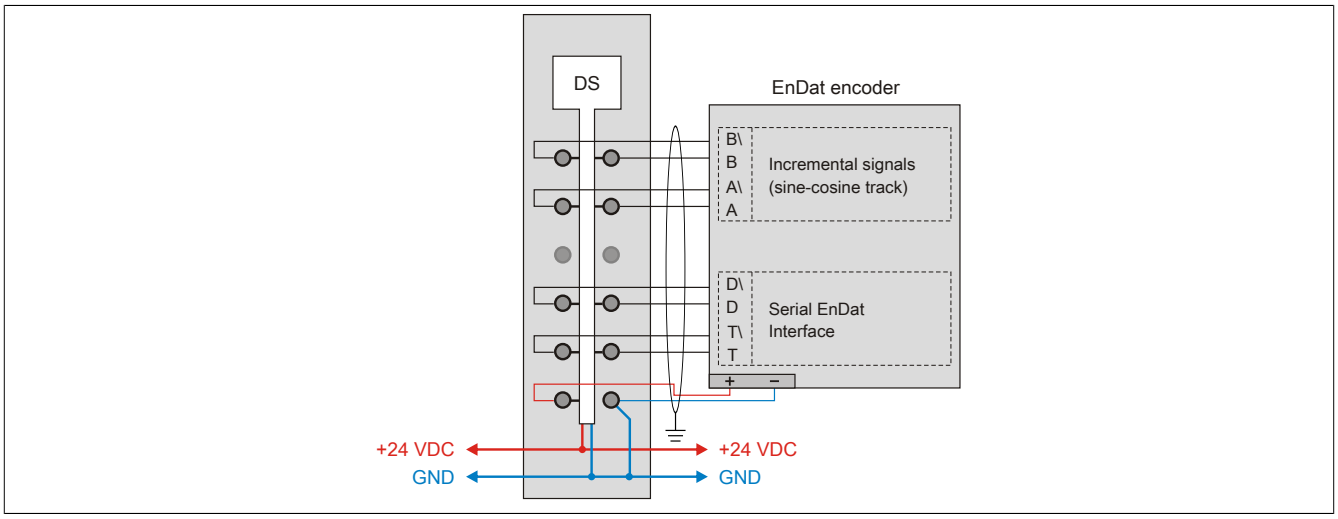
1) Depending on the configuration, a firmware update can take up to several minutes.

4.16.7.5 Pinout

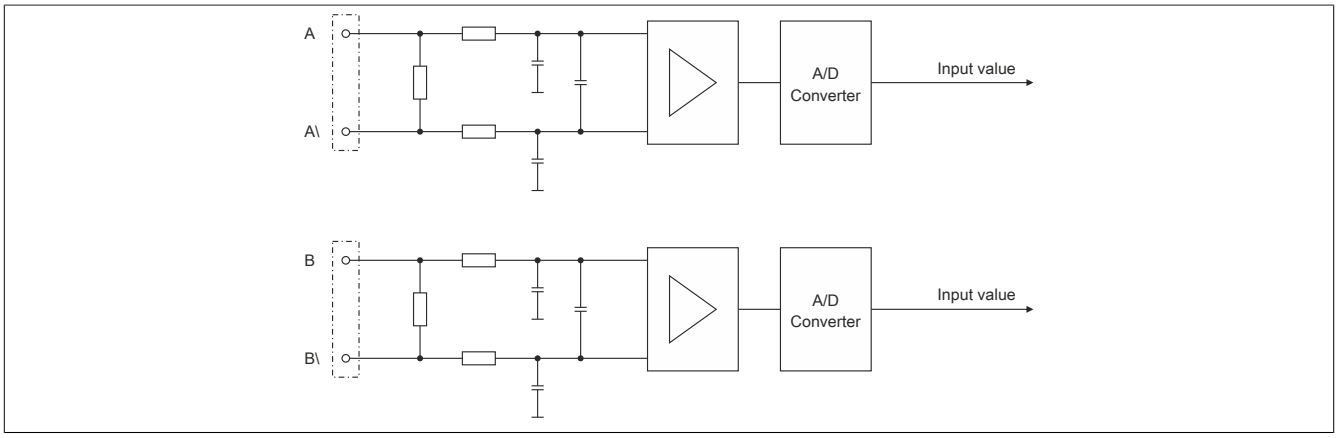
Shielded cables should be used for all signal lines.



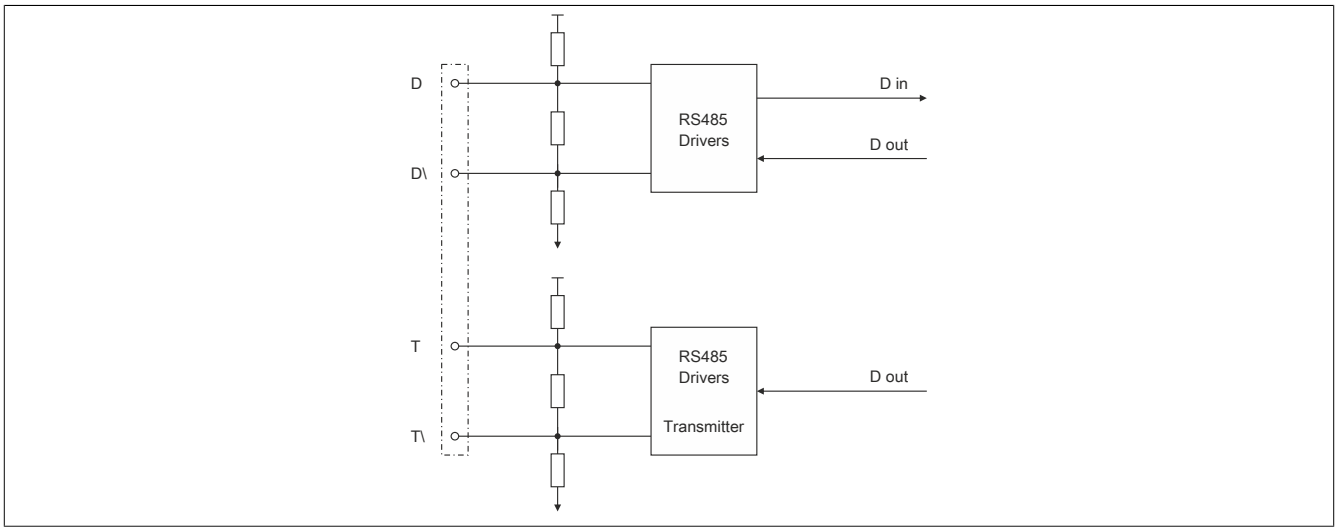
4.16.7.6 Connection example



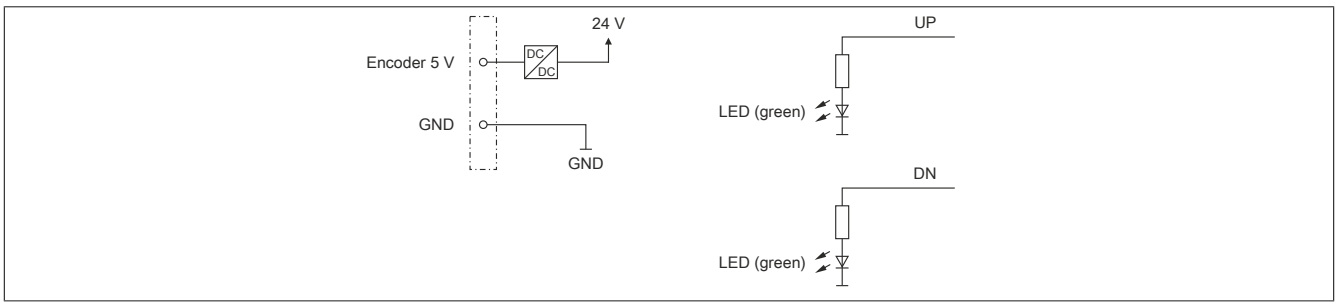
4.16.7.7 Input diagram for the incremental signals (sine-cosine track)



4.16.7.8 Input diagram for the serial EnDat interface



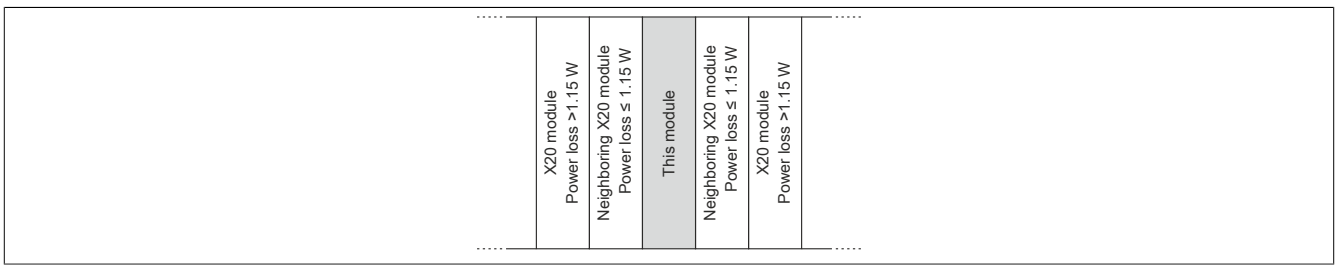
4.16.7.9 Encoder supply scheme and LEDs



4.16.7.10 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.16.7.11 Register description

4.16.7.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.16.7.11.2 Register overview - Function model 0 (standard)

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module configuration						
513	CfO_SIframeGenID	USINT				•
654	CfO_SystemCyclePrescaler	UINT				•
Basic functions						
683	SDCLifeCount	SINT	•			
4180	PositionHW	UDINT	•			
4188	PositionLW	UDINT	•			
	Position	DINT				
4172	PosTime (32-Bit)	DINT	•			
4174	PosTime (16-Bit)	INT	•			
4163	PosCycle	SINT	•			
Error management						
389	ErrorEnableID_1710	USINT				•
261	ErrorInfo	USINT	•			
	EncoderSupplyError	Bit 0				
	VssCheckError	Bit 2				
	SinCosPosError	Bit 3				
	EnDatComError	Bit 4				
	EnDatPosError	Bit 5				
	EnDatParSetError	Bit 6				
	EnDatRefWarning	Bit 7				
325	AckErrorInfo	USINT			•	
	AckEncoderSupplyError	Bit 0				
	AckVssCheckError	Bit 2				
	AckSinCosPosError	Bit 3				
	AckEnDatComError	Bit 4				
	AckEnDatPosError	Bit 5				
	AckEnDatParSetError	Bit 6				
	AckEnDatRefWarning	Bit 7				
4352	EnDatError	UINT	•			
4353	EnDatWarning	UINT	•			
4099	Acknowledging EnDat errors	USINT			•	
	EnDatAck	Bit 0				
Sin/Cos - Configuration						
1025	SinCosEnable	USINT				•
1027	SinCosRefSource	USINT				•
1034	SinCosVssMin	UINT				•
1038	SinCosVssMax	UINT				•
1044	SinCosQuitTime	UDINT				•
EnDat - Read ID						
4097	EnDatMode	USINT				•
4400 + N	OperatingParam_N (index N = 00 to 15)	UINT		•		
4352 + N	OperatingStatus_0N (index N = 0 to 3)	UINT		•		
4352 + N	ParamManuf_N (index N = 04 to 47)	UINT		•		
4416 + N	ParamManufEnDat22_N (index N = 01 to 63)	UINT		•		
EnDat - Read additional information						
4860 + N*8	EnDatInfoCmd0N (index N = 1 to 4)	UDINT				•
4935	Validity of info data	USINT	•			
	EnDatInfoOK01	Bit 0				
	...	...				
	EnDatInfoOK04	Bit 3				
4978 + N*16	EnDatInfo0N (index N = 1 to 4)	UINT	•			
		INT				
Flatstream mode						
4609	OutputMTU	USINT				•
4611	InputMTU	USINT				•
4613	FlatStreamMode	USINT				•
4615	Forward	USINT				•
4620	ForwardDelay	UINT				•

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
4672	InputSequence	USINT	●			
4672 + N	RxByteN (index N = 1 to 15)	USINT	●			
4704	OutputSequence	USINT			●	
4704 + N	TxByteN (index N = 1 to 15)	USINT			●	

4.16.7.11.3 Register overview - Function model 254 (bus controller)

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Module configuration							
513	-	CfO_SIframeGenID	USINT				●
654	-	CfO_SystemCyclePrescaler	UINT				●
Basic functions							
4180	0	PositionHW	UDINT	●			
4188	4	PositionLW	UDINT	●			
4163	15	PosCycle	SINT	●			
Error management							
389	-	ErrorEnableID_1710	USINT				●
261	14	ErrorInfo	USINT	●			
		EncoderSupplyError	Bit 0				
		VssCheckError	Bit 2				
		SinCosPosError	Bit 3				
		EnDatComError	Bit 4				
		EnDatPosError	Bit 5				
		EnDatParSetError	Bit 6				
		EnDatRefWarning	Bit 7				
325	6	AckErrorInfo	USINT			●	
		AckEncoderSupplyError	Bit 0				
		AckVssCheckError	Bit 2				
		AckSinCosPosError	Bit 3				
		AckEnDatComError	Bit 4				
		AckEnDatPosError	Bit 5				
		AckEnDatParSetError	Bit 6				
		AckEnDatRefWarning	Bit 7				
4352	-	EnDatError	UINT		●		
4353	-	EnDatWarning	UINT		●		
4099	-	Acknowledging EnDat errors	USINT				●
		EnDatAck	Bit 0				
Sin/Cos - Configuration							
1025	-	SinCosEnable	USINT				●
1027	-	SinCosRefSource	USINT				●
1034	-	SinCosVssMin	UINT				●
1038	-	SinCosVssMax	UINT				●
1044	-	SinCosQuitTime	UDINT				●
EnDat - Read ID							
4097	-	EnDatMode	USINT				●
4400 + N	-	OperatingParam_N (index N = 00 to 15)	UINT		●		
4352 + N	-	OperatingStatus_0N (index N = 0 to 3)	UINT		●		
4352 + N	-	ParamManuf_N (index N = 04 to 47)	UINT		●		
4416 + N	-	ParamManufEnDat22_N (index N = 01 to 63)	UINT		●		
EnDat - Read additional information							
4860 + N*8	-	EnDatInfoCmd0N (index N = 1 to 4)	UDINT				●
4935	-	Validity of info data	USINT		●		
		EnDatInfoOK01	Bit 0				
		...	...				
		EnDatInfoOK04	Bit 3				
4978 + N*16	-	EnDatInfo0N (index N = 1 to 4)	UINT		●		
			INT				
Flatstream mode							
4609	-	OutputMTU	USINT				●
4611	-	InputMTU	USINT				●
4613	-	FlatStreamMode	USINT				●
4615	-	Forward	USINT				●
4620	-	ForwardDelay	UINT				●
4672	8	InputSequence	USINT	●			
4672 + N	9 - 13	RxByteN (index N = 1 to 5)	USINT	●			
4704	0	OutputSequence	USINT			●	
4704 + N	1 - 5	TxByteN (index N = 1 to 5)	USINT			●	

1) The offset specifies the position of the register within the CAN object.

4.16.7.11.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.16.7.11.4 Module configuration

The following configuration registers can be used to define various module settings. They can be used, for example, to modify the module's behavior on an X2X Link network. The user can choose between 2 option registers.

4.16.7.11.4.1 Data query

Name:
CfO_SIframeGenID

This register can be used to define when the synchronous/cyclic input data is generated. "X2X cycle optimized" should be set for jitter-free data acquisition. "Fast reaction" can be set for the best performance.

Data type	Value	Information
USINT	9	Fast reaction
	14	X2X cycle optimized (bus controller default setting)

4.16.7.11.4.2 Prescale factor

Name:
CfO_SystemCyclePrescaler

In order for the module to communicate with the CPU as well as the EnDat encoder, the EnDat cycle time must be at least twice the module cycle time. The actual EnDat cycle time is a result of multiplying the module cycle time by the value in this register.

Data type	Value	Information
UINT	2	EnDat cycle: 200 to 400 µs (bus controller default setting)
	4	EnDat cycle: 400 to 800 µs
	8	EnDat cycle: 800 to 1,600 µs

4.16.7.11.5 Basic functions

This module can import a position when used together with an EnDat encoder. The received data is prepared in 2 different formats and given a time stamp. Six registers are available for further processing. This allows the user to select the format that best fits the application at hand.

4.16.7.11.5.1 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.16.7.11.5.2 Absolute position values

Name:
PositionHW
PositionLW

The absolute position of the encoder is defined using 64-bit resolution. The position value is stored in the PositionHW and PositionLW registers. The upper 32 bits are stored the PositionHW register, while the lower 32 bits are stored in the PositionLW register.

For SinCos signal evaluation, see 4.16.3.11.7.1 "Format of the SinCos signal" for information regarding the data format.

Data type	Value
2x UDINT	0 to 4,294,967,295

4.16.7.11.5.3 SDC position value

Name:
Position

The SDC library requires a signed 32-bit position value. The position's low word can be accessed separately for this. The value can also be used as default position value, however.

For SinCos signal evaluation, see 4.16.3.11.7.1 "Format of the SinCos signal" for information regarding the data format.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.16.7.11.5.4 NetTime of the position values

Name:
PosTime

This register is used to assign each recorded position of the current NetTime value. The NetTime is recorded with µs accuracy.
The SDC library requires a 16 bit value. The NetTime value is therefore also generated in this format.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	NetTime in µs
INT	-32,768 to 32,767	

4.16.7.11.5.5 Counter for position values

Name:
PosCycle

PosCycle is an integer counter that is incremented as soon as the module has saved a new valid position value.

Data type	Value
SINT	-128 to 127

4.16.7.11.6 Error management

This module can be used to diagnose error states. There are the following ways in which this is done:

- Module-based diagnostics
- EnDat-based diagnostics

4.16.7.11.6.1 Module-based diagnostics

The module diagnoses 7 different errors or warnings. Depending on the settings, the error bits can be called either individually or packed together.

Configuring errors and warnings

Name:
ErrorEnableID_1710

The implemented diagnostic algorithms can be enabled or disabled in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Encoder supply:	0	Error detection disabled
		1	Error detection enabled (Bus Controller default setting)
1	Reserved	-	
2	Vss Sin/Cos:	0	Error detection disabled
		1	Error detection enabled (Bus Controller default setting)
3	Position error:	0	Error detection disabled
		1	Error detection enabled (Bus Controller default setting)
4	EnDat - Communication:	0	Error detection disabled
		1	Error detection enabled (Bus Controller default setting)
5	EnDat - Position:	0	Error detection disabled
		1	Error detection enabled (Bus Controller default setting)
6	EnDat - Parameters:	0	Error detection disabled
		1	Error detection enabled (Bus Controller default setting)
7	EnDat - Reference warning:	0	Warning disabled
		1	Warning enabled (Bus Controller default setting)

Encoder supply:

The encoder voltage supply is below the permitted limit.

Vss Sin/Cos:

The voltage value for the Sin/Cos track violates the configured limit values.
→ See register 4.16.3.11.7.4 "SinCosVssMin" or 4.16.3.11.7.5 "SinCosVssMax".

Position error:

The determined position value violates the requirements of the application.

EnDat - Communication:

Communication error on the EnDat interface (e.g. incorrect checksum)

EnDat - Position:

Encoder evaluates the determined position value as invalid.

EnDat - Parameters:

Inconsistent register values for encoder identification
→ Countermeasures: Check wiring or rescan (see "EnDatAck")

EnDat - Reference warning:

The digital interface provides an absolute position value that can be used to accurately describe the axis position. The position value is homed to this absolute value at the beginning of a measurement. The analog interface can be used to incrementally sample changes that occur very rapidly. This enables the module to continue sampling the position value at a high resolution. Both the analog and the digital signal are sampled cyclically. If the value determined incrementally deviates from the absolute value during operation then the referencing warning is displayed and the position must be referenced again.

Status of errors and warnings

Name:
ErrorInfo

EncoderSupplyError
VssCheckError
PositionError
EnDatComError
EnDatPosError
EnDatParSetError
EnDatRefWarning

This register indicates which error or warning is currently active. For a description of errors, see "Configuring errors and warnings".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EncoderSupplyError	0	No error
		1	Encoder supply error
1	Reserved	-	
2	VssCheckError	0	No error
		1	Vss error on Sin/Cos track
3	PositionError	0	No error
		1	Position error
4	EnDatComError	0	No error
		1	EnDat communication error
5	EnDatPosError	0	Error detection disabled
		1	Error detection enabled
6	EnDatParSetError	0	Error detection disabled
		1	Error detection enabled
7	EnDatRefWarning	0	Warning disabled
		1	Warning enabled

Acknowledging errors and warnings

Name:
AckErrorInfo

AckEncoderSupplyError
AckVssCheckError
AckPositionError
AckEnDatComError
AckEnDatPosError
AckEnDatParSetError
AckEnDatRefWarning

This register is used to acknowledge an error message that occurred in the "Status of errors and warnings" register. For a description of errors, see "Configuring errors and warnings".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	AckEncoderSupplyError	0	No error acknowledgment
		1	Error acknowledgment
1	Reserved	-	
2	AckVssCheckError	0	No error acknowledgment
		1	Error acknowledgment
3	AckPositionError	0	No error acknowledgment
		1	Error acknowledgment
4	AckEnDatComError	0	No error acknowledgment
		1	Error acknowledgment
5	AckEnDatPosError	0	No error acknowledgment
		1	Error acknowledgment
6	AckEnDatParSetError	0	No error acknowledgment
		1	Error acknowledgment
7	AckEnDatRefWarning	0	No acknowledgment
		1	Acknowledgment

4.16.7.11.6.2 EnDat-based diagnostics

Memory areas are provided in the EnDat standard for error handling. Error management was tailored to utilize error detection according to the EnDat standard. Additional registers were implemented in the module which prepare these areas in the encoder memory.
The module allows access to all previously defined memory areas for error handling. The memory areas are mirrored in the module registers and can be interpreted by the user.
Detailed information regarding the errors that can be detected in this way can be found in the encoder's manual.

EnDat errors

Name:
EnDatError

This register is used to indicate critical conditions on the EnDat encoder. The system has generally ceased to work and requires service.

Data type	Value
UINT	See bit structure.

The bit structure described below is designed according to the general recommendations of the EnDat standard. The specification does not limit which trigger algorithms to use or which of the listed messages must be supported. Please refer to the encoder's manual for further details.

Bit structure:

Bit	Name	Value	Information
0	Illumination	0	OK
		1	Failed
1	Signal amplitude	0	OK
		1	Detected as having errors
2	Position value	0	OK
		1	Detected as having errors
3	Overvoltage	0	No
		1	Yes
4	Undervoltage	0	No
		1	Yes
5	Overcurrent	0	No
		1	Yes
6	Battery	0	OK
		1	Must be changed
7 - 15	Reserved	-	

EnDat warnings

Name:
EnDatWarning

This register is used to indicate critical conditions on the EnDat encoder. Encoder still functional, but must be checked immediately. This generally means that defined tolerances have been exceeded.

Data type	Value
UINT	See bit structure.

The bit structure described below is designed according to the general recommendations of the EnDat standard. The specification does not limit which trigger algorithms to use or which of the listed messages must be supported. Please refer to the encoder's manual for further details.

Bit structure:

Bit	Name	Value	Information
0	Frequency collision	0	No
		1	Yes
1	Temperature exceeded	0	No
		1	Yes
2	Control reserve - Lighting	0	Not required
		1	Required
3	Charge - Battery	0	OK
		1	Low
4	Reference point	0	Reached
		1	Not reached
5 - 15	Reserved	-	

Acknowledging EnDat errors

Name:
EnDatAck

"EnDatAck" acknowledges all errors and warnings from the "EnDatError" and "EnDatWarning" registers. It can also instruct the module to re-import the parameters for identification.

If one of the bits in this register is set, the system automatically resets it and the respective algorithm is run.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EnDatAck	0	No acknowledgment
		1	Acknowledge
1	Rescan - Identification register	0	Imported parameters retained
		1	Reimport parameters
2 - 7	Reserved	-	

4.16.7.11.7 Sin/Cos - Analog interface configuration

In addition to the digital EnDat interface, this module is also equipped with an analog interface for sampling a differential sine-cosine signal. To increase the resolution, the EnDat standard specifies a cooperation between the analog and digital information. This enables a highly dynamic representation of the position while maintaining high resolution.

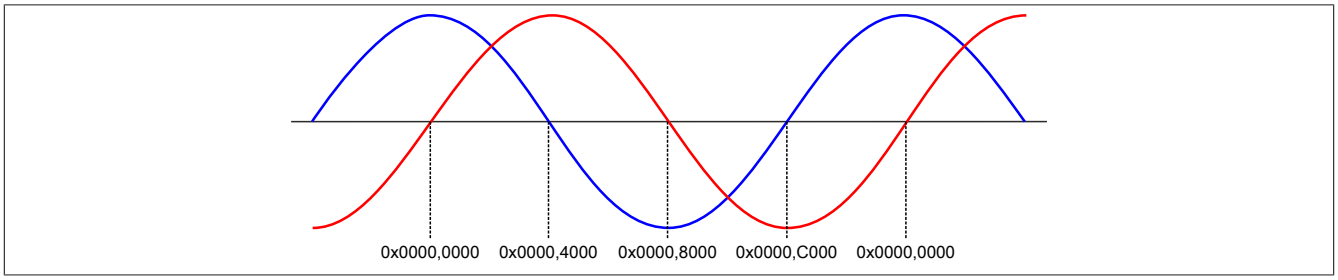
4.16.7.11.7.1 Format of the SinCos signal

The SinCos signal is represented as a position value in the 4.16.3.11.5.2 "Absolute position values" and 4.16.3.11.5.3 "SDC position value" registers. The following relationships apply:

- PositionLW and Position are identical in the function.
- PositionHW extends the integer range of PositionLW by adding multi-turn functionality.

64-bit register	PositionHW (unsigned)	PositionLW (unsigned)	
32-bit register	-	Position (signed)	
Format	Integer extension (to 48-bit)	Integer (16-bit)	Decimal places: (with 13-bit resolution)
Information		A full sine wave corresponds to an increment of the integer.	**15** **14** **13** **12** **11** **10** **9** **8** **7** **6** **5** **4** **3** **2** **1** **0** x x x x x x x x x x x x x 0 0 0 **Important:** The lower 3 bits always contain the value 0.
Word/DWord	DWord	Word 1	Word 0

Relationship between sine curve (red) and decimal places:



4.16.7.11.7.2 Enabling SinCos

Name:
SinCosEnable

This register must always have the value 1 for configuration reasons.

Data type	Value	Information
USINT	1	Bus controller default: 1

4.16.7.11.7.3 Enabling SinCos reference source

Name:
SinCosRefSource

This register must always have the value 1 for configuration reasons.

Data type	Value	Information
USINT	1	Bus controller default: 1

4.16.7.11.7.4 Configuring the lower Vss value

Name:
SinCosVssMin

This register specifies the lower limit value for the peak-to-peak voltage of the sine/cosine track. The incoming signal is monitored in this way. If the incoming value falls below this specified limit, then the module reports the corresponding error.

Data type	Value	Information
UINT	0 to 1500	Values in mV, bus controller default setting: 800

4.16.7.11.7.5 Configuring the upper Vss value

Name:
SinCosVssMax

This register specifies the upper limit value for the peak-to-peak voltage of the sine/cosine track. The incoming signal is monitored in this way. If the incoming value exceeds this specified limit, then the module reports the corresponding error.

Data type	Value	Information
UINT	0 to 1500	Values in mV, bus controller default setting: 1200

4.16.7.11.7.6 Configuring the delay time after errors

Name:
SinCosQuitTime

If an error is detected on the analog interface, the last correctly read values remain valid. An interval can be defined in this register at which the module begins receiving correct values again after the error state without processing them further internally. Only then will newly sampled correct analog values be recognized as valid.

Data type	Value	Information
UDINT	0 to 20000000	Values in µs, bus controller default setting: 100000

4.16.7.11.8 EnDat

4.16.7.11.8.1 EnDat - Digital interface configuration

The EnDat interface allows you to establish a point-to-point connection with exactly one EnDat encoder.

There are 2 ways to use the encoder data in the PLC program. One is to store the necessary encoder values temporarily in the module, where they can then be provided to the CPU. The other is to use the module's FlatStream mode, which supports the full range of commands defined in the EnDat specification.

Detailed information about the EnDat specification can be found in the document, "Technical Information – EnDat 2.2".

Configuring EnDat module properties

Name:
EnDatMode

This register is used to define various module properties.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EnDat interface	0	Disabled
		1	Enabled (bus controller default setting)
1	Format of imported position data	0	Unsigned (bus controller default setting)
		1	Signed
2	Fast EnDat cycle (6 MHz)	0	Enabled if encoder compatible (bus controller default setting)
		1	Disabled
3	Sin/Cos track	0	Enabled (bus controller default setting)
		1	Disabled
4 - 7	Reserved	-	

4.16.7.11.8.2 EnDat - Read ID

The EnDat interface does more than just help the user specify axis positions. It can also be used to readout certain data stored in the encoder memory.
The EnDat specification divides the encoder memory into logical groups. These include memory areas for the operating parameters, operating status, manufacturer parameters and manufacturer parameters according to EnDat 2.2.
The 4 most important memory areas are mirrored in the module registers. The information can be accessed in the application and used to identify a particular encoder.

Information:

There are different types of EnDat. Please keep this in mind. EnDat has been continuously expanded to include new technical possibilities while maintaining backward compatibility. Several advancements have been made to the standard, which has resulted in a non-uniform structure.

In general, data is queried from memory for identification purposes when the module is started. In addition, the data can be reimported using the "EnDatAck" register. The module reads the data from the encoder, which is then mapped for the PLC.

Operating Parameters

Name:
OperatingParam_00 to OperatingParam_15

These registers can be used to read out the current operating parameters. The data in these registers correspond exactly to the values on the encoder. More detailed information can be found in the encoder's manual or by referring to the latest EnDat specification.

Data type	Value
16x UINT	See encoder manual

Operating state

Name:
OperatingStatus_00 to OperatingStatus_03

This register can be used to read the encoder's current operating state. The first 2 registers from this group are identical to the "EnDatError" and "EnDatWarning" registers. A special setting is provided because they are update cyclically.
Information about write protection and other configuration settings is managed in registers 02 and 03. The data in these registers correspond exactly to the values on the encoder.
More detailed information can be found in the encoder's manual or by referring to the latest EnDat specification.

Data type	Value
4x UINT	See encoder manual

Manufacturer parameters

Name:
ParamManuf_04 to ParamManuf_47

These registers are used to prepare the manufacturer parameters according to the EnDat standard 2.1. The exact arrangement of information can be found in the documentation "Technical Information - EnDat 2.2".

Data type	Value
44x UINT	see "Technical Information - EnDat 2.2" or encoder manufacturer data

Additional manufacturer parameters according to EnDat 2.2

Name:
ParamManufEnDat22_00 to ParamManufEnDat22_63

These registers are used to prepare the manufacturer parameters according to the EnDat standard 2.2. The exact arrangement of information can be found in the documentation "Technical Information - EnDat 2.2".

Data type	Value
64x UINT	see "Technical Information - EnDat 2.2" or encoder manufacturer data

4.16.7.11.8.3 EnDat - Read additional information

In addition to the identification data, other information can also be accessed from the encoder. However, the following algorithm requires exact knowledge of the encoder's memory structure and the EnDat specification.

Configuration

There are 4 different channels that can be operated during a cycle. One register per channel each is used for configuration, (i.e. determines which data is read from the encoder and mirrored on the respective Info byte).

Transmitting EnDat commands

Name:
EnDatInfoCmd01 to EnDatInfoCmd04

This register controls which data is processed on the corresponding Info byte for each channel. The register consists of up to 4 separate 8-bit values.

Data type	Value
4x UDINT	See bit structure. Bus controller default: 0

Bit structure:

Bit	Name	Information	
0 - 7	Command	Selects the response section	
8 - 15	Memory area codes	MRS code	
		Parameters not in blocks	**Parameters arranged in blocks**
16 - 23	Memory ID	Parameter numbers	Block number
24 - 31	Memory ID	-	Parameter numbers

There is a difference when querying data from an encoder using an EnDat 2.1 command or an EnDat 2.2 command.
When querying encoder data with an EnDat 2.1 command (0x04 and 0x06), the parameter number and (optionally) the block number must be specified in addition to the MRS code.
When querying the memory with an EnDat 2.2 command, the parameter number and block number are not required. The module consecutively transmits all 4 words of the memory area, which was selected using the MRS code. The right command must be selected depending on which of the 4 response bytes is needed.

Memory area codes

The code to be defined is identical to the MRS code for the encoder memory. The EnDat specification has left a few of the encoders memory areas undefined and available for future developments. This is why a clear and reliable explanation cannot be provided here.
More detailed information can be found in the encoder's manual or by referring to the latest EnDat specification.

Parameter numbers

EnDat 2.1 requires the corresponding parameter number to be entered in order to specifically address the desired parameter in the encoder memory. Older EnDat versions did not divide the encoder memory into blocks. This is why there are memory areas that can be selected without specifying a block number. In this case, the parameter number must be entered on the third byte.
More detailed information can be found in the encoder's manual or by referring to the latest EnDat specification.

Block number

To expand the address range of the encoder memory, additional block numbers were added starting at the second section. If the desired parameter is located in this blocked area, then the block number must be specified on the third byte. In this case, the parameter number is entered on the fourth byte.
More detailed information can be found in the encoder's manual or by referring to the latest EnDat specification.

Call

After being configured correctly, the position value is transmitted cyclically to the module. Each channel has 2 registers that serve as temporary storage. The module confirms successful receipt by setting an OK bit. The EnDat specification does not specify in which format the parameters must be received. Therefore, the module provides the information in 2 ways. Which of the two registers should be used for further processing depends on the parameters being read.

Validity of info data

Name:
EnDatInfoOK01 to EnDatInfoOK04

This register's bits provide information about the validity of the current info data in temporary storage.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	EnDatInfoOK01	0	Value 01 invalid
		1	Value 01 valid
...	...	...	
3	EnDatInfoOK04	0	Value 04 invalid
		1	Value 04 valid
4 - 7	Reserved	-	

Reading EnDat information

Name:
EnDatInfo01 to EnDatInfo04

These registers provide the corresponding requested information as a signed or unsigned 2-byte value.
The EnDat specification does not specify the format of the received parameters. Which of the two data types should be used for further processing therefore depends on the parameter being read.

Data type	Value
UINT	0 to 65535
INT	-32,768 to 32,767

4.16.7.11.9 FlatStream communication

4.16.7.11.9.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

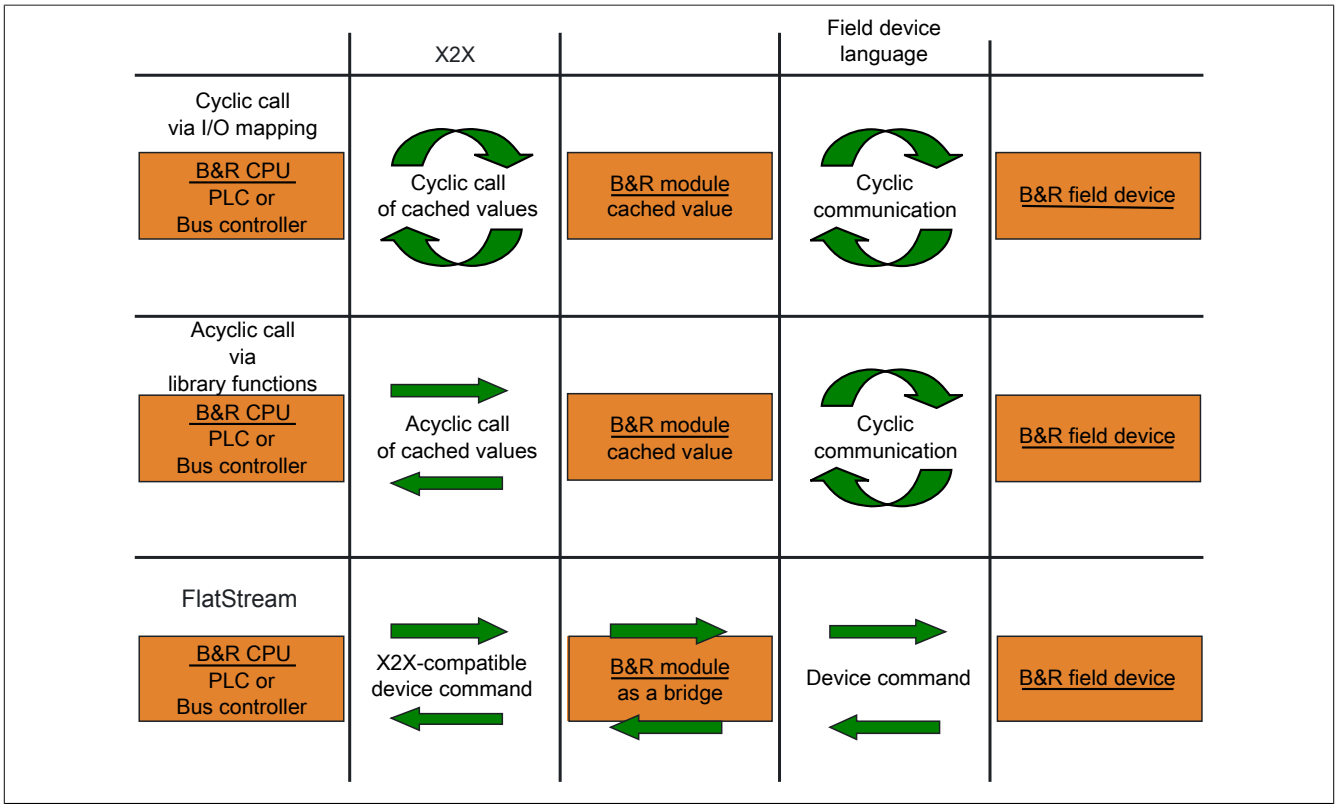


Figure 258: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.16.7.11.9.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.16.7.11.9.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

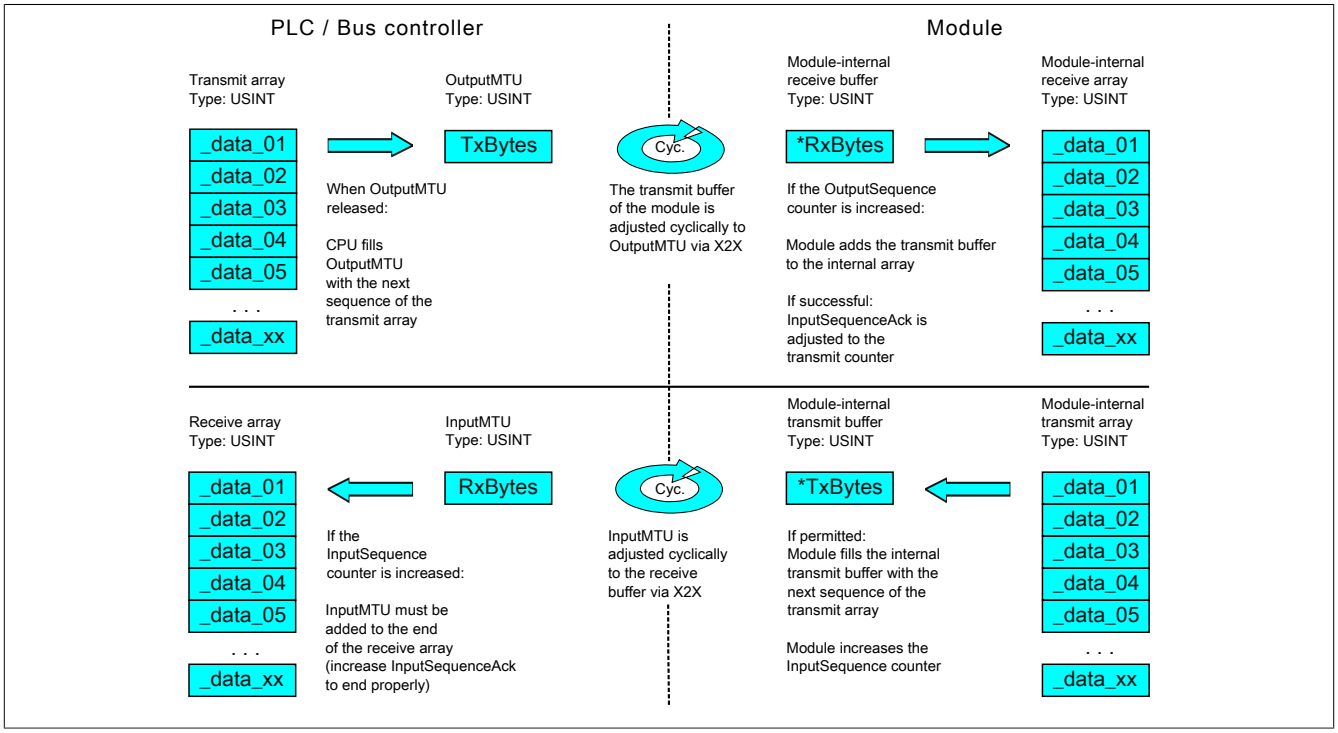


Figure 259: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.16.7.11.9.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

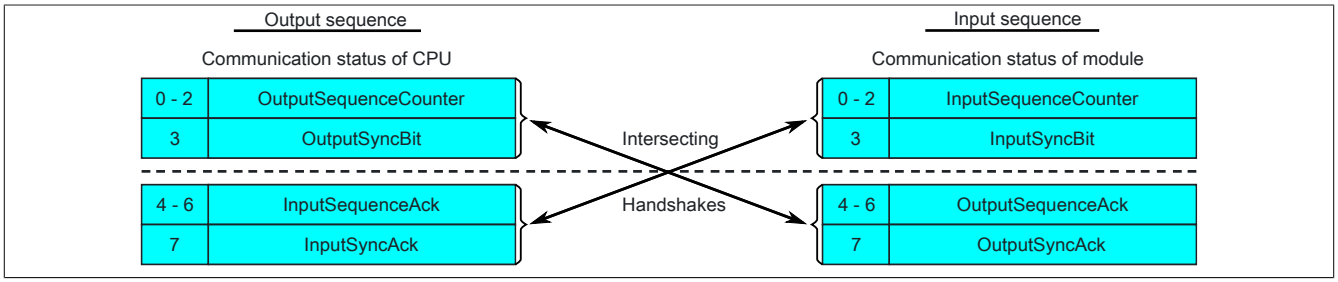


Figure 260: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

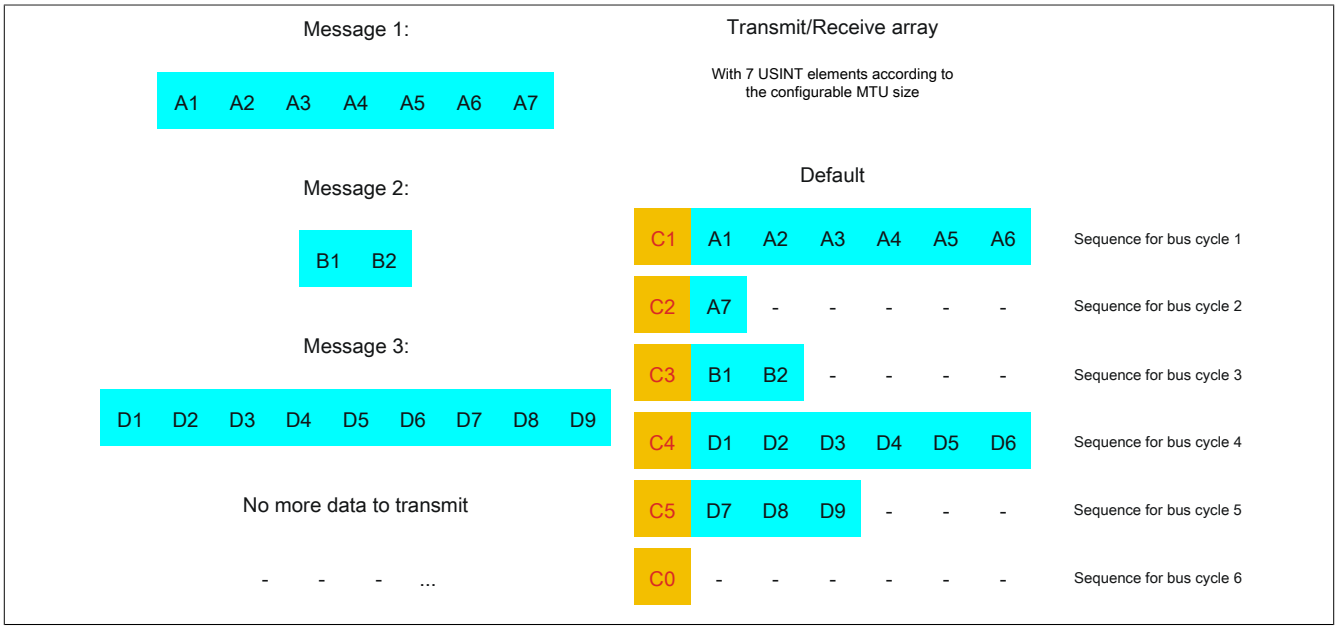


Figure 261: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 371: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 372: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

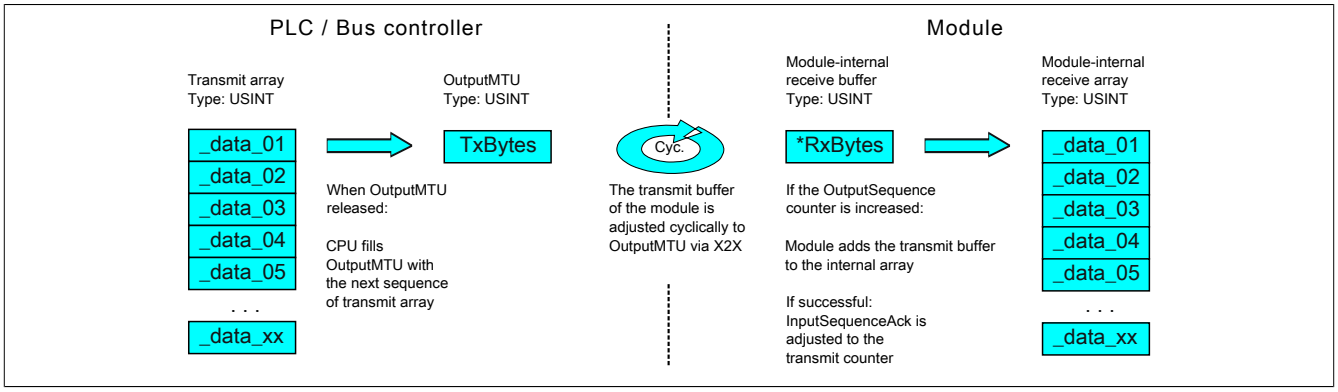


Figure 262: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

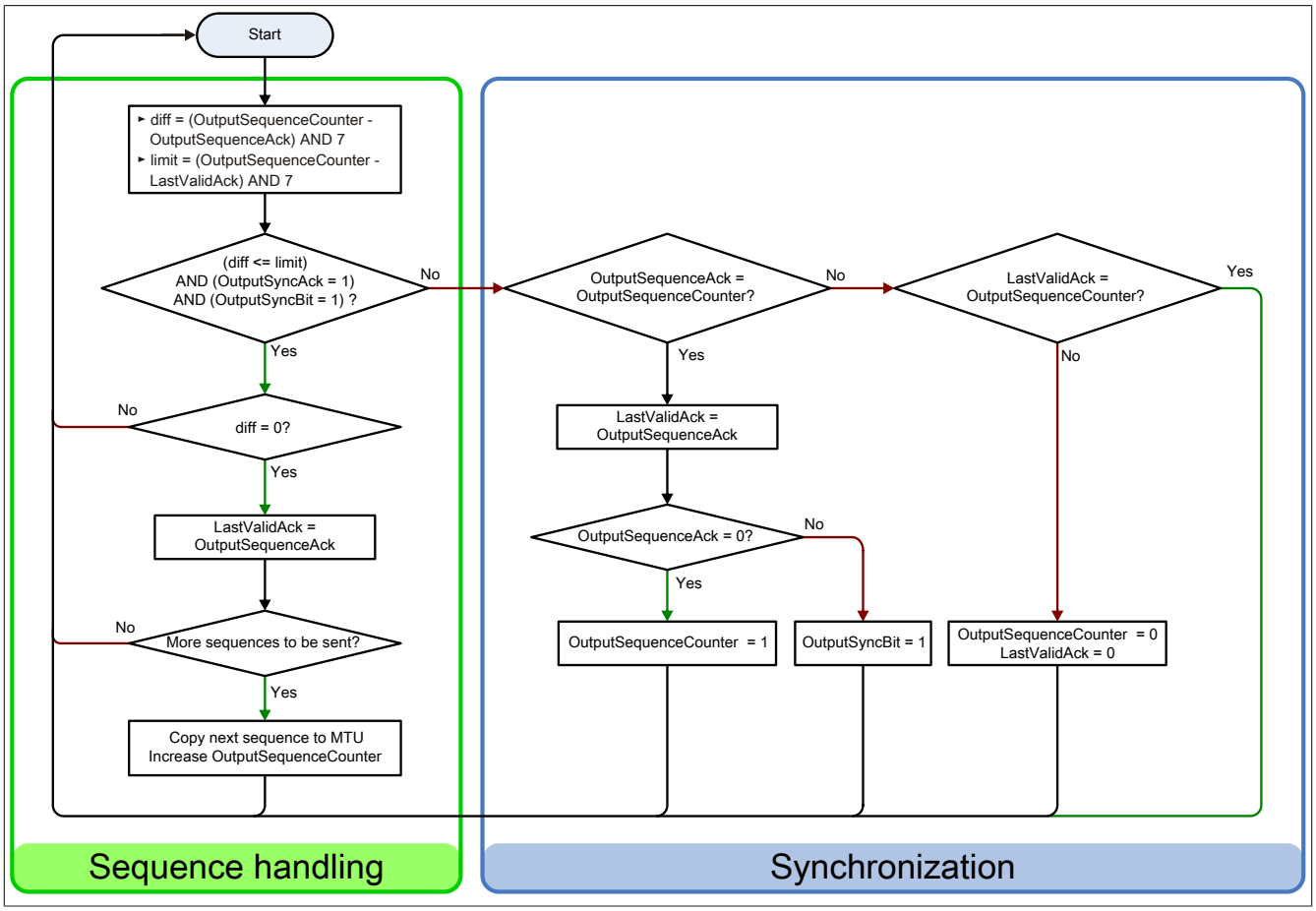


Figure 263: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

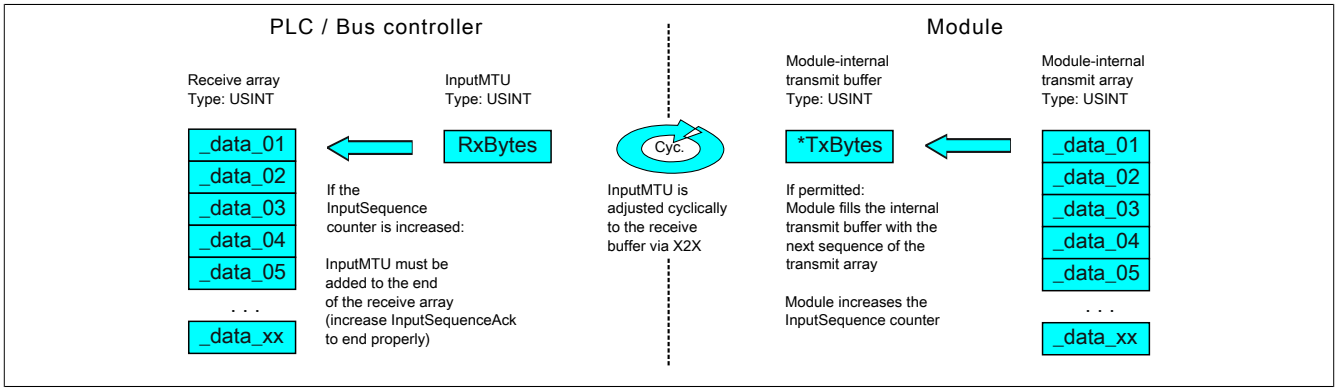


Figure 264: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

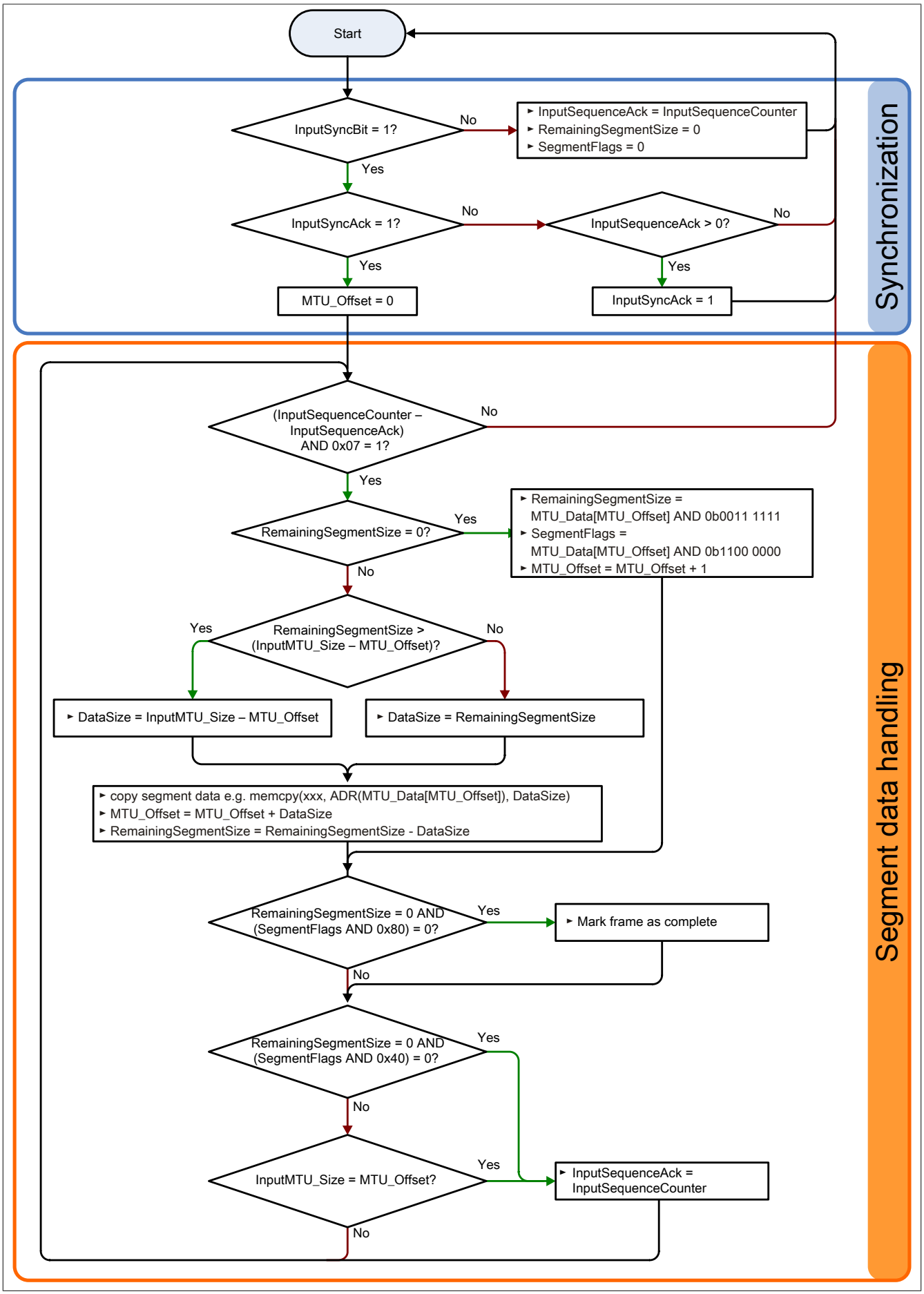


Figure 265: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

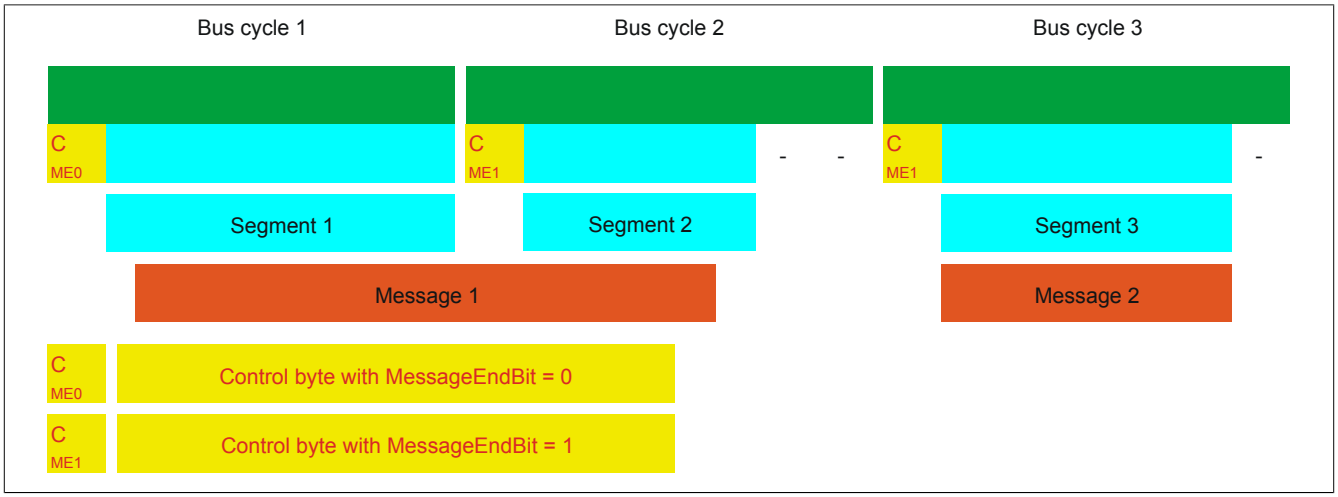


Figure 266: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

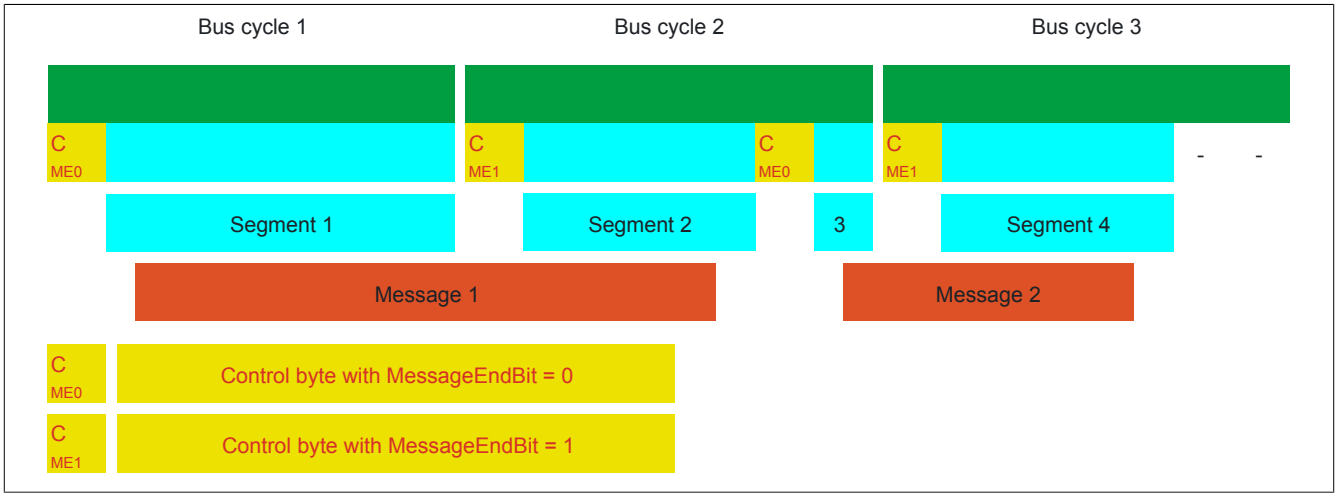


Figure 267: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

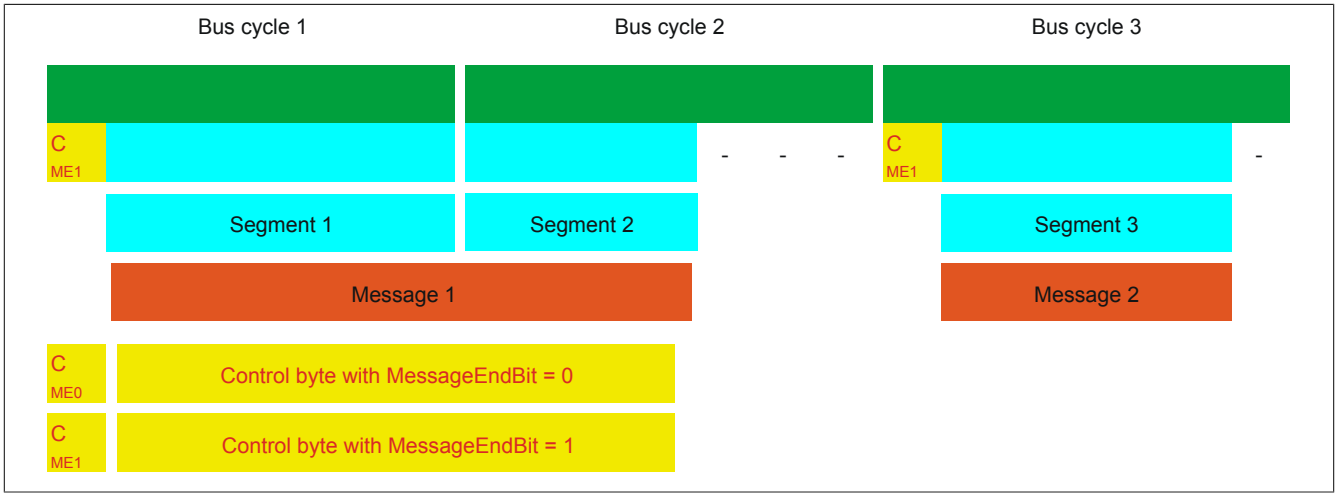


Figure 268: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

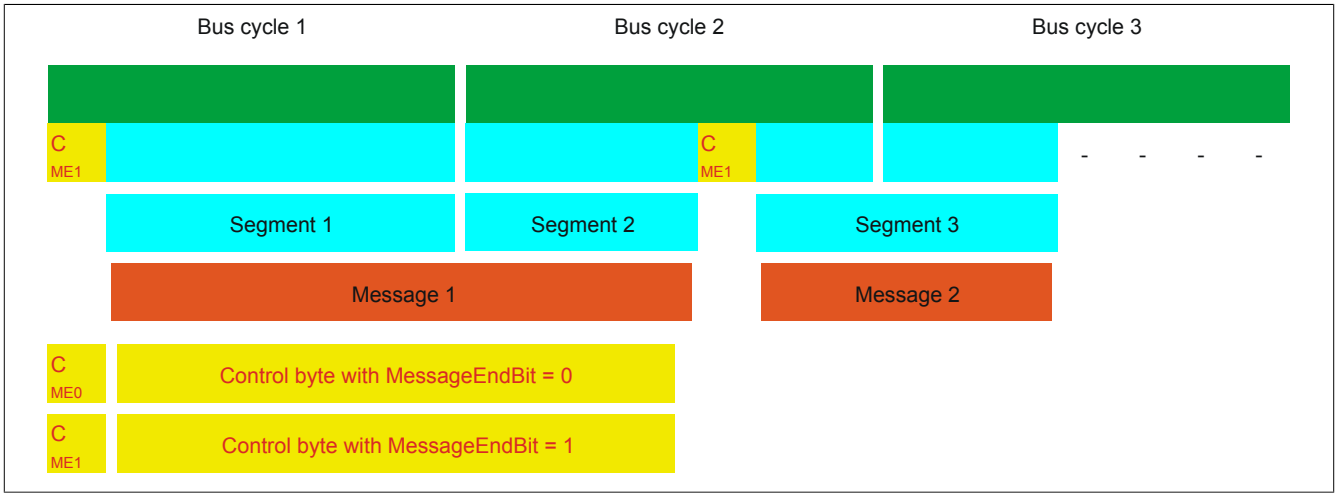


Figure 269: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

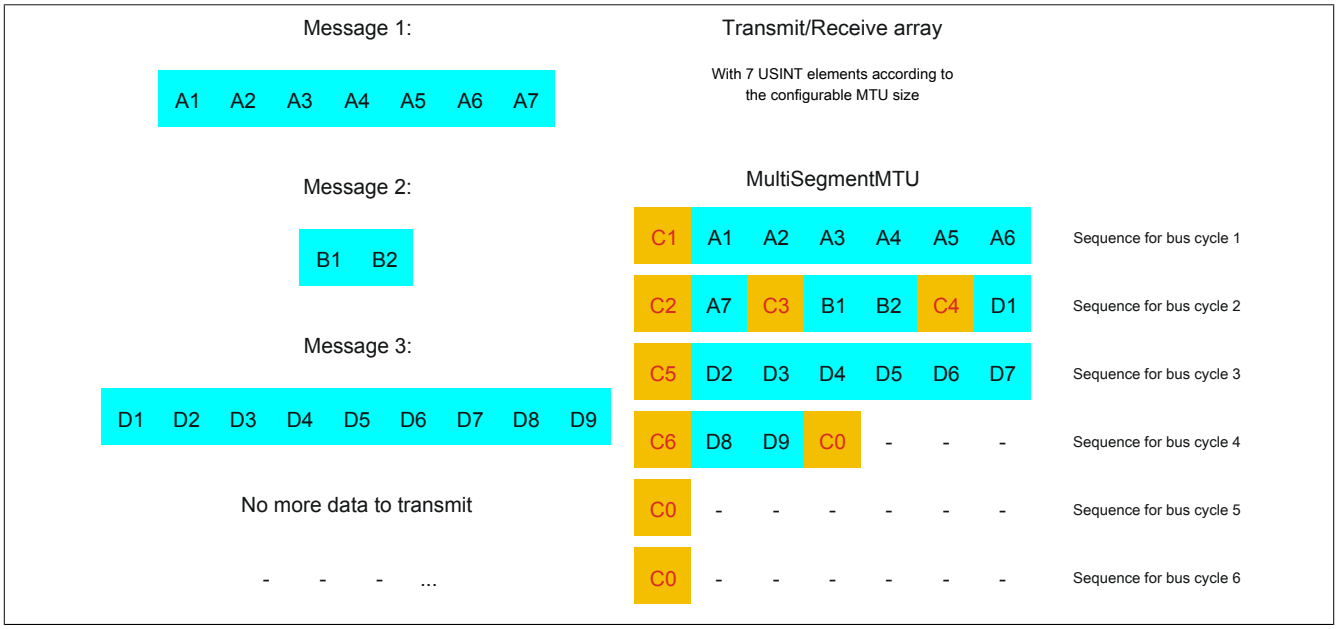


Figure 270: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			**C2 (control byte 2)**			**C3 (control byte 3)**		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 373: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			**C5 (control byte 5)**			**C6 (control byte 6)**		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 374: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

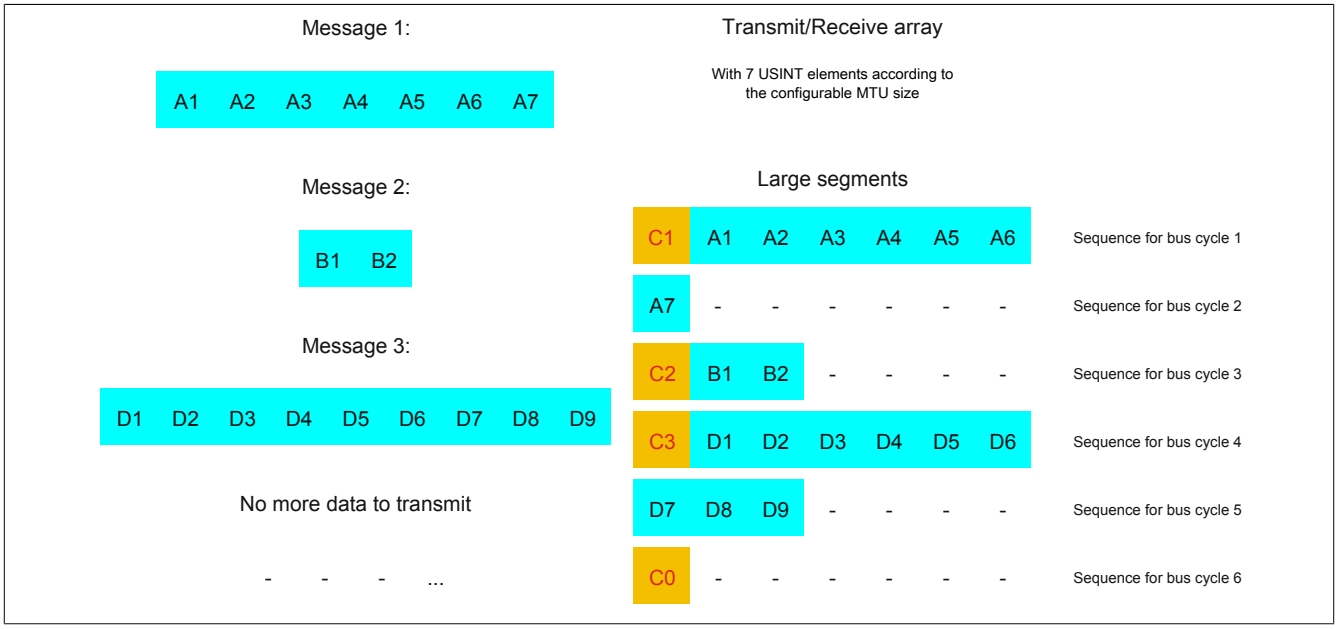


Figure 271: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 375: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

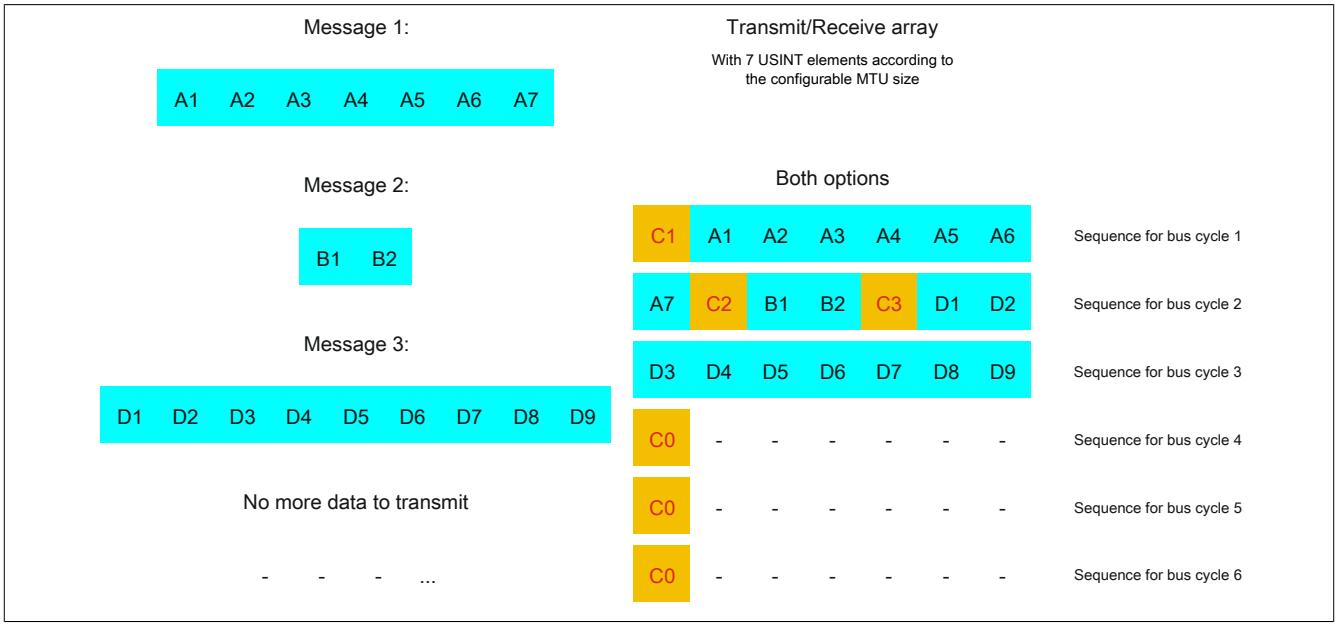


Figure 272: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 376: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.16.7.11.9.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

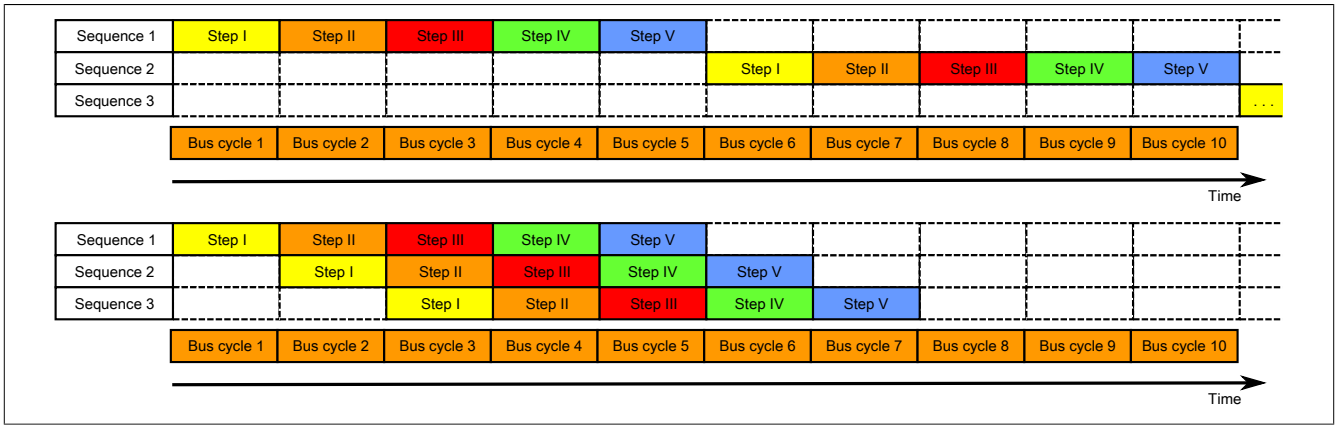


Figure 273: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

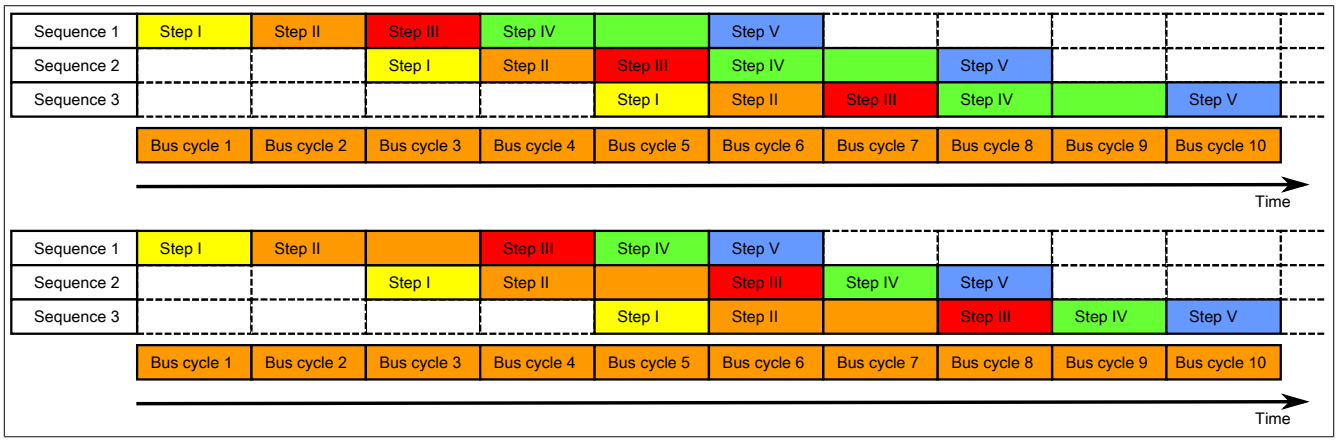


Figure 274: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

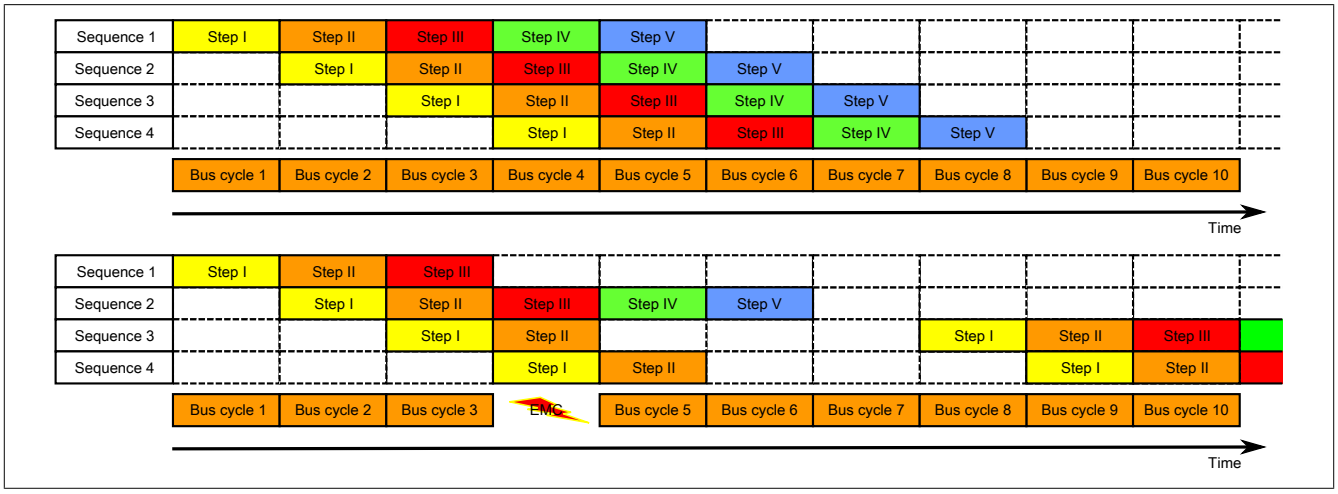


Figure 275: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.16.7.11.10 EnDat with FlatStream

EnDat is a synchronous interface capable of half-duplex communication. Various features have been included to ensure that signals are transmitted without errors.

- An automatically generated checksum is sent together with a signal and evaluated by the recipient.
- The command which the encoder is responding to is repeated at the start of a response.

In Flatstream mode, the module acts as a bridge between the CPU and the EnDat slave. EnDat-specific algorithms were implemented to monitor timeouts and handle checksums. During normal operation, the user does not have access to these details.

More detailed information can be found in the documentation "Technical Information - EnDat 2.2" and the encoder's manufacturer data.

4.16.7.11.10.1 Overview of conventional EnDat commands for the Flatstream mode

Command byte [hex]	Command	EnDat 2.2 only
0x00	Reset	
0x01	Acknowledge error	
0x04	Read parameter	
0x05	Write parameter	
0x06	Read parameter from memory block	•
0x07	Write parameter to memory block	•
0x08	Read word 1 from additional information	•
0x09	Read word 2 from additional information	•
0x0A	Read word 3 from additional information	•
0x0B	Read word 4 from additional information	•

4.16.7.11.10.2 Reset (0x00)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x00	Command (Reset)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x00	Repetition (safety)
Master		

4.16.7.11.10.3 Acknowledge error (0x01)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x01	Command (Acknowledge error)
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x01	Repetition (safety)
Master		

4.16.7.11.10.4 Read parameter (0x04)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x04	Command (read parameter)
2	MRS code	Memory area to read
3	Parameter no.	
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x04	Repetition (safety)
2	MRS code	
3	Parameter no.	
4	Value_L	Value read
5	Value_H	
Master		

4.16.7.11.10.5 Write parameter (0x05)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x05	Command (write parameter)
2	MRS code	Memory area to write to
3	Parameter no.	
4	Value_L	Value to be written
5	Value_H	
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x05	Repetition (safety)
2	MRS code	
3	Parameter no.	
Master		

4.16.7.11.10.6 Read parameter from memory block (0x06)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x06	Command (read parameter from memory block)
2	MRS code	Memory area to read
3	Block no.	
4	Parameter no.	
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x06	Repetition (safety)
2	MRS code	
3	Block no.	
4	Parameter no.	
5	Value_L	Value read
6	Value_H	
Master		

4.16.7.11.10.7 Write parameter in memory block (0x07)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x07	Command (write parameter in memory block)
2	MRS code	Memory area to write to
3	Block no.	
4	Parameter no.	
5	Value_L	Value to be written
6	Value_H	
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x07	Repetition (safety)
2	MRS code	
3	Block no.	
4	Parameter no.	
Master		

4.16.7.11.10.8 Read word 1 from additional information (0x08)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x08	Command (read word 1 from additional information)
2	MRS code	Memory area to read
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x08	Repetition (safety)
2	MRS code	
3	Value_L	Word 1 from additional information
4	Value_H	
Master		

4.16.7.11.10.9 Read word 2 from additional information (0x09)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x09	Command (read word 2 from additional information)
2	MRS code	Memory area to read
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x09	Repetition (safety)
2	MRS code	
3	Value_L	Read word 1 from additional information (overhead)
4	Value_H	
5	Value_L	Word 2 from additional information
6	Value_H	
Master		

4.16.7.11.10.10 Read word 3 from additional information (0x0A)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x0A	Command (read word 3 from additional information)
2	MRS code	Memory area to read
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x0A	Repetition (safety)
2	MRS code	
3	Value_L	Read word 1 from additional information (overhead)
4	Value_H	
5	Value_L	Read word 2 from additional information (overhead)
6	Value_H	
7	Value_L	Word 3 from additional information
8	Value_H	
Master		

4.16.7.11.10.11 Read word 4 from additional information (0x0B)

Master command

Protocol bytes		Information
No.	Name	
Master		
1	0x0B	Command (read word 4 from additional information)
2	MRS code	Memory area to read
Slave		

Slave response

Protocol bytes		Information
No.	Name	
Slave		
1	0x0B	Repetition (safety)
2	MRS code	
3	Value_L	Read word 1 from additional information (overhead)
4	Value_H	
5	Value_L	Read word 2 from additional information (overhead)
6	Value_H	
7	Value_L	Read word 3 from additional information (overhead)
8	Value_H	
9	Value_L	Word 4 from additional information
10	Value_H	
Master		

4.16.7.11.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
100 µs

4.16.7.11.12 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.16.8 X20DS4389

4.16.8.1 General information

This module is a digital signal processor module that is used for detecting and evaluating input edges and for creating edges.

High-speed input edges such as registration marks are acquired and given a precise input stamp independently of the X2X Link cycle time of the system. In the other direction, the module sets outputs at precisely defined times. This is done with a resolution of up to 125 ns.

In oversampling mode, the module acquires very short input patters whose low or high phases are shorter than the X2X Link cycle time. Similarly, output patterns (e.g. drum sequencers) can also be output with extremely short high/low times. Oversampling can take place with a scan rate of up to 25 µs.

If necessary, up to 4 events per edge detection unit are stored in a buffer (history elements).

Other functions include pulse duration measuring and differential time measuring.

- 4 digital input channels
- 4 digital channels, configurable as inputs or outputs
- 4 edge detection units with timestamp function (each can be used to measure pulse duration or differential time, 4 history elements per unit)
- 4x precise edge generation down to the µs (up to four edges per unit in each case)
- 4x oversampling (input and output signal)
- 24 VDC and GND for sensor/actuator supply

4.16.8.2 Order data

Model number	Short description	Figure
	Digital signal processing and preparation	
X20DS4389	X20 digital signal module, 4 digital inputs, 24 VDC, 4 digital outputs, 24 VDC, 0.1 A, oversampling I/O functions, time-triggered I/O functions, NetTime module	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 377: X20DS4389 - Order data

4.16.8.3 Technical data

Product ID	X20DS4389
Short description	
I/O module	4 digital input channels, 4 digital channels configurable as inputs or outputs, 4 edge detection units with timestamp function (each can be used to measure pulse duration or differential time, 4 history elements per unit), 4x edge generation with µs precision (up to 4 edges per unit), 4x oversampling (input and output signal)
General information	
B&R ID code	0xA93B
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using the status LED and software (output error status)
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Type of signal lines	Shielded cables must be used for all signal lines
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	4 + 4, configurable as inputs or outputs using software
Nominal voltage	24 VDC
Input voltage	24 VDC (-15% / +20%)
Input current at 24 VDC	Approx. 1.3 mA
Input circuit	Sink
Additional functions	4 edge detection units with timestamp function, 4x input oversampling
Input resistance	18.4 kΩ
Input frequency	40 kHz
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Digital outputs	
Design	Push / Pull / Push-Pull
Quantity	Up to 4, configurable as inputs or outputs using software
Nominal voltage	24 VDC
Switching voltage	24 VDC (-15% / +20%)
Nominal output current	0.1 A
Total nominal current	0.4 A
Output circuit	Sink and/or source
Output protection	Thermal cutoff if overcurrent or short circuit occurs, integrated protection for switching inductances
Diagnostic status	Output monitoring
Leakage current when switched off	Max. 25 µA
$R_{DS(on)}$	150 mΩ
Residual voltage	<0.9 V at 0.1 A rated current
Peak short circuit current	<10 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<2 µs
1 -> 0	<2 µs
Switching frequency	
Resistive load	Max. 24 kHz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Switching voltage + 0.6 VDC
Isolation voltage between channel and bus	500 V_{eff}
Additional functions	4x edge generation with µs precision, 4x output oversampling
Edge detection units	
Quantity	4
Operating mode	4 pulse duration measurements, relative or absolute times of input edges in µs resolution, 4 history elements per unit
Counter size	16/32-bit
Input frequency (max.)	40 kHz
Resolution	125 ns timestamp function

Table 378: X20DS4389 - Technical data

Product ID	X20DS4389
Signal form	Square wave pulse
Sensor supply	Module-internal, max. 600 mA
Edge generation units	
Quantity	4
Edge generation	
Absolute	Absolute to NetTime
Relative	Relative to other edges
Offset at relative edge generation	
Range of values	16 or 32 bit value
Resolution	1 µs
Actuator supply	Module-internal, max. 600 mA
Oversampling	
Quantity	4
Sample time	25 to 255 µs
Data volume	Up to 64-bit per X2X Link cycle in input and output direction
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 378: X20DS4389 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.16.8.4 LED status indicators

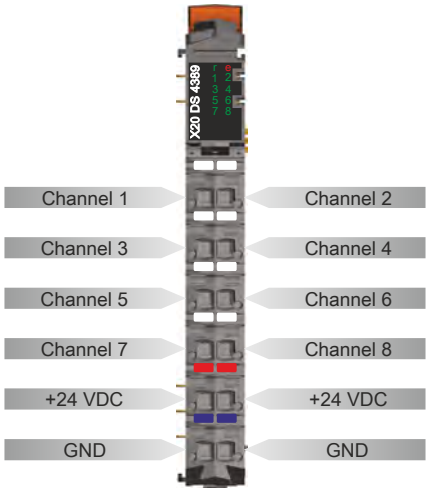
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	One of the following errors occurred: • Oversample output control error • Oversample output copy error • Edge detect poll cycle violation • Error on edge generator unit 1 - 4
	1 - 8	Green		Status of the corresponding digital signal

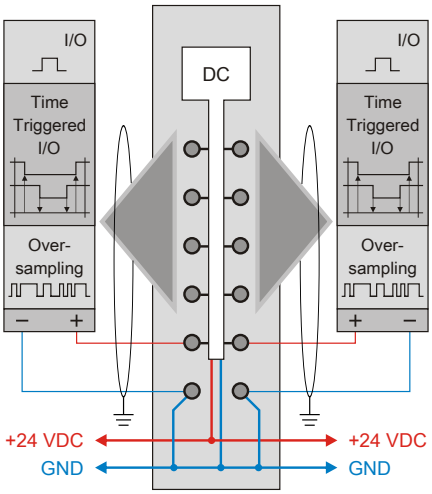
1) Depending on the configuration, a firmware update can take up to several minutes.

4.16.8.5 Pinout

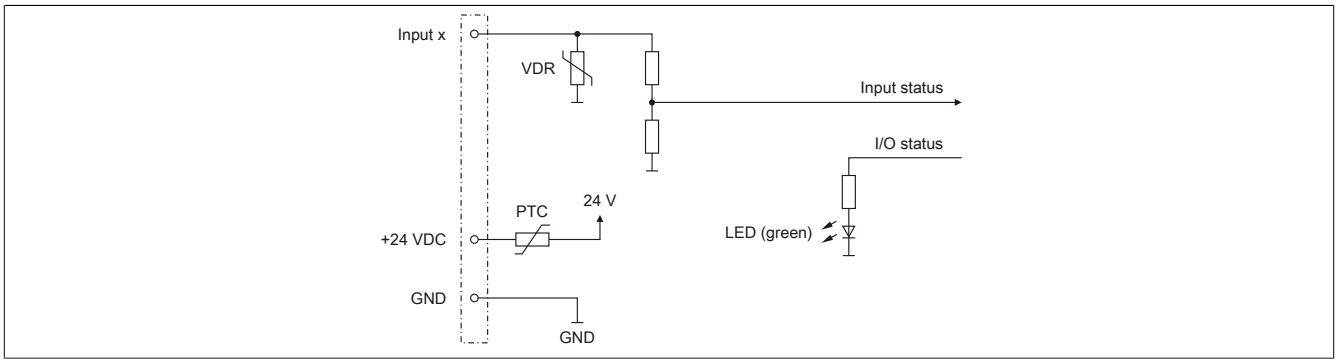
Shielded cables must be used for all signal lines.



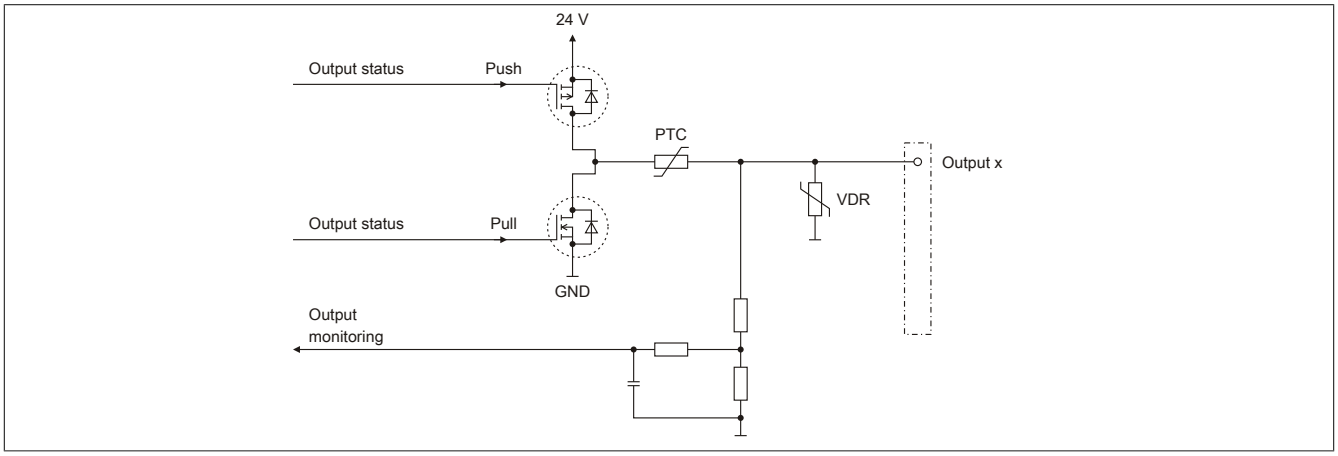
4.16.8.6 Connection example



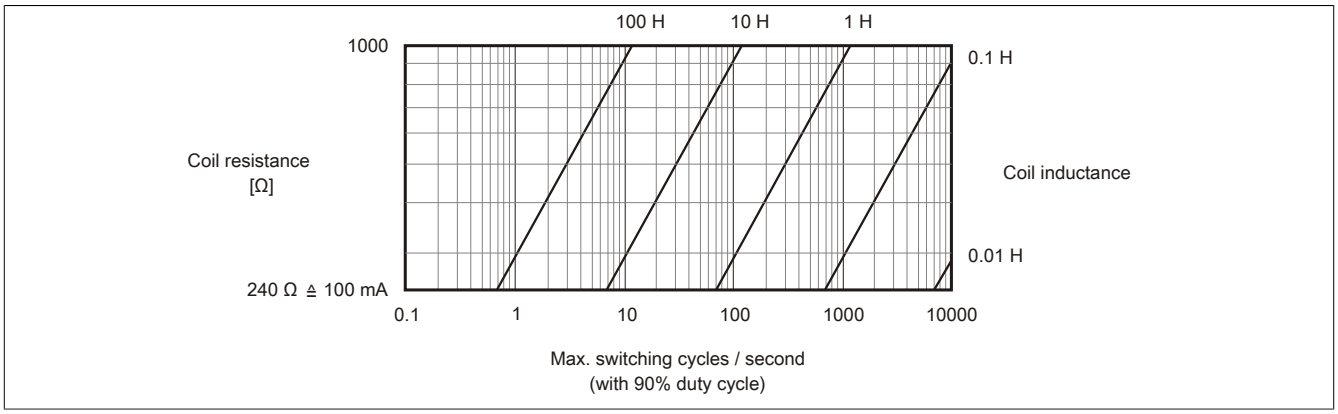
4.16.8.7 Input circuit diagram



4.16.8.8 Output circuit diagram



4.16.8.9 Switching inductive loads



4.16.8.10 Register description

4.16.8.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.16.8.10.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - General						
513	CfO_SIframeGenID	USINT				•
Configuration - System timer						
642	CfO_SystemCycleTime	UINT				•
646	CfO_SystemCycleOffset	INT				•
650	CfO_SystemCyclePrescaler	UINT				•
Configuration - Physical I/O						
769 + (N-1) * 2	CfO_PhyIOConfigCh0N (Index N = 1 to 8)	USINT				•
Configuration - Direct I/O						
899	CfO_DirectIOClearMask0_7	USINT				•
903	CfO_DirectIOSetMask0_7	USINT				•
905	CfO_OutputUpdateCycle	USINT				•
Configuration - Oversampled I/O						
1025	CfO_OversampleMode	USINT				•
1027	CfO_OversampleSampleCycleID	USINT				•
1029	CfO_OversampleRelativeCycleID	USINT				•
1031	CfO_OversampleConsumeCycleID	USINT				•
1033	CfO_OversampleOutputBits	USINT				•
1035	CfO_OversampleInputBits	USINT				•
1037	CfO_OversampleOutputWindow	USINT				•
1039	CfO_OversampleInputWindow	USINT				•
1041 + (N*2)	CfO_OversampleConfigInputN (Index N = 0 to 3)	USINT				•
1049 + (N*2)	CfO_OversampleConfigOutputN (Index N = 0 to 3)	USINT				•
Configuration - Edge detection						
2817	CfO_EdgeDetectPollCycleID	USINT				•
2828	CfO_EdgeDetectEventEnable	UDINT				•
3073 + (N-1) * 16	CfO_EdgeDetectUnit0NMode (Index N = 1 to 4)	USINT				•
3075 + (N-1) * 16	CfO_EdgeDetectUnit0NLeading (Index N = 1 to 4)	USINT				•
3077 + (N-1) * 16	CfO_EdgeDetectUnit0NMaster (Index N = 1 to 4)	USINT				•
3079 + (N-1) * 16	CfO_EdgeDetectUnit0NSlave (Index N = 1 to 4)	USINT				•
Configuration - Edge generator						
2945	CfO_EdgeGenPollCycleEventID	USINT				•
2947	CfO_EdgeGenConsumeCycleEventID	USINT				•
3585 + (N-1) * 64	CfO_EdgeGenUnit0NMode (Index N = 1 to 4)	USINT				•
3589 + (N-1) * 64	CfO_EdgeGenUnit0NTimestampFifoLim (Index N = 1 to 4)	USINT				•
3591 + (N-1) * 64	CfO_EdgeGenUnit0NTimestampRegCount (Index N = 1 to 4)	USINT				•
3596 + (N-1) * 64	CfO_EdgeGenUnit0NPickupDiff	UDINT				•
3602 + (N-1) * 64	CfO_EdgeGenUnit0NConfigEdge0 (Index N = 1 to 4)	UINT				•
3606 + (N-1) * 64	CfO_EdgeGenUnit0NConfigEdge1 (Index N = 1 to 4)	UINT				•
3610 + (N-1) * 64	CfO_EdgeGenUnit0NConfigEdge2 (Index N = 1 to 4)	UINT				•
3614 + (N-1) * 64	CfO_EdgeGenUnit0NConfigEdge3 (Index N = 1 to 4)	UINT				•
Communication - General						
546	ProtocolError (16-bit)	USINT	•			
547	ProtocolError (8-bit)	UINT	•			
550	ProtocolSequenceViolation (16-bit)	UINT	•			
551	ProtocolSequenceViolation (8-bit)	USINT	•			
Communication - Error register						
257	Error state - Output data and edge detection	USINT	•			
	OutputControlError	Bit 4				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
	OutputCopyError	Bit 5				
	EdgeDetectError	Bit 6				
259	Error messages register - Edge generator	USINT	•			
	EdgeGen01Error	Bit 0				
	EdgeGen01Warning	Bit 1				
	EdgeGen02Error	Bit 2				
	EdgeGen02Warning	Bit 3				
	EdgeGen03Error	Bit 4				
	EdgeGen03Warning	Bit 5				
	EdgeGen04Error	Bit 6				
	EdgeGen04Warning	Bit 7				
321	Acknowledge error messages - Output data and edge detection	USINT			•	
	QuitOutputControlError	Bit 4				
	QuitOutputCopyError	Bit 5				
	QuitEdgeDetectError	Bit 6				
323	Acknowledge error message register - Edge generator	USINT			•	
	QuitEdgeGen01Error	Bit 0				
	QuitEdgeGen01Warning	Bit 1				
	QuitEdgeGen02Error	Bit 2				
	QuitEdgeGen02Warning	Bit 3				
	QuitEdgeGen03Error	Bit 4				
	QuitEdgeGen03Warning	Bit 5				
	QuitEdgeGen04Error	Bit 6				
	QuitEdgeGen04Warning	Bit 7				
Communication - System timer						
683	SDCLifeCount	SINT	•			
Communication - Direct I/O						
915	"DigitalOutput" register	USINT			•	
	DigitalOutput03	Bit 2				
	DigitalOutput04	Bit 3				
	DigitalOutput07	Bit 6				
	DigitalOutput08	Bit 7				
927	"DigitalInput" register	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
Communication - Oversampled I/O (output)						
1059	Oversample register - Configuration	USINT			•	
	OversampleEnable	Bit 0				
	OversampleOutputValidate	Bit 1				
1063	OversampleOutputCycle	USINT			•	
	OversampleSampleOffset	USINT			•	
1088 + N	OversampleOutput0NSample1_8 (Index N = 1 to 4)	USINT			•	
1092 + N	OversampleOutput0NSample9_16 (Index N = 1 to 4)	USINT			•	
1096 + N	OversampleOutput0NSample17_24 (Index N = 1 to 4)	USINT			•	
1100 + N	OversampleOutput0NSample25_32 (Index N = 1 to 4)	USINT			•	
1104 + N	OversampleOutput0NSample33_40 (Index N = 1 to 4)	USINT			•	
1108 + N	OversampleOutput0NSample41_48 (Index N = 1 to 4)	USINT			•	
1112 + N	OversampleOutput0NSample49_56 (Index N = 1 to 4)	USINT			•	
1116 + N	OversampleOutput0NSample57_64 (Index N = 1 to 4)	USINT			•	
Communication - Oversampled I/O (input)						
1074	OversampleInputTime	INT	•			
1079	OversampleInputCycle	USINT	•			
1120 + N	OversampleInput0NSample64_57 (Index N = 1 to 4)	USINT	•			
1124 + N	OversampleInput0NSample56_49 (Index N = 1 to 4)	USINT	•			
1128 + N	OversampleInput0NSample48_41 (Index N = 1 to 4)	USINT	•			
1132 + N	OversampleInput0NSample40_33 (Index N = 1 to 4)	USINT	•			
1136 + N	OversampleInput0NSample32_25 (Index N = 1 to 4)	USINT	•			
1140 + N	OversampleInput0NSample24_17 (Index N = 1 to 4)	USINT	•			
1144 + N	OversampleInput0NSample16_9 (Index N = 1 to 4)	USINT	•			
1148 + N	OversampleInput0NSample8_1 (Index N = 1 to 4)	USINT	•			
Communication - Edge detection						
4098 + (N-1) * 32	EdgeDetect0NMastercount (16-bit) (Index N = 1 to 4)	INT	•			
4099 + (N-1) * 32	EdgeDetect0NMastercount (8-bit) (Index N = 1 to 4)	SINT	•			
4102 + (N-1) * 32	EdgeDetect0NSlavecount (16-bit) (Index N = 1 to 4)	INT	•			
4103 + (N-1) * 32	EdgeDetect0NSlavecount (8-bit) (Index N = 1 to 4)	SINT	•			
4108 + (N-1) * 32	EdgeDetect0NDifference (32-bit) (Index N = 1 to 4)	DINT	•			
4110 + (N-1) * 32	EdgeDetect0NDifference (16-bit) (Index N = 1 to 4)	INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
4116 + (N-1) * 32	EdgeDetect0NMastertime (32-bit) (Index N = 1 to 4)	DINT	●			
4118 + (N-1) * 32	EdgeDetect0NMastertime (16-bit) (Index N = 1 to 4)	INT	●			
4124 + (N-1) * 32	EdgeDetect0NSlavetime (32-bit) (Index N = 1 to 4)	DINT	●			
4126 + (N-1) * 32	EdgeDetect0NSlavetime (16-bit) (Index N = 1 to 4)	INT	●			
Communication - Edge generator						
6145 + (N-1) * 256	"EdgeGenEnable" register	USINT			●	
	EdgeGen0NEnable EdgeGen0NEnableReadback (Index N = 1 to 4)	Bit 0				
6147 + (N-1) * 256	EdgeGenSequence	USINT			●	
	EdgeGenSequenceReadback	USINT	●			
6180 + (N-1) * 256	EdgeGen0NOffset1 (Index N = 1 to 4) (32-bit) CfO_EdgeGen0NOffset_32bit1 (Index N = 1 to 4)	UDINT			●	●
6182 + (N-1) * 256	EdgeGen0NOffset1 (Index N = 1 to 4) (16-bit)	UINT			●	
6188 + (N-1) * 256	EdgeGen0NOffset2 (Index N = 1 to 4) (32-bit) CfO_EdgeGen0NOffset_32bit2 (Index N = 1 to 4)	UDINT			●	●
6190 + (N-1) * 256	EdgeGen0NOffset2 (Index N = 1 to 4) (16-bit)	UINT			●	
6196 + (N-1) * 256	EdgeGen0NOffset3 (Index N = 1 to 4) (32-bit) CfO_EdgeGen0NOffset_32bit3 (Index N = 1 to 4)	UDINT			●	●
6198 + (N-1) * 256	EdgeGen0NOffset3 (Index N = 1 to 4) (16-bit)	UINT			●	
6204 + (N-1) * 256	EdgeGen0NOffset4 (Index N = 1 to 4) (32-bit) CfO_EdgeGen0NOffset_32bit4 (Index N = 1 to 4)	UDINT			●	●
6206 + (N-1) * 256	EdgeGen0NOffset4 (Index N = 1 to 4) (16-bit)	UINT			●	
6212 + (N-1) * 256	EdgeGen0NTimestamp1 (Index N = 1 to 4) (32-bit)	UDINT			●	
6214 + (N-1) * 256	EdgeGen0NTimestamp1 (Index N = 1 to 4) (16-bit)	UINT			●	
6220 + (N-1) * 256	EdgeGen0NTimestamp2 (Index N = 1 to 4) (32-bit)	UDINT			●	
6222 + (N-1) * 256	EdgeGen0NTimestamp2 (Index N = 1 to 4) (16-bit)	UINT			●	
6228 + (N-1) * 256	EdgeGen0NTimestamp3 (Index N = 1 to 4) (32-bit)	UDINT			●	
6230 + (N-1) * 256	EdgeGen0NTimestamp3 (Index N = 1 to 4) (16-bit)	UINT			●	
6236 + (N-1) * 256	EdgeGen0NTimestamp4 (Index N = 1 to 4) (32-bit)	UDINT			●	
6238 + (N-1) * 256	EdgeGen0NTimestamp4 (Index N = 1 to 4) (16-bit)	UINT			●	

4.16.8.10.3 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.16.8.10.4 General

4.16.8.10.4.1 Use with Automation Studio

The module is only supported SG4 target systems via X2X and POWERLINK!

X2X Link supports a up to 28 bytes of synchronous data per module. To optimize use and to prevent needless data transfer, the data points can be adjusted as needed in Automation Studio. Data points that are not needed can be disabled, and the bit width of the data points can be defined.

4.16.8.10.4.2 Timestamp function

The timestamp function is based on synchronized timers. When a timestamp event occurs, the module immediately saves the current net time. After the respective data is transmitted to the CPU, including this precise time, the CPU can then evaluate the data using its own net time (or system time).

Conversely, the CPU can predefine output events, apply a timestamp and transfer them to the module. The module then executes the predefined action at the precise time defined by the CPU.

The resolution of the timestamp is up to 1/8 µs in both directions.

4.16.8.10.4.3 Synchronization jitter

Because the CPU – which determines the X2X net time – and the module have different clocks, the module's internal X2X net time must be synchronized with the CPU's net time. Due to this synchronization, the module's internal X2X net time is corrected by a maximum of 1/8 µs per system cycle if necessary. This synchronization jitter becomes noticeable when using the net time with 1/8 µs resolution (max. ±1/8 µs).

If a 100% exact 1/8 µs resolution without jitter is required, then the "localtime 1/8 µs" must be used (see the 4.16.4.11.11.3 "CfO_EdgeDetectUnitMode" register).

4.16.8.10.5 General registers

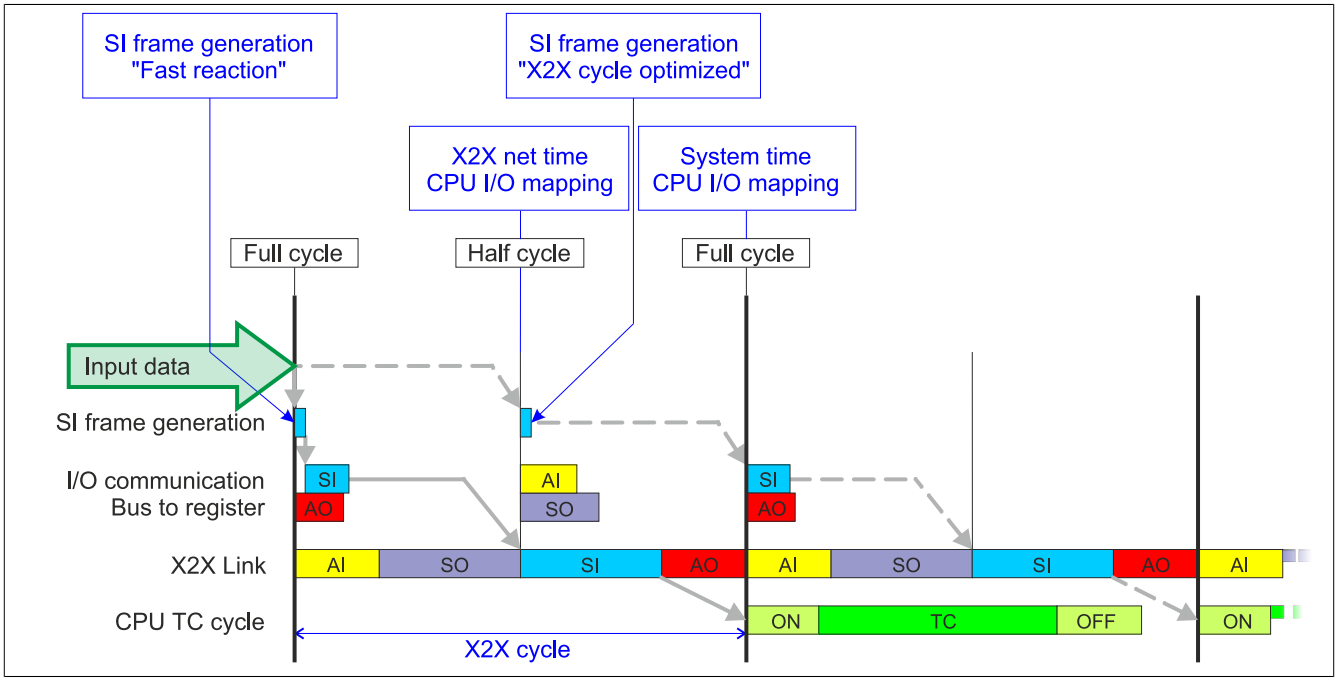
4.16.8.10.5.1 "CfO_SIframeGenID" register

Name:
CfO_SIframeGenID
"SI-frame generation" in the AS I/O configuration.

This register determines when the synchronous input data is generated for transfer. This has a decisive effect on the timing of the input data.

The setting "Fast reaction" causes the input data to be available one X2X cycle sooner in the CPU. However, this setting also has a negative effect on the minimum X2X cycle time.

Data type	Value	Information
USINT	9	X2X cycle optimized
	14	Fast reaction



4.16.8.10.5.2 "ProtocolError" register

Name:
ProtocolError

This register contains an error counter that specifies the number of X2X protocol errors. In the I/O configuration, the "Network information" parameter can be used to help configure a data point for this register with a bit width of 8 or 16 bits in the I/O mapping.

Data type	Value	Information
USINT	0 to 255	Error counter (8-bit)
UINT	0 to 65,535	Error counter (16-bit)

4.16.8.10.5.3 "ProtocolSequenceViolation" register

Name:
ProtocolSequenceViolation

This register contains an error counter that specifies the number of X2X sequence violations. In the I/O configuration, the "Network information" parameter can be used to help configure a data point with a bit width of 8 or 16 bits in the I/O mapping.

Data type	Value	Information
USINT	0 to 255	Error counter (8-bit)
UINT	0 to 65,535	Error counter (16-bit)

4.16.8.10.5.4 "SDCLifeCount" register

Name:
SDCLifeCount

Counter that is incremented with each system timer cycle. The "SDC information" setting in the AS I/O configuration can be used to activate this register in the I/O mapping as the data point, "SDCLifeCount".

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Value
SINT	-128 to 127

4.16.8.10.6 Error handling

If one of the functions detects an error, then an error bit is set in one of the error state registers. The application is now able to react accordingly and acknowledge the errors by setting a respective bit in the "Acknowledge error message" registers. This causes the bit to be reset in the error state register. If the source of the error persists, then the error bit is set again as soon as the error is detected again (i.e. cannot be reset).

Acknowledging the error does not affect the module's functionality. If possible, the module automatically resumes processing as soon as the source of the error has been corrected.

If an error occurs (not a warning), this is indicated by the red "e" LED on the module (double flash). This signal is automatically acknowledged as soon as the source of the error has been corrected.

4.16.8.10.6.1 Error state register - Output data and edge detection

Name:
OutputControlError
OutputCopyError
EdgeDetectError

Errors in the output data and cycle time settings are indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	OutputControlError	0	No error
		1	The module did not receive new data in time while in the mode "Output control mode = single", meaning that a bit that has already been output would have been output again by the output control buffer.
5	OutputCopyError	0	No error
		1	Oversampling output data could not be copied to the output control buffer. (e.g. an attempt was made to write oversampling output data to an address outside of the OversampleOutputWindow).
6	EdgeDetectError	0	No error
		1	Cycle time violation edge detection: The "EdgeDetectPollCycle" must be smaller than or equal to 255 µs. This error is caused if the cycle defined in the 4.16.4.11.11.1 "CfO_EdgeDetectPollCycleID" register is > 255 µs.
7	Reserved	-	

4.16.8.10.6.2 Error messages register - Edge generator

Name:
EdgeGen01Error to EdgeGen04Error
EdgeGen01Warning to EdgeGen04Warning

This register indicates edge detection errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	EdgeGen01Error	0	No error
		1	Unit 1 error[1)]
1	EdgeGen01Warning	0	No error
		1	Unit 1 warning[2)]
2	EdgeGen02Error	0	No error
		1	Unit 2 error[1)]
3	EdgeGen02Warning	0	No error
		1	Unit 2 warning[2)]
4	EdgeGen03Error	0	No error
		1	Unit 3 error[1)]
5	EdgeGen03Warning	0	No error
		1	Unit 3 warning[2)]
6	EdgeGen04Error	0	No error
		1	Unit 4 error[1)]
7	EdgeGen04Warning	0	No error
		1	Unit 4 warning[2)]

1) **Possible error:**

- Due to "EdgeGenPollCycle", one or more timestamps from the edge generator of a unit were not able to be processed in time, and it was not possible to make up for the difference (see: 4.16.8.10.12.7 "CfO_EdgeGenUnitPickupDiff")
- A branched ring-shaped chain of edges in a unit is attempting to set the timestamp for an edge, even though the FIFO of the configured physical channel is already full. (see: 4.16.8.10.12.8 "CfO_EdgeGenUnitConfigEdge"→Ring-shaped chain of edges)

2) Due to "EdgeGenPollCycle", one or more timestamps from the edge generator of a unit were not able to be processed in time, and it was possible to make up for the difference (see: (see: 4.16.8.10.12.7 "CfO_EdgeGenUnitPickupDiff" register)

4.16.8.10.6.3 Acknowledge error message register - Output data and edge detection

Name:
QuitOutputControlError
QuitOutputCopyError
QuitEdgeDetectError

Error messages from the 4.16.4.11.6.1 "Error state - Output data and edge detection" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	QuitOutputControlError	0	No change
		1	Acknowledge error
5	QuitOutputCopyError	0	No change
		1	Acknowledge error
6	QuitEdgeDetectError	0	No change
		1	Acknowledge error
7	Reserved	-	

4.16.8.10.6.4 Acknowledge error message register - Edge generator

Name:
QuitEdgeGen01Error to QuitEdgeGen04Error
QuitEdgeGen01Warning to QuitEdgeGen04Warning

Error messages from the 4.16.8.10.6.2 "Error messages - Edge generator" register can be acknowledged by setting the corresponding bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	QuitEdgeGen01Error	0	No change
		1	Acknowledge error
1	QuitEdgeGen01Warning	0	No change
		1	Acknowledge warning
2	QuitEdgeGen02Error	0	No change
		1	Acknowledge error
3	QuitEdgeGen02Warning	0	No change
		1	Acknowledge warning
4	QuitEdgeGen03Error	0	No change
		1	Acknowledge error
5	QuitEdgeGen03Warning	0	No change
		1	Acknowledge warning
6	QuitEdgeGen04Error	0	No change
		1	Acknowledge error
7	QuitEdgeGen04Warning	0	No change
		1	Acknowledge warning

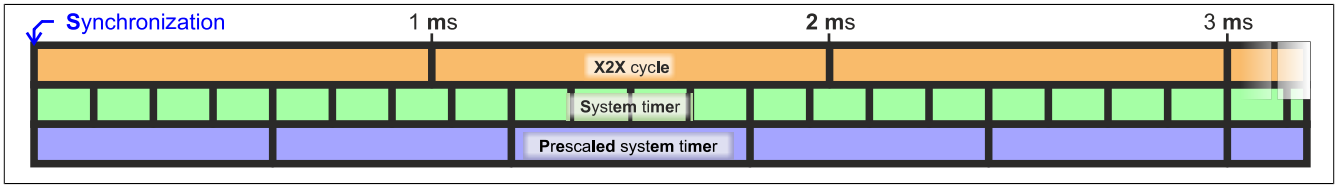
4.16.8.10.7 System timer

The module's individual functions all depend on a system timer. This internal "system cycle time" can be defined from 25 to 255 µs. The functions can also be run with the help of a configurable "prescaled system timer" to minimize the load on the module, thereby making it possible to use the shortest possible X2X cycle time.

The cycle of the "prescaled system timer" (and system timer) is referenced with the X2X Link as soon as the module has been started up and the X2X Link has been initialized. Since the system timer and the module's internal X2X net time use the same clock, the two run synchronously from that point on. An X2X cycle time that is not a multiple of the system cycle time results in an offset, which can be calculated.

The following values apply to the following example:

X2X cycle	1 ms
System timer	150 µs
Prescaled system timer	4



4.16.8.10.7.1 "CfO_SystemCycleTime" register

Name:
CfO_SystemCycleTime
"Cycle time" in the AS I/O configuration.

The cycle time of the system timer can be set in this register in steps of 1/8 µs. The value entered in the AS I/O configuration is automatically multiplied by 8.

Information:

A setting < 50 µs has a negative effect on the minimum X2X cycle time!

Data type	Value	Information
UINT	200 to 2047	System timer cycle time in steps of 1/8 µs (25 to 255,875 µs)

4.16.8.10.7.2 "CfO_SystemCycleOffset" register

Name:
CfO_SystemCycleOffset
"Cycle offset" in the AS I/O configuration.

The synchronization time for the system cycle can be offset in this register in steps of 1/8 µs. The value entered in the AS I/O configuration is automatically multiplied by 8.

Data type	Value	Information
INT	-32,768 to 32,767	Cycle offset in steps of 1/8 µs (-4096 to 4095.875 µs)

4.16.8.10.7.3 "CfO_SystemCyclePrescaler" register

Name:
CfO_SystemCyclePrescaler
"Cycle prescaler" in the AS I/O configuration.

The prescaler for setting the "Prescaled system timer" can be configured in this register. The cycle time of the specified system timer is a product of the system timer multiple set in this register.

The "prescaled system timer" can be used as alternative time source for the individual functions. This is useful if a function requires a very short system cycle. To reduce the load on the module in such a situation, other functions can be processed in a slow cycle.

Data type	Value	Information
UINT	2 to 128	Multiple of the system timer

4.16.8.10.8 Physical I/O configuration

4.16.8.10.8.1 "CfO_PhyIOConfigCh" registers

Name:
CfO_PhyIOConfigCh01 to CfO_PhyIOConfigCh08

The physical I/O channels can each be configured individually in these registers.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Push driver[1)]	0	Disabled
		1	Enabled
1	Pull driver[1)]	0	Disabled
		1	Enabled
2	Input inverted	0	Not inverted
		1	Inverse
3	Output inverted[1)]	0	Not inverted
		1	Inverse
4 - 7	Output function[1)]	0	Direct I/O
		1 to 15	Reserved

1) Only available for the I/O channels 3, 4, 7 and 8.

4.16.8.10.9 Direct I/O

Direct I/O makes it possible to use the physical I/Os like normal I/Os. Additionally, the application can only set or reset I/Os (e.g. an output channel is set by the edge generator and manually reset by the application).

4.16.8.10.9.1 "EdgeGenTimestamp" register

Name:
CfO_DirectIOClearMask0_7
"Direct control of output channel 03" to "Direct control of output channel 08" in the AS I/O configuration.

If the bit for the respective channel is set in this register, then the output is reset as soon as its direct I/O output channel is reset (4.16.5.11.9.3 "output control channel 7_0" or "DigitalOutput0x" register in the AS I/O mapping).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	-	
2	Output channel 3	0	No change
		1	Reset channel
3	Output channel 4	0	No change
		1	Reset channel
4 - 5	Reserved	-	
6	Output channel 7	0	No change
		1	Reset channel
7	Output channel 8	0	No change
		1	Reset channel

4.16.8.10.9.2 "CfO_DirectIOSetMask0_7" register

Name:
CfO_DirectIOSetMask0_7
"Direct control of output channel 03" to "Direct control of output channel 08" in the AS I/O configuration.

If the bit for the respective channel is set in this register, then the output is set as soon as its direct I/O output channel is set (4.16.5.11.9.3 "output control channel 7_0" or "DigitalOutput0x" register in the AS I/O mapping).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	-	
2	Output channel 3	0	No change
		1	Set channel
3	Output channel 4	0	No change
		1	Set channel
4 - 5	Reserved	-	
6	Output channel 7	0	No change
		1	Set channel
7	Output channel 8	0	No change
		1	Set channel

4.16.8.10.9.3 "CfO_OutputUpdateCycle" register

Name:
CfO_OutputUpdateCycle

This register sets the time of data output.

Data type	Value	Information
USINT	10	X2X cycle optimized (jitter-free)
	15	Fast reaction (with jitter)

4.16.8.10.9.4 "DigitalOutput" register

Name:
DigitalOutput03 and DigitalOutput04, DigitalOutput07 and DigitalOutput08

This register contains the bits for controlling the direct I/O output channels. Depending on how the 4.16.5.11.9.1 "CfO_DirectIOClearMask0_7" and 4.16.5.11.9.2 "CfO_DirectIOSetMask0_7" registers are configured, the digital outputs are set to the status of the respective bits in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	-	
2	DigitalOutput03	0 or 1	Output status of channel 3
3	DigitalOutput04	0 or 1	Output status of channel 4
4 - 5	Reserved	-	
6	DigitalOutput07	0 or 1	Output status of channel 7
7	DigitalOutput08	0 or 1	Output status of channel 8

4.16.8.10.9.5 "DigitalInput" register

Name:
DigitalInput01 to DigitalInput08

This register displays the status of the digital input channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalInput01	0 or 1	Input status of channel 1
...	...	...	
7	DigitalInput08	0 or 1	Input status of channel 8

4.16.8.10.10 Oversampled I/O

"Oversampled I/O" is based on input status buffers and output control buffers. Input data acquisition and output control occur in one sample cycle (one sample cycle equals one bit in the buffer). The precise time of an input buffer entry is indicated by its position in the buffer and the net time assigned to the buffer.

In "Output control mode = single" every output buffer entry is marked as invalid once it has been executed. This ensures that the outputs are not supplied with invalid data. In this mode, the application needs to ensure that the module is always supplied with valid data.

When using "Output control mode = continuous" the contents of the buffer are output again if the module is not supplied with new oversample output data.

4.16.8.10.10.1 Addressing the output control buffer

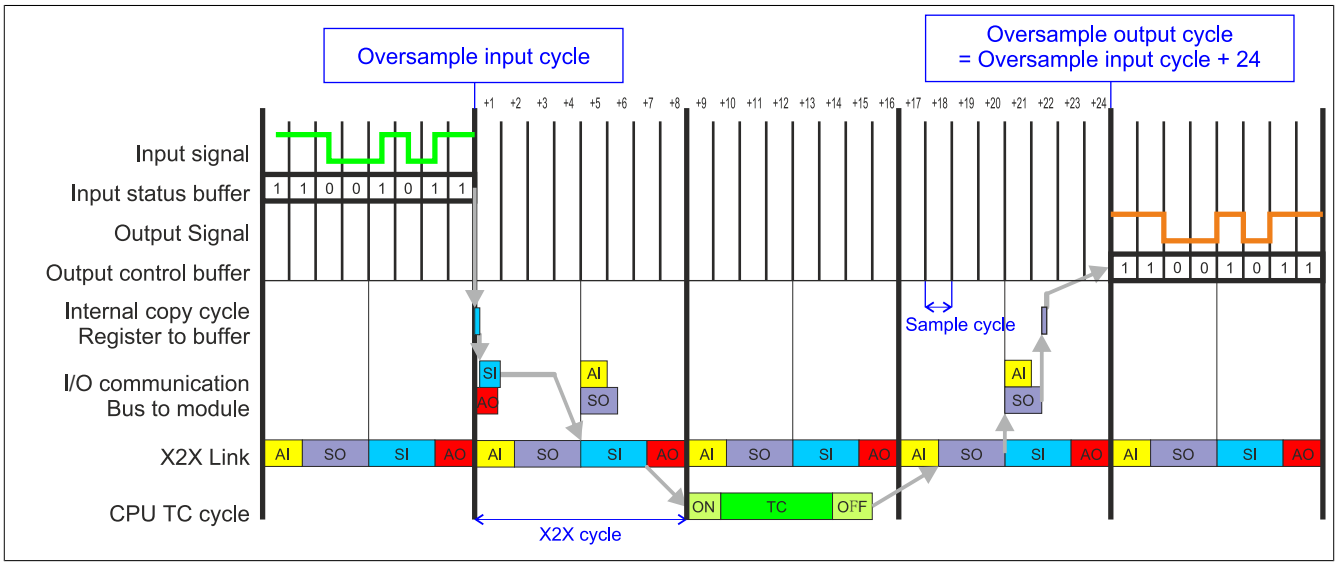
The module has one cyclic 256-bit output control buffer for each oversample channel. One bit is output from these buffers to the configured physical output channels in each "sample cycle". When new data is transferred to one of these buffers, the application must define where in the respective buffer the data should be written to. There are 2 possibilities (absolute or relative "Output mode" in the AS I/O configuration).

4.16.8.10.10.2 Absolute addressing of the output control buffer

With absolute addressing, in each cycle where "OversampleOutputValidate = True", in addition to the oversample output sample data (in the 4.16.4.11.10.15 "OversampleOutput0NSample" registers) an address must also be transferred in the 4.16.4.11.10.13 "OversampleOutputCycle" register. This address determines where in the output control buffer the new data should be copied to. In order to calculate this address, you must account for the contents of the 4.16.4.11.10.17 "OversampleInputCycle" register, which contains the address of the most recently output data, and the transfer time to the module. To help avoid incorrect addressing of the output control buffer, the buffer section that is capable of being written to can be limited using the 4.16.4.11.10.8 "OversampleOutputWindow" register. This window will always be shifted relative to the current sample address. An "OutputCopyError" will be triggered if an attempt is made to write to an address that is outside of this window.

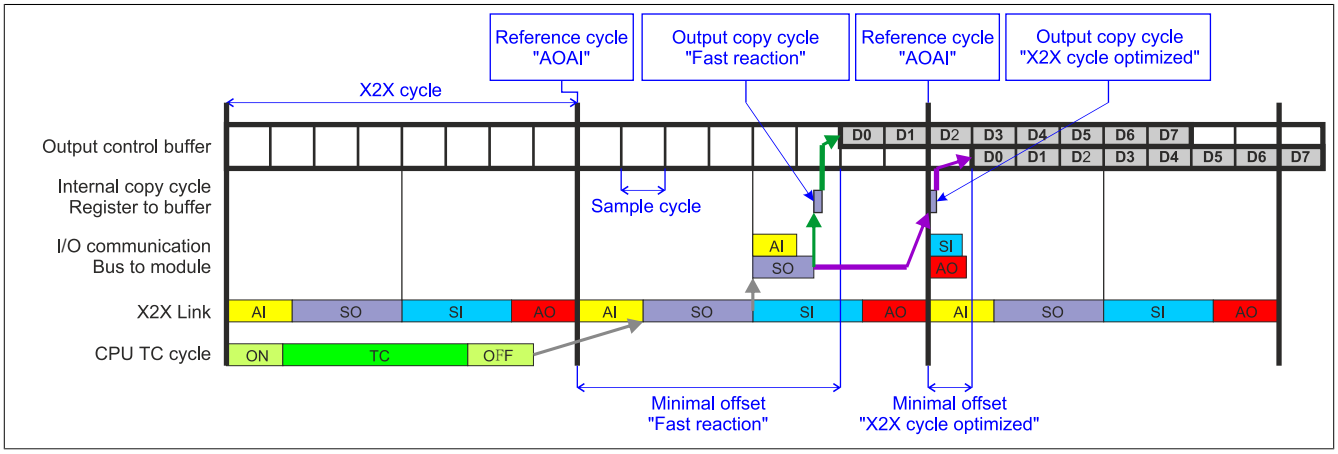
Example

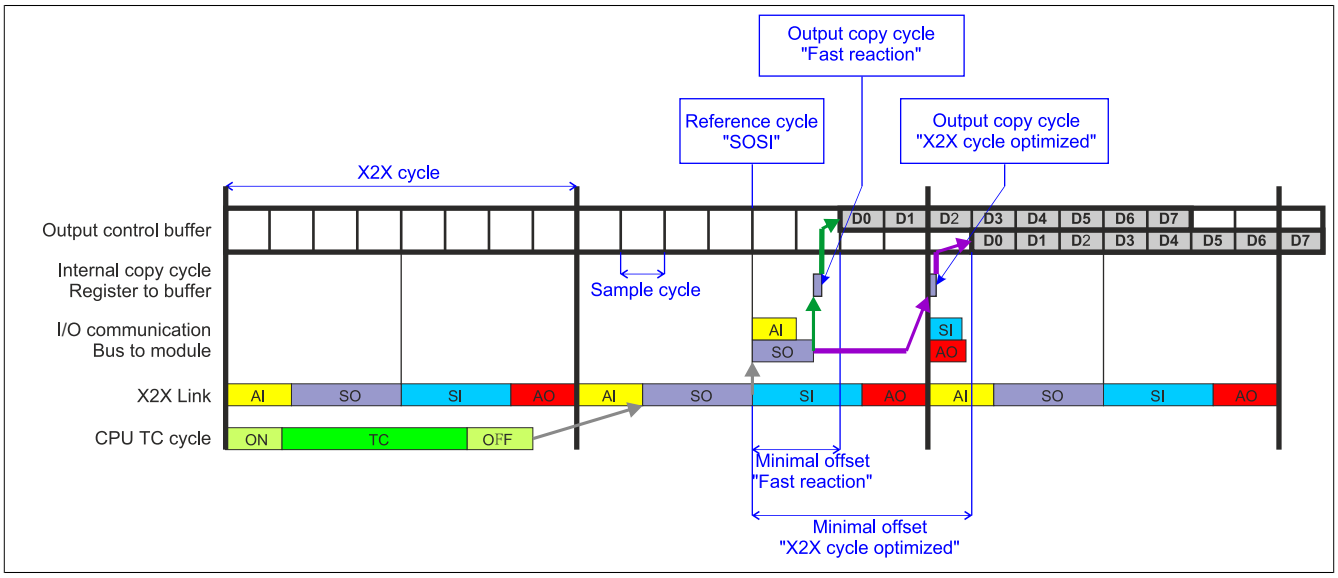
Timing from oversample input cycle to oversample output cycle in absolute output mode ("SI-frame generation = Fast reaction", "Output copy cycle = Fast reaction", 8 samples per X2X cycle):



4.16.8.10.10.3 Relative addressing of the output control buffer

When "OversampleOutputValidate = True", then the oversample output sample data is automatically copied to an address relative to the last referenced address at the defined "output copy cycle" time. The 4.16.4.11.10.14 "OversampleSampleOffset" register serves as the offset. The new data cannot start being output immediately at the "output copy cycle" time because it takes time to copy the data from the registers to the buffer. This means that an offset of 0 is not allowed. The relative output control buffer address + offset must point to an address within the "oversample output window". The "oversample output window" is always offset relative to the current sample address. An "OutputCopyError" is triggered if an attempt is made to write to an address that is outside of this window.





4.16.8.10.10.4 "CfO_OversampleMode" register

Name:
CfO_OversampleMode
"Output mode" in the AS I/O configuration
"Output control mode" in the AS I/O configuration.

The output control buffer can be configured globally for all channels in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Addressing the output control buffer "Output mode" in the AS I/O configuration.	0	Absolute addressing of the output control buffer
		1	Relative addressing of the output control buffer
1	Cyclic output control "Output control mode" in the AS I/O configuration.	0	Single - Output control buffer entry is marked invalid after execution.
		1	Continuous - Output control buffer entry is not changed.
2 - 7	Reserved	-	

Cyclic output control

If cyclic output control is enabled, then all data in the output control buffer is marked invalid as soon as it is output ("Output control mode = single"). An OutputControlError is generated if the module does not receive data in time, thereby causing a situation in which a bit that has already been output would be output in the buffer again. In such a situation, the output assumes the "Output default state" configured in the CfO_OversampleConfigOutput register.

If cyclic output control is disabled, then the data is output again if the output control buffer overflows ("Output control mode = continuous").

Information:

All 256 bits of the output control buffer are always output.

4.16.8.10.10.5 "CfO_OversampleSampleCycleID" register

Name:
CfO_OversampleSampleCycleID
"Sample cycle" in the AS I/O configuration.

The source of the sample cycle can be configured in this register. During each sample cycle, one bit from the output control buffers of the oversampled I/O channels is output to the configured physical output, and the status of the configured inputs is entered in one bit of the respective input status buffer.

Data type	Value	Information
USINT	2	System timer The value configured in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used as the sample cycle.
	3	Prescaled system timer The "prescaled system timer" is used as sample cycle.
	10	AOAI The sample cycle is clocked with the AOAI interrupt of the X2X cycle.
	14	SOSI The sample cycle is clocked with the SOSI interrupt of the X2X cycle.

4.16.8.10.10.6 "CfO_OversampleRelativeCycleID" register

Name:
CfO_OversampleRelativeCycleID
"Reference cycle" in the AS I/O configuration.

The source of the user interface reference cycle can be configured in this register.

- The input data is referenced at the time of the "reference cycle". The referenced data is then copied to the "oversample input sample register" at the time of "SI frame generation", while taking the "OversampleInputWindow" into account.
- With relative addressing of the output control buffer, the new sample data is copied to an address relative to the output control buffer address current to the "reference cycle".
- The reference cycle is also used to reference the sample cycle, and with it also the output data production and input data acquisition (e.g. to the X2X cycle).

Data type	Value	Information
USINT	2	System timer The value configured in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used as the reference cycle.
	3	Prescaled system timer The "prescaled system timer" is used as sample cycle.
	10	AOAI The sample cycle is referenced with the AOAI interrupt of the X2X cycle.
	14	SOSI The sample cycle is referenced with the SOSI interrupt of the X2X cycle.

4.16.8.10.10.7 "CfO_OversampleConsumeCycleID" register

Name:
CfO_OversampleConsumeCycleID
"Output copy cycle" in the AS I/O configuration.

At the time of the output copy cycle, data is copied from the 4.16.4.11.10.15 "OversampleOutput0NSample" registers into the output control buffer.

When "Output copy cycle = Fast reaction", it is not possible to determine when the data is copied to the output control buffer in either of the two addressing modes. The copy cycles will experience a certain degree of jitter depending on the module load. However, this only affects the moment of the internal copy procedures and therefore the moment of the earliest possible output sample. This will not affect the quality of the output signal. However, "Output copy cycle = Fast reaction" also has a negative effect on the minimum X2X cycle time.

When using the setting "Output copy cycle = X2X cycle optimized", be aware that the sample data cannot start being output immediately at the "Output copy cycle" time due to the internal copy cycle to the output control buffers.

Data type	Value	Information
USINT	10	X2X cycle optimized The output data is copied to the output control buffer with the AOAI interrupt of the X2X cycle.
	15	Fast reaction The output data is copied to the output control buffer immediately after being received.

4.16.8.10.10.8 "CfO_OversampleOutputBits" register

Name:
CfO_OversampleOutputBits
"User interface size" in the AS I/O configuration.

Specifies how many bits are transferred from the 4.16.4.11.10.15 "OversampleOutputONSample" registers to the output control buffers at the time of the "output copy cycle".

Data type	Value	Information
USINT	1 to 64	Output bits

4.16.8.10.10.9 "CfO_OversampleInputBits" register

Name:
CfO_OversampleInputBits
"User interface size" in the AS I/O configuration.

Specifies how many bits are transferred from the input status buffer to the 4.16.4.11.10.18 "OversampleInput0NSample" register during "SI frame generation".

Data type	Value	Information
USINT	1 to 64	Input bits

4.16.8.10.10.10 "CfO_OversampleOutputWindow" register

Name:
CfO_OversampleOutputWindow
"Output control mode" in the AS I/O configuration.

Determines the area in the output control buffer in which data can be written. The window is always offset relative to the current sample position. (a value of 128, for example, means that the 128 bits following the current sample cycle can be written to). An "OutputCopyError" is triggered if an attempt is made to write output sample data to a location outside of this window.
In AS, with the setting "Output control mode = Single", this register is set to 128 bits and with the setting "Output control mode = Continuous" it is set to 255 bits.

Data type	Value	Information
USINT	0 to 255	Output window

4.16.8.10.10.11 "CfO_OversampleInputWindow" register

Name:
CfO_OversampleInputWindow
"Input mode" in the AS I/O configuration.

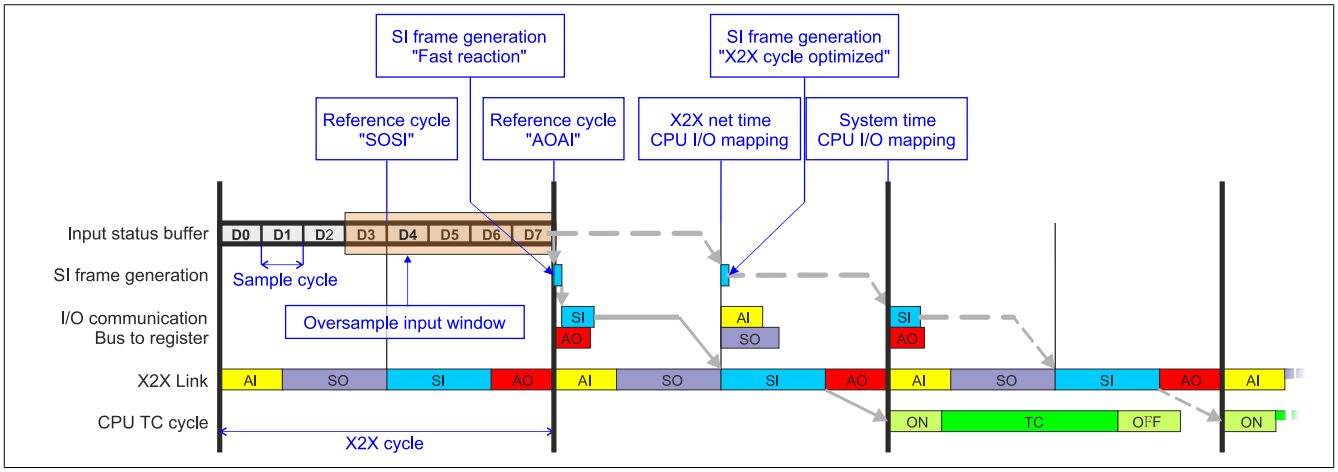
The "OversampleInputWindow" determines when the input data is referenced. It is located chronologically before "SI frame generation". If the reference time ("reference cycle") is within this window, then the referenced data is copied from the input status buffer to the OversampleInput0NSample register. If the time at which the reference occurs is outside the "OversampleInputWindow" then the data that is most recent at the time of "SI frame generation" is copied from the input status buffer to the 4.16.4.11.10.18 "OversampleInput0NSample" register.
This register is limited internally with to the value set in the 4.16.4.11.10.7 "CfO_OversampleInputBits" register.

Information:

As a result, the "OversampleInputTime" and the "OversampleInputCycle" are set either at the reference time or at the time of "SI frame generation".

In Automation Studio, this register is set to 63 when "Input mode = Referenced values" and to 0 when "Input mode = Most recent values".

Data type	Value	Information
USINT	0 to 63	Input window



4.16.8.10.10.12 "CfO_OversampleConfigInput" register

Name:
CfO_OversampleConfigInput
"Oversample I/O 01 →Input" to "Oversample I/O 04 → Input" in the AS I/O configuration

This register determines which physical input channel an oversample I/O input should be linked to.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Number of the physical input channel	0	Input channel 1
		..	
		7	Input channel 8
4 - 7	Reserved	-	

4.16.8.10.10.13 "CfO_OversampleConfigOutput" register

Name:
CfO_OversampleConfigOutput
"Oversample I/O 01 → Output" to "Oversample I/O 04 → Output" in the AS I/O configuration
"Oversample I/O 01 → Output control" to "Oversample I/O 04 → Output control" in the AS I/O configuration
"Oversample I/O 01 → Output default state" to "Oversample I/O 04 → Output default state" in the AS I/O configuration

This register helps configure the outputs of the individual oversample channels.

The "Output default state" bits determine which level the respective output assumes before oversampling is started. Furthermore, the output is set to the defined "Output default state" in the event of an error.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Number of the physical output channel "Oversample I/O 0x →Output" in the AS I/O configuration	2	Output channel 3
		3	Output channel 4
		6	Output channel 7
		7	Output channel 8
4	Output: Clear "Oversample I/O 0x →Output control" in the AS I/O configuration	0	Output cannot be reset by the oversample channel.
		1	Output can be reset by the oversample channel.
5	Output: Set "Oversample I/O 0x →Output control" in the AS I/O configuration	0	Output cannot be set by the oversample channel.
		1	Output can be set by the oversample channel.
6	Output default state: Clear "Oversample I/O 0x →Output default state" in the AS I/O configuration	0	Output not cleared by default
		1	Output cleared by default
7	Output default state: Set "Oversample I/O 0x →Output default state" in the AS I/O configuration	0	Output not set by default
		1	Output set by default

4.16.8.10.10.14 Oversample register - Configuration

Name:
OversampleEnable
OversampleOutputValidate

This register can be used to configure oversampling and the copy procedure for the output buffer.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	OversampleEnable	0	Disables oversampling (with the next reference cycle)
		1	Enables oversampling (with the next reference cycle)
1	OversampleOutputValidate	0	Disable the copy procedure to the output control buffer.
		1	Enables the copy procedure to the output control buffer. • Used to synchronize the oversampling procedure at startup. • This makes it possible to prevent new data from being transferred to the 4.16.4.11.10.15 "OversampleOutput0NSample" registers in each X2X cycle.
2 - 7	Reserved	-	

4.16.8.10.10.15 "OversampleOutputCycle" register

Name:
OversampleOutputCycle

When absolute addressing of the output control buffer is being used, this register specifies the address from which the new output sample data should be copied to the output control buffer.

Data type	Value	Information
USINT	0 to 255	Address of the output control buffer

4.16.8.10.10.16 "OversampleSampleOffset" register

Name:
OversampleSampleOffset

When relative addressing of the output control buffer is being used, this register serves as the offset for the new output sample data. (Sample address at the time of the "reference cycle" + Offset = address to which the new output sample data is copied in the output control buffer).

Data type	Value	Information
USINT	0 to 255	Offset of output sample data

4.16.8.10.10.17 "OversampleOutputSample" register

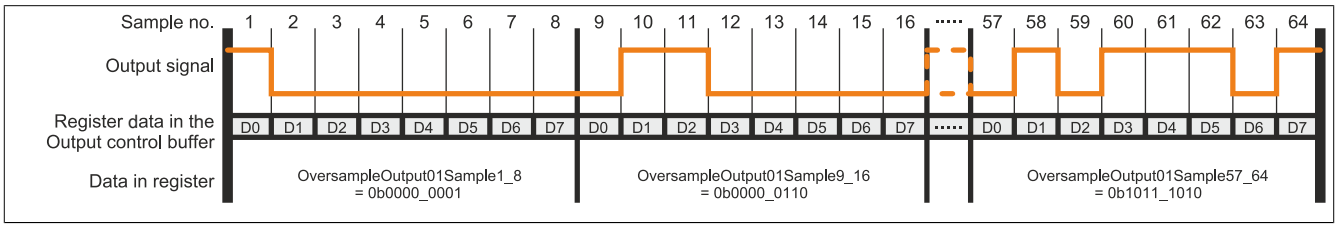
Name:
OversampleOutput01Sample1_8 to OversampleOutput04Sample1_8
OversampleOutput01Sample9_16 to OversampleOutput04Sample9_16
OversampleOutput01Sample17_24 to OversampleOutput04Sample17_24
OversampleOutput01Sample25_32 to OversampleOutput04Sample25_32
OversampleOutput01Sample33_40 to OversampleOutput04Sample33_40
OversampleOutput01Sample41_48 to OversampleOutput04Sample41_48
OversampleOutput01Sample49_56 to OversampleOutput04Sample49_56
OversampleOutput01Sample57_64 to OversampleOutput04Sample57_64

Contains the oversample output sample data. Up to 64 samples (8 bytes) for each oversample I/O channel can be synchronously transferred with a X2X cycle. This data is copied to the specified address (absolute or relative) in the output control buffer during the "output copy cycle". 1 bit of this data is then output during each "sample cycle" to the physical output that is assigned to the oversample I/O channel.
Bit 0 of "OversampleOutputSample8_1" is copied to the output control buffer first, meaning that it is the first bit that is output. "OversampleOutputSample64_57" bit 7 is the last bit to be output.

Data type	Value	Information
USINT	0 to 255	Output sample data

Example

Assignment of "OversampleOutputSample" register data to output signal



4.16.8.10.10.18 "OversampleInputTime" register

Name:
OversampleInputTime

This register contains the 2 low-order bytes of the X2X net time from the moment at which the oversample input data was referenced. This provides an easy way to accurately calculate the time of each individual input sample.

Data type	Value	Information
INT	-32,768 to 32,767	X2X net time of the input data

4.16.8.10.10.19 "OversampleInputCycle" register

Name:
OversampleInputCycle

This register provides the width of the input status buffer address for the input sample data.
Furthermore, the value in this register can be used for referencing an absolute addressing of the output control buffer.

Data type	Value	Information
USINT	0 to 255	Input status buffer address

4.16.8.10.10.20 "OversampleInputSample" register

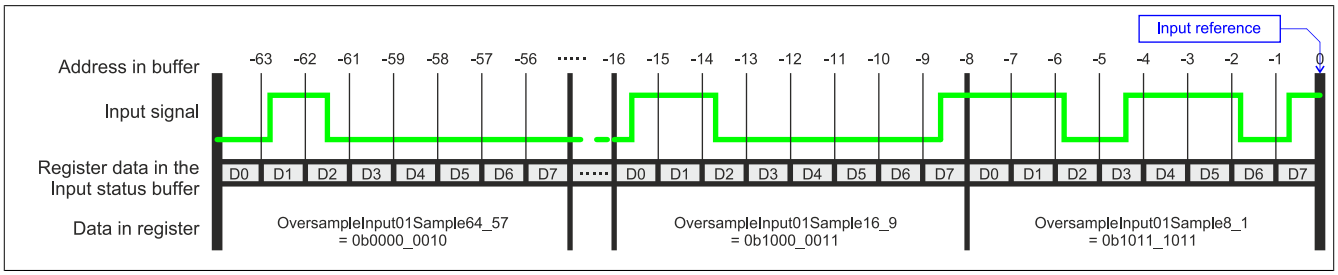
Name:
OversampleInput01Sample8_1 to OversampleInput04Sample8_1
OversampleInput01Sample16_9 to OversampleInput04Sample16_9
OversampleInput01Sample24_17 to OversampleInput04Sample24_17
OversampleInput01Sample32_25 to OversampleInput04Sample32_25
OversampleInput01Sample40_33 to OversampleInput04Sample40_33
OversampleInput01Sample48_41 to OversampleInput04Sample48_41
OversampleInput01Sample56_49 to OversampleInput04Sample56_49
OversampleInput01Sample64_57 to OversampleInput04Sample64_57

The data of the four oversample input status buffers are copied to this register at the time of "SI frame generation". A maximum of 64 samples (8 bytes) per oversample I/O channel can be synchronously retrieved from the oversample input status buffer with each X2X cycle.
The most recent input sample bit is stored in "OversampleInputSample8_1" bit 7. The oldest input sample is stored in "OversampleInputSample64_57" bit 0.

Data type	Value	Information
USINT	0 to 255	Input sample data

Example

Input signal and resulting data in "OversampleInputSample"



4.16.8.10.11 Edge detection

The module's edge detection function identifies edges with µs precision. The concept is based on a maximum of 4 units. A master and a slave edge can be configured for each unit.

At each master edge, the net time of the master edge and the net time of a previous slave edge (if present) are logged. A "master counter" and a "slave counter" can always be used to determine how many edges have been detected since the last X2X cycle.

The module has a history for the timestamp and counters, which can store up to 4 elements per unit. This makes it possible to measure multiple edges precisely within a single X2X cycle.

4.16.8.10.11.1 "CfO_EdgeDetectPollCycleID" register

Name:
CfO_EdgeDetectPollCycleID
"Polling cycle" in the AS I/O configuration.

The source of the polling cycle can be configured in this register.

Information:

The polling cycle must be less than or equal to 255 µs. Setting the cycle > 255 µs causes an EdgeDetectError.

Data type	Value	Information
USINT	2	System timer The time set in the 4.16.4.11.7.1 "CfO_SystemCycleTime" register is used for the polling cycle.
	3	Prescaled system timer The time set in the 4.16.4.11.7.3 "CfO_SystemCyclePrescaler" register is used for the polling cycle.

4.16.8.10.11.2 "CfO_EdgeDetectEventEnable" register

Name:
CfO_EdgeDetectEventEnable
"Edge detection mode" in the AS I/O configuration.

The bits in this register determine at which edges on the individual input channels an interrupt should be triggered for the edge detection.

In "event triggered" mode, the net time of each edge is recorded immediately an interrupt. However, an extremely large amount of interrupts within a short amount of time can prevent the module from being able to process any other operations in time!

In "polling" mode, only the net time of the first edge that occurs within a polling cycle is recorded. This ensures that the module is not overloaded by too many edges.

In the AS IO configuration, this register is initialized with 0x00000000 when "Edge detection mode = polling" and with 0xFFFFFFFF when "Edge detection mode = event triggered".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Physical input 1	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
...		...	
7	Physical input 8	0	No interrupt triggered at falling edge.
		1	Interrupt triggered at falling edge.
8 - 15	Reserved	-	
16	Physical input 1	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
...		...	
23	Physical input 8	0	No interrupt triggered at rising edge.
		1	Interrupt triggered at rising edge.
24 - 31	Reserved	-	

4.16.8.10.11.3 "CfO_EdgeDetectUnitMode" register

Name:
CfO_EdgeDetectUnit01Mode to CfO_EdgeDetectUnit04Mode
"Time base" in the AS I/O configuration.
"Slave edge" in the AS I/O configuration.
"Master edge" in the AS I/O configuration.

When using a "time base" with 1/8 µs resolution, keep in mind that the timestamps produced also have a resolution of exactly 1/8 µs. The respective conversions must be made for calculating in combination with the CPU system time or X2X net time.

Furthermore, synchronization jitter also plays a role when using the setting "time base = net time resolution 1/8 µs" (see: 4.16.4.11.4.3 "Synchronization jitter"). This means that exactly identical input edges can cause slight differences in the results. If a 100% exact 1/8 µs resolution is required, then the "local resolution 1/8 µs" must be used.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	"Time base" in the AS I/O configuration.	0	Local time 1/8 µs (AS: Local resolution 1/8 µs)
		1	Local time 1 µs (AS: Local resolution 1 µs)
		2	Net time 1/8 µs (AS: Net time resolution 1/8 µs)
		3	Net time 1 µs (AS: Net time resolution 1 µs)
2 - 5	Reserved	-	
6	"Slave edge" in the AS I/O configuration.	0	Disabled
		1	Enabled
7	"Master edge" in the AS I/O configuration.	0	Disabled
		1	Enabled

4.16.8.10.11.4 "CfO_EdgeDetectUnitLeading" register

Name:
CfO_EdgeDetectUnit01Leading to CfO_EdgeDetectUnit04Leading
"Slave leading" in the AS I/O configuration.

When a slave edge occurs, the current net time is always saved within the module. A FIFO is provided inside the module which always stores the last 16 slave stamps (even when a master edge occurs).

This value determines from which position the slave time should be retrieved from the FIFO when a master edge occurs. This can be used to measure average periodic signals over multiple cycles.

Data type	Value	Information
USINT	0 to 15	Position in the slave edge FIFO

4.16.8.10.11.5 "CfO_EdgeDetectUnitMaster" register

Name:
CfO_EdgeDetectUnit01Master to CfO_EdgeDetectUnit01Master
"Master edge" in the AS I/O configuration.

This register is used to select the source of the master edge for the respective "edge detection unit".

Data type	Value	Information
USINT	0	Rising edge on physical input 1
	...	...
	7	Rising edge on physical input 8
	16	Falling edge on physical input 1
	...	...
	23	Falling edge on physical input 8

4.16.8.10.11.6 "CfO_EdgeDetectUnitSlave" register

Name:
CfO_EdgeDetectUnit01Slave to CfO_EdgeDetectUnit04Slave
"Slave edge" in the AS I/O configuration.

This register is used to select the source of the slave edge for the respective "edge detection unit".

Data type	Value	Information
USINT	0	Rising edge on physical input 1
	...	...
	7	Rising edge on physical input 8
	16	Falling edge on physical input 1
	...	...
	23	Falling edge on physical input 8

4.16.8.10.11.7 "EdgeDetectSlavecount" register

Name:
EdgeDetect01Slavecount to EdgeDetect04Slavecount

The reference pulses of the detected slave edges are counted continuously in this register. The contents of this register are only updated when a master edge occurs. Up to 4 history elements can be enabled for these counters in the AS I/O configuration. These counters can detect if multiple slave edges occur before a master edge.

Data type	Value	Information
SINT	-128 to 127	Number of detected slave edges (8-bit)
INT	-32,768 to 32,767	Number of detected slave edges (16-bit)

4.16.8.10.11.8 "EdgeDetectDifference" register

Name:
EdgeDetect01Difference to EdgeDetect04Difference

Contains the time difference between a master edge and the last slave edge addressed via "Slave leading".

Data type	Value	Information
INT	-32,768 to 32,767	Time difference between master/slave edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Time difference between master/slave edge (32-bit)

4.16.8.10.11.9 "EdgeDetectMastercount" register

Name:
EdgeDetect01Mastercount to EdgeDetect04Mastercount

The reference pulses of the detected master edges are counted in this register.

Data type	Value	Information
SINT	-128 to 127	Number of detected master edges (8-bit)
INT	-32,768 to 32,767	Number of detected master edges (16-bit)

4.16.8.10.11.10 "EdgeDetectMastertime" register

Name:
EdgeDetect01Mastertime to EdgeDetect04Mastertime

The exact net time is copied in this register when a master edge occurs.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of master edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of master edge (32-bit)

4.16.8.10.11.11 "EdgeDetectSlavetime" register

Name:
EdgeDetect01Slavetime to EdgeDetect04Slavetime

When a master edge occurs, the exact net time of any slave edge that may have occurred prior to the master edge and addressed by "Slave leading" is copied in this register. Only one slave time can be taken from the "Slave leading FIFO" for each master edge. Only EdgeDetectSlavecount can indicate if multiple edges have occurred before a master edge.

Data type	Value	Information
INT	-32,768 to 32,767	Net time of the slave edge (16-bit)
DINT	-2,147,483,648 to 2,147,483,647	Net time of the slave edge (32-bit)

History:

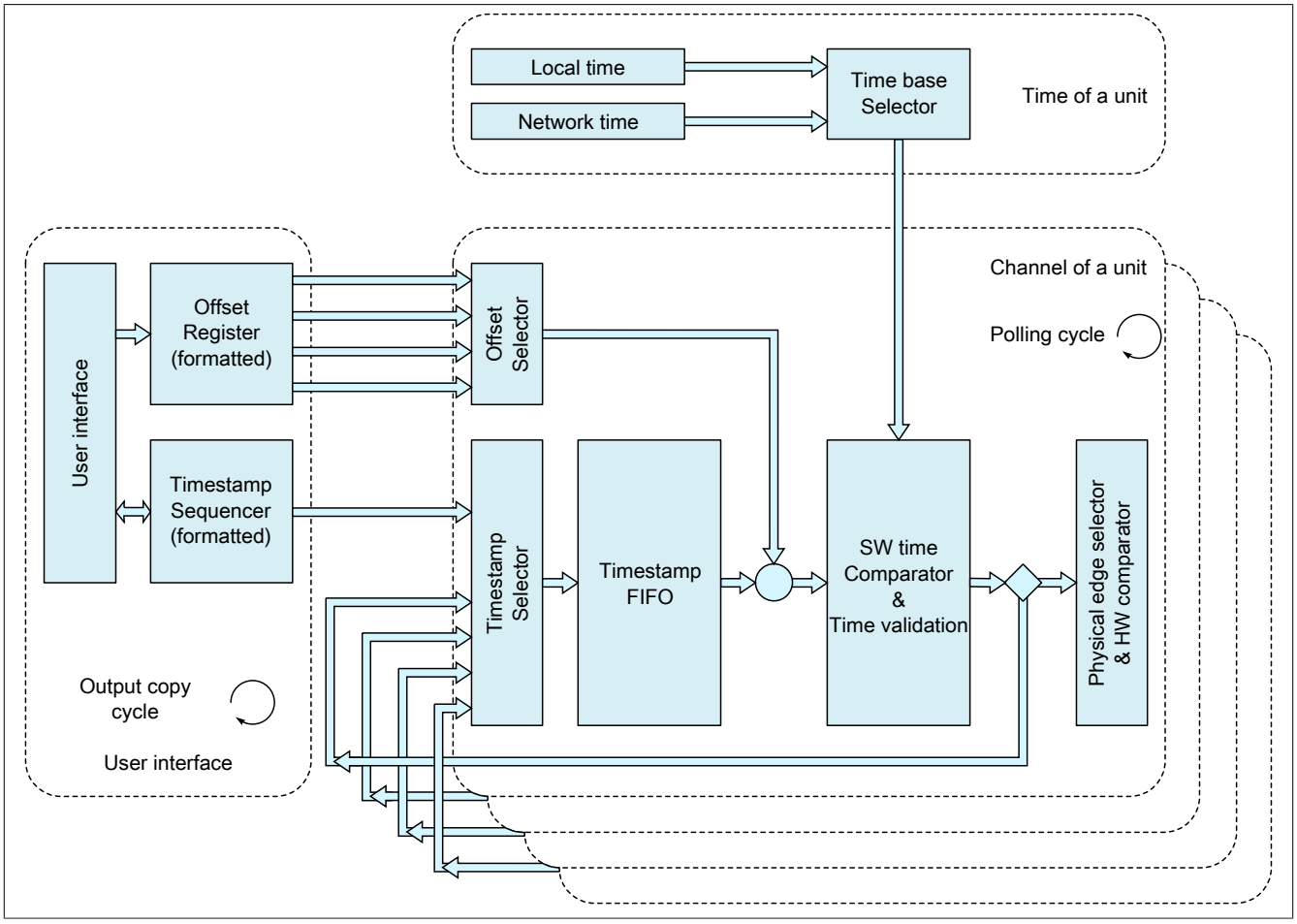
In AS, a history of up to 4 elements can be enabled in the I/O configuration for the following registers: 4.16.8.10.11.7 "EdgeDetectSlavecount", 4.16.8.10.11.8 "EdgeDetectDifference", 4.16.4.11.11.10 "EdgeDetectMastertime" and 4.16.8.10.11.11 "EdgeDetectSlavetime". Configured history elements are all transferred synchronously with each X2X cycle. This makes it possible to measure multiple edges precisely within a single X2X cycle.

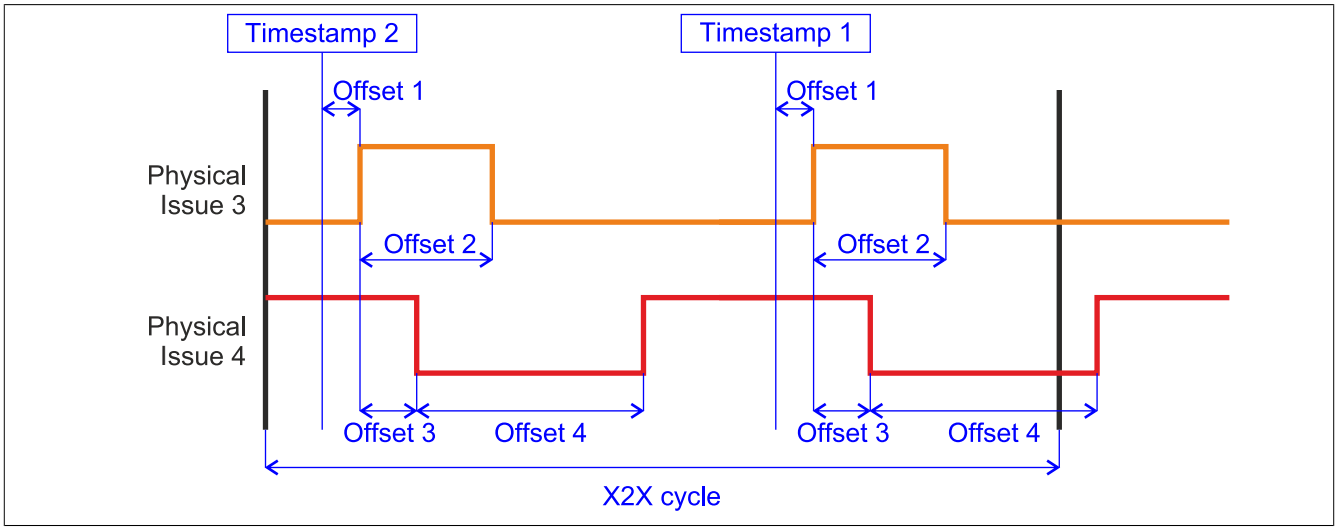
Information:

When the history is enabled, the maximum number of data bytes (28 bytes) that can be transferred synchronously via the X2X Link is reached quickly (especially if 32-bit data points are used).

4.16.8.10.12 Edge generator

The edge generator is based on 4 units. The units are able to generate edges independently of the X2X cycle. For each unit, up to 4 timestamps can be set per X2X cycle. The individual edges can then be referenced to this timestamp or to other edges using an offset.





4.16.8.10.12.1 Mode "DigitalCamSwitch"

"Unit 0x" in AS I/O configuration.

Starting with upgrade 1.1.0.2, "DigitalCamSwitch" mode can also be selected for each unit when configuring the edge generator in AS Studio.
In this mode, the entire configuration and operation take place exclusively with the function blocks from the "ASMcDcs" motion library. For more information, see the corresponding ASMcDcs function block descriptions.

4.16.8.10.12.2 "CfO_EdgeGenPollCycleEventID" register

Name:
CfO_EdgeGenPollCycleEventID
"Generation cycle" in the AS I/O configuration.

To ensure edge output with µs precision, edge generation is based on internal hardware components. One such comparator is available for one rising and one falling edge respectively for each physical output channel. The data for the comparators is prepared in "EdgeGenPollCycle". Therefore, a maximum of one rising and one falling edge can be generated for each physical output channel per "EdgeGenPollCycle". If timestamps are set that cannot be processed in time due to this limitation, then an "EdgeGen0Warning" is generated. Processing of such timestamps is made up for as quickly as possible, as long as they are within "EdgeGenUnit0PickupDiff".
A shorter "Generation cycle" means that an enabled edge generator function has a less negative effect on the minimum X2X cycle time.

Data type	Value	Information
USINT	2	System timer
	3	Prescaled system timer

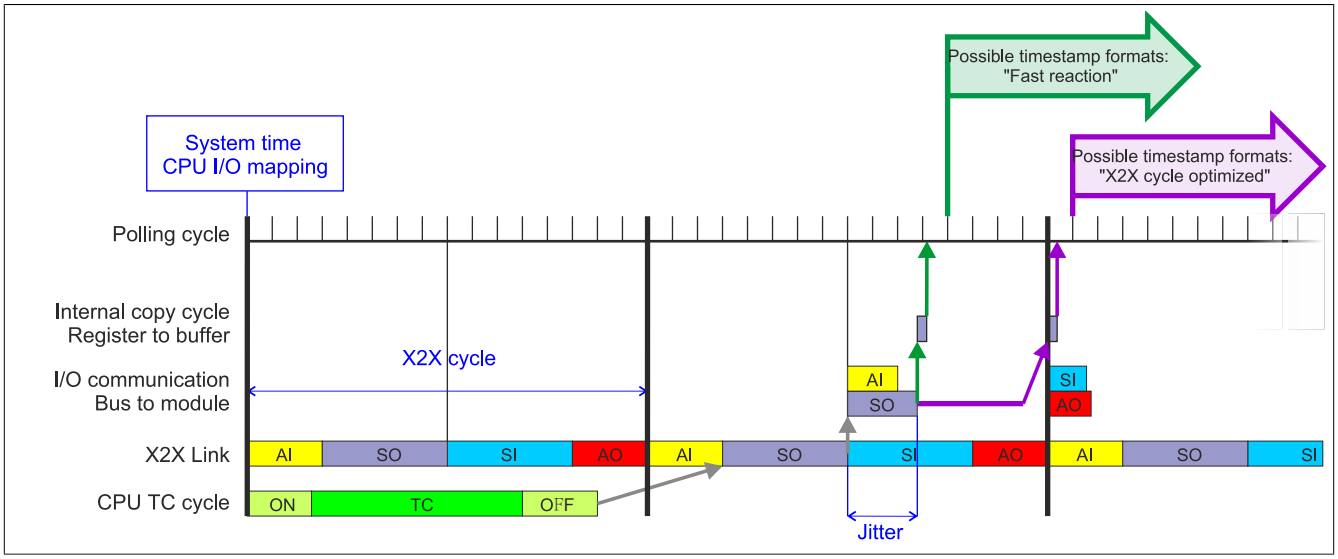
4.16.8.10.12.3 "CfO_EdgeGenConsumeCycleEventID" register

Name:
CfO_EdgeGenConsumeCycleEventID

This register determines when the output data for edge generation is applied within the X2X cycle.

Data type	Value	Information
USINT	10	"X2X cycle optimized" The data is force-applied between the periods ASYNC IN (AI) and ASYNC OUT (AO).
	15	"Fast reaction (with jitter)" The data is applied immediately after SYNC OUT (SO) processing.

The "Fast reaction" setting results in jitter because the copy cycle of the SYNC OUT data can take different amounts of time. However, this only affects the moment at which the internal copy cycle takes place and therefore possibly also the earliest possible timestamp. Timestamps that are set outside of this jitter range are not affected by this.



4.16.8.10.12.4 "CfO_EdgeGenUnitMode" register

Name:
CfO_EdgeGenUnit01Mode to CfO_EdgeGenUnit04Mode
"Time base" in the AS I/O configuration.
"Timestamp format" in the AS I/O configuration.
"Offset format" in the AS I/O configuration.
"Unit 01" to "Unit 04" in the AS I/O configuration

These registers contain the configuration bits for the respective units.

If "timestamp resolution = 1/8 µs" is used, be aware that the timestamp data must also have a resolution of 1/8 µs. Because the CPU system time and the X2X net time only have µs resolution, the system time or the net time must be offset by 3 bits to the left or multiplied by 8 in the application. This value can then be used as reference for timestamps with a resolution of 1/8 µs. It is also possible to use 1/8 µs timestamps from input edges as a reference.

When using the net time with 1/8 µs resolution, the synchronization jitter affects the output results (see: 4.16.4.11.4.3 "Synchronization jitter").

Because the local time is not synchronized with the CPU system time or the X2X net time, this can only be used effectively together with a time source from the module (e.g. input edge timestamp on "local time").

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Resolution of the timestamp "Time base" in the AS I/O configuration.	0	1 µs
		1	1/8 µs
1	Number of bits in the timestamp register "Timestamp format" in the AS I/O configuration.	0	16-bit
		1	32-bit
2	Offset resolution "Time base" in the AS I/O configuration.	0	1 µs
		1	1/8 µs
3	Number of bits in the offset register "Offset format" in the AS I/O configuration.	0	16-bit
		1	32-bit
4	Time base "Time base" in the AS I/O configuration.	0	Net time
		1	Local time
5 - 6	Reserved	-	
7	Enable/disable units "Unit 0x" in the AS I/O configuration.	0	Disabled
		1	Enabled

4.16.8.10.12.5 "CfO_EdgeGenUnitTimestampFifoLim" register

Name:
CfO_EdgeGenUnit01TimestampFifoLim to CfO_EdgeGenUnit04TimestampFifoLim

Specifies how many timestamps in the FIFO a unit can be transferred to. The FIFO serves as a memory buffer for timestamps in the future. The timestamps must be entered in the FIFO in the same order in which they should be output. This means it is not possible to set a timestamp in the future followed by an earlier timestamp. The 4.16.8.10.12.11 "EdgeGenSequenceReadback" register can be used to indicate if the defined limit has been reached.

Data type	Value	Information
USINT	1 to 12	FIFO limit (AS default: 12)

4.16.8.10.12.6 "CfO_EdgeGenUnitTimestampRegCount" register

Name:
CfO_EdgeGenUnit01TimestampRegCount to CfO_EdgeGenUnit04TimestampRegCount
"Timestamp elements" in the AS I/O configuration.

This register determines how many timestamps can be transferred per X2X cycle.

Data type	Value	Information
USINT	1 to 4	Number of timestamps per X2X cycle

4.16.8.10.12.7 "CfO_EdgeGenUnitPickupDiff" register

Name:
CfO_EdgeGenUnit01PickupDiff to CfO_EdgeGenUnit04PickupDiff

This register determines how far in the past timestamps can go so that the difference in time can be regained. Timestamps in the past are processed as quickly as possible as long as they are located within the difference specified in this register. EdgeGenWarning is triggered if a timestamp was not able to be processed in time and its difference had to be regained. If the difference in time for a timestamp was not able to be regained because it is outside of the specified difference value, then "EdgeGenError" is also reported in addition to "EdgeGenWarning".

In AS, if "Timestamp format = 16-bit" this register is initialized with 65535 (0xFFFF), and if "Timestamp format = 32-bit" it is initialized with 134,217,728 (0x8000000).

Data type	Value	Information
UDINT	0 to 65,535	Difference to be regained in µs when "Offset format = 16-bit"
	0 to 134217728	Difference to be regained in µs when "Offset format = 32-bit"

4.16.8.10.12.8 "CfO_EdgeGenUnitConfigEdge" register

Name:
CfO_EdgeGenUnit01ConfigEdge to CfO_EdgeGenUnit04ConfigEdge
"Unit 01→ Edge" to "Unit 04→ Edge" in the AS I/O configuration.
"Unit 01→ Mode" to "Unit 04→ Mode" in the AS I/O configuration.
"Unit 01→ Offset" to "Unit 04→ Offset" in the AS I/O configuration.
"Unit 01→ Unit 01" to "Unit 04→ Unit 04" in the AS I/O configuration.

The properties of each of the 4 edges of a unit can be configured in this register.

Ring-shaped chain of edges:

If the individual edges are linked together in a ring shape (e.g. edge 2 is relative to edge 1 and edge 1 is relative to edge 2) then a header must be determined for the ring using bit 11 "ring head enable" bit so that this type of cycle can start without timestamp. In AS, the "ring head enable" bit (bit 11) is set for edge 1 in all units by default. If this type of ring is branched (e.g. a third edge is relative to an edge within the ring) then you must make sure that the internal FIFO, which is available to every physical I/O edge, does not overflow. This happens if more than 12 edges are created by the ring, but should not be output until much later. If this situation occurs, whereby a ring creates edges even though the FIFO is full, then an EdgeGenError error is generated.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 4	Physical edge "Unit 0x →Edge" in the AS I/O configuration.	2	Channel 3 rising edge
		3	Channel 4 rising edge
		6	Channel 7 rising edge
		7	Channel 8 rising edge
		18	Channel 3 falling edge
		19	Channel 4 falling edge
		22	Channel 7 falling edge
		23	Channel 8 falling edge
5 - 7	Reserved	-	
8 - 10	Timestamp of FIFO source "Unit 0x →Mode" in the AS I/O configuration.	0	User interface, absolute
		1 to 3	Reserved
		4	Edge 1, relative
		5	Edge 2, relative
		6	Edge 3, relative
		7	Edge 4, relative
11	Ring-shaped chain Default in AS for "Edge 01 = 1", "Edge 02 = 0", "Edge 03 = 0", "Edge 04 = 0"	0	Disabled
		1	Enabled
12 -13	Offset register numbers "Unit 0x →Offset" in the AS I/O configuration.	0	Offset register 0
		1	Offset register 1
		2	Offset register 2
		3	Offset register 3
14	Reserved	-	
15	Switch edge on/off. "Unit 0x →Unit 0x" in the AS I/O configuration.	0	Disabled
		1	Enabled

4.16.8.10.12.9 "EdgeGenEnable" register

Name:
EdgeGen01Enable to EdgeGen04Enable
EdgeGen01EnableReadback to EdgeGen04EnableReadback
"Unit 01" to "Unit 04" in the AS I/O configuration

The units of the edge generator can be enabled/disabled using this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	EdgeGen0NEnable EdgeGen0NEnableReadback	0	Disabled
		1	Enabled
1 - 7	Reserved	-	

4.16.8.10.12.10 "EdgeGenSequence" register

Name:
EdgeGen01Sequence to EdgeGen04Sequence

If new timestamp data is to be applied to the module, then the sequence number must be increased by the number of timestamp elements that have to be applied. If multiple elements are transferred within one X2X cycle, then you must make sure that the individual timestamps are placed in the FIFO in the same order in which they occur chronologically. This means that data from "EdgeGenTimestamp4" arrives first in the FIFO, and data from "EdgeGenTimestamp1" arrives last.

Data type	Value	Information
SINT	-128 to 127	Sequence number for generating switching edges

4.16.8.10.12.11 "EdgeGenSequenceReadback" register

Name:
EdgeGen01SequenceReadback to EdgeGen04SequenceReadback

This register reads back the sequence number. Like the 4.16.8.10.12.10 "EdgeGenSequence" register, this register is increased when the transferred timestamps are able to be accepted by the module. If the module is not able to accept any new stamps (e.g. because EdgeGenUnitTimestampFifoLim has been reached), then this register indicates the number of the last sequence accepted by the module.

Data type	Value	Information
SINT	-128 to 127	Last sequence number accepted by the module for edge generation.

4.16.8.10.12.12 Offset formats

Automation Studio provides 3 different parameters for setting offsets.

- **Offset format:** This parameter allows you to select the file type (16 or 32-bit) for cyclic transfer, and only affects the "EdgeGenOffset" register.
  Acyclic transfer of offset values with the "CfO_EdgeGenOffset_32bit" register is not affected by this parameter and always remains 32 bits wide.
- **Offset 01 to Offset 04:** This parameter has 2 possible settings:
  - Initial configuration: The offset value is only written once during configuration.
  - Cyclic data: A data point is created in the AS I/O mapping and the offset value is written cyclically.
- **Offset 01 value to Offset 04 value:** The actual offset value.

"EdgeGenOffset" register

Name:
EdgeGen01Offset1 to EdgeGen04Offset1
...
EdgeGen01Offset4 to EdgeGen04Offset4
"Offset 01 value" to "Offset 04 value" in the AS I/O configuration

The 4 offsets of an edge generator unit are written in this register. Depending on the configuration in the 4.16.8.10.12.4 "Edge generator unit mode" register, the offset values are handled as µs or in 1/8 µs.

For information regarding how to use the register and set the offset formats in Automation Studio, see 4.16.8.10.12.12 "Offset formats".

Data type	Value	Information
UINT	0 to 65535	16-bit offset
UDINT	0 to 134217728	Offset when "Offset format = 32-bit" and "Time base" = 1 µs
	0 to 1,073,741,824	Offset when "Offset format = 32-bit" and "Time base" = 1/8 µs

"CfO_EdgeGenOffset_32bit" register

Name:
CfO_EdgeGen01Offset_32bit1 to CfO_EdgeGen04Offset_32bit1
...
CfO_EdgeGen01Offset_32bit4 to CfO_EdgeGen04Offset_32bit4

The 4 offsets of an edge generator unit can be written acyclically using this register. Depending on the configuration in the 4.16.8.10.12.4 "Edge generator unit mode" register, the offset values are handled as µs or in 1/8 µs.

For information regarding how to use the register and set the offset formats in Automation Studio, see 4.16.8.10.12.12 "Offset formats".

Data type	Value	Information
UDINT	0 to 134217728	Offset when "Offset format = 32-bit" and "Time base" = 1 µs
	0 to 1,073,741,824	Offset when "Offset format = 32-bit" and "Time base" = 1/8 µs

4.16.8.10.12.13 "EdgeGenTimestamp" register

Name:
EdgeGen01Timestamp1 to EdgeGen04Timestamp1
...
EdgeGen01Timestamp4 to EdgeGen04Timestamp4

Registers for the timestamps to which edges pending generation are referenced. Up to 4 timestamp elements (net times) can be transferred per X2X cycle. Between 1 and 4 of these timestamp elements are placed in the FIFO, depending on how much the sequence number is increased by. If an attempt is made to set timestamps to a time that has already passed, then a EdgeGenWarning is generated (see: 4.16.8.10.12.7 "CfO_EdgeGenUnitPickupDiff" register).

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.16.8.10.13 Minimum X2X cycle time

The minimum X2X cycle time is strongly dependent on the configured functions and the resulting load on the module. In general, a "Fast reaction" setting and a very short system cycle (50 µs) have a negative influence on the minimum X2X cycle time. This can lead to errors when the X2X cycle time is short.

4.17 Dummy modules

The dummy module is used as a placeholder to prevent configuration errors caused by empty slots.

4.17.1 Brief information

Product ID	Short description	on page
X20IF0000	X20 dummy interface module (non-functional)	1869
X20ZF0000	Dummy X20 module (non-functional)	1870
X20ZF000F	Dummy X20 module (non-functional)	1872

4.17.2 X20IF0000

4.17.2.1 General information

Covers for unused interface module slots are included with X20 CPUs. If an X20 system is used in a maritime environment, then the system will be subjected to increased vibration fatigue. In order to achieve the stability necessary for operation, the X20IF0000 dummy interface module from the X20 series is used instead of the covers.

- Cover for unused interface module slots
- IF dummy modules required if the X20 system is subjected to increased vibration fatigue
- Module with no electrical function

4.17.2.2 Order data

Model number	Short description	Figure
	Dummy modules	
X20IF0000	X20 dummy interface module (non-functional)	

Table 379: X20IF0000 - Order data

4.17.2.3 Technical data

Product ID	X20IF0000
Short description	
Accessories	Non-functional dummy module
General information	
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
GL	Yes
LR	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In X20 CPU, X20BB3x and X20BB8x

Table 380: X20IF0000 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.17.3 X20ZF0000

4.17.3.1 General information

The module is used as a place holder for later system expansion.

- Place holder for later system expansion
- Used as a terminal holder
- Module with no electrical function

4.17.3.2 Order data

Model number	Short description	Figure
	Dummy modules	
X20ZF0000	Dummy X20 module (non-functional)	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 381: X20ZF0000 - Order data

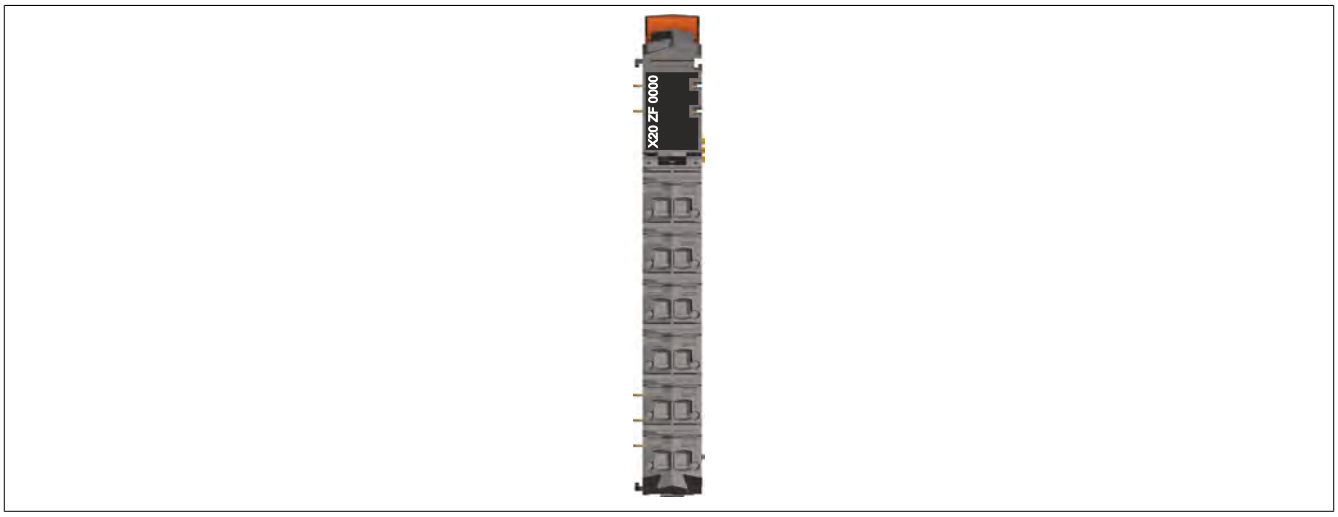
4.17.3.3 Technical data

Product ID	X20ZF0000
Short description	
Accessories	Non-functional dummy module
General information	
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
GL	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or 1x X20TB12 terminal block separately Order 1x X20BM11 bus module or 1x X20BM01 supply bus module separately
Spacing	$12.5^{+0.2}$ mm

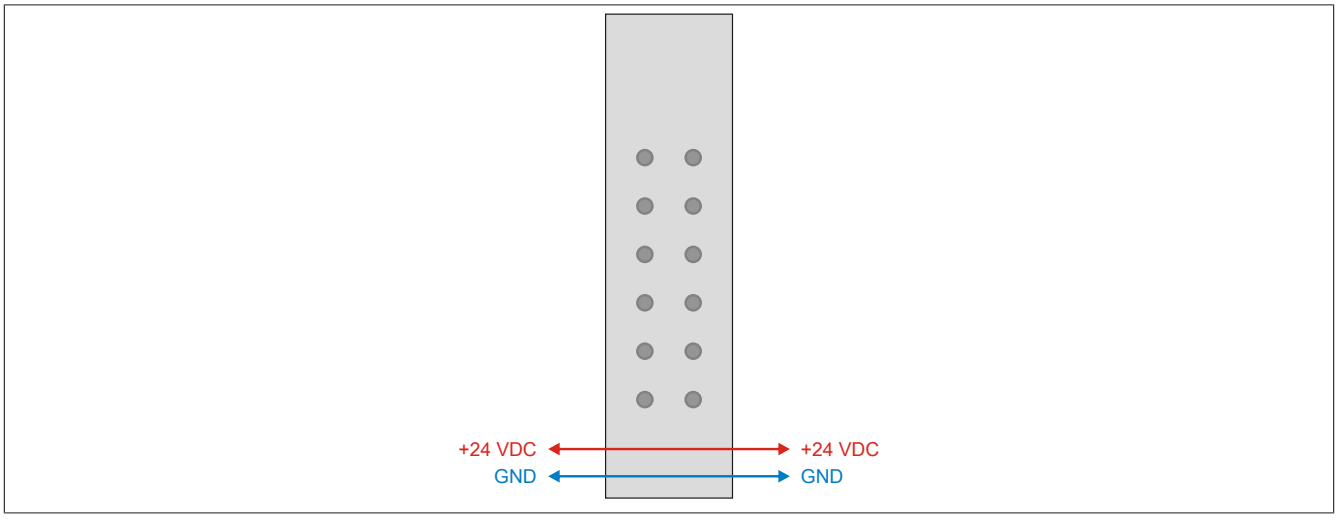
Table 382: X20ZF0000 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.17.3.4 Pinout



4.17.3.5 Connection example



4.17.4 X20ZF000F

4.17.4.1 General information

The module is used as a placeholder for later system expansion.

- Placeholder for later system expansion
- Used as a terminal holder
- Module with no electrical function

4.17.4.2 Order data

Model number	Short description	Figure
	Dummy modules	
X20ZF000F	Dummy X20 module (non-functional)	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1E	X20 terminal block, 12-pin, 24 VDC keyed, 2x PT1000 integrated for terminal temperature compensation	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 383: X20ZF000F - Order data

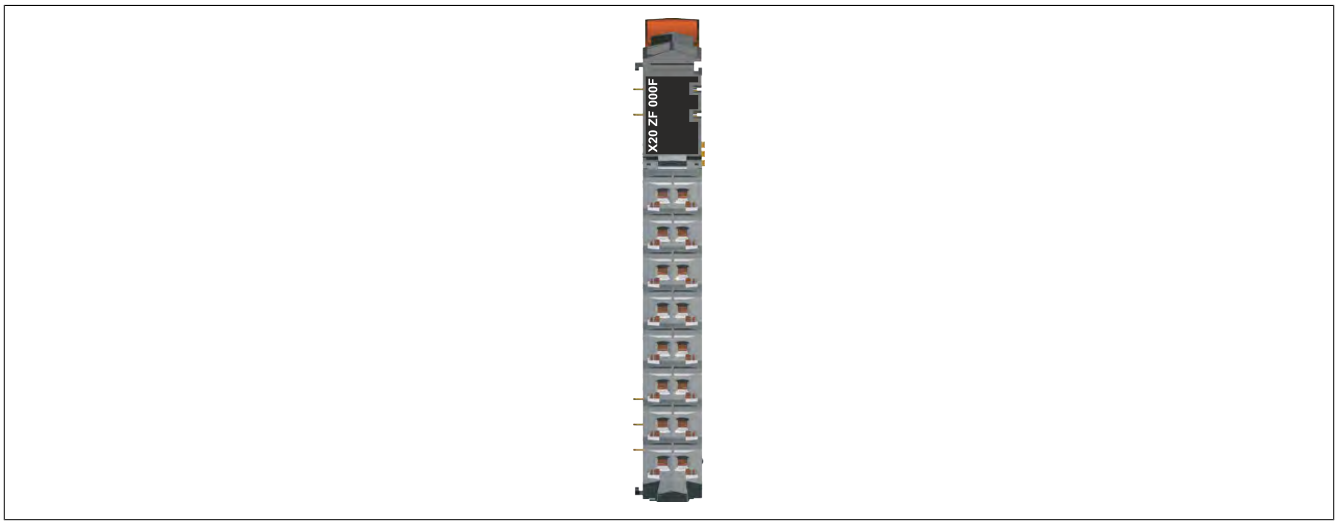
4.17.4.3 Technical data

Product ID	X20ZF000F
Short description	
Accessories	Non-functional dummy module
General information	
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1]	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1E or 1x X20TB1F terminal block separately Order 1x X20BM11 bus module or 1x X20BM01 supply bus module separately
Spacing	$12.5^{+0.2}$ mm

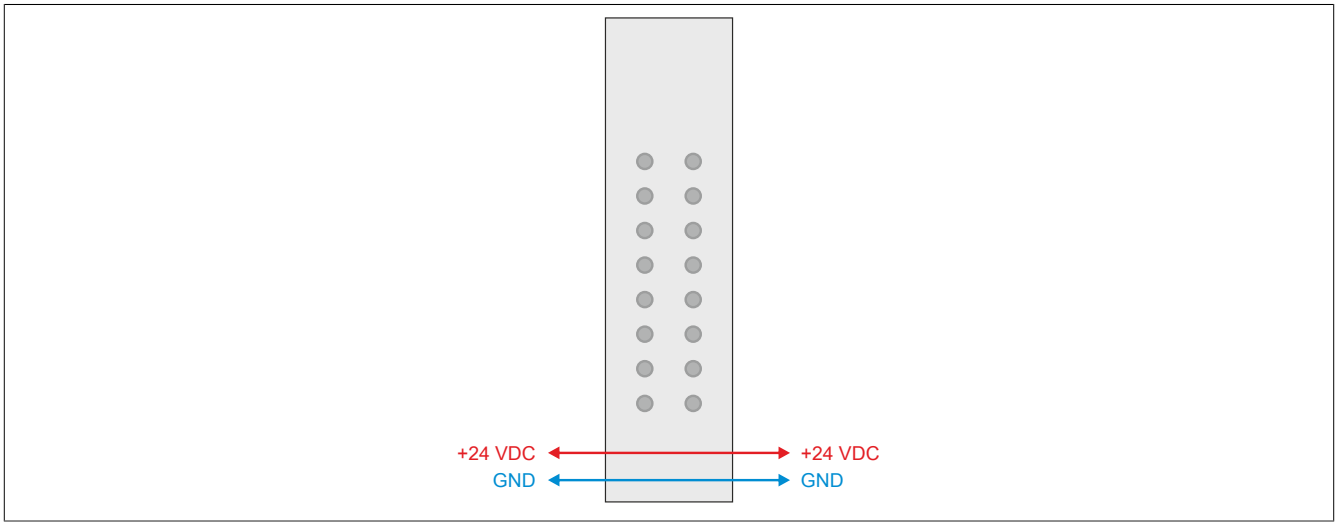
Table 384: X20ZF000F - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.17.4.4 Pinout



4.17.4.5 Connection example



4.18 X20 electronics module communication

The CS modules allow complex devices to be remotely connected to the X20 system via a serial interface.

4.18.1 Brief information

Product ID	Short description	on page
X20CS1011	X20 interface module, 1 Moeller SmartWire interface	1875
X20CS1012	X20 interface module, 1 M-Bus master interface, integrated slave supply	1890
X20CS1013	X20 interface module, 1x DALI master	1938
X20CS1020	X20 interface module, 1 RS232 interface, max. 115.2 kbit/s	1949
X20CS1030	X20 interface module, 1 RS422/485 interface, max. 115.2 kbit/s	1992
X20CS1070	X20 interface module, 1x CAN, max. 1 Mbit/s, object buffer in transmit and receive direction	2035
X20CS2770	X20 interface module, 2x CAN, max. 1 Mbit/s, object buffer in transmit and receive direction	2079
X20cCS1020	X20 interface module, coated, 1 RS232 interface, max. 115.2 kbit/s	1949
X20cCS1030	X20 interface module, coated, 1 RS422/485 interface, max. 115.2 kbit/s	1992

4.18.2 X20CS1011

4.18.2.1 General information

SmartWire from the company Moeller makes it possible to very easily integrate switching devices such as contactors or motor protection switches in the X20 system without extensive wiring. It replaces the control circuit wiring between the controller and switching devices with pluggable, pre-assembled connection cables.

Although SmartWire is an intelligent connection, this changes almost nothing for the machine programmer. Integration in the X20 system via the interface module cuts down on overall communication. The individual switching devices can simply be viewed as digital inputs and outputs.

Practical applications

SmartWire allows up to 16 switching devices to be connected using pre-assembled cables and attached to the X20 SmartWire interface module. The system can configure itself completely at the push of a button without additional intervention or effort. This replaces the wiring test that was previously necessary.

At the same time, the device configuration is known to the system. If a device is no longer available due to an error or intervention, it will be detected immediately. Once corrected, the system continues to run.

The interface module is designed as a normal electronic module, which means it can be placed anywhere on the remote backplane.

- X2X SmartWire master for controlling up to 16 SmartWire slaves
- Simple connection using pre-assembled connection cables
- Moeller SmartWire modules for Moeller standard switching devices
- Replaces control circuit wiring
- Contactor activation
- Contactor switching status
- Motor circuit breaker status
- 24 VDC control voltage via SmartWire connection cable

4.18.2.2 Order data

Model number	Short description	Figure
	X20 electronics module communication	
X20CS1011	X20 interface module, 1 Moeller SmartWire interface	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Undefined	
X20CA4S00.0005	SmartWire attachement cable, X20TB12 to SmartWire connector, 0.5 m	
X20CA4S00.0015	SmartWire attachement cable, X20TB12 to SmartWire connector, 1.5 m	

Table 385: X20CS1011 - Order data

4.18.2.3 Technical data

Product ID	X20CS1011
Short description	
Communication module	1 SmartWire master for controlling up to 16 slaves
General information	
B&R ID code	0xA38D
Status indicators	SmartWire bus function, external supply voltage, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
SmartWire operating state	Yes, using status LED and software
U Aux	Yes, using status LED
Power output	
Internal I/O	6.8 W for supplying external slaves (equal to 16 slaves each with 0.425 W)
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
SmartWire bus - X2X Link	Yes
SmartWire supply (17 VDC) - I/O supply	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Interface	
Type	SmartWire (LIN bus)
Design	Connection made using 12-pin X20TB12 terminal block
Transfer rate	19200 bit/s
SmartWire	
Data format	1 start bit, 8 data bits, no parity bit, 1 stop bit
Max. distance	4 m
Configuration button	
Internal	Integrated in the module on the bottom of the housing.
External	Connection via 12-pin terminal block N.O. contact, not electrically isolated (use potential-free contact)
SWIRE terminal 1 (24 VDC)	
Voltage drop for reverse polarity protection at 3 A	Max. 0.1 VDC
Voltage range	Voltage and supply
Current load	Max. 3 A
Short circuit protection	No, only with external fuse
Monitoring	20 VDC < 24 VDC Aux < 29.4 VDC (via firmware)
SWIRE terminal 2	
Daisy chain signal	5 VDC, CMOS level
SWIRE terminal 5 (bus level)	
Dominant	<2 VDC
Recessive	>14.85 VDC
SWIRE terminal 6 (17 VDC)	
Voltage range	Typ. 16.6 VDC (16.3 VDC to 16.8 VDC)
Summation current	Max. 400 mA for 16 SmartWire slaves
Short circuit protection	Yes
Monitoring	14.2 VDC < 17 VDC Aux < 17.9 VDC (via firmware)
U-Aux (24 VDC aux supply)	
Connection	Externally via 12-pin terminal block [2)]
Input voltage	24 VDC -15 % / +20 %
Fuse	Recommended line fuse: 3 A, slow-blow
Summation current	Max. 3 A for 16 SmartWire slaves
Reverse polarity protection	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20

Table 386: X20CS1011 - Technical data

Product ID	X20CS1011
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order SmartWire attachment cable X20CA4S00.00xx separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 386: X20CS1011 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Using an external feed makes it possible to shut down via E-stop or switching relay

4.18.2.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel
	e + r	Red on / Green single flash		Invalid firmware
	S + R	Green		The "S" and "R" LEDs indicate the status of the SmartWire interface.
	A	Green	Off	U-Aux supply missing or too low
			On	U-Aux supply OK

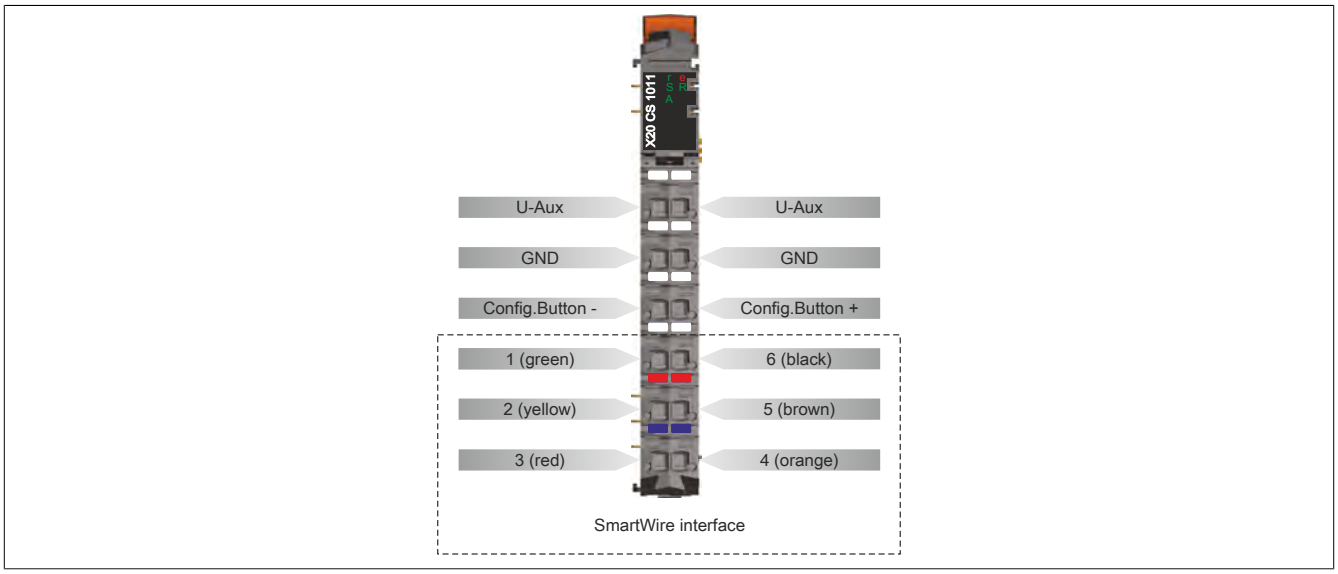
1) Depending on the configuration, a firmware update can take up to several minutes.

"S" and "R" LEDs

The status of the SmartWire interface is indicated by the "S" and "R" LEDs.

S	R	Firmware status	Description
Off	Off	CHECK_INT_FRAM	Initialization
		CHECK_LIN_SUPPLY	Wait until 17 VDC bus is OK
		INT_ERROR_STATE	Internal error has occurred (remains)
Off	On	SET_TRANSCEIVER_MODE	Initialization of transceiver
		RESET_UART	Initialization of UART + 10 ms delay
		READ_REVISION_CNT	Initialization (revision counter from FLASH)
Blinking slowly	Blinking slowly	INIT_LIN_SCAN	Initialization for bus scan
		RUN_LIN_SCAN	Perform bus scan
		INIT_LIN_SETUP	Initialization for RUN_LIN_SETUP
		RUN_LIN_SETUP	Perform bus setup
		STORE_REVISION_CNT	Revision counter in FLASH
		WAIT_FOR_PUSHBUTTON	Wait for configuration button after bus scan and difference with existing configuration
Blinking slowly	Blinking quickly	TIME_DELAY	4 s optical confirmation signal after pressing the configuration button
On	Blinking slowly	DP_CFG_CHECK	Check of the configuration by the higher-level CPU (not currently used)
		SET_SLAVES_TO_OP	Switch SmartWire stack to Operational
		SET_SLAVES_TO_PREOP	Switch SmartWire stack to Preoperational
		INIT_LIN_SCHED	Initialization for RUN_LIN_SCHED
		RUN_LIN_SCHED (PREOP)	RUN SmartWire scheduler (in PREOP)
On	On	RUN_LIN_SCHED (OP)	RUN SmartWire scheduler (in OP)
Blinking slowly	On	IDLE_STATE	RUN SmartWire without scheduler (no slaves connected)
Blinking quickly	On	LIN_ERROR_STATE	ERROR LIN-BUS has occurred (remains)

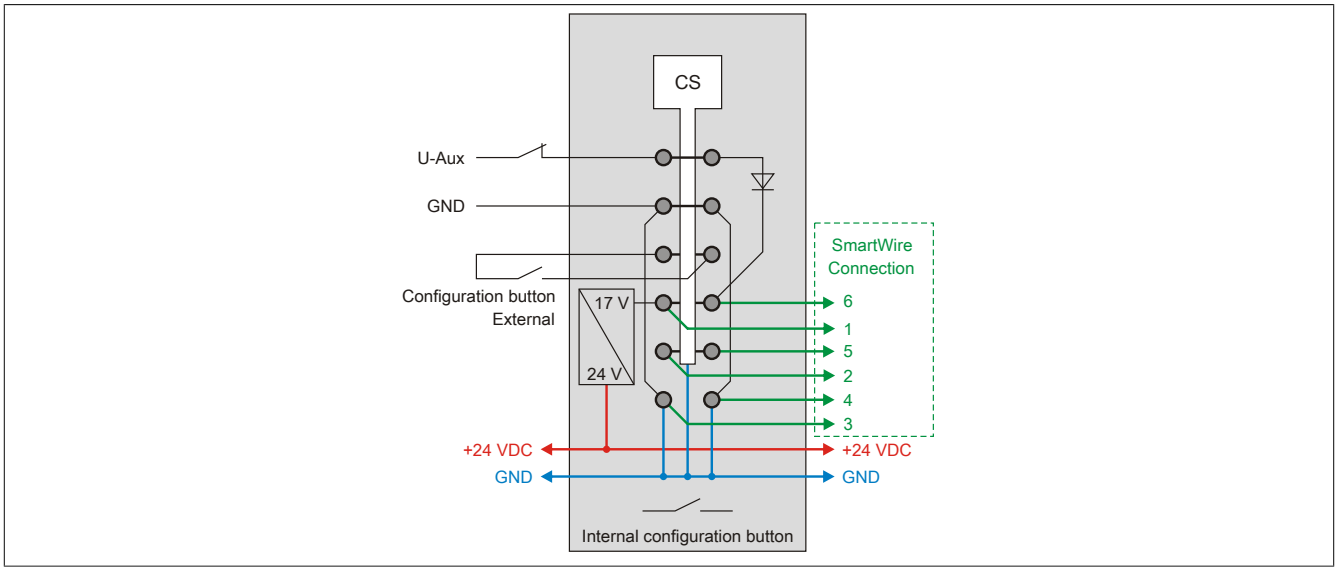
4.18.2.5 Pinout



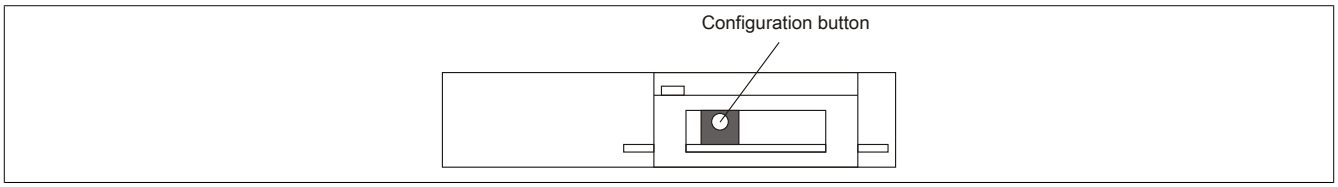
Information:

X20CA4S00.00xx SmartWire cables are delivered with the X20TB12 terminal block fully installed.

4.18.2.6 Connection example



4.18.2.7 Configuration button



A configuration button is integrated on the underside of the interface module housing. It can be used to completely configure the entire system.

After adding or removing SmartWire sensors/actuators, pressing the configuration button rescans the SmartWire bus and saves the new configuration in the X20 SmartWire interface module.

In addition to the internal configuration button, it is also possible to connect an external configuration button to the terminal block.

4.18.2.8 Register description

4.18.2.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.18.2.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
5121	FastOutput01_02	USINT			●	
5123	FastOutput03_04	USINT			●	
...	...					
5133	FastOutput13_14	USINT			●	
5135	FastOutput15_16	USINT			●	
257	SmartWireEnable	USINT				●
259	Smart WireMode	USINT				●
8193 + (N-1) * 32	VendorNCfg (Index N = 1 to 16)	USINT				●
8195 + (N-1) * 32	DeviceNCfg (Index N = 1 to 16)	USINT				●
Communication						
557	MasterOperatingState	USINT	●			
550	MasterStatus	UINT	●			
546	SlaveStatus	UINT	●			
4097 + (N-1) * 32	InputN (Index N = 01 to 16)	USINT	●			
513 + (N-1) * 2	SlaveStatusN (Index N = 01 to 16)	USINT		●		
8193 + (N-1) * 32	VendorN (Index N = 1 to 16)	USINT		●		
8195 + (N-1) * 32	DeviceN (Index N = 1 to 16)	USINT		●		

4.18.2.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
5121	0	FastOutput01_02	USINT			●	
5123	1	FastOutput03_04	USINT			●	
...	...	...					
5133	6	FastOutput13_14	USINT			●	
5135	7	FastOutput15_16	USINT			●	
257	-	SmartWireEnable	USINT				●
259	-	Smart WireMode	USINT				●
8193 + (N-1) * 32	-	VendorNCfg (Index N = 1 to 16)	USINT				●
8195 + (N-1) * 32	-	DeviceNCfg (Index N = 1 to 16)	USINT				●
Communication							
77	-	MasterOperatingState	USINT		●		
70	-	MasterStatus	UINT		●		
66	-	SlaveStatus	UINT		●		
4097 + (N-1) * 32	N - 1	InputN (Index N = 01 to 16)	USINT	●			
513 + (N-1) * 2	-	SlaveStatusN (Index N = 01 to 16)	USINT		●		
8193 + (N-1) * 32	-	VendorN (Index N = 1 to 16)	USINT		●		
8195 + (N-1) * 32	-	DeviceN (Index N = 1 to 16)	USINT		●		

1) The offset specifies the position of the register within the CAN object.

4.18.2.8.3.1 CAN I/O bus controller

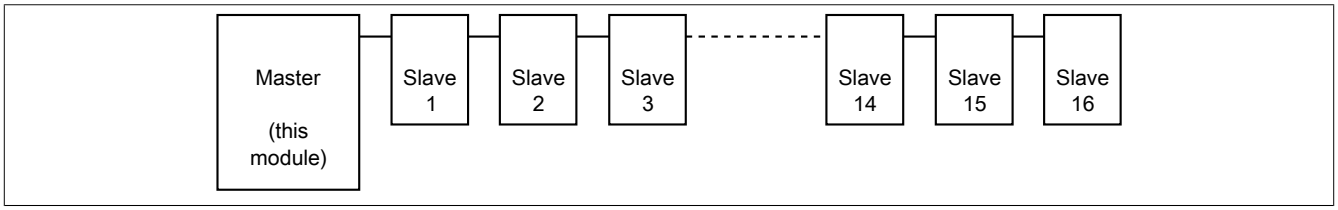
The module occupies 2 analog logical slots on CAN-I/O.

4.18.2.8.4 Communication module Basic Master for SmartWire

SmartWire is essentially a master-slave system.

- All data traffic is initiated by the master, but the system can only contain one master.
- The SmartWire master can control up to 16 SmartWire slaves.
- The total scheduling time is 160 ms (i.e. after 160 ms, all 16 slaves have been queried one time).
- The maximum allowed bus extension is 2.6 m.
- Due to the automatic bus configuration, the numbering of the individual slaves is determined by the line structure of the bus.

This results in the following order:



Node address = Physical position in the bus line

4.18.2.8.5 Functions

4.18.2.8.5.1 Scan SmartWire

Automatically started and run after the system is turned on (default settings).

This procedure terminates if

- the set and actual configuration of the bus are identical: system changes to normal operation (i.e cyclic data exchange)
- or if there is a deviation between the set and actual configuration: error present, cyclic data transfer is not started

4.18.2.8.5.2 Setup SmartWire

Can be activated by pressing the configuration button or using a software command:

- if no configuration is saved
- if a SmartWire scan was just terminated due to error

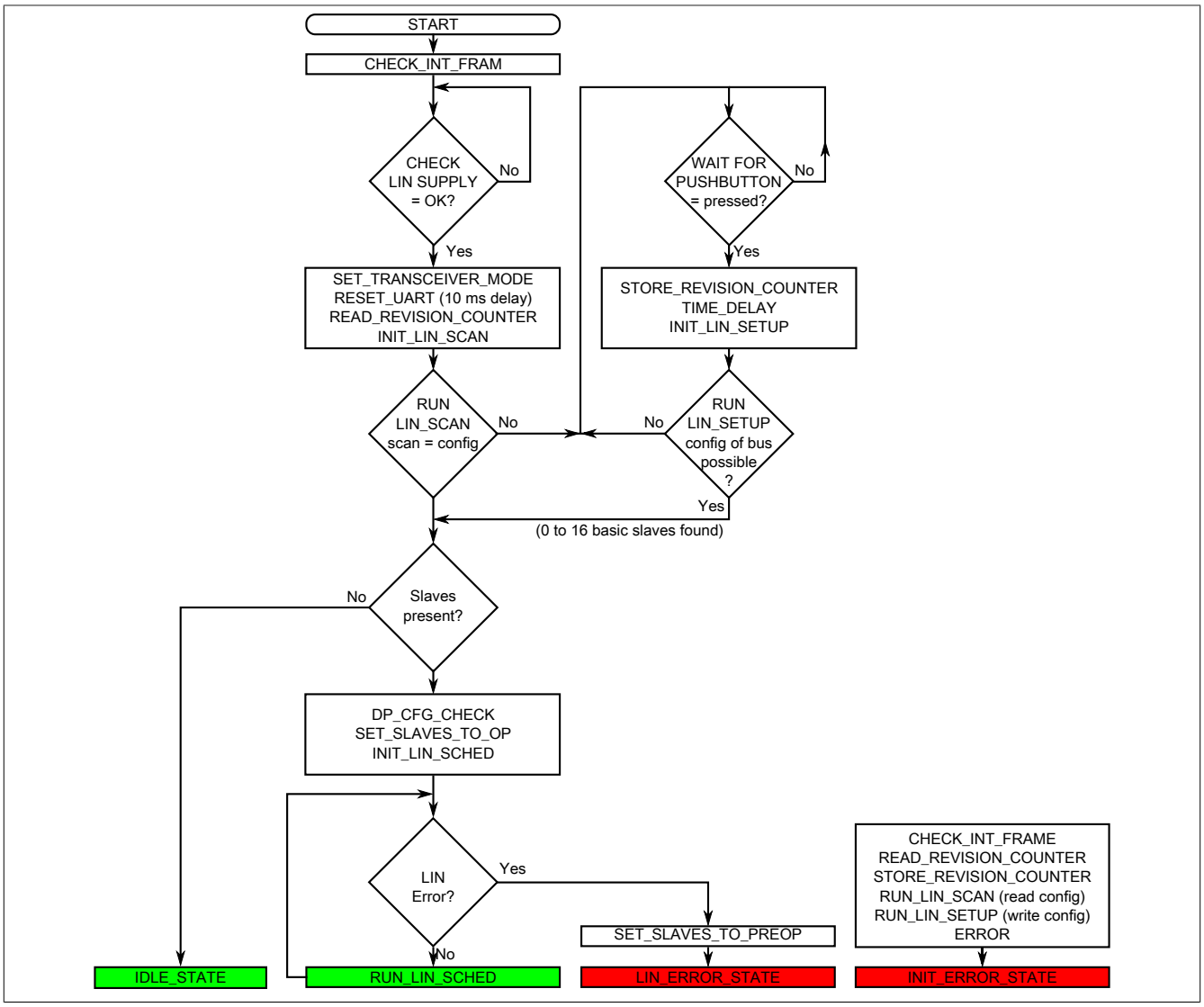
During setup, all connected stations are saved remanently in the master as new set configuration. Valid stations are uniquely identified by the two parameters 4.18.2.8.14.3 "Device ID" and 4.18.2.8.14.2 "Vendor ID".

4.18.2.8.6 Show operating state of the master

The current state of the master state machine is indicated in this register.

Data type	Value	Code	Description
USINT	1	CHECK_INT_FRAM	Init State
	2	CHECK_LIN_SUPPLY	Waiting for 17 V voltage OK
	3	SET_TRANSCEIVER_MODE	Turn on transceiver
	4	RESET_UART UART	Reset
	6	INIT_LIN_SCAN	Init before bus scan
	7	RUN_LIN_SCAN	Bus scan is running
	8	WAIT_FOR_PUSHBUTTON	Scan != Configuration, waiting for Config button
	9	TIME_DELAY	Delay before bus setup
	10	INIT_LIN_SETUP	Init before bus setup
	11	RUN_LIN_SETUP	Bus setup is running (new configuration)
	12	DP_CFG_CHECK	PLC has set "Wait for configuration"
	15	SET_SLAVES_TO_OP	Sets slaves to OP mode (after successful scan or setup)
	16	SET_SLAVES_TO_PREOP	Sets slaves to PREOP mode (after errors have occurred, before LIN_ERROR or INT_ERROR)
	19	INIT_LIN_SCHED	Init bus scheduling
	20	RUN_LIN_SCHED	Bus scheduler is running
	21	LIN_ERROR_STATE	A fatal bus error has occurred (permanent)
	22	INT_ERROR_STATE	A fatal internal error has occurred (permanent)
	23	IDLE_STATE	Idle because there is no slave connected (permanent)

4.18.2.8.6.1 Flow chart of SmartWire master operating status



The register receives the following value after successfully starting:

Value	Code	Description
20	RUN_LIN_SCHED	Bus scheduler is running

4.18.2.8.7 Status of the master

Name:
MasterStatus

The current status information for the master is shown in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	LIN_BUS_SETUP_COMPLETE	0	Saved configuration does not match the actual hardware on the bus
		1	Setup finished: SCAN or SETUP after config button is valid
1	LIN_FATAL_ERROR	0	No error on the bus
		1	SmartWire bus is defective: e.g. short circuit, no echo → more than 10 consecutive communication errors have occurred. **Information:** **The failure of a slave is not a communication error. Instead it is indicated in the slave status and the scheduler continues to run!**
2	LIN_MASTER_PREOP	0	SmartWire stack not in PREOP mode
		1	SmartWire stack in PREOP mode
3	LIN_MASTER_OP	0	SmartWire stack not in OP mode
		1	SmartWire stack in OP mode
4	LIN_GLOBAL_CONTROL	0	No command sent
		1	Set SmartWire stack to OP mode: Bit is written to the enable bit and can be read back
5	Reserved	0	
6	LIN_POWER_SUPPLY_STATE	0	Bus voltage supply is not OK
		1	Bus voltage supply is OK
7	Reserved	0	
8	DP_CHECK_COMPLETED	0	Not a valid configuration
		1	Configuration check completed (Not Used) (could optionally be written by the PLC, if the SCAN (configuration) is OK and was able to be read back from here)
9	Reserved	0	
10	DP_RECONFIGURATION	0	X2X Reconfiguration → X2X configuration button not pressed
		1	X2X Reconfiguration → X2X configuration button can be read back
11 - 15	Reserved	0	

The register receives the following value after successfully starting:

Equal to the decimal value: 345

Bit	Description	Value	Information
0	LIN_BUS_SETUP_COMPLETE	1	SmartWire setup complete: SCAN or SETUP after config button is valid
3	LIN_MASTER_OP	1	SmartWire stack in OP mode
4	LIN_GLOBAL_CONTROL	1	Set SmartWire stack to OP mode - Command set
6	LIN_POWER_SUPPLY_STATE	1	Bus voltage supply is OK
7	DP_CHECK_COMPLETED	1	Configuration is Ok

4.18.2.8.8 Status of all slaves

Name:
SlaveStatus

The current state of the slave is indicated collectively in this register.

In the event of an error, the failed slaves are indicated in the respective bits, and in the status registers individually set up for the slaves (see 4.18.2.8.14.1 "SlaveStatus1 to SlaveStatus16").

Data is exchanged cyclically as long as none of these bits are set. If an error does error, then I/O transfer is stopped. The bus can be started again after the error has been corrected or a setup has been performed again (see 4.18.2.8.13 "Basic application registers "SmartWireEnable" and "SmartWireMode"").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Slave 1	0	Ok
		1	Errors
...		...	
15	Slave 16	0	Ok
		1	Errors

4.18.2.8.9 Transfer control bits to slaves

Name:
FastOutput01_02 to FastOutput15_16

In these registers, the control bits are transferred to 2 consecutive slaves. Each slave receives 4 control bits, that must be selected from the 8 data bytes depending on the node address (1 to 16). These 4 control bits are assigned fixed values and utilization of the bits by the slave is optional.

All of the slaves evaluate this telegram. It must be sent cyclically by the master so that the slaves can ensure that the master is still functioning without any problems within the monitoring time (lifeguarding time = 400 ms).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Slave N	0	Digital output 1 reset
		1	Digital output 1 set
...		..	
3	Slave N	0	Digital output 4 reset
		1	Digital output 4 set
4	Slave N + 1	0	Digital output 1 reset
		1	Digital output 1 set
...		..	
7	Slave N + 1	0	Digital output 4 reset
		1	Digital output 4 set

4.18.2.8.10 Read input data from slave

Name:
Input01 to Input16

Each slave sends its input data and/or its status to the master.

The data volume consumes 1 byte per slave. Each slave has one diagnostics bit, which it sends to the master with the cyclic data. This bit is a message bit if an application error occurs (on the module). It is always located in the highest value bit.

The master can constantly evaluate this bit. The diagnostic bit is set on the slave if the status of the slave is "Error". Slaves that do not have any input data will still send a byte that is used to make their status data available. This is required because the master also monitors the slaves for proper functionality through the receipt of this byte.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Input state - Digital input 1	0 or 1	
...		...	
3	Input state - Digital input 4	0 or 1	
4 - 6	Reserved	0	
7	Error status	0	No error on the slave
		1	Error on the slave

4.18.2.8.11 Configure the function breakpoints on the master

Name:
SmartWireEnable

This register can be used to configure function breakpoints that may be implemented in master state machine.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Enable SmartWire stack	0	Disabled
		1	Enabled
1	Set SmartWire stack mode	0	Sets PREOP mode (scheduler is already running, output data will still be output with 0)
		1	Sets OP mode
2	Reserved	0	
3	Software "Config button"	0	Not pressed
		1	Pressed (necessary so that slaves can also be reconfigured)
4 - 7	Reserved	0	

4.18.2.8.12 Configure the operating mode of the master

Name:
SmartWireMode

This register can be used to configure the master operating mode.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Operating mode	00	CONFIG from RAM (controller)
		01	Read CONFIG from flash (default)
		10	Write CONFIG to flash
		11	Reserved
2 - 7	Reserved	0	

4.18.2.8.13 Basic application registers "SmartWireEnable" and "SmartWireMode"

By default, the SmartWire bus is started automatically and must at least be configured using an external method (e.g. external button or push-button).

If sensors / actuators are added to or removed from the SmartWire bus, then the configuration procedure must be restarted so that the SmartWire bus will be rescanned and the new configuration saved remanently in the master.

These registers can and must be used for special conditions and for acknowledging errors.

The library commands are sent asynchronously via X2X Link. The following conditions could cause errors on the module and are therefore not permitted:

- The command register SmartWireMode is written to first. It is possible to write to the SmartWireEnable register once the function block reports that it is finished.
- The function block status response is checked in the application
- The specified response from the master status information must arrive in order for the master state machine to function properly

4.18.2.8.13.1 Starting the bus when Manual Start has been configured

Status information after startup:

Value (decimal)	Register	Information
1	MasterOperatingState	Init State
0	MasterStatus	
0	SlaveStatus	

If Manual start is selected for the bus in the configuration, then the AsIOAccWrite() function from the AsIOAcc library must be used to write to the two registers in the specified order.

Value (decimal)	Register	Information
1	SmartWireMode	Configuration from rem. memory
3	SmartWireEnable	Command for STACK ON / OPERATIONAL

Status information after error-free startup of the bus:

Value (decimal)	Register	Information
20	MasterOperatingState	"RUN without error if SlaveStatus = 0"
345	MasterStatus	"RUN without error if SlaveStatus = 0"
0	SlaveStatus	No slave errors

4.18.2.8.13.2 Starting the bus after slave error

Status information after slave error

In this case, a change to MasterOperatingState and MasterStatus cannot be detected at first, although the respective error bits are set in the SlaveStatus. The slaves have failed, and data is no longer being exchanged.

Value (decimal)	Register	Information
20	MasterOperatingState	
345	MasterStatus	
x	SlaveStatus	Bits for the faulty slaves have been set

To set the master to a defined state, the bus must first be stopped with the following write commands.

Value (decimal)	Register	Information
0	SmartWireMode	All off
0	SmartWireEnable	All off

Wait until the commands have been completed successfully, which is indicated in the MasterStatus. Bit 4 is cleared: Response indicating that the bus is no longer operational.

Value (decimal)	Register	Information
20	MasterOperatingState	
329	MasterStatus	
0	SlaveStatus	

The bus can be restarted using the write commands after the errors have been corrected:

Value (decimal)	Register	Information
1	SmartWireMode	Configuration from rem. memory
3	SmartWireEnable	Command for STACK ON / OPERATIONAL

Status information after error-free startup of the bus:

Value (decimal)	Register	Information
20	MasterOperatingState	"RUN without error if SlaveStatus = 0"
345	MasterStatus	"RUN without error if SlaveStatus = 0"
0	SlaveStatus	No slave errors

Different status information can result depending on the present error situation (see 4.18.2.8.6 "MasterOperatingState").

Typical situation when there are hardware configuration differences:

Value (decimal)	Register	Information
0	MasterOperatingState	
80	MasterStatus	
0	SlaveStatus	

Information:

A stop command must be sent before a new start command can be applied!

4.18.2.8.14 Advanced applications

The following registers are used for advanced diagnostics, for reading back the current configuration and for creating a configuration from the application. The registers that have already been written and their respective contents are, of course, valid.

4.18.2.8.14.1 Status of the individual slaves

Name:
SlaveStatus1 to SlaveStatus16

These registers display the respective slave status.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0		0	Slave integrated on the bus
		1	Slave failure on the bus
1 - 7	Reserved	0	

4.18.2.8.14.2 Read slave vendor ID

Name:
Vendor1 to Vendor16

These registers display the respective slave Vendor ID.

Data type	Value	Information
USINT	x	Slave vendor ID

4.18.2.8.14.3 Read slave device ID

Name:
Device1 to Device16

These registers display the respective slave device ID.

Data type	Value	Information
USINT	x	Slave device ID

4.18.2.8.14.4 Write slave vendor ID

Name:
Vendor1Cfg to Vendor16Cfg

The desired vendor ID for the slave can be written in these registers.

Data type	Value	Information
USINT	x	Slave vendor ID

4.18.2.8.14.5 Write slave device ID

Name:
Device1Cfg to Device16Cfg

The desired device ID for the slave can be written in these registers.

Data type	Value	Information
USINT	x	Slave device ID

Import the configuration without starting the bus

For safety reasons, it is possible to import the configuration for the connected bus without starting cyclic data transfer. This actual configuration can be compared with the set configuration stored in the application. Cyclic data transfer can be started if the configurations are the same. An error is reported if they are not the same.

Manual start is configured, status information after startup:

Value (decimal)	Register	Information
1	MasterOperatingState	Init State
0	MasterStatus	
0	SlaveStatus	

The function AsIOAccWrite() from the library AsIOAcc must be used to write the two registers in the specified order.

Value (decimal)	Register	Information
0	SmartWireMode	RAM memory configuration
9	SmartWireEnable	Command for STACK ON / PREOPERATIONAL and CONFIG-BUTTON

Status information after error-free import of the bus configuration:

Value (decimal)	Register	Information
20	MasterOperatingState	"RUN without error if SlaveStatus = 0"
1349	MasterStatus	"PREOP and no errors"
0	SlaveStatus	No slave errors

Once these commands have been completed, the connected slave modules are imported and stored in the remanent memory for subsequent startups.

The function AsIOAccRead() from the library AsIOAcc must now be used to read all corresponding registers Vendor1 to Vendor16 and Device1 to Device 16 . If the configuration matches, then the bus can now be started using the standard command:

Value (decimal)	Register	Information
1	SmartWireMode	Configuration from rem. memory
3	SmartWireEnable	Command for STACK ON / OPERATIONAL

Status information after error-free startup of the bus:

Value (decimal)	Register	Information
20	MasterOperatingState	"RUN without error if SlaveStatus = 0"
345	MasterStatus	"RUN without error if SlaveStatus = 0"
0	SlaveStatus	No slave errors

Bus configuration settings

Manual start is configured, status information after startup:

Value (decimal)	Register	Information
1	MasterOperatingState	Init State
0	MasterStatus	
0	SlaveStatus	

A running bus can, of course, also be stopped with the standard command and re-configured!

The function AsIOAccWrite() from the library AsIOAcc must now be used to write the respective data to all registers Vendor1Cfg to Vendor16Cfg and Device1Cfg to Device16Cfg. All vendor and device registers that are not being used must be set to zero. This does not cause a change in the status registers.

To save the data in remanent memory, the function AsIOAccWrite() from the library AsIOAcc must be used to write to the two registers in the specified order.

Value (decimal)	Register	Information
2	SmartWireMode	WRITE rem. memory configuration
1	SmartWireEnable	Command for STACK ON / OPERATIONAL

Status information after error-free configuration:

Value (decimal)	Register	Information
20	MasterOperatingState	"RUN without error if SlaveStatus = 0"
325	MasterStatus	"PREOP without errors"
0	SlaveStatus	No slave errors

The bus can now be started using the standard command for the bus:

Value (decimal)	Register	Information
1	SmartWireMode	Configuration from rem. memory
3	SmartWireEnable	Command for STACK ON / OPERATIONAL

Status information after error-free startup of the bus:

Value (decimal)	Register	Information
20	MasterOperatingState	"RUN without error if SlaveStatus = 0"
345	MasterStatus	"RUN without error if SlaveStatus = 0"
0	SlaveStatus	No slave errors

4.18.2.8.15 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.18.3 X20CS1012

4.18.3.1 General information

The X20 system is now being expanded to include a new M-Bus master communication slice. This single-width module can be placed anywhere in an X20 I/O system and can therefore be used as a decentralized solution in distributed topologies. The M-Bus master supports transfer rates of 300, 2400 and 9600 Bit/s and up to 64 slaves can be connected and supplied via the M-Bus.

The M-Bus (meter bus) is a relatively simple fieldbus for collecting consumption data, such as from electricity or heat meters. It is based on reverse polarity proof two-wire connections and uses the master-slave principle.

- Supply for up to 64 slaves on the M-Bus
- Decentralized use of the communication interface

4.18.3.2 Order data

Model number	Short description	Figure
	X20 electronics module communication	
X20CS1012	X20 interface module, 1 M-Bus master interface, integrated slave supply	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 387: X20CS1012 - Order data

4.18.3.3 Technical data

Product ID	X20CS1012
Short description	
Communication module	1 M-Bus master for controlling up to 64 slaves
General information	
B&R ID code	0xCABF
Status indicators	Data transfer, M-Bus supply, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Data transfer	Yes, using status LED
M-Bus supply	Yes, using status LED and software
Power consumption	
Bus	0.2 W
Internal I/O	0.35 W + (number of slaves * 0.08 W)
Module power dissipation	0.55 W + (number of slaves * 0.006 W)
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
M-Bus - X2X Link	Yes
M-Bus - I/O supply	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1]	Yes
GOST-R	Yes
Isolation voltage between M-Bus and X2X Link	500 VDC, 1 min
Interfaces	
Interface	
Type	M-Bus master
Design	Connection made using 12-pin X20TB12 terminal block
Transfer rate	300, 2400 or 9600 bit/s
Max. distance	See section "M-Bus"
Number of slaves	Max. 64
Internal resistance of the master	Max. 6 Ω
Bus voltage mark at 0 mA	I/O supply voltage (+ 11.5 to 13.5 V)
Bus voltage drop with space	12 to 13.5 V
Overload cutoff	250 mA ±10%
Bit threshold	6 to 9 mA
Collision threshold	24 to 36 mA
Received readjustment time	Max. 10 s [2]
Bus cable	Shielded or unshielded
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 388: X20CS1012 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Dependent on the changes to the load on the M-Bus (e.g. switching slaves on and off)

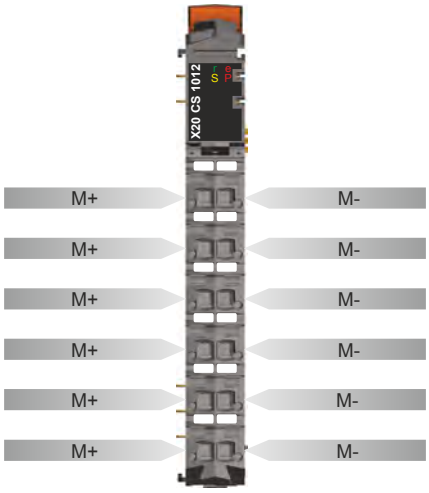
4.18.3.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

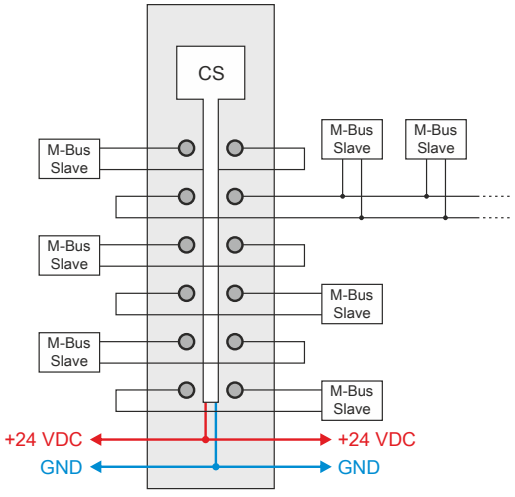
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	S	Yellow	Off	No slaves sending data
			On	At least one slave is sending data via the M-Bus
	P	Red	Off	M-Bus supply ok
			On	Short-circuit or overload on M-Bus

1) Depending on the configuration, a firmware update can take up to several minutes.

4.18.3.5 Pinout



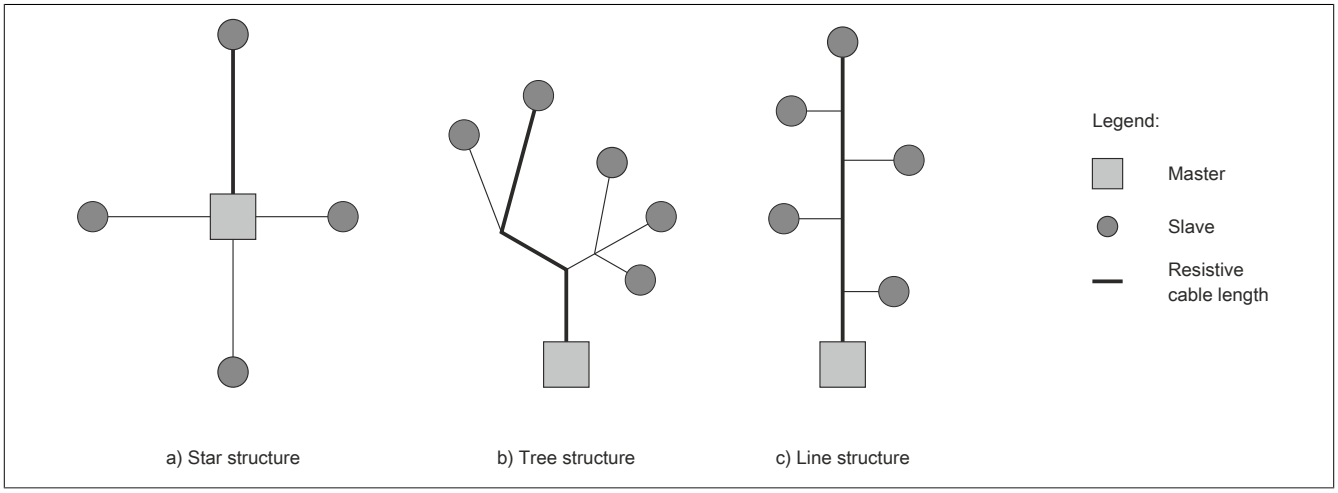
4.18.3.6 Connection example



4.18.3.7 M-Bus

4.18.3.7.1 Bus topology

The bus topology has a significant influence on the maximum load of an M-Bus network. In general a star structure is preferred over a tree structure and in turn a tree structure is preferred over a line structure. Furthermore, connecting the slaves to the bus the same way provides better values than connecting them all at the end of the branches after all other parameters have been determined.



4.18.3.7.2 Cable cross section

The cable being used has a specific capacity and resistance, which in turn has an effect on the operation of the bus. The resistive influence of the cable means a loss of voltage on the line, which is subsequently not available for supplying the bus. In order to guarantee sufficient power, the voltage on the slaves must never be less than 12 V neither when sending from the master to the slave, nor in the opposite direction. The deciding factor in this case is the longest branch of the network whose length is referred to as the resistive cable length.

The cable's capacity causes signal distortion during data transfer because the slew rates of the rising and falling edges are slowed down. For example, replacing a 3 km branch in a network with two 1.5 km branches will improve the signal. The total distance of the network is referred to as the capacitive cable length (the sum of all segment lengths).

Information:

The maximum permissible line resistance (for the longest loop) is 250 Ω.

The maximum permissible line capacitance for the entire bus is 500 nF.

4.18.3.7.3 Transmission current and bit threshold

The bit threshold on the master is typically 7.5 mA. Therefore, a slave transmission current of 15 mA results in the least amount of signal distortion while the highest amount occurs at 11 or 20 mA.

4.18.3.7.4 Transfer rate

A lower transfer rate decreases the influence of the signal distortion caused by cable capacity and bit threshold.

Information:

Starting with a total bus length >1 km, the slaves must be operated at a baud rate <9600 bit/s.

4.18.3.7.5 Calculating the resistive bus length

The resistive cable length must be calculated in order to ensure a sufficient power supply of 12 V on the M-Bus. What matters most here is the longest segment between the master and slave.

The resistive bus length is calculated using the following formula without taking an increased bus current caused by a defective receiver into account:

$$L_{res} = \frac{V_{I/O} - (n * 0.0015 + 0.02) * 6 - 12.6}{(n * 0.0015 + 0.02) * R_L} * 1000$$

L_{res} ... Resistive bus length [m]
n ... Number of slaves (all at end of line)
R_L ... Line resistance (loop resistance [Ω/km])
$V_{I/O}$ ... I/O supply voltage [V]

Examples for calculating the maximum resistive bus length:

No.	Example	Maximum resistive bus length
1	• 64 slaves (all at end of line) • 19.2 V I/O supply voltage • 0.5 mm² wire cross-section	675 m
2	• 64 slaves (all at end of line) • 28.8 V I/O supply voltage • 1.5 mm² wire cross-section	5340 m

4.18.3.7.6 Accounting for the capacitive bus length

The total distance of the network is referred to as the capacitive bus length (the sum of all segment lengths). The capacitive bus length depends on two factors:

- Distributed capacitance of cable
- Transfer rate

Distributed capacitance of cable

A lower distributed capacitance on a cable means a higher capacitive bus length.

Transfer rate

A lower transfer rate on an M-Bus system means a higher capacitive bus length.

Example of a cable with a distributed capacitance of 50 nF/km:

Transfer rate	Capacitive bus length
9600 bit/s	1 km
2400 bit/s	4 km
300 bit/s	10 km

4.18.3.7.7 Bus installation

Cables with twisted pair wires and a cross-section of 0.5 mm² to 1.5 mm² are normally used for bus installation (according to standard: J-Y(ST)Y nx2x0.8). The shield on shielded cables only has to be grounded to the module on one side. On the slaves, the shielding must be high resistance for DC and low frequency signals.

4.18.3.7.8 Repeater

Repeaters can be used to further expand the M-Bus network.

4.18.3.8 Register description

4.18.3.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.18.3.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Module configuration						
774	CfO_FunctionModel	UINT				•
M-Bus - Configuration						
Index * 16 + 767	CfO_LengthData1 to CfO_LengthData8	USINT				•
Index * 16 + 775	CfO_BaudData1 to CfO_BaudData8	USINT				•
Index * 16 + 761	CfO_PAdrData1 to CfO_PAdrData8	USINT				•
Index * 16 + 765	CfO_IndexData1 to CfO_IndexData8	USINT				•
Index * 16 + 773	CfO_ReqTimeData1 to CfO_ReqTimeData8	USINT				•
Index * 16 + 770	CfO_MBusModeData1 to CfO_MBusModeData8	UINT				•
Index * 16 + 763	CfO_ToutOffData1 to CfO_ToutOffData8	USINT				•
Index * 8 + 1009	CfO_ReplData1 to CfO_ReplData8	(U)SINT				•
Index * 8 + 1010	CfO_ReplData1 to CfO_ReplData8	(U)INT				•
Index * 8 + 1012	CfO_ReplData1 to CfO_ReplData8	(U)DINT REAL				•
M-Bus - Communication						
513	MBusCommand	USINT			•	•
263	MBusOperation	USINT	•			
257	MBusState	USINT	•			
259	ValidDataByte	USINT	•			
	ValidData1	Bit 0	•			
	...	...	•			
	ValidData8	Bit 7	•			
261	InvalidDataByte	USINT	•			
	InvalidData1	Bit 0	•			
	...	...	•			
	InvalidData8	Bit 7	•			
Index * 8 + 265	Data1 to Data8	(U)SINT	•			
Index * 8 + 266	Data1 to Data8	(U)INT	•			
Index * 8 + 268	Data1 to Data8	(U)DINT REAL	•			
337	ChangedSNByte	USINT	•			
Index * 8 + 900	SNData1 to SNData8	UDINT		•		
FlatStream						
2051	InputMTU	USINT				•
2049	OutputMTU	USINT				•
2113	InputSequence	USINT	•			
Index * 2 + 2113	RxByte1 to RxByte15	USINT	•			
2177	OutputSequence	USINT			•	
Index * 2 + 2177	TxByte1 to TxByte15	USINT			•	
2053	FlatstreamMode	USINT				•
2055	Forward	USINT				•
2057	ForwardDelay	UINT				•

4.18.3.8.3 Function model 254 - Bus controller

Register	Offset [1]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Module configuration							
774	-	CfO_FunctionModel	UINT				●
M-Bus - Configuration							
Index * 16 + 767	-	CfO_LengthData1 to CfO_LengthData8	USINT				●
Index * 16 + 775	-	CfO_BaudData1 to CfO_BaudData8	USINT				●
Index * 16 + 761	-	CfO_PAdrData1 to CfO_PAdrData8	USINT				●
Index * 16 + 765	-	CfO_IndexData1 to CfO_IndexData8	USINT				●
Index * 16 + 773	-	CfO_ReqTimeData1 to CfO_ReqTimeData8	USINT				●
Index * 16 + 770	-	CfO_MBusModeData1 to CfO_MBusMode-Data8	UINT				●
Index * 16 + 763	-	CfO_ToutOffData1 to CfO_ToutOffData8	USINT				●
Index * 8 + 1009	-	CfO_ReplData1 to CfO_ReplData8	(U)SINT				●
Index * 8 + 1010	-	CfO_ReplData1 to CfO_ReplData8	(U)INT				●
Index * 8 + 1012	-	CfO_ReplData1 to CfO_ReplData8	(U)DINT REAL				●
M-Bus - Communication							
8	8	MBusCommand	USINT			●	●
11	11	MBusOperation	USINT	●			
8	8	MBusState	USINT	●			
9	9	ValidDataByte	USINT	●			
10	10	InvalidDataByte	USINT	●			
Index * 4 + 5	Index * 4 + 8	Data1 to Data8	(U)SINT	●			
Index * 4 + 6	Index * 4 + 8	Data1 to Data8	(U)INT	●			
Index * 4 + 8	Index * 4 + 8	Data1 to Data8	(U)DINT REAL	●			
337	-	ChangedSNByte	USINT		●		
Index * 8 + 900	-	SNData1 to SNData8	UDINT		●		
FlatStream							
2051	-	InputMTU	USINT				●
2049	-	OutputMTU	USINT				●
0	0	InputSequence	USINT	●			
Index * 1 + 0	Index * 1 + 0	RxByte1 to RxByte7	USINT	●			
0	0	OutputSequence	USINT			●	
Index * 1 + 0	Index * 1 + 0	TxByte1 to TxByte7	USINT			●	
2053	-	FlatstreamMode	USINT				●
2055	-	Forward	USINT				●
2057	-	ForwardDelay	UINT				●

1) The offset specifies the position of the register within the CAN object.

4.18.3.8.3.1 CAN I/O bus controller

The module occupies 3 analog logical slots on CAN-I/O.

4.18.3.8.4 General information

The M-Bus standard is a serial bus system that handles half-duplex or asynchronous communication. The high level of variability provided by this protocol enables a wide range of information to be handled via the same interface. In basic M-Bus networks, the master communicates with up to 250 slaves via the "primary address". In later stages of development, the secondary address (4 bytes) was then also specified. This made it possible to significantly increase the number of slaves in a network.

Important information about the module

- Generally: Primary address used (1 to 250)
- Secondary address only supported via FlatStream
- Bus can supply 64 slaves with power

4.18.3.8.5 Module configuration

The flexible design of the M-Bus protocol can quickly add up to a lot of configuration work. That's why B&R offers two different user interfaces for the module: "Standard" and "FlatStream". The user-friendly B&R Standard interface allows users to view up to eight values requested cyclically from the M-Bus network. In FlatStream mode, the module acts as a bridge between the PLC and the M-Bus slave, which makes all M-Bus functions available.

Information:

The B&R Standard interface is statically configured and based on cyclic registers. Because X2X Link can only transfer a certain number of values cyclically, the user must make his selection accordingly.

4.18.3.8.5.1 Settings for operation

Name:
CfO_FunctionModel

This register can be used to enable either the Standard or FlatStream interface, which makes the module much more efficient.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	B&R Standard Interface	0	Disabled
		1	Enabled
1	FlatStream	0	Disabled
		1	Enabled
3 - 7	Reserved	0	

4.18.3.8.6 M-Bus - Configuration

Separate configuration registers are provided for each value to read. These must be configured correctly in order to call up a counter value from the M-Bus network. The user must know the following values from the slave:

- Transfer rate configured on the slave
- Primary address configured on the slave (value: 1 to 250, otherwise only point-to-point connection is possible)
- Data type / data length of value
- How the slave's memory is structured

Information:

The following section "M-Bus - Configuration" is based solely on the B&R Standard interface.

4.18.3.8.6.1 Data length

Name:
CfO_LengthData1 to CfO_LengthData8

The Standard interface is able to request data from the M-Bus slave with different lengths. When using Automation Studio the value of the "Length" register is a result of the data type defined for the X2X Link. All common data types with up to 4 bytes in length are supported.

Data type	Value
USINT	0 to 7

Bit structure:

Bit	Name	Value	Information
0 - 5	Data length code	00 0000	USINT
		00 0001	SINT
		00 0010	UINT
		00 0100	UINT
		00 1000	UDINT
		01 0000	UDINT
		10 0000	REAL
6 - 7	Reserved	0	

4.18.3.8.6.2 Transfer rate

Name:
CfO_BaudData1 to CfO_BaudData8

This register can be used to define the transfer rate for retrieving the desired values.

Data type	Value
USINT	1 to 8

Bit structure:

Bit	Name	Value	Information
0 - 3	Baud rate (Code)	0000	Reserved!
		0001	300 bit/s
		0010	600 bit/s
		0011	1200 bit/s
		0100	2400 bit/s
		0101	4800 bit/s
		0110	9600 bit/s
		0111	19200 bit/s
		1000	38400 bit/s
4 - 7	Reserved	0	

4.18.3.8.6.3 Address

Name:
CfO_PAdrData1 to CfO_PAdrData8

This register can be used to define the address where the desired values will be requested from.

Data type	Value
USINT	1 to 250 (254)

Special addresses:

Value	Information
251 to 253	Reserved (in accordance with M-Bus specification)
254	Broadcast address (response from all connected slaves - risk of collision)

4.18.3.8.6.4 Index

Name:
CfO_IndexData1 to CfO_IndexData8

This register is used to specify the ordinal number of the value (independent of the medium). This value results from the order of values in the slave. The value is then transferred to the data register.

Data type	Value
USINT	1 to 255

4.18.3.8.6.5 Specifies the refresh time

Name:
CfO_ReqTimeData1 to CfO_ReqTimeData8

Slave value requests can be triggered manually or time-based. Time-based request requires the refresh time value to be specified in the "RequestTime" register. The respective unit is specified in the "MBusMode" register.

Data type	Value
USINT	1 to 255 [s, min]

4.18.3.8.6.6 M-Bus mode

Name:
CfO_MBusModeData1 to CfO_MBusModeData8

To speed up the module's boot procedure, various configuration details that define the module's behavior have been combined in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	Byte offset	0 - 7	See "Byte Offset" section
3 - 4	Reserved	0	
5	InitFrame	0	No extra frame
		1	Send extra frame
6	ApplicationResetFrame	0	No extra frame
		1	Send extra frame
7	Replacement value strategy	0	Retain last valid value
		1	Replace with static value
8	Time-based reading out	0	Disabled
		1	Enabled
9	Manually triggered reading	0	Disabled
		1	Read via the "MBusCommand" register (see 4.18.3.8.7.1 "M-Bus commands" on page 1901)
10	Unit of periodic read	0	[s] - Second
		1	[min] - Minute
11 - 15	Reserved	0	

Byte offset

The M-Bus specification allows for many individual data types. In order to also read these counter values with up to 64 bits, a slave value may have to be read using two data registers. The byte offset can be defined to read a specific part of the value.

4.18.3.8.6.7 Timeout offset

Name:
CfO_ToutOffData1 to CfO_ToutOffData8

The timeout for the M-Bus communication generally depends on the currently defined transfer rate. The user can also define an offset value in addition to the calculated standard timeout.

Timeout = standard timeout + (timeout offset * 10 ms)

Data type	Value
USINT	0 to 255: Resolution: 10 ms

4.18.3.8.6.8 Static replacement value

Name:
CfO_ReplData1 to CfO_ReplData8

This register is used to define the static replacement value if the replacement value strategy "Replace with static value" was enabled in "M-Bus mode". The data register takes on this value if an invalid input value is detected.

Data type	Value
(U)SINT (U)INT (U)DINT REAL	According to data type

4.18.3.8.7 M-Bus - Communication

Three important control and status bytes are provided in the B&R interface for communication with the M-Bus slaves. For example the "MBusCommand" register can be used to switch UART on/off to increase the system's energy efficiency.

Up to 8 cyclic input registers are registered depending on the configuration. Manually configured data must be requested via the "MBusCommand" register. The "ValidDataByte" and "InvalidDataByte" registers can be used to determine the quality of the value currently read.

Information:

The following section "M-Bus - Communication" is based solely on the B&R Standard interface.

4.18.3.8.7.1 M-Bus commands

Name:
MBusCommand

This register can be used to apply different commands to the module. The module only responds to positive edges.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Activate UART	0 → 1	Execute command
1	Read manually triggered values	0 → 1	Execute command
2	Acknowledge the "MBusState" register	0 → 1	Execute command
3 - 6	Reserved	0	
7	Deactivate UART	0 → 1	Execute command

Bit 0 and 7

The level converter is switched on by default when the module boots. These bits can be used to switch it on or off from the application to save electricity, for example.

4.18.3.8.7.2 M-Bus operation

Name:
MBusOperation

This register shows the user which task the module is currently processing. The LSB is always set when the UART is active. Manual commands are indicated by an increase of one in this byte while being processed.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	UART	0	Inactive
		1	Active
1	Read values	0	-
		1	Command being processed
2	Refresh/reset the "MBusState" register	0	-
		1	Command being processed[1)]
3 - 6	Reserved	0	
7	UART	0	Inactive
		1	Active

1) Bit 2 is only set for one X2X cycle. Requesting this bit is not recommended when operating the module behind a bus controller.

4.18.3.8.7.3 M-Bus status

Name:
MBusState

This register contains the current M-Bus network error state. All bits are managed in non-volatile memory. This means they must be reset via the "MBusCommand" register (see 4.18.3.8.7.1 "M-Bus commands" on page 1901).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Kollisionserkennung	0	Addressing OK
		1	Address repeated on bus
1	Read error (at least one)	0	Configured values OK
		1	Unable to read value
2	Checksums	0	Received checksum OK
		1	Error in input direction
3	M-Bus load	0	Power supply OK
		1	Load too high on M-Bus network
4	Communication aborted due to overflow	0	Communication OK
		1	The master is overloaded and cannot take on any additional requests. Measures taken: Repeat the request![1)]
5	Communication aborted due to level converter	0	Communication OK
		1	Level converter is OFF (aborted at runtime or not started).
6	Data exchange since startup	0	Valid data not yet received
		1	Valid data received at least one time
7	UART off MBUS ENABLE	0	M-Bus drive, level converter not active
		1	Module ready for communication

1) Communication is reestablished automatically as soon as the pending communication jobs have been processed.

4.18.3.8.7.4 Valid data

Name:
ValidDataByte

ValidData1 to ValidData8

This register indicates (by bit) which of the max. eight read values are valid.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	ValidData1	0	Value 1 invalid
		1	Value 1 valid
...	...	...	...
7	ValidData8	0	Value 8 invalid
		1	Value 8 valid

4.18.3.8.7.5 Invalid data

Name:
InvalidDataByte

InvalidData1 to InvalidData8

Validity of the read values can be checked redundantly. This register indicates (by bit) which of the max. eight read values are invalid.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	InvalidData1	0	Value 1 valid
		1	Value 1 invalid
...	...	...	...
7	InvalidData8	0	Value 8 valid
		1	Value 8 invalid

4.18.3.8.7.6 Data

Name:
Data1 to Data8

Each cyclic data register contains the respective pre-configured value from the M-Bus network. The data type of the data register was designed to be variable and must be specified by the user during configuration.

Information:

Because X2X Link can only transfer a certain number of bytes cyclically, the user must make his selection accordingly.

Data type	Value
(U)SINT (U)INT (U)DINT REAL	According to data type

4.18.3.8.7.7 Change the serial number of an M-bus slave

Name:
ChangedSNByte

This register indicates (by bit) whether one of the M-Bus slave serial numbers on the bus has changed. Only the serial numbers of the slaves accessed via the B&R interface are checked. The respective bit is toggled if a change is detected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	SN (Slave 1)	0 -> 1	Slave1: Serial number changed
		1 -> 0	
...	...	...	...
7	SN (Slave 8)	0 -> 1	Slave8: Serial number changed
		1 -> 0	

4.18.3.8.7.8 M-Bus slave serial numbers

Name:
SNData1 to SNData8

These registers contain the serial numbers of the M-Bus slaves that are accessed via the B&R interface. They are implemented acyclically and can be read using the AsIOAcc library.

Data type	Value
UDINT	0 to 4,294,967,295

4.18.3.8.8 FlatStream communication

4.18.3.8.8.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

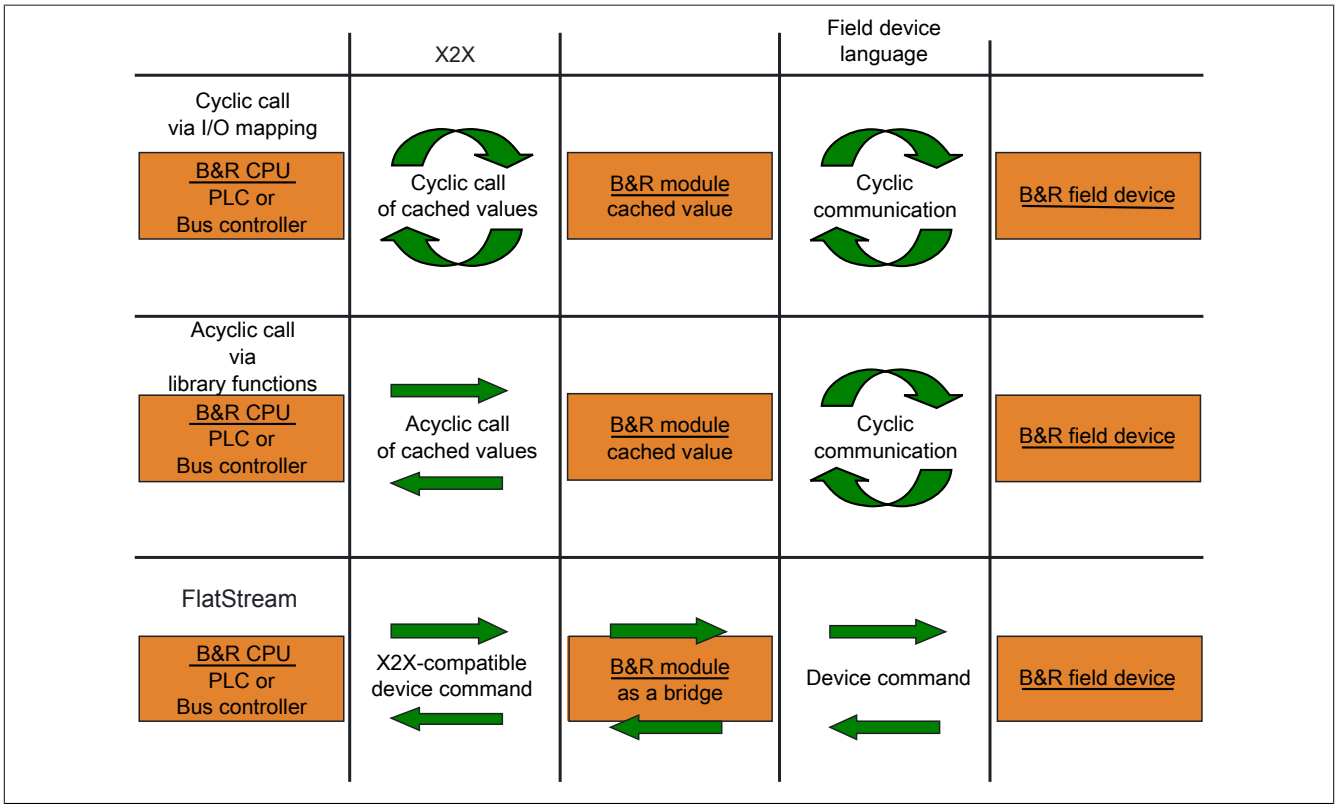


Figure 276: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.18.3.8.8.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.18.3.8.8.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

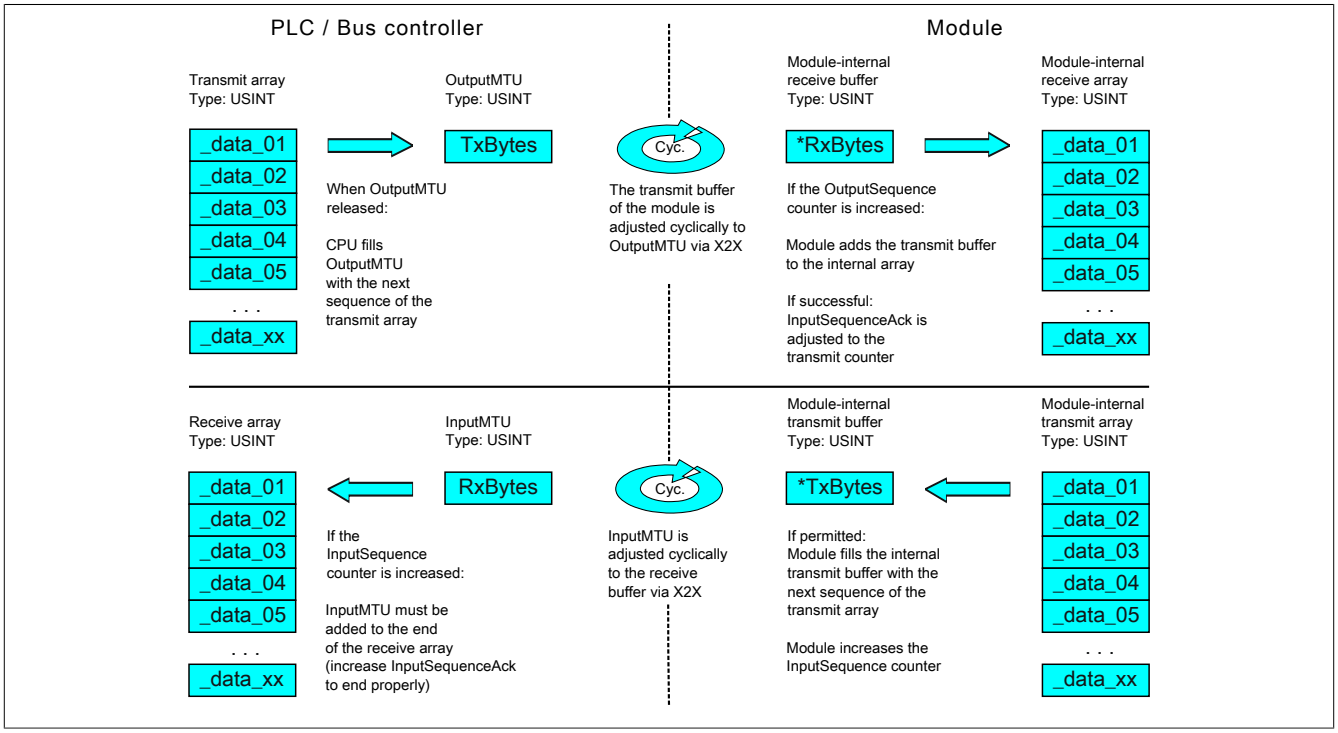


Figure 277: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.18.3.8.8.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

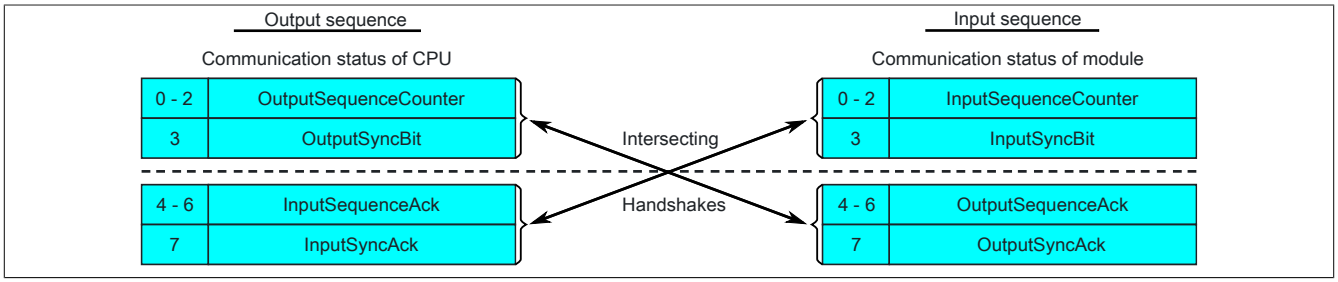


Figure 278: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

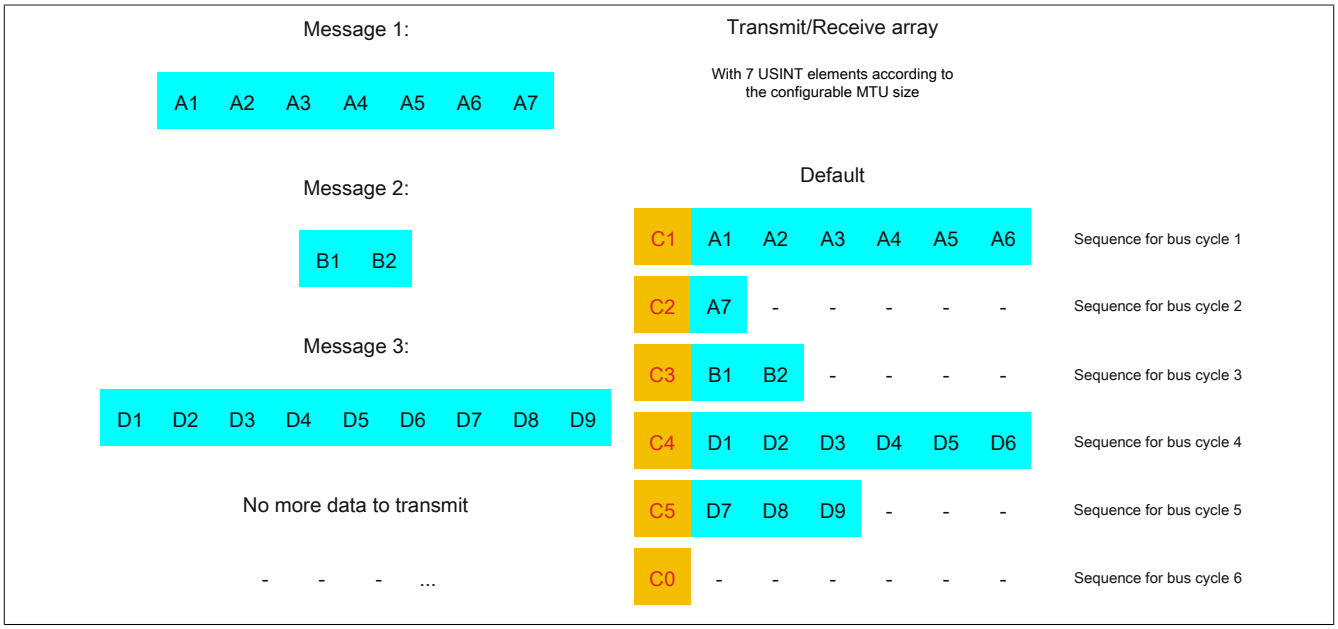


Figure 279: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 389: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 390: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

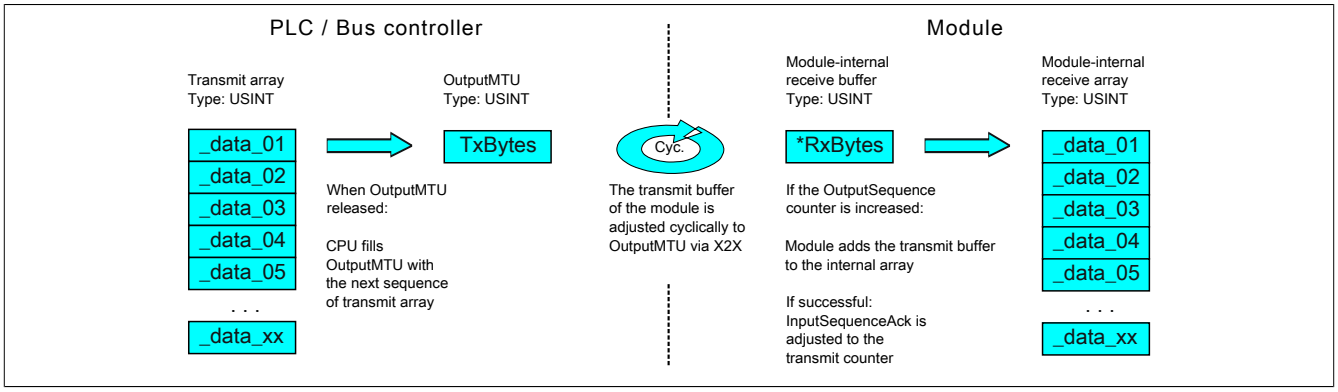


Figure 280: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

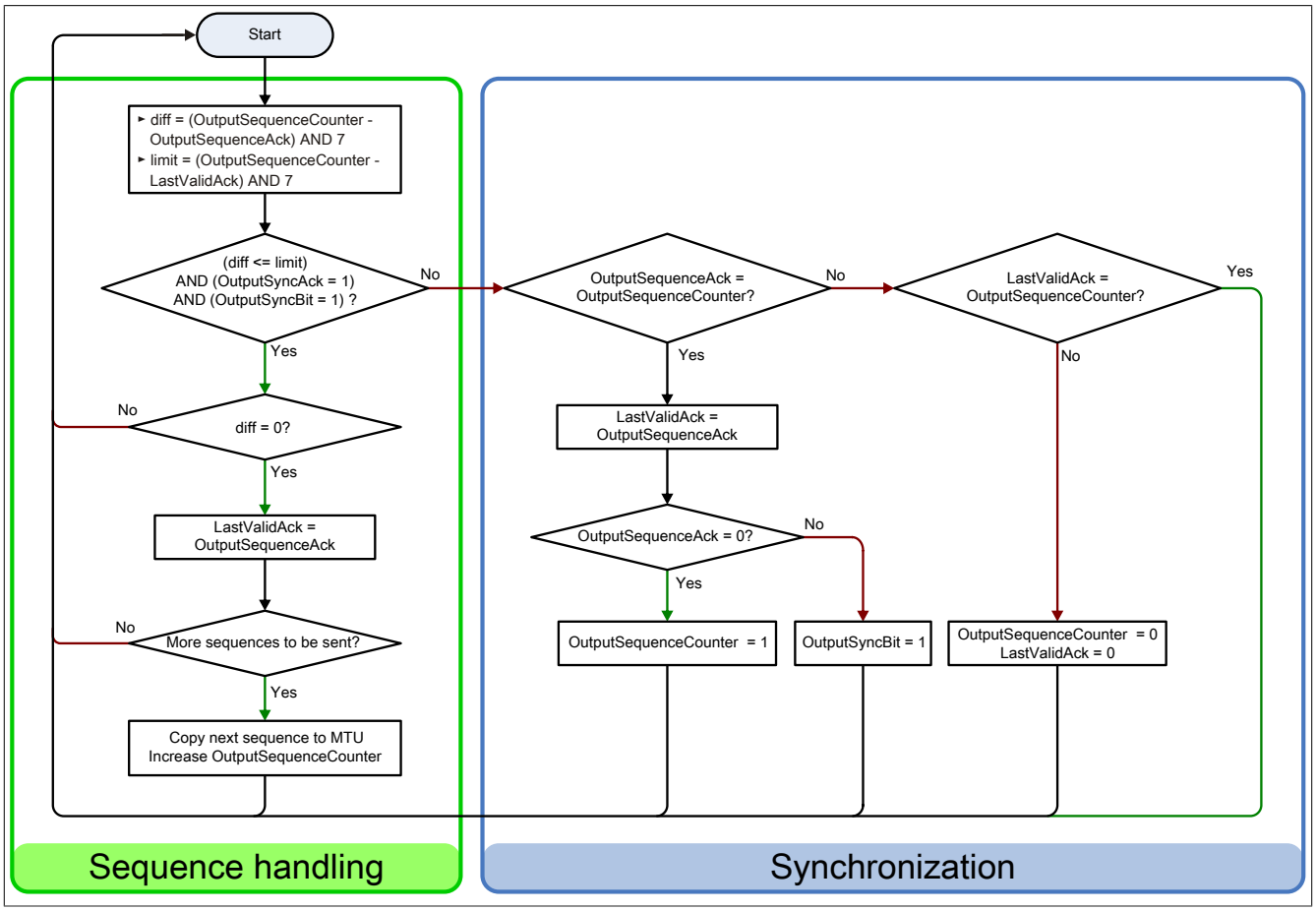


Figure 281: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

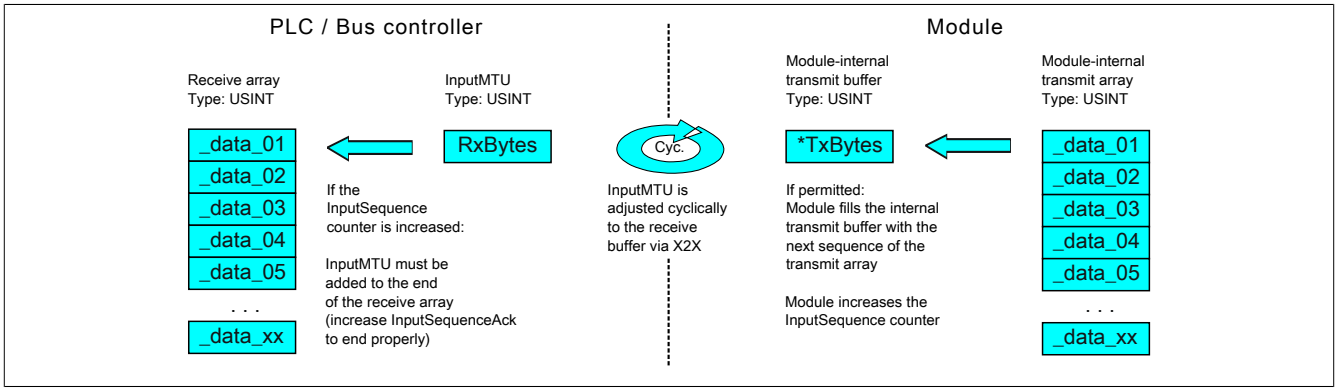


Figure 282: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

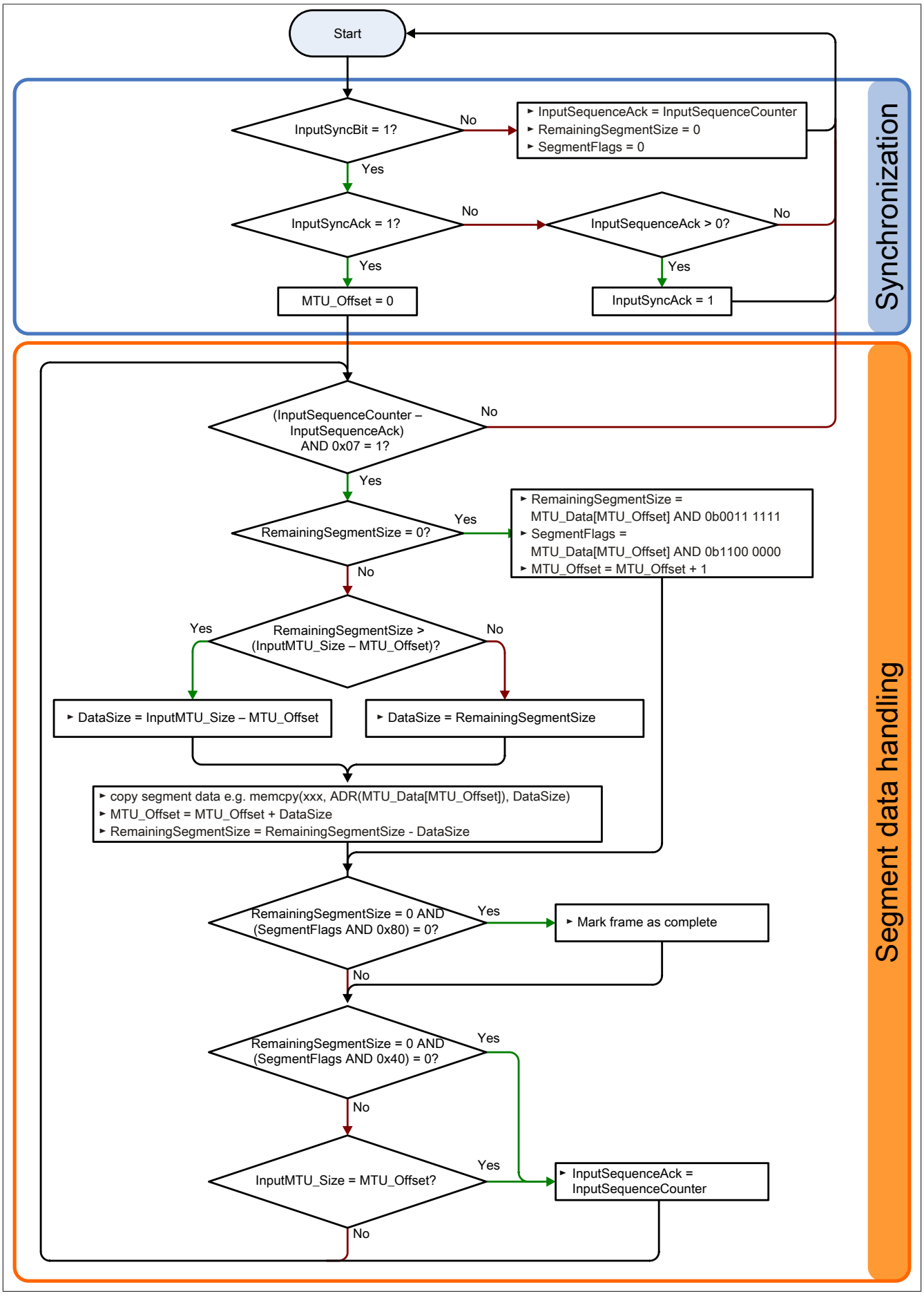


Figure 283: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

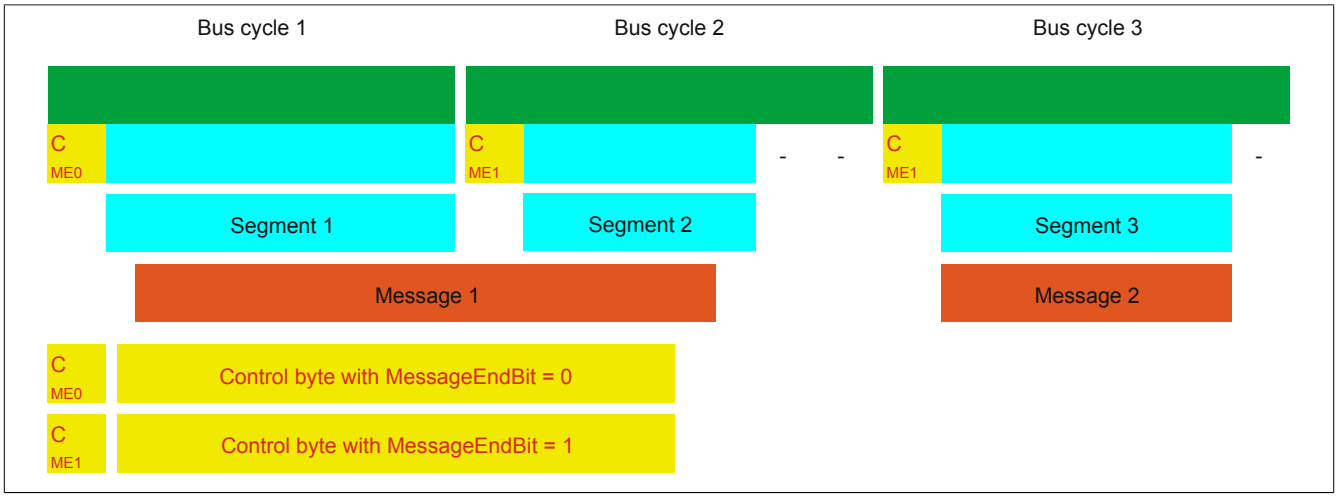


Figure 284: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

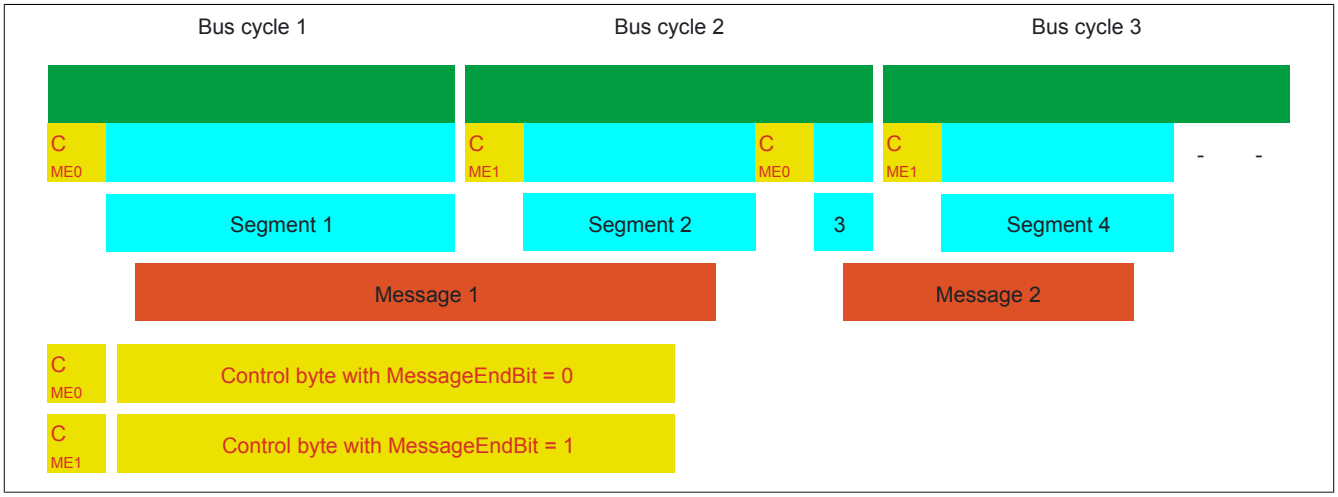


Figure 285: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

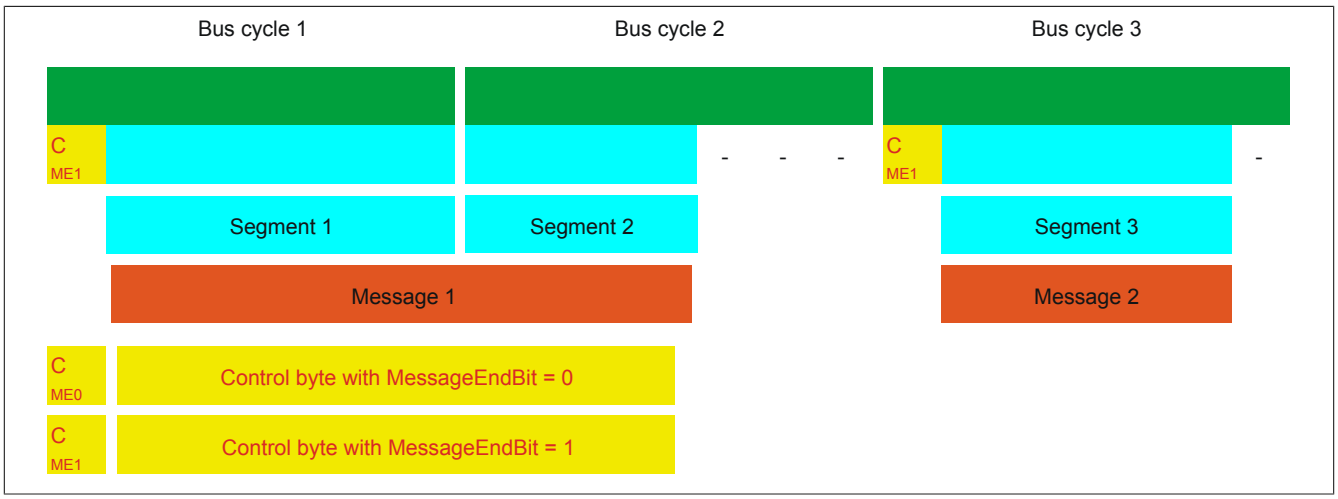


Figure 286: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

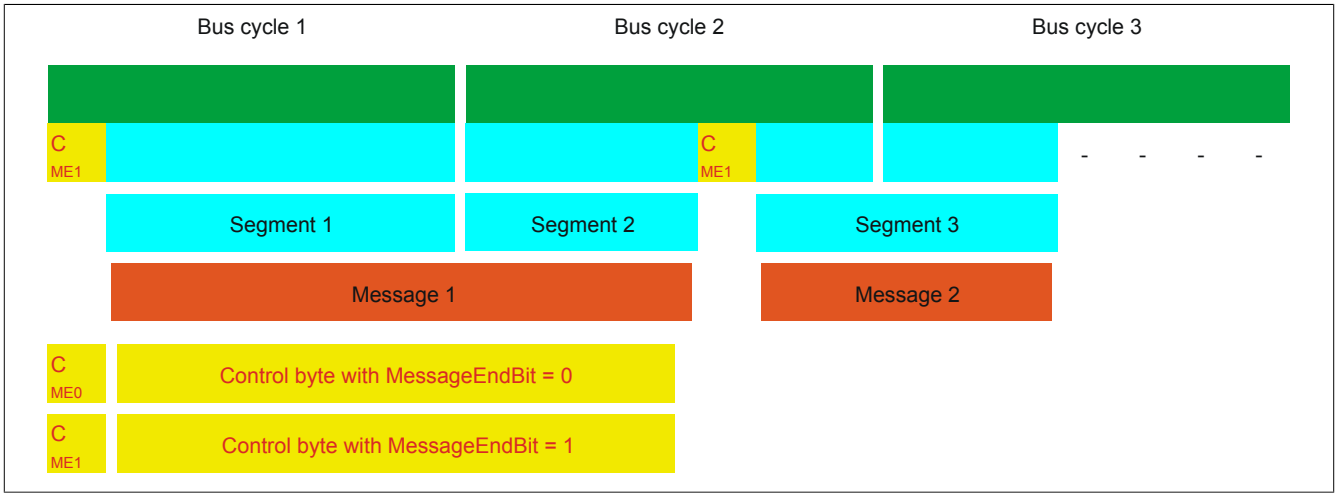


Figure 287: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

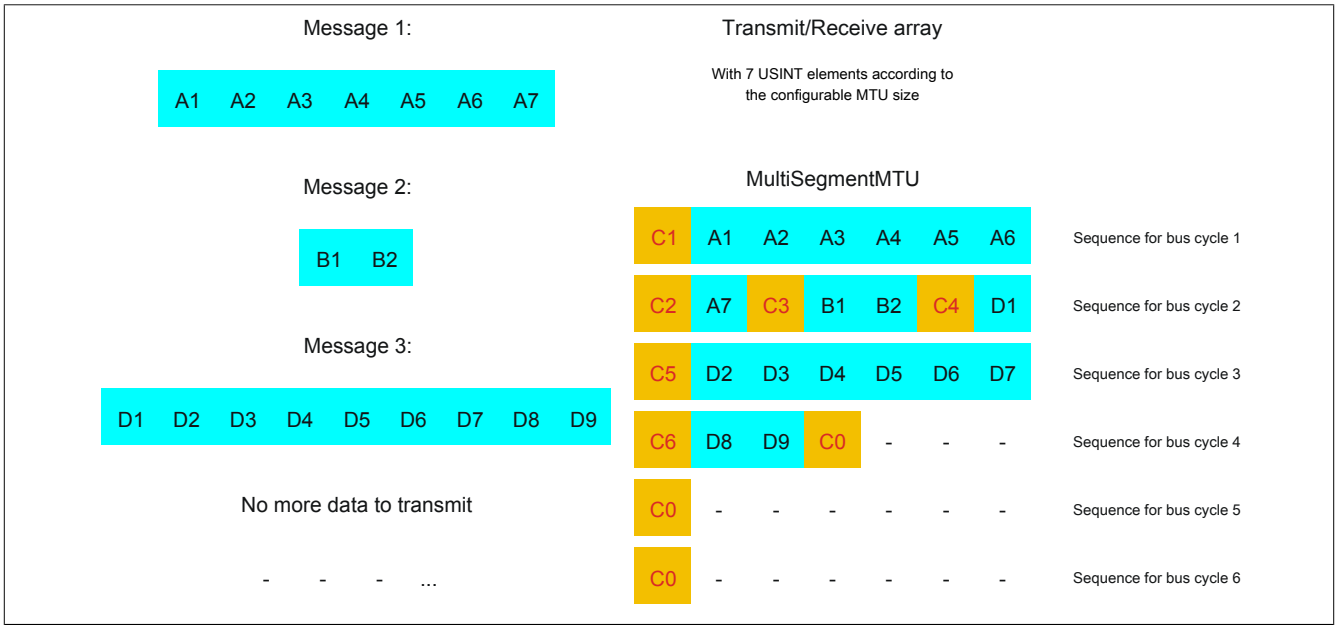


Figure 288: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 391: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 392: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

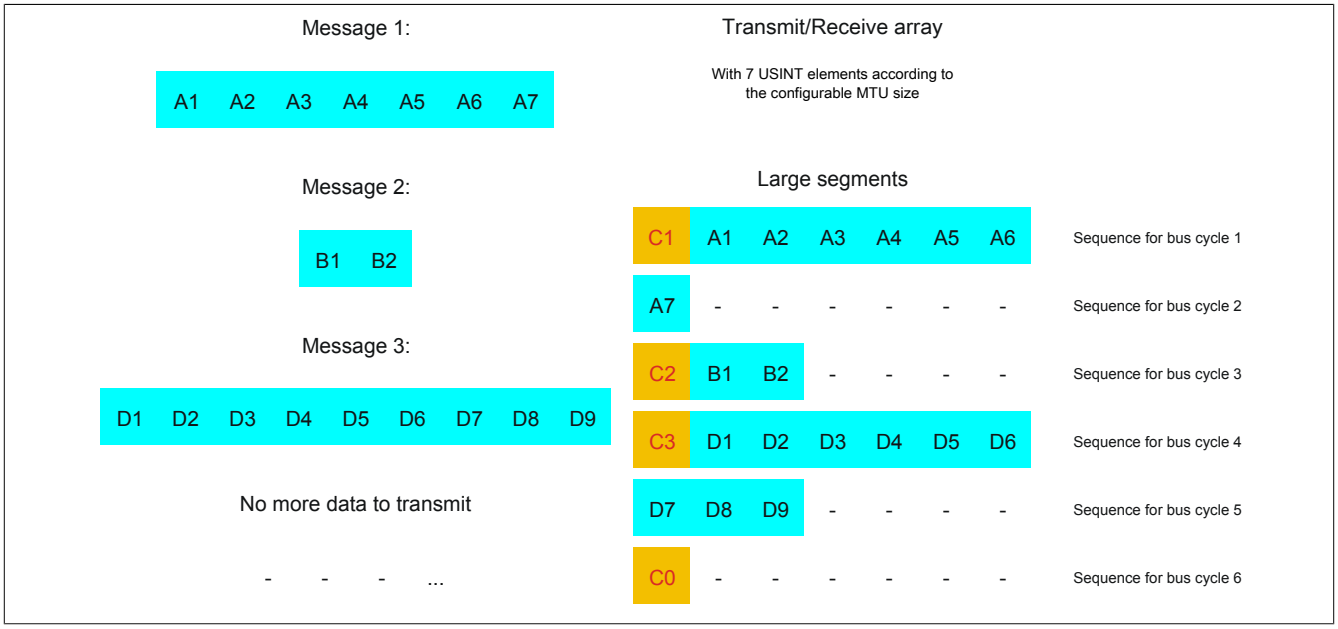


Figure 289: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 393: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

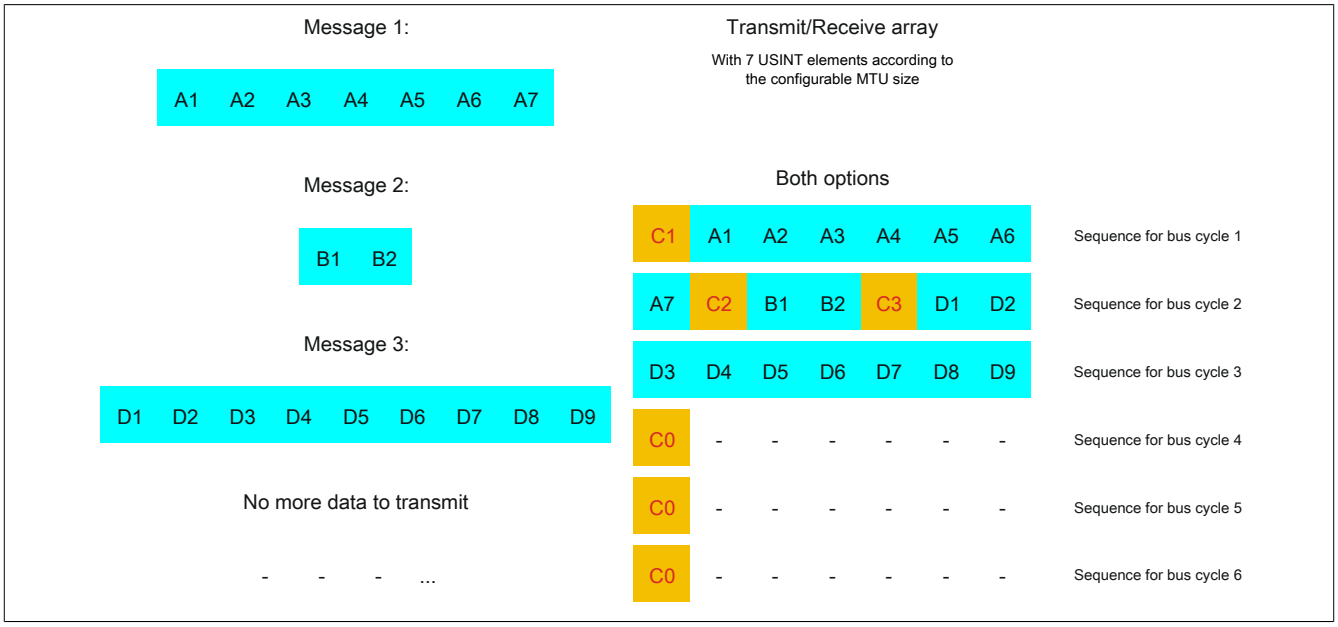


Figure 290: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 394: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.18.3.8.8.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

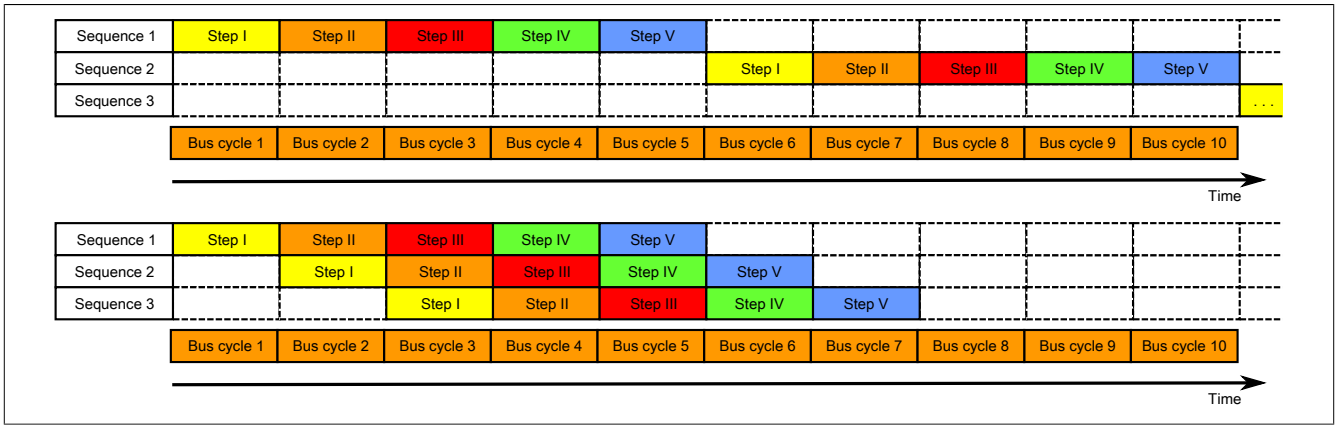


Figure 291: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

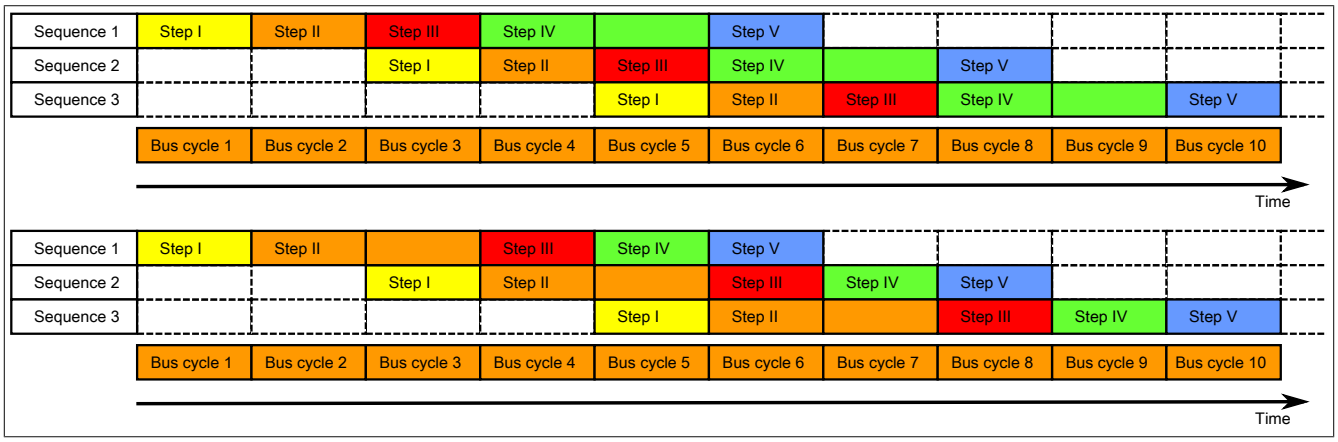


Figure 292: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

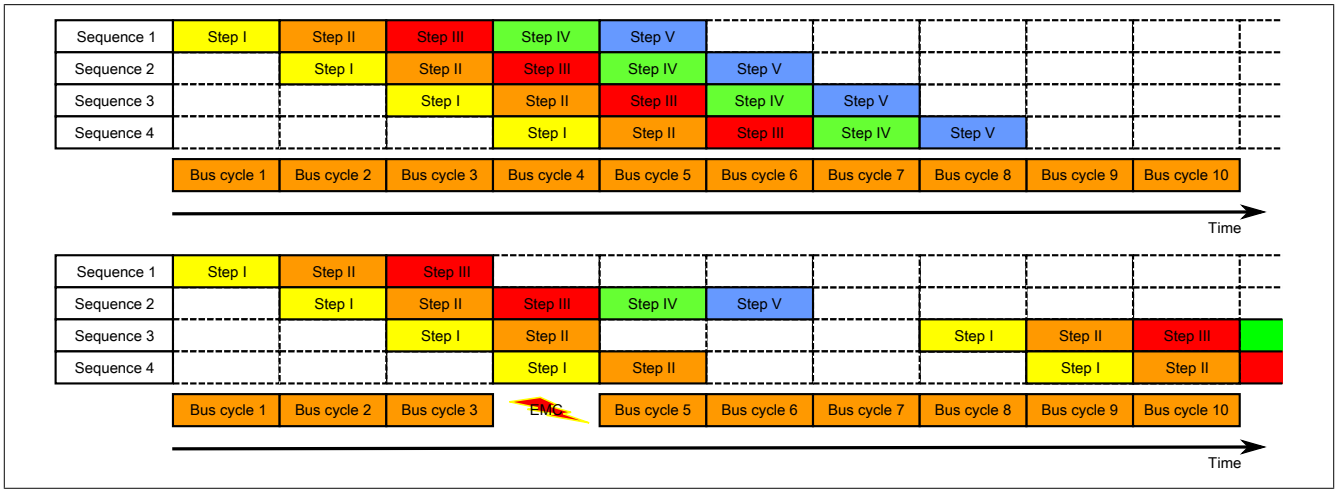


Figure 293: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.18.3.8.9 M-Bus with FlatStream

When using FlatStream communication, the module acts as a bridge between the X2X master and an intelligent field device connected to the module. FlatStream mode can be used for either point-to-point connections as well as for bus systems. Specific algorithms such as timeout and checksum monitoring are usually managed automatically. During normal operation, the user does not have direct access to these details.

Operation

The M-Bus specification recognizes four different frame types. From the application standpoint, only "long frames" are generated and transferred when using the M-Bus via FlatStreams. Due to the flexible design of the M-Bus protocol, the user must include the corresponding slave configuration with each request.

FlatStream structure		
In-/OutputSequence	Rx-/TxBytes	
(unchanged)	Control byte (unchanged)	M-Bus data (FlatStream)

4.18.3.8.9.1 FlatStream in output direction

FlatStream query

This standard protocol specifies that a data query via FlatStream consists of a main part and two index records. An index record is made up of an introduction containing various information and followed by a parameter block.

Introduction

The primary role of the main part is to assign a synchronization number and register the protocol type.

Note 1
When registering an undefined protocol type, the module works with the standard protocol.

Note 2
Because there is currently only one protocol type defined, the corresponding configuration bytes should be set to 1. This will allow the protocol to be expanded later without becoming incompatible with existing projects.

Bytes	Name	Value	Description
1	Frame number: For synchronization in the application	0 - 255	The frame number is repeated in the module's response. This allows the later response from the module to be distinctly attributed to the request.
2	Index Record Count "i"	2!	Number of subsequent index records
3	Protocol type	0	Native M-Bus (level converter mode) - see "Native M-Bus"
		1	Data query (raw data / parameters)
4	Reserved	1!	
...	Index record (configuration)		
...	Index record (data query)		

Native M-Bus

The "Native M-Bus" protocol type provides universal communication within the M-Bus network. It can be used to assemble and send M-Bus frames in the application.

A conventional data query is possible using a raw data or parameter query.

Index record 0

Configuration block

The interface parameters for defining the module's behavior in the M-Bus network must be chosen configuration part.

Information:

With the standard protocol, the index record must be resent with each request for configuration.

Introduction

Bytes	Name	Value	Description
1	Index record type	0!	Module interface configuration
2	Counter (config parameter)	5!	Number of subsequent M-Bus parameters
3	Length of parameter block - Low	19!	Length of index record description
4	Length of parameter block - High	0!	Length of index record description

Parameter block

Configuration parameter 0 - Addressing type

Bytes	Name	Value	Description
1	Parameter number	0!	
2	Length	1!	
3	Addressing type	1	Addressing via primary address
		2	Addressing via secondary address

Configuration parameter 1 - Address

Bytes	Name	Value	Description
4	Parameter number	1!	
5	Length	4!	
6	Address - LowLow	1 - 255	Primary address
7	Address - LowHigh	0 - 255	0!, if primary addressing
8	Address - HighLow	0 - 255	0!, if primary addressing
9	Address - HighHigh	0 - 255	0!, if primary addressing

Configuration parameter 2 - Transfer rate

Bytes	Name	Value	Description
10	Parameter number	2!	
11	Length	2!	
12	Transfer rate Low	0 - 255	Verified transfer rates 300 bit/s, 2400 bit/s, 9600 bit/s
13	Transfer rate High	0 - 255	

Configuration parameter 3 - Timeout offset

Bytes	Name	Value	Description
14	Parameter number	3!	
15	Length	1!	
16	TimeoutOffset	0 - 255	Additional time for timeout monitoring on the M-Bus (Resolution: 10 ms)

Configuration parameter 4 - Extra frames

Bytes	Name	Value	Description
17	Parameter number	4!	
18	Length	1!	
19	M-Bus options	Bit 0 … 1	Send Init frame
		Bit 1 … 1	Send application reset
		Bit 6 … 1	Set frame count bit[1)]
		Bit 7 … 1	Request media and version

1) Some M-Bus slaves use this bit to switch to a another data set.

Index record 1

Data query block

The M-Bus parameters to be retrieved from the memory of the M-Bus slaves are requested in the request part. The user can request certain parameters from the slave or the entire slave memory.

Introduction

Bytes	Name	Value	Description
1	Index record type	1!	Data request for M-Bus slave
2	Counter (data parameter) = (d + 1)	0	• Communication via native M-Bus • Read out M-Bus raw data
		1 - 20	Number of parameters to read out
3	Length of subsequent block - Low	0 - 255	• Length of M-Bus frame to be sent • Length of parameter block • 0! with raw data query
4	Length of subsequent block - High	0 - 255	• Length of M-Bus frame to be sent • Length of parameter block • 0! with raw data query
...	Depending on request: • Native M-Bus frame • Parameter block		*Not needed if raw data query = 0*

M-Bus frame

M-Bus frame to be sent

Bytes	Name	Value	Description
1	TxByte 1	0 - 255	Byte 1 in output direction
2	TxByte 2	0 - 255	Byte 2 in output direction
n	TxByte n	0 - 255	Byte n in output direction

Parameter block

Data parameter 0

Bytes	Name	Value	Description
1	Parameter number	0!	
2	Data index	1 - 255	Data index in the M-Bus frame

Data parameter 1

Bytes	Name	Value	Description
2	Parameter number	1!	
3	Data index	1 - 255	Data index in the M-Bus frame

Data parameter d

Bytes	Name	Value	Description
...	Parameter number	d!	
...	Data index	1 - 255	Data index in the M-Bus frame

4.18.3.8.9.2 FlatStream in input direction

FlatStream response

The standard protocol has three different responses according to the request.

Response error

The error response is sent when the module receives an invalid or incomplete request.

Bytes	Name	Value	Description
1	Frame number: For synchronization in the application	0 - 255	The frame number is repeated in the module's response. This allows the response from the module to be distinctly attributed to the request.
2	Error code - LowLow	0 - 255	See error code table
3	Error code - LowHigh	0 - 255	See error code table
4	Error code - HighLow	0 - 255	See error code table
5	Error code - HighHigh	0 - 255	See error code table
6	Additional information - LowLow	0 - 255	Optional
7	Additional information - LowHigh	0 - 255	Optional
8	Additional information - HighLow	0 - 255	Optional
9	Additional information - HighHigh	0 - 255	Optional

Error codes

Error code and name	Error description
0x11111111	An M-Bus counter not responding to a data request. This can be caused by many different things: • Counter not connected • Counter defective • Counter with selected addressing parameters not found on bus
0x22222222	This error code is sent if the secondary address is addressed and the selected counter does not respond.
0x33333333	An invalid transfer rate sent via stream will not be evaluated. An M-Bus frame is not sent, the FlatStream interface responds directly with this error code.
0x44444444	If an occur occurs when querying data on the bus, the data query is terminated and this error code returned.
0x55555555	Communication aborted due to overflow (See bit 4 in section 4.18.3.8.7.3 "M-Bus status")
0x66666666	The M-Bus frame's checksum is checked before the data is evaluated by the M-Bus counter. If it does not match up, then the error code is sent right to the CPU and processing of the received data is stopped.
0x77777777	Stream (CPU -> IOM) error. The number of parameters may be incorrect. The stream undergoes very careful examination (i.e. a stream with errors will never be used).
0x88888888	Overload during M-Bus communication
0x99999999	Communication aborted due to level converter (See bit 5 in section 4.18.3.8.7.3 "M-Bus status")
0xAAAAAAAA	It is not possible to interpret the slave data. The MBus slave being used is not compatible with the parameter query. The MBus slave must be implemented using the native MBus protocol or a raw data query.

Additional information

Additional information	Error description
0x00000001	Number of index records is lower than 2
0x00000002	Stream length doesn't match
0x00000004	Index numbers don't match
0x00000008	Incorrect number of parameters per index record
0x00000010	Index length too short
0x00000020	Incorrect parameter number for index record 0
0x00000040	Incorrect parameter length for index record 0
0x00000080	Invalid addressing type
0x00000100	Invalid address
0x00000200	Invalid transfer rate
0x00000400	Invalid TimeoutOffset
0x00000800	Invalid extra frame configuration

Response - native M-Bus

This response corresponds with a successfully transferred M-Bus frame created within the application.

Bytes	Name	Value	Description
1	Frame number: For synchronization in the application	0 - 255	The frame number is repeated in the module's response. This allows the response from the module to be distinctly attributed to the request.
2	Reserved	0	
...	Response		

Response

Bytes	Name	Value	Description
1	RxByte 1	0 - 255	Byte 1 in input direction
2	RxByte 2	0 - 255	Byte 2 in input direction
n	RxByte n	0 - 255	Byte n in input direction

Response - Raw data

The raw data response is sent if the M-Bus slave's entire memory is requested.

Bytes	Name	Value	Description
1	Frame number: For synchronization in the application	0 - 255	The frame number is repeated in the module's response. This allows the response from the module to be distinctly attributed to the request.
2	M-Bus status	0 - 255	Status info from M-Bus header
3	Raw data frame	0 - 255	Includes all bytes sent by the M-Bus slave.
...		0 - 255	

Response - Parameters

The parameter response is sent if one or more parameters from an M-Bus slave have been requested.

Bytes	Name	Value	Description
1	Frame number: For synchronization in the application	0 - 255	The frame number is repeated in the module's response. This allows the response from the module to be distinctly attributed to the request.
2	M-Bus status	0 - 255	Status info from M-Bus header
3	Parameter count "p"	0 - 255	Number of parameters received
4	M-Bus address	0 - 255	Primary address
5	Serial number - LowLow	0 - 255	Secondary address
6	Serial number - LowHigh	0 - 255	Secondary address
7	Serial number - HighLow	0 - 255	Secondary address
8	Serial number - HighHigh	0 - 255	Secondary address
9	VendorID – Low \ Version	0 - 255	See "MBus option (IndexRecord 0)"
10	VendorID – High \ Medium	0 - 255	See "MBus option (IndexRecord 0)"
11	Data structure (M-Bus)	1	Fixed data structure
		2	Variable data structure
...	Received parameter 1 through p		*Not needed if parameter count = 0*

Received parameter

Bytes	Name	Value	Description
1	Medium	0 - 255	Medium of subsequent counter value
2	Index	0 - 255	Index of subsequent counter value
3	Data length	1 - 8	Length of the counter value
		255	If the parameter number is invalid
4	DIF	0 - 255	0!, if fixed data structure
5	VIF	0 - 255	0!, if fixed data structure
6	Counter value	0 - 255	LowLowLowLowLowLowLowLow
...		...	...
13		0 - 255	HighHighHighHighHighHighHigh

4.18.3.8.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.18.3.8.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 s

4.18.4 X20CS1013

4.18.4.1 General information

The module is a DALI control device with an integrated power supply. Up to 64 operating devices can be connected.

DALI stands for Digital Addressable Lighting Interface and enables easy and safe control of light fixtures using a standardized digital operating device interface. The DALI bus conforms with IEC EN 62386 and is now supported by many electronic ballast manufacturers.

- Integrated power supply
- Up to 64 operating devices (individual addresses)
- Up to 16 groups (group addresses)
- Up to 16 scenes (scene lighting values)

4.18.4.2 Order data

Model number	Short description	Figure
	X20 electronics module communication	
X20CS1013	X20 interface module, 1x DALI master	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 395: X20CS1013 - Order data

4.18.4.3 Technical data

Product ID	X20CS1013
Short description	
Communication module	DALI master
General information	
B&R ID code	0xDE85
Diagnostics	
Module status	Yes, with status LED and software
Bus status	Yes, with status LED and software
Power consumption	
24 VDC	Max. 2.8 W
Bus	Max. 0.25 W
Thermal loss	
24 VDC	0.6 W
Bus	0.4 W
Electrical isolation	
PLC - Terminal block	Yes
Isolation voltage	
Terminal block - PLC	510 VAC / 1 minute
PLC - Ground	510 VAC / 1 minute
Certification	
CE	Yes
Dali bus	
Insulation system	Basic insulation
No load voltage	16.5 V ±5%
Signal voltage	
Low	-6.5 V to 6.5 V (typically 0 V)
High	11.5 V to 20.5 V (typically 16 V)
Signal current	
Low	≤250 mA (internally limited)
High	≤130 mA at voltages ≥11.5 V
Transfer rate	1200 baud
Maximum number of slaves	64
Data signal slew rate (Manchester bi-phase)	
Negative edge	10 µs ≤ t_{fall} ≤ 100 µs
Positive edge	10 µs ≤ t_{rise} ≤ 100 µs
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at altitudes above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Protection in accordance with EN 60529	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 396: X20CS1013 - Technical data

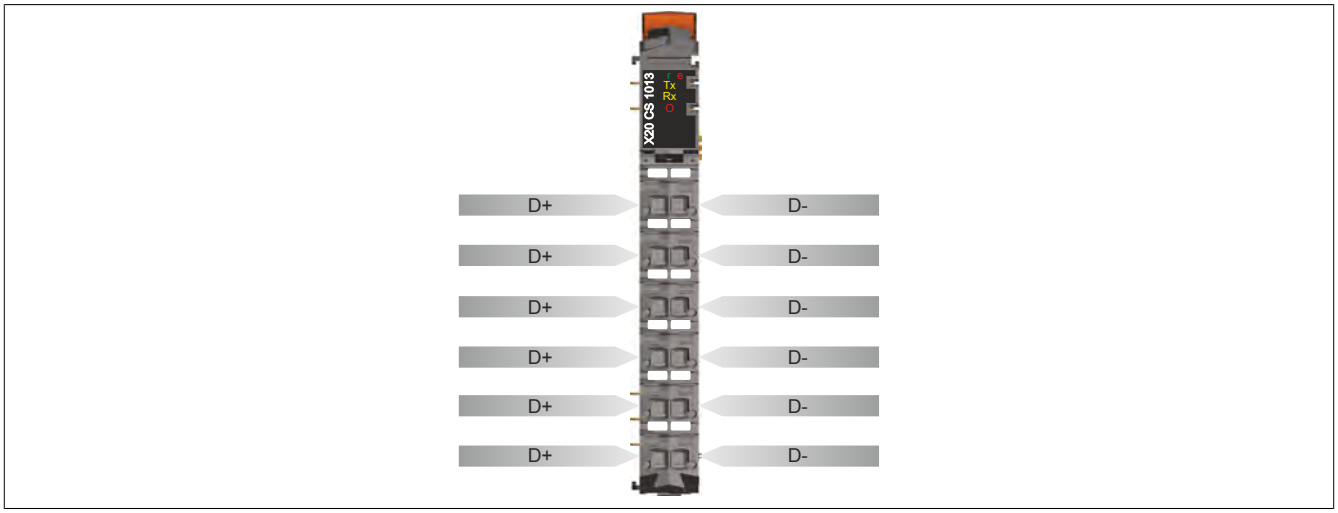
4.18.4.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			On	RUN mode
			Double flash	BOOT mode (during firmware update)[1)]
	e	Red	Off	No power to module or everything OK
			On	Error status
	Tx	Yellow		Control device (master) transmitting
	Rx	Yellow		Operating device (slave) responding
	O	Red		Error status: Overload or short circuit

1) Depending on the configuration, a firmware update can take up to several minutes.

4.18.4.5 Pinout



4.18.4.6 Using an external power supply

Since the internal DALI power supply provides sufficient power for a configuration with up to 64 slaves, the module is not designed for an external power supply.

Warning!

Using an additional DALI power supply may result in damage to the module.

4.18.4.7 Register description

4.18.4.7.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.18.4.7.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
258	Dali_State	UINT	•			
263	Dali_RequestCounter	USINT	•			
261	Dali_AnswerCounter	USINT	•			
265	Dali_Answer	USINT	•			
257	Dali_Enable	USINT			•	
262	Dali_Control	UINT			•	
265	Dali_Address	USINT			•	
267	Dali_Command	USINT			•	

4.18.4.7.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
258	0	Dali_State	UINT	•			
263	3	Dali_RequestCounter	USINT	•			
261	2	Dali_AnswerCounter	USINT	•			
265	4	Dali_Answer	USINT	•			
257	0	Dali_Enable	USINT			•	
262	2	Dali_Control	UINT			•	
265	4	Dali_Address	USINT			•	
267	5	Dali_Command	USINT			•	

1) The offset specifies the position of the register within the CAN object.

4.18.4.7.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.18.4.7.4 General information

DALI stands for Digital Addressable Lighting Interface and is mainly used to control lighting systems. The communication standard is intended for building automation systems and described in the IEC 62386 standard.

4.18.4.7.4.1 The DALI protocol

The DALI standard specifies bidirectional communication based on the "request and answer" principle. A DALI network may contain multiple masters. The serial asynchronous interface transmits voltage signals at a transfer rate of 1200 bits/s.
According to the DALI standard, up to 64 individual addresses can be assigned on the network. In addition, all of the slaves in the network can be addressed via broadcast and group addresses. 16 different group addresses can be assigned independently of the individual slave addresses. This makes it possible to send a command to multiple slaves at the same time.

4.18.4.7.5 DALI - Communication

The module provides the user with a channel for communicating with and controlling DALI slaves in a DALI network.

The multi-master mode described in the DALI standard is accepted by the module but not actively supported.

4.18.4.7.5.1 Communication in the DALI network

The module supports all commands defined in the DALI standard.

Communication in the DALI network takes place using the 2 bytes of the following registers:

- "Address of the DALI slave"
- "Direct or indirect command for receiver"

Some commands are described in the DALI specification with the structure "YAAA AAAS XXXX XXXX". In order to translate this representation to the B&R interface, the two registers "DALI_Address" and "DALI_Command" must be viewed with "Byte" as the unit.

Dali_Address								Dali_Command							
MSB	6	5	4	3	2	1	LSB	7	6	5	4	3	2	1	0
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Y	A	A	A	A	A	A	S	X	X	X	X	X	X	X	X

Key

Y	Address type
A	Address
S	Command type
X	Command

Address of the DALI slave

Name:
Dali_Address

This register provides the module with the address of the DALI slave being addressed. It also defines the address type (single or group address) and command type (direct or indirect command).

Data type	Value	
USINT	0 to 159	Single or group address for direct or indirect command
	254	Broadcast address for direct DALI command
	255	Broadcast address for indirect DALI command

Bit structure:

Bit	Name	Value	Information
0	Type of the subsequent command	0	Direct DALI command
		1	Indirect DALI command
1 - 6	Address	0 to 63	Address of an individual slave
		0 to 15	Address of a group of slaves
7	Type of the subsequent address	0	Addressing of an individual slave
		1	Addressing of a group of slaves

Direct or indirect command for receiver

Name:
Dali_Command

This register provides the module with the direct or indirect command for the receiver in the DALI network.

Data type	Value	Information
USINT	0 to 255	DALI or slave-specific command

4.18.4.7.5.2 Status in the DALI network

Name:
Dali_State

This register is used to indicate the current status of the DALI network.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Enables/Disables the level converter	0	Communication off
		1	Communication on
1	Status of the last request	0	Valid request not yet sent
		1	Transmit procedure successful
2	Status of the last response	0	No response since the last request
		1	Receive procedure successful
3	Collision (multi-master)	0	No collision
		1	Collision in the DALI network
4 - 7	Reserved	-	
8	Transmit error	0	No error
		1	Transmit procedure failed
9	Receive error	0	No error
		1	Invalid response received
10	TX busy	0	No transmission activity
		1	Transmission taking place
11	RX busy	0	No receiving activity
		1	Receiving taking place
12 - 15	Reserved	-	

4.18.4.7.5.3 Transmission counter

Name:
Dali_RequestCounter

This register provides the user with information about how many DALI messages have already been sent by the module.

Data type	Value
USINT	0 to 255

4.18.4.7.5.4 Response counter

Name:
Dali_AnswerCounter

This register provides the user with information about how many DALI messages have already been received by the module.

Data type	Value
USINT	0 to 255

4.18.4.7.5.5 Response from DALI network

Name:
Dali_Answer

This register provides the user with access to the last valid response from the downstream DALI network.

Data type	Value
USINT	0 to 255

4.18.4.7.5.6 Enabling the communication channel

Name:
Dali_Enable

This register is used to enable or disable the communication channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Turn communication on/off (via software)	0	Turn communication channel off
		1	Turn communication channel on
1	Turn power saving mode on/off	0	Supply DALI network
		1	Turn internal power supply for the module off
2 - 7	Reserved	-	

Information:

for communication in the DALI network, the internal power supply in the module must be turned on.

4.18.4.7.5.7 Controlling the DALI module

Name:
Dali_Control

This register is used to control the module. The respective command is transported via X2X Link and then executed by the module. The register is edge-triggered (i.e. this type of command is only triggered if the state of the respective bit changes).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Requests command (pos. edge)	0	No action
		1	Transmits request in the DALI network
1	Reserved	-	
2	Acknowledges the status byte (pos. edge)	0	No action
		1	Resets the status byte
3	Acknowledges the transmission counter (pos. edge)	0	No action
		1	Resets the transmission counter
4	Acknowledges the response counter (pos. edge)	0	No action
		1	Resets the response counter
5 - 15	Reserved	-	

4.18.4.7.6 Excerpt from the DALI specification

4.18.4.7.6.1 General

The DALI standard involves 2 different command types. Direct commands control the brightness of the lights on the DALI slave being addressed. This type of communication runs only from the master to the slave.

Setting the LSB in the address register will use the included command for independent digital communication. The commands are also transferred from the master to the slave. Some requests require a response from the slave. In this case, communication from the slave to the master must also be possible.

4.18.4.7.6.2 Direct DALI commands (ARC)

These commands can be used to directly set the brightness of each DALI slave. The statements 1 to 254 correspond to a brightness of the connected DALI slave based on the following formula:

$$P = 10^{\frac{Value - 1}{253 / 3}} * \frac{P_{max}}{1000}$$

Command 0 can also be transmitted to switch off a DALI slave. In this case, the brightness decreases slowly at first and then shuts off when a critical power level is crossed.

Command 255 serves as an internal mask value. It is not applied by the DALI slave, which means it has no effect on its behavior.

4.18.4.7.6.3 Indirect DALI commands for lamp wattage

Indirect commands make digital communication possible on the DALI network. In addition to the commands defined in the DALI standard, some manufacturers of DALI slaves also define their own commands.

Selected standardized DALI commands

Source: EN 62386-102:2009

Code (dec.)	Function
Indirect control commands	
0	Switches off the light immediately – No smooth transition
1	200 ms dimming up – Possible to configure the dimming speed separately – No further change once maximum is reached – Command ignored when light is off
2	200 ms dimming down – Possible to configure the dimming speed separately – No further change once minimum is reached – Command does not turn light off
3	Increases the brightness by one step – No smooth transition – No further change once maximum is reached – Command ignored when light is off
4	Decreases the brightness by one step – No smooth transition – No further change once minimum is reached – Command does not turn light off
5	Maximum brightness – No smooth transition – Turns the light on
6	Minimum brightness – No smooth transition – Turns the light on
7	Decrease brightness by one step (including switching off) – No smooth transition – Command can turn light off
8	Increase brightness by one step (including switching on) – No smooth transition – Turns the light on
9	Commence DACP sequence – Starts direct power control – Dimming speed adjusted dynamically by the control device – DACP sequence required at the end
10 - 15	Reserved
16 - 31	Enables scene 0 to 15 – Power regulated to the level stored in the scene

4.18.4.7.6.4 Indirect DALI commands for configuration

Indirect commands make digital communication possible on the DALI network. In addition to the commands defined in the DALI standard, some manufacturers of DALI slaves also define their own commands.

Information:

Some indirect DALI commands must be repeated within 100 ms. The module does not evaluate specified addresses and commands, which means this repetition must be ensured by the application.

Selected standardized DALI commands

Source: EN 62386-102:2009

Code (dec.)	Function	Response
Configuration commands[1)]		
32	Resets nonvolatile memory – DALI slave requires up to 300 ms for execution	
33	Reads out the current power level – Stores the current power value in the DTR – Command code 152 required	
34 - 41	Reserved	
Save DTR value[1)]		

Code (dec.)	Function	Response
42	Save as maximum power value	
43	Save as minimum power value	
44	Save power value as value for event of error	
45	Save power value as switch-on value	
46	Save value as dimming time	
47	Save value as dimming speed	
48 - 63	Reserved	
Used for setting system parameters[1)]		
64 - 79	Save DTR value as selected scene 0 to 15 – Scene number = Command number - 64	
80 - 95	Removes DALI slave from scene 0 to 15 – Scene number = Command number - 80	
96 - 111	Adds DALI slave to group 0 to 15 – Group number = Command number - 96	
112 - 127	Removes DALI slave from group 0 to 15 – Group number = Command number - 112	
128	Save DTR value as short address	
129 - 143	Reserved	
Request commands		
144	Checks the general status	**Bit / Value / Function** 0 / 0 / DALI slave status OK 0 / 1 / DALI slave status not OK 1 / 0 / Light status OK 1 / 1 / Light status not OK 2 / 0 / Light off 2 / 1 / Light on 3 / 0 / Last requested power level permissible 3 / 1 / Last requested power level not permissible 4 / 0 / Last dimming procedure complete 4 / 1 / Dimming procedure not yet complete 5 / 0 / DALI slave not in reset state 5 / 1 / DALI slave in reset state 6 / 0 / DALI slave has short address 6 / 1 / DALI slave has no short address 7 / 0 / Reset or control command not yet received by DALI slave 7 / 1 / Reset or control command received by DALI slave
145	Checks communication readiness	Yes/No
146	Checks for light failure	Yes/No
147	Checks whether light is currently on	Yes/No
148	Checks whether the last requested power value was applied	Yes/No
149	Checks whether the DALI slave is in reset state	Yes/No
150	Checks whether the DALI slave has a short address	Yes/No
151	Checks whether the DALI slave has a version number	The response depends on the DALI slave: • Yes/No (DALI slave has a version number or not) • Version number
152	Checks the DTR value	DTR value
153	Checks the device type	DALI-specific code for categorizing DALI slaves
154	Checks the physical minimum level (greater than 0)	Value of physical minimum level
155	Checks for power failure	Yes/No
156 - 159	Reserved	
160	Checks the current power level	Current power level or 255 if the light is being warmed up
161	Checks the maximum value	Maximum value
162	Checks the minimum value	Minimum value
163	Checks the switch-on power level	Switch-on power level
164	Checks the power level in the event of error	Power level in the event of error
165	Checks the dimming time and dimming speed	**Bit / Function** 0 - 3 / Dimming speed 4 - 7 / Dimming time
166 - 175	Reserved	
176 - 191	Checks the light level for scene 0 to 15	
192	Checks whether the DALI slave member is part of group 0 to 7	**Bit / Value / Function** 0 / 0 / Slave not in group 0 0 / 1 / Slave in group 0 ... / / 7 / 0 / Slave not in group 7 7 / 1 / Slave in group 7

<table>
<tr><th>Code (dec.)</th><th>Function</th><th>Response</th></tr>
<tr><td>193</td><td>Checks whether the DALI slave member is part of group 8 to 15</td><td>
<table>
<tr><th>Bit</th><th>Val-ue</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>Slave not in group 8</td></tr>
<tr><td>1</td><td>Slave in group 8</td></tr>
<tr><td>...</td><td></td><td></td></tr>
<tr><td rowspan="2">7</td><td>0</td><td>Slave not in group 15</td></tr>
<tr><td>1</td><td>Slave in group 15</td></tr>
</table>
</td></tr>
<tr><td>194</td><td>Checks a 24-bit random address (H)</td><td>Random address (higher 8 bits)</td></tr>
<tr><td>195</td><td>Checks a 24-bit random address (M)</td><td>Random address (middle 8 bits)</td></tr>
<tr><td>196</td><td>Checks a 24-bit random address (L)</td><td>Random address (lower 8 bits)</td></tr>
<tr><td>197 - 223</td><td>Reserved</td><td></td></tr>
<tr><td>224 - 255</td><td>Checks application-specific defined commands</td><td></td></tr>
</table>

1) Any command in the range 32 to 129 must be repeated within the next 100 ms. No other commands can be transmitted to the DALI slave being addressed during this time.

4.18.4.7.6.5 DALI special commands

In the DALI standard, special commands are described as a bit structure represented by the arrangement YAAAAAAS XXXXXXXX (see also section 4.18.4.7.5.1 "Communication in the DALI network"). This chapter contains information about he most important special commands from the DALI specification.

Leave special modes

TERMINATE

YAAAAAAS XXXXXXXX 10100001 00000000

Switches all DALI slaves on the bus in normal mode

Write DTR

DATA TRANSFER REGISTER (DTR)

YAAAAAAS XXXXXXXX 10100011 xxxxxxxx

Writes the bit pattern xxxxxxxx to the Data Transfer Register (DTR)

Special addressing for address assignment

INITIALISE

YAAAAAAS XXXXXXXX 10100101 xxxxxxxx

Allows commands for special addressing within the next 15 minutes.

Information:

- **The command must be sent twice within 100 ms.**
- **"TERMINATE" can be used to exit initialization early.**
  Reinitializing (before the 15 minutes is completed) extends initialization by a further 15 minutes.

RANDOMISE

YAAAAAAS XXXXXXXX 10100111 00000000

Information:

The command must be sent twice within 100 ms.

SEARCHADDRH
SEARCHADDRM
SEARCHADDRL

YAAAAAAS XXXXXXXX 10110001 hhhhhhhh
10110011 mmmmmmmm
10110101 llllllll

"hhhhhhhh", "mmmmmmmm" and "llllllll" represent the currently "selected" 24-bit address in the DALI network.

COMPARE

YAAAAAAS XXXXXXXX 10101001 00000000

All slaves in the DALI network with a 24-bit address less than or equal to hhhhhhhh mmmmmmmm llllllll respond with YES. By repeatedly assigning new search addresses and using "COMPARE", it is possible to select the currently initialized slave with the smallest 24-bit address.

PROGRAM SHORT ADDRESS

YAAAAAAS XXXXXXXX 10110111 0aaaaaa1

The selected slave takes on the short address assigned to aaaaaa.

QUERY SHORT ADDRESS

YAAAAAAS XXXXXXXX = 10111011 00000000

The selected slave responds with its current short address. If no short address has been assigned, it responds with 255. This can be used to check the possible success of address assignment.

VERIFY SHORT ADDRESS

YAAAAAAS XXXXXXXX 10111001 0aaaaaa1

The selected slave responds with YES if the value specified on aaaaaa corresponds to its short address. This can be used to check the possible success of address assignment.

WITHDRAW

YAAAAAAS XXXXXXXX 10101011 00000000

The selected slave is excluded from the subsequent search with "COMPARE" statements but remains initialized and can be selected.

PHYSICAL SELECTION

YAAAAAAS XXXXXXXX = 10111101 00000000

The selected slave is excluded from the subsequent search with "COMPARE" statements, no longer initialized and can no longer be selected.

Additional special commands

Additional special commands can be found in the DALI standard.

4.18.4.7.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.18.4.7.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
30 ms

4.18.5 X20(c)CS1020

4.18.5.1 General information

In addition to the standard I/O, complex devices often need to be connected. The X20CS communication modules are designed precisely for cases like this. As normal X20 electronics modules, they can be placed anywhere on the remote backplane.

- RS232 interface for serial, remote connection of complex devices to the X20 system

4.18.5.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.18.5.3 Order data

Model number	Short description	Figure
	X20 electronics module communication	
X20CS1020	X20 interface module, 1 RS232 interface, max. 115.2 kbit/s	
X20cCS1020	X20 interface module, coated, 1 RS232 interface, max. 115.2 kbit/s	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 397: X20CS1020, X20cCS1020 - Order data

4.18.5.4 Technical data

Product ID	X20CS1020	X20cCS1020
Short description		
Communication module	1x RS232	
General information		
B&R ID code	0x1FCF	0xE7F2
Status indicators	Data transfer, operating status, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Data transfer	Yes, using status LED	
Power consumption		
Bus	0.01 W	
Internal I/O	1.44 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
IF1 - Bus	Yes	
IF1 - I/O supply	No	
Certification		
CE	Yes	
cULus	Yes	-
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 1)	Yes	-
KC	Yes	-
GL	Yes	-
LR	Yes	-
GOST-R	Yes	
Interfaces		
IF1 interface		
Signal	RS232	
Design	Connection made using 12-pin X20TB12 terminal block	
Max. distance	900 m	
Transfer rate	Max. 115.2 kbit/s	
FIFO	1 kB	
Handshake lines	RTS, CTS	
Controller	UART type 16C550 compatible	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 398: X20CS1020, X20cCS1020 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

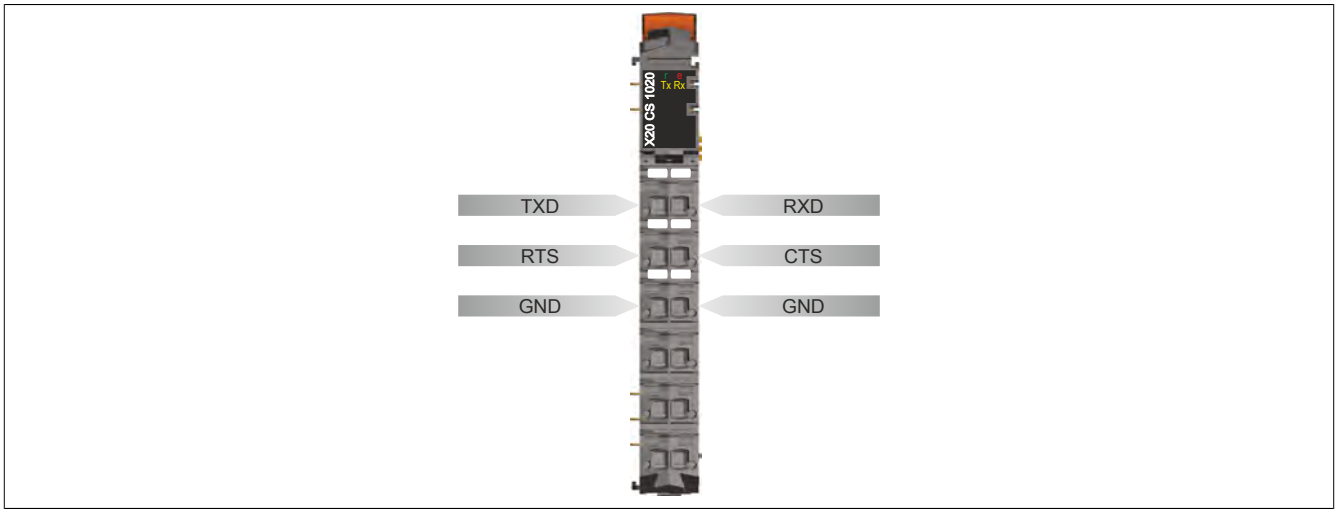
4.18.5.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	An I/O error has occurred, see 4.18.5.8.9.1 "Error message status bits"
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	Tx	Yellow	On	The module transmits data via the RS232 interface.
	Rx	Yellow	On	The module receives data via the RS232 interface.

1) Depending on the configuration, a firmware update can take up to several minutes.

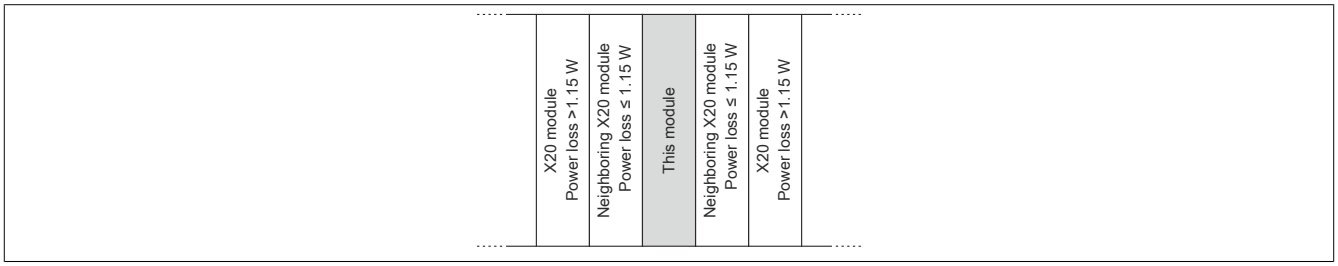
4.18.5.6 Pinout



4.18.5.7 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.18.5.8 Register description

4.18.5.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.18.5.8.2 Function model 2 - Stream and Function model 254 - Cyclic stream

The "Stream" and "Cyclic stream" function models use a module-specific driver for the operating system. The interface can be controlled using the "DVFrame" library and be reconfigured at runtime.

Function model - Stream

In the "Stream" function model, the CPU communicates with the module acyclically. The interface is relatively convenient, but the timing is very imprecise.

Function model - Cyclic stream

The "Cyclic stream" function model was implemented later. From the application's point of view, there is no difference between the "Stream" and "Cyclic stream" function models. Internally, however, the cyclic I/O registers are used to ensure that communication follows deterministic timing.

Information:

- **In order to use the "Stream" and "Cyclic stream" function models, you must be using B&R controllers of the type "SG4".**

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Module – Configuration						
-	AsynSize	-				
Status messages – Configuration						
50	CfO_RxStateIgnoreMask	UINT				•
6273	CfO_ErrorID0007	USINT				•
Status messages – Communication						
6145	ErrorByte	USINT	•			
	StartBitError	Bit 0				
	StopBitError	Bit 1				
	ParityError	Bit 2				
	RXoverrun	Bit 3				
6209	ErrorQuitByte	USINT			•	
	QuitStartBitError	Bit 0				
	QuitStopBitError	Bit 1				
	QuitParityError	Bit 2				
	QuitRXoverrun	Bit 3				

4.18.5.8.3 Function model 254 - FlatStream

The "FlatStream" function model provides independent communication between an X2X Link master and the module. This interface was implemented as a separate function model for the module. Serial information is transferred via cyclic input and output registers. The sequence and control bytes are used to control this data stream (see 4.3.7.10.8 "FlatStream communication").

When using the Flatstream function model, the user can choose whether to use the "AsFltGen" library in AS for implementation or to adapt Flatstream handling directly to the individual requirements of the application.

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Serial interface – Configuration						
1	phyMode	USINT				•
12	phyBaud	UDINT				•
3	phyData	USINT				•
5	phyStop	USINT				•
7	phyParity	USINT				•
Handshake – Configuration						
66	rxlLock	UINT				•
70	rxlUnlock	UINT				•
34	hssXOn	UINT				•
38	hssXOff	UINT				•
42	hssPeriod	UINT				•
19	hshTxF	USINT				•
29	hshRxF	USINT				•
27	hshSet	USINT				•
25	hshClr	USINT				•
17	hshInv	USINT				•
Frame – Configuration						
74	rxCto	UINT				•
106	txCto	UINT				•
78	rxEomSize	UINT				•
110	txEomSize	UINT				•
Index * 4 + 82	rxEomCharN (Index N = 0 to 3)	UINT				•
Index * 4 + 114	txEomCharN (Index N = 0 to 3)	UINT				•
Status messages – Configuration						
50	CfO_RxStateIgnoreMask	UINT				•
6273	CfO_ErrorID0007	USINT				•
Status messages – Communication						
6145	ErrorByte	USINT	•			
	StartBitError	Bit 0				
	StopBitError	Bit 1				
	ParityError	Bit 2				
	RXoverrun	Bit 3				
6209	ErrorQuitByte	USINT			•	
	QuitStartBitError	Bit 0				
	QuitStopBitError	Bit 1				
	QuitParityError	Bit 2				
	QuitRXoverrun	Bit 3				
FlatStream						
225	OutputMTU	USINT				•
227	InputMTU	USINT				•
229	Mode	USINT				•
231	Forward	USINT				•
238	ForwardDelay	UINT				•
128	InputSequence	USINT	•			
Index + 128	RxByteN (Index N = 1 to 27)	USINT	•			
160	OutputSequence	USINT			•	
Index + 160	TxByteN (Index N = 1 to 27)	USINT			•	

4.18.5.8.4 Function model 254 - Bus controller

The "Bus controller" function model is a reduced form of the "FlatStream" function model. Instead of up to 27 Tx / Rx bytes, a maximum of 7 Tx / Rx bytes can be used.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Serial interface – Configuration							
257	-	phyMode_CANIO	USINT				●
268	-	phyBaud_CANIO	UDINT				●
259	-	phyData_CANIO	USINT				●
261	-	phyStop_CANIO	USINT				●
263	-	phyParity_CANIO	USINT				●
Handshake – Configuration							
322	-	rxILock_CANIO	UINT				●
326	-	rxIUnlock_CANIO	UINT				●
290	-	hssXOn_CANIO	UINT				●
294	-	hssXOff_CANIO	UINT				●
298	-	hssPeriod_CANIO	UINT				●
275	-	hshTxF_CANIO	USINT				●
285	-	hshRxF_CANIO	USINT				●
281	-	hshClr_CANIO	USINT				●
283	-	hshSet_CANIO	USINT				●
287	-	hshFrm_CANIO	USINT				●
273	-	hshInv_CANIO	USINT				●
Frame – Configuration							
330	-	rxCto_CANIO	UINT				●
362	-	txCto_CANIO	UINT				●
334	-	rxEomSize_CANIO	UINT				●
366	-	txEomSize_CANIO	UINT				●
Index*4 + 338	-	rxEomCharN (N = 0 to 3)	UINT				●
Index*4 + 370	-	txEomCharN (N = 0 to 3)	UINT				●
Status messages – Configuration							
306	-	CfO_RxStateIgnoreMask_CANIO	UINT				●
6273	-	CfO_ErrorID0007	USINT				●
Status messages – Communication							
6145	-	ErrorByte	USINT		●		
		StartBitError	Bit 0				
		StopBitError	Bit 1				
		ParityError	Bit 2				
		RXoverrun	Bit 3				
6209	-	ErrorQuitByte	USINT				●
		QuitStartBitError	Bit 0				
		QuitStopBitError	Bit 1				
		QuitParityError	Bit 2				
		QuitRXoverrun	Bit 3				
FlatStream							
225	-	OutputMTU	USINT				●
227	-	InputMTU	USINT				●
229	-	Mode	USINT				●
231	-	Forward	USINT				●
238	-	ForwardDelay	UINT				●
128	0	InputSequence	USINT	●			
Index + 128	Index	RxByteN (Index N = 1 to 7)	USINT	●			
160	0	OutputSequence	USINT			●	
Index + 160	Index	TxByteN (Index N = 1 to 7)	USINT			●	

1) The offset specifies the position of the register within the CAN object.

4.18.5.8.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.18.5.8.5 Serial interface – Configuration

The user has to configure 5 registers to operate the serial interface.

4.18.5.8.5.1 Mode_IF

Name:
phyMode
phyMode_CANIO

This register is used to determine the current operating mode of the interface.

Enabling the interface is only permitted after complete configuration of the other registers. If parameters need to be changed, the interface must first be disabled.

Data type	Value	Description
USINT	0	RS232 interface disabled (default)
	2	RS232 interface enabled

4.18.5.8.5.2 Baudrate_IF

Name:
phyBaud
phyBaud_CANIO

This register is used to set the baud rate of the interface in bit/s.

Data type	Value	Description
UDINT	1200	1.2 kbaud
	2400	2.4 kbaud
	4800	4.8 kbaud
	9600	9.6 kbaud
	19200	19.2 kbaud
	38400	38.4 kbaud
	57600	57.6 kbaud
	115200	115.2 kbaud

4.18.5.8.5.3 Databit_IF

Name:
phyData
phyData_CANIO

This register is used to specify the number of bits to be transferred for each character.

Data type	Value	Description
USINT	7	7 data bits
	8	8 data bits (default)

4.18.5.8.5.4 Stoppbit_IF

Name:
phyStop
phyStop_CANIO

This register is used to define the number of stop bits.

Data type	Value	Description
USINT	2	1 stop bit (default)
	4	2 stop bits

4.18.5.8.5.5 Parity_IF

Name:
phyParity
phyParity_CANIO

This register is used to define the parity check type. Possible values are ASCII coded.

Data type	Value	Description
USINT	48	"0" - (low) bit is always 0
	49	"1" - (high) bit is always 1
	69	"E" - (even) even parity (default)
	78	"N" - (no) no bit
	79	"O" - (odd) odd parity

4.18.5.8.6 Handshake - Configuration

In order to guarantee that serial communication runs smoothly, the size of the receive buffer in the module must be known. In addition, the user can configure a software or hardware handshake algorithm.

4.18.5.8.6.1 Locking the receive buffer

Name:
rxlLock
rxlLock_CANIO

This register is used to configure the upper threshold of the receive buffer.

The two registers "Lock" and "Unlock" can be used for "flow control" monitoring of the communication. If the amount of data from the module input exceeds the "Lock" register value, flow control switches to the "passive" state. To return to the "active" or "ready" state, the amount of data in the receive buffer must fall under the default value of the "Unlock" register.

Information:

These registers simulate the behavior of a Schmitt trigger, so the value of the "Lock" register must be greater than the value of the "Unlock" register.

Data type	Value	Description
UINT	0 to 4095	Upper threshold of the receive buffer (default = 1024)

4.18.5.8.6.2 Unlocking the receive buffer

Name:
rxlUnlock
rxlUnlock_CANIO

This register is used to configure the lower threshold of the receive buffer.

The two registers "Lock" and "Unlock" can be used for "flow control" monitoring of the communication. If the amount of data from the module input exceeds the "Lock" register value, flow control switches to the "passive" state. To return to the "active" or "ready" state, the amount of data in the receive buffer must fall under the default value of the "Unlock" register.

Information:

These registers simulate the behavior of a Schmitt trigger, so the value of the "Lock" register must be greater than the value of the "Unlock" register.

Data type	Value	Description
UINT	0 to 4095	Lower threshold of the receive buffer (default = 512)

4.18.5.8.6.3 RTS evaluation

Name:
hshRxF
hshRxF_CANIO

These registers can be used to configure how the hardware handshake line RTS is controlled depending on the fill level of the receive buffer.

The two registers "TxF" and 'RxF" can be used to enable flow control for the input or output direction. Communication takes place here via a ring buffer.

Information:

Only one hsh register can be configured for controlling the RTS line.

Data type	Value	Description
USINT	0	RTS line freely available for other flow control methods (default)
	16	RTS line is controlled by the fill level of the receive buffer

4.18.5.8.6.4 CTS evaluation

Name:
hshTxF
hshTxF_CANIO

This register is used to configure how the CTS hardware handshake line is evaluated. Make sure wiring to the peer station is correct when CTS query is enabled.

The two registers "TxF" and 'RxF" can be used to enable flow control for the input or output direction. Communication takes place here via a ring buffer.

Data type	Value	Description
USINT	0	CTS line ignored, data can be sent at any time (default)
	1	CTS line active and is being used for flow control, transmit enable from the peer station

4.18.5.8.6.5 Turn on software handshake

Name:
hssXOn
hssXOn_CANIO

This register can be used to configure the XOn character. The value 17 is the default, but any other value can also be configured.

The two registers "XOn" and "XOff" can be used to initiate a software handshake for flow control. When doing so, a valid ASCII character must be configured in both registers.

Data type	Value	Description
UINT	0 to 255	XOn ASCII character
	65535	No software handshake (default)

4.18.5.8.6.6 Turn off software handshake

Name:
hssXOff
hssXOff_CANIO

This register can be used to configure the XOff character. The value 19 is the default, but any other value can also be configured.

The two registers "XOn" and "XOff" can be used to initiate a software handshake for flow control. When doing so, a valid ASCII character must be configured in both registers.

Data type	Value	Description
UINT	0 to 255	XOff ASCII character
	65535	No software handshake (default)

4.18.5.8.6.7 Handshake repetition

Name:
hssPeriod
hssPeriod_CANIO

When using a software handshake, some applications require periodic repetition of the current status. The repeat time can be defined in this register in ms for this purpose.

Data type	Value	Description
UINT	0	Automatic status repeat disabled
	500 to 10000	Repeat time in ms (default = 5000)

4.18.5.8.6.8 Enable handshake manually

Name:
hshSet
hshSet_CANIO

The two registers "Set" and "Clr" can be used to manually manage the handshake via the application.

These registers can be used to force the output level of the RTS hardware handshake line to remain active.

Information:

Only one hsh register can be configured for controlling the RTS line.

Data type	Value	Description
USINT	0	RTS line freely available for other flow control methods (default)
	16	RTS line enabled

4.18.5.8.6.9 Disable handshake manually

Name:
hshClr
hshClr_CANIO

The two registers "Set" and "Clr" can be used to manually manage the handshake via the application.

These registers can be used to force the output level of the RTS hardware handshake line to remain passive.

Information:

Only one hsh register can be configured for controlling the RTS line.

Data type	Value	Description
USINT	0	RTS line freely available for other flow control methods (default)
	16	RTS line disabled

4.18.5.8.6.10 Frame detection

Name:
hshFrm
hshFrm_CANIO

This register is used to generally enable hardware-based frame detection. The RTS line is enabled as long as data is being sent. This Tx-Framing mode can be used to control external interface converters.

Information:

Only one hsh register can be configured for controlling the RTS line.

Data type	Value	Description
USINT	0	RTS line freely available for other flow control methods (default)
	80	RTS line Tx-Framing switched on

4.18.5.8.6.11 Inverting RTS/CTS

Name:
hshInv
hshInv_CANIO

This register can be used to create a logical inverse of the RTS/CTS signals.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	RTS signal	0	Inverse off (default)
		1	Inverse on
1	CTS signal	0	Inverse off (default)
		1	Inverse on
2 - 7	Reserved	0	

4.18.5.8.7 Frame - Configuration

Different message termination codes can be specified in order to correctly create transmitted Tx frames and correctly interpret received Rx frames.

4.18.5.8.7.1 Terminating when a receive timeout occurs

Name:
rxCto
rxCto_CANIO

This register is used to set the duration until a receive timeout is triggered.

The message is considered to be terminated when nothing is transfered for the specified duration.
The time is specified here in characters to ensure that it is independent of the transfer rate. The number of characters is then multiplied by the time needed to transfer a character.

Data type	Value	Description
UINT	0	Function disabled
	1 to 65535	Receive timeout in characters (default = 4)

4.18.5.8.7.2 Terminating when a transmit timeout occurs

Name:
txCto
txCto_CANIO

This register is used to set the duration until a transmit timeout is triggered.

The message is considered to be terminated when nothing is transfered for the specified duration.
The time is specified here in characters to ensure that it is independent of the transfer rate. The number of characters is then multiplied by the time needed to transfer a character.

Data type	Value	Description
UINT	0	Function disabled
	1 to 65535	Transmit timeout in characters (default = 5)

4.18.5.8.7.3 Maximum number of bytes received

Name:
rxEomSize
rxEomSize_CANIO

These registers configure the maximum number of bytes in the receive frame.

The message is considered to be ended as soon as a frame with the specified size in bytes is transferred. The longest possible frame length is the size of the 4096-byte receive buffer. Larger frames cause the Receive Overrun error.

Data type	Value	Description
UINT	0	Function disabled
	1 to 4096	Configurable receive frame length in characters (default = 256)

4.18.5.8.7.4 Maximum number of bytes transmitted

Name:
txEomSize
txEomSize_CANIO

These registers configure the maximum number of bytes in the transmit frame.

The message is considered to be ended as soon as a frame with the specified size in bytes is transferred. The longest possible frame length is the size of the 4096-byte transmit buffer. The configured transmit timeout is maintained after the frame has been sent.

Data type	Value	Description
UINT	0	Function disabled
	1 to 4096	Configurable transmit frame length in characters (default = 4096)

4.18.5.8.7.5 Define receive terminator

Name:
rxEomChar0 to rxEomChar3
rxEomChar0_CANIO to rxEomChar3_CANIO

It is possible to configure a receive terminator for all registers.

The message is considered to be terminated as soon as one of the defined characters is transferred.

Data type	Value	Description
UINT	0 to 255	Frame terminator (ASCII code)
	65535	Function disabled (default)

4.18.5.8.7.6 Define transmit terminator

Name:
txEomChar0 to txEomChar3
txEomChar0_CANIO to txEomChar3_CANIO

It is possible to configure a transmit terminator for all registers.

The message is considered to be terminated as soon as one of the defined characters is transferred.

Data type	Value	Description
UINT	0 to 255	Frame terminator (ASCII code)
	65535	Function disabled (default)

4.18.5.8.8 Status messages - Configuration

The status messages provide the user with information about the current situation in the downstream serial network.

4.18.5.8.8.1 Error detection setting

Name:
CfO_RxStateIgnoreMask
CfO_RxStateIgnoreMask_CANIO

This register has a direct effect on UART operation. Error detection in general can be disabled using the low byte. If error detection is not disabled, the high byte can be used to specify that a detected error should be interpreted as the end of the message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Reserved	0	
4	StartBitError	0	Detecting a faulty start bit
		1	Ignore
5	StopBitError	0	Detecting a faulty stop bit
		1	Ignore
6	ParityError	0	Detecting a faulty parity bit
		1	Ignore
7	RXoverrun	0	Detecting an overflow in the receive direction
		1	Ignore
8 - 11	Reserved	0	
12	StartBitError corresponds to the end of the frame (if bit 4 = 0)	0	Only display error inside the module
		1	Also signal end of frame
13	StopBitError corresponds to the end of the frame (if bit 5 = 0)	0	Only display error inside the module
		1	Also signal end of frame
14	ParityError corresponds to the end of the frame (if bit 6 = 0)	0	Only display error inside the module
		1	Also signal end of frame
15	RXoverrun corresponds to the end of the frame (if bit 7 = 0)	0	Only display error inside the module
		1	Also signal end of frame

4.18.5.8.8.2 Forward error to the application

Name:
CfO_ErrorID0007

If the UART inside the module reports an error, this byte can be used to specify which error messages are forwarded to the application.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name		Information
0	StartBitError	0	Ignore
		1	Indicating a faulty start bit
1	StopBitError	0	Ignore
		1	Indicating a faulty stop bit
2	ParityError	0	Ignore
		1	Indicating a faulty parity bit
3	RXoverrun	0	Ignore
		1	Indicating an overflow in the receive direction
4 - 7	Reserved	0	

4.18.5.8.9 Status messages - Communication

After configuration is completed, up to four status messages can be evaluated in the application.

4.18.5.8.9.1 Error message status bits

Name:
StartBitError
StopBitError
ParityError
RXoverrun

This register is used to transfer the individual bits that indicate an error. If a error occurs, the corresponding bit is set and maintained until it is acknowledged.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StartBitError	0	No error
		1	Start bit error occurred[1)]
1	StopBitError	0	No error
		1	Stop bit error occurred[1)]
2	ParityError	0	No error
		1	Parity bit error occurred[1)]
3	RXoverrun	0	No error
		1	Receive buffer overflow occurred[2)]
4 - 7	Reserved	0	

1) This error can result from things such as mismatched interface configurations or problems with the wiring.
2) This data point reports a receive buffer overrun. The buffer capacity on the module is exhausted and all subsequent data arriving at the interface is lost. An overrun always means that the data received on the module is not read fast enough by the higher-level system.
The solution here is to optimize the cycle times of all transfer routes and task classes involved and utilize the available handshake options.

4.18.5.8.9.2 Acknowledging the status bits

Name:
QuitStartBitError
QuitStopBitError
QuitParityError
QuitRXoverrun

This register is used to transfer the individual bits that acknowledge an indicated error state. After one of the bits has been set, it can be reset using the corresponding acknowledgment bit.
If the error is still actively pending, the error status bit is not deleted. The acknowledgment bit can only be reset if the error status bit is no longer set.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitStartBitError	0	No acknowledgment
		1	Acknowledge start bit error
1	QuitStopBitError	0	No acknowledgment
		1	Acknowledge stop bit error
2	QuitParityError	0	No acknowledgment
		1	Acknowledge parity bit error
3	QuitRXoverrun	0	No acknowledgment
		1	Acknowledge receive buffer overflow error
4 - 7	Reserved	0	

4.18.5.8.10 FlatStream communication

4.18.5.8.10.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

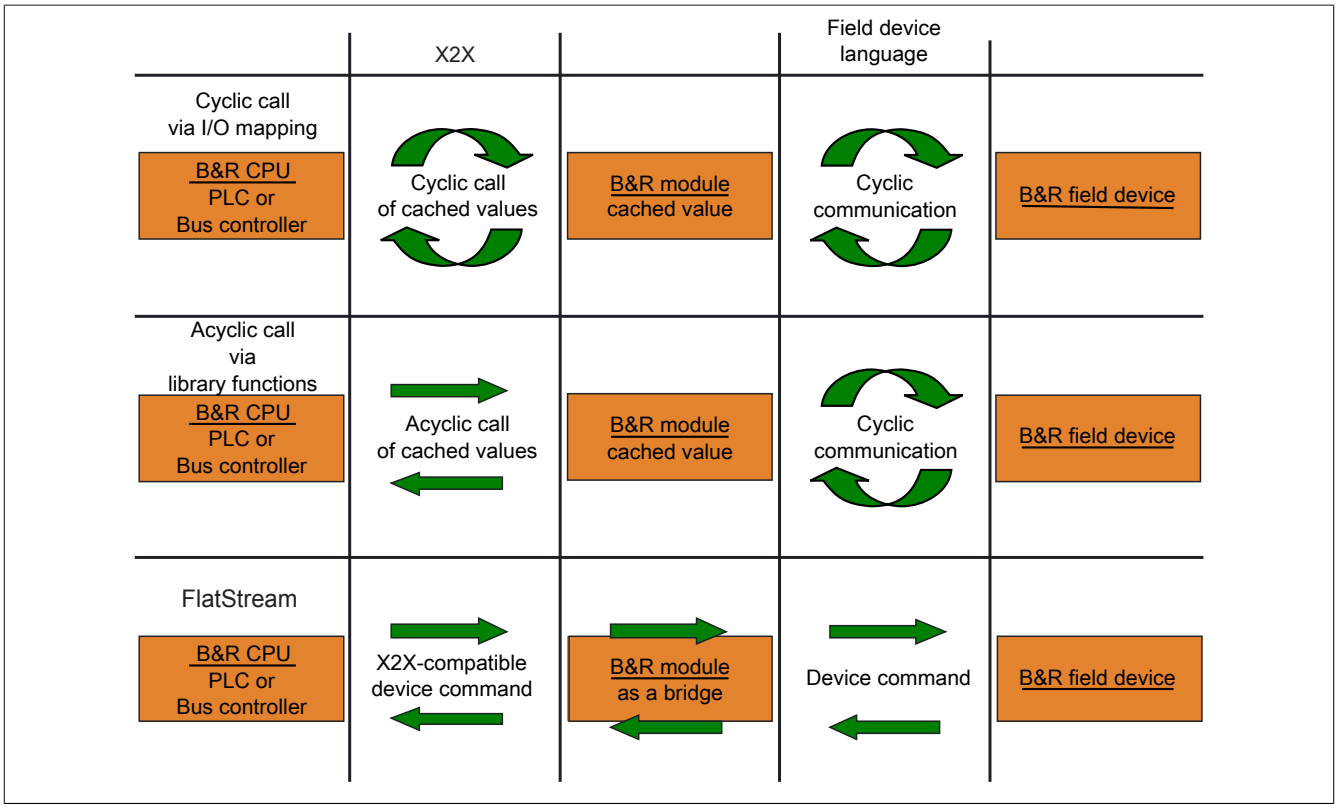


Figure 294: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.18.5.8.10.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.18.5.8.10.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

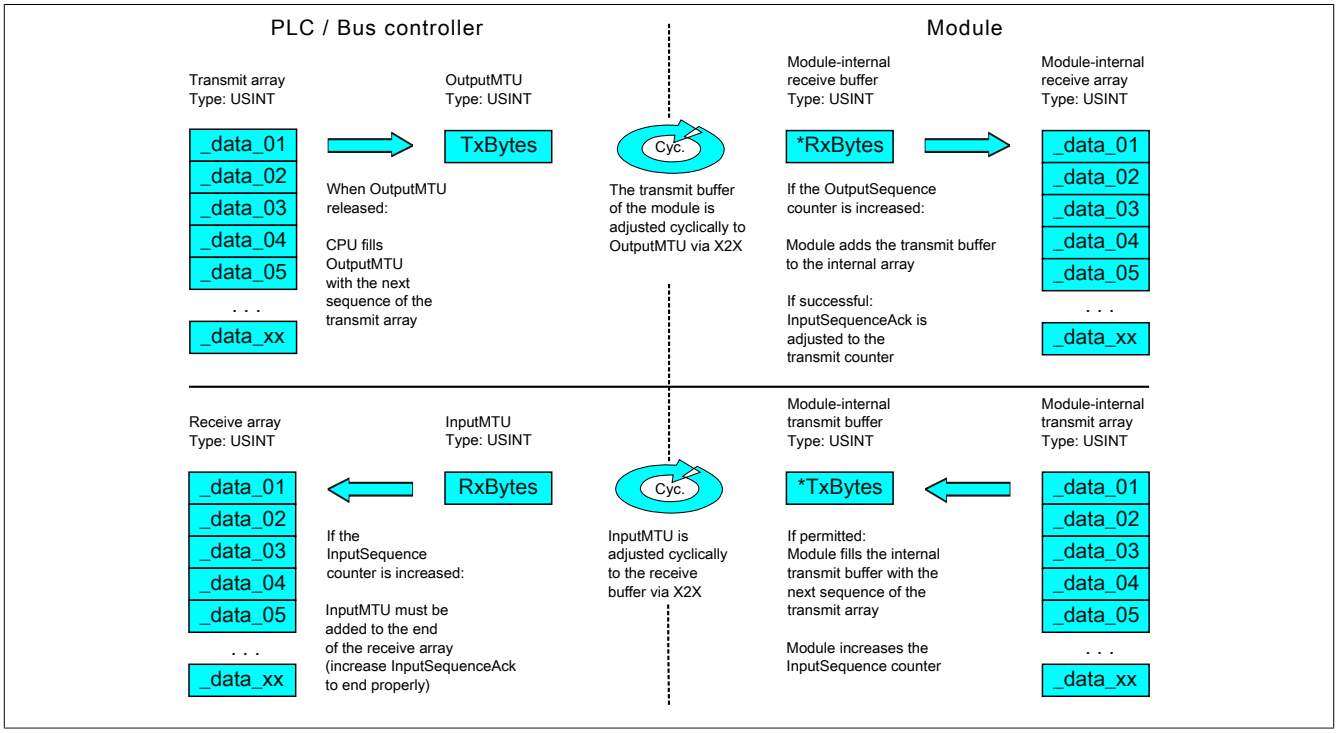


Figure 295: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.18.5.8.10.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Format of input and output bytes

Name:

"Format of Flat stream" in Automation Studio

This function sets how the Flatstream input and output bytes (Tx or Rx bytes) are transferred.

- **packed variable:** Transfers data as an array
- **byte variables:**Transfers data as individual bytes

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

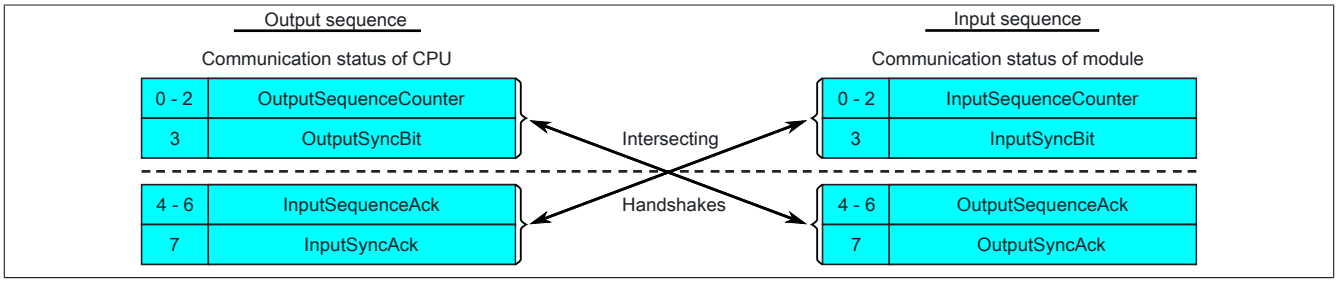


Figure 296: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

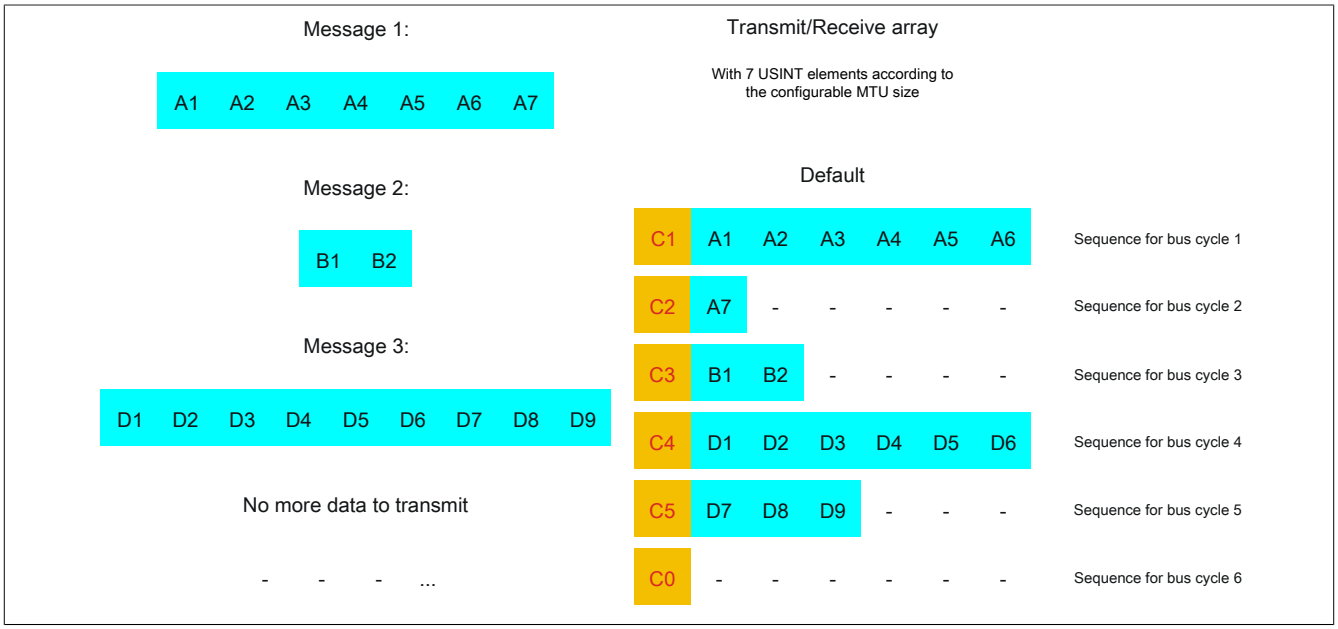


Figure 297: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 399: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 400: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

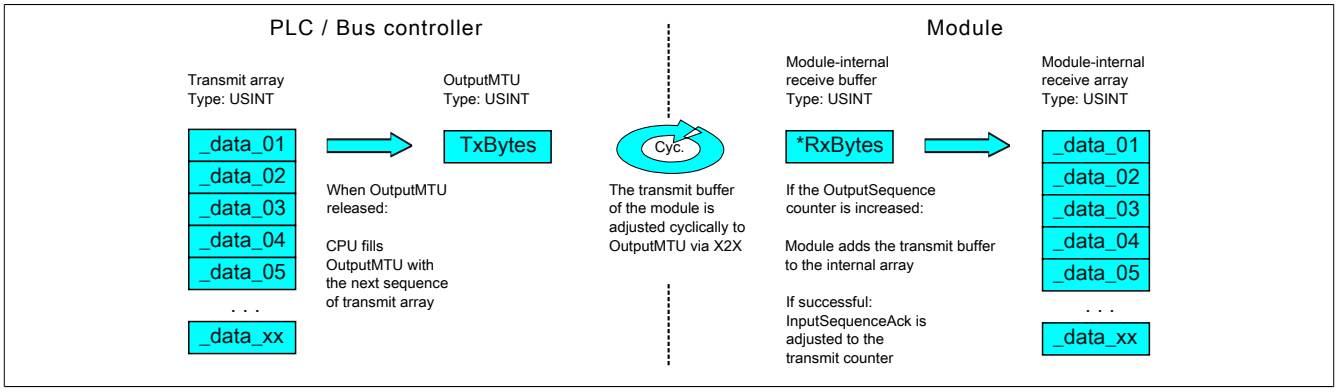


Figure 298: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

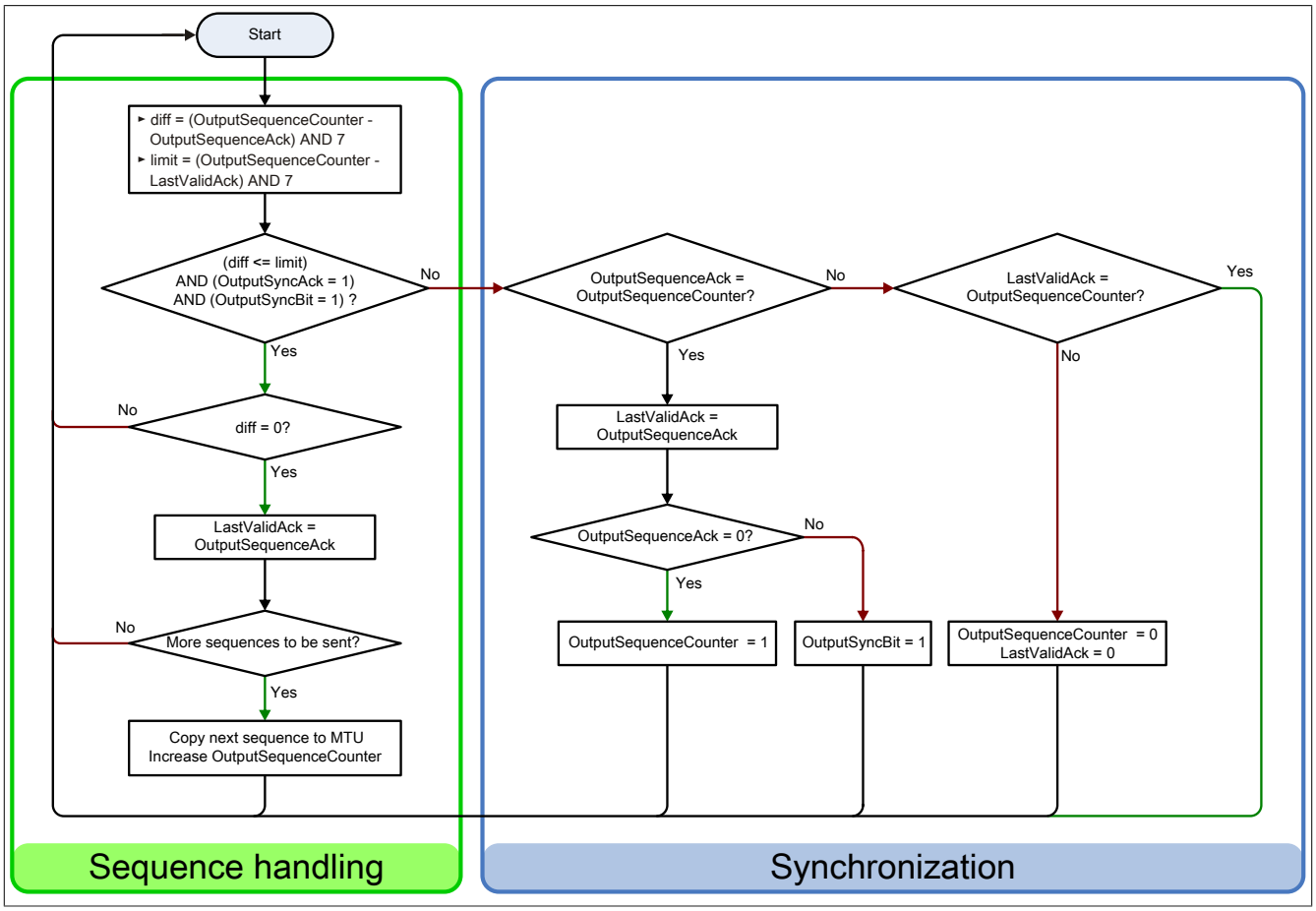


Figure 299: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

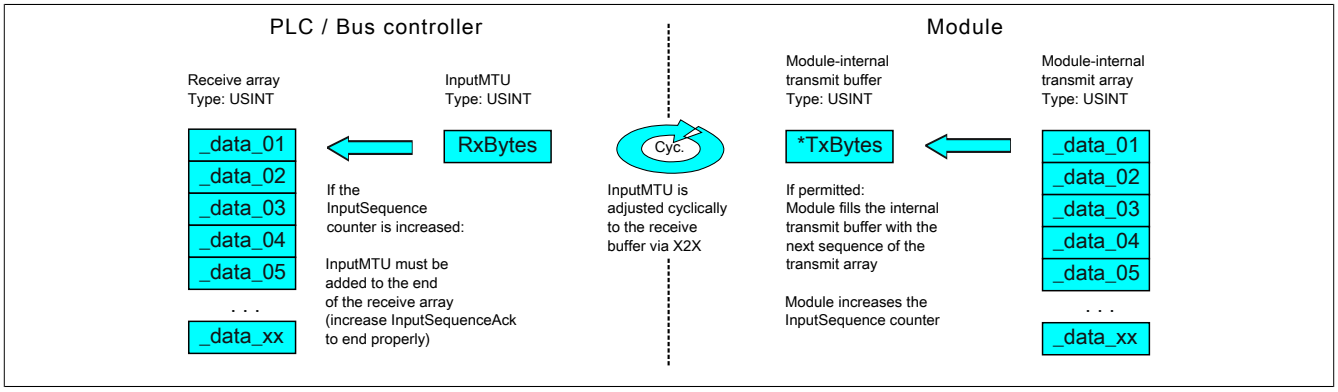


Figure 300: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

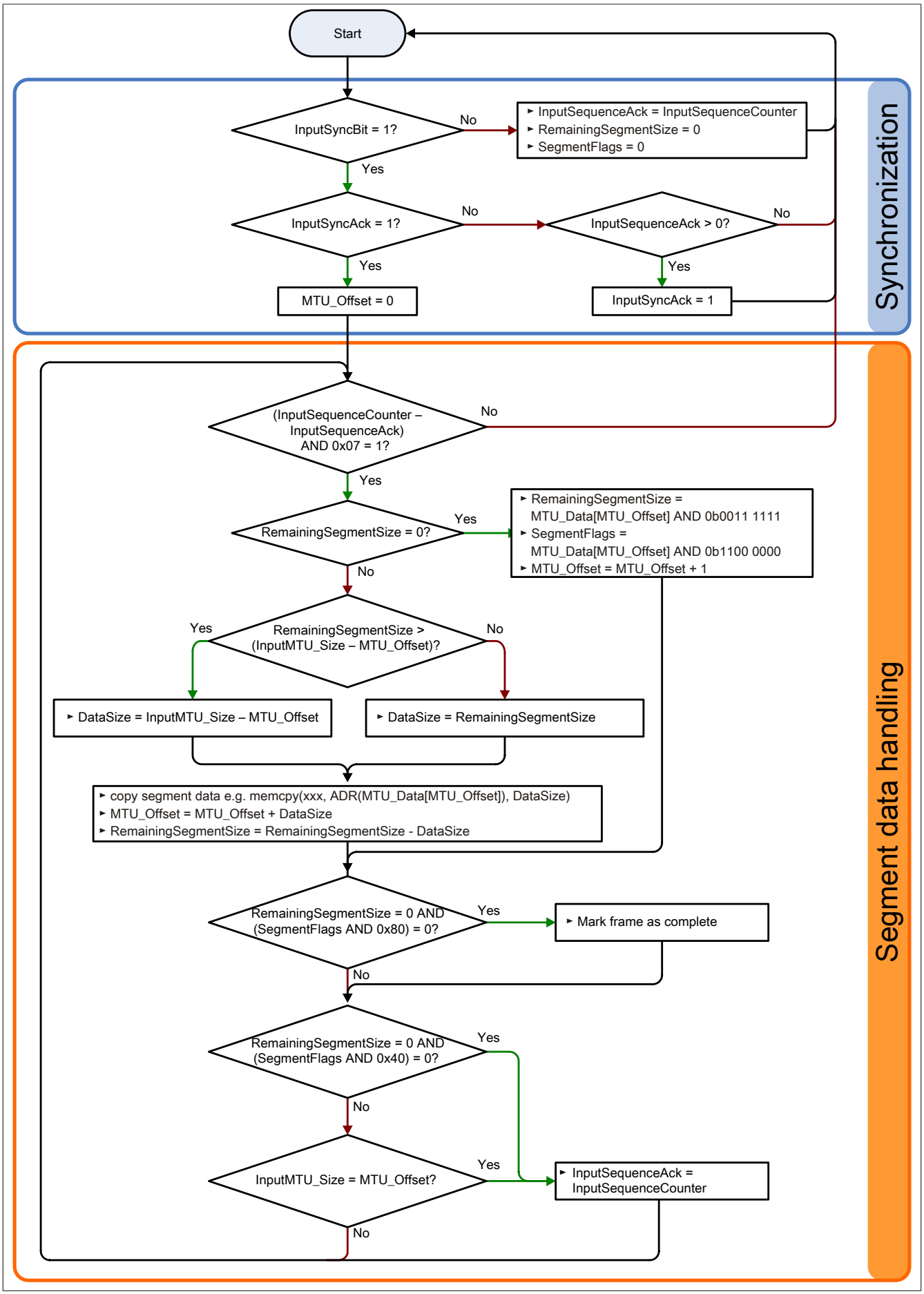


Figure 301: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

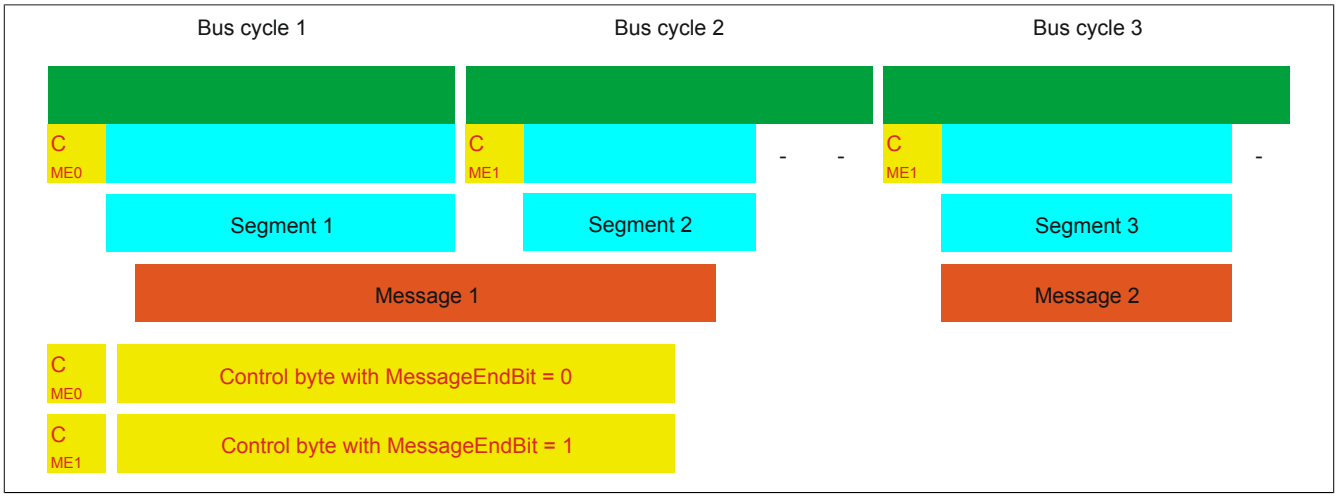


Figure 302: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

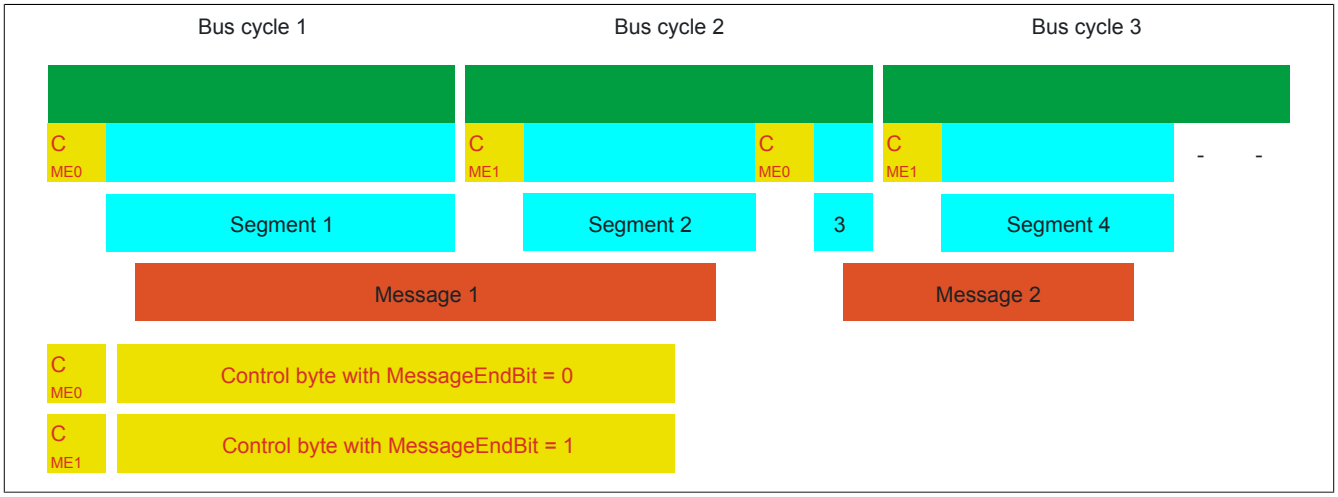


Figure 303: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

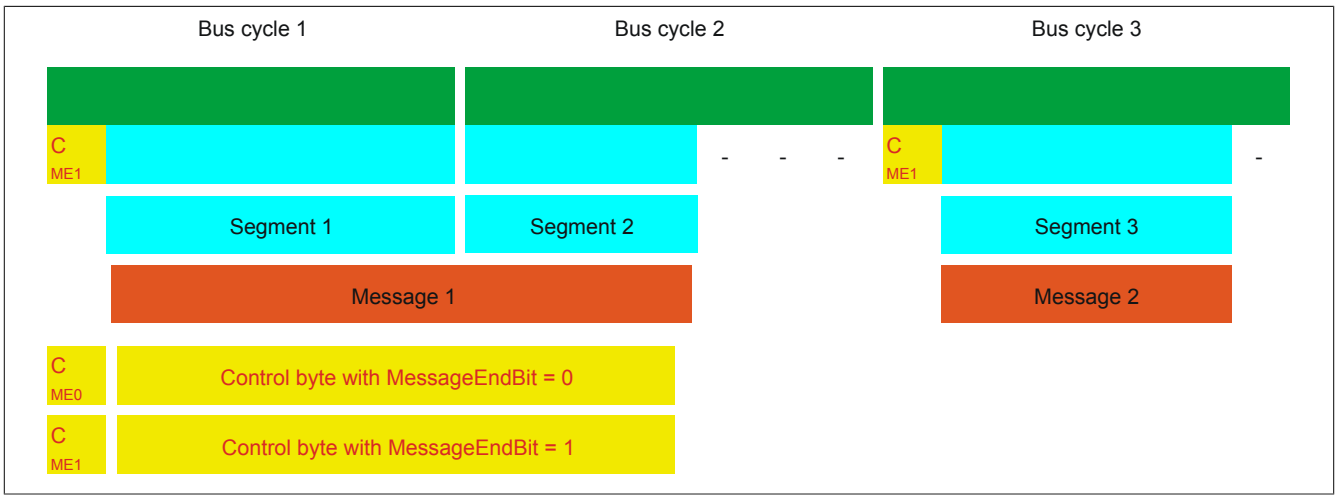


Figure 304: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

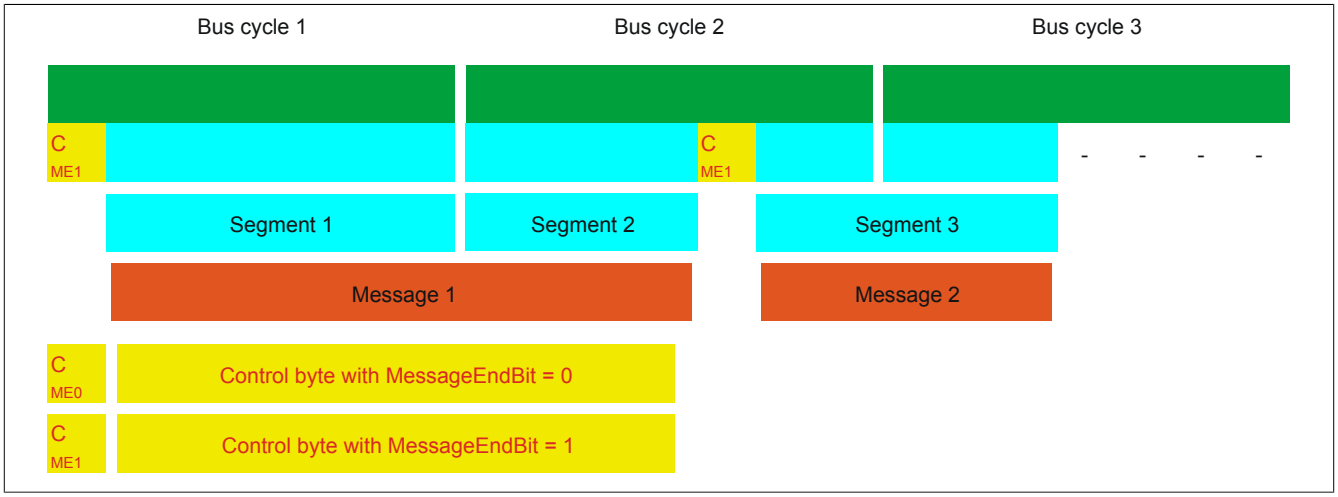


Figure 305: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

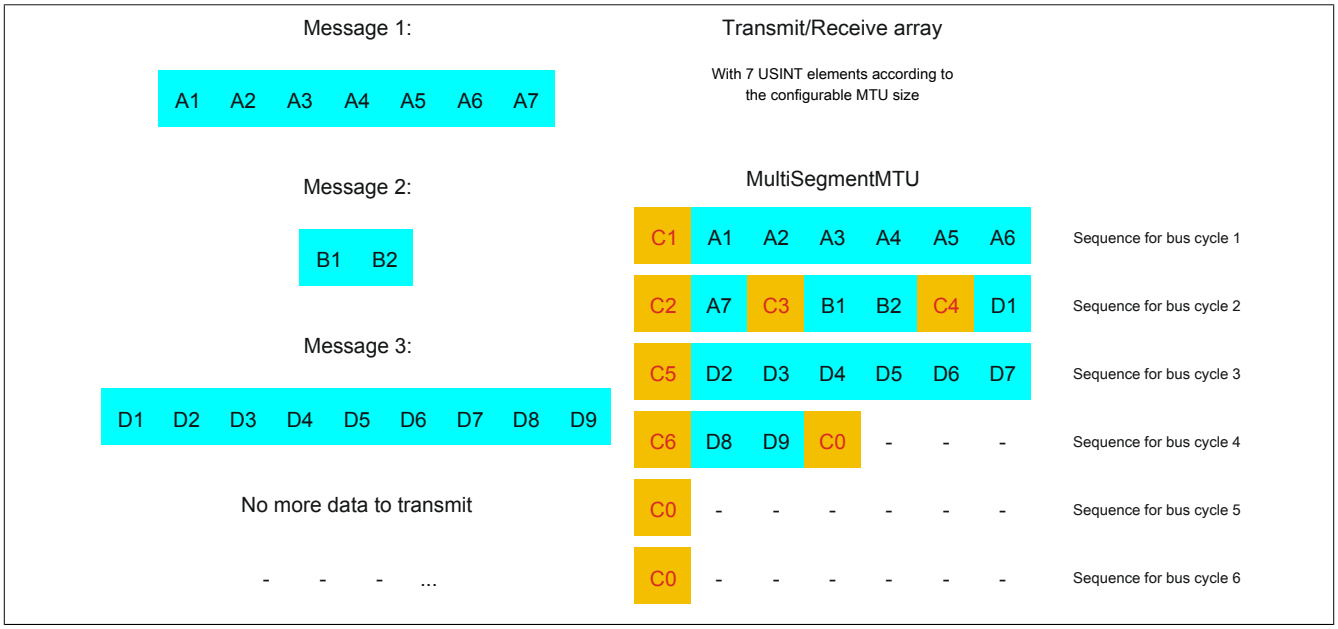


Figure 306: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 401: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 402: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

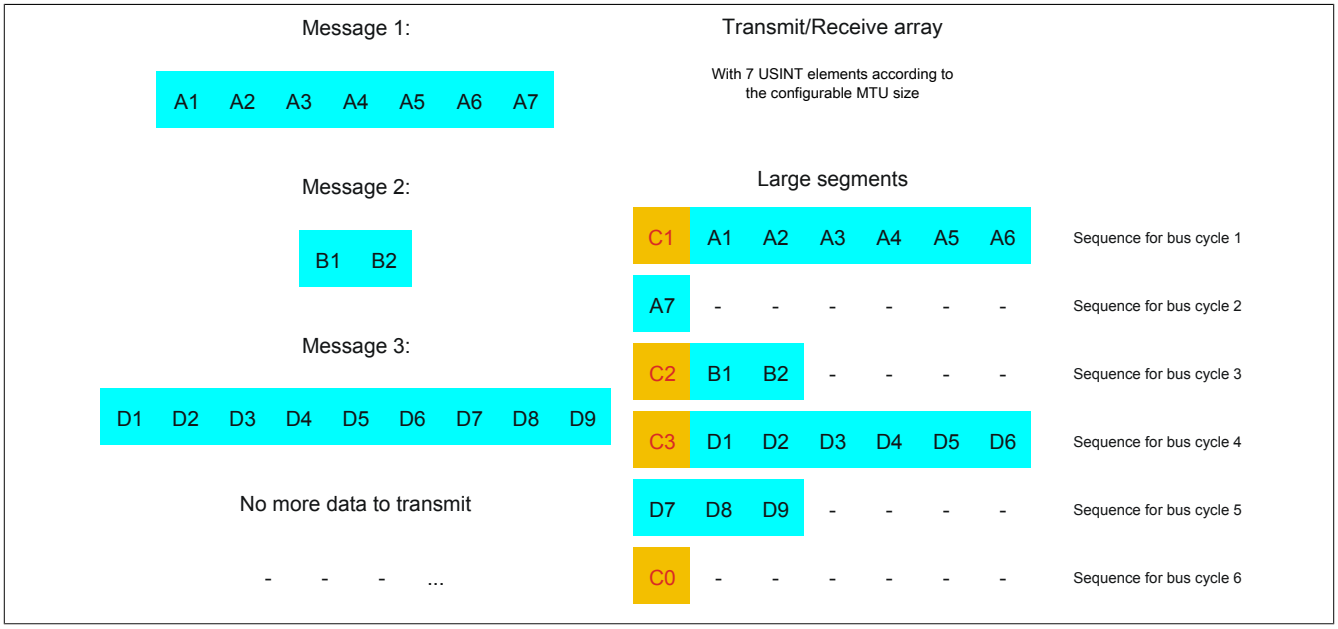


Figure 307: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 403: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

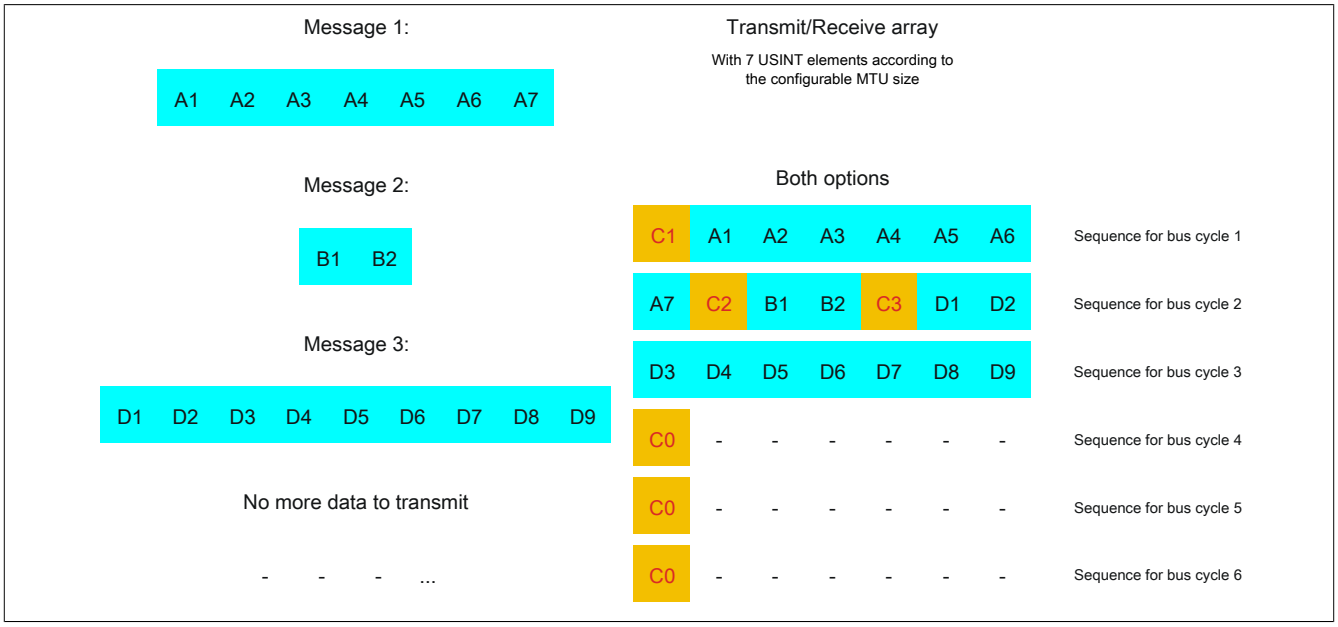


Figure 308: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 404: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.18.5.8.10.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

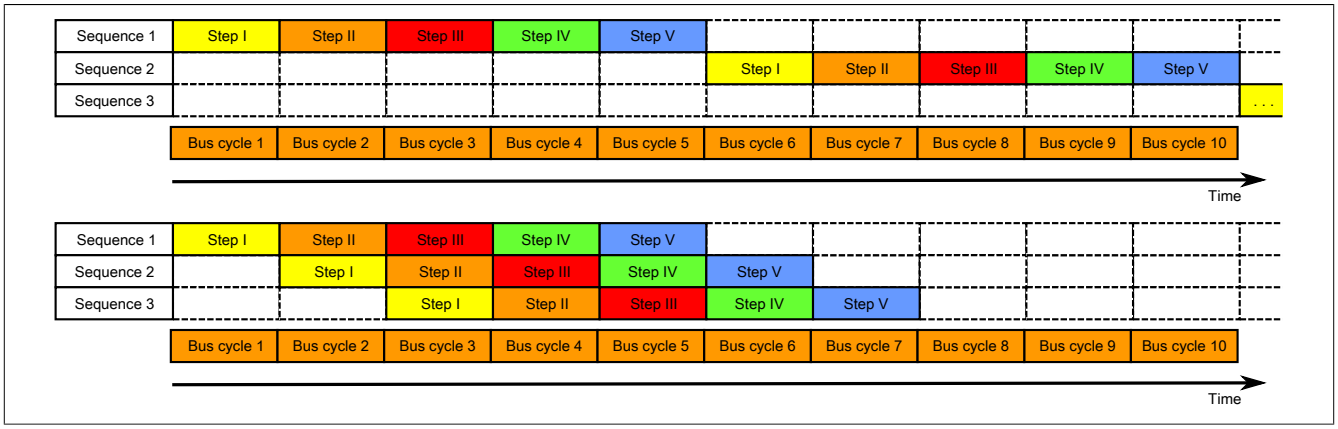


Figure 309: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

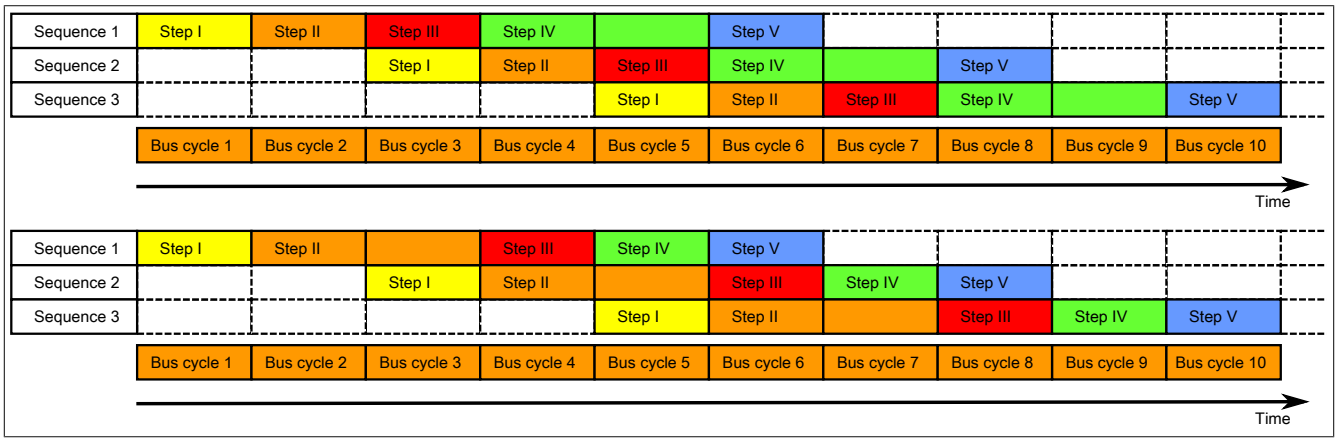


Figure 310: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

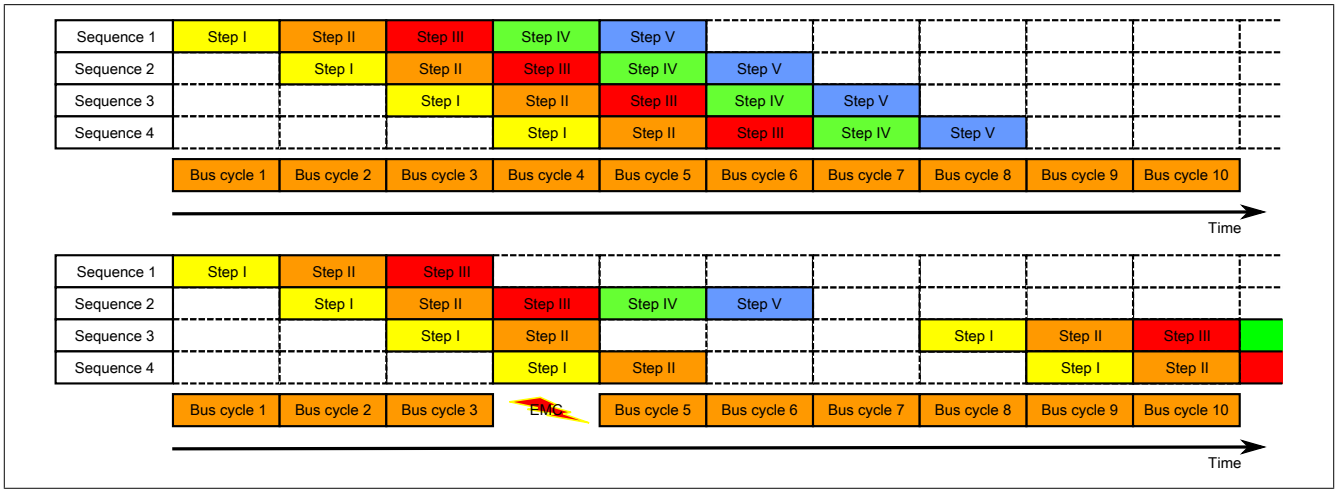


Figure 311: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.18.5.8.11 Serial with FlatStream

When using FlatStream communication, the module acts as a bridge between the X2X Link master and an intelligent field device connected to the module. FlatStream mode can be used for either point-to-point connections as well as for multidrop systems. Specific algorithms such as timeout and checksum monitoring are usually managed automatically. During normal operation, the user does not have access to these details.

In a serial network, the module is always the master (DTE). Various adjustments can be made to ensure that signals are transmitted without errors.
The user can, for example, define a handshake algorithm or set the baud rate in order to adapt the transmission quality to the requirements of the application.

Operation

When using FlatStream, the general structure of the FlatStream frame must be maintained.

Input/Output sequence	Tx/Rx bytes	
(unchanged)	Control byte (unchanged)	Serial frame (without hand-shake or similar measures)

4.18.5.8.12 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

4.18.5.8.13 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.18.5.8.14 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.18.6 X20(c)CS1030

4.18.6.1 General information

In addition to the standard I/O, complex devices often need to be connected. The X20CS communication modules are intended precisely for cases like this. As normal X20 electronics modules, they can be placed anywhere on the remote backplane.

- RS485/RS422 interface for serial, remote connection of complex devices to the X20 system
- Integrated terminating resistor

4.18.6.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.18.6.3 Order data

Model number	Short description	Figure
	X20 electronics module communication	
X20CS1030	X20 interface module, 1 RS422/485 interface, max. 115.2 kbit/s	
X20cCS1030	X20 interface module, coated, 1 RS422/485 interface, max. 115.2 kbit/s	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 405: X20CS1030, X20cCS1030 - Order data

4.18.6.4 Technical data

Product ID	X20CS1030	X20cCS1030
Short description		
Communication module	1x RS485/RS422	
General information		
B&R ID code	0x1FD0	0xE500
Status indicators	Data transfer, terminating resistor, operating status, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Data transfer	Yes, using status LED	
Terminating resistor	Yes, using status LED	
Power consumption		
Bus	0.01 W	
Internal I/O	1.44 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
IF1 - Bus	Yes	
IF1 - I/O supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	-
GOST-R	Yes	
Interfaces		
IF1 interface		
Signal	RS485/RS422	
Design	Connection made using 12-pin X20TB12 terminal block	
Max. distance	1200 m	
Transfer rate	Max. 115.2 kbit/s	
FIFO	1 kB	
Terminating resistor	Integrated in the module	
Controller	UART type 16C550 compatible	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB06 or X20T-B12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm	

Table 406: X20CS1030, X20cCS1030 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.18.6.5 LED status indicators

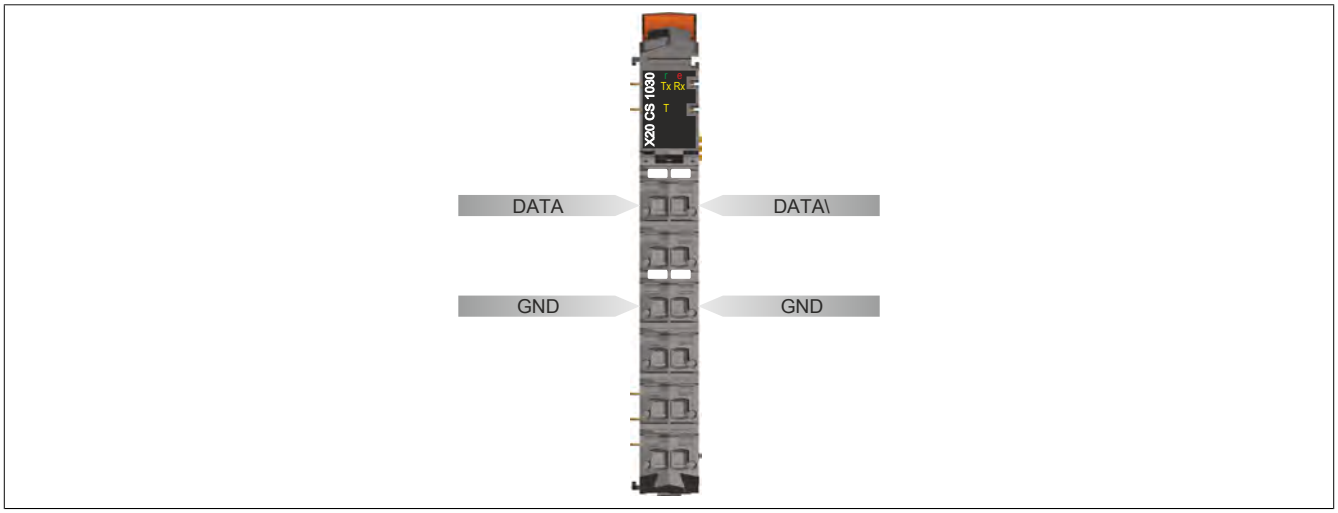
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	An I/O error has occurred, see 4.18.5.8.9.1 "Error message status bits"
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	Tx	Yellow	On	The module transmits data via the RS485/RS422 interface
	Rx	Yellow	On	The module receives data via the RS485/RS422 interface
	T	Yellow	On	Terminating resistor integrated in the module switched on

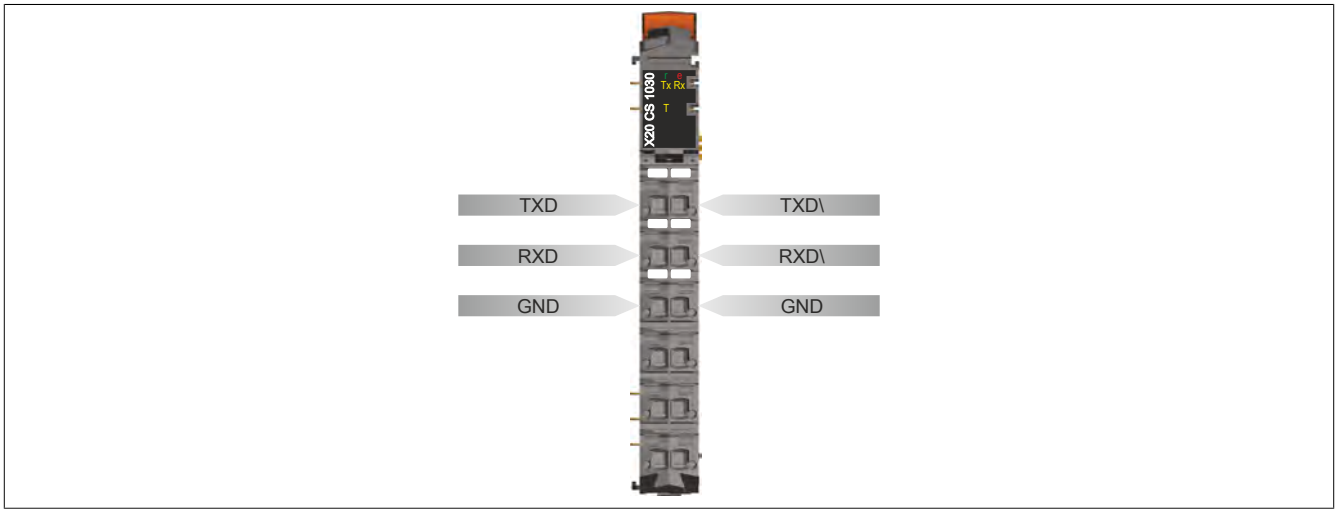
1) Depending on the configuration, a firmware update can take up to several minutes.

4.18.6.6 Pinout

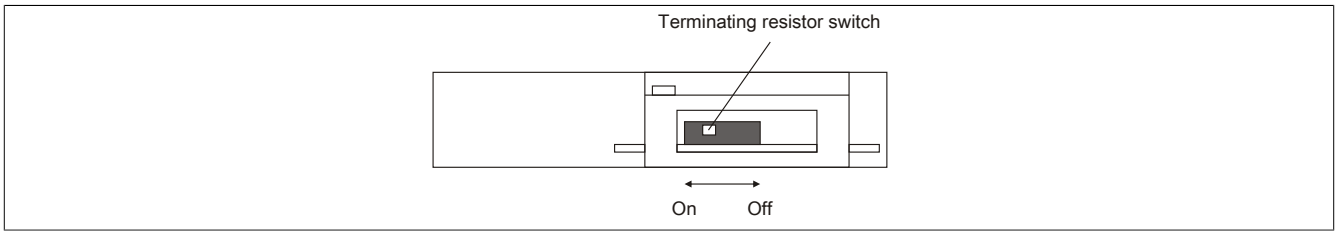
RS485 mode



RS422 mode



4.18.6.7 Terminating resistor

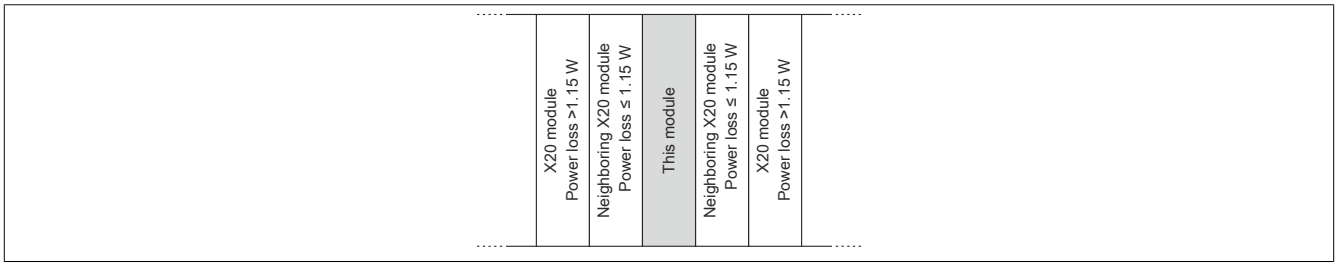


A terminating resistor is integrated in the communication module. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "T" LED.

4.18.6.8 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.18.6.9 Register description

4.18.6.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.18.6.9.2 Function model 2 - Stream and Function model 254 - Cyclic stream

The "Stream" and "Cyclic stream" function models use a module-specific driver for the operating system. The interface can be controlled using the "DVFrame" library and be reconfigured at runtime.

Function model - Stream

In the "Stream" function model, the CPU communicates with the module acyclically. The interface is relatively convenient, but the timing is very imprecise.

Function model - Cyclic stream

The "Cyclic stream" function model was implemented later. From the application's point of view, there is no difference between the "Stream" and "Cyclic stream" function models. Internally, however, the cyclic I/O registers are used to ensure that communication follows deterministic timing.

Information:

- **In order to use the "Stream" and "Cyclic stream" function models, you must be using B&R controllers of the type "SG4".**

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Module – Configuration						
-	AsynSize	-				
Status messages – Configuration						
50	CfO_RxStateIgnoreMask	UINT				•
6273	CfO_ErrorID0007	USINT				•
Status messages – Communication						
6145	ErrorByte	USINT	•			
	StartBitError	Bit 0				
	StopBitError	Bit 1				
	ParityError	Bit 2				
	RXoverrun	Bit 3				
6209	ErrorQuitByte	USINT			•	
	QuitStartBitError	Bit 0				
	QuitStopBitError	Bit 1				
	QuitParityError	Bit 2				
	QuitRXoverrun	Bit 3				

4.18.6.9.3 Function model 254 - FlatStream

The "FlatStream" function model provides independent communication between an X2X Link master and the module. This interface was implemented as a separate function model for the module. Serial information is transferred via cyclic input and output registers. The sequence and control bytes are used to control this data stream (see 4.3.7.10.8 "FlatStream communication").

When using the Flatstream function model, the user can choose whether to use the "AsFltGen" library in AS for implementation or to adapt Flatstream handling directly to the individual requirements of the application.

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Serial interface – Configuration						
1	phyMode	USINT				•
12	phyBaud	UDINT				•
3	phyData	USINT				•
5	phyStop	USINT				•
7	phyParity	USINT				•
Handshake – Configuration						
66	rxlLock	UINT				•
70	rxlUnlock	UINT				•
34	hssXOn	UINT				•
38	hssXOff	UINT				•
42	hssPeriod	UINT				•
Frame – Configuration						
74	rxCto	UINT				•
106	txCto	UINT				•
78	rxEomSize	UINT				•
110	txEomSize	UINT				•
Index * 4 + 82	rxEomCharN (Index N = 0 to 3)	UINT				•
Index * 4 + 114	txEomCharN (Index N = 0 to 3)	UINT				•
Status messages – Configuration						
50	CfO_RxStateIgnoreMask	UINT				•
6273	CfO_ErrorID0007	USINT				•
Status messages – Communication						
6145	ErrorByte	USINT	•			
	StartBitError	Bit 0				
	StopBitError	Bit 1				
	ParityError	Bit 2				
	RXoverrun	Bit 3				
6209	ErrorQuitByte	USINT			•	
	QuitStartBitError	Bit 0				
	QuitStopBitError	Bit 1				
	QuitParityError	Bit 2				
	QuitRXoverrun	Bit 3				
FlatStream						
225	OutputMTU	USINT				•
227	InputMTU	USINT				•
229	Mode	USINT				•
231	Forward	USINT				•
238	ForwardDelay	UINT				•
128	InputSequence	USINT	•			
Index + 128	RxByteN (Index N = 1 to 27)	USINT	•			
160	OutputSequence	USINT			•	
Index + 160	TxByteN (Index N = 1 to 27)	USINT			•	

4.18.6.9.4 Function model 254 - Bus controller

The "Bus controller" function model is a reduced form of the "FlatStream" function model. Instead of up to 27 Tx / Rx bytes, a maximum of 7 Tx / Rx bytes can be used.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Serial interface – Configuration							
257	-	phyMode_CANIO	USINT				●
268	-	phyBaud_CANIO	UDINT				●
259	-	phyData_CANIO	USINT				●
261	-	phyStop_CANIO	USINT				●
263	-	phyParity_CANIO	USINT				●
Handshake – Configuration							
322	-	rxILock_CANIO	UINT				●
326	-	rxIUnlock_CANIO	UINT				●
290	-	hssXOn_CANIO	UINT				●
294	-	hssXOff_CANIO	UINT				●
298	-	hssPeriod_CANIO	UINT				●
Frame – Configuration							
330	-	rxCto_CANIO	UINT				●
362	-	txCto_CANIO	UINT				●
334	-	rxEomSize_CANIO	UINT				●
366	-	txEomSize_CANIO	UINT				●
Index*4 + 338	-	rxEomCharN (N = 0 to 3)	UINT				●
Index*4 + 370	-	txEomCharN (N = 0 to 3)	UINT				●
Status messages – Configuration							
306	-	CfO_RxStateIgnoreMask_CANIO	UINT				●
6273	-	CfO_ErrorID0007	USINT				●
Status messages – Communication							
6145	-	ErrorByte	USINT		●		
		StartBitError	Bit 0				
		StopBitError	Bit 1				
		ParityError	Bit 2				
		RXoverrun	Bit 3				
6209	-	ErrorQuitByte	USINT				●
		QuitStartBitError	Bit 0				
		QuitStopBitError	Bit 1				
		QuitParityError	Bit 2				
		QuitRXoverrun	Bit 3				
FlatStream							
225	-	OutputMTU	USINT				●
227	-	InputMTU	USINT				●
229	-	Mode	USINT				●
231	-	Forward	USINT				●
238	-	ForwardDelay	UINT				●
128	0	InputSequence	USINT	●			
Index + 128	Index	RxByteN (Index N = 1 to 7)	USINT	●			
160	0	OutputSequence	USINT			●	
Index + 160	Index	TxByteN (Index N = 1 to 7)	USINT			●	

1) The offset specifies the position of the register within the CAN object.

4.18.6.9.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.18.6.9.5 Serial interface – Configuration

The user has to configure 5 registers to operate the serial interface.

4.18.6.9.5.1 Mode_IF

Name:
phyMode
phyMode_CANIO

This register is used to determine the current operating mode of the interface.

Enabling the interface is only permitted after complete configuration of the other registers. If parameters need to be changed, the interface must first be disabled.

Data type	Value	Description
USINT	0	Interface disabled (default)
	4	RS422 interface enabled[1)]
	5	RS422 interface enables as a bus[2)]
	6	RS485 interface enabled with echo
	7	RS485 interface enabled without echo

1) Connection between 2 stations
2) Connections between multiple stations possible. Transmit lines connected as with RS485 TriState.

4.18.6.9.5.2 Baudrate_IF

Name:
phyBaud
phyBaud_CANIO

This register is used to set the baud rate of the interface in bit/s.

Data type	Value	Description
UDINT	1200	1.2 kbaud
	2400	2.4 kbaud
	4800	4.8 kbaud
	9600	9.6 kbaud
	19200	19.2 kbaud
	38400	38.4 kbaud
	57600	57.6 kbaud
	115200	115.2 kbaud

4.18.6.9.5.3 Databit_IF

Name:
phyData
phyData_CANIO

This register is used to specify the number of bits to be transferred for each character.

Data type	Value	Description
USINT	7	7 data bits
	8	8 data bits (default)

4.18.6.9.5.4 Stoppbit_IF

Name:
phyStop
phyStop_CANIO

This register is used to define the number of stop bits.

Data type	Value	Description
USINT	2	1 stop bit (default)
	4	2 stop bits

4.18.6.9.5.5 Parity_IF

Name:
phyParity
phyParity_CANIO

This register is used to define the parity check type. Possible values are ASCII coded.

Data type	Value	Description
USINT	48	"0" - (low) bit is always 0
	49	"1" - (high) bit is always 1
	69	"E" - (even) even parity (default)
	78	"N" - (no) no bit
	79	"O" - (odd) odd parity

4.18.6.9.6 Handshake - Configuration

In order to guarantee that serial communication runs smoothly, the size of the receive buffer in the module must be known. In addition, the user can configure a software or hardware handshake algorithm.

4.18.6.9.6.1 Locking the receive buffer

Name:
rxlLock
rxlLock_CANIO

This register is used to configure the upper threshold of the receive buffer.

The two registers "Lock" and "Unlock" can be used for "flow control" monitoring of the communication. If the amount of data from the module input exceeds the "Lock" register value, flow control switches to the "passive" state. To return to the "active" or "ready" state, the amount of data in the receive buffer must fall under the default value of the "Unlock" register.

Information:

These registers simulate the behavior of a Schmitt trigger, so the value of the "Lock" register must be greater than the value of the "Unlock" register.

Data type	Value	Description
UINT	0 to 4095	Upper threshold of the receive buffer (default = 1024)

4.18.6.9.6.2 Unlocking the receive buffer

Name:
rxlUnlock
rxlUnlock_CANIO

This register is used to configure the lower threshold of the receive buffer.

The two registers "Lock" and "Unlock" can be used for "flow control" monitoring of the communication. If the amount of data from the module input exceeds the "Lock" register value, flow control switches to the "passive" state. To return to the "active" or "ready" state, the amount of data in the receive buffer must fall under the default value of the "Unlock" register.

Information:

These registers simulate the behavior of a Schmitt trigger, so the value of the "Lock" register must be greater than the value of the "Unlock" register.

Data type	Value	Description
UINT	0 to 4095	Lower threshold of the receive buffer (default = 512)

4.18.6.9.6.3 Turn on software handshake

Name:
hssXOn
hssXOn_CANIO

This register can be used to configure the XOn character. The value 17 is the default, but any other value can also be configured.

The two registers "XOn" and "XOff" can be used to initiate a software handshake for flow control. When doing so, a valid ASCII character must be configured in both registers.

Data type	Value	Description
UINT	0 to 255	XOn ASCII character
	65535	No software handshake (default)

4.18.6.9.6.4 Turn off software handshake

Name:
hssXOff
hssXOff_CANIO

This register can be used to configure the XOff character. The value 19 is the default, but any other value can also be configured.

The two registers "XOn" and "XOff" can be used to initiate a software handshake for flow control. When doing so, a valid ASCII character must be configured in both registers.

Data type	Value	Description
UINT	0 to 255	XOff ASCII character
	65535	No software handshake (default)

4.18.6.9.6.5 Handshake repetition

Name:
hssPeriod
hssPeriod_CANIO

When using a software handshake, some applications require periodic repetition of the current status. The repeat time can be defined in this register in ms for this purpose.

Data type	Value	Description
UINT	0	Automatic status repeat disabled
	500 to 10000	Repeat time in ms (default = 5000)

4.18.6.9.7 Frame - Configuration

Different message termination codes can be specified in order to correctly create transmitted Tx frames and correctly interpret received Rx frames.

4.18.6.9.7.1 Terminating when a receive timeout occurs

Name:
rxCto
rxCto_CANIO

This register is used to set the duration until a receive timeout is triggered.

The message is considered to be terminated when nothing is transfered for the specified duration.
The time is specified here in characters to ensure that it is independent of the transfer rate. The number of characters is then multiplied by the time needed to transfer a character.

Data type	Value	Description
UINT	0	Function disabled
	1 to 65535	Receive timeout in characters (default = 4)

4.18.6.9.7.2 Terminating when a transmit timeout occurs

Name:
txCto
txCto_CANIO

This register is used to set the duration until a transmit timeout is triggered.

The message is considered to be terminated when nothing is transfered for the specified duration.
The time is specified here in characters to ensure that it is independent of the transfer rate. The number of characters is then multiplied by the time needed to transfer a character.

Data type	Value	Description
UINT	0	Function disabled
	1 to 65535	Transmit timeout in characters (default = 5)

4.18.6.9.7.3 Maximum number of bytes received

Name:
rxEomSize
rxEomSize_CANIO

These registers configure the maximum number of bytes in the receive frame.

The message is considered to be ended as soon as a frame with the specified size in bytes is transferred. The longest possible frame length is the size of the 4096-byte receive buffer. Larger frames cause the Receive Overrun error.

Data type	Value	Description
UINT	0	Function disabled
	1 to 4096	Configurable receive frame length in characters (default = 256)

4.18.6.9.7.4 Maximum number of bytes transmitted

Name:
txEomSize
txEomSize_CANIO

These registers configure the maximum number of bytes in the transmit frame.

The message is considered to be ended as soon as a frame with the specified size in bytes is transferred. The longest possible frame length is the size of the 4096-byte transmit buffer. The configured transmit timeout is maintained after the frame has been sent.

Data type	Value	Description
UINT	0	Function disabled
	1 to 4096	Configurable transmit frame length in characters (default = 4096)

4.18.6.9.7.5 Define receive terminator

Name:
rxEomChar0 to rxEomChar3
rxEomChar0_CANIO to rxEomChar3_CANIO

It is possible to configure a receive terminator for all registers.

The message is considered to be terminated as soon as one of the defined characters is transferred.

Data type	Value	Description
UINT	0 to 255	Frame terminator (ASCII code)
	65535	Function disabled (default)

4.18.6.9.7.6 Define transmit terminator

Name:
txEomChar0 to txEomChar3
txEomChar0_CANIO to txEomChar3_CANIO

It is possible to configure a transmit terminator for all registers.

The message is considered to be terminated as soon as one of the defined characters is transferred.

Data type	Value	Description
UINT	0 to 255	Frame terminator (ASCII code)
	65535	Function disabled (default)

4.18.6.9.8 Status messages - Configuration

The status messages provide the user with information about the current situation in the downstream serial network.

4.18.6.9.8.1 Error detection setting

Name:
CfO_RxStateIgnoreMask
CfO_RxStateIgnoreMask_CANIO

This register has a direct effect on UART operation. Error detection in general can be disabled using the low byte. If error detection is not disabled, the high byte can be used to specify that a detected error should be interpreted as the end of the message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Reserved	0	
4	StartBitError	0	Detecting a faulty start bit
		1	Ignore
5	StopBitError	0	Detecting a faulty stop bit
		1	Ignore
6	ParityError	0	Detecting a faulty parity bit
		1	Ignore
7	RXoverrun	0	Detecting an overflow in the receive direction
		1	Ignore
8 - 11	Reserved	0	
12	StartBitError corresponds to the end of the frame (if bit 4 = 0)	0	Only display error inside the module
		1	Also signal end of frame
13	StopBitError corresponds to the end of the frame (if bit 5 = 0)	0	Only display error inside the module
		1	Also signal end of frame
14	ParityError corresponds to the end of the frame (if bit 6 = 0)	0	Only display error inside the module
		1	Also signal end of frame
15	RXoverrun corresponds to the end of the frame (if bit 7 = 0)	0	Only display error inside the module
		1	Also signal end of frame

4.18.6.9.8.2 Forward error to the application

Name:
CfO_ErrorID0007

If the UART inside the module reports an error, this byte can be used to specify which error messages are forwarded to the application.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name		Information
0	StartBitError	0	Ignore
		1	Indicating a faulty start bit
1	StopBitError	0	Ignore
		1	Indicating a faulty stop bit
2	ParityError	0	Ignore
		1	Indicating a faulty parity bit
3	RXoverrun	0	Ignore
		1	Indicating an overflow in the receive direction
4 - 7	Reserved	0	

4.18.6.9.9 Status messages - Communication

After configuration is completed, up to four status messages can be evaluated in the application.

4.18.6.9.9.1 Error message status bits

Name:
StartBitError
StopBitError
ParityError
RXoverrun

This register is used to transfer the individual bits that indicate an error. If a error occurs, the corresponding bit is set and maintained until it is acknowledged.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StartBitError	0	No error
		1	Start bit error occurred[1)]
1	StopBitError	0	No error
		1	Stop bit error occurred[1)]
2	ParityError	0	No error
		1	Parity bit error occurred[1)]
3	RXoverrun	0	No error
		1	Receive buffer overflow occurred[2)]
4 - 7	Reserved	0	

1) This error can result from things such as mismatched interface configurations or problems with the wiring.
2) This data point reports a receive buffer overrun. The buffer capacity on the module is exhausted and all subsequent data arriving at the interface is lost. An overrun always means that the data received on the module is not read fast enough by the higher-level system.
The solution here is to optimize the cycle times of all transfer routes and task classes involved and utilize the available handshake options.

4.18.6.9.9.2 Acknowledging the status bits

Name:
QuitStartBitError
QuitStopBitError
QuitParityError
QuitRXoverrun

This register is used to transfer the individual bits that acknowledge an indicated error state. After one of the bits has been set, it can be reset using the corresponding acknowledgment bit.
If the error is still actively pending, the error status bit is not deleted. The acknowledgment bit can only be reset if the error status bit is no longer set.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitStartBitError	0	No acknowledgment
		1	Acknowledge start bit error
1	QuitStopBitError	0	No acknowledgment
		1	Acknowledge stop bit error
2	QuitParityError	0	No acknowledgment
		1	Acknowledge parity bit error
3	QuitRXoverrun	0	No acknowledgment
		1	Acknowledge receive buffer overflow error
4 - 7	Reserved	0	

4.18.6.9.10 FlatStream communication

4.18.6.9.10.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

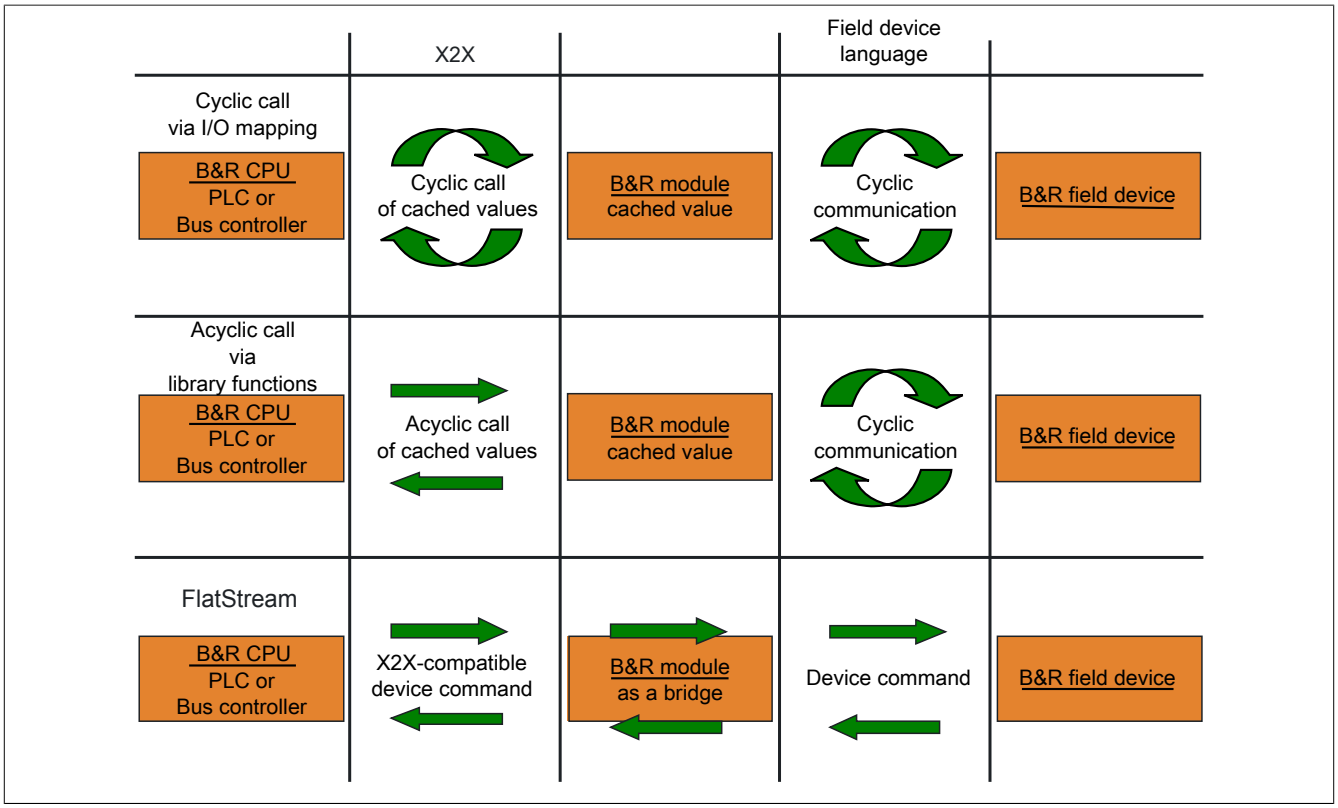


Figure 312: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.18.6.9.10.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.18.6.9.10.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

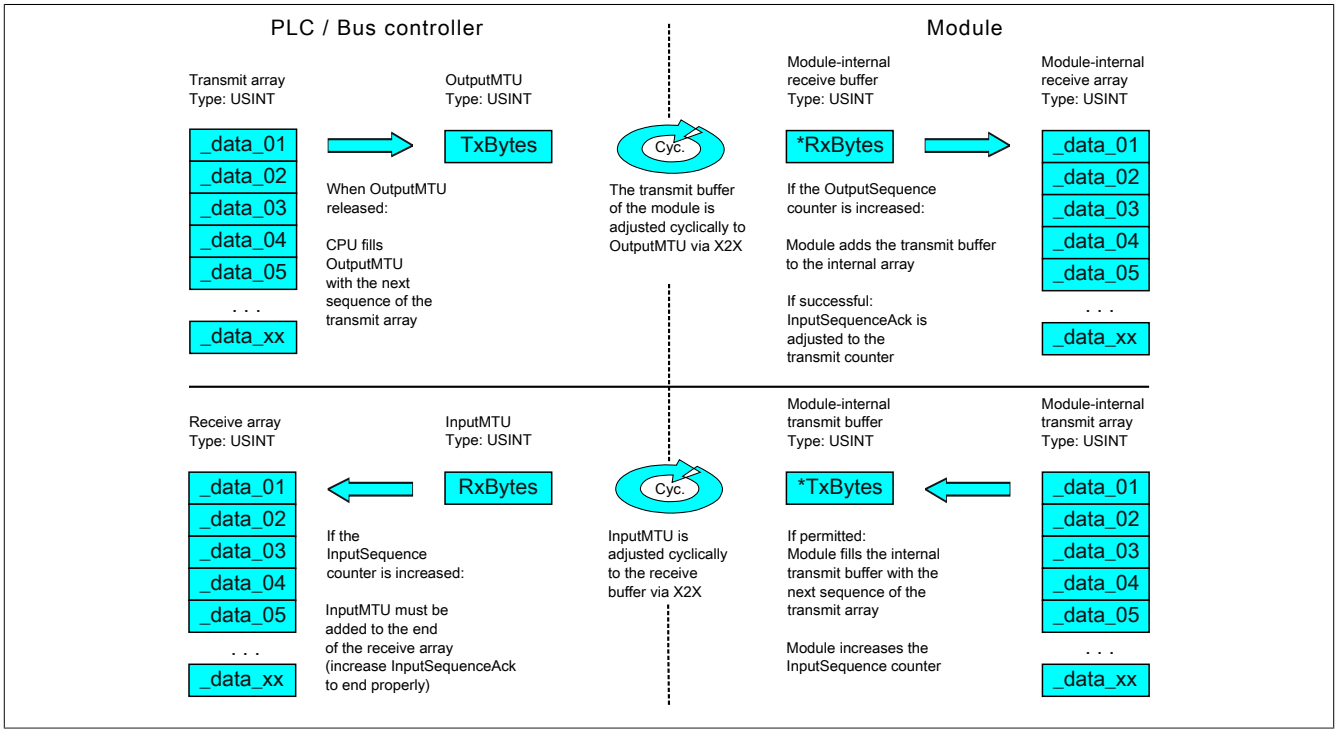


Figure 313: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.18.6.9.10.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Format of input and output bytes

Name:

"Format of Flat stream" in Automation Studio

This function sets how the Flatstream input and output bytes (Tx or Rx bytes) are transferred.

- **packed variable:** Transfers data as an array
- **byte variables:**Transfers data as individual bytes

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

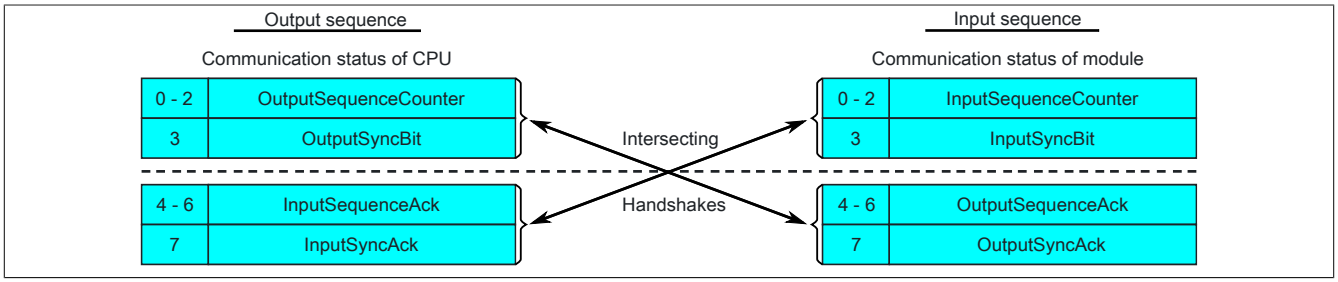


Figure 314: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

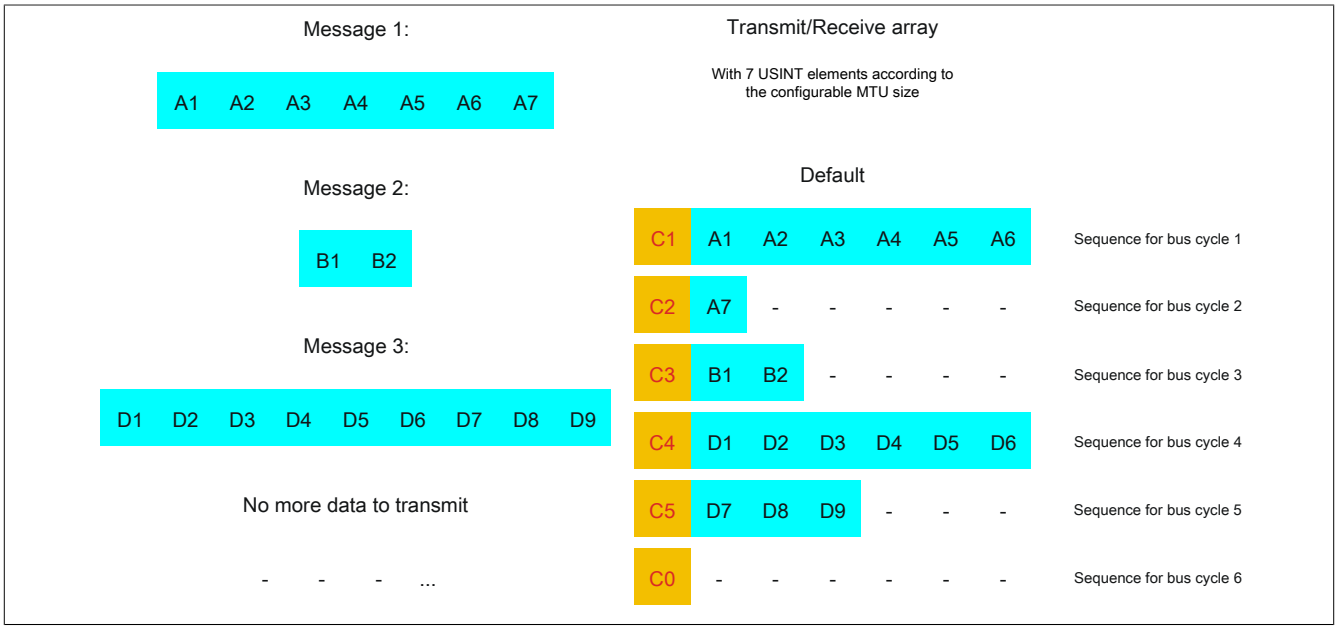


Figure 315: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 407: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 408: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

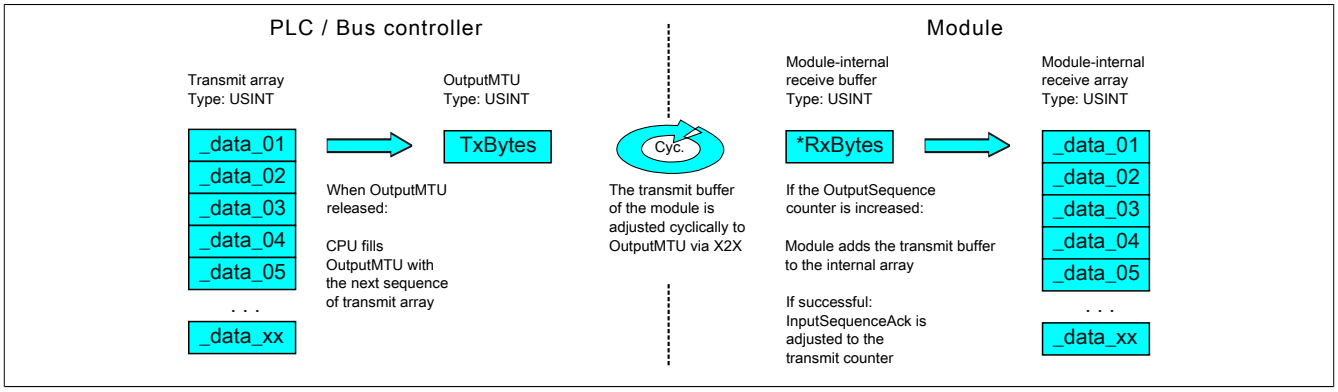


Figure 316: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

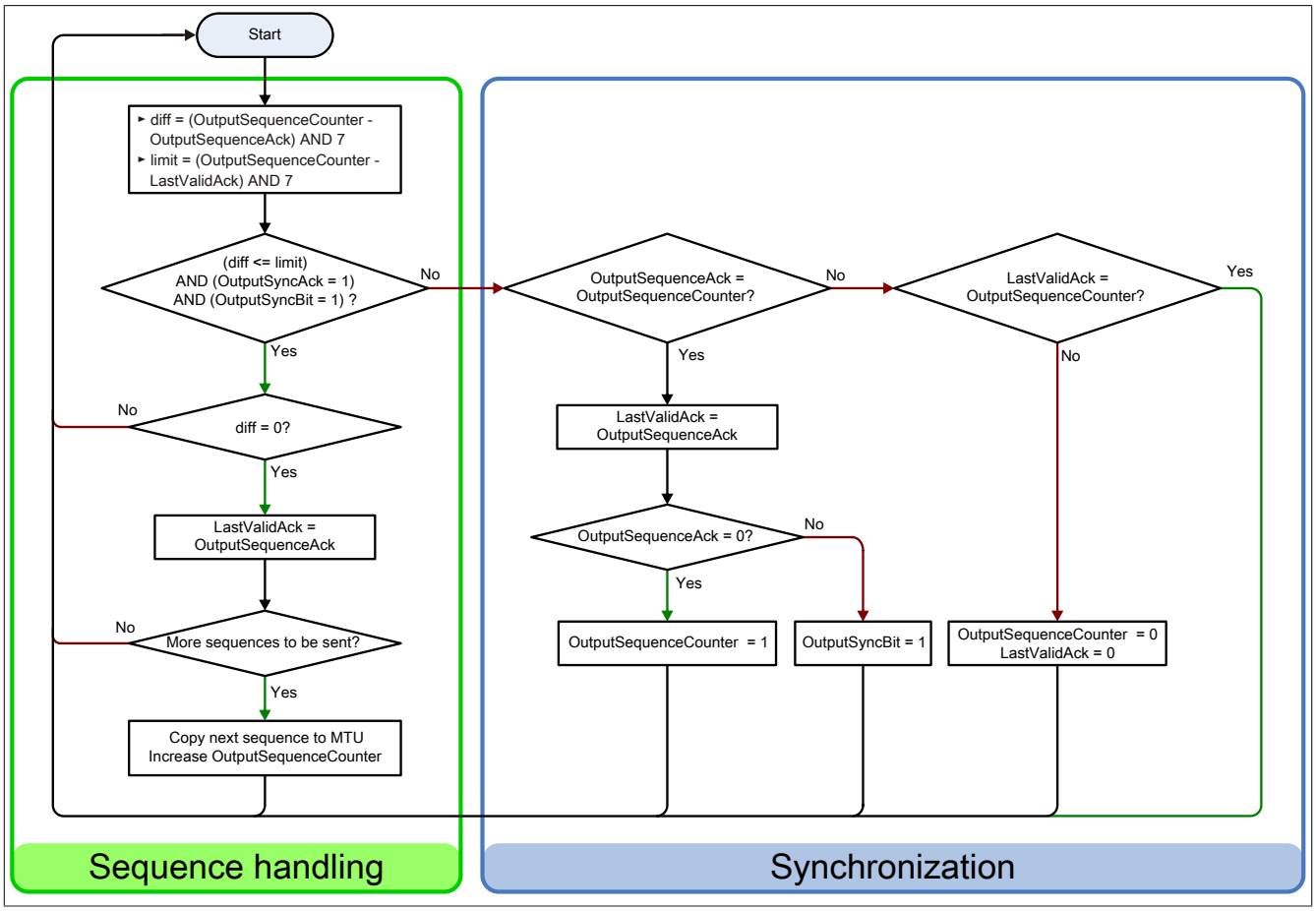


Figure 317: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

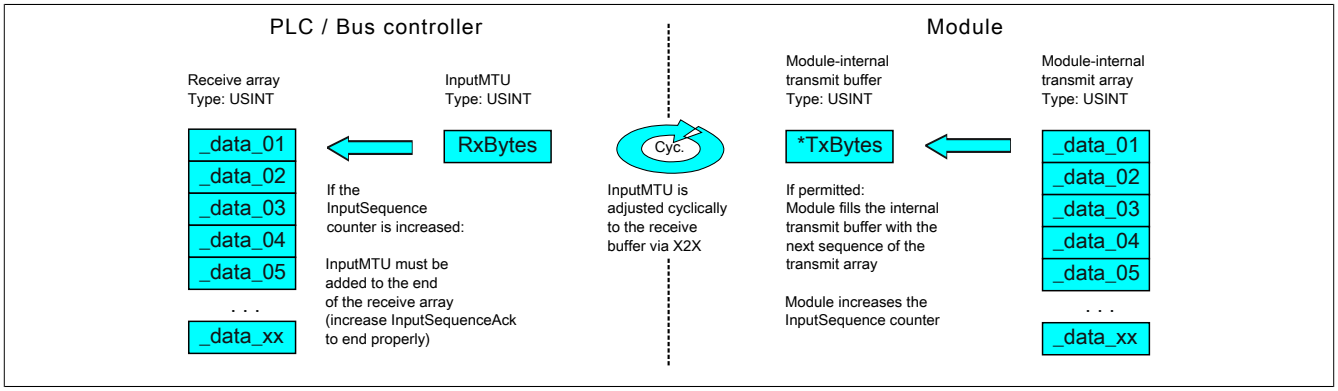


Figure 318: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

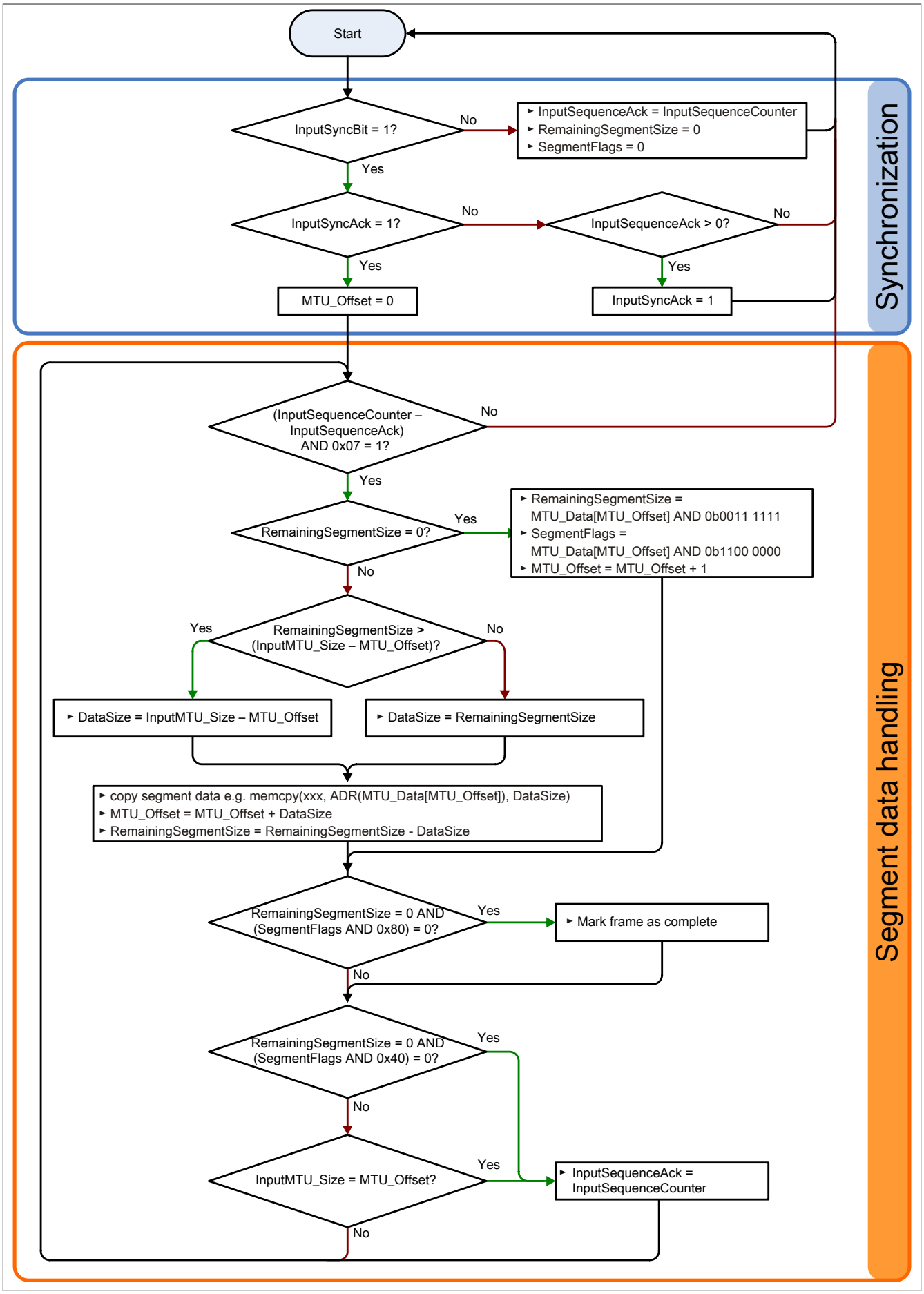


Figure 319: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

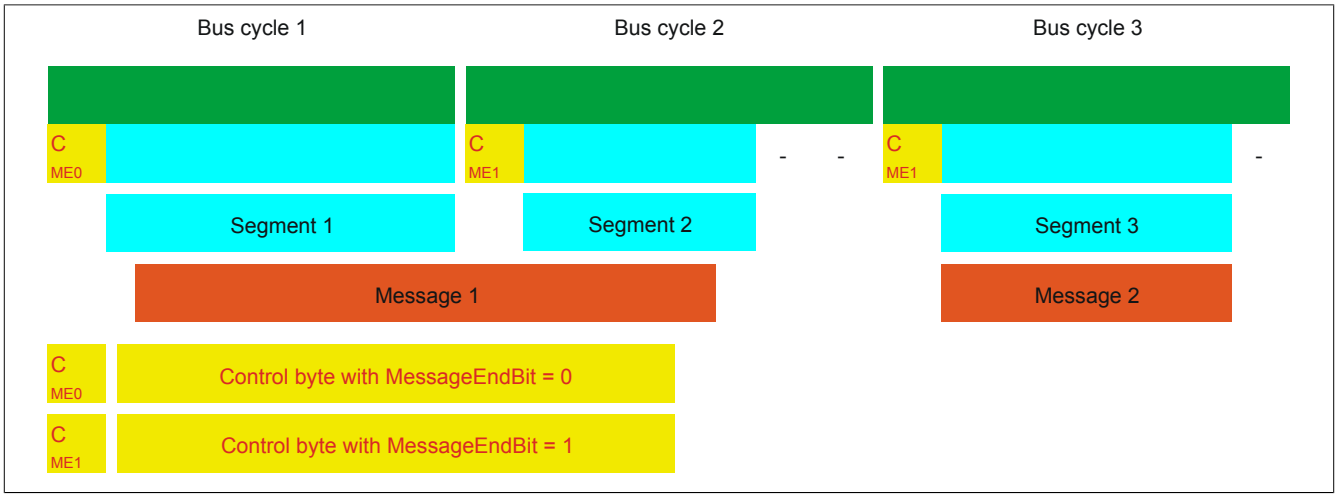


Figure 320: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

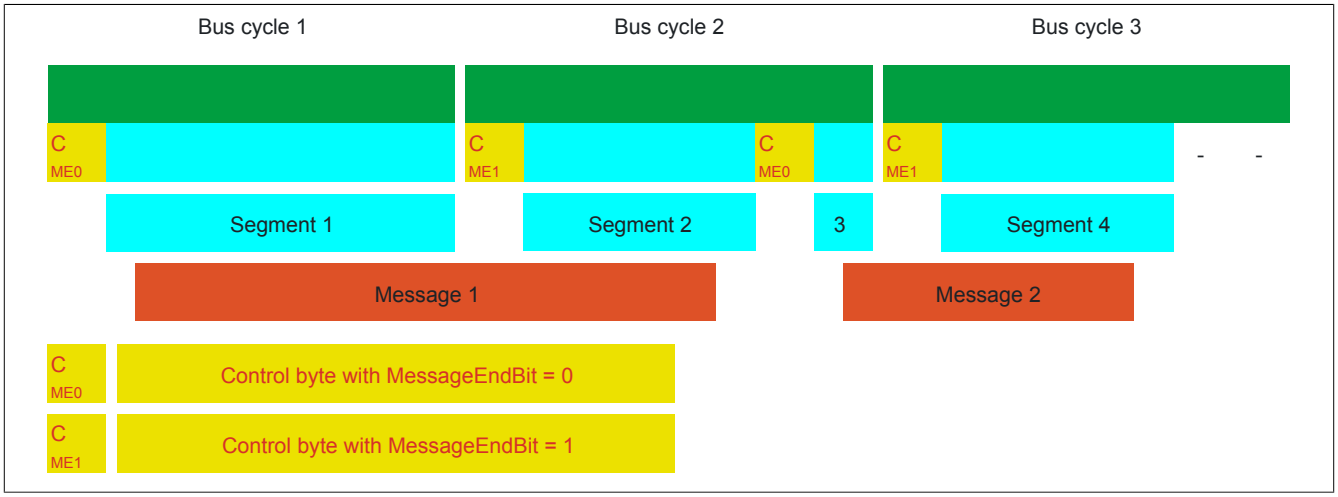


Figure 321: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

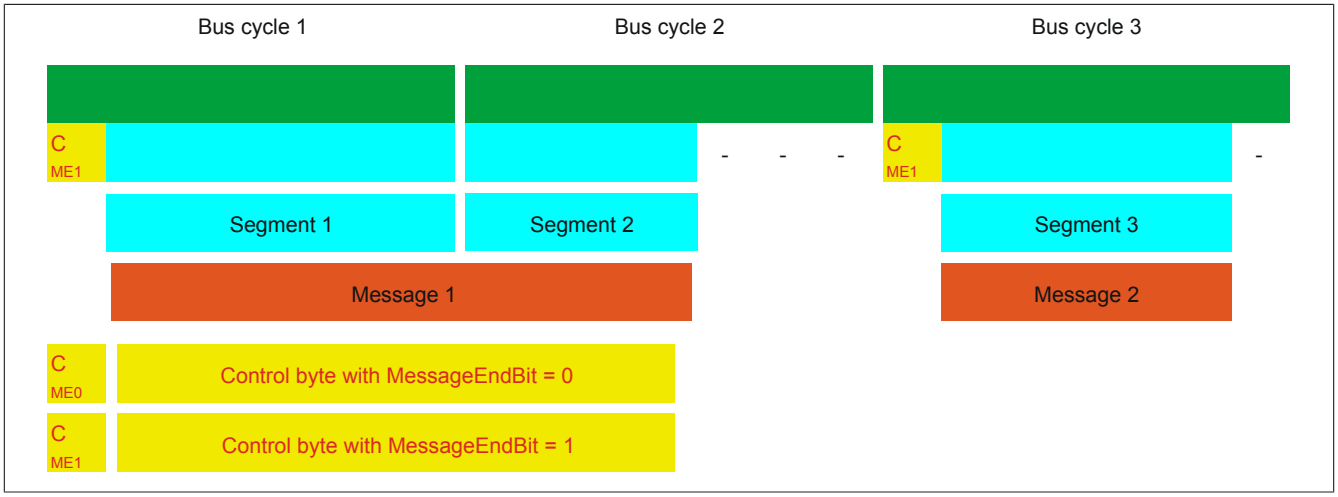


Figure 322: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

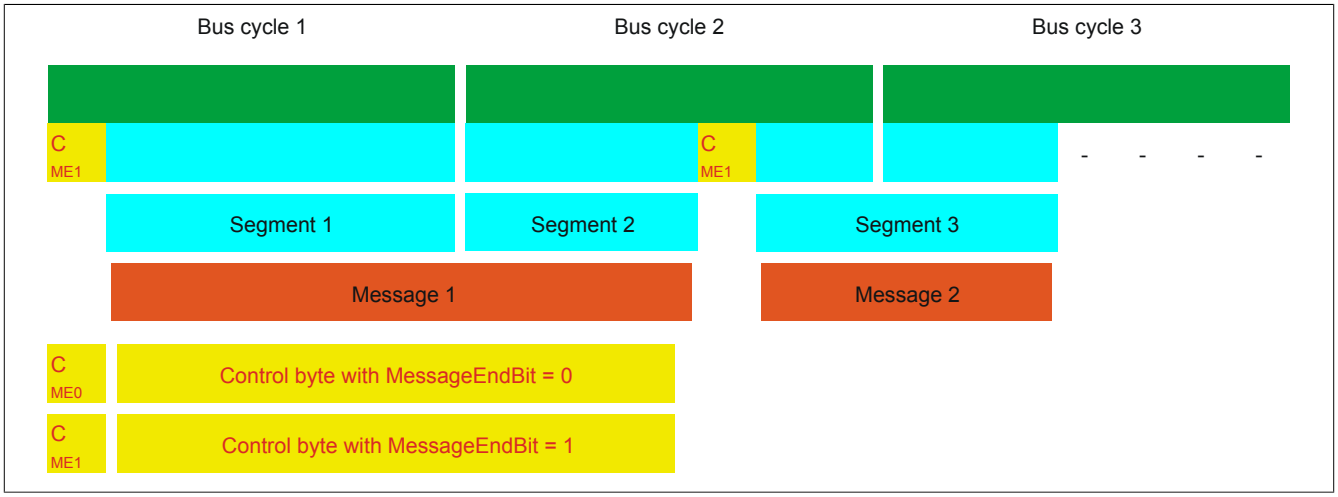


Figure 323: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

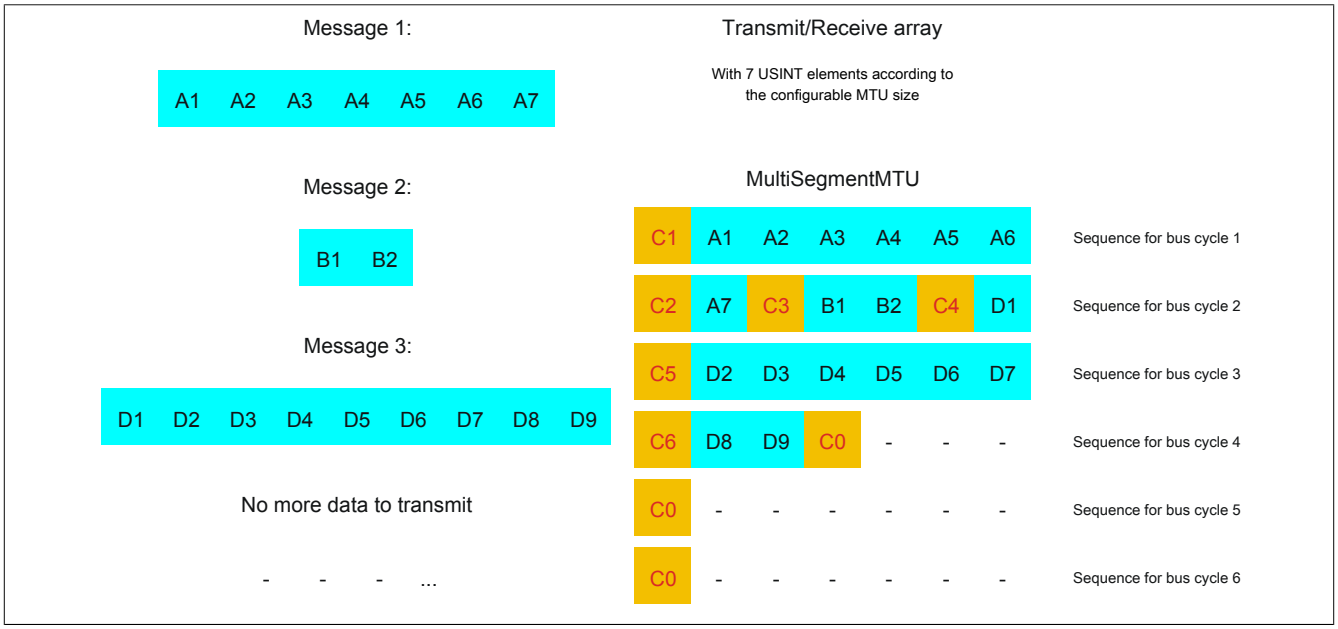


Figure 324: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 409: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 410: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

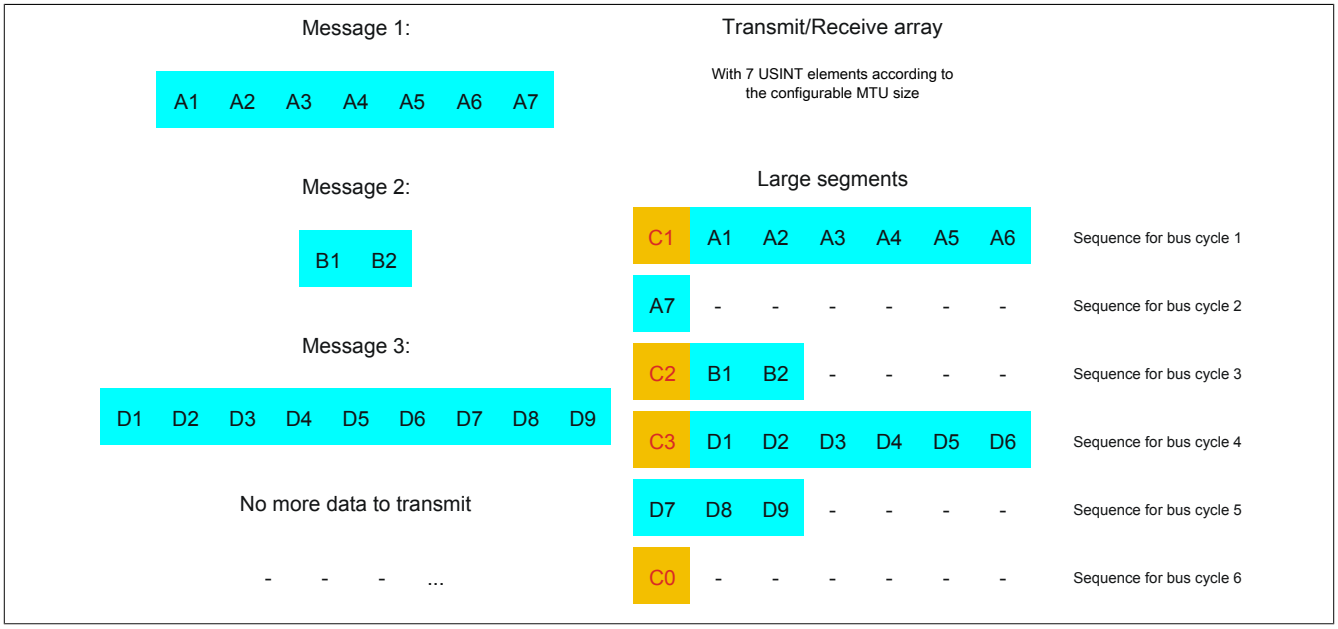


Figure 325: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 411: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

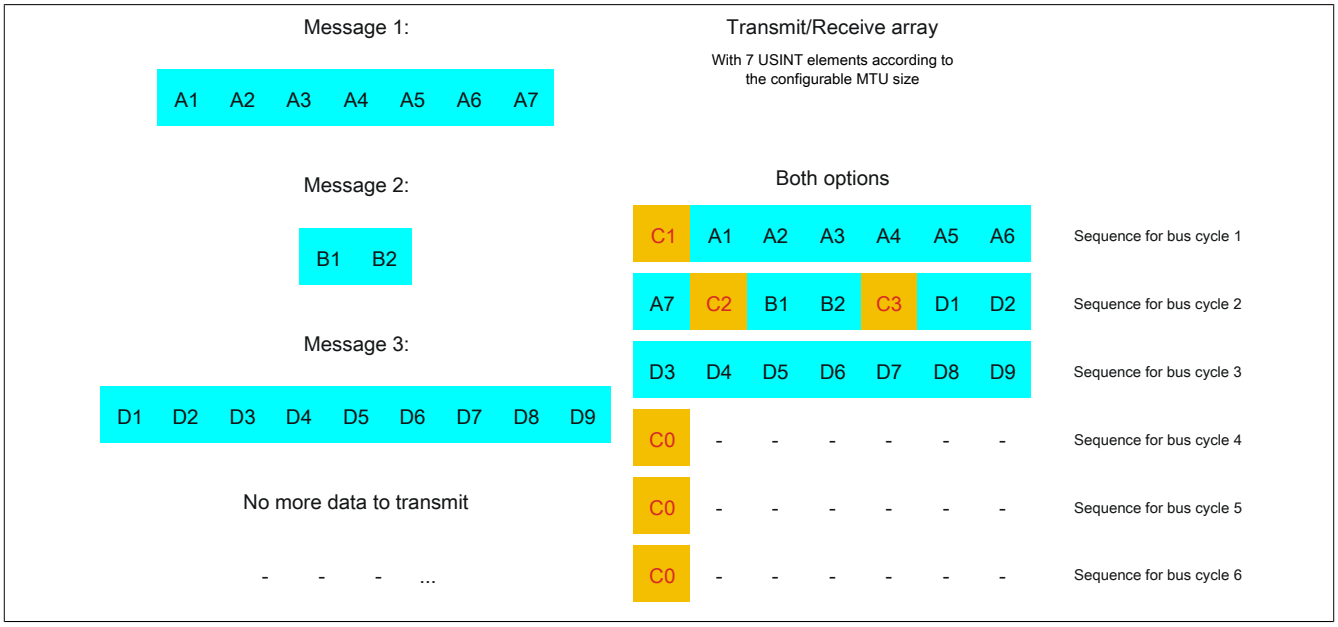


Figure 326: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 412: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.18.6.9.10.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

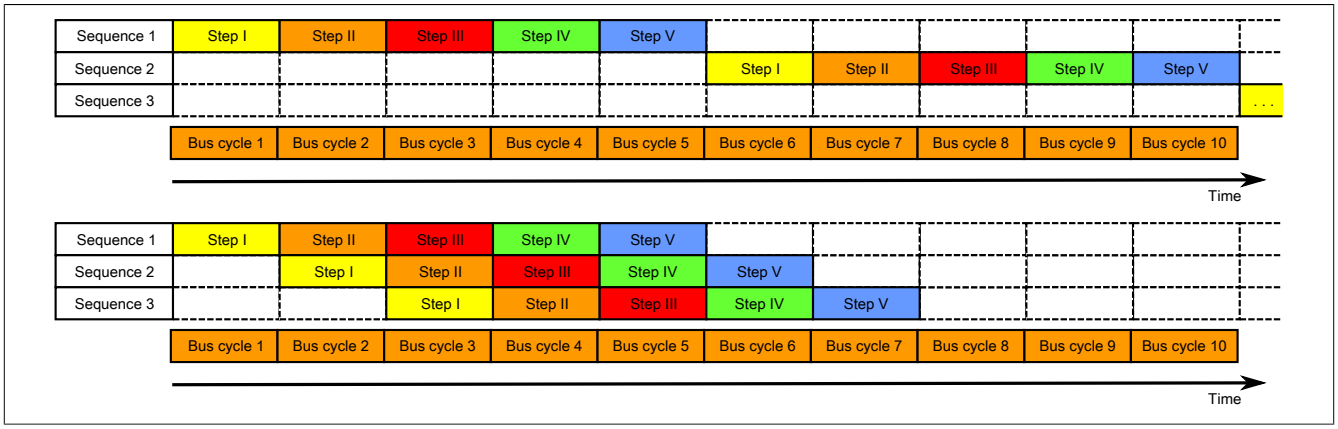


Figure 327: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

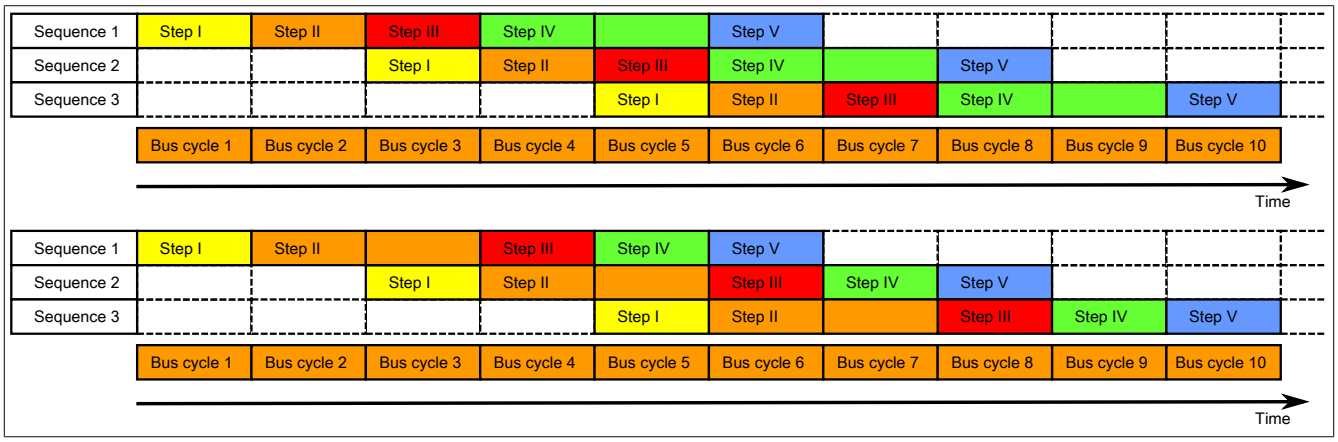


Figure 328: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

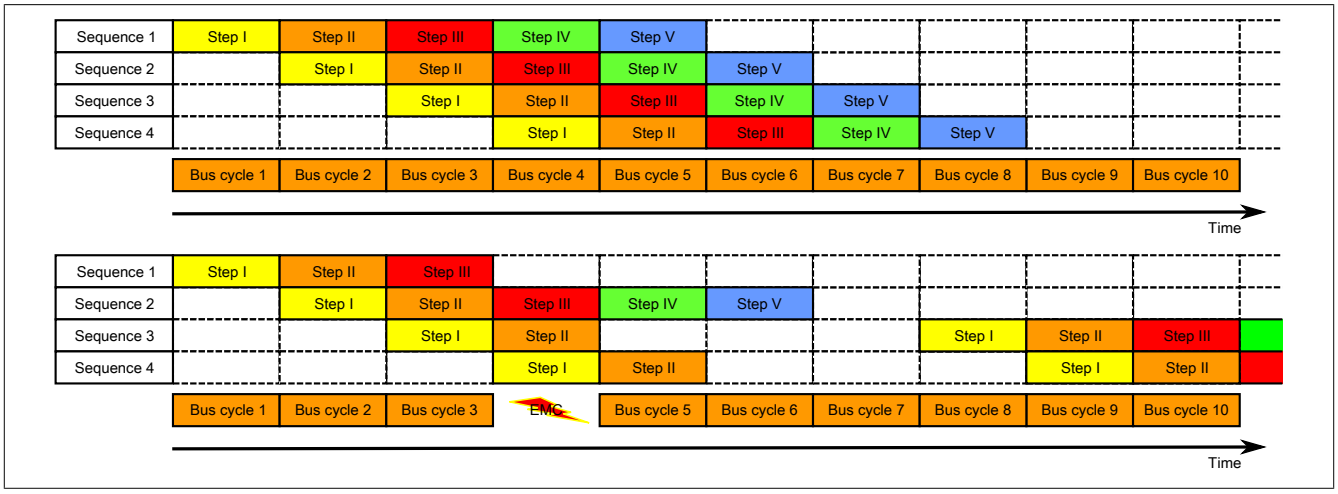


Figure 329: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.18.6.9.11 Serial with FlatStream

When using FlatStream communication, the module acts as a bridge between the X2X Link master and an intelligent field device connected to the module. FlatStream mode can be used for either point-to-point connections as well as for multidrop systems. Specific algorithms such as timeout and checksum monitoring are usually managed automatically. During normal operation, the user does not have access to these details.

In a serial network, the module is always the master (DTE). Various adjustments can be made to ensure that signals are transmitted without errors.
The user can, for example, define a handshake algorithm or set the baud rate in order to adapt the transmission quality to the requirements of the application.

Operation

When using FlatStream, the general structure of the FlatStream frame must be maintained.

Input/Output sequence	Tx/Rx bytes	
(unchanged)	Control byte (unchanged)	Serial frame (without hand-shake or similar measures)

4.18.6.9.12 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

4.18.6.9.13 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.18.6.9.14 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.18.7 X20CS1070

4.18.7.1 General information

In addition to the standard I/O, complex devices often need to be connected. The X20CS communication modules are designed precisely for cases like this. As normal X20 electronics modules, they can be placed anywhere on the remote backplane.

- CAN bus interface for serial, remote connection of complex devices to the X20 system
- Integrated terminating resistor

4.18.7.2 Order data

Model number	Short description	Figure
	X20 electronics module communication	
X20CS1070	X20 interface module, 1x CAN, max. 1 Mbit/s, object buffer in transmit and receive direction	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 413: X20CS1070 - Order data

4.18.7.3 Technical data

Product ID	X20CS1070
Short description	
Communication module	1x CAN bus
General information	
B&R ID code	0x1FD1
Status indicators	Data transfer, terminating resistor, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	
Bus	0.01 W
Internal I/O	1.44 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
IF1 - Bus	Yes
IF1 - I/O supply	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Signal	CAN bus
Design	Connection made using 12-pin X20TB12 terminal block
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Terminating resistor	Integrated in the module
Controller	SJA 1000
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 414: X20CS1070 - Technical data

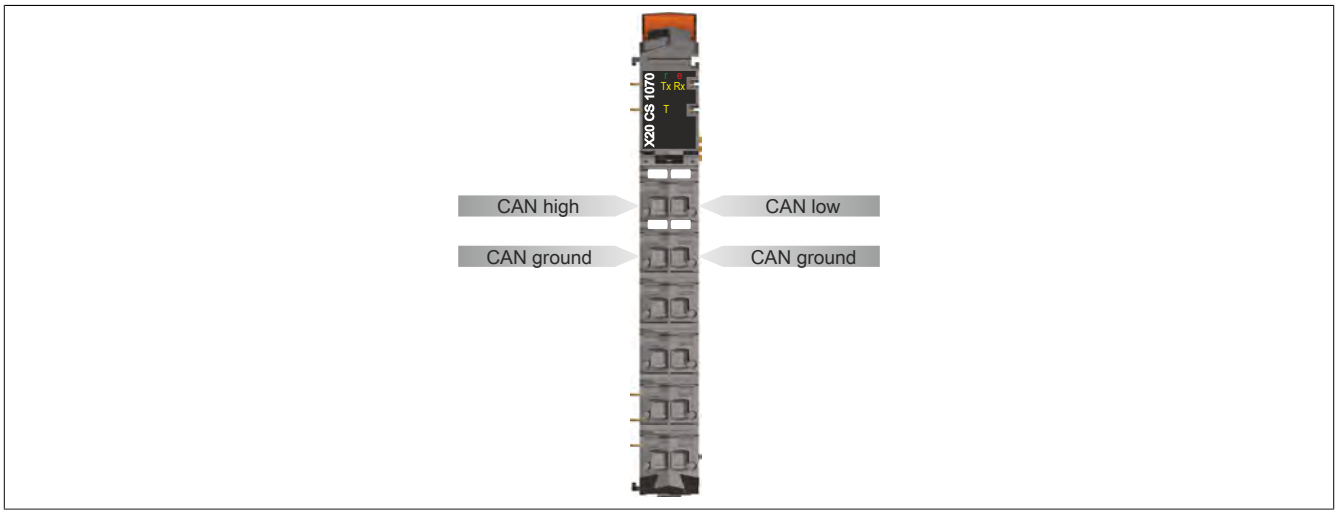
4.18.7.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

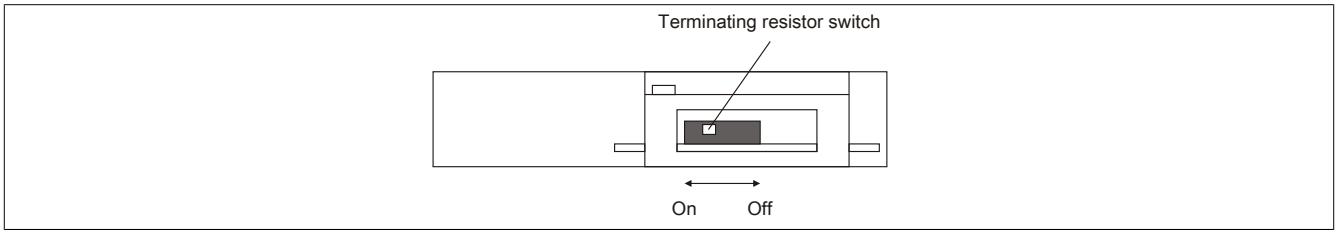
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	I/O error occurred • CAN bus: Warning, passive or off • Buffer overflow
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	Tx	Yellow	On	The module is sending data via the CAN bus interface
	Rx	Yellow	On	The module is receiving data via the CAN bus interface
	T	Yellow	On	Terminating resistor integrated in the module switched on

1) Depending on the configuration, a firmware update can take up to several minutes.

4.18.7.5 Pinout



4.18.7.6 Terminating resistor

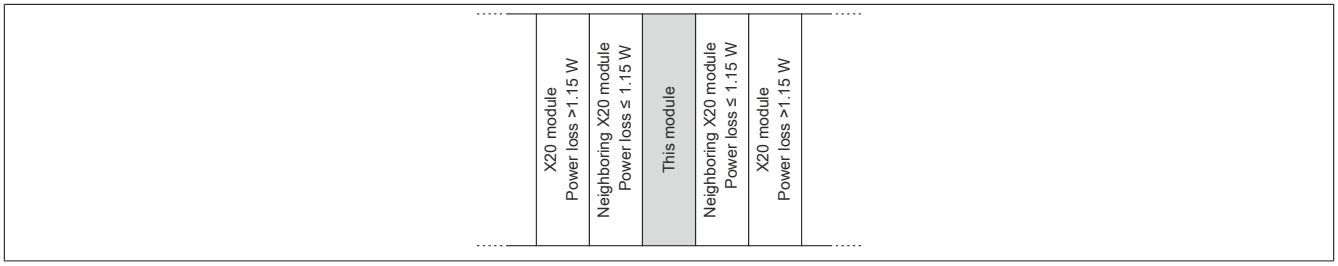


A terminating resistor is integrated in the communication module. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "T" LED.

4.18.7.7 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.18.7.8 Register description

4.18.7.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.18.7.8.2 Function model 0 - Flat

In the "Flat" function model, CAN information is transferred via cyclic input and output registers. All data for a CAN object (8 CAN data bytes, identifier, status, etc.) is accessible as individual data points (see also 4.18.7.8.7 "CAN object" on page 2042).

To transmit a CAN object, the CAN identifier, the CAN data (max. 8 bytes) and the number of bytes to be transmitted must be written to the cyclic I/O data points. Then, "TXCount" is increased to send the transmission. The data is held in the module's internal buffer (max. 18 objects) and transmitted over the CAN network at the next available opportunity.

Receiving information from the CAN network uses the same algorithm. The module saves the CAN messages in its internal buffer along with the respective identifiers. Then the CAN identifier, the CAN data (max. 8 bytes) and the number of bytes to be processed are written to the cyclic I/O data points. "RXCount" tells the application how much new data must be taken from these input data points.

Information:

- **The "CAN_Lib" library can't be used.**

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Interface - Configuration						
257	ConfigBaudrate	USINT				•
259	ConfigSJW	USINT				•
261	ConfigSPO	USINT				•
266	ConfigTXtrigger	UINT				•
673	Cfo_FIFOTXlimit	USINT				•
677	Cfo_TXRXinfoFlags	USINT				•
Interface - Communication						
641	TXCount	USINT			•	
513	TXCountReadBack	USINT	•			
545	TXCountLatchReadBack	USINT	•			
515	RXCount	USINT	•			
547	RXCountLatch	USINT	•			
Send buffer						
645	TXDataSize	USINT			•	
652	TXIdent	UDINT			•	
Index * 2 + 657	TXDataByte0 to TXDataByte7	USINT			•	
Index * 4 + 658	TXDataWord0 to TXDataWord3	UINT			•	
Index * 8 + 660	TXDataLong0 to TXDataLong1	UDINT			•	
Receive buffer 0						
517	RXDataSize0	USINT	•			
524	RXIdent0	UDINT	•			
Index * 2 + 529	RXData0Byte0 to RXData0Byte7	USINT	•			
Index * 4 + 530	RXData0Word0 to RXData0Word3	UINT	•			
Index * 8 + 532	RXData0Long0 to RXData0Long1	UDINT	•			
Receive buffer 1						
549	RXDataSize1	USINT	•			
556	RXIdent1	UDINT	•			
Index * 2 + 561	RXData1Byte0 to RXData1Byte7	USINT	•			
Index * 4 + 562	RXData1Word0 to RXData1Word3	UINT	•			
Index * 8 + 564	RXData1Long0 to RXData1Long1	UDINT	•			

4.18.7.8.3 Function model 2 - Stream and Function model 254 - Cyclic stream

The "Stream" and "Cyclic stream" function models use a module-specific driver for the CPU's operating system. The interface can be controlled using the "CAN_Lib" library and be reconfigured at runtime.

Function model - Stream

In the "Stream" function model, the CPU communicates with the module acyclically. The interface is relatively convenient, but the timing is very imprecise.

Function model - Cyclic stream

The "Cyclic stream" function model was implemented later. From the application's point of view, there is no difference between the "Stream" and "Cyclic stream" function models. Internally, however, the cyclic I/O registers are used to ensure that communication follows deterministic timing.

Information:

- **In order to use the "Stream" and "Cyclic stream" function models, you must be using B&R controllers of the type "SG4".**

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Module - Configuration						
-	AsynSize	-				
Interface - Configuration						
6273	CfO_ErrorID0007	USINT				•
Interface - Communication						
6145	CAN error status	USINT	•			
	CANwarning	Bit 0				
	CANpassive	Bit 1				
	CANbusoff	Bit 2				
	CANRXoverrun	Bit 3				
6209	CAN error acknowledgment	USINT			•	
	QuitCANwarning	Bit 0				
	QuitCANpassive	Bit 1				
	QuitCANbussoff	Bit 2				
	QuitCANRXoverrun	Bit 3				

4.18.7.8.4 Function model 254 - FlatStream

The "FlatStream" function model provides independent communication between an X2X Link master and the module. This interface was implemented as a separate function model for the CAN module. CAN information (identifier, status, etc.) is transferred via cyclic input and output registers. The sequence and control bytes are used to control this data stream (see 4.3.7.10.8 "FlatStream communication" on page 223).

When using the Flatstream function model, the user can choose whether to use the "AsFltGen" library in AS for implementation or to adapt Flatstream handling directly to the individual requirements of the application.

Information:

- **The "CAN_Lib" library can't be used.**
- **Higher data rates can be achieved between X2X master and module compared to the "Flat" function model.**

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Interface - Configuration						
257	ConfigBaudrate	USINT				•
259	ConfigSJW	USINT				•
261	ConfigSPO	USINT				•
266	ConfigTXtrigger	UINT				•
6273	CfO_ErrorID0007	USINT				•
Interface - Communication						
6145	CAN error status	USINT	•			
	CANwarning	Bit 0				
	CANpassive	Bit 1				
	CANbusoff	Bit 2				
	CANRXoverrun	Bit 3				
6209	CAN error acknowledgment	USINT			•	
	QuitCANwarning	Bit 0				
	QuitCANpassive	Bit 1				
	QuitCANbussoff	Bit 2				
	QuitCANRXoverrun	Bit 3				
FlatStream - Configuration						
193	outputMTU	USINT				•
195	inputMTU	USINT				•
197	mode	USINT				•
199	forward	USINT				•
206	forwardDelay	UINT				•
FlatStream - Communication						
0	InputSequence	USINT	•			
Index * 1 + 0	RxByte1 to RxByte27	USINT	•			
32	OutputSequence	USINT			•	
Index * 1 + 32	TxByte1 to TxByte27	USINT			•	

4.18.7.8.5 Function model 254 - Bus controller

The "Bus controller" function model is a reduced form of the "FlatStream" function model. Instead of up to 27 Tx / Rx bytes, a maximum of 7 Tx / Rx bytes can be used.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Interface - Configuration							
257	-	ConfigBaudrate	USINT				•
259	-	ConfigSJW	USINT				•
261	-	ConfigSPO	USINT				•
266	-	ConfigTXtrigger	UINT				•
6273	-	CfO_ErrorID0007	USINT				•
Interface - Communication							
6145	-	CAN error status	USINT		•		
		CANwarning	Bit 0				
		CANpassive	Bit 1				
		CANbusoff	Bit 2				
		CANRXoverrun	Bit 3				
6209	-	CAN error acknowledgment	USINT				•
		QuitCANwarning	Bit 0				
		QuitCANpassive	Bit 1				
		QuitCANbussoff	Bit 2				
		QuitCANRXoverrun	Bit 3				
FlatStream - Configuration							
193	-	outputMTU	USINT				•
195	-	inputMTU	USINT				•
197	-	mode	USINT				•
199	-	forward	USINT				•
206	-	forwardDelay	UINT				•
FlatStream - Communication							
0	0	InputSequence	USINT	•			
Index * 1 + 0	Index * 1 + 0	RxByte1 to RxByte7	USINT	•			
32	0	OutputSequence	USINT			•	
Index * 1 + 32	Index * 1 + 0	TxByte1 to TxByte7	USINT			•	

1) The offset specifies the position of the register within the CAN object.

4.18.7.8.5.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.18.7.8.6 Using this module with SGC target systems

> **Note:**
>
> **This module can only be used with SGC target systems if the function model is set to "Flatstream" or "Flat".**

4.18.7.8.7 CAN object

A CAN object is always made up of a 4-byte identifier and a maximum of 8 subsequent data bytes. This also results in the relationship between CAN object length and the amount of CAN payload data. This is important because the number of CAN payload data bytes for communication via "FlatStream" always has to be determined using the frame length.

Composition of a CAN object / CAN frame

Bytes	Function	Information
1	Code	ID bit 0 to 7
2		ID bit 8 to 15
3		ID bit 16 to 23
4		ID bit 24 to 31
5 - 12	CAN payload data	0 to 8 CAN payload data bytes

Code

The 32 bits (4 bytes) of the CAN identifier are used as follows:

Bit	Description	Value	Information
0	Frame format	0	Standard frame format (SFF) with an 11-bit identifier
		1	Extended frame format (EFF) with an 29-bit identifier
1	Frame type	0	Data frame
		1	Remote frame (RTR)
2	Reserved	-	
3 - 31	CAN identifier for telegram to be transmitted	x	Extended frame format (EFF) with 29 bits Standard frame format (SFF) with 11 bits[1)]

1) Only bits 21 to 31 used; bits 3 to 20 = 0

4.18.7.8.7.1 CAN module data stream

In function model 254, the data packets to be transferred in a data stream are referred to as frames.

Information:

For the CAN module, that means:

- **A frame always contains one CAN object and therefore cannot be longer than 12 bytes.**
- **The CAN object is only transferred to the transmit buffer after the frame has been completed.**
- **The CAN payload data length has a fixed relationship with the frame length and the actual size of the CAN object. The following rules apply:**
  - **CAN payload data length = Frame length - 4**
  - **Frame length = CAN payload data length + 4**

4.18.7.8.8 Interface - Configuration

4.18.7.8.8.1 Transfer rate

Name:
ConfigBaudrate

"Baud rate" in the AS I/O configuration.

Configuration of the CAN transfer rate for the interface.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Transfer rate	1	10 kbit/s
		2	20 kbit/s
		3	50 kbit/s
		4	100 kbit/s
		5	125 kbit/s
		6	250 kbit/s
		7	500 kbit/s (default)
		8	800 kbit/s
		9	1000 kbit/s
4 - 7	Reserved	-	

4.18.7.8.8.2 Synchronization Jump Width

Name:
ConfigSJW

"Synchronization jump width" in the AS I/O configuration.

The synchronization jump width (SJW) is used to resynchronize the sample point within a CAN telegram.

A detailed description of the SJW can be found in the CAN specification.

Data type	Value	Meaning
USINT	0 to 4	Synchronization jump width (default = 3)

4.18.7.8.8.3 Offset for the sampling instant

Name:
ConfigSPO

"Sample point offset" in the AS I/O configuration.

Offset for the sample point of the individual bits on the CAN bus.

A detailed description of the SPO can be found in the CAN specification.

Data type	Value	Meaning
USINT	0 to 1	Sample point offset (default = 0)

4.18.7.8.8.4 Start of transmission

Name:
ConfigTXtrigger

"TX objects / TX triggers" in the AS I/O configuration.

Defines the number of CAN objects that must be copied to the transmit buffer before the transmission is started.

Data type	Value	Meaning
UINT	0 to 8	Number of CAN objects in the transmit buffer before transmission is started (default = 1)

4.18.7.8.8.5 Configuration of error messages

Name:
CfO_ErrorID0007

This register must be used first to configure the error messages that have to be transferred. If the corresponding enable bit is not set, no error status will be sent to the higher-level system when the error occurs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	CANwarning	0	Disabled
		1	Enabled
1	CANpassive	0	Disabled
		1	Enabled
2	CANbussoff	0	Disabled
		1	Enabled
3	CANRXoverrun	0	Disabled
		1	Enabled
4 - 7	Reserved	-	

4.18.7.8.8.6 Size of the transmit buffer

Name:
Cfo_FIFOTXlimit

"TX FIFO size" in the AS I/O configuration.

Determines the size of the transmit buffer for the respective interface.

Data type	Value	Meaning
USINT	0 to 18	Size of the transmit buffer (default = 1)

4.18.7.8.8.7 Display of unprocessed elements remaining in transmit/receive buffer

Name:
Cfo_TXRXinfoFlags

This register can be used to specify that the number of unprocessed elements in the transmit and receive buffers is indicated in the upper 4 bits of the "TxCountReadback" and "RxCount" registers for the interface.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TxFifoInfo "Mode of channel TXCountReadBack" in the AS I/O configuration	0	The "TXCountReadBack" on page 2046 and "TXCountLatchReadBack" on page 2046 registers are used to read back "TXCount".
		1	The lower 4 bits of the "TXCountReadBack" on page 2046 and "TXCountLatchReadBack" on page 2046 registers are used to read back "TXCount". The upper 4 bits are used to return the number of frames in the transmit buffer that have not been transmitted.
1	RxFifoInfo "Mode of channel RXCount" in the AS I/O configuration	0	The "RXCount" on page 2046 and "RXCountLatch" on page 2047 registers are used to indicate the number of telegrams that have been received.
		1	The lower 4 bits of the "RXCount" on page 2046 and "RXCountLatch" on page 2047 registers are used to indicate the number of telegrams received. The upper 4 bits are used to indicate the number of received but not acknowledged telegrams in the receive buffer.
2 - 7	Reserved	-	

4.18.7.8.9 Interface - Communication

4.18.7.8.9.1 CAN error status

Name:
CAN error status

The bits in this register indicate the error states defined in the CAN protocol. If an error occurs, the corresponding bit is set. For an error bit to be reset, the corresponding bit must be acknowledged (see 4.18.7.8.9.2 "CAN error acknowledgment" on page 2045).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	CANwarning	0	No error
		1	CANwarning error on IF1
1	CANpassive	0	No error
		1	CANpassive error on IF1
2	CANbusoff	0	No error
		1	CANbusoff error on IF1
3	CANRXoverrun	0	No error
		1	CANRXoverrun error on IF1
4 - 7	Reserved	-	

4.18.7.8.9.2 CAN error acknowledgment

Name:
CAN error acknowledgment

Setting the bits in this register acknowledges the error assigned to the bit and clears the corresponding bit in the "CAN error status" register. The application thus informs the module that it has recognized the error state.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	QuitCANwarning	0	No acknowledgment
		1	Acknowledge CANwarning error on IF1
1	QuitCANpassive	0	No acknowledgment
		1	Acknowledge CANpassive error on IF1
2	QuitCANbussoff	0	No acknowledgment
		1	Acknowledge CANbusoff error on IF1
3	QuitCANRXoverrun	0	No acknowledgment
		1	Acknowledge CANRXoverrun error on IF1
4 - 7	Reserved	-	

4.18.7.8.9.3 New CAN telegram for transmit buffer

Name:
TXCount

By increasing this value, the application notifies the module that a new CAN telegram should be transferred into the transmit buffer.

Data type	Value
USINT	0 to 255

4.18.7.8.9.4 Read "TXCount"

Name:
TXCountReadBack

The value of "TXCount" is copied from the module into this register. This makes it possible for the application task to verify that the CAN telegram data was transfered from the module correctly.

The meaning of the value depends on the "TxFifoInfo" bit. This is located in the Cfo_TXRXinfoFlags register

Data type	Value	"TxFifoInfo" bit	Meaning
USINT	0 to 255	0	Read back "TX-Count"
		1	See bit structure.

Bit structure:

Bit	Function	Value	Information
0 - 3	Read back "TX-Count"	0 to 15	Only the lower 4 bits
4 - 7	Number of frames in the transmit buffer that have not been transmitted	0 to 15	If this number exceeds the 15 (a maximum of 18 possible), the value 15 is returned.

4.18.7.8.9.5 Read "TXCount" from the previous cycle

Name:
TXCountLatchReadBack

This register is used to copy the "TxCount" value from the previous cycle from the module. In the event of an X2X Link or POWERLINK transfer error, this makes it possible to determined if the error occurred on the way from the CPU to the module or on the way from the module to the CPU (see 4.18.7.8.10.4 "Taking possible errors into consideration when transmitting" on page 2048).

The meaning of the value depends on the "TxFifoInfo" on page 2044 bit in the "Cfo_TXRXinfoFlags" register.

Data type	Value	"TxFifoInfo" bit	Meaning
USINT	0 to 255	0	TX-Count read back from the previous cycle
		1	See bit structure.

Bit structure:

Bit	Function	Value	Information
0 - 3	TX-Count read back from the previous cycle	0 to 15	Only the lower 4 bits
4 - 7	Number of frames in the transmit buffer that have not been transmitted	0 to 15	From the previous cycle

4.18.7.8.9.6 Counter for received CAN telegrams

Name:
RXCount

This counter is increased by 1 with each CAN telegram. The application task can thus detect when new data is received and get it from the corresponding "RXData" registers.

The meaning of the value depends on the "RxFifoInfo" on page 2044 bit in the "Cfo_TXRXinfoFlags" register.

Data type	Value	"RxFifoInfo" bit	Meaning
USINT	0 to 255	0	Counter for received telegrams
		1	See bit structure.

Bit structure:

Bit	Function	Value	Information
0 - 3	Counter for received telegrams	0 to 15	Only the lower 4 bits
4 - 7	Number of unacknowledged telegrams in the receive buffer	0 to 15	

4.18.7.8.9.7 Read "RXCount" from the previous cycle

Name:
RXCountLatch

This register always contains the "RXCount" value from the previous cycle. It can be used to detect transfer errors from the module to the CPU (see 4.18.7.8.10.4 "Taking possible errors into consideration when transmitting" on page 2048).

The meaning of the value depends on the "RxFifoInfo" on page 2044 bit in the "Cfo_TXRXinfoFlags" register.

Data type	Value	"RxFifoInfo" bit	Meaning
USINT	0 to 255	0	Counter for received telegrams from the previous cycle
		1	See bit structure.

Bit structure:

Bit	Function	Value	Information
0 - 3	Counter for received telegrams from the previous cycle	0 to 15	Only the lower 4 bits
4 - 7	Number of telegrams in the receive buffer from the previous cycle	0 to 15	

4.18.7.8.10 Send buffer

4.18.7.8.10.1 Number of CAN payload data bytes

Name:
TXDataSize

Number of CAN payload data bytes to be transmitted If a value less than 0 is specified here, this CAN telegram is marked as being invalid and is not transferred into the transmit buffer. This is useful in connection with transmit error detection between the module and the CPU (see 4.18.7.8.10.4 "Taking possible errors into consideration when transmitting" on page 2048).

Data type	Value	Meaning
USINT	-128 to 8	Amount of CAN payload data to be transmitted (Default = 0).

4.18.7.8.10.2 Identifier of the CAN telegram to be transmitted.

Name:
TXIdent

Identifier of the CAN telegram to be transmitted. The frame format and the identifier format are also defined in this register.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Frame format	0	Standard frame format (SFF) with an 11-bit identifier
		1	Extended frame format (EFF) with an 29-bit identifier
1	Frame type	0	Data frame
		1	Remote frame (RTR)
2	Reserved	-	
3 - 31	CAN identifier for telegram to be transmitted	x	Extended frame format (EFF) with 29 bits Standard frame format (SFF) with 11 bits[1)]

1) Only bits 21 to 31 used; bits 3 to 20 = 0

4.18.7.8.10.3 Configuration of the CAN payload data being sent

Name:
TXDataByte0 to TXDataByte7
TXDataWord0 to TXDataWord3
TXDataLong0 to TXDataLong1

CAN payload data in the transmit direction. The 8 payload data bytes for a telegram can be used as data points with 8 individual bytes, 4 words or 2 longs as needed.

Data type	Value	Description
USINT	0 to 255	CAN payload data transmitted as bytes
UINT	0 to 65,535	CAN payload data transmitted as words
UDINT	0 to 4.294.967.295	CAN payload data transmitted as longs

4.18.7.8.10.4 Taking possible errors into consideration when transmitting

Data on the POWERLINK network or X2X Link can be lost due to transmission errors. One-time failures of cyclic data are tolerated by the I/O systems. This is possible since all I/O data is re-transferred in the subsequent cycle. A transfer error cannot be detected from the I/O variables; they remain frozen on the value from the last cycle.

These tolerated one-time I/O failures can lead to data loss or the delayed CAN telegram transmission. The counter feedback is derived on the module and used to detect these cases.

Register for counter feedback:

- "TXCountReadBack" on page 2046
- "TXCountLatchReadBack" on page 2046

4.18.7.8.11 Receive buffers 0 and 1

4.18.7.8.11.1 Number of valid CAN payload data bytes

Name:
RXDataSize0
RXDataSize1

Number of valid CAN payload data bytes.

This register also uses the value -1 (0xFF) to indicate a general error or gap in the input data stream. Details regarding the error that has occurred can be seen in the "" on page register.

Data type	Value	Meaning
USINT	1 to 8	Number CAN payload data
	-1	Error

4.18.7.8.11.2 Identifier of the received data

Name:
RXIdent0
RXIdent1

Identifiers assigned to the received data. The frame format and the identifier format can also be read from this register.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Frame format	0	Standard frame format (SFF) with an 11-bit identifier
		1	Extended frame format (EFF) with an 29-bit identifier
1	Frame type	0	Data frame
		1	Remote frame (RTR)
2	Reserved	-	
3 - 31	CAN identifier for telegram to be transmitted	x	Extended frame format (EFF) with 29 bits Standard frame format (SFF) with 11 bits[1)]

1) Only bits 21 to 31 used; bits 3 to 20 = 0

4.18.7.8.11.3 Configuration of the CAN payload data to be received

Name:
RXData0Byte0 to RXData0Byte7
RXData0Word0 to RXData0Word3
RXData0Long0 to RXData0Long1

RXData1Byte0 to RXData1Byte7
RXData1Word0 to RXData1Word3
RXData1Long0 to RXData1Long1

These registers hold the payload data of the CAN object to be transferred from the receive buffer to the CPU in the current cycle. If new data is received or if the receive buffer contains additional CAN objects, these registers are overwritten with the new data in the next cycle.

To avoid losing CAN objects, the application must respond immediately to a change in the "RXCount" and copies the data from these registers.

The maximum 8 bytes for a CAN telegram can be used as data points with 8 individual bytes, 4 words or 2 longs as needed.

Data type	Value	Description
USINT	0 to 255	Received CAN payload data as bytes
UINT	0 to 65,535	Received CAN payload data as words
UDINT	0 to 4.294.967.295	Received CAN payload data as longs

4.18.7.8.12 FlatStream communication

4.18.7.8.12.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

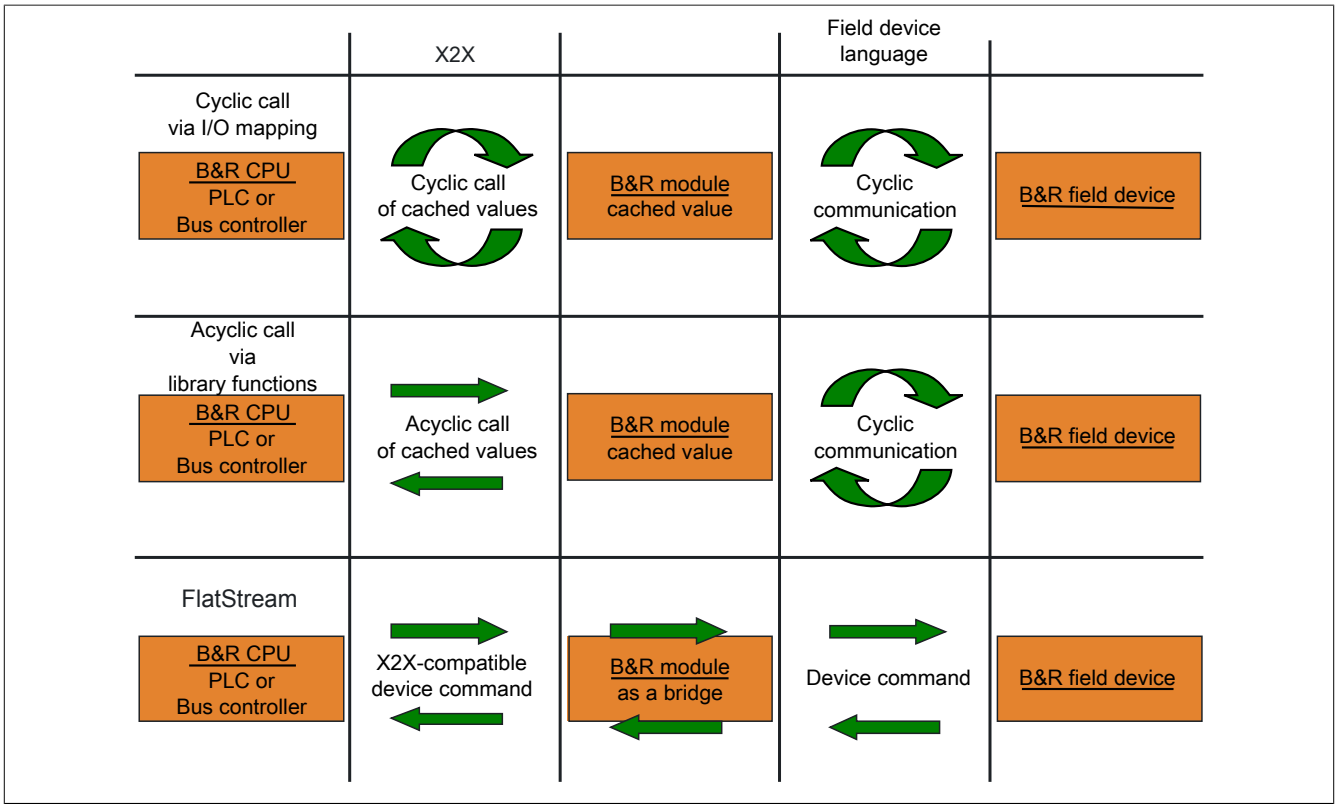


Figure 330: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.18.7.8.12.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.18.7.8.12.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

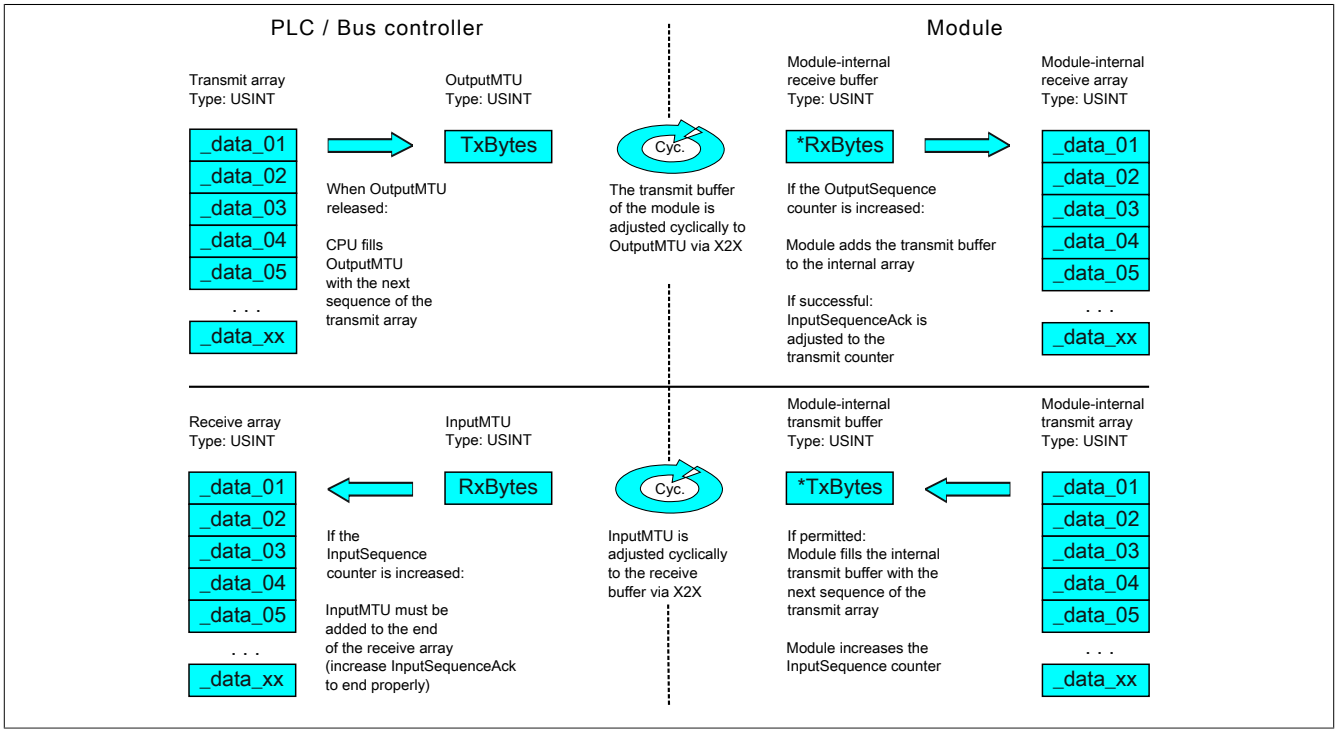


Figure 331: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.18.7.8.12.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Format of input and output bytes

Name:

"Format of Flat stream" in Automation Studio

This function sets how the Flatstream input and output bytes (Tx or Rx bytes) are transferred.

- **packed variable:** Transfers data as an array
- **byte variables:**Transfers data as individual bytes

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

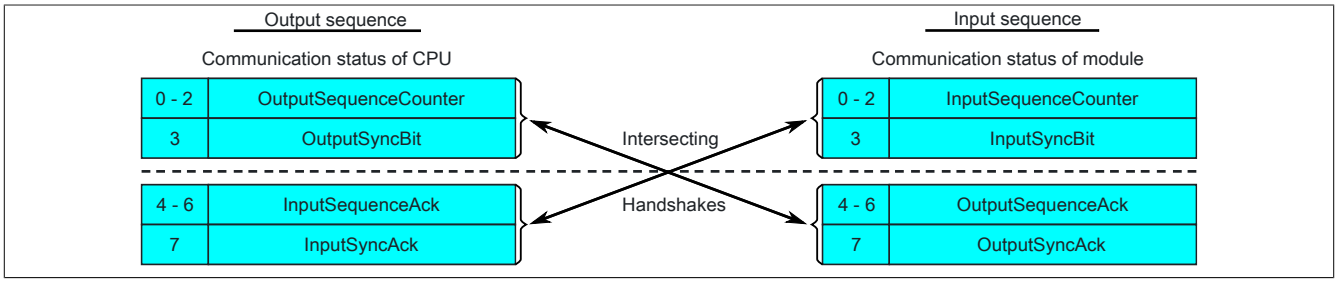


Figure 332: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

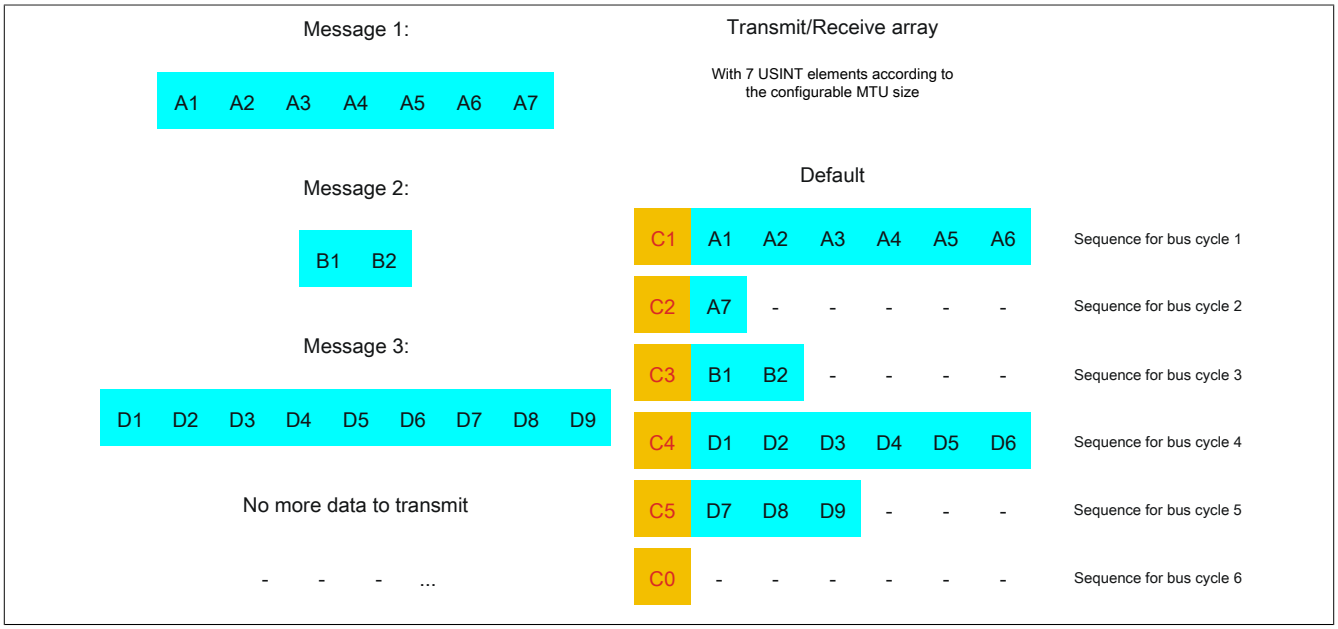


Figure 333: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 415: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 416: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

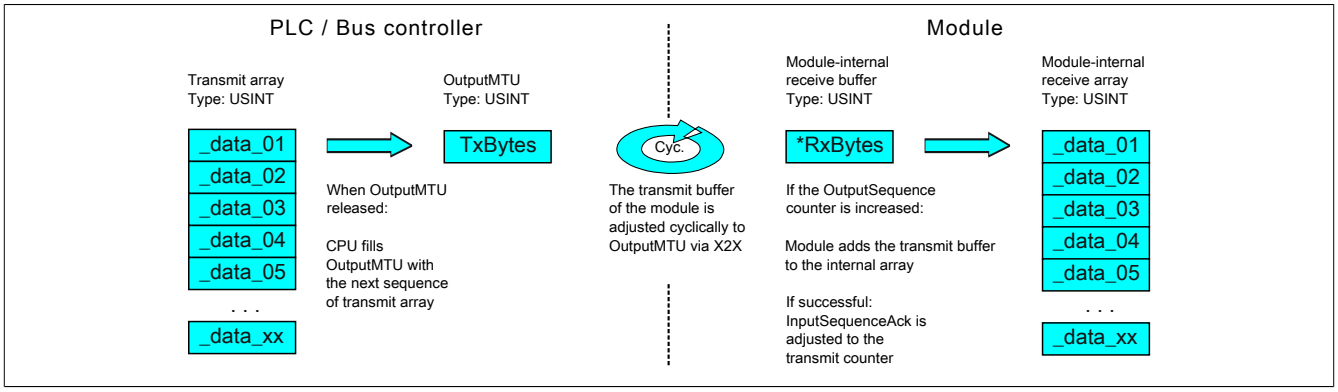


Figure 334: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

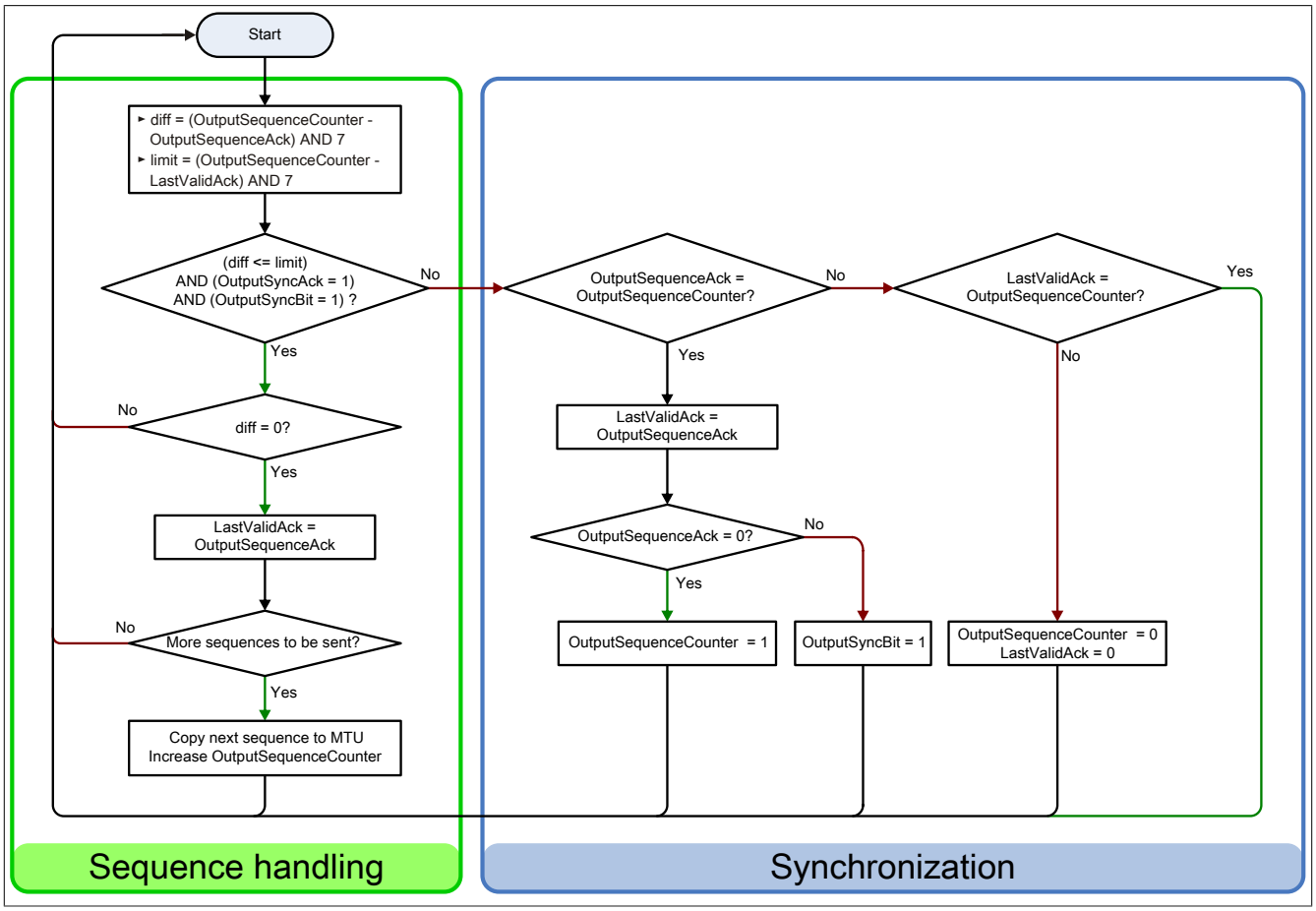


Figure 335: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

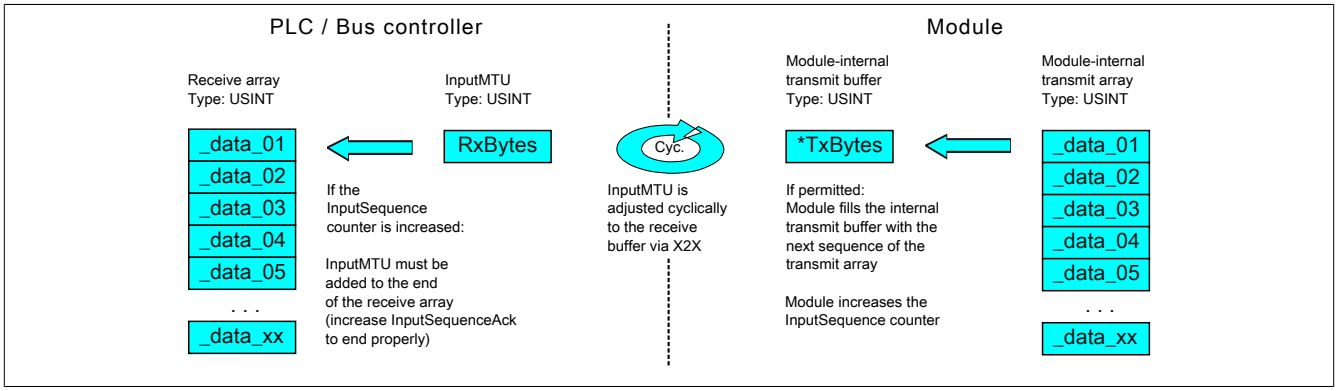


Figure 336: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

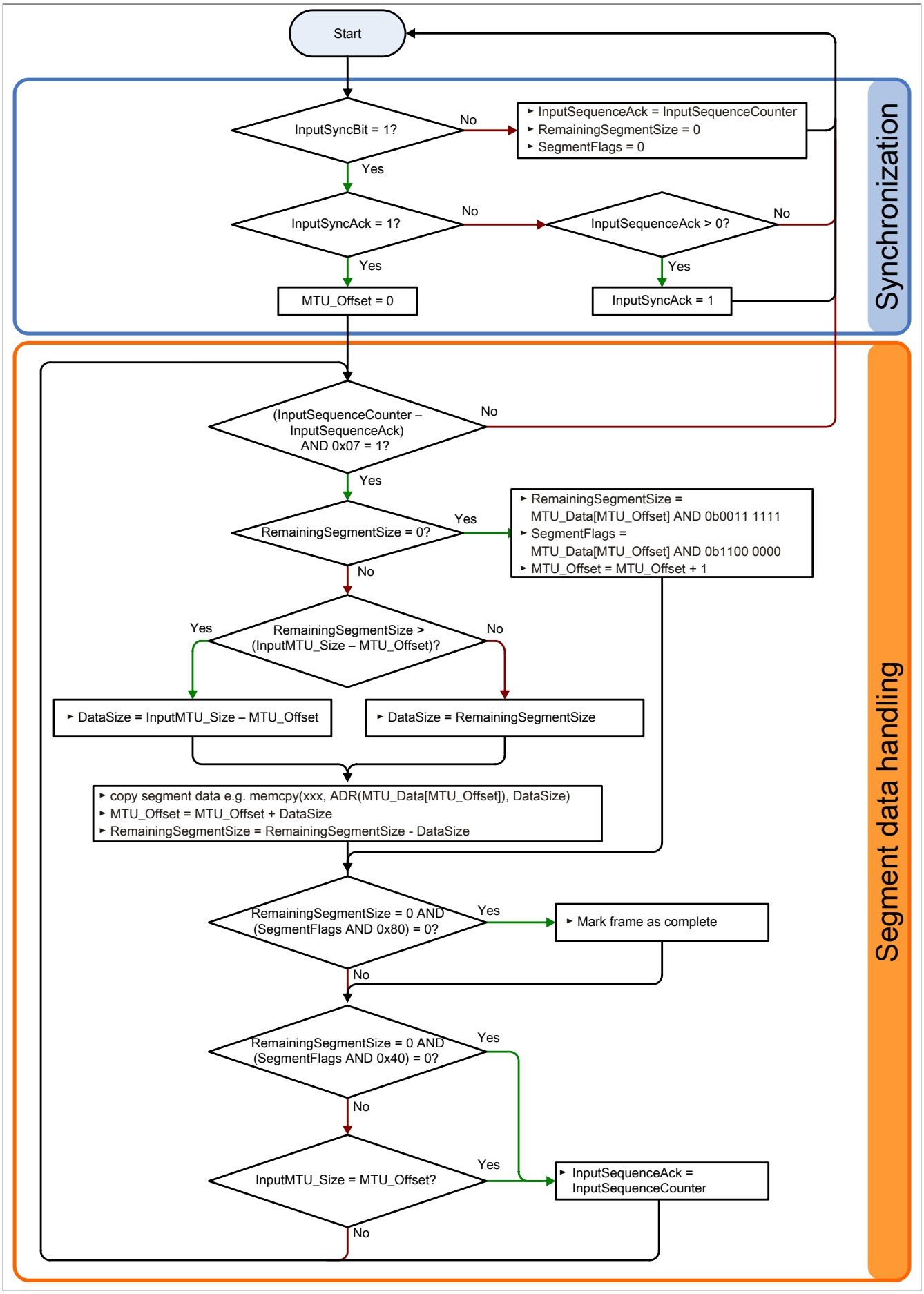


Figure 337: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

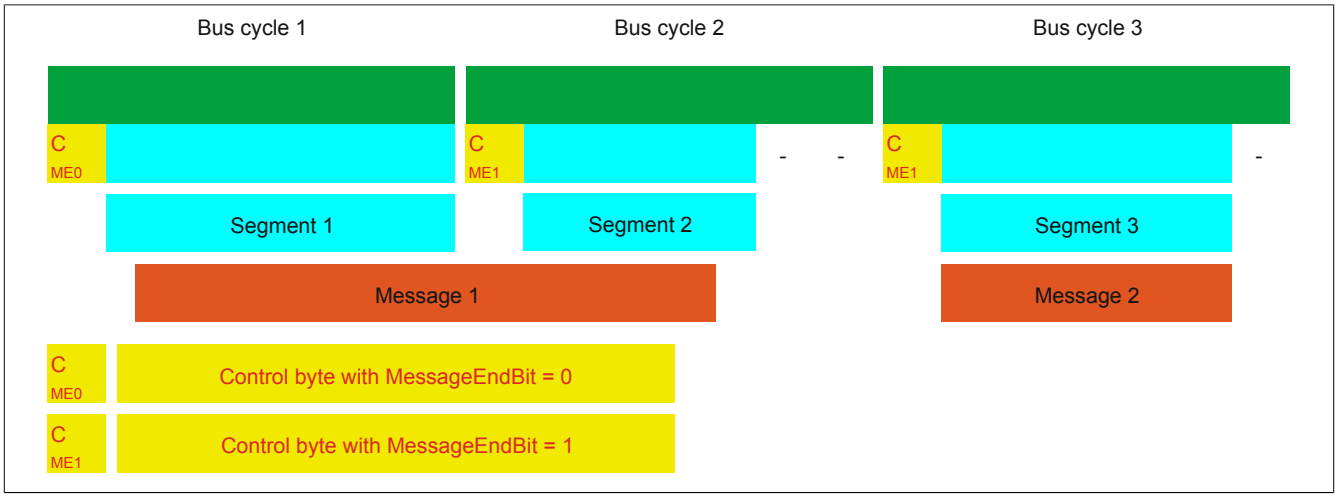


Figure 338: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

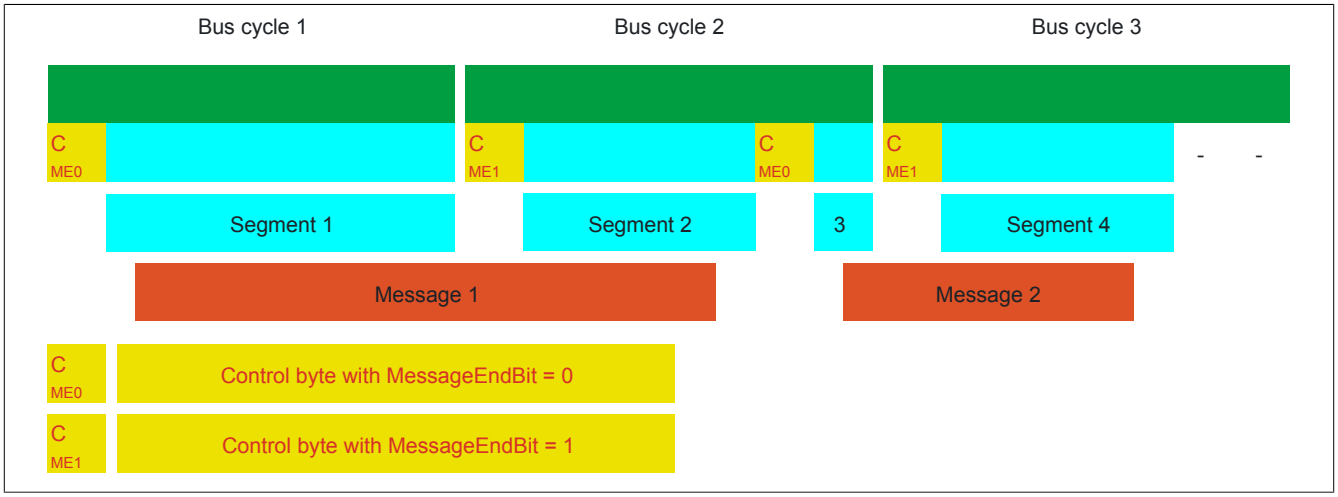


Figure 339: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

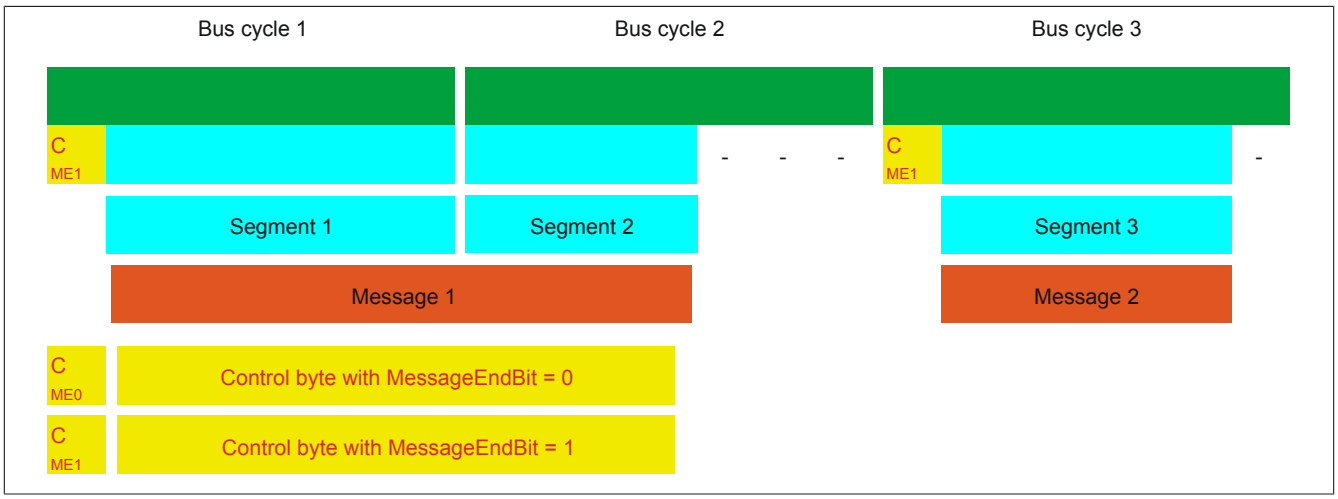


Figure 340: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

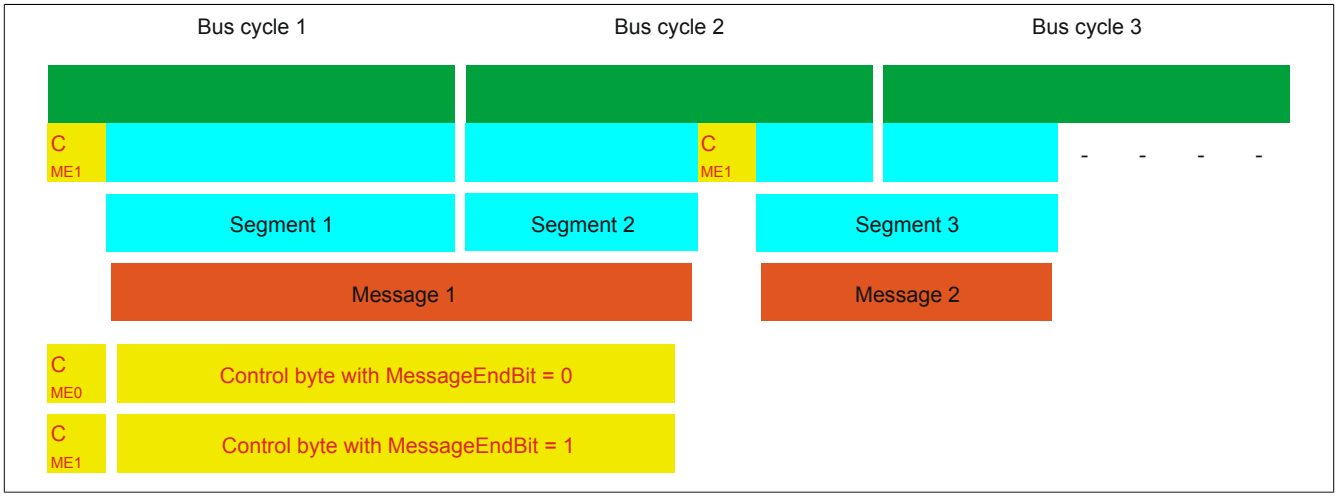


Figure 341: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

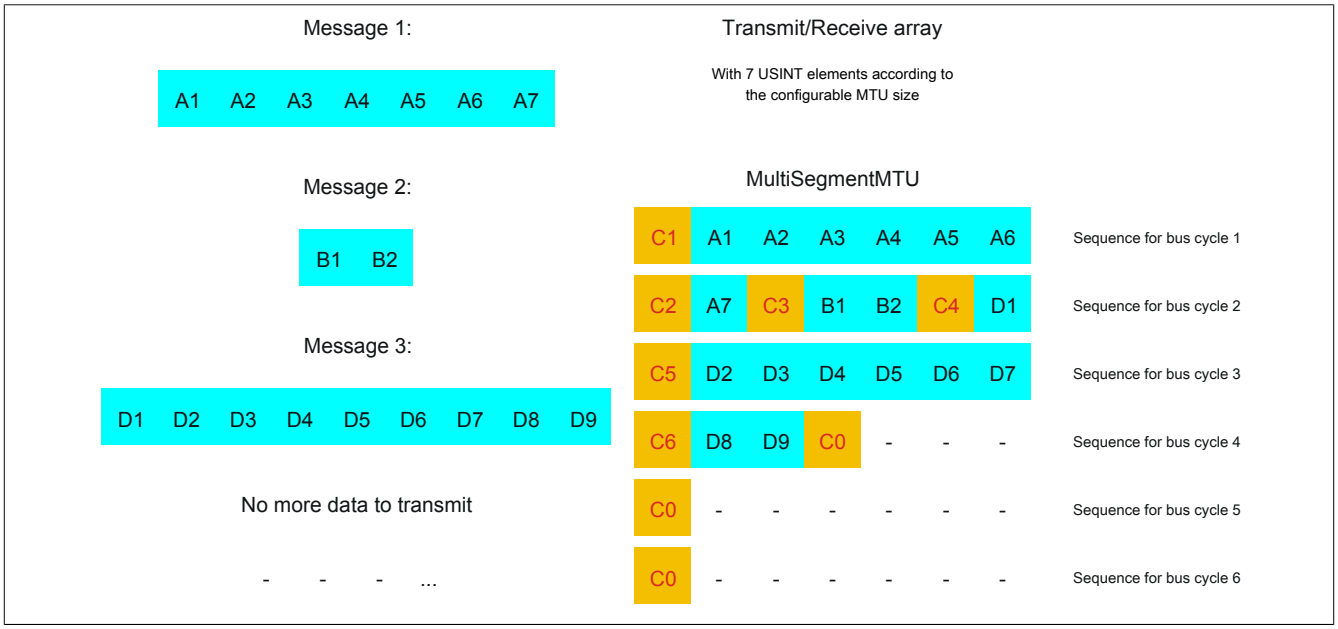


Figure 342: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 417: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 418: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

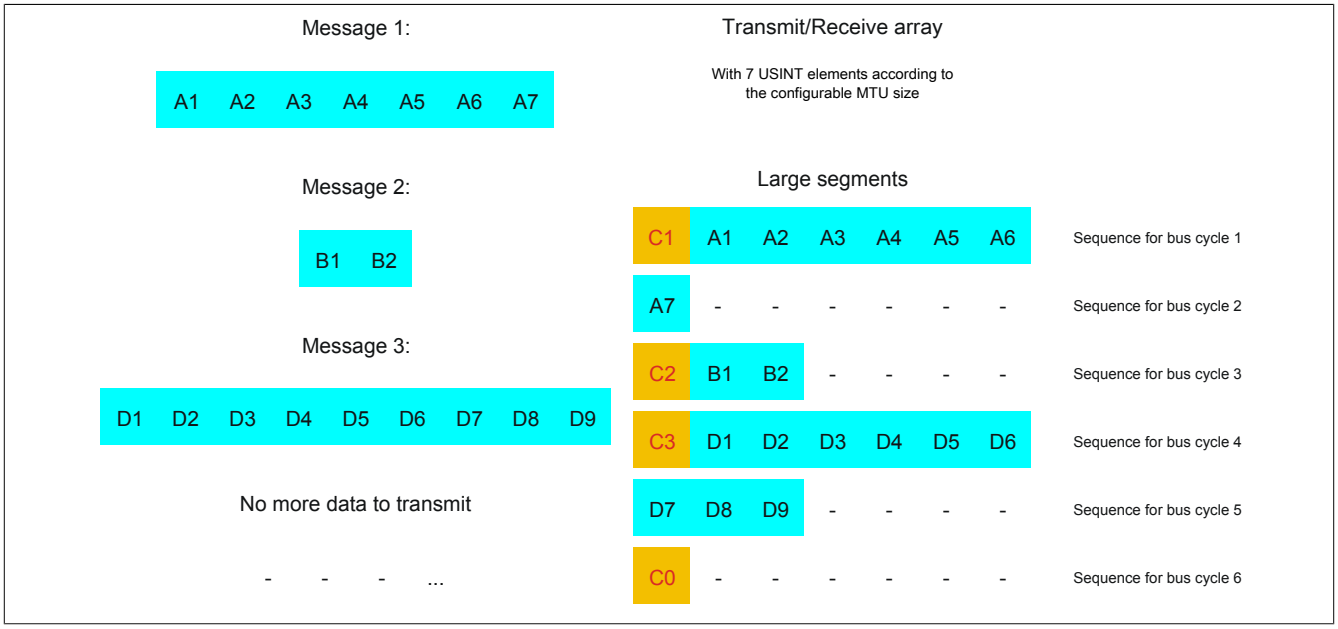


Figure 343: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 419: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

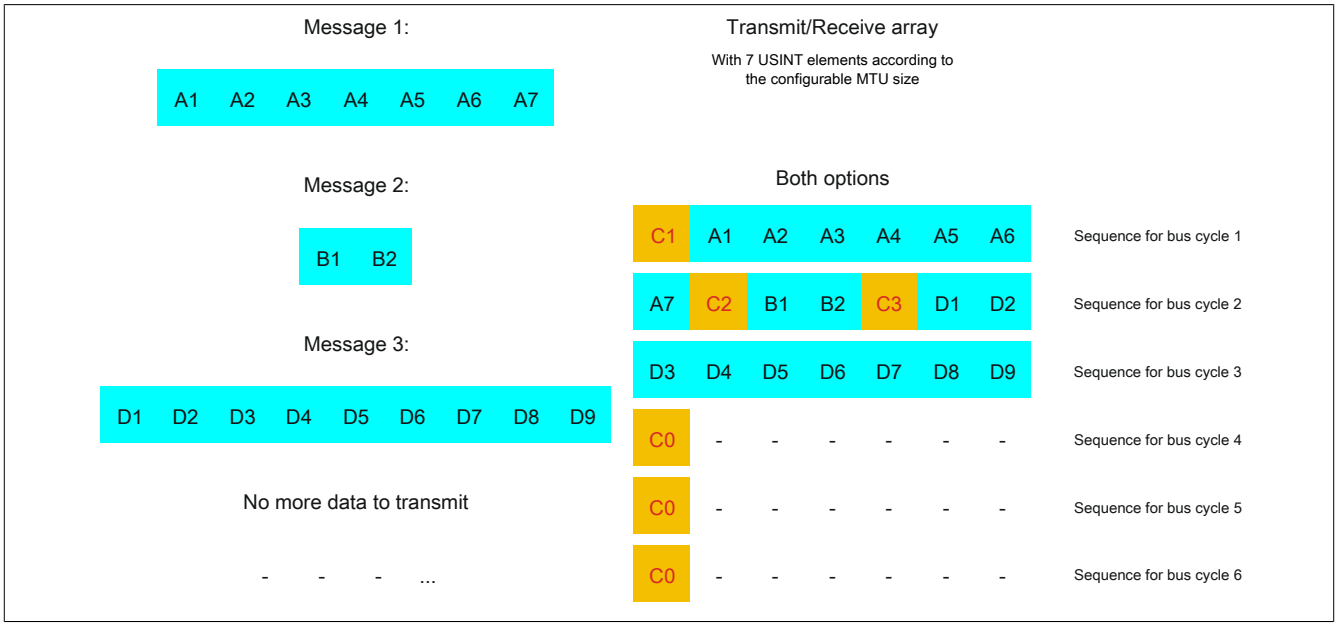


Figure 344: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 420: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.18.7.8.12.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

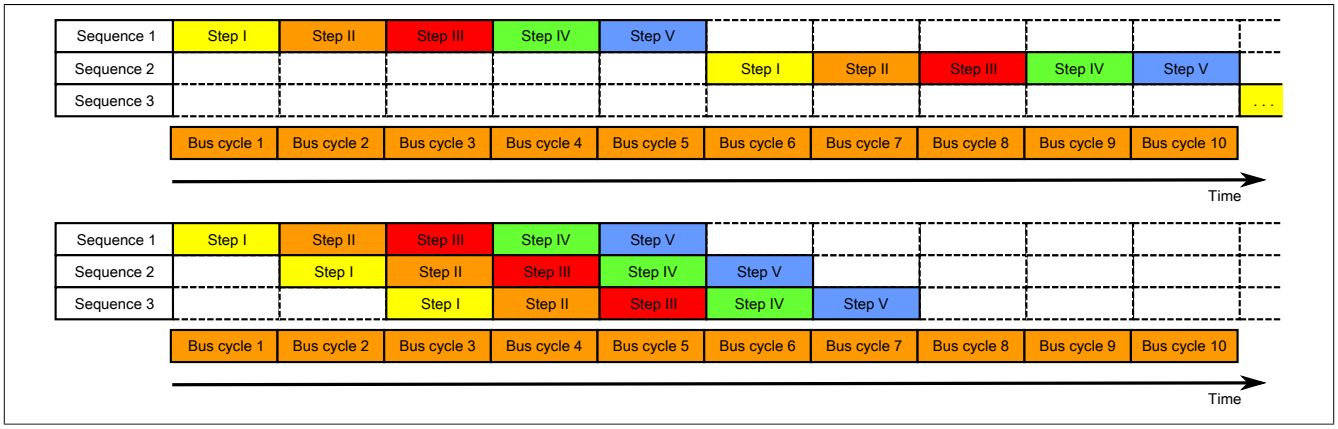


Figure 345: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

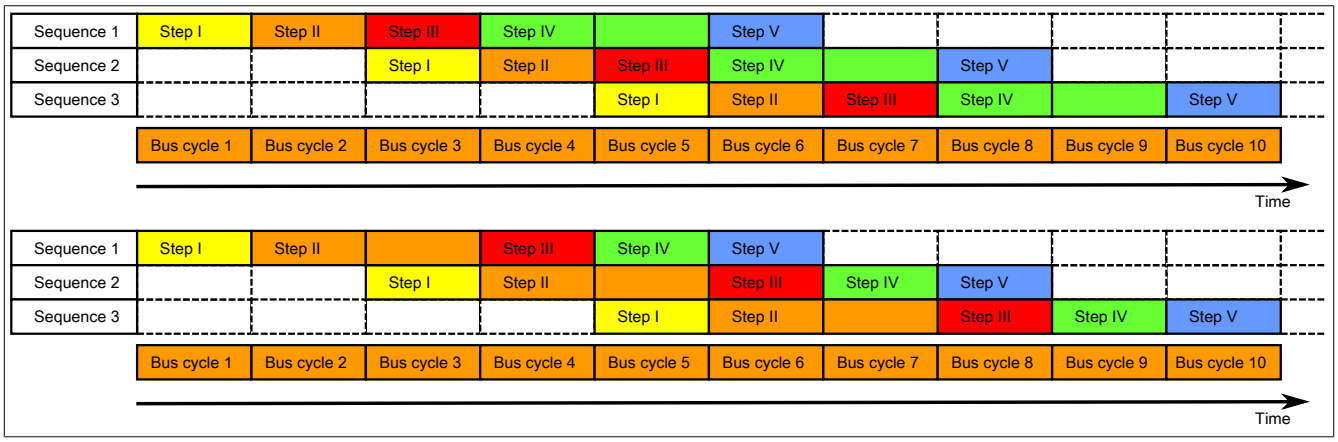


Figure 346: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

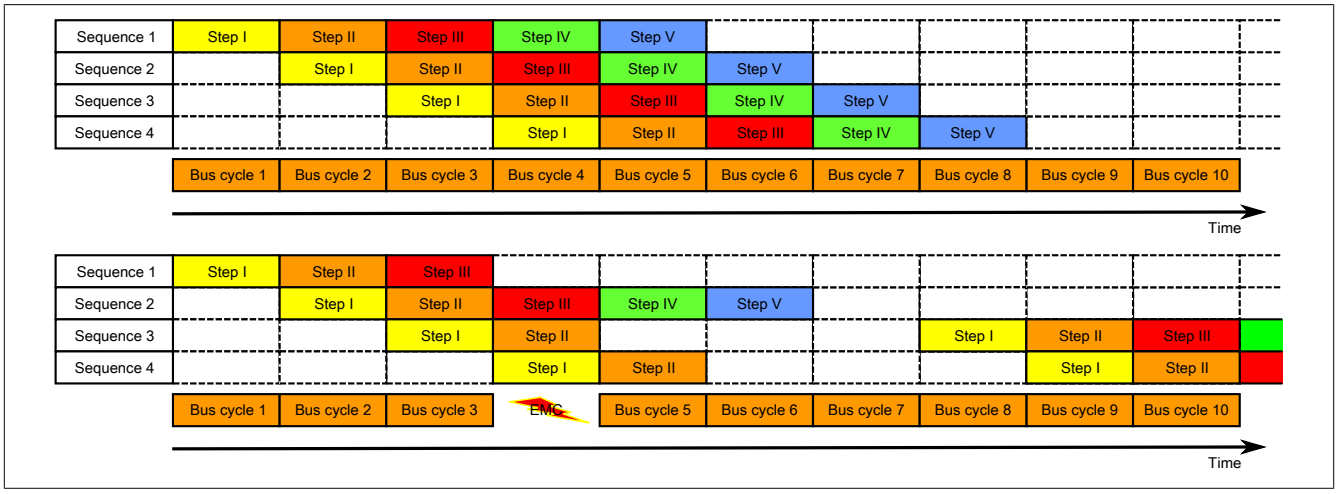


Figure 347: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.18.7.8.13 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

4.18.7.8.14 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.18.7.8.15 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.18.8 X20CS2770

4.18.8.1 General information

In addition to the standard I/O, complex devices often need to be connected. The X20 CS communication modules are intended precisely for cases like this. As normal X20 electronics modules, they can be placed anywhere on the remote backplane.

- 2 CAN bus interfaces for serial, remote connection of complex devices to the X20 system
- Integrated terminating resistors

4.18.8.2 Order data

Model number	Short description	Figure
	X20 electronics module communication	
X20CS2770	X20 interface module, 2x CAN, max. 1 Mbit/s, object buffer in transmit and receive direction	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 421: X20CS2770 - Order data

4.18.8.3 Technical data

Product ID	X20CS2770
Short description	
Communication module	2x CAN bus
General information	
B&R ID code	0xA009
Status indicators	Data transfer, terminating resistor, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
IF1 - Bus	Yes
IF1 - I/O supply	Yes
IF1 - IF2	Yes
IF2 - Bus	Yes
IF2 - I/O supply	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2	Yes
KC	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Signal	CAN bus
Design	Connection made using 12-pin X20TB12 terminal block
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Terminating resistor	Integrated in the module
Controller	SJA 1000
IF2 interface	
Signal	CAN bus
Design	Connection made using 12-pin X20TB12 terminal block
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Terminating resistor	Integrated in the module
Controller	SJA 1000
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 422: X20CS2770 - Technical data

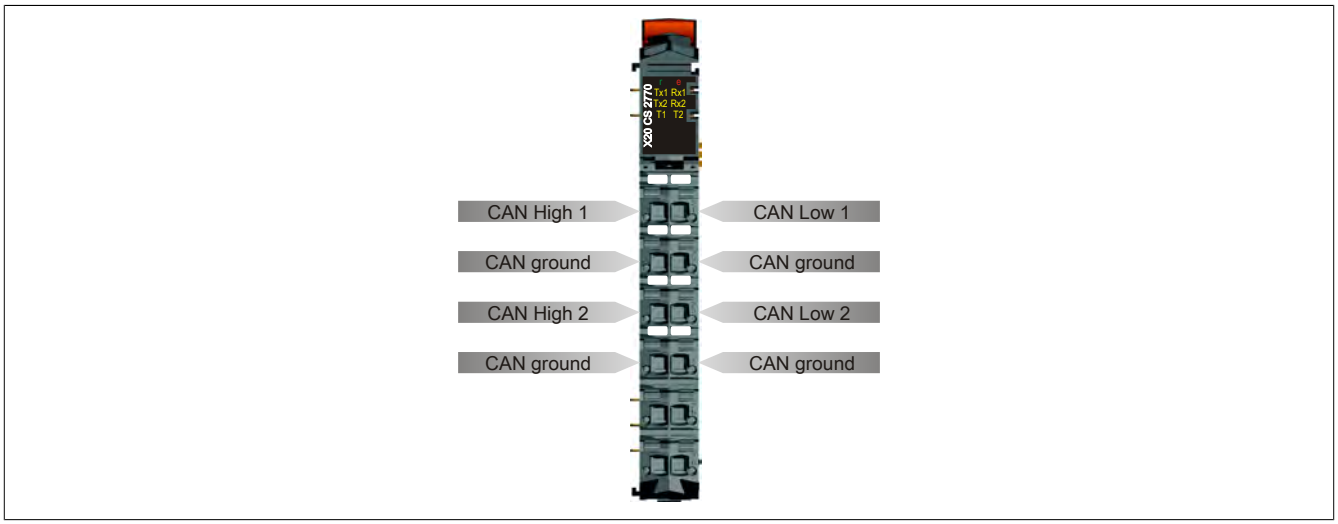
4.18.8.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

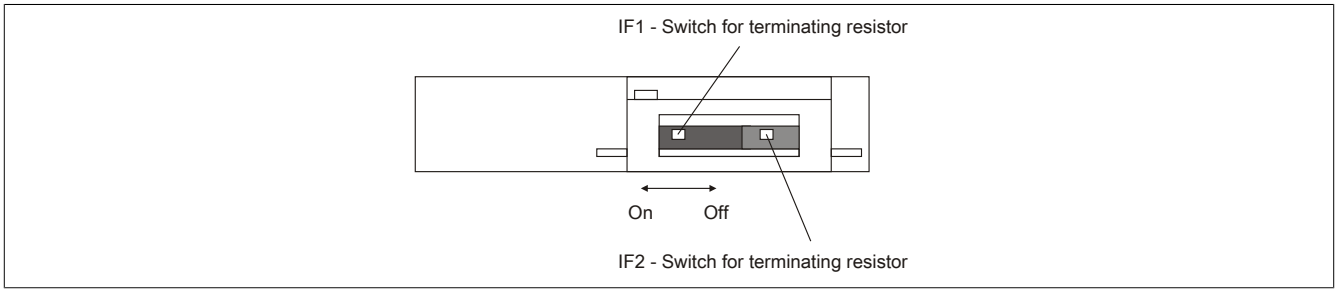
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	I/O error occurred • CAN bus: Warning, passive or off • Buffer overflow
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	Tx1/2	Yellow	On	The module is sending data via the CAN bus interface IF1/IF2
	Rx1/2	Yellow	On	The module is receiving data via the CAN bus interface IF1/IF2
	T1/2	Yellow	On	The integrated terminating resistor for the CAN bus interface IF1/IF2 is turned on

1) Depending on the configuration, a firmware update can take up to several minutes.

4.18.8.5 Pinout



4.18.8.6 Terminating resistors

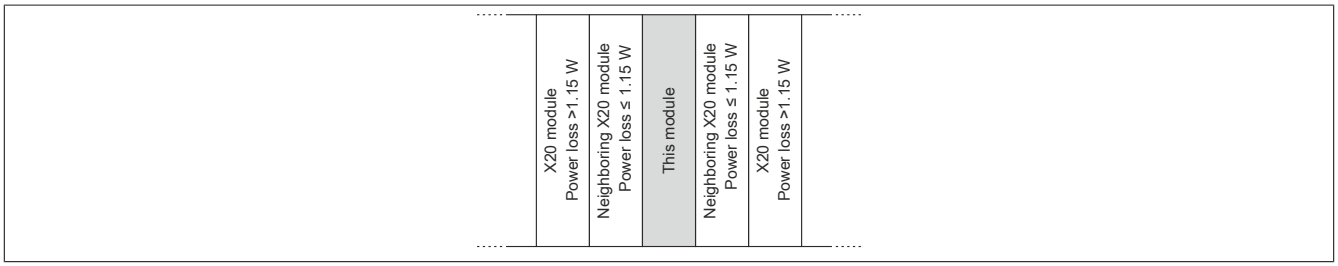


Two terminating resistors are integrated in the communication module. The respective resistor can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "T1" or "T2" LED.

4.18.8.7 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.18.8.8 Register description

4.18.8.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.18.8.8.2 Function model 0 - Flat

In the "Flat" function model, CAN information is transferred via cyclic input and output registers. All data for a CAN object (8 CAN data bytes, identifier, status, etc.) is accessible as individual data points (see also 4.18.7.8.7 "CAN object" on page 2042).

To transmit a CAN object, the CAN identifier, the CAN data (max. 8 bytes) and the number of bytes to be transmitted must be written to the cyclic I/O data points. Then, "TX0[x]Count" is increased to send the transmission. The data is held in the module's internal buffer (max. 18 objects) and transmitted over the CAN network at the next available opportunity.

Receiving information from the CAN network uses the same algorithm. The module saves the CAN messages in its internal buffer along with the respective identifiers. Then the CAN identifier, the CAN data (max. 8 bytes) and the number of bytes to be processed are written to the cyclic I/O data points. RX0[x]Count tells the application how much new data must be taken from these input data points.

Information:

- **The "CAN_Lib" library can't be used.**

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Interface - Configuration						
257	Config01Baudrate	USINT				•
259	Config01SJW	USINT				•
261	Config01SPO	USINT				•
266	Config01TXtrigger	UINT				•
673	Cfo_FIFOTXlimit01	USINT				•
677	Cfo_TXRXinfoFlags01	USINT				•
769	Config02Baudrate	USINT				•
771	Config02SJW	USINT				•
773	Config02SPO	USINT				•
778	Config02TXtrigger	UINT				•
1185	Cfo_FIFOTXlimit02	USINT				•
1189	Cfo_TXRXinfoFlags02	USINT				•
Interface - Communication						
641	TX01Count	USINT			•	
513	TX01CountReadBack	USINT	•			
515	RX01Count	USINT	•			
1153	TX02Count	USINT			•	
1025	TX02CountReadBack	USINT	•			
1027	RX02Count	USINT	•			
Transmit buffer IF1						
645	TX01DataSize	USINT			•	
652	TX01Ident	UDINT			•	
Index * 2 + 657	TX01DataByte0 to TX01DataByte7	USINT			•	
Index * 4 + 658	TX01DataWord0 to TX01DataWord3	UINT			•	
Index * 8 + 660	TX01DataLong0 to TX01DataLong1	UDINT			•	
Receive buffer IF1						
517	RX01DataSize	USINT	•			
524	RX01Ident	UDINT	•			
Index * 2 + 529	RX01DataByte0 to RX01DataByte7	USINT	•			
Index * 4 + 530	RX01DataWord0 to RX01DataWord3	UINT	•			
Index * 8 + 532	RX01DataLong0 to RX01DataLong1	UDINT	•			
Transmit buffer IF2						
1157	TX02DataSize	USINT			•	
1164	TX02Ident	UDINT			•	
Index * 2 + 1170	TX02DataByte0 to TX02DataByte7	USINT			•	
Index * 4 + 658	TX02DataWord0 to TX02DataWord3	UINT			•	
Index * 8 + 1172	TX02DataLong0 to TX02DataLong1	UDINT			•	
Receive buffer IF2						
1029	RX02DataSize	USINT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
1036	RX02Ident	UDINT	•			
Index * 2 + 1041	RX02DataByte0 to RX02DataByte7	USINT	•			
Index * 4 + 1042	RX02DataWord0 to RX02DataWord3	UINT	•			
Index * 8 + 1044	RX02DataLong0 to RX02DataLong1	UDINT	•			

4.18.8.8.3 Function model 2 - Stream and Function model 254 - Cyclic stream

The "Stream" and "Cyclic stream" function models use a module-specific driver for the CPU's operating system. The interface can be controlled using the "CAN_Lib" library and be reconfigured at runtime.

Function model - Stream

In the "Stream" function model, the CPU communicates with the module acyclically. The interface is relatively convenient, but the timing is very imprecise.

Function model - Cyclic stream

The "Cyclic stream" function model was implemented later. From the application's point of view, there is no difference between the "Stream" and "Cyclic stream" function models. Internally, however, the cyclic I/O registers are used to ensure that communication follows deterministic timing.

Information:

- **In order to use the "Stream" and "Cyclic stream" function models, you must be using B&R controllers of the type "SG4".**

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Module - Configuration						
-	AsynSize	-				
Interface - Configuration						
6273	CfO_ErrorID0007	USINT				•
Interface - Communication						
6145	CAN error status	USINT	•			
	CANIF1warning	Bit 0				
	CANIF1passive	Bit 1				
	CANIF1busoff	Bit 2				
	CANIF1RXoverrun	Bit 3				
	CANIF2warning	Bit 4				
	CANIF2passive	Bit 5				
	CANIF2busoff	Bit 6				
	CANIF2RXoverrun	Bit 7				
6209	CAN error acknowledgment	USINT			•	
	QuitCANIF1warning	Bit 0				
	QuitCANIF1passive	Bit 1				
	QuitCANIF1bussoff	Bit 2				
	QuitCANIF1RXoverrun	Bit 3				
	QuitCANIF2warning	Bit 4				
	QuitCANIF2passive	Bit 5				
	QuitCANIF2bussoff	Bit 6				
	QuitCANIF2RXoverrun	Bit 7				

4.18.8.8.4 Function model 254 - FlatStream

The "FlatStream" function model provides independent communication between an X2X Link master and the module. This interface was implemented as a separate function model for the CAN module. CAN information (identifier, status, etc.) is transferred via cyclic input and output registers. The sequence and control bytes are used to control this data stream (see 4.3.7.10.8 "FlatStream communication" on page 223).

When using the Flatstream function model, the user can choose whether to use the "AsFltGen" library in AS for implementation or to adapt Flatstream handling directly to the individual requirements of the application.

Information:

- **The "CAN_Lib" library can't be used.**
- **Higher data rates can be achieved between X2X master and module compared to the "Flat" function model.**

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Interface - Configuration						
257	Config01Baudrate	USINT				•
259	Config01SJW	USINT				•
261	Config01SPO	USINT				•
266	Config01TXtrigger	UINT				•
769	Config02Baudrate	USINT				•
771	Config02SJW	USINT				•
773	Config02SPO	USINT				•
778	Config02TXtrigger	UINT				•
6273	CfO_ErrorID0007	USINT				•
Interface - Communication						
6145	CAN error status	USINT	•			
	CANIF1warning	Bit 0				
	CANIF1passive	Bit 1				
	CANIF1busoff	Bit 2				
	CANIF1RXoverrun	Bit 3				
	CANIF2warning	Bit 4				
	CANIF2passive	Bit 5				
	CANIF2busoff	Bit 6				
	CANIF2RXoverrun	Bit 7				
6209	CAN error acknowledgment	USINT			•	
	QuitCANIF1warning	Bit 0				
	QuitCANIF1passive	Bit 1				
	QuitCANIF1bussoff	Bit 2				
	QuitCANIF1RXoverrun	Bit 3				
	QuitCANIF2warning	Bit 4				
	QuitCANIF2passive	Bit 5				
	QuitCANIF2bussoff	Bit 6				
	QuitCANIF2RXoverrun	Bit 7				
FlatStream - Configuration						
193	output01MTU	USINT				•
195	input01MTU	USINT				•
197	mode01	USINT				•
199	forward01	USINT				•
206	forwardDelay01	UINT				•
209	output02MTU	USINT				•
211	input02MTU	USINT				•
213	mode02	USINT				•
215	forward02	USINT				•
222	forwardDelay02	UINT				•
FlatStream - Communication						
0	Input01Sequence	USINT	•			
64	Input02Sequence	USINT	•			
Index * 1 + 0	Rx01Byte1 to Rx01Byte27	USINT	•			
Index * 1 + 64	Rx02Byte1 to Rx02Byte27	USINT	•			
32	Output01Sequence	USINT			•	
96	Output02Sequence	USINT			•	
Index * 1 + 32	Tx01Byte1 to Tx01Byte27	USINT			•	
Index * 1 + 96	Tx02Byte1 to Tx02Byte27	USINT			•	

4.18.8.8.5 Function model 254 - Bus controller

The "Bus controller" function model is a reduced form of the "FlatStream" function model. Instead of up to 27 Tx / Rx bytes, a maximum of 7 Tx / Rx bytes can be used.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Interface - Configuration							
257	-	Config01Baudrate	USINT				•
259	-	Config01SJW	USINT				•
261	-	Config01SPO	USINT				•
266	-	Config01TXtrigger	UINT				•
769	-	Config02Baudrate	USINT				•
771	-	Config02SJW	USINT				•
773	-	Config02SPO	USINT				•
778	-	Config02TXtrigger	UINT				•
6273	-	CfO_ErrorID0007	USINT				•
Interface - Communication							
6145	-	CAN error status	USINT		•		
		CANIF1warning	Bit 0				
		CANIF1passive	Bit 1				
		CANIF1busoff	Bit 2				
		CANIF1RXoverrun	Bit 3				
		CANIF2warning	Bit 4				
		CANIF2passive	Bit 5				
		CANIF2busoff	Bit 6				
		CANIF2RXoverrun	Bit 7				
6209	-	CAN error acknowledgment	USINT				•
		QuitCANIF1warning	Bit 0				
		QuitCANIF1passive	Bit 1				
		QuitCANIF1bussoff	Bit 2				
		QuitCANIF1RXoverrun	Bit 3				
		QuitCANIF2warning	Bit 4				
		QuitCANIF2passive	Bit 5				
		QuitCANIF2bussoff	Bit 6				
		QuitCANIF2RXoverrun	Bit 7				
FlatStream - Configuration							
193	-	output01MTU	USINT				•
195	-	input01MTU	USINT				•
197	-	mode01	USINT				•
199	-	forward01	USINT				•
206	-	forwardDelay01	UINT				•
209	-	output02MTU	USINT				•
211	-	input02MTU	USINT				•
213	-	mode02	USINT				•
215	-	forward02	USINT				•
222	-	forwardDelay02	UINT				•
FlatStream - Communication							
0	0	Input01Sequence	USINT	•			
64	8	Input02Sequence	USINT	•			
Index * 1 + 0	Index * 1 + 0	Rx01Byte1 to Rx01Byte7	USINT	•			
Index * 1 + 64	Index * 1 + 8	Rx02Byte1 to Rx02Byte7	USINT	•			
32	0	Output01Sequence	USINT			•	
96	8	Output02Sequence	USINT			•	
Index * 1 + 32	Index * 1 + 0	Tx01Byte1 to Tx01Byte7	USINT			•	
Index * 1 + 96	Index * 1 + 8	Tx02Byte1 to Tx02Byte7	USINT			•	

1) The offset specifies the position of the register within the CAN object.

4.18.8.8.5.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.18.8.8.6 Using this module with SGC target systems

Note:

This module can only be used with SGC target systems if the function model is set to "Flatstream" or "Flat".

4.18.8.8.7 CAN object

A CAN object is always made up of a 4-byte identifier and a maximum of 8 subsequent data bytes. This also results in the relationship between CAN object length and the amount of CAN payload data. This is important because the number of CAN payload data bytes for communication via "FlatStream" always has to be determined using the frame length.

Composition of a CAN object / CAN frame

Bytes	Function	Information
1	Code	ID bit 0 to 7
2		ID bit 8 to 15
3		ID bit 16 to 23
4		ID bit 24 to 31
5 - 12	CAN payload data	0 to 8 CAN payload data bytes

Code

The 32 bits (4 bytes) of the CAN identifier are used as follows:

Bit	Description	Value	Information
0	Frame format	0	Standard frame format (SFF) with an 11-bit identifier
		1	Extended frame format (EFF) with an 29-bit identifier
1	Frame type	0	Data frame
		1	Remote frame (RTR)
2	Reserved	-	
3 - 31	CAN identifier for telegram to be transmitted	x	Extended frame format (EFF) with 29 bits Standard frame format (SFF) with 11 bits[1)]

1) Only bits 21 to 31 used; bits 3 to 20 = 0

4.18.8.8.7.1 CAN module data stream

In function model 254, the data packets to be transferred in a data stream are referred to as frames.

Information:

For the CAN module, that means:

- **A frame always contains one CAN object and therefore cannot be longer than 12 bytes.**
- **The CAN object is only transferred to the transmit buffer after the frame has been completed.**
- **The CAN payload data length has a fixed relationship with the frame length and the actual size of the CAN object. The following rules apply:**
  - **CAN payload data length = Frame length - 4**
  - **Frame length = CAN payload data length + 4**

4.18.8.8.8 Interface - Configuration

4.18.8.8.8.1 Transfer rate

Name:
Config01Baudrate
Config02Baudrate

"Baud rate" in the AS I/O configuration.

Configuration of the CAN transfer rate for the respective interface.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Transfer rate	1	10 kbit/s
		2	20 kbit/s
		3	50 kbit/s
		4	100 kbit/s
		5	125 kbit/s
		6	250 kbit/s
		7	500 kbit/s (default)
		8	800 kbit/s
		9	1000 kbit/s
4 - 7	Reserved	-	

4.18.8.8.8.2 Synchronization Jump Width

Name:
Config01SJW
Config02SJW

"Synchronization jump width" in the AS I/O configuration.

The synchronization jump width (SJW) is used to resynchronize the sample point within a CAN telegram.

A detailed description of the SJW can be found in the CAN specification.

Data type	Value	Meaning
USINT	0 to 4	Synchronization jump width (default = 3)

4.18.8.8.8.3 Offset for the sampling instant

Name:
Config01SPO
Config02SPO

"Sample point offset" in the AS I/O configuration.

Offset for the sample point of the individual bits on the CAN bus.

A detailed description of the SPO can be found in the CAN specification.

Data type	Value	Meaning
USINT	0 to 1	Sample point offset (default = 0)

4.18.8.8.8.4 Start of transmission

Name:
Config01TXtrigger
Config02TXtrigger

"TX objects / TX triggers" in the AS I/O configuration.

Defines the number of CAN objects that must be copied to the transmit buffer before the transmission is started.

Data type	Value	Meaning
UINT	0 to 8	Number of CAN objects in the transmit buffer before transmission is started (default = 1)

4.18.8.8.8.5 Configuration of error messages

Name:
CfO_ErrorID0007

This register must be used first to configure the error messages that have to be transferred. If the corresponding enable bit is not set, no error status will be sent to the higher-level system when the error occurs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	CANIF1warning	0	Disabled
		1	Enabled
1	CANIF1passive	0	Disabled
		1	Enabled
2	CANIF1bussoff	0	Disabled
		1	Enabled
3	CANIF1RXoverrun	0	Disabled
		1	Enabled
4	CANIF2warning	0	Disabled
		1	Enabled
5	CANIF2passive	0	Disabled
		1	Enabled
6	CANIF2bussoff	0	Disabled
		1	Enabled
7	CANIF2RXoverrun	0	Disabled
		1	Enabled

4.18.8.8.8.6 Size of the transmit buffer

Name:
Cfo_FIFOTXlimit01
Cfo_FIFOTXlimit02

"TX FIFO size" in the AS I/O configuration.

Determines the size of the transmit buffer for the respective interface.

Data type	Value	Meaning
USINT	0 to 18	Size of the transmit buffer (default = 1)

4.18.8.8.8.7 Display of unprocessed elements remaining in transmit/receive buffer

Name:
Cfo_TXRXinfoFlags01
Cfo_TXRXinfoFlags02

This register can be used to specify that the number of unprocessed elements in the transmit and receive buffers is indicated in the upper 4 bits of the "TX0[x]CountReadBack" and "RX0[x]Count" registers for the respective interface.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TxFifoInfo "Mode of channel TX0[x]CountReadBack" in the AS I/O configuration	0	The "TX0[x]Count" is read in the "TX0[x]CountReadBack" on page 2091 register.
		1	The "TX0[x]Count" is read in the "TX0[x]CountReadBack" on page 2091 register. The upper 4 bits are used to return the number of frames in the transmit buffer that have not been transmitted.
1	RxFifoInfo "Mode of channel RX0[x]Count" in the AS I/O configuration	0	The number of received telegrams is shown in the "RX0[x]Count" on page 2091 register.
		1	The number of received telegrams is shown in the lower 4 bits of the "RX0[x]Count" on page 2091 register. The upper 4 bits are used to indicate the number of received but not acknowledged telegrams in the receive buffer.
2 - 7	Reserved	-	

4.18.8.8.9 Interface - Communication

4.18.8.8.9.1 CAN error status

Name:
CAN error status

The bits in this register indicate the error states defined in the CAN protocol. If an error occurs, the corresponding bit is set. For an error bit to be reset, the corresponding bit must be acknowledged (see 4.18.8.8.9.2 "CAN error acknowledgment" on page 2090).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	CANIF1warning	0	No error
		1	CANwarning error on IF1
1	CANIF1passive	0	No error
		1	CANpassive error on IF1
2	CANIF1busoff	0	No error
		1	CANbusoff error on IF1
3	CANIF1RXoverrun	0	No error
		1	CANRXoverrun error on IF1
4	CANIF2warning	0	No error
		1	CANwarning error on IF2
5	CANIF2passive	0	No error
		1	CANpassive error on IF2
6	CANIF2busoff	0	No error
		1	CANbusoff error on IF2
7	CANIF2RXoverrun	0	No error
		1	CANRXoverrun error on IF2

4.18.8.8.9.2 CAN error acknowledgment

Name:
CAN error acknowledgment

Setting the bits in this register acknowledges the error assigned to the bit and clears the corresponding bit in the "CAN error status" register. The application thus informs the module that it has recognized the error state.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	QuitCANIF1warning	0	No acknowledgment
		1	Acknowledge CANwarning error on IF1
1	QuitCANIF1passive	0	No acknowledgment
		1	Acknowledge CANpassive error on IF1
2	QuitCANIF1bussoff	0	No acknowledgment
		1	Acknowledge CANbusoff error on IF1
3	QuitCANIF1RXoverrun	0	No acknowledgment
		1	Acknowledge CANRXoverrun error on IF1
4	QuitCANIF2warning	0	No acknowledgment
		1	Acknowledge CANwarning error on IF2
5	QuitCANIF2passive	0	No acknowledgment
		1	Acknowledge CANpassive error on IF2
6	QuitCANIF2bussoff	0	No acknowledgment
		1	Acknowledge CANbusoff error on IF2
7	QuitCANIF2RXoverrun	0	No acknowledgment
		1	Acknowledge CANRXoverrun error on IF2

4.18.8.8.9.3 New CAN telegram for transmit buffer

Name:
TX01Count
TX02Count

By increasing this value, the application notifies the module that a new CAN telegram should be transferred into the transmit buffer.

Data type	Value
USINT	0 to 255

4.18.8.8.9.4 Read "TX0[x]Count"

Name:
TX01CountReadBack
TX02CountReadBack

The value of "TX0[x]Count" is copied from the module into this register. This makes it possible for the application task to verify that the CAN telegram data was transfered from the module correctly.

The meaning of the value depends on the "TxFifoInfo" bit. This is located in the Cfo_TXRXinfoFlags0[x] register.

Data type	Value	"TxFifoInfo" bit	Meaning
USINT	0 to 255	0	Read "TX0[x]Count"
		1	See bit structure.

Bit structure:

Bit	Function	Value	Information
0 - 3	Read "TX0[x]Count"	0 to 15	Only the lower 4 bits
4 - 7	Number of frames in the transmit buffer that have not been transmitted	0 to 15	If this number exceeds the 15 (a maximum of 18 possible), the value 15 is returned.

4.18.8.8.9.5 Counter for received CAN telegrams

Name:
RX01Count
RX02Count

This counter is increased by 1 with each CAN telegram. The application task can thus detect when new data is received and get it from the corresponding "RX0[x]Data" registers.

The meaning of the value depends on the "Cfo_TXRXinfoFlags0[x]" on page 2089 bit in the "Cfo_TXRXinfoFlags" register.

Data type	Value	"RxFifoInfo" bit	Meaning
USINT	0 to 255	0	Counter for received telegrams
		1	See bit structure.

Bit structure:

Bit	Function	Value	Information
0 - 3	Counter for received telegrams	0 to 15	Only the lower 4 bits
4 - 7	Number of unacknowledged telegrams in the receive buffer	0 to 15	

4.18.8.8.10 Transmit buffer for IF1 and IF2

4.18.8.8.10.1 Number of CAN payload data bytes

Name:
TX01DataSize
TX02DataSize

Number of CAN payload data bytes to be transmitted If a value less than 0 is specified here, this CAN telegram is marked as being invalid and is not transferred into the transmit buffer. This is useful in connection with transmit error detection between the module and the CPU (see 4.18.8.8.10.4 "Taking possible errors into consideration when transmitting" on page 2092).

Data type	Value	Meaning
USINT	-128 to 8	Amount of CAN payload data to be transmitted (Default = 0).

4.18.8.8.10.2 Identifier of the CAN telegram to be transmitted.

Name:
TX01Ident
TX02Ident

Identifier of the CAN telegram to be transmitted. The frame format and the identifier format are also defined in this register.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Frame format	0	Standard frame format (SFF) with an 11-bit identifier
		1	Extended frame format (EFF) with an 29-bit identifier
1	Frame type	0	Data frame
		1	Remote frame (RTR)
2	Reserved	-	
3 - 31	CAN identifier for telegram to be transmitted	x	Extended frame format (EFF) with 29 bits Standard frame format (SFF) with 11 bits[1)]

1) Only bits 21 to 31 used; bits 3 to 20 = 0

4.18.8.8.10.3 Configuration of the CAN payload data being sent

Name:
TX0[x]DataByte0 to TX0[x]DataByte7
TX0[x]DataWord0 to TX0[x]DataWord3
TX0[x]DataLong0 to TX0[x]DataLong1

CAN payload data in the transmit direction. The 8 payload data bytes for a telegram can be used as data points with 8 individual bytes, 4 words or 2 longs as needed.

Data type	Value	Description
USINT	0 to 255	CAN payload data transmitted as bytes
UINT	0 to 65,535	CAN payload data transmitted as words
UDINT	0 to 4.294.967.295	CAN payload data transmitted as longs

4.18.8.8.10.4 Taking possible errors into consideration when transmitting

Data on the POWERLINK network or X2X Link can be lost due to transmission errors. One-time failures of cyclic data are tolerated by the I/O systems. This is possible since all I/O data is re-transferred in the subsequent cycle. A transfer error cannot be detected from the I/O variables; they remain frozen on the value from the last cycle.

These tolerated one-time I/O failures can lead to data loss or the delayed CAN telegram transmission. The counter feedback is derived on the module and used to detect these cases.

Register for counter feedback: "TX0[x]CountReadBack" on page 2091

4.18.8.8.11 Receive buffer for IF1 and IF2

4.18.8.8.11.1 Number of valid CAN payload data bytes

Name:
RX01DataSize
RX02DataSize

Number of valid CAN payload data bytes.

This register also uses the value -1 (0xFF) to indicate a general error or gap in the input data stream. Details regarding the error that has occurred can be seen in the "" on page register.

Data type	Value	Meaning
USINT	1 to 8	Number CAN payload data
	-1	Error

4.18.8.8.11.2 Identifier of the received data

Name:
RX01Ident
RX02Ident

Identifiers assigned to the received data. The frame format and the identifier format can also be read from this register.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Frame format	0	Standard frame format (SFF) with an 11-bit identifier
		1	Extended frame format (EFF) with an 29-bit identifier
1	Frame type	0	Data frame
		1	Remote frame (RTR)
2	Reserved	-	
3 - 31	CAN identifier for telegram to be transmitted	x	Extended frame format (EFF) with 29 bits Standard frame format (SFF) with 11 bits[1)]

1) Only bits 21 to 31 used; bits 3 to 20 = 0

4.18.8.8.11.3 Configuration of the CAN payload data to be received

Name:
RX0[x]DataByte0 to RX0[x]DataByte7
RX0[x]DataWord0 to RX0[x]DataWord3
RX0[x]DataLong0 to RX0[x]DataLong1

These registers hold the payload data of the CAN object to be transferred from the receive buffer to the CPU in the current cycle. If new data is received or if the receive buffer contains additional CAN objects, these registers are overwritten with the new data in the next cycle.

To avoid losing CAN objects, the application must respond immediately to a change in the "RX0[x]Count" and copies the data from these registers.

The maximum 8 bytes for a CAN telegram can be used as data points with 8 individual bytes, 4 words or 2 longs as needed.

Data type	Value	Description
USINT	0 to 255	Received CAN payload data as bytes
UINT	0 to 65,535	Received CAN payload data as words
UDINT	0 to 4.294.967.295	Received CAN payload data as longs

4.18.8.8.12 FlatStream communication

4.18.8.8.12.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

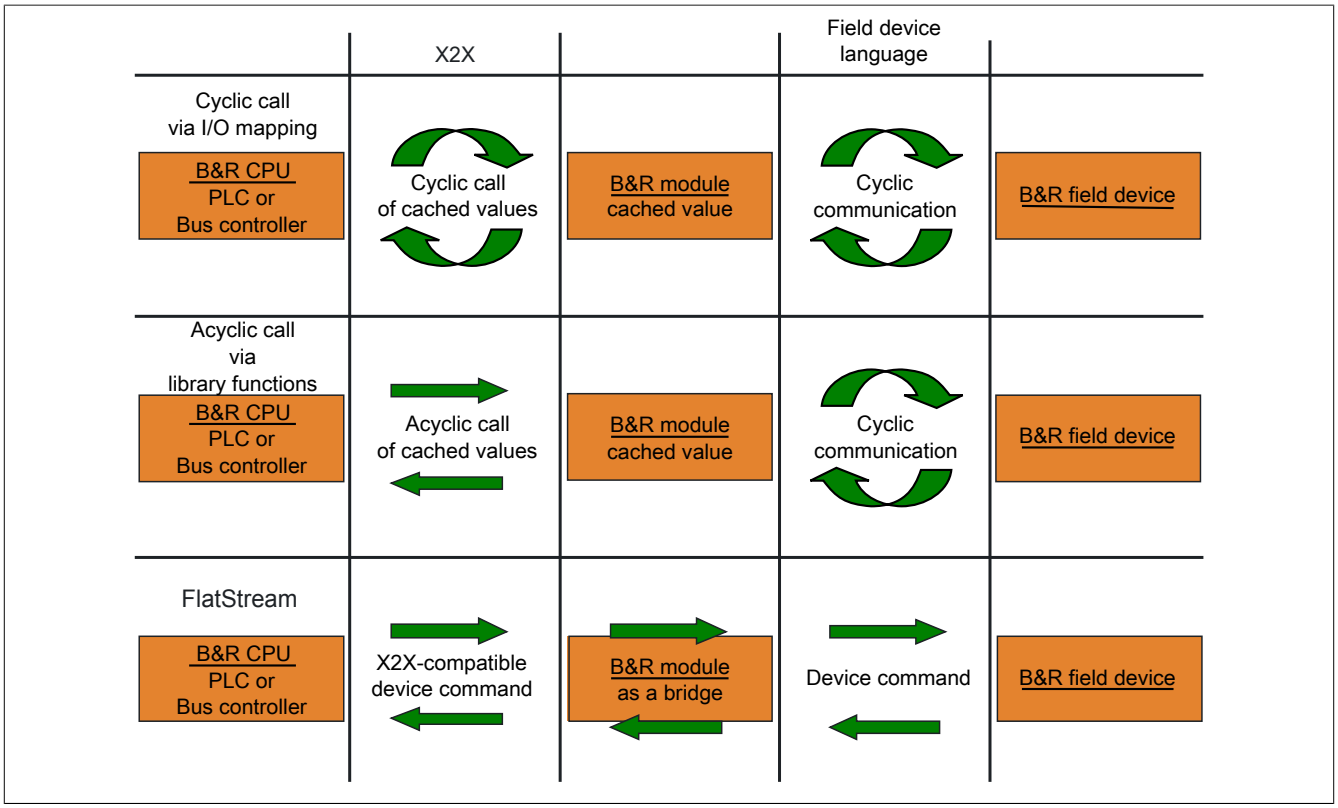


Figure 348: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.18.8.8.12.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.18.8.8.12.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

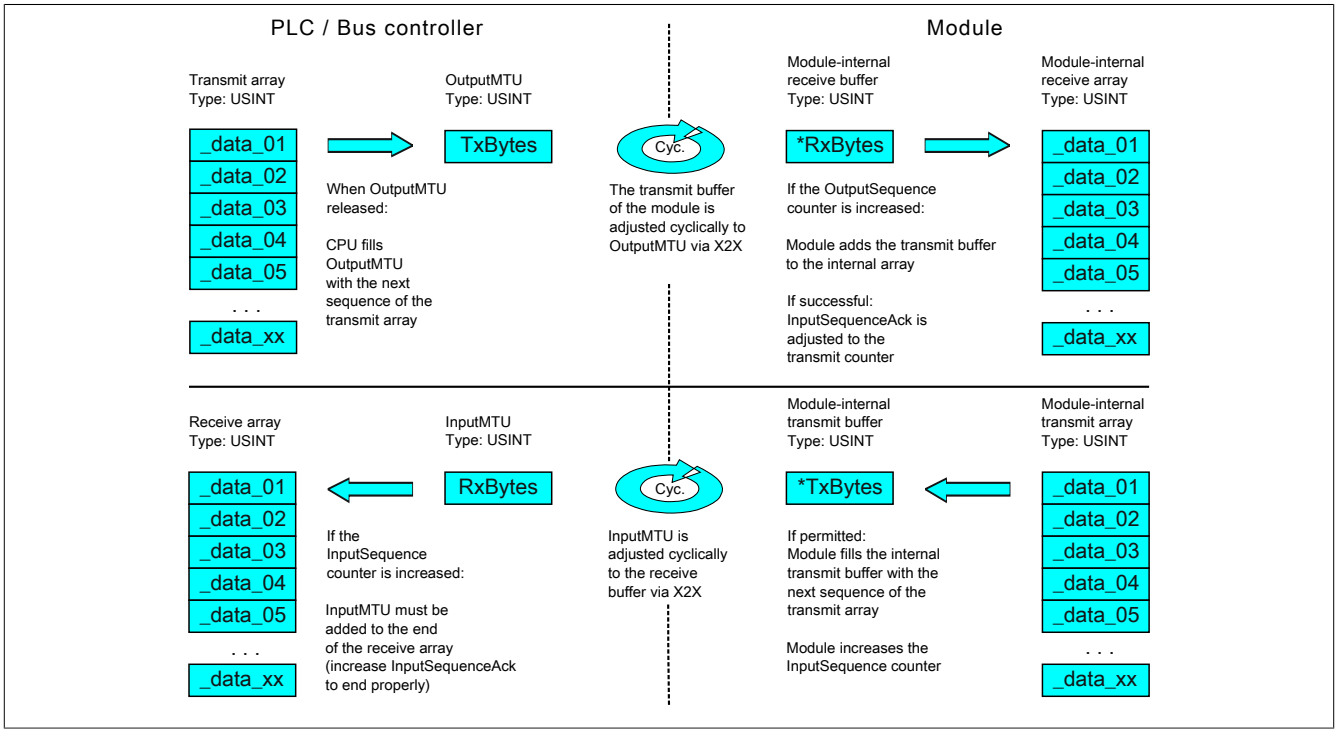


Figure 349: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.18.8.8.12.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Format of input and output bytes

Name:

"Format of Flat stream" in Automation Studio

This function sets how the Flatstream input and output bytes (Tx or Rx bytes) are transferred.

- **packed variable:** Transfers data as an array
- **byte variables:**Transfers data as individual bytes

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

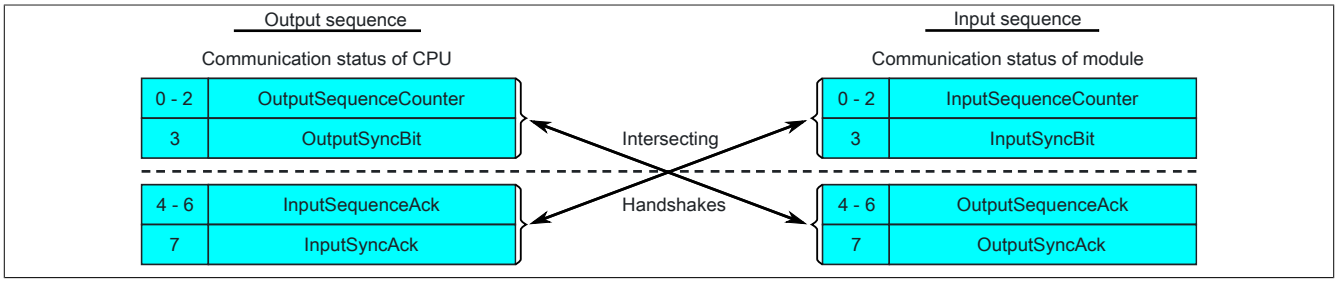


Figure 350: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

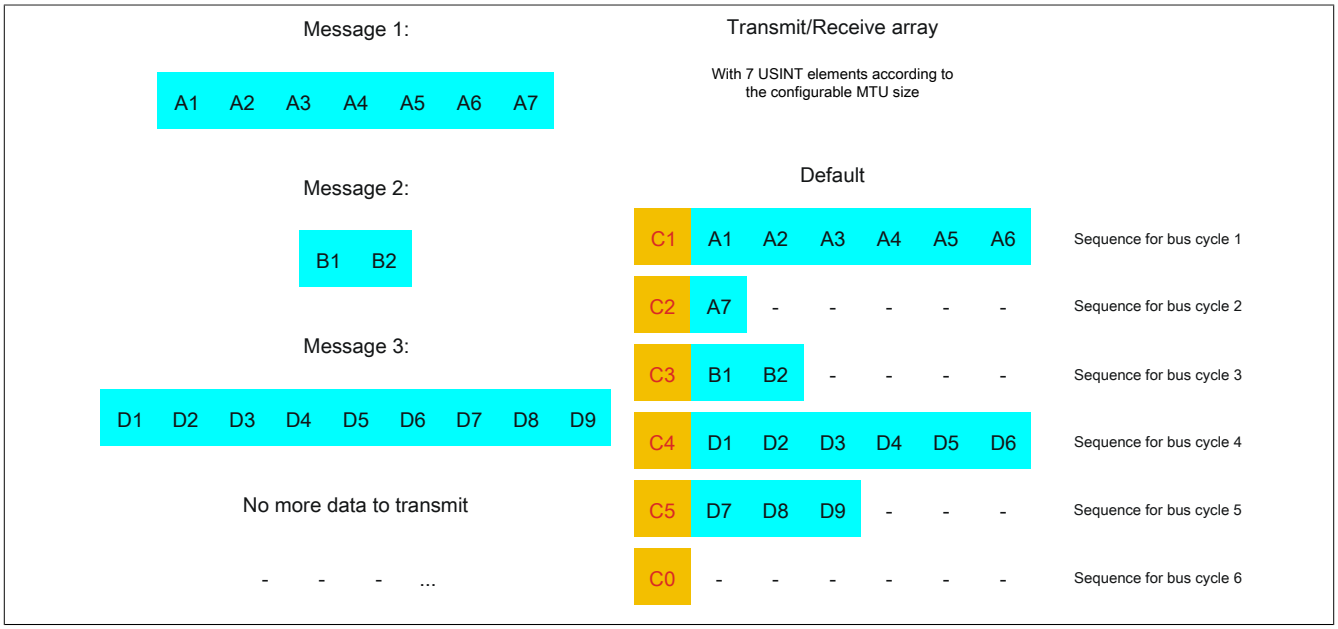


Figure 351: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 423: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 424: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

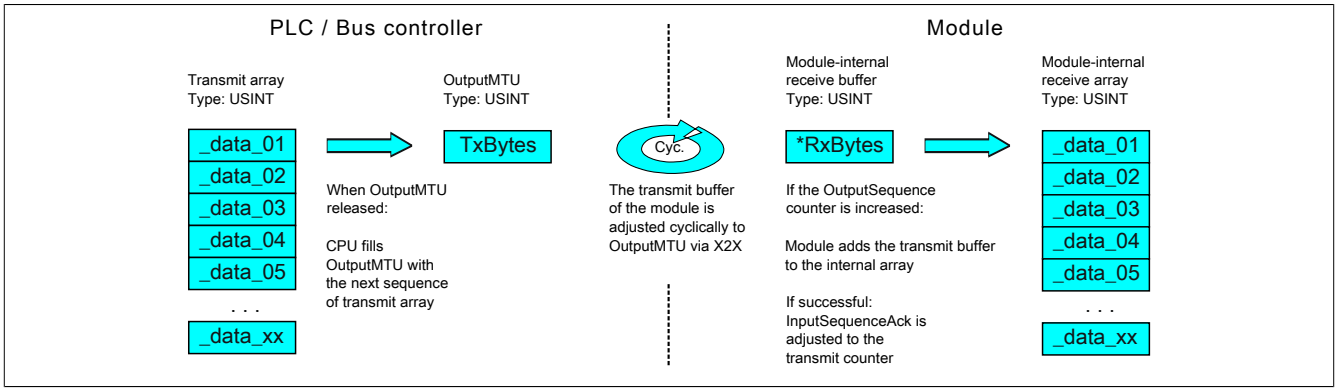


Figure 352: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

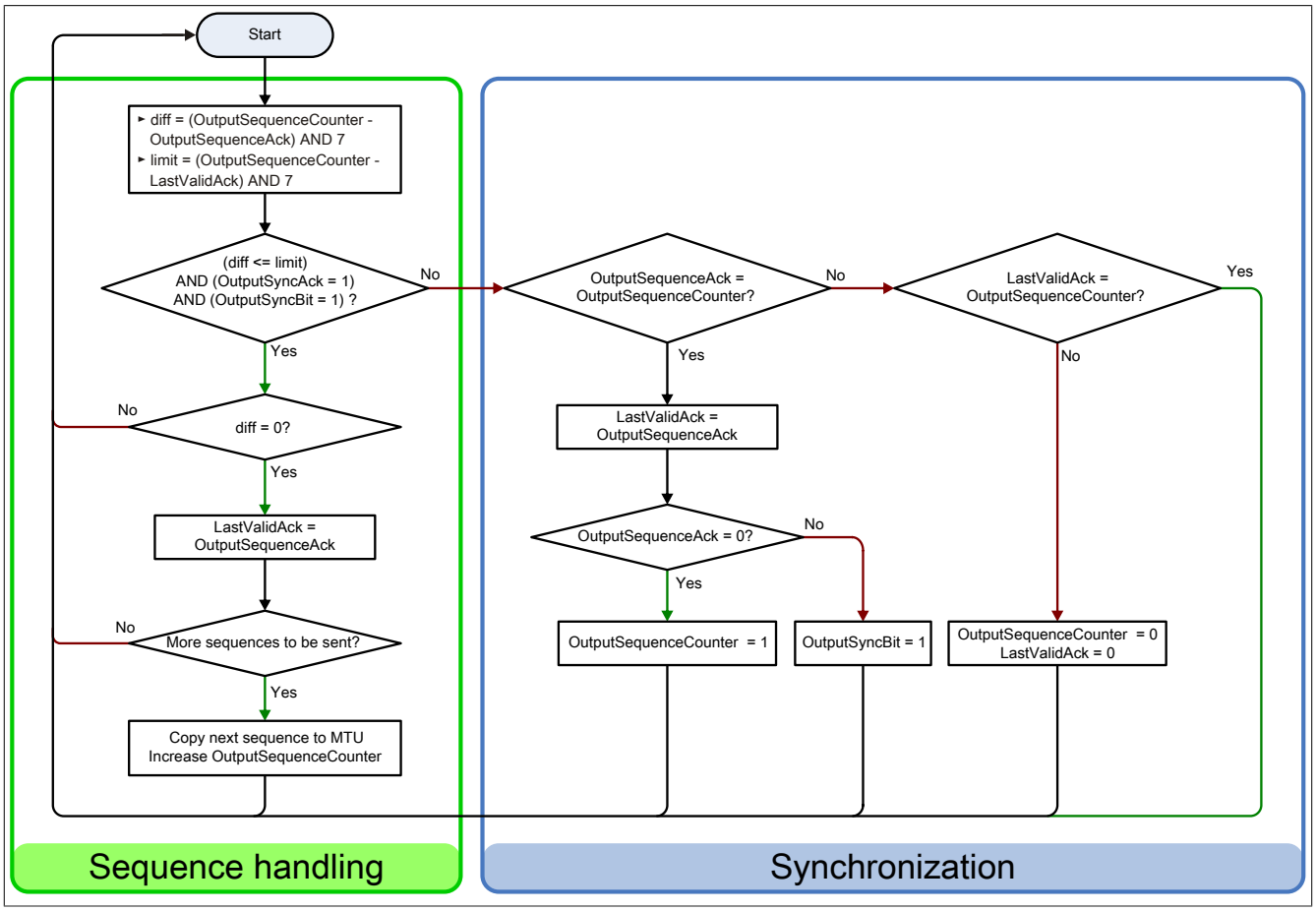


Figure 353: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

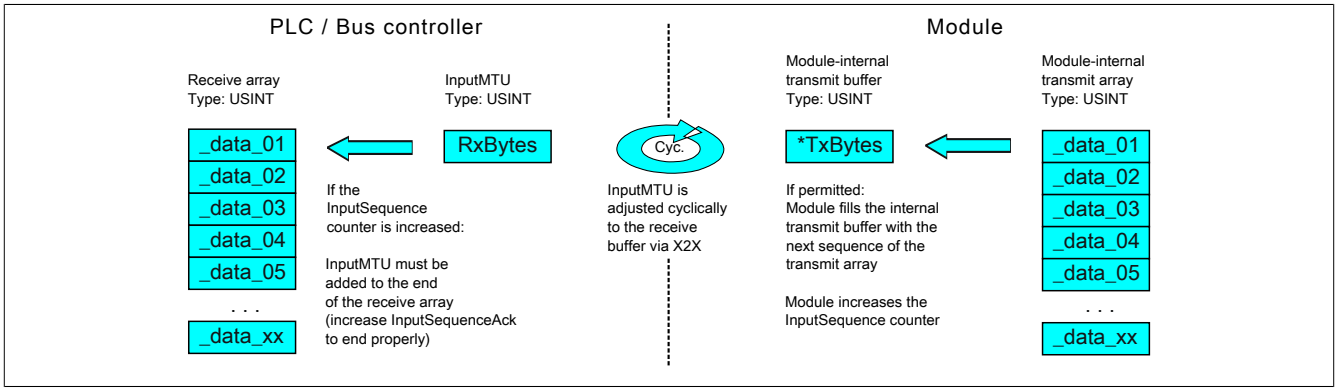


Figure 354: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

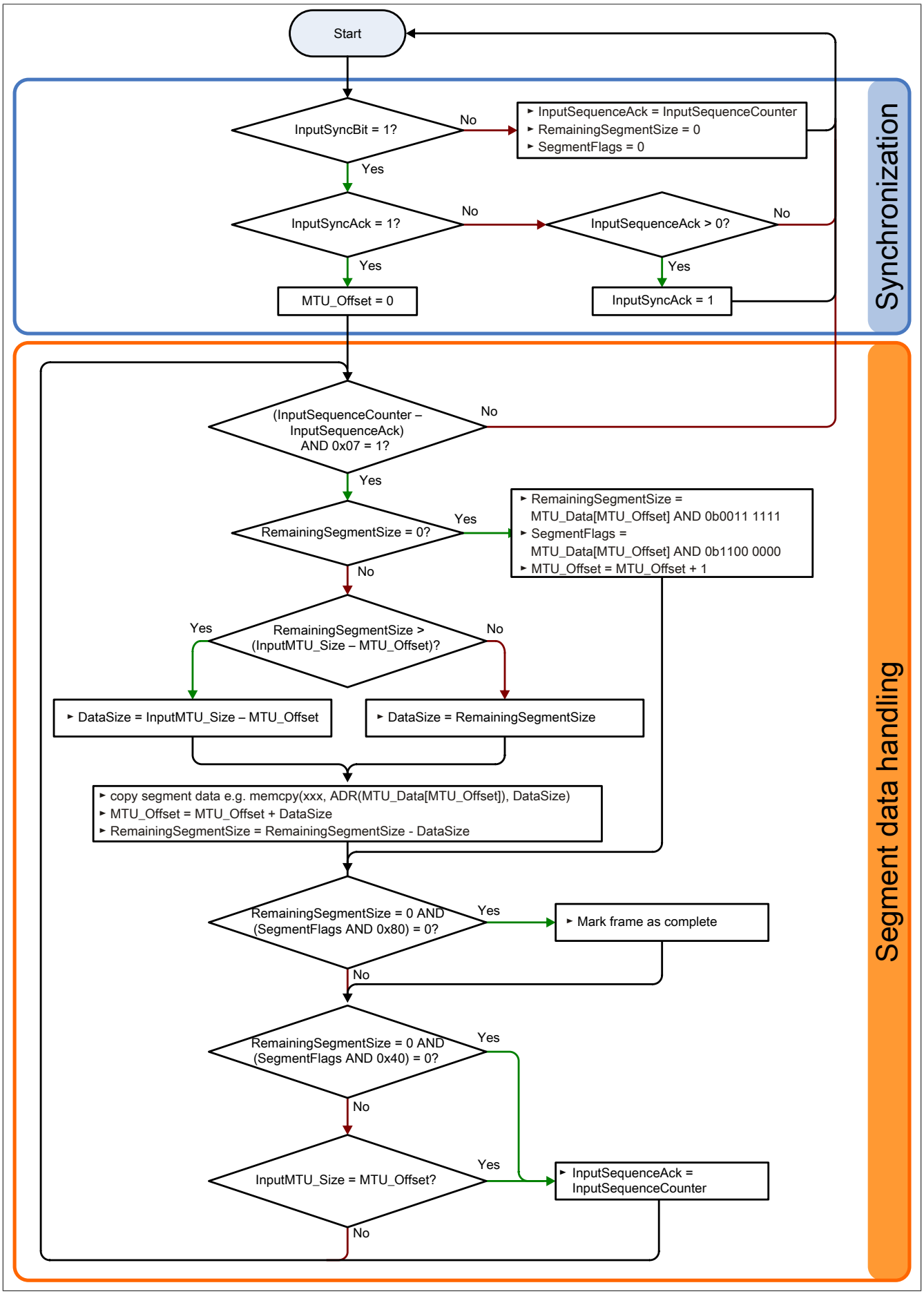


Figure 355: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

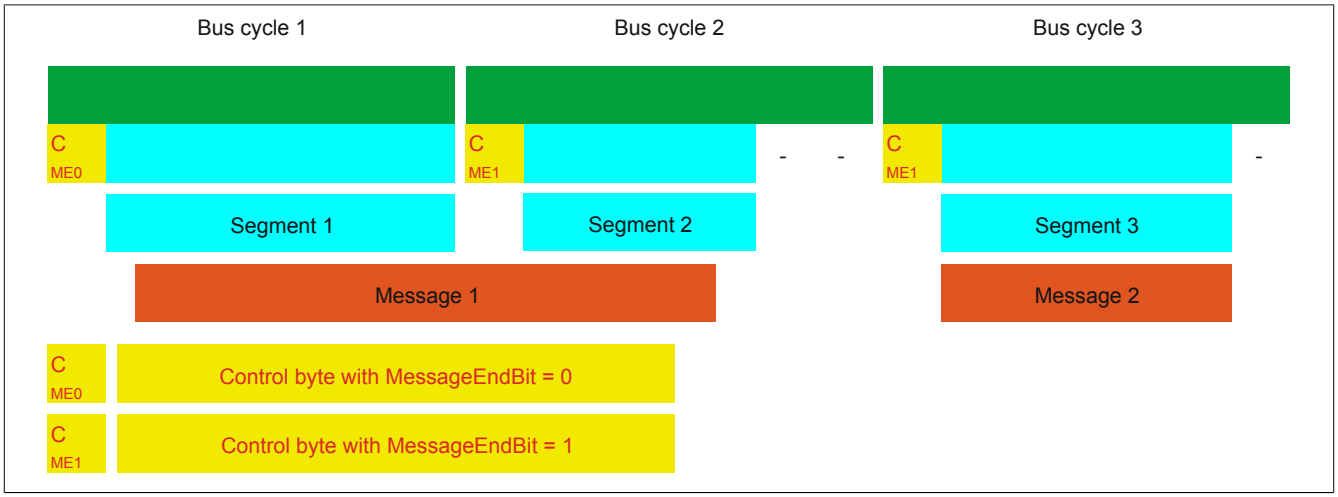


Figure 356: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

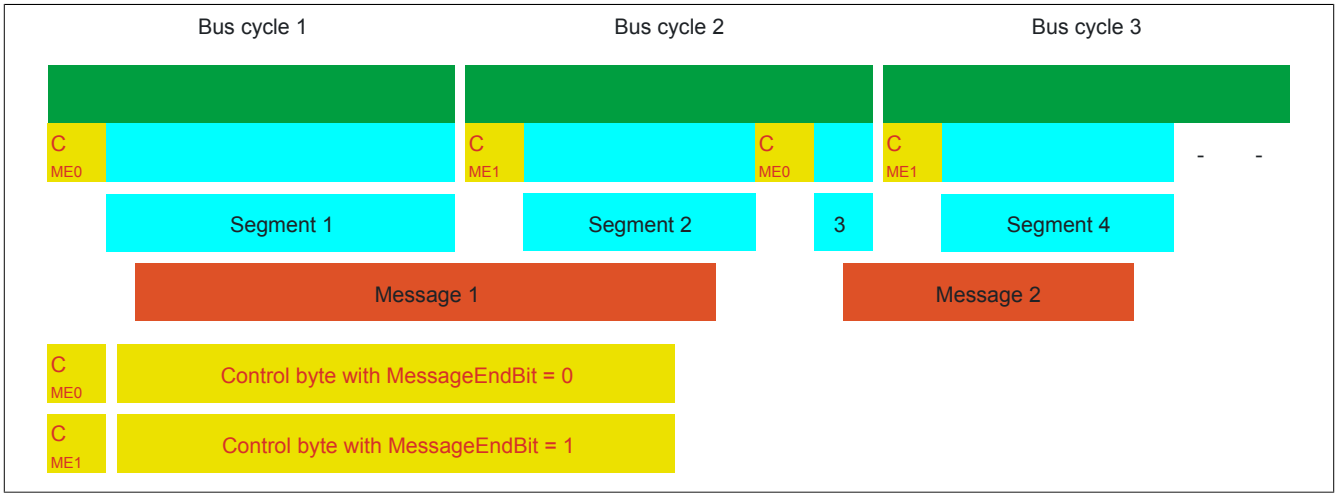


Figure 357: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

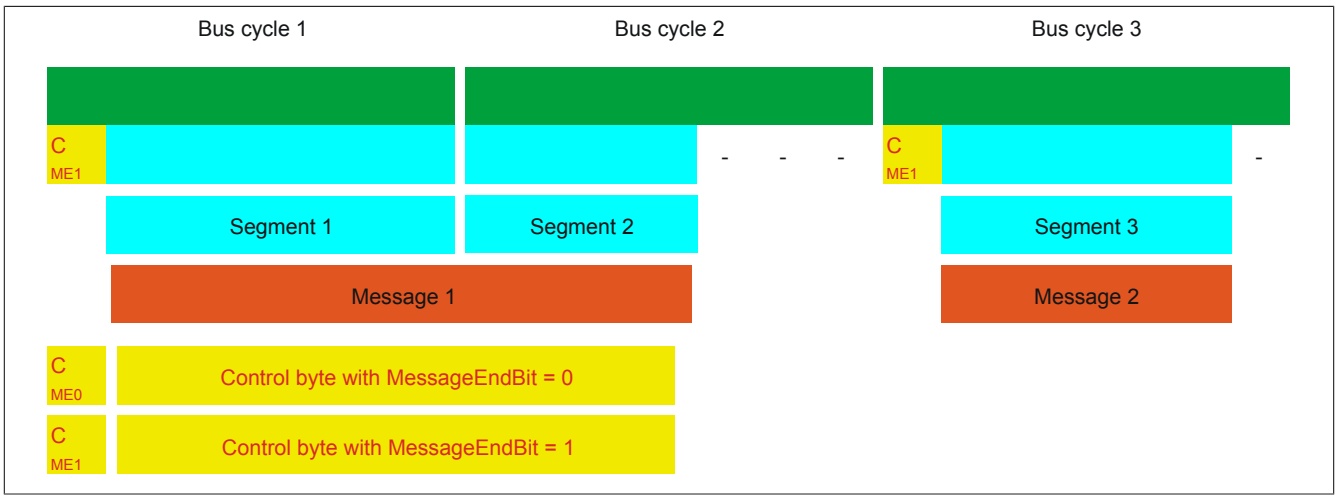


Figure 358: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

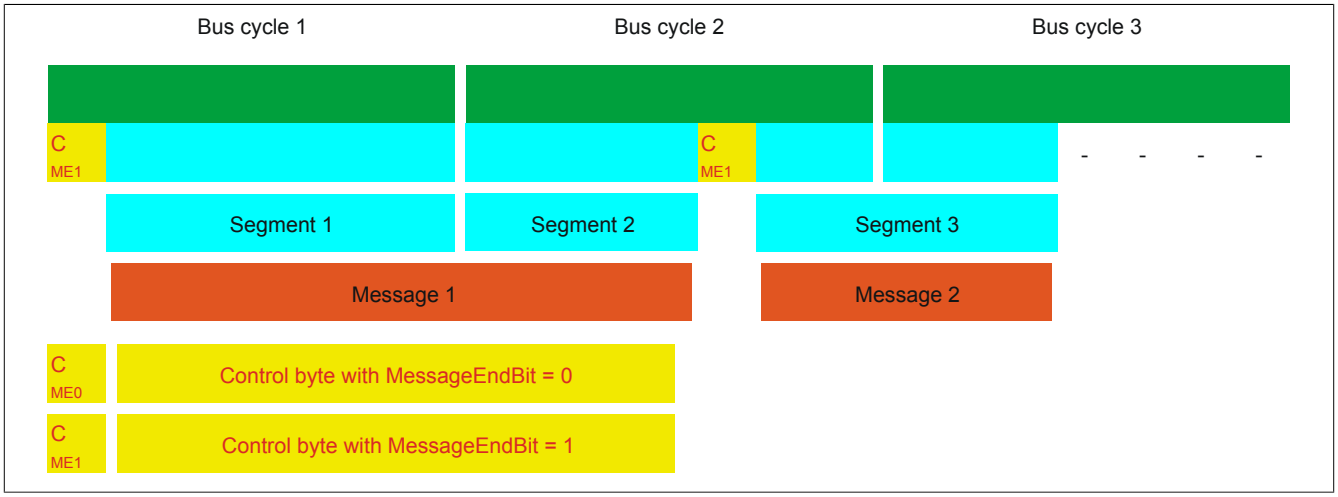


Figure 359: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

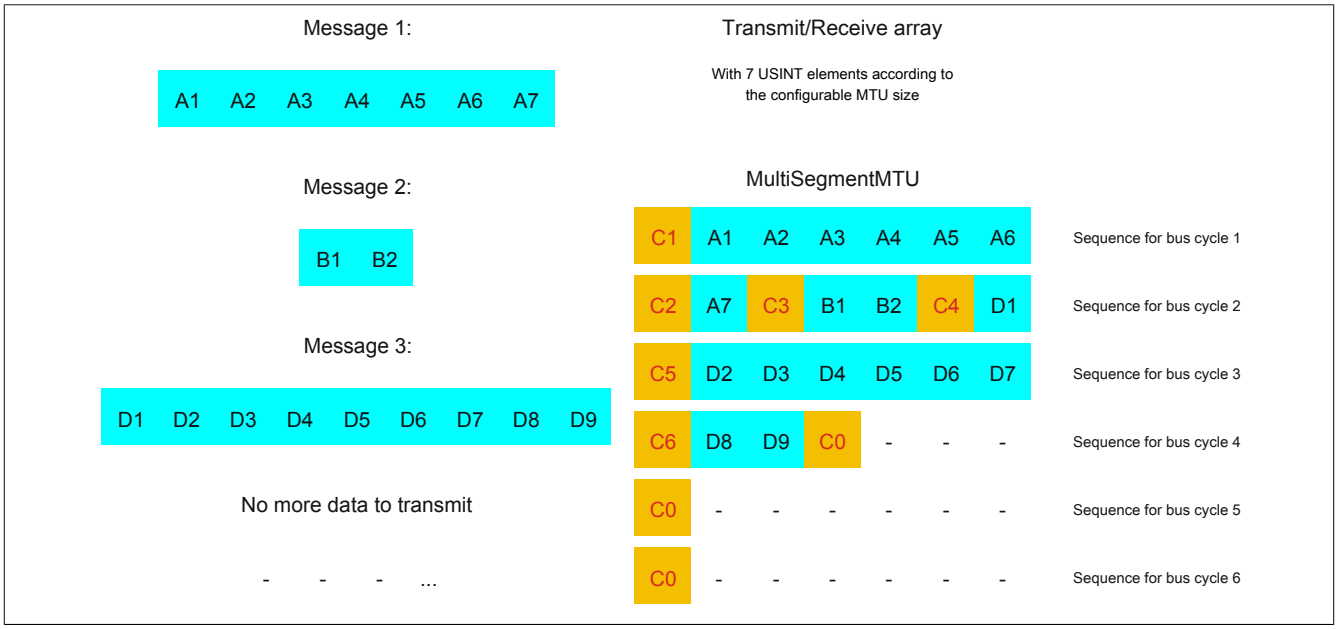


Figure 360: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 425: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 426: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

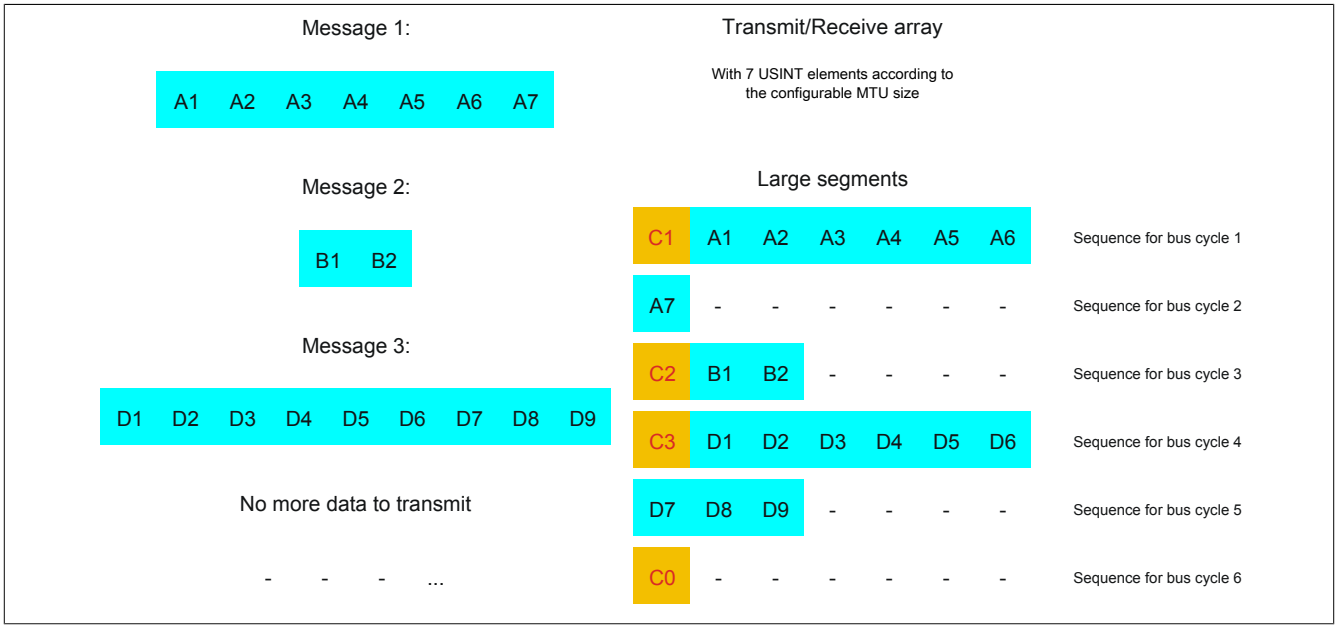


Figure 361: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 427: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

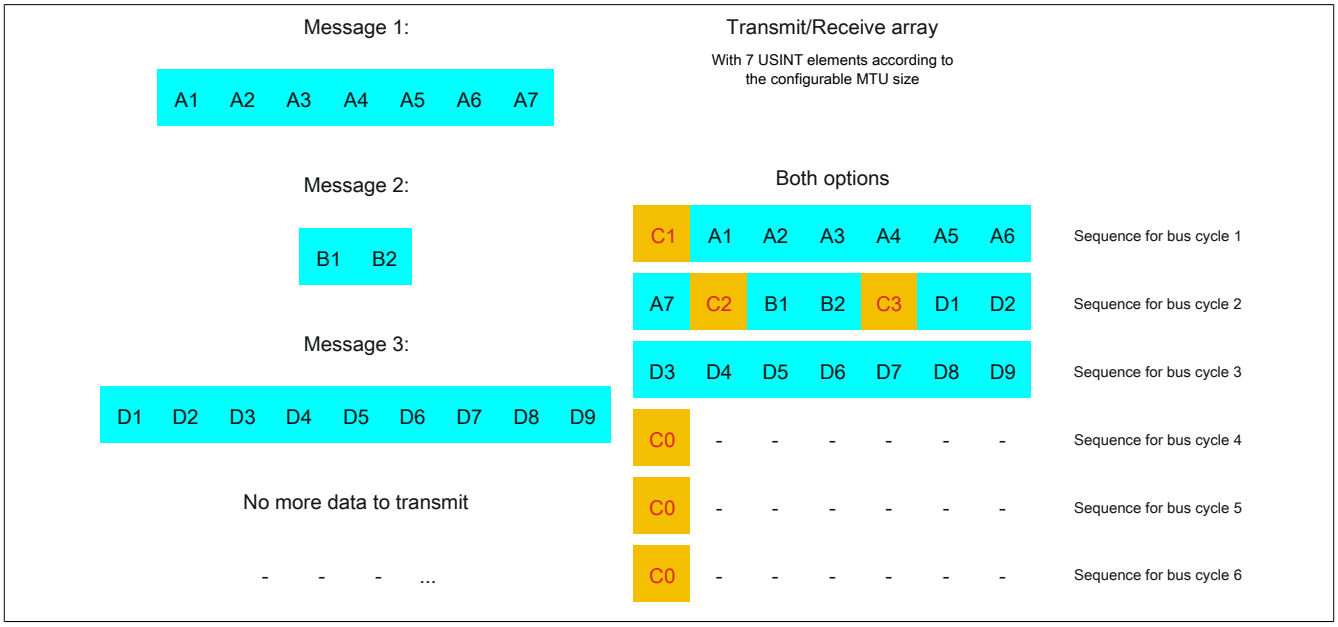


Figure 362: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 428: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.18.8.8.12.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

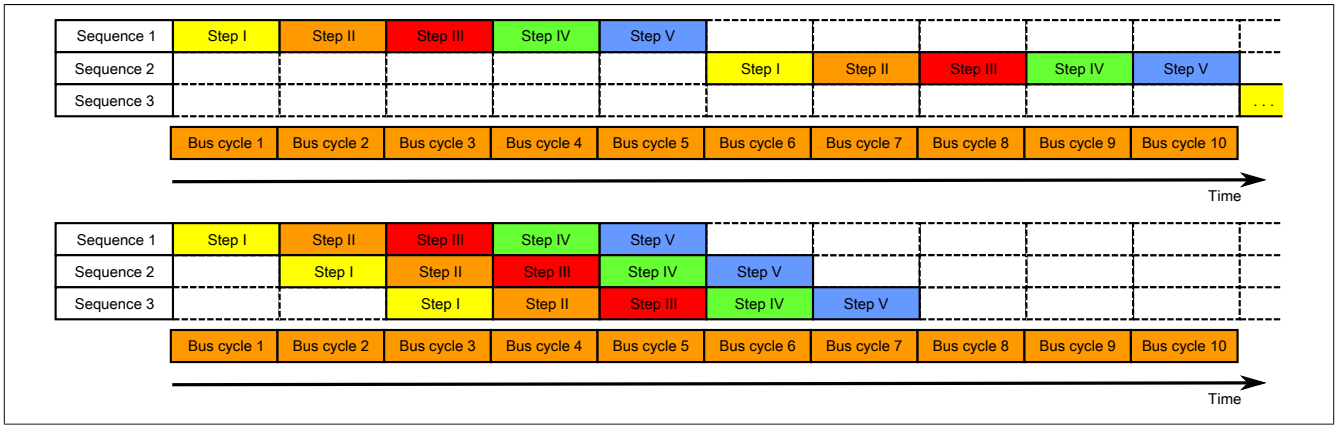


Figure 363: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

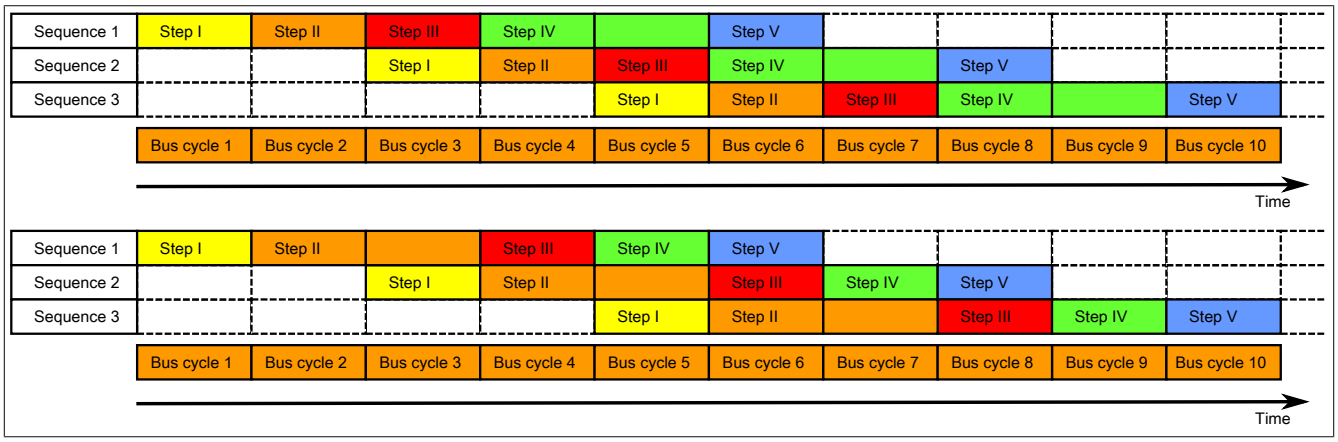


Figure 364: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

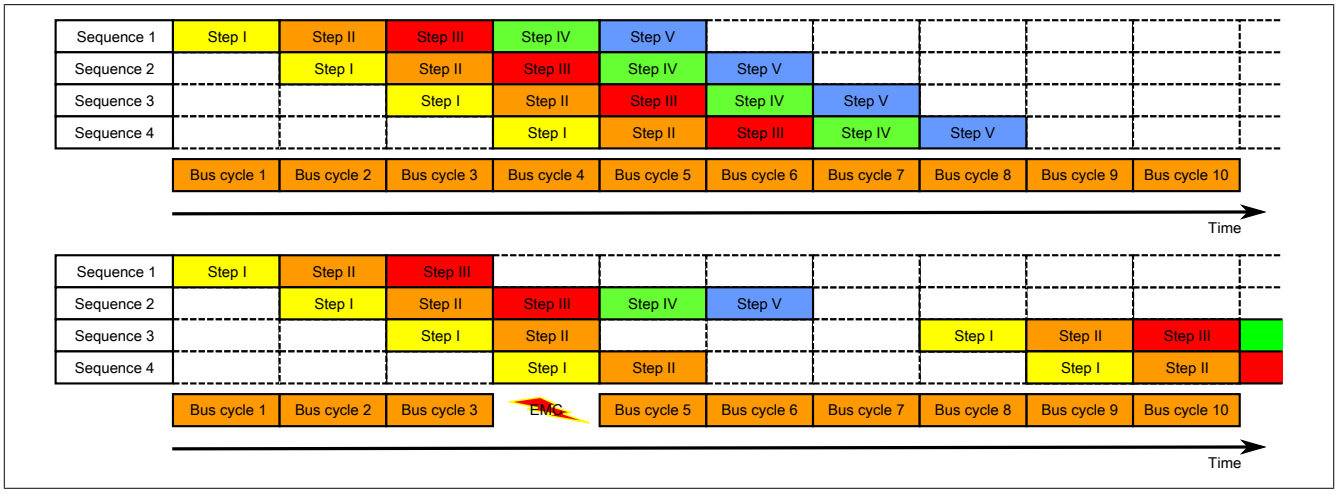


Figure 365: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.18.8.8.13 Acyclic frame size

Name:
AsynSize

When the stream is used, data is exchanged internally between the module and CPU. For this purpose, a defined amount of acyclic bytes is reserved for this slot.
Increasing the acyclic frame size leads to increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Value	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

4.18.8.8.14 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.18.8.8.15 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
200 µs

4.19 Expandable bus controllers

The expandable bus controller is based on the POWERLINK bus controller X20BCx083. The bus modules expanded to the left allow connection of up to two interface or hub expansion modules, depending on the bus controller.

Despite the sleek profile of only 62.5mm and 87.5, the bus controller contains the supply feed for the bus controller, the X2X Link bus supply, and the I/O module feed. No additional power modules are necessary.

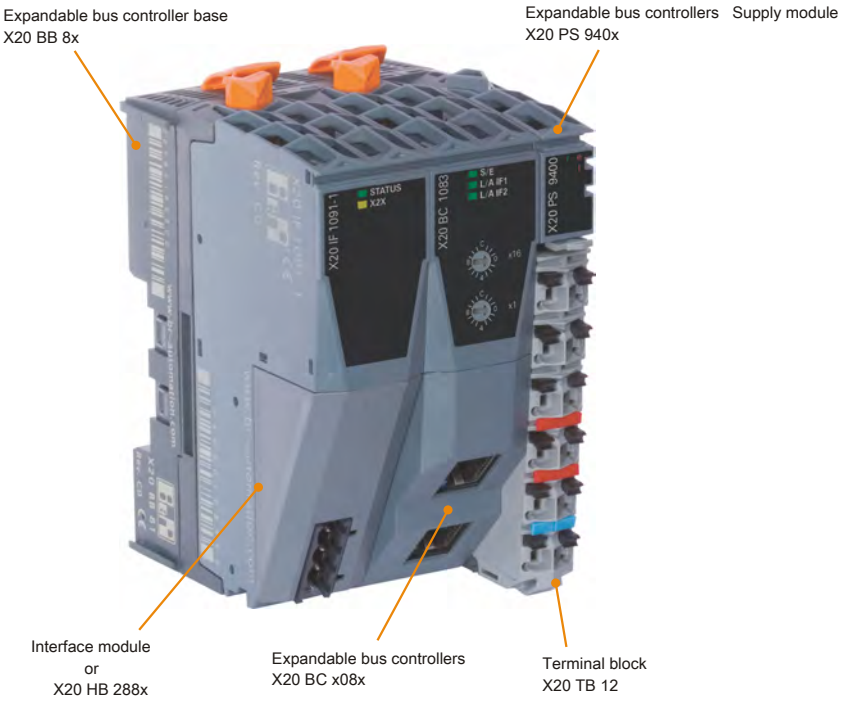


Figure 366: Modular structure of the expandable bus controller

4.19.1 Brief information

Product ID	Short description	on page
X20BC1083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, supports X20 interface module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	2125
X20BC8083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, supports X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	2132
X20BC8084	X20 bus controller, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	2138
X20BC80G3	X20 bus controller, 1 EtherNet/IP interface, supports expansion with X20 EtherCAT junction modules, 2x RJ45, order bus base, power supply module and terminal block separately.	2145
X20cBC1083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, supports X20 interface module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	2125
X20cBC8083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, supports X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	2132
X20cBC8084	X20 bus controller, coated, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	2138

4.19.2 X20(c)BC1083

4.19.2.1 General information

The X20BC1083 bus controller makes it possible to connect X2X Link I/O nodes to POWERLINK V1 and V2. It is also possible to operate the X2X Link cycle synchronously 1:1 or synchronous to POWERLINK using a prescaler.

POWERLINK is a standard protocol for Fast Ethernet with hard real-time properties. The Ethernet POWERLINK Standardization Group (EPSG) ensures that the standard remains open and is continually developed: www.ethernet-powerlink.org

The bus modules expanded to the left allow connection of up to two interface modules in addition to the bus controller.

- POWERLINK
- I/O configuration and FW update via the fieldbus
- Integrated hub for efficient cabling
- Up to two slots for interface modules

4.19.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.19.2.3 Order data

Model number	Short description	Figure
	Expandable bus controllers	
X20BC1083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, supports X20 interface module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
X20cBC1083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, supports X20 interface module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	System modules for expandable bus controllers	
X20IF1091-1	X20 interface module, for expandable bus controller, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately	
	X20 interface module communication	
X20IF1041-1	X20 interface module, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately	
X20IF1043-1	X20 interface module, for DTM configuration, 1 CANopen slave interface, electrically isolated, order 1x TB2105 terminal block separately	
X20IF1051-1	X20 interface module, for DTM configuration, 1 DeviceNet scanner (master) interface, electrically isolated, order 1x TB2105 terminal block separately	
X20IF1053-1	X20 interface module, for DTM configuration, 1 DeviceNet adapter (slave) interface, electrically isolated, order 1x TB2105 terminal block separately	
X20IF1061-1	X20 interface module for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated	
X20IF1063-1	X20 interface module, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated	
X20IF10A1-1	X20 interface module, for DTM configuration, 1 ASi master interface, electrically isolated, order 1x TB704 terminal block separately	
X20IF10D1-1	X20 interface module, for DTM configuration, 1 EtherNet/IP scanner (master) interface, electrically isolated	
X20IF10D3-1	X20 interface module, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated	
X20IF10E1-1	X20 interface module for DTM configuration, 1 PROFINET RT controller (master) interface, electrically isolated	
X20IF10E3-1	X20 interface module, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated	
X20IF10G3-1	X20 interface module for DTM configuration, 1 EtherCAT slave interface, electrically isolated	
X20IF10H3-1	X20 interface module for DTM configuration, 1 Sercos III slave interface, electrically isolated	

Table 429: X20BC1083, X20cBC1083 - Order data

Model number	Short description	Figure
X20cIF1061-1	X20 interface module coated, for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated	
X20cIF1063-1	X20 interface module, coated, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated	
X20cIF10D3-1	X20 interface module, coated, for DTM configuration, 1 Ether-Net/IP adapter (slave) interface, electrically isolated	
X20cIF10E3-1	X20 interface module, coated, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated	

Table 429: X20BC1083, X20cBC1083 - Order data

4.19.2.4 Technical data

Product ID	X20BC1083	X20cBC1083
Short description		
Bus controller	POWERLINK (V1/V2) controlled node with up to 2 slots for interface modules	
General information		
B&R ID code	0x2268	0xE217
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Power consumption		
Bus	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - X2X Link	Yes	
Fieldbus - I/O	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Fieldbus	POWERLINK (V1/V2) controlled node	
Design	2x shielded RJ45 (hub)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Min. cycle time [2]		
Fieldbus	200 µs	
X2X Link	200 µs	
Synchronization between bus systems possible	Yes	
Cyclic data		
Input data	Max. 1488 bytes	
Output data	Max. 1488 bytes	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	0 to 55°C	
Vertical installation	0 to 50°C	
Derating	-	
Storage	-25 to 70°C	
Transport	-25 to 70°C	

Table 430: X20BC1083, X20cBC1083 - Technical data

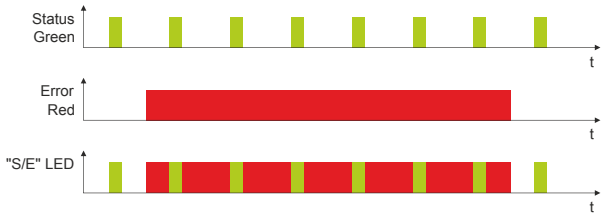
Product ID	X20BC1083	X20cBC1083
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB81 or X20B-B82 bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS9400 power supply module separately Order 1x X20cBB81 or X20cB-B82 bus base separately
Spacing [3]		
X20BB81	62.5$^{+0.2}$ mm	
X20BB82	87.5$^{+0.2}$ mm	

Table 430: X20BC1083, X20cBC1083 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB81 or X20BB82 bus base. Up to two interfaces modules and one X20PS9400 or X20PS9402 supply module are also always required for the bus controller.

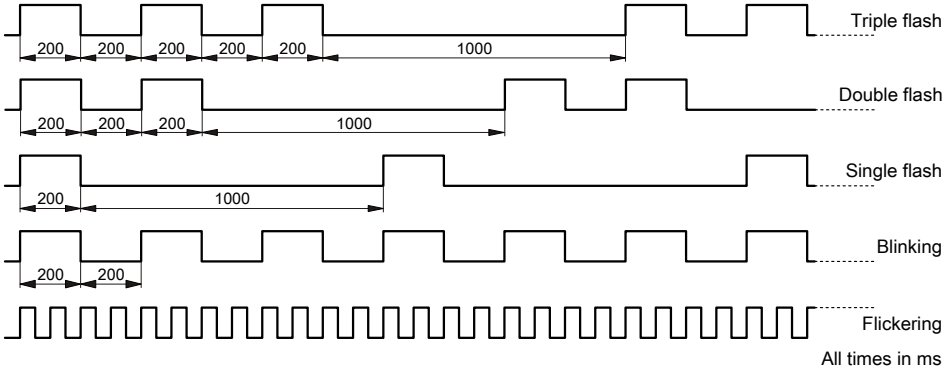
4.19.2.5 LED status indicators

Figure	LED	Color	Status	Description
	S/E[1]	Green	Off	No power supply or mode is NOT_ACTIVE. The controlled node (CN) is either not getting power, or it is in the NOT_ACTIVE state. The CN waits in this state for about 5 seconds after a restart. Communication is not possible with the module. If no POWERLINK communication is detected during these 5 seconds, the CN goes into the BASIC_ETHERNET state (flickering). If POWERLINK communication is detected before this time passes, however, the CN goes directly into the PRE_OPERATIONAL_1 state.
			Flickering	BASIC_ETHERNET mode. The CN has not detected any POWERLINK communication. It is possible to communicate directly with the CN in this state (e.g. with UDP, IP, etc.). If POWERLINK communication is detected while in this state, the CN goes into the PRE_OPERATIONAL_1 state.
			Single flash	PRE_OPERATIONAL_1 mode. When operated on a POWERLINK V1 manager, the CN goes directly into the PRE_OPERATIONAL_2 state. When operated on a POWERLINK V2 manager, the CN waits until an SoC frame is received and then goes into the PRE_OPERATIONAL_2 state.
			Double flash	PRE_OPERATIONAL_2 mode. The CN is normally configured by the manager in this state. Issuing a command (POWERLINK V2) or setting the data valid flag in the output data (POWERLINK V1) then switches to the READY_TO_OPERATE state.
			Triple flash	READY_TO_OPERATE mode. In a POWERLINK V1 network, the CN automatically switches to the OPERATIONAL state as soon as input data is present. In a POWERLINK V2 network, the manager switches to the OPERATIONAL state by issuing a command.
			On	OPERATIONAL mode. PDO mapping is active and cyclic data is being evaluated.

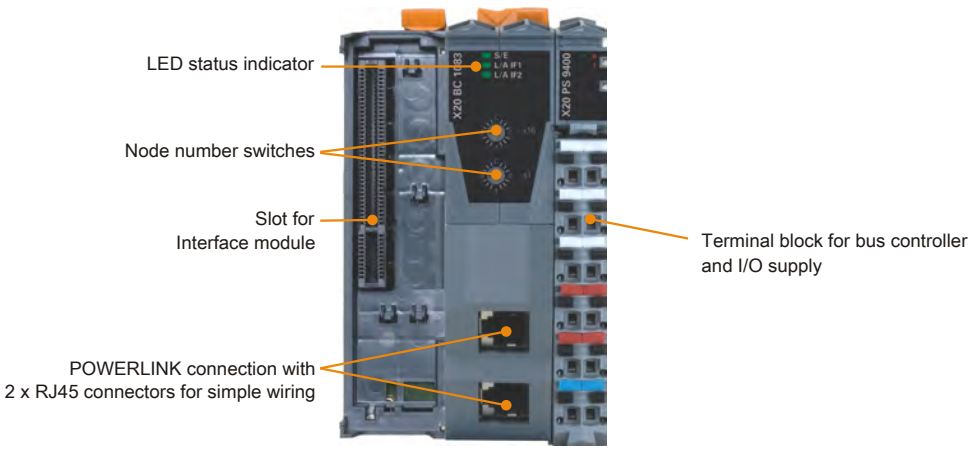
Figure	LED	Color	Status	Description
			Blinking	STOPPED mode. No output data is produced or input data supplied. It is only possible to enter or leave this state after the manager has given the appropriate command.
		Red	On	The controlled node (CN) is in an error state (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: • The LED blinks red several times immediately after startup. This is not an error. • The LED is lit red for CNs with configured physical node number 0 but that have not yet been assigned a node number via Dynamic Node Allocation (DNA).
	L/A IFx	Green	On	Link established to the remote station
			Blinking	A link to the remote station has been established and there is activity on bus.

1) The Status/Error LED "S/E" is a green/red dual LED.

Status LEDs - Blinking patterns



4.19.2.6 Operating and connection elements



4.19.2.7 POWERLINK node number

The node number for the POWERLINK node is set using the two number switches. Node numbers between 0x01 and 0xEF are permitted.

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node Operation as a controlled node.
0xF0 - 0xFF	Reserved, switch position not permitted

4.19.2.8 Dynamic Node Allocation (DNA)

The node numbers of all POWERLINK bus controllers can be assigned dynamically. This has the following advantages:

- No need to set the node number switch
- Easier installation
- Reduced error sources

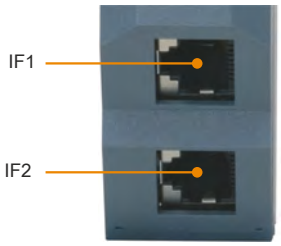
For information about configuration as well as an example, see the AS help system (Communication → POWERLINK → General information → Dynamic Node Allocation (DNA)).

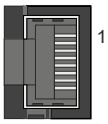
Information:

The IF1 interface must always be used as the input from the preceding node.

4.19.2.9 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.19.2.10 Slot for interface modules

Depending on the bus base, up to two interface modules can be installed on the left side of the expandable bus controller:

Bus base	Slots for interface modules
X20BB81	1
X20BB82	2

Table 431: Slots for interface modules for various bus bases

4.19.2.11 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.19.2.12 SG3

This module is not supported on SG3 targets.

4.19.2.13 SG4

This module comes with preinstalled firmware. The firmware is also part of the Automation Runtime operating system for the PLC. If the two versions are different, the Automation Runtime firmware is loaded to the module.

The latest firmware is made available automatically when updating Automation Runtime.

4.19.3 X20(c)BC8083

4.19.3.1 General information

The X20BC8083 bus controller makes it possible to connect X2X Link I/O nodes to POWERLINK. It is also possible to operate the X2X Link cycle synchronously 1:1 or synchronous to POWERLINK using a prescaler.

POWERLINK is a standard protocol for Fast Ethernet with hard real-time properties. The Ethernet POWERLINK Standardization Group (EPSG) ensures that the standard remains open and is continually developed: www.ethernet-powerlink.org

The bus modules expanded to the left allow connection of up to two hub expansion modules in addition to the bus controller. Each expansion module is equipped with two RJ45 connections. This means that a basic device provides up to six hub ports.

- POWERLINK
- I/O configuration and FW update via the fieldbus
- Integrated hub for efficient cabling
- Up to two slots for hub expansion modules
- 2x/4x/6x Fast Ethernet hub

4.19.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.19.3.3 Order data

Model number	Short description	Figure
	Expandable bus controllers	
X20BC8083	X20 bus controller, 1 POWERLINK interface, integrated 2-port hub, supports X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
X20cBC8083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, supports X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	System modules for the X20 hub system	
X20HB1881	X20 hub expansion module, integrated 1-port hub, for fiber optic cable	
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45	
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable	
X20cHB1881	X20 hub expansion module, coated, integrated 1-port hub, for fiber optic cable	
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45	
X20cHB2881	X20 hub expansion module, coated, integrated 2-port hub, for fiber optic cable	

Table 432: X20BC8083, X20cBC8083 - Order data

4.19.3.4 Technical data

Product ID	X20BC8083	X20cBC8083
Short description		
Bus controller	POWERLINK (V1/V2) controlled node with up to 2 slots for hub expansion modules	
General information		
B&R ID code	0x2673	0xE218
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Power consumption		
Bus	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - X2X Link	Yes	
Fieldbus - I/O	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Fieldbus	POWERLINK (V1/V2) controlled node	
Design	2x shielded RJ45 (hub)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Min. cycle time [2)]		
Fieldbus	200 µs	
X2X Link	200 µs	
Synchronization between bus systems possible	Yes	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB8x bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS9400 power supply module separately Order 1x X20cBB8x bus base separately

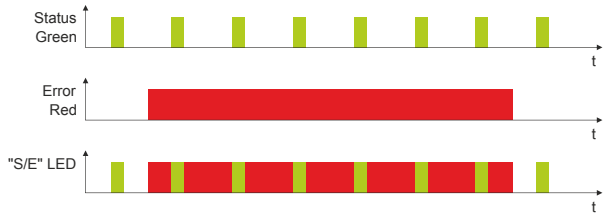
Table 433: X20BC8083, X20cBC8083 - Technical data

Product ID	X20BC8083	X20cBC8083
Spacing [3]		
X20BB80	37.5 +0.2 mm	
X20BB81	62.5+0.2 mm	
X20BB82	87.5+0.2 mm	

Table 433: X20BC8083, X20cBC8083 - Technical data

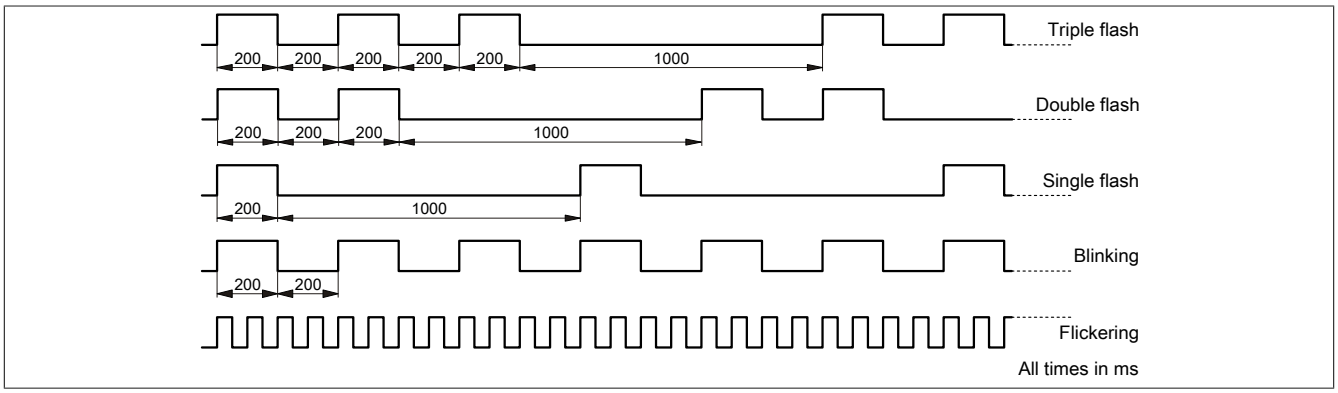
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB80 bus base. Up to two X20HB2880 hub expansion modules and one X20PS9400 or X20PS9402 supply module are also always required for the bus controller.

4.19.3.5 LED status indicators

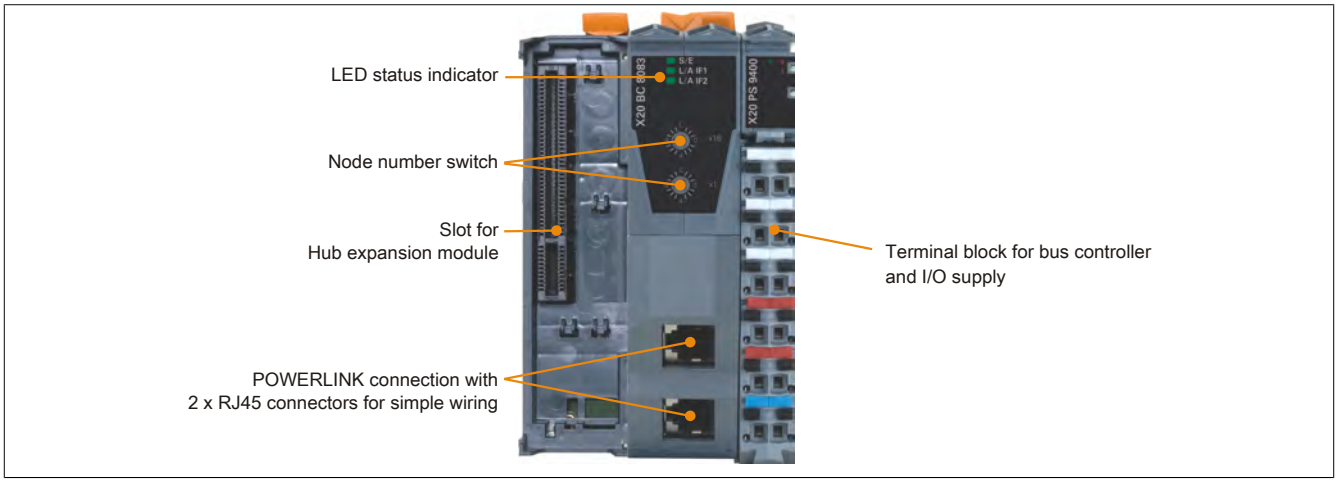
Figure	LED	Color	Status	Description
	S/E[1]	Green	Off	No power supply or mode is NOT_ACTIVE. The controlled node (CN) is either not getting power, or it is in the NOT_ACTIVE state. The CN waits in this state for about 5 seconds after a restart. Communication is not possible with the module. If no POWERLINK communication is detected during these 5 seconds, the CN goes into the BASIC_ETHERNET state (flickering). If POWERLINK communication is detected before this time passes, however, the CN goes directly into the PRE_OPERATIONAL_1 state.
			Flickering	BASIC_ETHERNET mode. The CN has not detected any POWERLINK communication. It is possible to communicate directly with the CN in this state (e.g. with UDP, IP, etc.). If POWERLINK communication is detected while in this state, the CN goes into the PRE_OPERATIONAL_1 state.
			Single flash	PRE_OPERATIONAL_1 mode. When operated on a POWERLINK V1 manager, the CN goes directly into the PRE_OPERATIONAL_2 state. When operated on a POWERLINK V2 manager, the CN waits until an SoC frame is received and then goes into the PRE_OPERATIONAL_2 state.
			Double flash	PRE_OPERATIONAL_2 mode. The CN is normally configured by the manager in this state. Issuing a command (POWERLINK V2) or setting the data valid flag in the output data (POWERLINK V1) then switches to the READY_TO_OPERATE state.
			Triple flash	READY_TO_OPERATE mode. In a POWERLINK V1 network, the CN automatically switches to the OPERATIONAL state as soon as input data is present. In a POWERLINK V2 network, the manager switches to the OPERATIONAL state by issuing a command.
			On	OPERATIONAL mode. PDO mapping is active and cyclic data is being evaluated.
			Blinking	STOPPED mode. No output data is produced or input data supplied. It is only possible to enter or leave this state after the manager has given the appropriate command.
		Red	On	The controlled node (CN) is in an error state (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: • The LED blinks red several times immediately after startup. This is not an error. • The LED is lit red for CNs with configured physical node number 0 but that have not yet been assigned a node number via Dynamic Node Allocation (DNA).
	L/A IFx	Green	On	Link established to the remote station
			Blinking	A link to the remote station has been established and there is activity on bus.

1) The Status/Error LED "S/E" is a green/red dual LED.

Status LEDs - Blinking patterns



4.19.3.6 Operating and connection elements



4.19.3.7 POWERLINK node number

The node number for the POWERLINK node is set using the two number switches. Node numbers between 0x01 and 0xEF are permitted.

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node Operation as a controlled node.
0xF0 - 0xFF	Reserved, switch position not permitted

4.19.3.8 Dynamic Node Allocation (DNA)

The node numbers of all POWERLINK bus controllers can be assigned dynamically. This has the following advantages:

- No need to set the node number switch
- Easier installation
- Reduced error sources

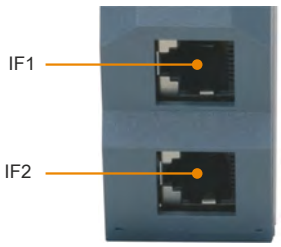
For information about configuration as well as an example, see the AS help system (Communication → POWERLINK → General information → Dynamic Node Allocation (DNA)).

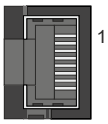
Information:

The IF1 interface must always be used as the input from the preceding node.

4.19.3.9 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



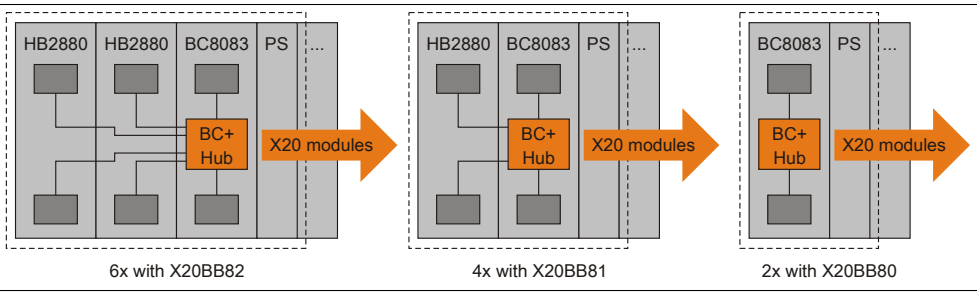
Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.19.3.10 Slot for hub expansion modules

Depending on the bus base, up to 2 hub expansion modules can be installed on the left side of the bus controller:

Bus base	Slot for hub expansion modules
X20BB81	1
X20BB82	2

The X20HB2880 hub expansion module for the bus controller is equipped with 2 RJ45 connections, which means that up to 6 hub ports are available.



4.19.3.11 SG3

This module is not supported on SG3 targets.

4.19.3.12 SG4

This module comes with preinstalled firmware. The firmware is also part of the Automation Runtime operating system for the PLC. If the two versions are different, the Automation Runtime firmware is loaded to the module.

The latest firmware is made available automatically when updating Automation Runtime.

4.19.4 X20(c)BC8084

4.19.4.1 General information

The X20BC8084 bus controller makes it possible to connect X2X Link I/O nodes to POWERLINK. It is also possible to operate the X2X Link cycle synchronously 1:1 or synchronous to POWERLINK using a prescaler.

POWERLINK is a standard protocol for Fast Ethernet with hard real-time properties. The Ethernet POWERLINK Standardization Group (EPSG) ensures that the standard remains open and is continually developed: www.ethernet-powerlink.org

Systems with redundant cabling can be implemented easily using POWERLINK. Unlike ring redundancy, cable redundancy does not require cable looping, which can sometimes be problematic. This allows the creation of all types of tree structures. When using a device with the link selector function, data is always transferred via the highest quality network lines. The link selector function is integrated in the bus controller X20BC8084.

- POWERLINK
- I/O configuration and FW update via the fieldbus
- Integrated compact link selector function
- Two active hub expansion modules can be connected to the bus controller
- Redundant supply possible

4.19.4.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.19.4.3 Order data

Model number	Short description	Figure
	Expandable bus controllers	
X20BC8084	X20 bus controller, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
X20cBC8084	X20 bus controller, coated, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply	
	System modules for expandable bus controllers	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	System modules for X20 redundancy systems	
X20HB2885	X20 hub expansion module, integrated active 2-port hub, 2x RJ45	
X20HB2886	X20 hub expansion module, integrated active 2-port hub, 2 fiber optic interfaces	
	System modules for the X20 redundancy system	
X20cHB2885	X20 hub expansion module, coated, integrated active 2-port hub, 2x RJ45	

Table 434: X20BC8084, X20cBC8084 - Order data

4.19.4.4 Technical data

Product ID	X20BC8084	X20cBC8084
Short description		
Bus controller	POWERLINK (V1/V2) controlled node with compact link selector	
General information		
B&R ID code	0x2674	0xDF10
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Power consumption		
Bus	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - X2X Link	Yes	
Fieldbus - I/O	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Fieldbus	POWERLINK (V1/V2) controlled node	
Design	2x shielded RJ45	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Min. cycle time [2)]		
Fieldbus	200 µs	
X2X Link	200 µs	
Synchronization between bus systems possible	Yes	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	

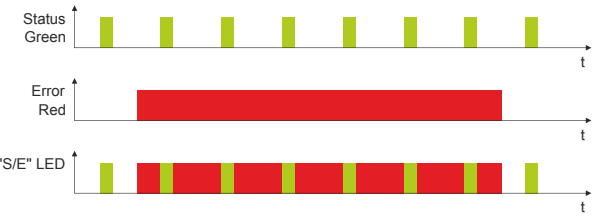
Table 435: X20BC8084, X20cBC8084 - Technical data

Product ID	X20BC8084	X20cBC8084
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 or X20PS9402 power supply module separately Order 1x X20BB80 or X20BB82 bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS9400 power supply module separately Order 1x X20cBB80 or X20cBB82 bus base separately
Spacing 3) X20BB80 X20BB82	 37.5 +0.2 mm 87.5+0.2 mm	

Table 435: X20BC8084, X20cBC8084 - Technical data

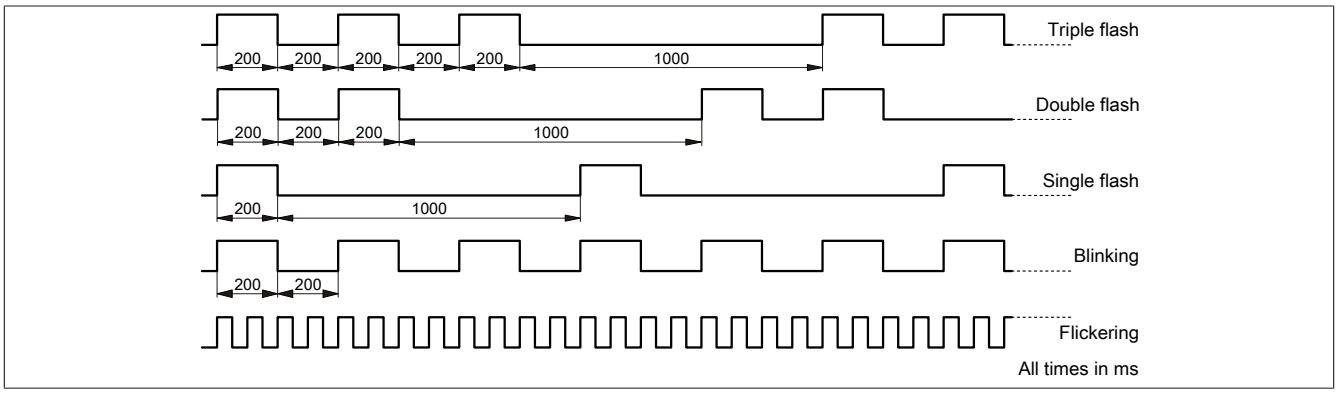
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
3) Spacing is based on the width of the X20BB81 or X20BB82 bus base. In addition, an X20PS9400 or X20PS9402 supply module is always required for the bus controller. To save cabling for external hubs, the X20BC8084 can be expanded with two active hub modules, the X20HB2885 or the X20HB2886.

4.19.4.5 LED status indicators

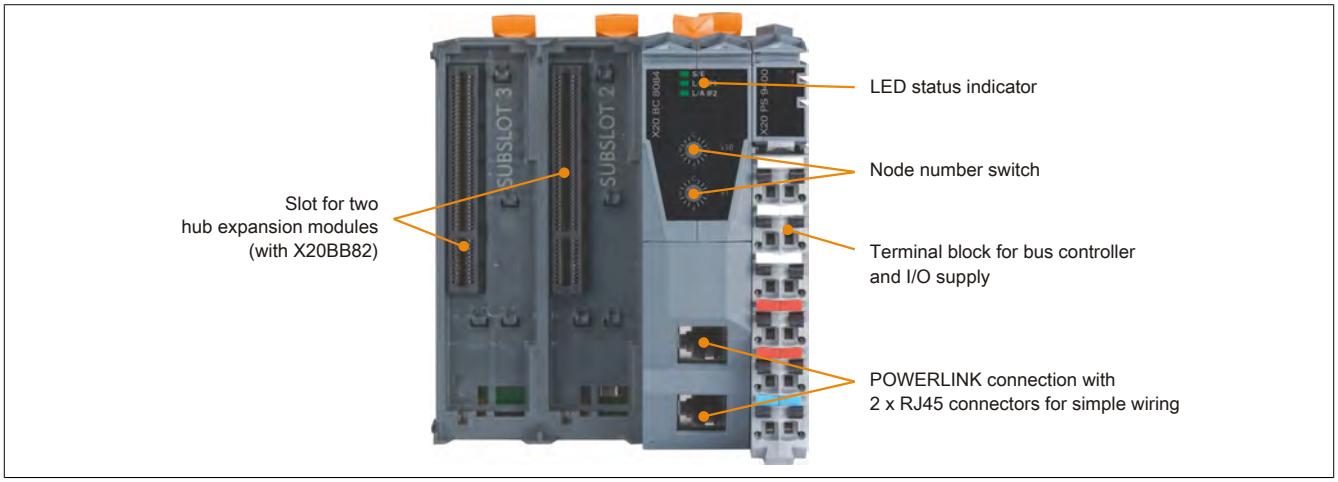
Figure	LED	Color	Status	Description
	S/E1)	Green	Off	No power supply or mode is NOT_ACTIVE. The controlled node (CN) is either not getting power, or it is in the NOT_ACTIVE state. The CN waits in this state for about 5 seconds after a restart. Communication is not possible with the module. If no POWERLINK communication is detected during these 5 seconds, the CN goes into the BASIC_ETHERNET state (flickering). If POWERLINK communication is detected before this time passes, however, the CN goes directly into the PRE_OPERATIONAL_1 state.
			Flickering	BASIC_ETHERNET mode. The CN has not detected any POWERLINK communication. It is possible to communicate directly with the CN in this state (e.g. with UDP, IP, etc.). If POWERLINK communication is detected while in this state, the CN goes into the PRE_OPERATIONAL_1 state.
			Single flash	PRE_OPERATIONAL_1 mode. When operated on a POWERLINK V1 manager, the CN goes directly into the PRE_OPERATIONAL_2 state. When operated on a POWERLINK V2 manager, the CN waits until an SoC frame is received and then goes into the PRE_OPERATIONAL_2 state.
			Double flash	PRE_OPERATIONAL_2 mode. The CN is normally configured by the manager in this state. Issuing a command (POWERLINK V2) or setting the data valid flag in the output data (POWERLINK V1) then switches to the READY_TO_OPERATE state.
			Triple flash	READY_TO_OPERATE mode. In a POWERLINK V1 network, the CN automatically switches to the OPERATIONAL state as soon as input data is present. In a POWERLINK V2 network, the manager switches to the OPERATIONAL state by issuing a command.
			On	OPERATIONAL mode. PDO mapping is active and cyclic data is being evaluated.
			Blinking	STOPPED mode. No output data is produced or input data supplied. It is only possible to enter or leave this state after the manager has given the appropriate command.
		Red	On	The controlled node (CN) is in an error state (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: • The LED blinks red several times immediately after startup. This is not an error. • The LED is lit red for CNs with configured physical node number 0 but that have not yet been assigned a node number via Dynamic Node Allocation (DNA).
	L/A IFx	Green	On	Link established to the remote station
			Blinking	A link to the remote station has been established and there is activity on bus.

1) The Status/Error LED "S/E" is a green/red dual LED.

Status LEDs - Blinking patterns



4.19.4.6 Operating and connection elements



4.19.4.7 POWERLINK node number

The node number for the POWERLINK node is set using the two number switches. Node numbers between 0x01 and 0xEF are permitted.

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node Operation as a controlled node.
0xF0 - 0xFF	Reserved, switch position not permitted

4.19.4.8 Dynamic Node Allocation (DNA)

The node numbers of all POWERLINK bus controllers can be assigned dynamically. This has the following advantages:

- No need to set the node number switch
- Easier installation
- Reduced error sources

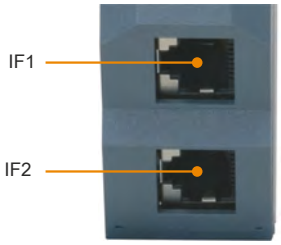
For information about configuration as well as an example, see the AS help system (Communication → POWERLINK → General information → Dynamic Node Allocation (DNA)).

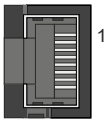
Information:

The IF1 interface must always be used as the input from the preceding node.

4.19.4.9 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
Shielded RJ45	8	Termination	

4.19.4.10 SG3

This module is not supported on SG3 targets.

4.19.4.11 SG4

This module comes with preinstalled firmware. The firmware is also part of the Automation Runtime operating system for the PLC. If the two versions are different, the Automation Runtime firmware is loaded to the module.

The latest firmware is made available automatically when updating Automation Runtime.

4.19.4.12 POWERLINK cable redundancy system

It is often indispensable to have redundant network cabling, especially in systems that handle technical processes. The potential for danger, especially to the lines that run through the system, is disproportionately high in relation to the need to keep communication active in all operating situations. This risk is effectively reduced with double cabling that is routed separately.

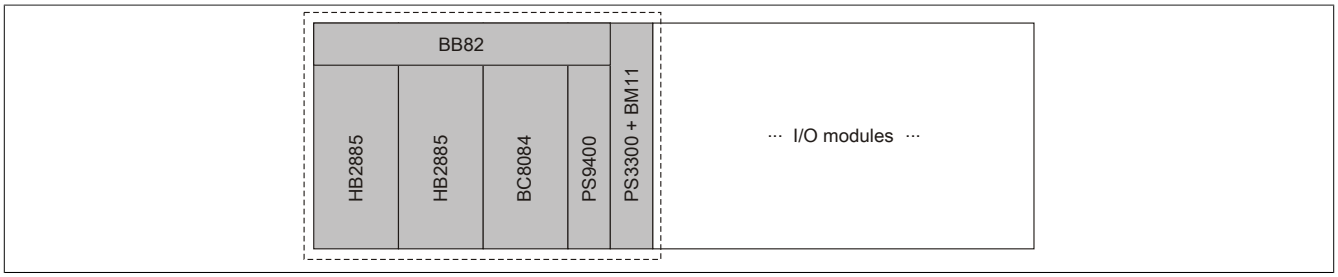
The POWERLINK cable redundancy system is based on the principle of doubling the transfer routing as well as providing continual and simultaneous monitoring. That means data is simultaneously fed into two cable lines using a corresponding mechanism. The same mechanisms are used to receive these telegrams from the redundant network.

Details about the structure of a redundancy system can be found in the "Redundancy for control systems" user's manual. The user's manual is available in the Downloads section of the B&R website www.br-automation.com.

4.19.4.13 Redundant supply voltage

When operating the bus controller with two X20HB2885 hub modules, a redundant supply voltage for the system can be easily implemented using two X20 supply modules.

Hardware configuration for redundant supply voltage



Connection example for supply modules

X20PS9400

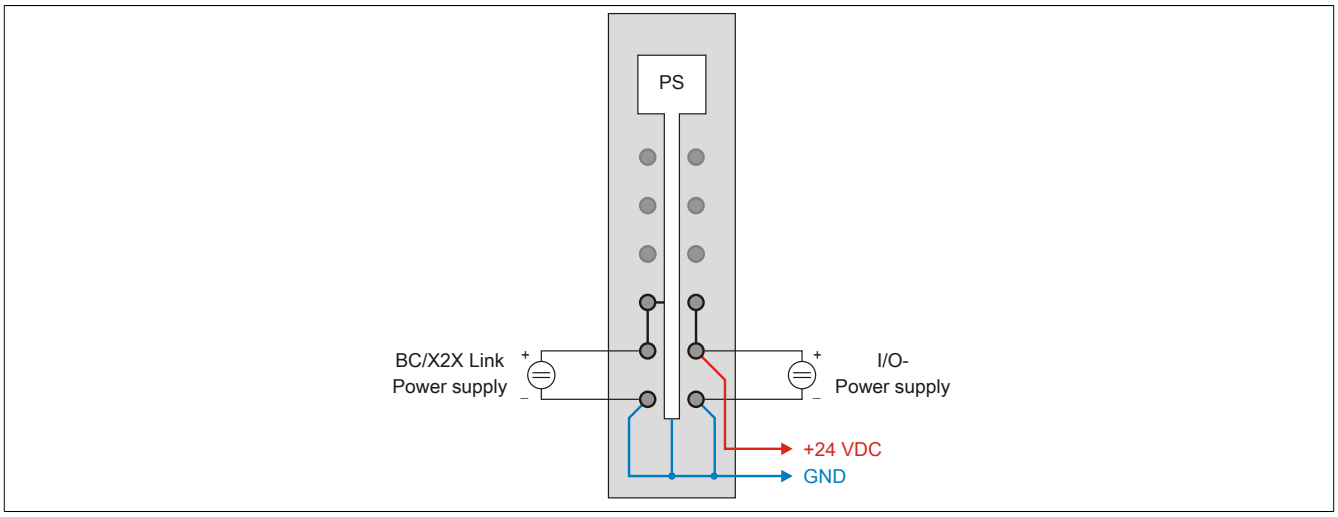


Figure 367: The X20PS9400 is connected as usual

X20PS3300

The supply module X20PS3300 is operated with a X20BM11 bus module. Only the BC/X2X Link supply is connected. A redundant I/O supply is not possible. By using the X20BM11 bus module, the I/O supply of the X20PS9400 supply module is connected to the I/O modules.

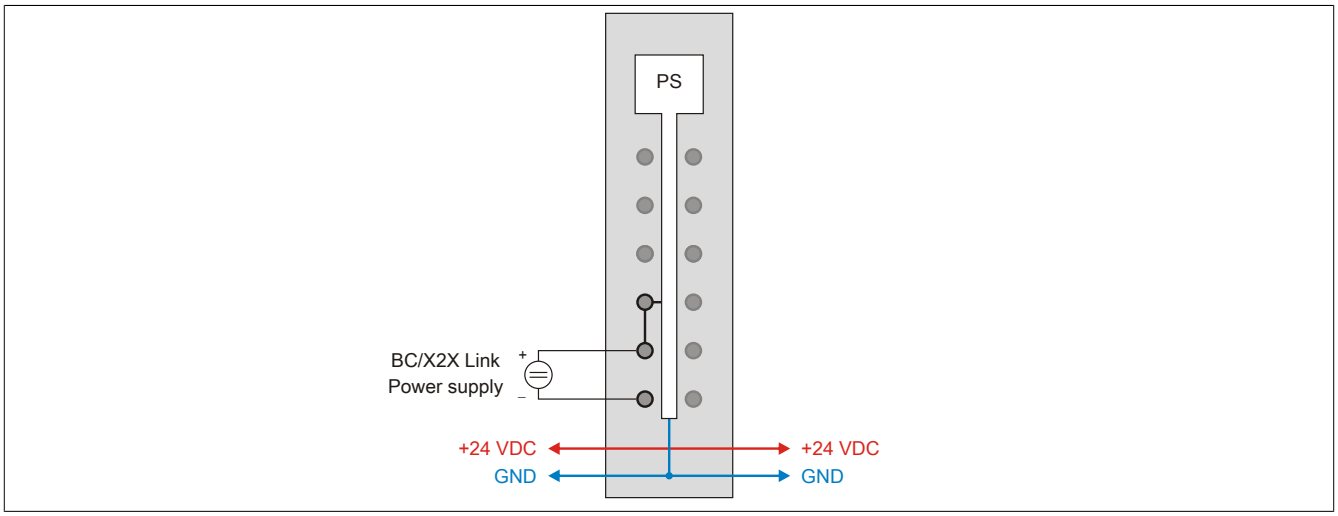


Figure 368: Only the BC/X2X Link supply is connected for the X20PS3300

4.19.5 X20BC80G3

4.19.5.1 General information

EtherCAT is an Ethernet-based fieldbus developed by Beckhoff. The protocol is suitable for hard and soft real-time requirements in automation technology. In addition to a ring structure, which becomes logically necessary because of the summation frame telegram used, the EtherCAT technology also physically supports topologies such as line, tree, star (limited) and combinations of these topologies. B&R's X20BC80G3 (expandable bus controller module) and X20HB88G0 (stand alone junction base module) are available for implementing these topologies.

EtherCAT slave devices take the data designated for them from a telegram as it is passing through the device. Input data is also inserted in the telegram as it is passing through. The X20BC80G3 bus controller allows X2X Link I/O modules to be coupled to EtherCAT and can be operated on any EtherCAT master system. A transition between IP20 and IP67 protection outside of the control cabinet is possible by aligning X20, X67 or XV modules one after the other as needed at distances up to 100 m.

Master systems without FoE (File Access over EtherCAT) support require an appropriate configuration tool to transfer the configuration (optional).

By expanding the bus module to the left, the X20BC80G3 bus controller has an additional slot available for an X20HB28G0 EtherCAT junction module. The junction module is equipped with two RJ45 connections. This means that a basic device provides four hub ports.

- Fieldbus: EtherCAT
- Auto-configuration of I/O modules
- I/O configuration and firmware update via the fieldbus (FoE)
- Full support of the modular slice concept via CoE (CANopen over EtherCAT)
- Configurable I/O cycle (0.2 to 4 ms)
- Synchronization between the fieldbus and X2X Link
- One slot for X20HB28G0 EtherCAT junction module

Information:

Only the default function model is supported (see respective module description) when the bus controller automatically configures multi-function modules.

All other function models are supported when configured accordingly (see EtherCAT user's manual). The easy-to-use B&R FieldbusDESIGNER can help in this regard and is available for free download from www.br-automation.com/designer.

4.19.5.2 Order data

Model number	Short description	Figure
	Expandable bus controllers	
X20BC80G3	X20 bus controller, 1 EtherNet/IP interface, supports expansion with X20 EtherCAT junction modules, 2x RJ45, order bus base, power supply module and terminal block separately.	
	Required accessories	
	System modules for bus controllers	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
X20PS9402	X20 supply module, for bus controller and internal I/O supply, X2X Link supply, supply not electrically isolated	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for the X20 hub system	
X20HB28G0	X20 EtherCAT junction module, integrated 2-port EtherCAT junction, 2x RJ45	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 436: X20BC80G3 - Order data

4.19.5.3 Technical data

Product ID	X20BC80G3
Short description	
Bus controller	EtherCAT bus controller with one slot for 1 junction module
General information	
B&R ID code	0xAEC2
Status indicators	Module status, bus function
Diagnostics	
Module status	Yes, with status LED and software status
Bus function	Yes, with status LED and software status
Power consumption	
Bus	1.79 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Fieldbus - X2X Link	Yes
Fieldbus - I/O	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1]	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Fieldbus	EtherCAT slave
Design	2x shielded RJ45
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100 BASE-TX
Half-duplex	Yes
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Hub runtime	750 ns [2]
Min. cycle time [3]	
Fieldbus	200 µs
X2X Link	200 µs
Synchronization between bus systems possible	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0,5°C per 100 m
EN 60529 protection	IP20

Table 437: X20BC80G3 - Technical data

Product ID	X20BC80G3
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order supply module 1x X20PS9400 or X20PS9402 separately Order 1x X20BB81 bus base separately
Spacing 4)	62.5 +0.2 mm

Table 437: X20BC80G3 - Technical data

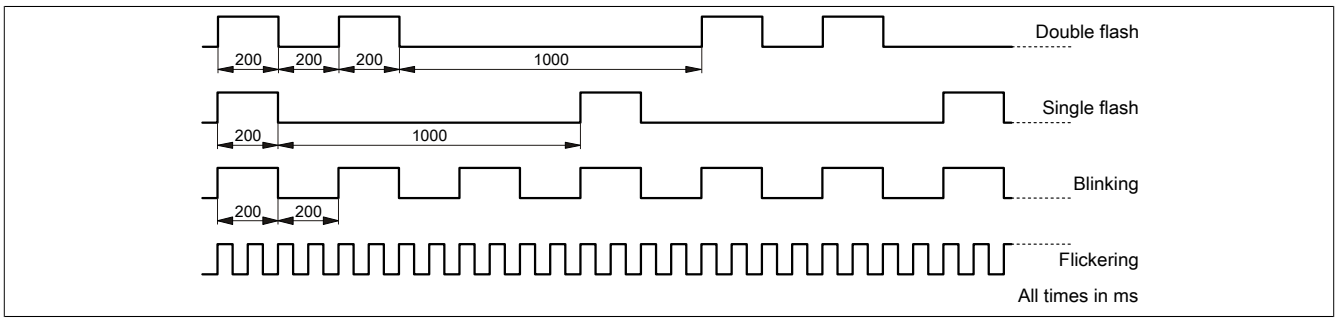
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) For the interfaces on the X20HB28G0 EtherCAT junction module, the hub runtime is 1.1 µs instead of 750 ns.
3) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
4) Spacing is based on the width of the X20BB81 bus base. One X20HB28G0 hub expansion module and one X20PS9400 or X20PS9402 supply module are also always required for the bus controller.

4.19.5.4 LED status indicators

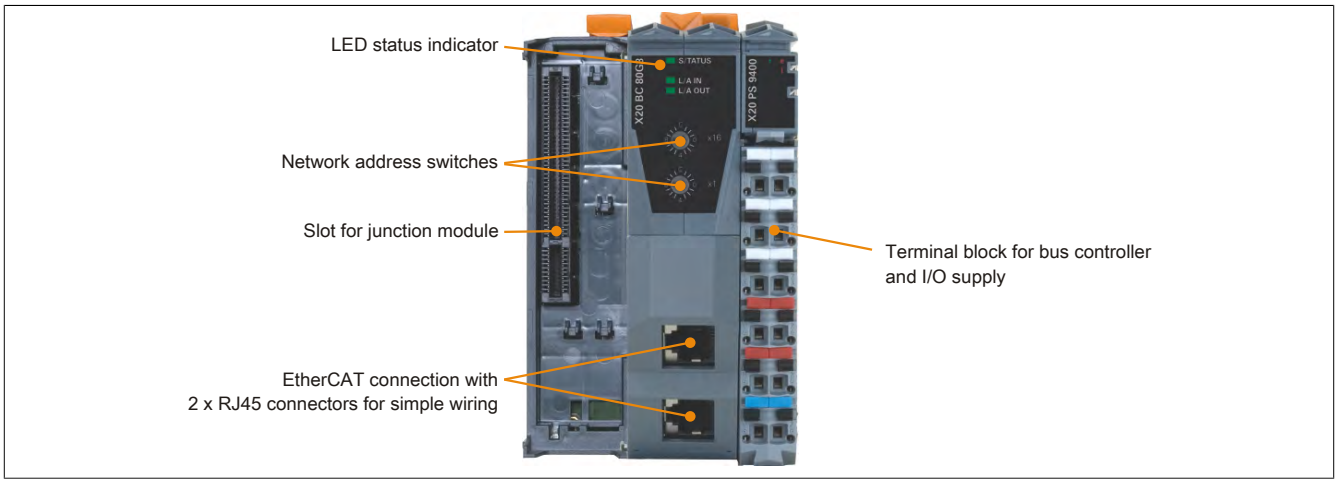
Figure	LED	Color	Status	Description
	STATUS1)	Green	On	The bus controller is OPERATIONAL.
			Blinking	PREOPERATIONAL status
			Single flash	SAFE-OPERATIONAL status
			Flickering	The bus controller has started and is not yet in INIT status or it is in BOOTSTRAP status (e.g.while downloading firmware).
			Off	INIT status
		Red	On	A critical communication or application error has occurred.
			Blinking	Invalid configuration data
			Single flash	The bus controller has an internal error and changed the EtherCAT status on its own
			Double flash	Watchdog timeout (process data watchdog or EtherCAT watchdog)
			Flickering	Error in the start procedure (INIT status has been achieved, but the error indicator bit in the AL status register is set)
			Off	No error
	L/A IN L/A OUT	Green	Blinking	The respective LED blinks when Ethernet activity is present (PORT OPEN) on the corresponding RJ45 port (IN, OUT).
			On	Connection (link) established, however no communication (PORT OPEN).
			Off	No physical Ethernet connection exists (PORT CLOSED).

1) The "STATUS" LED is a green/red dual LED and is used to indicate EtherCAT states ERROR and RUN.

Status LEDs - Blinking patterns

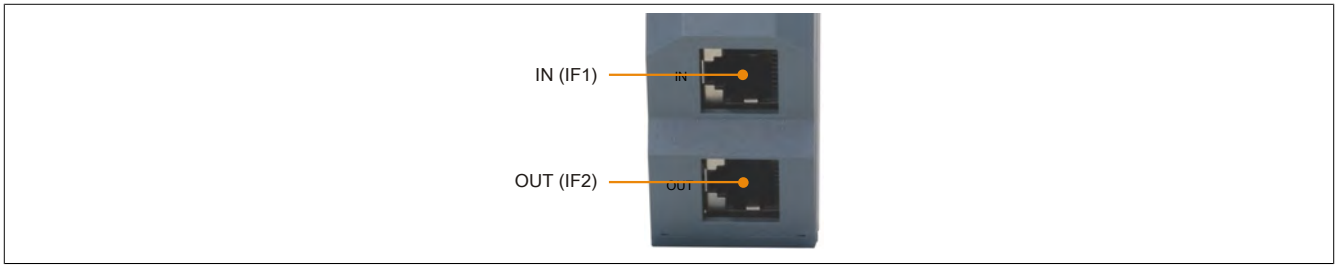


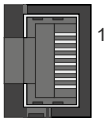
4.19.5.5 Operating and connection elements



4.19.5.6 RJ45 ports

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.19.5.7 EtherCAT network address switch

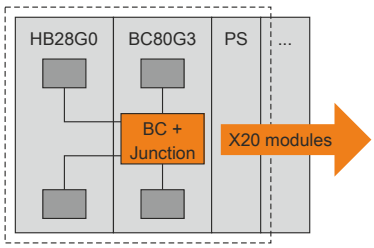
A slave alias address can be set using the two network address switches on the bus controller. During the initialization phase (during start-up), the bus controller writes the value of the address switch to the ESC register 0x12 or 0x13. However, the value is only accepted in the register if the value of the switch value is between 0x00 and 0xFA (decimal 250).

Switch position	Description
0x00 to 0xFA	Writes the address switch value to the "Station Alias" register.
0xFB to 0xFE	Address switch value not used. ESC Alias registers not changed.
0xFF	Address switch value not used. ESC Alias registers not changed. The bus controller boots with the default values if the address switch is set to the value "0xFF" before a restart. All set parameters remain unchanged in flash memory.

The master determines whether the alias address is used for the slave addressing by setting the corresponding bit in the ESC DL control register (bit 24).

4.19.5.8 Slot

The bus controller is equipped with an additional slot. The X20HB28G0 EtherCAT junction module is operated in this slot. The junction module is equipped with 2 RJ45 connections, which means that 4 ports are available.



4x with X20BB81

4.20 Expandable bus controllers system modules

The expandable X20 bus controllers are made up of a bus controller fieldbus interface, a bus controller system module and an X20TB12 terminal block.

Expandable bus controller system modules include the base module and the supply module for providing power to the entire system.

4.20.1 Brief information

Product ID	Short description	on page
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	2150
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	2152
X20IF1091-1	X20 interface module, for expandable bus controller, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately	2154
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	2150
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	2152

4.20.2 X20(c)BB81

4.20.2.1 General information

The bus module has an expansion slot. The following modules are used on this module:

- Base module (BC, HB, etc.)
- Add-on module (IF, HB, etc.)
- Supply module

The left and right end plates are included in the delivery.

- Bus base with one expansion slot

Information:

The bus controller must be placed in the rightmost slot.

4.20.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.20.2.3 Order data

Model number	Short description	Figure
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	

Table 438: X20BB81, X20cBB81 - Order data

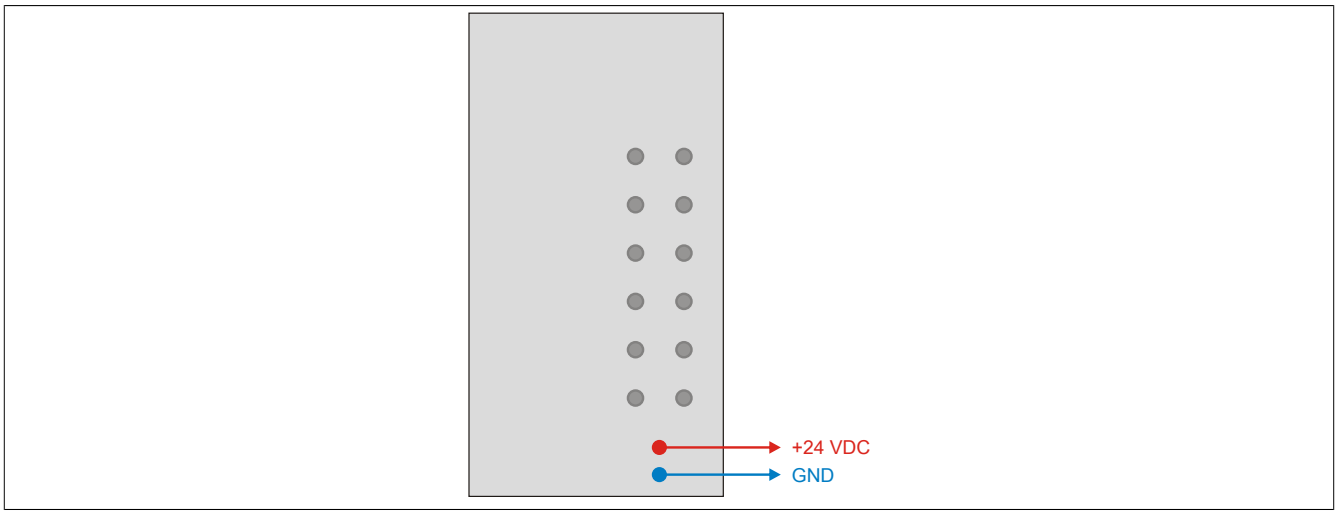
4.20.2.4 Technical data

Product ID	X20BB81	X20cBB81
Short description		
Bus module	Bus base with one expansion slot	
General information		
Power consumption		
Bus	0.35 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 1)	Yes	
KC	Yes	-
GOST-R	Yes	
I/O supply		
Nominal voltage	24 VDC	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Left and right X20 locking plates included in delivery	
Spacing	62.5$^{+0.2}$ mm	

Table 439: X20BB81, X20cBB81 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.20.2.5 Voltage routing



4.20.3 X20(c)BB82

4.20.3.1 General information

The bus module has two expansion slots. The following modules are used on this module:

- Base module (BC, HB, etc.)
- Two add-on modules (IF, HB, etc.)
- Supply module

The left and right end plates are included in the delivery.

- Bus base with two expansion slots

> **Information:**
>
> **The bus controller must be placed in the rightmost slot.**

4.20.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

> **For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.**

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.20.3.3 Order data

Model number	Short description	Figure
	System modules for expandable bus controllers	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	

Table 440: X20BB82, X20cBB82 - Order data

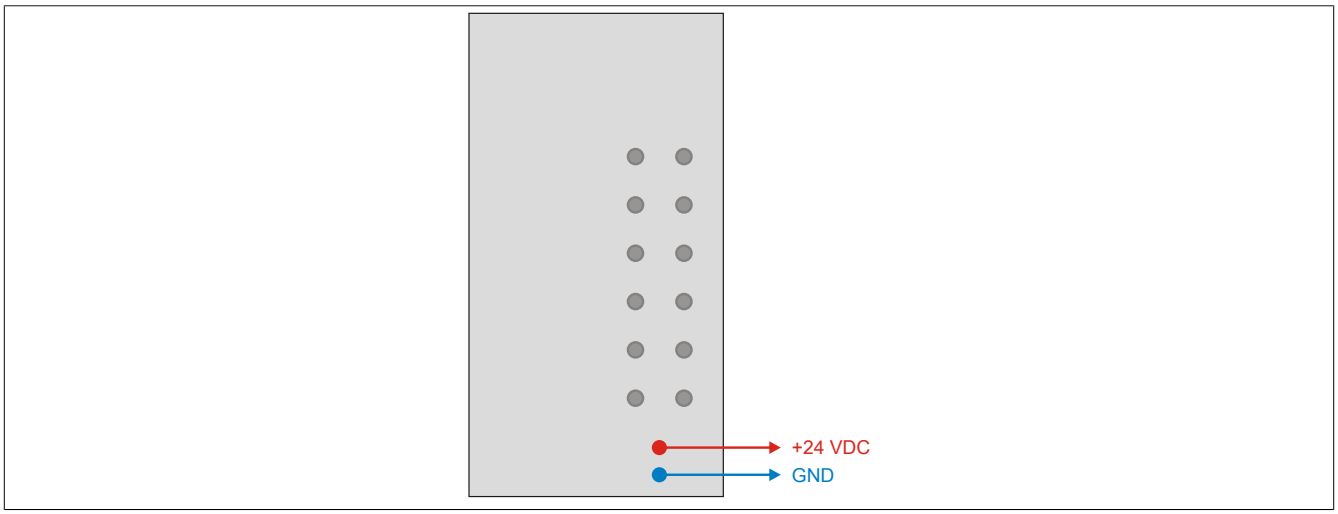
4.20.3.4 Technical data

Product ID	X20BB82	X20cBB82
Short description		
Bus module	Bus base with 2 expansion slots	
General information		
Power consumption		
Bus	0.35 W	
Internal I/O	-	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
I/O supply		
Nominal voltage	24 VDC	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Left and right X20 locking plates included in delivery	
Spacing	87.5$^{+0.2}$ mm	

Table 441: X20BB82, X20cBB82 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.20.3.5 Voltage routing



4.20.4 X20IF1091-1

4.20.4.1 General information

The interface module is operated in the X20BC1083 expandable bus controller. It is equipped with an X2X Link master interface.

- X2X Link connection

4.20.4.2 Order data

Model number	Short description	Figure
	System modules for expandable bus controllers	
X20IF1091-1	X20 interface module, for expandable bus controller, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB704.9	Accessory terminal block, 4-pin, screw clamps 2.5 mm²	
0TB704.91	Accessory terminal block, 4-pin, cage clamp terminal block 2.5 mm²	

Table 442: X20IF1091-1 - Order data

4.20.4.3 Technical data

Product ID	X20IF1091-1
Short description	
Communication module	1x X2X Link master
General information	
B&R ID code	0x2525
Status indicators	Module status, data transfer
Diagnostics	
Module status	Yes, using status LED
Data transfer	Yes, using status LED
Power consumption	1.29 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	X2X Link master
Design	4-pin male multipoint connector
Number of stations	Max. 253
Bus terminating resistor	Internal
Internal bus supply	No
Network topology	Line
Distance between 2 stations	Max. 100 m
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB704 terminal block separately
Slot	In the X20BC1083-1 expandable bus controller

Table 443: X20IF1091-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

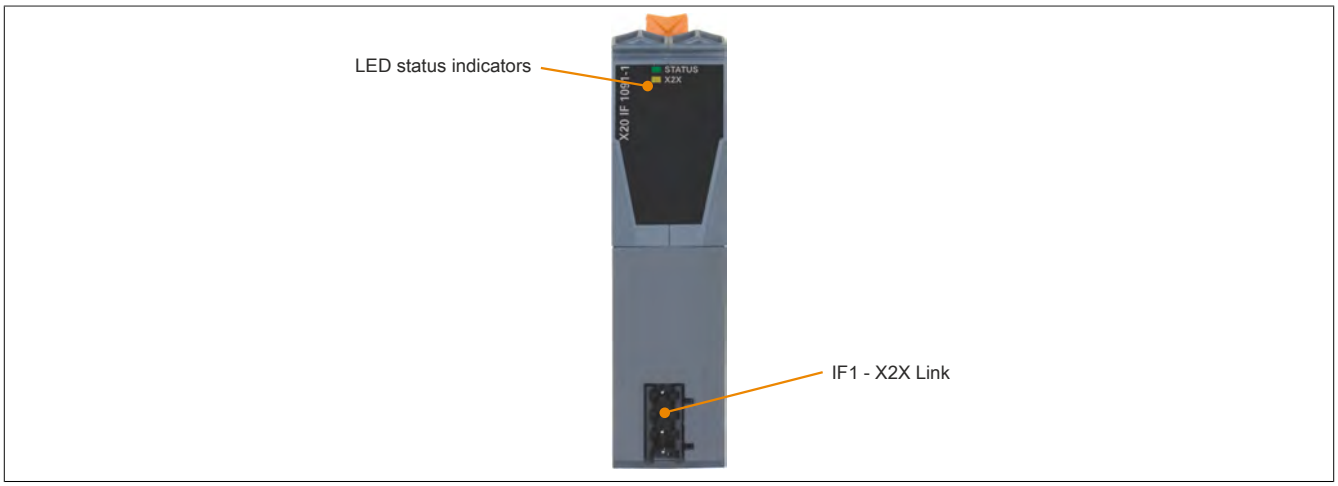
4.20.4.4 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.20.4.5 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	Bus controller booting
	X2X	Yellow	On	The module sends data via the X2X Link interface

4.20.4.6 Operating and connection elements



4.20.4.7 X2X Link interface (IF1)

Interface	Pinout		
	Terminal	Function	
	1	X2X	
	2	X2X⊥	
	3	X2X\	
	4	SHLD	Shield
4-pin male multipoint connector			

4.20.4.8 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.21 Fieldbus CPUs

Fieldbus CPUs are a variation of Compact CPUs. Their modular structure makes it easy to meet the unique requirements of each application.

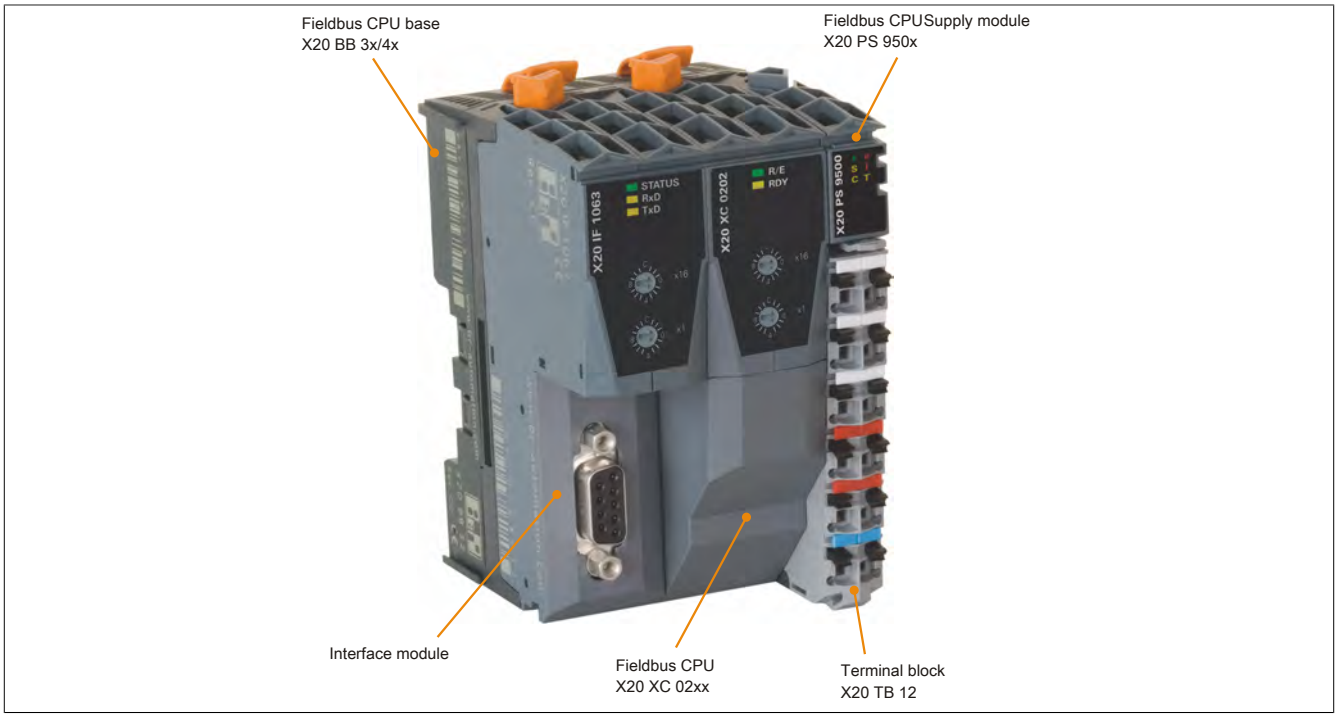


Figure 369: Modular structure of the Fieldbus CPU

Adaptable to individual requirements

- Embedded µP 25 with or without Ethernet on-board
- Embedded µP 16

- PROFIBUS DP master
- PROFIBUS DP slave
- CAN bus
- RS232
- RS485/RS422

- Bus module with RS232 connection
- Bus module with RS232 and CAN bus connections
- Both versions with one or two slots for interface modules

- Supply module for Fieldbus CPU, X2X Link bus supply and I/O
- RS232 interface connection
- CAN bus connection
- Without or without electrical isolation of the CPU/X2X Link supply

- 12-pin terminal block

The battery-free CPU

To meet the high demands of the market, the Fieldbus CPU was designed to run without a battery. This makes it completely maintenance-free. The following features make operation without a buffer battery possible.

The real-time clock is buffered for approx. 1000 hours by a gold foil capacitor.

This FRAM stores its contents ferroelectrically. Unlike normal SRAM, this does not require a battery.

Compact design

Despite the sleek profile of only 62,5 mm, the CPU supply, the X2X Link bus supply, and the I/O module supply are integrated in the CPU. No additional power modules are necessary.

4.21.1 Brief information

Product ID	Short description	on page
X20XC0201	X20 fieldbus CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus and interface module according to fieldbus CPU base, order power supply module, bus base and terminal block separately	2160
X20XC0202	X20 fieldbus CPU, µP 25, 750 kB SRAM, 3 MB FlashPROM, support of RS232, CAN bus and interface module according to fieldbus CPU base, order power supply module, bus base and terminal block separately	2160
X20XC0292	X20 fieldbus CPU, µP 25 750 kB SRAM, 3 MB FlashPROM, support of RS232, CAN bus and interface module, according to fieldbus CPU base, 1 Ethernet interface 100 Base-T, order bus base, power supply module and terminal block separately	2160

4.21.2 X20XC0201, X20XC0202, X20XC0292

4.21.2.1 General information

Fieldbus CPUs are variations of Compact CPUs. In addition to these features, there is also the option of connecting fieldbus modules to the left side. These CPUs make applications possible in which data preprocessing has to take place remotely within the I/O bus connection.

- Embedded µP 16 / µP 25 with additional I/O processor
- 100/750 kB User SRAM
- 1 MB / 3 MB User FlashPROM
- X20XC0292: Onboard Ethernet
- Up to two slots for fieldbus modules
- Only 62.5 mm wide
- No battery

4.21.2.2 Order data

XC0201, XC0202

XP0292

Model number	Short description
	Fieldbus CPUs
X20XC0201	X20 fieldbus CPU, µP 16, 100 kB SRAM, 1 MB FlashPROM, support of RS232, CAN bus and interface module according to fieldbus CPU base, order power supply module, bus base and terminal block separately
X20XC0202	X20 fieldbus CPU, µP 25, 750 kB SRAM, 3 MB FlashPROM, support of RS232, CAN bus and interface module according to fieldbus CPU base, order power supply module, bus base and terminal block separately
X20XC0292	X20 fieldbus CPU, µP 25 750 kB SRAM, 3 MB FlashPROM, support of RS232, CAN bus and interface module, according to fieldbus CPU base, 1 Ethernet interface 100 Base-T, order bus base, power supply module and terminal block separately
	Required accessories
	System modules for compact CPUs
X20PS9500	X20 supply module for compact and fieldbus CPUs and internal I/O supply, X2X Link supply
X20PS9502	X20 supply module, for compact and fieldbus CPUs and internal I/O supply, X2X Link supply, supply not electrically isolated
	System modules for fieldbus CPUs
X20BB32	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB37	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB42	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20BB47	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
	Terminal blocks
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed

Table 444: X20XC0201, X20XC0202, X20XC0292 - Order data

Model number	Included in delivery
X20AC0SL1	X20 locking plate, left
X20AC0SR1	X20 locking plate, right

4.21.2.3 Technical data

Product ID	X20XC0201	X20XC0202	X20XC0292
Short description			
Interfaces	-		1x Ethernet onboard
System module	CPU		
General information			
B&R ID code	0x2563	0x2564	0xA252
Status indicators	CPU function		CPU function, Ethernet
Diagnostics			
CPU function	Yes, using status LED		
Ethernet	-		Yes, using status LED
Overtemperature	-	Yes, using software	
Power consumption	2 W	2.2 W	2.8 W
Temperature sensor	No	Yes	
ACOPOS capability	Limited (User PROM)	Yes	
Visual Components support	Limited (User PROM)	Yes	
Additional power dissipation caused by the actuators (resistive) [W]	-		
Certification			
CE	Yes		
cULus	Yes		
cCSAus HazLoc Class 1 Division 2	Yes		
ATEX Zone 2 [1]	Yes		
KC	Yes		
GL	Yes		
GOST-R	Yes		
Controller			
Real-time clock [2]	Yes, 1 s resolution, -18 to 28 ppm accuracy at 25°C		
Processor			
Type	Embedded µP 16	Embedded µP 25	
Integrated I/O processor	Processes I/O data points in the background		
Backup battery	No		
Shortest task class cycle time	4 ms	2 ms	
Typical instruction cycle time	0.8 µs	0.5 µs	
Permanent variables			
Buffer duration	>10 years		
Memory	2.75 kB FRAM [3]		
Standard memory			
User PROM	1 MB FlashPROM	3 MB FlashPROM	
User RAM	100 kB SRAM [4]	750 kB SRAM [4]	
Slots for fieldbus modules			
X20BB3x	1		
X20BB4x	2		
Interfaces			
IF2 interface			
Signal	-		Ethernet
Design	-		1x RJ45 shielded
Cable length	-		Max. 100 m between 2 stations (segment length)
Transfer rate	-		100 Mbit/s
Transmission			
Physical layer	-		100BASE-TX
Half-duplex	-		Yes
Full-duplex	-		No
Autonegotiation	-		No
Auto-MDI / MDIX	-		Yes
On base module			
X20BB32 and X20BB42 [5]	Fieldbus CPU base module with integrated RS232 interface		
X20BB37 and X20BB47 [6]	Fieldbus CPU base module with integrated RS232 and CAN interfaces		
Operating conditions			
Mounting orientation			
Horizontal	Yes		
Vertical	Yes		
Installation at elevations above sea level			
0 to 2000 m	No limitations		
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m		
EN 60529 protection	IP20		
Environmental conditions			
Temperature			
Operation			
Horizontal installation	-25 to 60°C		
Vertical installation	-25 to 50°C		
Derating	-		
Storage	-40 to 85°C		
Transport	-40 to 85°C		

Table 445: X20XC0201, X20XC0202, X20XC0292 - Technical data

Product ID	X20XC0201	X20XC0202	X20XC0292
Relative humidity			
Operation	5 to 95%, non-condensing		
Storage	5 to 95%, non-condensing		
Transport	5 to 95%, non-condensing		
Mechanical characteristics			
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9500 or X20PS9502 power supply module separately Order 1x X20BB3x/4x fieldbus CPU base separately		
Spacing 7)			
X20BB3x	62.5+0.2 mm		
X20BB4x	87.5+0.2 mm		

Table 445: X20XC0201, X20XC0202, X20XC0292 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The real-time clock is buffered for approx. 1000 hours by a gold foil capacitor. The gold foil capacitor is completely charged after 18 continuous hours of operation.
3) This FRAM stores its contents ferroelectrically. Therefore, no backup battery is needed.
4) Not buffered.
5) For technical data, see the data sheet for the X20PS9500 power supply module.
6) For technical data, see the data sheet for the X20PS9502 power supply module.
7) Spacing is based on the width of the X20BB3x/4x fieldbus CPU base. The CPU always requires up to two fieldbus modules and one supply module X20PS9500 or X20PS9502.

4.21.2.4 LED status indicators

X20XC020x

Figure	LED	Color	Status	Description
	R/E	Green	On	Application running
		Red	On	SERVICE mode
			Off	1)
	RDY	Yellow	On	SERVICE mode
			Off	1)

1) BOOT mode: R/E and RDY LEDs are off and the power supply LED is blinking

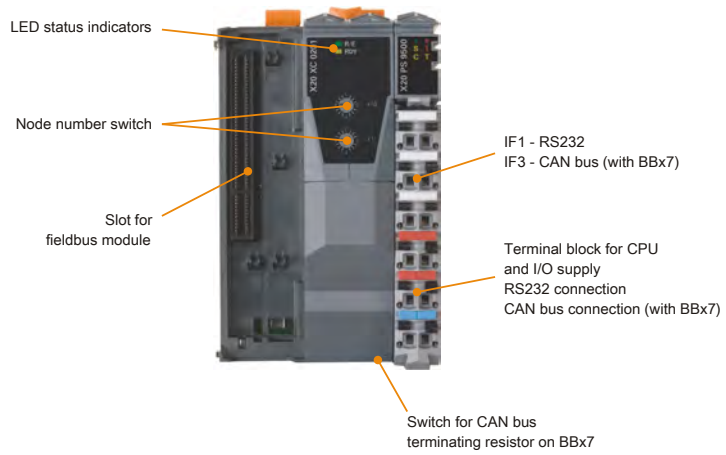
X20XC0292

Figure	LED	Color	Status	Description
	R/E	Green	On	Application running
		Red	On	SERVICE mode
		Off		1)
	RDY	Yellow	On	SERVICE mode
			Off	1)
	L/A	Green	On	A link to the peer station has been established.
			Blinking	A link to the peer station has been established. Indicates Ethernet activity is taking place on the bus.

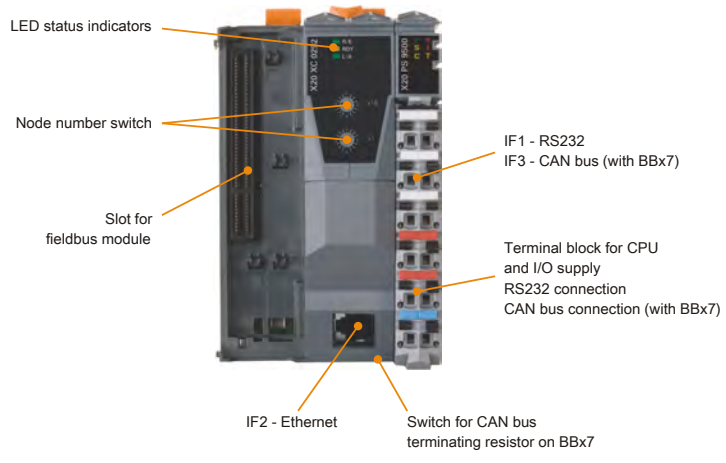
1) BOOT mode: R/E and RDY LEDs are off and the power supply LED is blinking

4.21.2.5 Operating and connection elements

X20XC0201 and X20XC0202



X20XC0292



4.21.2.6 Node number switches

The node number is set using the two hex switches. The switch setting can be evaluated by the application program at any time. The operating system only evaluates the switch position when the device is switched on.

Switch position	Operating mode	Description
0x00	BOOT	In this switch position, the operating system can be installed via the RS232 interface configured as the online interface. User Flash is deleted only after the update begins.
0x01 - 0xFE	RUN	RUN mode, the application is running.
0xFF	Diagnostics	Boots the CPU in Diagnostics mode. Program sections in User RAM and User FlashPROM are not initialized. Following diagnostics mode, the CPU always boots with a **cold restart**.

X20XP0201 and X20XP0202

When used with the X20BB37 or X20BB47 bus module, the CPUs have access to a CAN bus interface. The INA2000 station number for CAN is set using the node number switches.

X20XP0292

This CPU is equipped with an onboard Ethernet interface. When used with the X20BB37 or X20BB47 bus module, it also has access to a CAN bus interface.

The number set using the two hex switches defines the INA2000 station number of both the CAN and the Ethernet interface.

4.21.2.7 Ethernet interface (IF2)

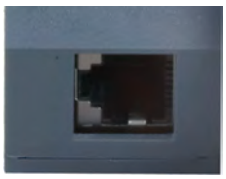
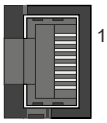


Figure 370: X20 compact CPUs - Ethernet interface for X20CP0291 and X20CP0292

The X20XC0292 is equipped with an Ethernet interface. The connection is made using a 100 BASE-T twisted pair RJ45 socket.

Pinout

Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).

Information:

The Ethernet interface (IF2) is not suited for POWERLINK.

Starting with operating system version 1.07, CPUs have a default IP address.

IP address: 192.168.0.1
Subnet mask: 255.255.0.0

4.21.2.8 Slot for fieldbus modules

Up to two fieldbus modules can be connected to the left side of the Fieldbus CPUs depending on the CPU base:

CPU base	Slots for fieldbus modules
X20BB32, X20BB37	1
X20BB42, X20BB47	2

Table 446: X20 Fieldbus CPUs - Slots for fieldbus modules depending on CPU base

The X20 system can be connected to various bus and network systems by selecting the appropriate fieldbus modules. The following fieldbus modules can be operated with the CPUs:

Module	Description
X20IF1020	X20 interface module, 1 RS232, max. 115.2 kbit/s, electrically isolated
X20IF1030	X20 interface module, 1 RS485/RS422, max. 115.2 kbit/s, electrically isolated
X20IF1041-1	X20 interface module for DTM configuration, 1 CANopen master interface, electrically isolated
X20IF1043-1	X20 interface module for DTM configuration, 1 CANopen slave interface, electrically isolated
X20IF1051-1	X20 interface module for DTM configuration, 1 DeviceNet scanner interface, electrically isolated
X20IF1053-1	X20 interface module for DTM configuration, 1 DeviceNet slave (adapter) interface, electrically isolated
X20IF1061	X20 interface module, 1 Profibus DP master interface, max.12 Mbit/s, max. 3.5 KB input data and max. 3.5 KB output data, electrically isolated
X20IF1061-1	X20 interface module for DTM configuration, 1 PROFIBUS DP V1 master interface, electrically isolated
X20IF1063	X20 interface module, 1 Profibus DP slave interface, max.12 Mbit/s, electrically isolated
X20IF1063-1	X20 interface module for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated
X20IF1074	X20 interface module for SGC, 1 CAN interface, max. 1 Mbit/s, electrically isolated,...
X20IF10A1-1	X20 interface module for DTM configuration, 1 ASi master interface, electrically isolated
X20IF10D1-1	X20 interface module for DTM configuration, 1 EtherNet/IP scanner interface, electrically isolated
X20IF10D3-1	X20 interface module for DTM configuration, 1 EtherNet/IP slave interface, electrically isolated
X20IF10E1-1	X20 interface module for DTM configuration, 1 PROFINET RT controller (master), electrically isolated
X20IF10E3-1	X20 interface module for DTM configuration, 1 PROFINET RT device (slave), electrically isolated
X20IF10G3-1	X20 interface module for DTM configuration, 1 EtherCAT slave interface, electrically isolated
X20IF10H3-1	X20 interface module for DTM configuration, 1 Sercos III slave interface, electrically isolated

Table 447: X20 fieldbus CPUs - Possible fieldbus modules

4.21.2.9 Programming the system flash memory

General information

CPUs are delivered with a runtime system. When delivered, the node number switch is set to switch position 0x00 (bootstrap loader mode).

A suitable switch position must be set (0x01 to 0xFE) in order to boot the PLC in RUN mode. Updating the runtime system is only possible in RUN mode.

Runtime system update

The runtime system can be updated via the programming environment. When updating the runtime system via an online connection, the following procedure must be carried out:

1. An online runtime system update is only possible if the processor is in RUN mode. For this to be true, the node number must be set to a value in the range 0x01 to 0xFE.
2. Switch on the power.
3. The runtime system update is performed via the existing online connection. The online connection can be established via the onboard serial RS232 interface, for example. If a CPU has an Ethernet interface, then it too can be used to perform the update.
4. Start B&R Automation Studio.
5. Start the update procedure by selecting **Online** from the **Project** menu. Select **Transfer Automation Runtime** from the pop-up menu. Now follow the instructions given by B&R Automation Studio.
6. A window opens up for setting the runtime system version. The runtime system version is already pre-selected by the project settings made by the user. The drop-down menu can be used to select one of the runtime system versions stored in the project. Clicking on the **Browse** button allows a runtime system version to be loaded from the hard drive or CD.

   Clicking on **Next** opens a pop-up window that allows the user to select whether modules with target memory SYSTEM ROM should be transferred during the subsequent runtime system update. If not, these modules can also be transferred later during an application download.

   Clicking on **Next** opens a dialog box where the user can set the CAN transfer rate, CAN ID and CAN node number (the CAN node number set here is only relevant if an interface module does not have a CAN node number switch). The CAN node number must be between decimal 01 and 99. Assigning a unique node number is especially important with online communication over a CAN network (INA2000 protocol).
7. The update procedure is started by clicking on **Next**. Update progress is shown in a message box.

   > **Information:**
   >
   > **User flash memory is deleted.**
8. When the update procedure is complete, the online connection is reestablished automatically.
9. The PLC is now ready for use.

Updating the runtime system is possible not only via an online connection, but also via a CAN network, serial network (INA2000 protocol) or Ethernet network, depending on the system configuration.

4.22 Fieldbus CPUs system modules

The X20 system Fieldbus CPUs consist of the Fieldbus CPU, Fieldbus CPU system modules and the X20TB12 terminal block.

Fieldbus CPU system modules include the base module and the supply modules for providing power to the entire system.

4.22.1 Brief information

Product ID	Short description	on page
X20BB32	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included	2168
X20BB37	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, Slot for X20 interface module, X20 connection, X20 locking plates X20AC0SL1/ X20AC0SR1 (left and right) included	2170
X20BB42	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included	2172
X20BB47	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	2174
X20IF1074	X20 interface module, for SGC, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately	2176

4.22.2 X20BB32

4.22.2.1 General information

The bus module is the base for all X20 Fieldbus CPUs.

The left and right end plates are included in the delivery.

- Base for all X20 Fieldbus CPUs
- RS232 connection

Information:

The bus controller must be placed in the rightmost slot.

4.22.2.2 Order data

Model number	Short description	Figure
	System modules for fieldbus CPUs	
X20BB32	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, Slot for X20 interface module, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	

Table 448: X20BB32 - Order data

4.22.2.3 Technical data

Product ID	X20BB32
Short description	
Bus module	X20 fieldbus CPU base, backplane for fieldbus CPU, fieldbus CPU supply module and interface module
Interfaces	1x RS232 connection
General information	
Power consumption	
Bus	0.35 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - RS232	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20

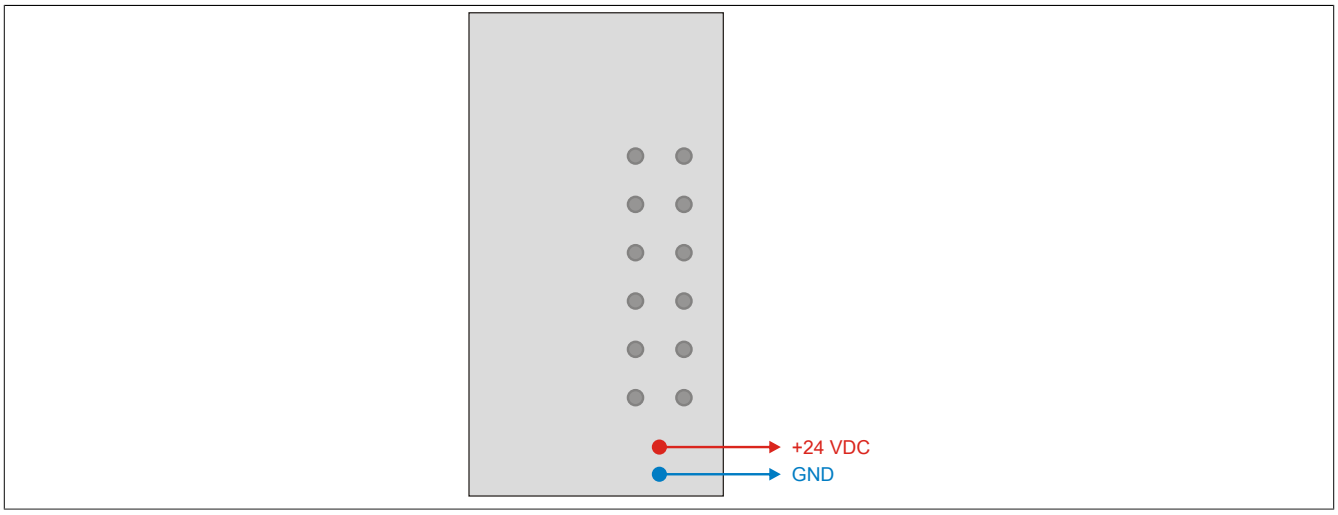
Table 449: X20BB32 - Technical data

Product ID	X20BB32
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Left and right X20 locking plates included in delivery
Spacing	$62.5^{+0.2}$ mm

Table 449: X20BB32 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.22.2.4 Voltage routing



4.22.3 X20BB37

4.22.3.1 General information

The bus module is the base for all X20 Fieldbus CPUs.

The left and right end plates are included in the delivery.

- Base for all X20 Fieldbus CPUs
- RS232 connection
- CAN bus connection
- Integrated terminating resistor for CAN bus

Information:

The bus controller must be placed in the rightmost slot.

4.22.3.2 Order data

Model number	Short description	Figure
	System modules for fieldbus CPUs	
X20BB37	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, Slot for X20 interface module, X20 connection, X20 locking plates X20AC0SL1/X20AC0SR1 (left and right) included	

Table 450: X20BB37 - Order data

4.22.3.3 Technical data

Product ID	X20BB37
Short description	
Bus module	X20 fieldbus CPU base, backplane for fieldbus CPU, fieldbus CPU supply module and interface module
Interfaces	1x RS232 connection, 1x CAN bus connection
General information	
Power consumption	
Bus	0.56 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - CAN bus	No
Bus - RS232	No
RS232 - CAN bus	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m

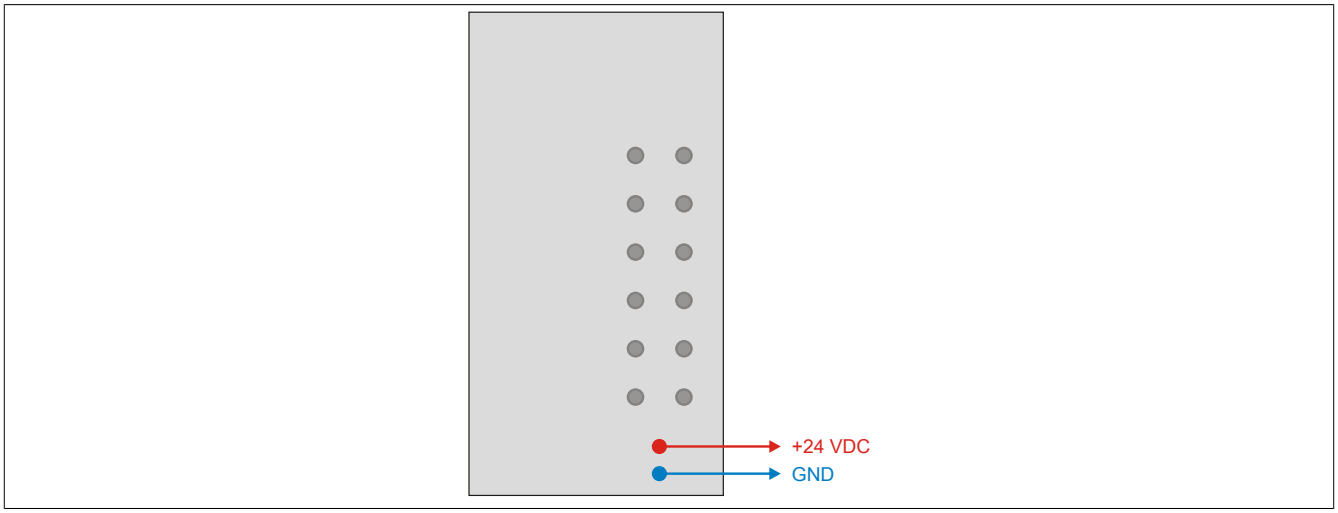
Table 451: X20BB37 - Technical data

Product ID	X20BB37
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Left and right X20 locking plates included in delivery
Spacing	62.5 $^{+0.2}$ mm

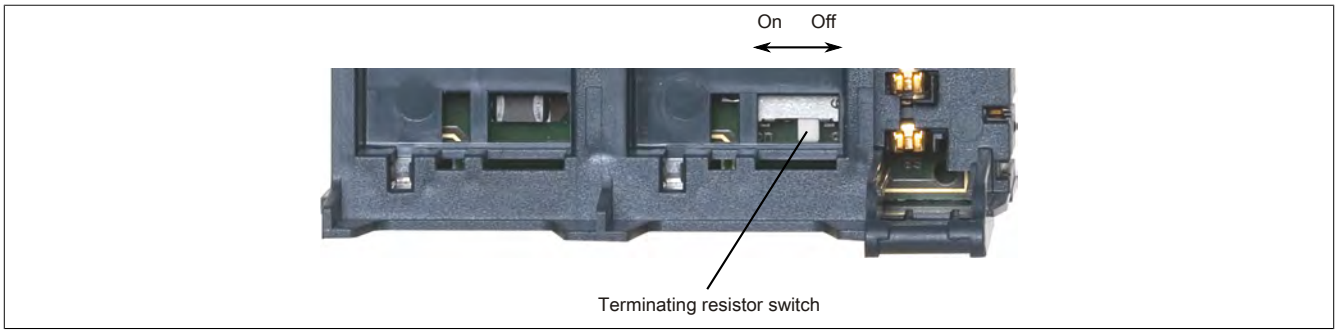
Table 451: X20BB37 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.22.3.4 Voltage routing



4.22.3.5 Terminating resistor for CAN bus



The bus module has an integrated CAN bus terminating resistor. The terminating resistor is turned on and off with a switch. An active terminating resistor is indicated on the supply module by the "T" LED.

4.22.4 X20BB42

4.22.4.1 General information

The bus module is a base for all X20 Fieldbus CPUs. It is equipped with 2 slots for interface modules.

The left and right end plates are included in the delivery.

- Base for all X20 Fieldbus CPUs
- 2 slots for interface modules
- RS232 connection

> **Information:**
>
> **The bus controller must be placed in the rightmost slot.**

4.22.4.2 Order data

Model number	Short description	Figure
	System modules for fieldbus CPUs	
X20BB42	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	

Table 452: X20BB42 - Order data

4.22.4.3 Technical data

Product ID	X20BB42
Short description	
Bus module	X20 fieldbus CPU base, backplane for fieldbus CPU, fieldbus CPU supply module and two interface modules
Interfaces	1x RS232 connection
General information	
Power consumption	
Bus	0.35 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - RS232	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m

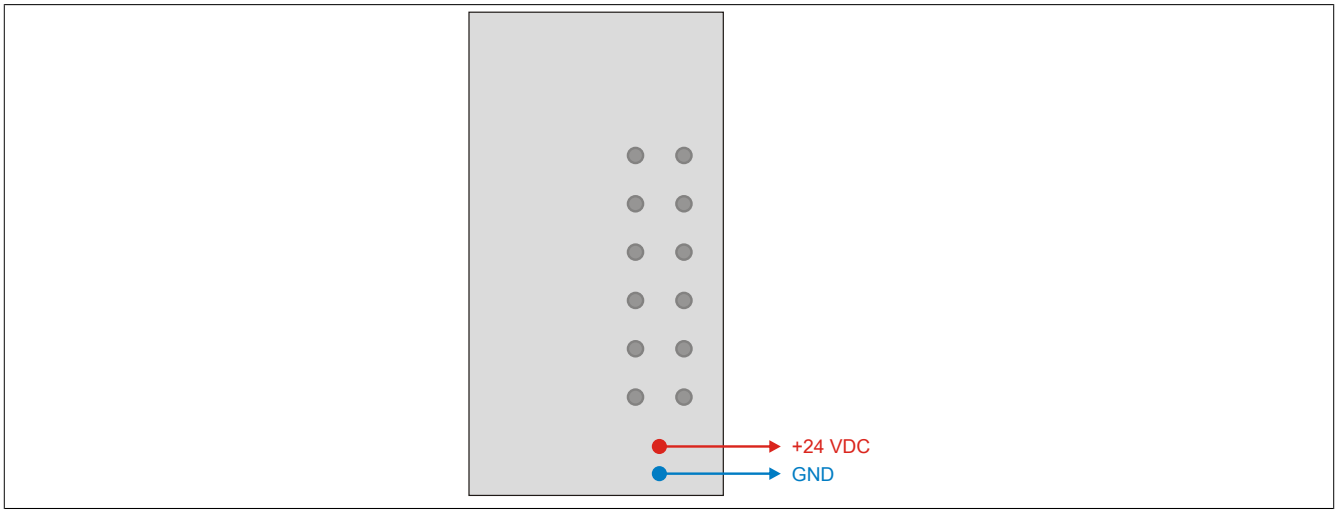
Table 453: X20BB42 - Technical data

Product ID	X20BB42
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Left and right X20 locking plates included in delivery
Spacing	87.5$^{+0.2}$ mm

Table 453: X20BB42 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.22.4.4 Voltage routing



4.22.5 X20BB47

4.22.5.1 General information

The bus module is a base for all X20 Fieldbus CPUs. It is equipped with 2 slots for interface modules.

The left and right end plates are included in the delivery.

- Base for all X20 Fieldbus CPUs
- 2 slots for interface modules
- RS232 connection
- CAN bus connection
- Integrated terminating resistor for CAN bus

Information:

The bus controller must be placed in the rightmost slot.

4.22.5.2 Order data

Model number	Short description	Figure
	System modules for fieldbus CPUs	
X20BB47	X20 fieldbus CPU base, for fieldbus CPU and compact CPU power supply module, base for integrated RS232 and CAN bus interface, 2 slots for X20 interface modules, X20 connection, X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	

Table 454: X20BB47 - Order data

4.22.5.3 Technical data

Product ID	X20BB47
Short description	
Bus module	X20 fieldbus CPU base, backplane for fieldbus CPU, fieldbus CPU supply module and two interface modules
Interfaces	1x RS232 connection, 1x CAN bus connection
General information	
Power consumption	
Bus	0.56 W
Internal I/O	-
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - CAN bus	No
Bus - RS232	No
RS232 - CAN bus	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
I/O supply	
Nominal voltage	24 VDC
Permitted contact load	10 A

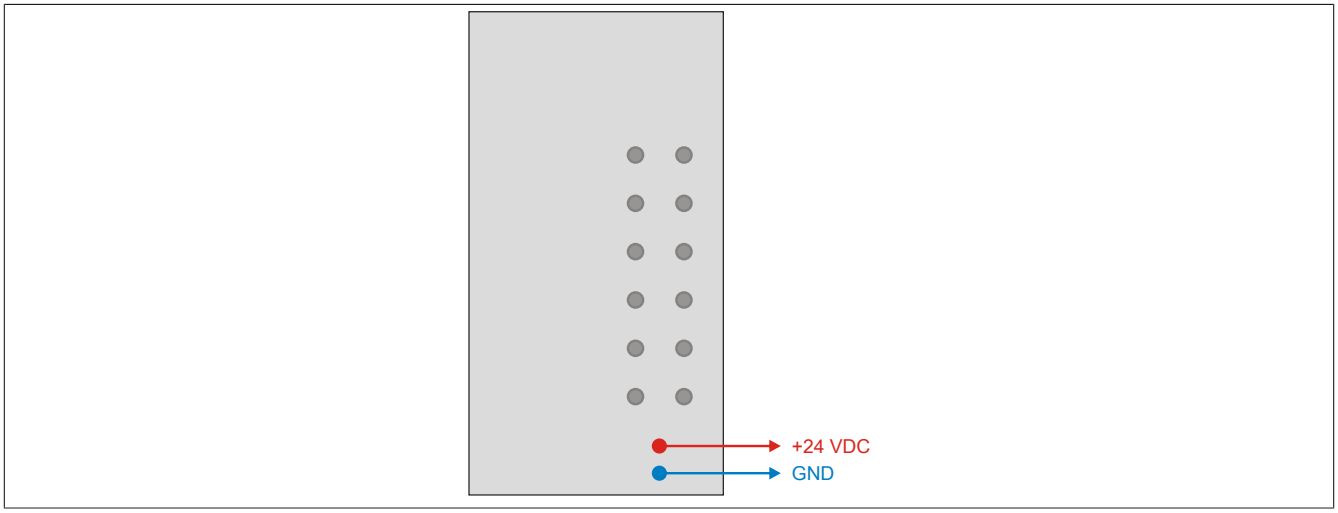
Table 455: X20BB47 - Technical data

Product ID	X20BB47
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Left and right X20 locking plates included in delivery
Spacing	87.5$^{+0.2}$ mm

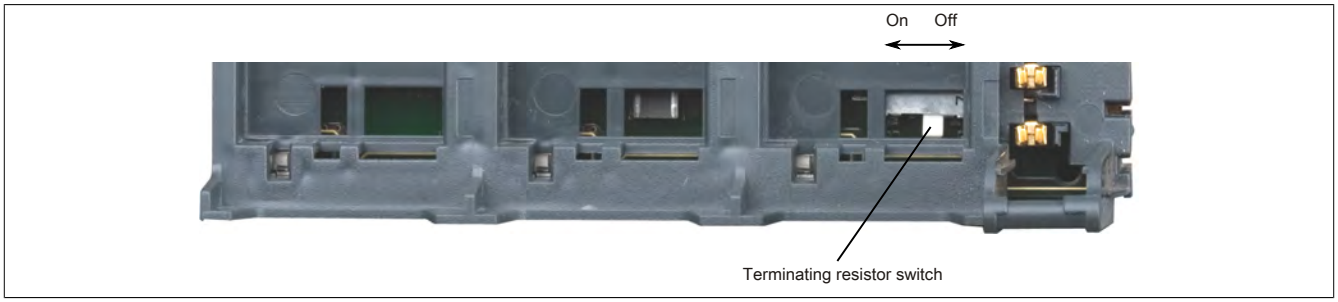
Table 455: X20BB47 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.22.5.4 Voltage routing



4.22.5.5 Terminating resistor for CAN bus



The bus module has an integrated CAN bus terminating resistor. The terminating resistor is turned on and off with a switch. An active terminating resistor is indicated on the supply module by the "T" LED.

4.22.6 X20IF1074

4.22.6.1 General information

The module is an interface module for the X20 fieldbus CPU.

- CAN bus connection
- Integrated terminating resistor

4.22.6.2 Order data

Model number	Short description	Figure
	System modules for fieldbus CPUs	
X20IF1074	X20 interface module, for SGC, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	

Table 456: X20IF1074 - Order data

4.22.6.3 Technical data

Product ID	X20IF1074
Short description	
Communication module	1x CAN bus
General information	
B&R ID code	0xA399
Status indicators	Module status, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	0.69 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Signal	CAN bus
Design	5-pin male multipoint connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Terminating resistor	Integrated in the module
Controller	SJA 1000
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB2105 terminal block separately
Slot	In X20 fieldbus CPU

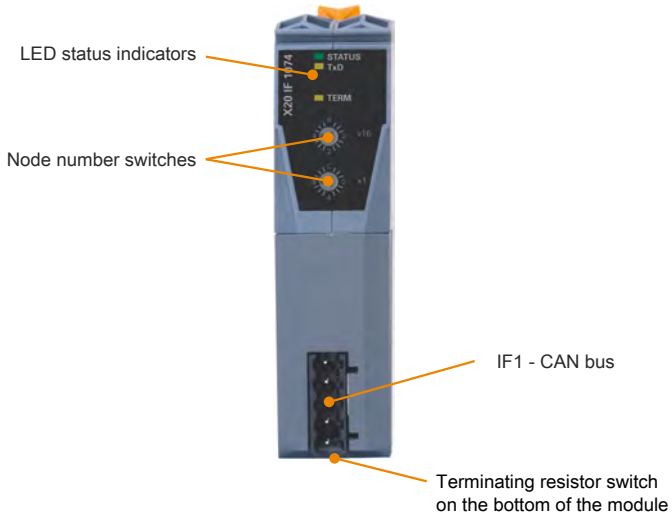
Table 457: X20IF1074 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.22.6.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	TxD	Yellow	On	The module is sending data via the CAN bus interface
	TERM	Yellow	On	Terminating resistor integrated in the module switched on.

4.22.6.5 Operating and connection elements

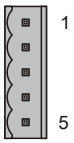


4.22.6.6 Node number switch

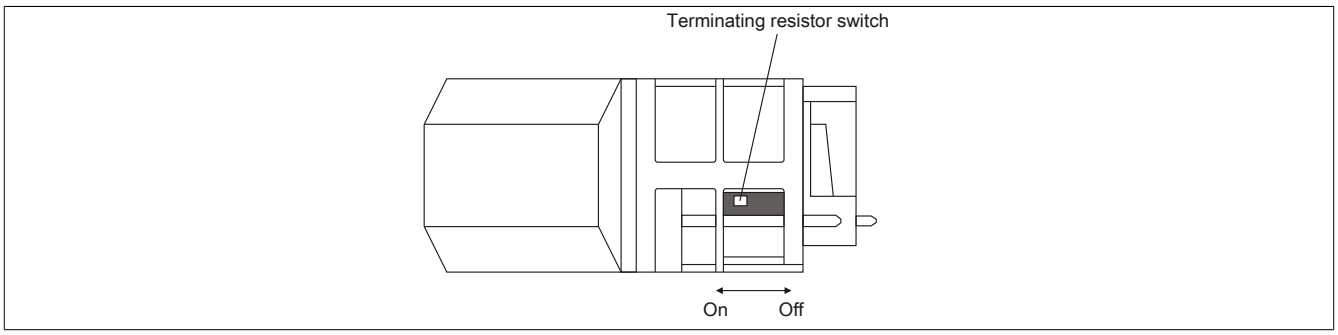
The node number for the interface is set with the two hex switches.

4.22.6.7 CAN bus interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	**Terminal**	**Function**	
	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	

4.22.6.8 Terminating resistor



A terminating resistor is integrated in the interface module. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.22.6.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23 X20 interface module communication

The interface modules are added to the X20 CPU as an application-specific interface expansion.

4.23.1 Brief information

Product ID	Short description	on page
X20IF1020	X20 interface module, 1 RS232 interface, max. 115.2 kbit/s, electrically isolated	2181
X20IF1030	X20 interface module, 1 RS422/485 interface, max. 115.2 kbit/s, electrically isolated	2184
X20IF1041-1	X20 interface module, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately	2187
X20IF1043-1	X20 interface module, for DTM configuration, 1 CANopen slave interface, electrically isolated, order 1x TB2105 terminal block separately	2191
X20IF1051-1	X20 interface module, for DTM configuration, 1 DeviceNet scanner (master) interface, electrically isolated, order 1x TB2105 terminal block separately	2195
X20IF1053-1	X20 interface module, for DTM configuration, 1 DeviceNet adapter (slave) interface, electrically isolated, order 1x TB2105 terminal block separately	2199
X20IF1061	X20 interface module, 1 PROFIBUS DP V0/V1 master interface, max. 12 Mbit/s, max. 3.5 kB input data and max. 3.5 kB output data, electrically isolated	2203
X20IF1061-1	X20 interface module for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated	2206
X20IF1063	X20 interface module, 1 PROFIBUS DP V0 slave interface, max. 12 Mbit/s, electrically isolated	2210
X20IF1063-1	X20 interface module, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated	2213
X20IF1065	X20 interface module, 1 PROFIBUS DP V1 slave interface, max. 12 Mbit/s, electrically isolated	2217
X20IF1072	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately	2220
X20IF1082	X20 interface module, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function	2224
X20IF1082-2	X20 interface module, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function PRC function	2230
X20IF1086-2	X20 interface module, 1 POWERLINK interface, managing or controlled node, PRC function, 1 fiber optic connection	2236
X20IF1091	X20 interface module, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately	2242
X20IF10A1-1	X20 interface module, for DTM configuration, 1 ASi master interface, electrically isolated, order 1x TB704 terminal block separately	2245
X20IF10D1-1	X20 interface module, for DTM configuration, 1 EtherNet/IP scanner (master) interface, electrically isolated	2249
X20IF10D3-1	X20 interface module, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated	2253
X20IF10E1-1	X20 interface module for DTM configuration, 1 PROFINET RT controller (master) interface, electrically isolated	2257
X20IF10E3-1	X20 interface module, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated	2261
X20IF10G3-1	X20 interface module for DTM configuration, 1 EtherCAT slave interface, electrically isolated	2265
X20IF10X0	X20 interface module, 1 redundancy link interface 1000BASE-SX, CPU-CPU data synchronization module for controller redundancy	2269
X20IF2181-2	X20 interface module, 1x link selector for POWERLINK cable redundancy, POWERLINK functions: - Managing node - Controlled node for iCN operation - Redundant managing node for controller redundancy - Ring redundancy - 2x hub - Multi ASend - PRC function 2x RJ45	2273
X20IF2772	X20 interface module, 2 CAN bus interfaces, max. 1 Mbit/s, electrically isolated, order 2x TB2105 terminal block separately	2279
X20IF2792	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, 1 X2X Link master interface, electrically isolated, order 1x TB2105 and 1x TB704 terminal block separately	2283
X20cIF1030	X20 interface module, coated, 1 RS422/485 interface, max. 115.2 kbit/s, electrically isolated	2184
X20cIF1041-1	X20 interface module, coated, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately	2187
X20cIF1061-1	X20 interface module coated, for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated	2206
X20cIF1063-1	X20 interface module, coated, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated	2213
X20cIF1072	X20 interface module, coated, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately	2220
X20cIF1082-2	X20 interface module, coated, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function PRC function	2230
X20cIF10D3-1	X20 interface module, coated, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated	2253
X20cIF10E3-1	X20 interface module, coated, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated	2261
X20cIF10X0	X20 interface module, coated, 1 redundancy link interface 1000 Base-FX, CPU-CPU data synchronization for controller redundancy	2269
X20cIF2181-2	X20 interface module, coated, 1x link selector for POWERLINK cable redundancy, POWERLINK functions: - Managing node - Controlled node for iCN operation - Redundant managing node for controller redundancy - Ring redundancy - 2x hub - Multi ASend - PRC function 2x RJ45	2273

4.23.2 X20IF1020

4.23.2.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with an RS232 interface.

- The RS232 interface can be configured as an online interface

4.23.2.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1020	X20 interface module, 1 RS232 interface, max. 115.2 kbit/s, electrically isolated	
	Optional accessories	
	Cables	
0G0001.00-090	PC - PLC/PW cable, RS232, online cable	

Table 458: X20IF1020 - Order data

4.23.2.3 Technical data

Product ID	X20IF1020
Short description	
Communication module	1x RS232
General information	
B&R ID code	0x1F27
Status indicators	Module status, data transfer
Diagnostics	
Module status	Yes, using status LED
Data transfer	Yes, using status LED
Power consumption	0.33 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Signal	RS232
Design	9-pin male DSUB connector
Max. distance	900 m
Transfer rate	Max. 115.2 kbit/s
Network-capable	No
FIFO	16 bytes in transmit and receive direction
Handshake lines	RTS, CTS
Controller	UART type 16C550 compatible
Data formats	
Data bits	5 to 8
Parity	Yes / No / Even / Odd
Stop bits	1 or 2
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In X20 CPU

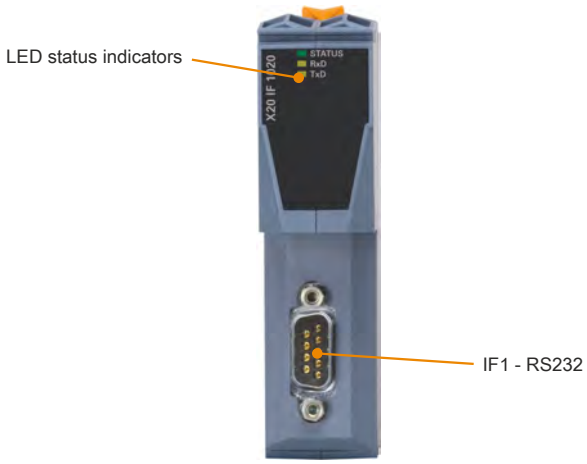
Table 459: X20IF1020 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

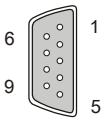
4.23.2.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	RxD	Yellow	On	The module receives data via the RS232 interface
	TxD	Yellow	On	The module sends data via the RS232 interface

4.23.2.5 Operating and connection elements



4.23.2.6 RS232 interface (IF1)

Interface	Pinout		
	Pin	RS232	
 9-pin male DSUB connector	1	NC	
	2	RxD	Receive signal
	3	TxD	Transmit signal
	4	NC	
	5	GND	Ground
	6	NC	
	7	RTS	Request To Send
	8	CTS	Clear To Send
	9	NC	

4.23.2.7 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.3 X20(c)IF1030

4.23.3.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with an RS485/RS422 interface.

- RS485/RS422 connection

4.23.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.3.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1030	X20 interface module, 1 RS422/485 interface, max. 115.2 kbit/s, electrically isolated	
X20cIF1030	X20 interface module, coated, 1 RS422/485 interface, max. 115.2 kbit/s, electrically isolated	
	Optional accessories	
	Infrastructure components	
0G1000.00-090	Bus connector, RS485, for PROFIBUS networks	

Table 460: X20IF1030, X20cIF1030 - Order data

4.23.3.4 Technical data

Product ID	X20IF1030	X20cIF1030
Short description		
Communication module	1x RS485/RS422	
General information		
B&R ID code	0x1F28	0xE233
Status indicators	Module status, data transfer	
Diagnostics		
Module status	Yes, using status LED	
Data transfer	Yes, using status LED	
Power consumption	0.4 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - IF1	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
IF1 interface		
Signal	RS485/RS422	
Design	9-pin female DSUB connector	
Max. distance	1200 m	
Transfer rate	Max. 115.2 kbit/s	
FIFO	16 bytes in transmit and receive direction	
Terminating resistor	External T-connector (0G1000.00-090)	
Controller	UART type 16C550 compatible	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	In X20 CPU	In X20c CPU

Table 461: X20IF1030, X20cIF1030 - Technical data

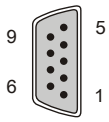
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.3.5 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	RxD	Yellow	On	The module is receiving data via the RS485/RS422 interface
	TxD	Yellow	On	The module is sending data via the RS485/RS422 interface

4.23.3.6 Operating and connection elements

4.23.3.7 RS485/RS422 interface (IF1)

Interface	Pinout		
	Pin	RS485	RS422
User interface RS485/RS422  9-pin female DSUB connector	1	Reserved	Reserved
	2	Reserved	TxD[1)]
	3	DATA	RxD
	4	Reserved	Reserved
	5	GND	GND
	6	+5 V / 50 mA	+5 V / 50 mA
	7	Reserved	TXD\[1)]
	8	DATA\	RXD\
	9	Reserved	Reserved

1) RS422 send data is TRISTATE-capable.

4.23.3.8 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.4 X20(c)IF1041-1

4.23.4.1 General information

The interface module is equipped with a CANopen master interface. It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

- CANopen master
- Integrated terminating resistor

4.23.4.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.4.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1041-1	X20 interface module, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately	
X20cIF1041-1	X20 interface module, coated, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	

Table 462: X20IF1041-1, X20cIF1041-1 - Order data

4.23.4.4 Technical data

Product ID	X20IF1041-1	X20cIF1041-1
Short description		
Communication module	CANopen master	
General information		
B&R ID code	0xA709	0xE505
Status indicators	Module status, network status, data transfer, terminating resistor	
Diagnostics		
Module status	Yes, using status LED and software	
Network status	Yes, using status LED and software	
Data transfer	Yes, using status LED	
Terminating resistor	Yes, using status LED	
Power consumption	1.1 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - IF1	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
IF1 interface		
Fieldbus	CANopen master	
Design	5-pin male multipoint connector	
Max. distance	1000 m	
Transfer rate	Max. 1 Mbit/s	
Terminating resistor	Integrated in the module	
Controller	netX100	
Memory	8 MB SDRAM	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x TB2105 terminal block separately	
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller	In the X20c CPU and in the X20cBC1083 expandable bus controller

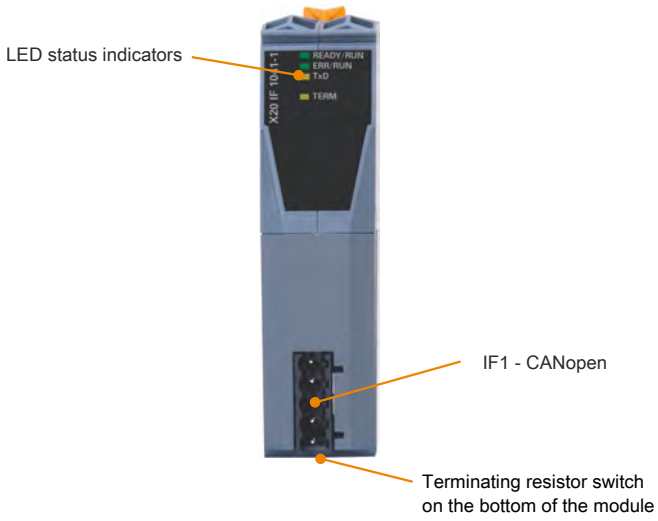
Table 463: X20IF1041-1, X20cIF1041-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.4.5 LED status indicators

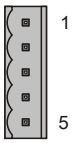
Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	Blinking	Error when booting
			On	Communication on the PCI bus has not yet been started
	ERR/RUN	Green/red	Off	Module executes a reset
			Green on Red blinking with double pulse	CANopen communication disrupted. This may be due to one of the following reasons: • The CAN bus cable is broken or the CAN bus controller is in "Bus off" mode • The module is in PREOPERATIONAL mode • At least one configured CANopen slave is not functioning
			Green on Red blinking	Communication was stopped (the module is in STOPPED mode)
		Green	Blinking	Communication is being started (module is being initialized)
			On	Communication is ready
	TxD	Yellow	Flickering or on	Module sending data via the CANopen interface
	TERM	Yellow	On	Terminating resistor integrated in the module switched on

4.23.4.6 Operating and connection elements

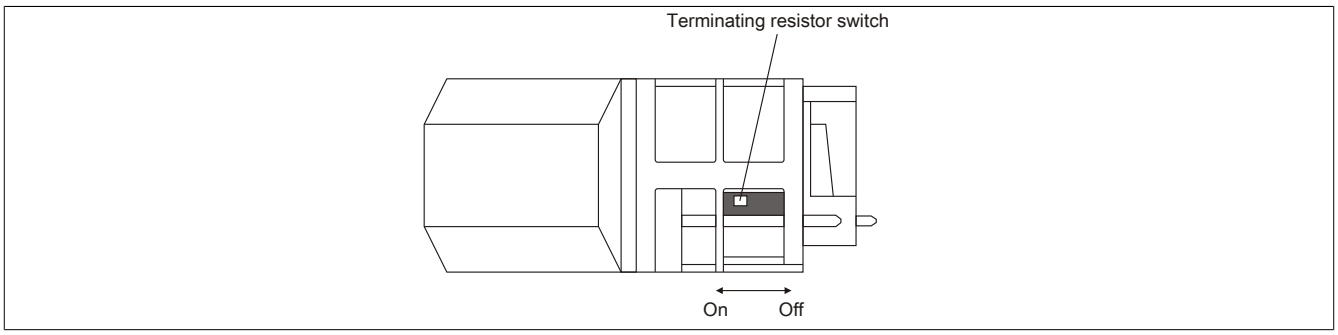


4.23.4.7 CAN bus interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	Terminal	Function	
	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	

4.23.4.8 Terminating resistor



A terminating resistor is integrated in the interface module. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.23.4.9 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.4.9.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.4.10 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.5 X20IF1043-1

4.23.5.1 General information

The interface module is equipped with a CANopen slave interface. It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

- CANopen slave
- Integrated terminating resistor

4.23.5.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1043-1	X20 interface module, for DTM configuration, 1 CANopen slave interface, electrically isolated, order 1x TB2105 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	

Table 464: X20IF1043-1 - Order data

4.23.5.3 Technical data

Product ID	X20IF1043-1
Short description	
Communication module	CANopen slave
General information	
B&R ID code	0xA70B
Status indicators	Module status, network status, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED and software
Network status	Yes, using status LED and software
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	CANopen slave
Design	5-pin male multipoint connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Terminating resistor	Integrated in the module
Controller	netX100
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB2105 terminal block separately
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller

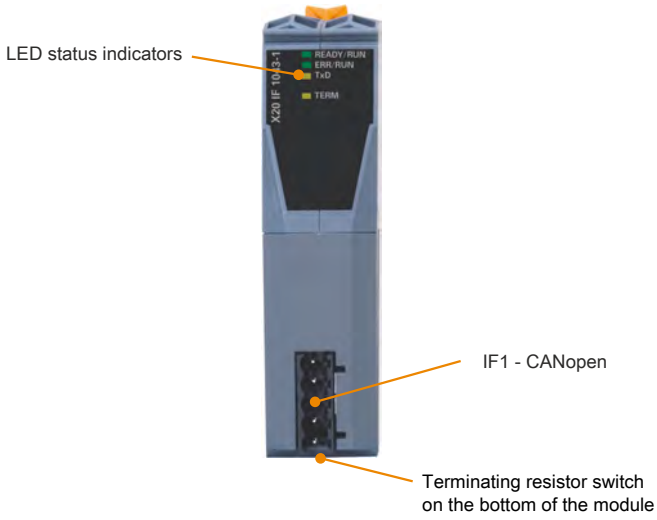
Table 465: X20IF1043-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.5.4 LED status indicators

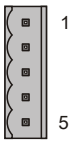
Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	Blinking	Error when booting
			On	Communication on the PCI bus has not yet been started
	ERR/RUN	Green/red	Off	Module executes a reset
			Green blinking with double pulse Red blinking with double pulse	CANopen communication disrupted. This may be due to one of the following reasons: • The CAN bus cable is broken or the CAN bus controller is in "Bus off" mode • The module is in PREOPERATIONAL mode • CANopen communication was stopped (the module is in STOPPED mode)
			Green blinking Red blinking with double pulse	CANopen communication was stopped by the master
		Green	Blinking	Communication is being started (module is being initialized)
			On	Communication is ready
	TxD	Yellow	Flickering or on	Module sending data via the CANopen interface
	TERM	Yellow	On	Terminating resistor integrated in the module switched on

4.23.5.5 Operating and connection elements

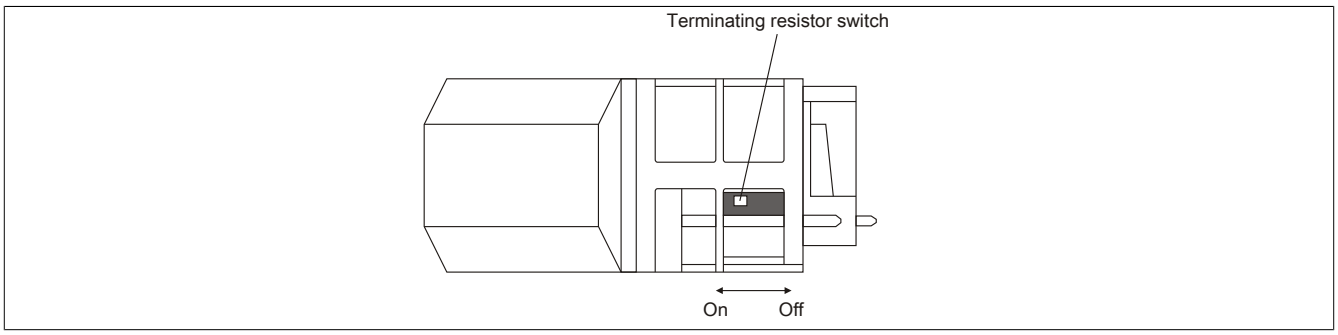


4.23.5.6 CAN bus interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	Terminal	Function	
	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	

4.23.5.7 Terminating resistor



A terminating resistor is integrated in the interface module. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.23.5.8 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.5.8.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.5.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.6 X20IF1051-1

4.23.6.1 General information

The interface module is equipped with a DeviceNet scanner interface. It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

- DeviceNet Scanner
- Integrated terminating resistor

4.23.6.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1051-1	X20 interface module, for DTM configuration, 1 DeviceNet scanner (master) interface, electrically isolated, order 1x TB2105 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	

Table 466: X20IF1051-1 - Order data

4.23.6.3 Technical data

Product ID	X20IF1051-1
Short description	
Communication module	DeviceNet scanner (master)
General information	
B&R ID code	0xA70C
Status indicators	Module status, network status, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED and software
Network status	Yes, using status LED and software
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	DeviceNet scanner (master)
Design	5-pin male multipoint connector
Max. distance	500 m
Transfer rate	Max. 500 kbit/s
Terminating resistor	Integrated in the module
Controller	netX100
Memory	8 MB SDRAM
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB2105 terminal block separately
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller

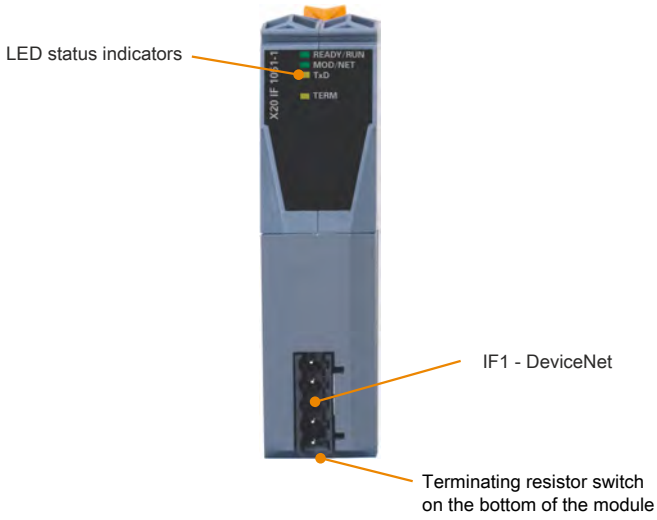
Table 467: X20IF1051-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.6.4 LED status indicators

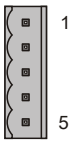
Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	On	Communication on the PCI bus has not yet been started
	MOD/NET	Green/red	Off	Module supply not connected or module is not online
		Green	Blinking	Module is online but the I/O connection is not active
			On	Module is online and the I/O connection is active ("operating")
		Red	Blinking	The red LED blinks if at least one of the following errors has occurred: • Minor fault (recoverable fault) • Connection error • No DeviceNet supply voltage
			On	Critical fault or critical connection error (double MAC ID, bus failure or module defect)
	TxD	Yellow	Flickering or on	Module sending data via the DeviceNet interface
	TERM	Yellow	On	Terminating resistor integrated in the module switched on

4.23.6.5 Operating and connection elements



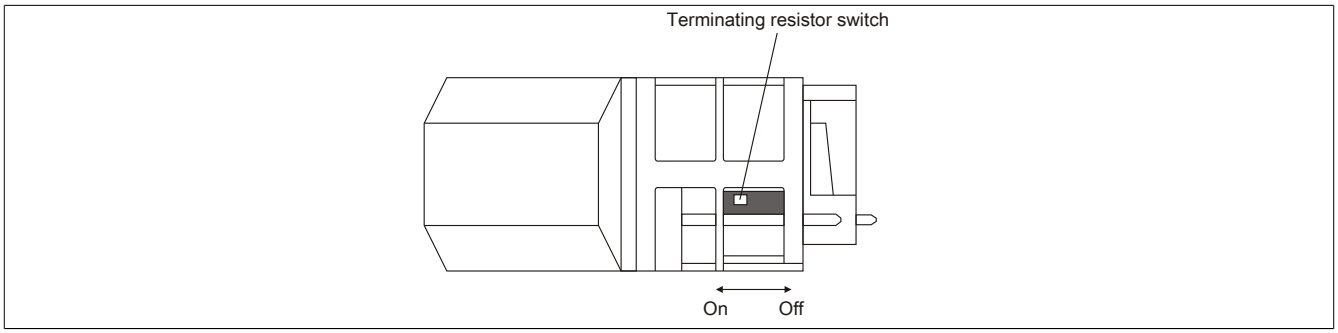
4.23.6.6 DeviceNet interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	Terminal	DeviceNet	
	1	CAN⊥ (V-)	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	V+	Supply voltage[1)]

1) The 24 VDC in the DeviceNet network must be fed in externally in order to guarantee correct operation and data exchange. 24 VDC is not made available by the device.

4.23.6.7 Terminating resistor



A terminating resistor is integrated in the interface module. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.23.6.8 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.6.8.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.6.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.7 X20IF1053-1

4.23.7.1 General information

The interface module is equipped with a DeviceNet slave (adapter) interface. It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

- DeviceNet slave (adapter)
- Integrated terminating resistor

4.23.7.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1053-1	X20 interface module, for DTM configuration, 1 DeviceNet adapter (slave) interface, electrically isolated, order 1x TB2105 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	

Table 468: X20IF1053-1 - Order data

4.23.7.3 Technical data

Product ID	X20IF1053-1
Short description	
Communication module	DeviceNet adapter (slave)
General information	
B&R ID code	0xA715
Status indicators	Module status, network status, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED and software
Network status	Yes, using status LED and software
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	DeviceNet adapter (slave)
Design	5-pin male multipoint connector
Max. distance	500 m
Transfer rate	Max. 500 kbit/s
Terminating resistor	Integrated in the module
Controller	netX100
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB2105 terminal block separately
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller

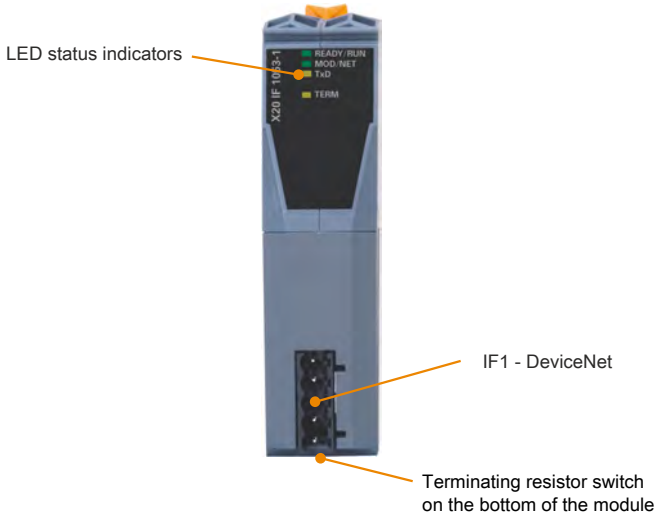
Table 469: X20IF1053-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.7.4 LED status indicators

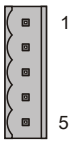
Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	On	Communication on the PCI bus has not yet been started
	MOD/NET	Green/red	Off	Module supply not connected or module is not online
		Green	Blinking	Module is online but the I/O connection is not active
			On	Module is online and the I/O connection is active ("operating")
		Red	Blinking	The red LED blinks if at least one of the following errors has occurred: • Minor fault (recoverable fault) • Connection error • No DeviceNet supply voltage
			On	Critical fault or critical connection error (double MAC ID, bus failure or module defect)
	TxD	Yellow	Flickering or on	Module sending data via the DeviceNet interface
	TERM	Yellow	On	Terminating resistor integrated in the module switched on

4.23.7.5 Operating and connection elements



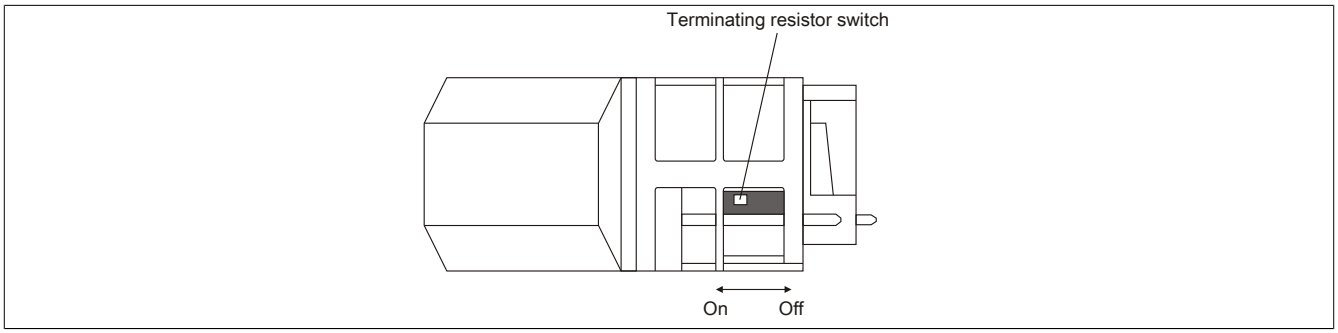
4.23.7.6 DeviceNet interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	Terminal	DeviceNet	
	1	CAN⊥ (V-)	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	V+	Supply voltage[1)]

1) The 24 VDC in the DeviceNet network must be fed in externally in order to guarantee correct operation and data exchange. 24 VDC is not made available by the device.

4.23.7.7 Terminating resistor



A terminating resistor is integrated in the interface module. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.23.7.8 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.7.8.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.7.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.8 X20IF1061

4.23.8.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with a PROFIBUS DP V1 master interface.

- PROFIBUS DP V1 master

4.23.8.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1061	X20 interface module, 1 PROFIBUS DP V0/V1 master interface, max. 12 Mbit/s, max. 3.5 kB input data and max. 3.5 kB output data, electrically isolated	
	Optional accessories	
	Infrastructure components	
0G1000.00-090	Bus connector, RS485, for PROFIBUS networks	

Table 470: X20IF1061 - Order data

4.23.8.3 Technical data

Product ID	X20IF1061
Short description	
Communication module	PROFIBUS DP V0/V1 master
General information	
B&R ID code	0x1F22
Status indicators	Module status, bus status
Diagnostics	
Module status	Yes, using status LED and software
Bus status	Yes, using status LED and software
Power consumption	1.4 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	PROFIBUS DP V0/V1 master
Design	9-pin female DSUB connector
Max. distance	1200 m
Transfer rate	Max. 12 Mbit/s
Terminating resistor	External T-connector (0G1000.00-090)
Controller	EC1
Memory	8 MB SDRAM
Cyclic data	
Input data	3.5 kB
Output data	3.5 kB
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In X20 CPU

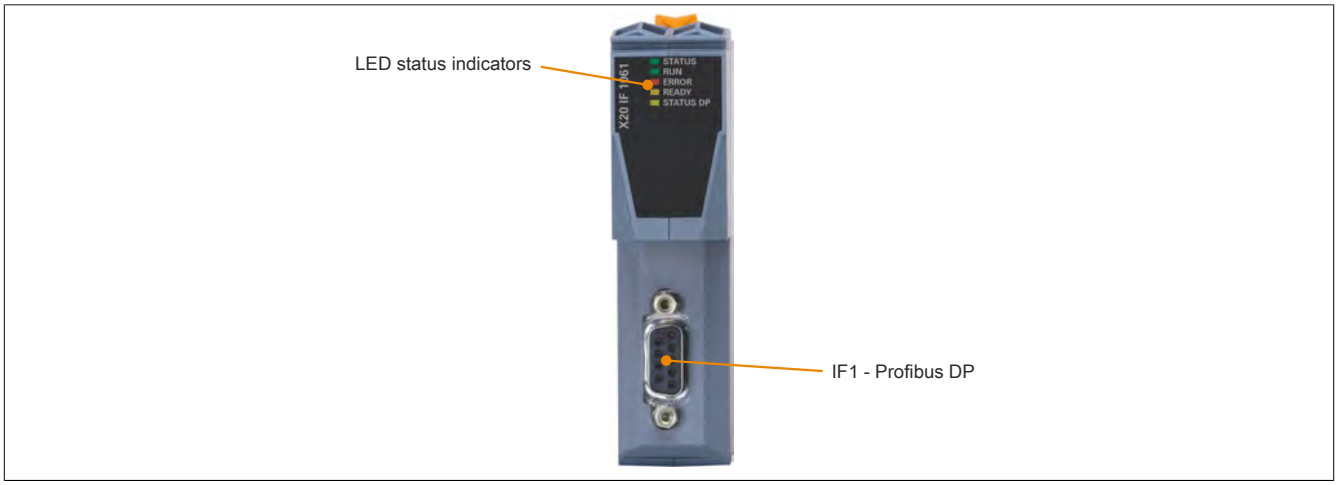
Table 471: X20IF1061 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

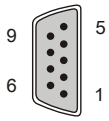
4.23.8.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	RUN	Green	On	Communication running
			Cyclic blinking	Communication stopped
			Irregular blinking	Missing or faulty configuration
			Off	No communication
	ERROR	Red	On	PROFIBUS error
			Off	No error
	READY	Yellow	On	Module ready
			Cyclic blinking	Bootstrap loader active
			Irregular blinking	Hardware or system error
			Off	Hardware defect
	STATUS DP	Yellow	On	Sending data or token
			Off	No token

4.23.8.5 Operating and connection elements



4.23.8.6 PROFIBUS DP interface

Interface	Pinout		
	Pin	RS485	
 9-pin female DSUB connector	1	Reserved	
	2	Reserved	
	3	RxD/TxD-P	Data[1]
	4	CNTR-P	Transmit enable
	5	DGND	Electrically isolated supply
	6	CP	Electrically isolated supply
	7	Reserved	
	8	RxD/TxD-N	Data\[2]
	9	CNTR-N	Transmit enable\
	CNTR ... Directional switch for external repeater		

1) Cable color: Red
2) Cable color: Green

4.23.8.7 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.9 X20(c)IF1061-1

4.23.9.1 General information

The interface module functions as a DP V1 master. It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

- PROFIBUS DP V1 master

4.23.9.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.9.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1061-1	X20 interface module for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated	
X20cIF1061-1	X20 interface module coated, for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated	
	Optional accessories	
	Infrastructure components	
0G1000.00-090	Bus connector, RS485, for PROFIBUS networks	

Table 472: X20IF1061-1, X20cIF1061-1 - Order data

4.23.9.4 Technical data

Product ID	X20IF1061-1	X20cIF1061-1
Short description		
Communication module	1x PROFIBUS DP V0/V1 master	
General information		
B&R ID code	0xA716	0xE234
Status indicators	Module status, data transfer	
Diagnostics		
Module status	Yes, using status LED and software	
Network status	Yes, using status LED and software	
Data transfer	Yes, using status LED	
Power consumption	1.8 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - IF1	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Interfaces		
IF1 interface		
Fieldbus	PROFIBUS DP V0/V1 master	
Design	9-pin female DSUB connector	
Max. distance	1200 m	
Transfer rate	Max. 12 Mbit/s	
Controller	netX100	
Memory	8 MB SDRAM	
Cyclic data		
Input data	Max. 3.5 kB	
Output data	Max. 3.5 kB	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller	In the X20c CPU and in the X20cBC1083 expandable bus controller

Table 473: X20IF1061-1, X20cIF1061-1 - Technical data

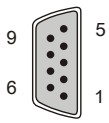
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.9.5 LED status indicators

Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	Blinking	Boot error
			On	Communication on the PCI bus has not yet been started
	STATUS DP	Green	Acyclic blinking	No configuration or stack error
			Cyclic blinking	Bus is configured, but communication has not yet been enabled by the application
			On	Communication established with all slaves
		Red	Cyclic blinking	Communication to at least one slave has been disrupted
			On	Communication to one/all slave(s) has been disrupted
	RxD	Yellow	On	The module is receiving data via the PROFIBUS DP master interface
	TxD	Yellow	On	The module is transmitting data via the PROFIBUS DP master interface

4.23.9.6 Operating and connection elements

4.23.9.7 PROFIBUS DP interface

Interface	Pinout		
	Pin	RS485	
 9-pin female DSUB connector	1	Reserved	
	2	Reserved	
	3	RxD/TxD-P	Data[1]
	4	CNTR-P	Transmit enable
	5	DGND	Electrically isolated supply
	6	CP	Electrically isolated supply
	7	Reserved	
	8	RxD/TxD-N	Data\[2]
	9	CNTR-N	Transmit enable\
	CNTR ... Directional switch for external repeater		

1) Cable color: Red
2) Cable color: Green

4.23.9.8 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.9.8.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.9.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.9.10 Minimum DTM version for coated modules

Information:

The minimum DTM version required by coated modules is 1.0370.140220.12186. This version is included beginning with Automation Studio upgrade packs V4.0.18.x and V3.0.90.29.

4.23.10 X20IF1063

4.23.10.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with a PROFIBUS DP V0 slave interface.

- PROFIBUS DP V0 slave connection

4.23.10.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1063	X20 interface module, 1 PROFIBUS DP V0 slave interface, max. 12 Mbit/s, electrically isolated	
	Optional accessories	
	Infrastructure components	
0G1000.00-090	Bus connector, RS485, for PROFIBUS networks	

Table 474: X20IF1063 - Order data

4.23.10.3 Technical data

Product ID	X20IF1063
Short description	
Communication module	1x PROFIBUS DP V0 slave
General information	
B&R ID code	0x1F23
Status indicators	Module status, data transfer
Diagnostics	
Module status	Yes, using status LED
Data transfer	Yes, using status LED
Power consumption	0.87 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	PROFIBUS DP V0 slave
Design	9-pin female DSUB connector
Max. distance	1200 m
Transfer rate	Max. 12 Mbit/s
Terminating resistor	External T-connector (0G1000.00-090)
Controller	VPC3+C
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In X20 CPU

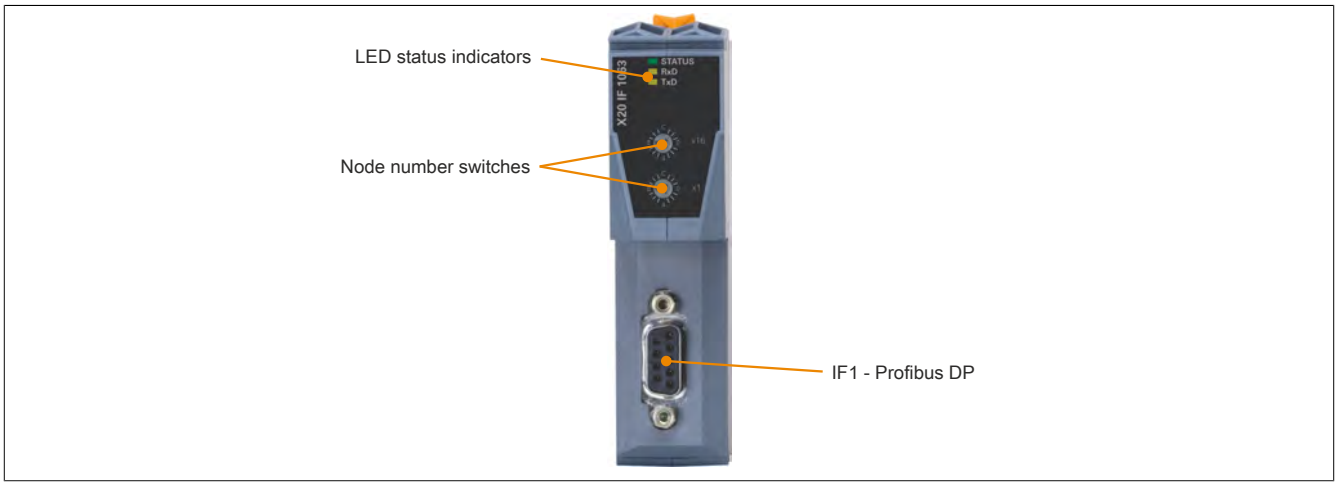
Table 475: X20IF1063 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.10.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	RxD	Yellow	On	The module receives data via the PROFIBUS DP slave interface
	TxD	Yellow	On	The module sends data via the PROFIBUS DP slave interface

4.23.10.5 Operating and connection elements

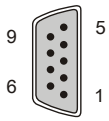


4.23.10.6 Node number switch

The node number for the interface is set with the two hex switches.

4.23.10.7 PROFIBUS DP interface

Interface	Pinout		
	Pin	RS485	
	1	Reserved	
	2	Reserved	
	3	RxD/TxD-P	Data[1]
	4	CNTR-P	Transmit enable
	5	DGND	Electrically isolated supply
	6	CP	Electrically isolated supply
	7	Reserved	
	8	RxD/TxD-N	Data\[2]
	9	CNTR-N	Transmit enable\
	CNTR ... Directional switch for external repeater		



9-pin female DSUB connector

1) Cable color: Red
2) Cable color: Green

4.23.10.8 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.11 X20(c)IF1063-1

4.23.11.1 General information

The interface module functions as a DP V1 slave. It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

- PROFIBUS DP V1 slave

4.23.11.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.11.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1063-1	X20 interface module, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated	
X20cIF1063-1	X20 interface module, coated, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated	
	Optional accessories	
	Infrastructure components	
0G1000.00-090	Bus connector, RS485, for PROFIBUS networks	

Table 476: X20IF1063-1, X20cIF1063-1 - Order data

4.23.11.4 Technical data

Product ID	X20IF1063-1	X20cIF1063-1
Short description		
Communication module	1x PROFIBUS DP V0/V1 slave	
General information		
B&R ID code	0xA717	0xE235
Status indicators	Module status, data transfer	
Diagnostics		
Module status	Yes, using status LED and software	
Network status	Yes, using status LED and software	
Data transfer	Yes, using status LED	
Power consumption	1.8 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - IF1	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Interfaces		
IF1 interface		
Fieldbus	PROFIBUS DP V0/V1 slave	
Design	9-pin female DSUB connector	
Max. distance	1200 m	
Transfer rate	Max. 12 Mbit/s	
Controller	netX100	
Cyclic data		
Input data	Max. 244 bytes	
Output data	Max. 244 bytes	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller	In the X20c CPU and in the X20cBC1083 expandable bus controller

Table 477: X20IF1063-1, X20cIF1063-1 - Technical data

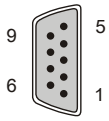
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.11.5 LED status indicators

Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	Blinking	Boot error
			On	Communication on the PCI bus has not yet been started
	STATUS DP	Green	On	RUN, cyclic communication
		Red	On	Faulty configuration (e.g. master configuration and interface card configuration do not match)
			Cyclic flash	STOP, no communication, connection error
			Acyclic flash	Slave not configured
	RxD	Yellow	On	The module receives data via the PROFIBUS DP slave interface
	TxD	Yellow	On	The module sends data via the PROFIBUS DP slave interface

4.23.11.6 Operating and connection elements

4.23.11.7 PROFIBUS DP interface

Interface	Pinout		
	Pin	RS485	
 9-pin female DSUB connector	1	Reserved	
	2	Reserved	
	3	RxD/TxD-P	Data[1]
	4	CNTR-P	Transmit enable
	5	DGND	Electrically isolated supply
	6	CP	Electrically isolated supply
	7	Reserved	
	8	RxD/TxD-N	Data\[2]
	9	CNTR-N	Transmit enable\
	CNTR ... Directional switch for external repeater		

1) Cable color: Red
2) Cable color: Green

4.23.11.8 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.11.8.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.11.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.11.10 Minimum DTM version for coated modules

Information:

The minimum DTM version required by coated modules is 1.0370.140220.12186. This version is included beginning with Automation Studio upgrade packs V4.0.18.x and V3.0.90.29.

4.23.12 X20IF1065

4.23.12.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with a PROFIBUS DP V1 slave interface.

- PROFIBUS DP V1 slave connection

4.23.12.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1065	X20 interface module, 1 PROFIBUS DP V1 slave interface, max. 12 Mbit/s, electrically isolated	
	Optional accessories	
	Infrastructure components	
0G1000.00-090	Bus connector, RS485, for PROFIBUS networks	

Table 478: X20IF1065 - Order data

4.23.12.3 Technical data

Product ID	X20IF1065
Short description	
Communication module	1x PROFIBUS DP V0/V1 slave
General information	
B&R ID code	0xA4C6
Status indicators	Module status, bus status
Diagnostics	
Module status	Yes, using status LED and software
Bus status	Yes, using status LED and software
Power consumption	1.4 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	PROFIBUS DP V0/V1 slave
Design	9-pin female DSUB connector
Max. distance	1200 m
Transfer rate	Max. 12 Mbit/s
Terminating resistor	External T-connector (0G1000.00-090)
Controller	EC1
Memory	8 kB SDRAM
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In X20 CPU

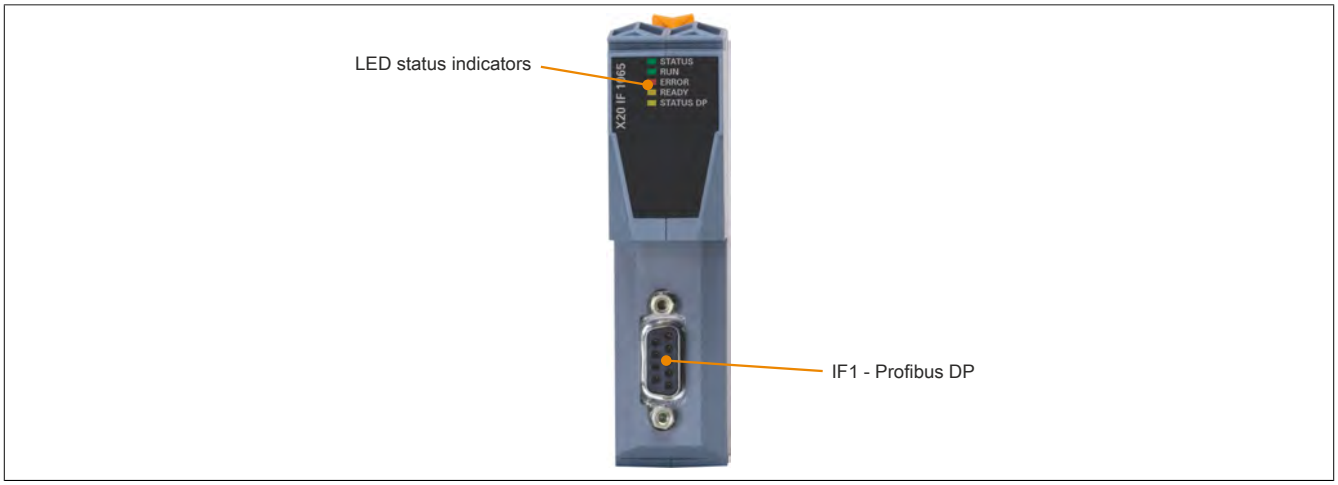
Table 479: X20IF1065 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

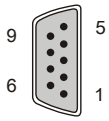
4.23.12.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	RUN	Green	On	Communication running
			Cyclic blinking	Communication stopped
			Irregular blinking	Missing or faulty configuration
			Off	No communication
	ERROR	Red	On	PROFIBUS error
			Off	No error
	READY	Yellow	On	Module ready
			Cyclic blinking	Bootstrap loader active
			Irregular blinking	Hardware or system error
			Off	Hardware defect
	STATUS DP	Yellow	On	Sending data or token
			Off	No token

4.23.12.5 Operating and connection elements



4.23.12.6 PROFIBUS DP interface

Interface	Pinout		
	Pin	RS485	
 9-pin female DSUB connector	1	Reserved	
	2	Reserved	
	3	RxD/TxD-P	Data[1]
	4	CNTR-P	Transmit enable
	5	DGND	Electrically isolated supply
	6	CP	Electrically isolated supply
	7	Reserved	
	8	RxD/TxD-N	Data\[2]
	9	CNTR-N	Transmit enable\
	CNTR ... Directional switch for external repeater		

1) Cable color: Red
2) Cable color: Green

4.23.12.7 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.13 X20(c)IF1072

4.23.13.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with a CAN bus interface.

- CAN bus connection
- Integrated terminating resistor

4.23.13.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.13.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1072	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately	
X20cIF1072	X20 interface module, coated, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	

Table 480: X20IF1072, X20cIF1072 - Order data

4.23.13.4 Technical data

Product ID	X20IF1072	X20cIF1072
Short description		
Communication module	1x CAN bus	
General information		
B&R ID code	0x1F20	0xE506
Status indicators	Module status, data transfer, terminating resistor	
Diagnostics		
Module status	Yes, using status LED	
Data transfer	Yes, using status LED	
Terminating resistor	Yes, using status LED	
Power consumption	0.79 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - IF1	Yes	
Certification		
CE	Yes	
cULus	Yes	-
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	-
KC	Yes	-
GL	Yes	-
LR	Yes	-
GOST-R	Yes	
Interfaces		
IF1 interface		
Signal	CAN bus [2]	
Design	5-pin male multipoint connector	
Max. distance	1000 m	
Transfer rate	Max. 1 Mbit/s	
Terminating resistor	Integrated in the module	
Controller	SJA 1000	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x TB2105 terminal block separately	
Slot	In X20 CPU	

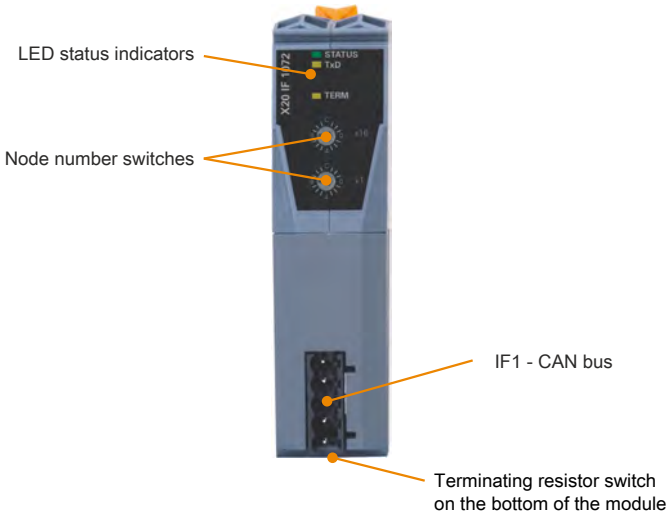
Table 481: X20IF1072, X20cIF1072 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) This CAN bus interface can be configured as a CANopen master in Automation Studio 3.0 and higher.

4.23.13.5 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	TxD	Yellow	On	The module is sending data via the CAN bus interface
	TERM	Yellow	On	Terminating resistor integrated in the module switched on

4.23.13.6 Operating and connection elements

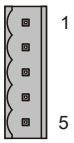


4.23.13.7 Node number switch

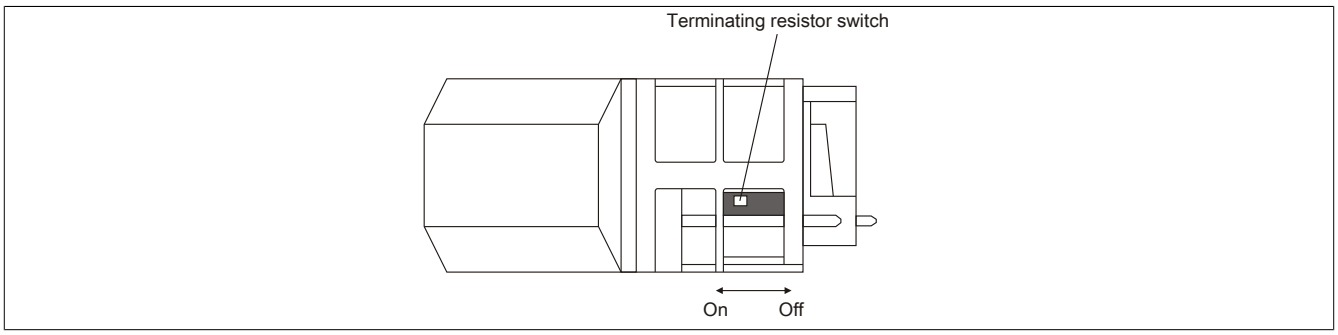
The node number for the interface is set with the two hex switches.

4.23.13.8 CAN bus interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	**Terminal**	**Function**	
	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	

4.23.13.9 Terminating resistor



A terminating resistor is integrated in the interface module. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.23.13.10 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.14 X20IF1082

4.23.14.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with an POWERLINK interface.

The interface has two RJ45 sockets. Both connections lead to an integrated hub. This makes it easy to create daisy-chain connections using POWERLINK.

- POWERLINK V1/V2 for real-time Ethernet communication
- Integrated hub for efficient cabling
- Configurable ring redundancy

4.23.14.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1082	X20 interface module, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function	

Table 482: X20IF1082 - Order data

Optional accessories

Model number	Short description
X20CA0E61.xxxxx	POWERLINK connection cable RJ45 to RJ45, 0.2 to 20 m
X20CA0E61.0500	POWERLINK connection cable RJ45 to RJ45, 50 m

4.23.14.3 Technical data

Product ID	X20IF1082
Short description	
Communication module	1x POWERLINK (V1/V2) managing or controlled node
General information	
B&R ID code	0x1F1F
Status indicators	Module status, bus function
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED and software
Power consumption	2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - X1	Yes
PLC - X2	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
Fieldbus	POWERLINK (V1/V2) managing or controlled node
Type	Type 3 2)
Design	2x shielded RJ45 (hub)
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100BASE-TX
Half-duplex	Yes
Full-duplex	No
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Hub runtime	0.96 to 1 µs
Controller	POWERLINK MAC
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In X20 CPU

Table 483: X20IF1082 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) See the POWERLINK help system under "General information, Hardware - IF/LS".

4.23.14.4 LED status indicators

Figure	LED	Color	Status	Description
	S/E	Green/Red		Status/Error LED. The LED indicators are described in section 4.12.3.4.1 ""S/E" LED".
	L/A IFx	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus

4.23.14.4.1 "S/E" LED

The Status/Error LED is a green/red dual LED. The LED status can have different meanings depending on the operating mode.

4.23.14.4.1.1 Ethernet mode

In this mode, the interface is operated as an Ethernet interface.

Green - Status	Description
On	Interface being operated as an Ethernet interface

Table 484: Status/Error LED - Ethernet operating mode

4.23.14.4.1.2 POWERLINK V1

Status LED		Status of the POWERLINK node
Green	Red	
On	Off	The POWERLINK node is running with no errors.
Off	On	A system error has occurred. The error type can be read using the PLC logbook. An irreparable problem has occurred. The system cannot properly carry out its tasks. This state can only be changed by resetting the module.
Blinking alternately		The POWERLINK managing node has failed. This error code can only occur when operated as a controlled node. This means that the configured node number lies within the range 0x01 - 0xFD.
Off	Blinking	System failure. The red blinking LED signals an error code (see section 4.12.2.4.2 "System failure error codes").
Off	Off	Module is: • Off • Starting up • Not configured correctly in Automation Studio • Defective

Table 485: Status/Error LED - POWERLINK V1 operating mode

4.23.14.4.1.3 POWERLINK

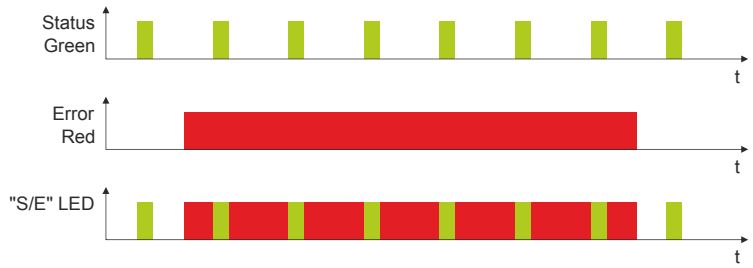
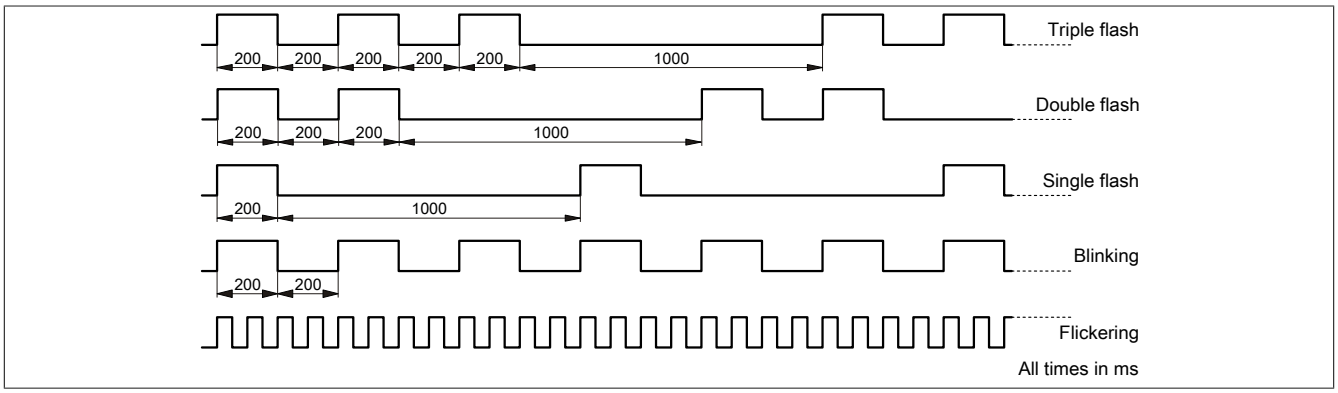
Red - Error	Description
On	The module is in an error mode (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: The LED blinks red several times immediately after startup. This is not an error.

Table 486: Status/Error LED as Error LED - POWERLINK operating mode

Green - Status	Description
Off	**Mode** The module is in NOT_ACTIVE mode or: • Switched off • Starting up • Not configured correctly in Automation Studio • Defective **Managing node (MN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to PRE_OPERATIONAL_1 mode. If POWERLINK communication is detected before the time expires, however, then the MN will not be started. **Controlled node (CN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to BASIC_ETHERNET mode. If POWERLINK communication is detected before this time expires, however, the module switches immediately to PRE_OPERATIONAL_1 mode.
Green flickering (approx. 10 Hz)	**Mode** The module is in BASIC_ETHERNET mode. The interface is being operated as an Ethernet TCP/IP interface. **Managing node (MN)** This state can only be changed by resetting the module. **Controlled node (CN)** If POWERLINK communication is detected while in this state, the module will transition to the PRE_OPERATIONAL_1 state.
Single flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_1 mode. **Managing node (MN)** The MN starts "reduced cycle" operation. Cyclic communication is not yet taking place. **Controlled node (CN)** The module can be configured by the MN in this state. The CN waits until it receives an SoC frame and then switches to the PRE_OPERATIONAL_2 mode. An LED lit red in this state indicates failure of the MN.
Double flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_2 mode. **Managing node (MN)** The MN begins cyclic communication (cyclic input data is not yet being evaluated). The CNs are configured in this state. **Controlled node (CN)** The module can be configured by the MN in this state. A command then switches the module to READY_TO_OPERATE mode. An LED lit red in this mode indicates failure of the MN.
Triple flash (approx. 1 Hz)	**Mode** The module is in the READY_TO_OPERATE state. **Managing node (MN)** Cyclic and asynchronous communication is taking place. Any received PDO data is ignored. **Controlled node (CN)** The configuration of the module is completed. Normal cyclic and asynchronous communication is taking place. The PDO data sent corresponds to the PDO mapping. Cyclic data is not yet being evaluated, however. An LED lit red in this mode indicates failure of the MN.
On	**Mode** The module is in PRE_OPERATIONAL_2 mode. PDO mapping is active and cyclic data is being evaluated.
Blinking (approx. 2.5 Hz)	**Mode** The module is in STOPPED mode. **Managing node (MN)** This status is not possible for the MN. **Controlled node (CN)** No output data is produced or input data supplied. It is only possible to enter or leave this mode after the MN has given the appropriate command.

Table 487: Status/Error LED as Status LED - POWERLINK operating mode

Status LEDs - Blinking patterns



4.23.14.4.1.4 System failure error codes

Incorrect configuration or defective hardware can cause a system stop error.

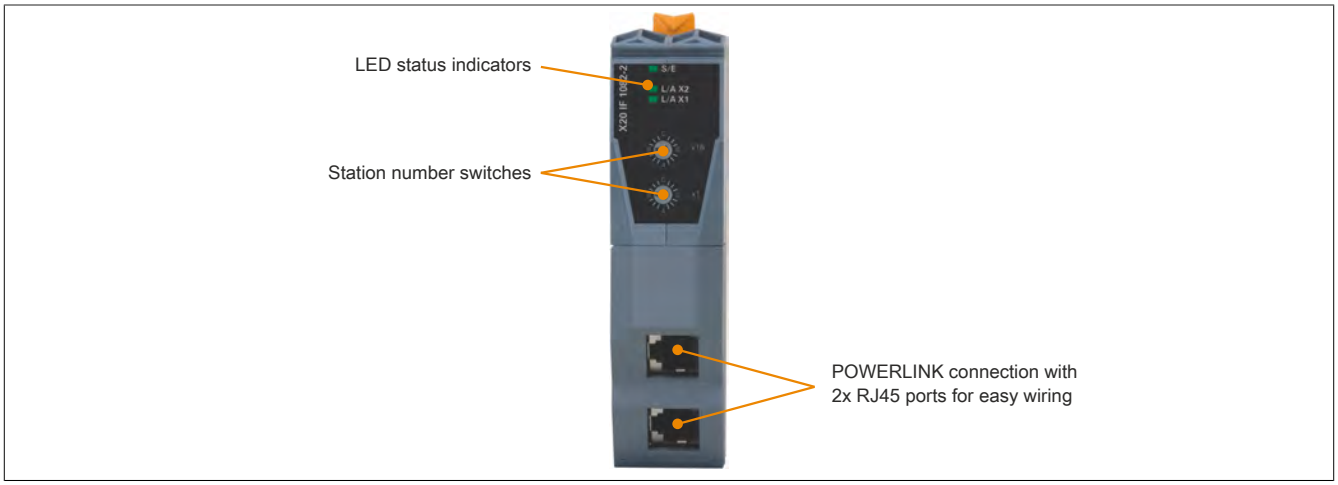
The error code is indicated by the red Error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. The error code is output cyclically every 2 seconds.

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	•	•	•	-	Pause	•	•	•	-	Pause
Hardware error: The module or a system component is defective and must be replaced.	-	•	•	-	Pause	-	•	•	-	Pause

Table 488: Status/Error ("S/E") LED - System failure error codes

Key:
- • ... 150 ms
- - ... 600 ms
- Pause ... 2 second delay

4.23.14.5 Operating and connection elements



4.23.14.6 POWERLINK node number

The node number for the POWERLINK station is set using the two number switches. The node number can also be directly configured using Automation Studio.

4.23.14.6.1 POWERLINK V1

Switch position	Description
0x00	Operation as managing node.
0x01 - 0xFD	Node number of the POWERLINK node. Operation as controlled node.
0xFE - 0xFF	Reserved, switch position not permitted

Table 489: POWERLINK V1 - Node numbers

4.23.14.6.2 POWERLINK

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node.
0xF0	Operation as a managing node.
0xF1 - 0xFF	Reserved, switch position not permitted

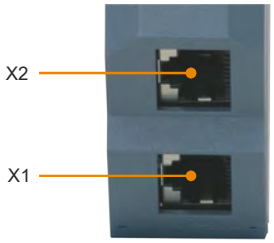
Table 490: POWERLINK node number

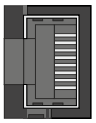
4.23.14.6.3 Ethernet mode

In this mode, the interface is operated as an Ethernet interface. The INA2000 station number can be set using the B&R Automation Studio software.

4.23.14.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.23.14.8 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.15 X20(c)IF1082-2

4.23.15.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with an POWERLINK interface.

The interface has two RJ45 sockets. Both connections lead to an integrated hub. This makes it easy to create daisy-chain connections using POWERLINK.

- POWERLINK for real-time Ethernet communication
- Integrated hub for efficient cabling
- Configurable ring redundancy
- Poll response chaining
- Dynamic Node Allocation (DNA)

4.23.15.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.15.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1082-2	X20 interface module, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function PRC function	
X20cIF1082-2	X20 interface module, coated, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function PRC function	

Table 491: X20IF1082-2, X20cIF1082-2 - Order data

Optional accessories

Model number	Short description
X20CA0E61.xxxxx	POWERLINK connection cable RJ45 to RJ45, 0.2 to 20 m
X20CA0E61.0500	POWERLINK connection cable RJ45 to RJ45, 50 m

4.23.15.4 Technical data

Product ID	X20IF1082-2	X20cIF1082-2
Short description		
Communication module	1x POWERLINK (V1/V2) managing or controlled node	
General information		
B&R ID code	0xA7A3	0xE236
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Power consumption	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - X1	Yes	
PLC - X2	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 1)	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Fieldbus	POWERLINK (V1/V2) managing or controlled node	
Type	Type 4 2)	
Design	2x shielded RJ45 (hub)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Controller	POWERLINK MAC	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	In X20 CPU	In X20c CPU

Table 492: X20IF1082-2, X20cIF1082-2 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) See the POWERLINK help system under "General information, Hardware - IF/LS".

4.23.15.5 LED status indicators

Figure	LED	Color	Status	Description
	S/E	Green/Red		Status/Error LED. The LED indicators are described in section 4.12.3.4.1 ""S/E" LED".
	L/A X1/X2	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus

4.23.15.5.1 "S/E" LED

The Status/Error LED is a green/red dual LED. The LED status can have different meanings depending on the operating mode.

4.23.15.5.1.1 Ethernet mode

In this mode, the interface is operated as an Ethernet interface.

Green - Status	Description
On	Interface being operated as an Ethernet interface

Table 493: Status/Error LED - Ethernet operating mode

4.23.15.5.1.2 POWERLINK V1

Status LED		Status of the POWERLINK node
Green	Red	
On	Off	The POWERLINK node is running with no errors.
Off	On	A system error has occurred. The error type can be read using the PLC logbook. An irreparable problem has occurred. The system cannot properly carry out its tasks. This state can only be changed by resetting the module.
Blinking alternately		The POWERLINK managing node has failed. This error code can only occur when operated as a controlled node. This means that the configured node number lies within the range 0x01 - 0xFD.
Off	Blinking	System failure. The red blinking LED signals an error code (see section 4.12.2.4.2 "System failure error codes").
Off	Off	Module is: • Off • Starting up • Not configured correctly in Automation Studio • Defective

Table 494: Status/Error LED - POWERLINK V1 operating mode

4.23.15.5.1.3 POWERLINK

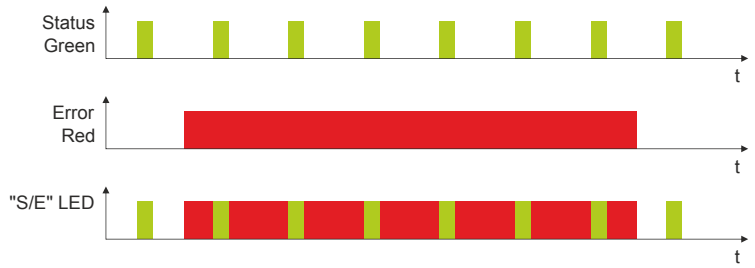
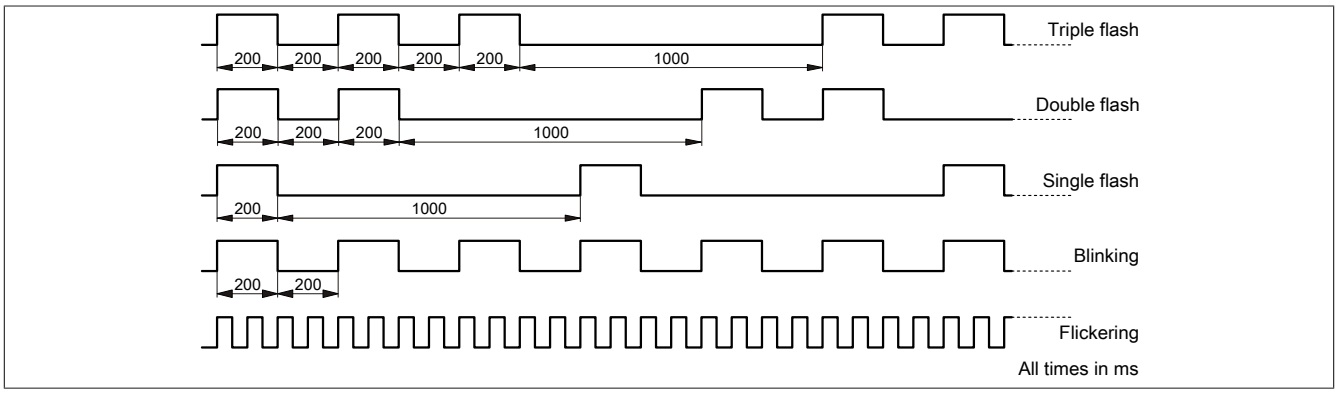
Red - Error	Description
On	The module is in an error mode (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: The LED blinks red several times immediately after startup. This is not an error.

Table 495: Status/Error LED as Error LED - POWERLINK operating mode

Green - Status	Description
Off	**Mode** The module is in NOT_ACTIVE mode or: • Switched off • Starting up • Not configured correctly in Automation Studio • Defective **Managing node (MN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to PRE_OPERATIONAL_1 mode. If POWERLINK communication is detected before the time expires, however, then the MN will not be started. **Controlled node (CN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to BASIC_ETHERNET mode. If POWERLINK communication is detected before this time expires, however, the module switches immediately to PRE_OPERATIONAL_1 mode.
Green flickering (approx. 10 Hz)	**Mode** The module is in BASIC_ETHERNET mode. The interface is being operated as an Ethernet TCP/IP interface. **Managing node (MN)** This state can only be changed by resetting the module. **Controlled node (CN)** If POWERLINK communication is detected while in this state, the module will transition to the PRE_OPERATIONAL_1 state.
Single flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_1 mode. **Managing node (MN)** The MN starts "reduced cycle" operation. Cyclic communication is not yet taking place. **Controlled node (CN)** The module can be configured by the MN in this state. The CN waits until it receives an SoC frame and then switches to the PRE_OPERATIONAL_2 mode. An LED lit red in this state indicates failure of the MN.
Double flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_2 mode. **Managing node (MN)** The MN begins cyclic communication (cyclic input data is not yet being evaluated). The CNs are configured in this state. **Controlled node (CN)** The module can be configured by the MN in this state. A command then switches the module to READY_TO_OPERATE mode. An LED lit red in this mode indicates failure of the MN.
Triple flash (approx. 1 Hz)	**Mode** The module is in the READY_TO_OPERATE state. **Managing node (MN)** Cyclic and asynchronous communication is taking place. Any received PDO data is ignored. **Controlled node (CN)** The configuration of the module is completed. Normal cyclic and asynchronous communication is taking place. The PDO data sent corresponds to the PDO mapping. Cyclic data is not yet being evaluated, however. An LED lit red in this mode indicates failure of the MN.
On	**Mode** The module is in PRE_OPERATIONAL_2 mode. PDO mapping is active and cyclic data is being evaluated.
Blinking (approx. 2.5 Hz)	**Mode** The module is in STOPPED mode. **Managing node (MN)** This status is not possible for the MN. **Controlled node (CN)** No output data is produced or input data supplied. It is only possible to enter or leave this mode after the MN has given the appropriate command.

Table 496: Status/Error LED as Status LED - POWERLINK operating mode

Status LEDs - Blinking patterns



4.23.15.5.1.4 System failure error codes

Incorrect configuration or defective hardware can cause a system stop error.

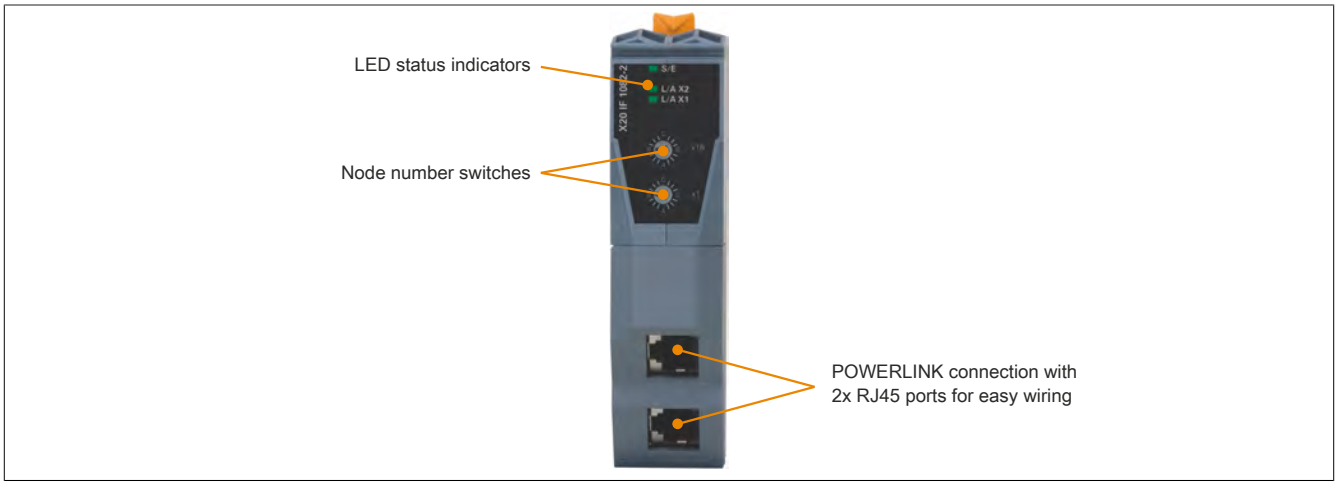
The error code is indicated by the red Error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. The error code is output cyclically every 2 seconds.

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	•	•	•	-	Pause	•	•	•	-	Pause
Hardware error: The module or a system component is defective and must be replaced.	-	•	•	-	Pause	-	•	•	-	Pause

Table 497: Status/Error ("S/E") LED - System failure error codes

Key:
- • ... 150 ms
- - ... 600 ms
- Pause ... 2 second delay

4.23.15.6 Operating and connection elements



4.23.15.7 POWERLINK node number

The node number for the POWERLINK station is set using the two number switches. The node number can also be directly configured using Automation Studio.

4.23.15.7.1 POWERLINK V1

Switch position	Description
0x00	Operation as managing node.
0x01 - 0xFD	Node number of the POWERLINK node. Operation as controlled node.
0xFE - 0xFF	Reserved, switch position not permitted

Table 498: POWERLINK V1 - Node numbers

4.23.15.7.2 POWERLINK

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node.
0xF0	Operation as a managing node.
0xF1 - 0xFF	Reserved, switch position not permitted

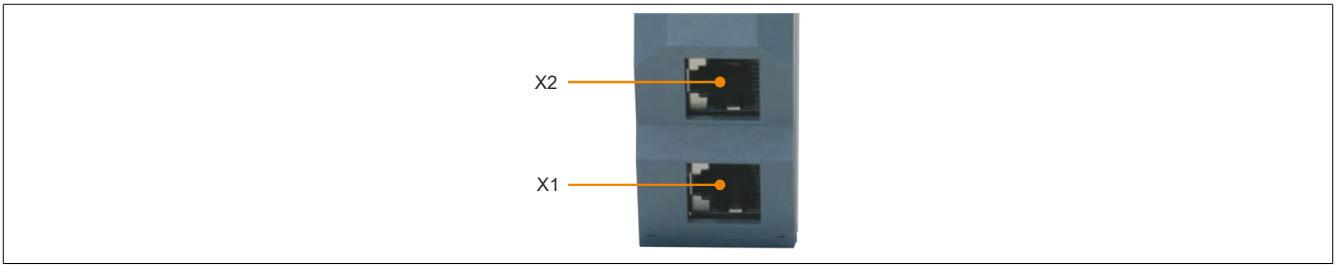
Table 499: POWERLINK node number

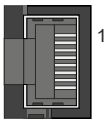
4.23.15.7.3 Ethernet mode

In this mode, the interface is operated as an Ethernet interface. The INA2000 station number can be set using the B&R Automation Studio software.

4.23.15.8 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.23.15.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.16 X20IF1086-2

4.23.16.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with an POWERLINK interface.

This interface uses a 100 Base-FX port. The POWERLINK connection is made using 62.5/125 µm or 50/125 µm fiber optic multimode cable with a duplex LC connection. The module and network status is indicated using LEDs.

- POWERLINK for real-time Ethernet communication
- 100 Base-FX port
- Poll response chaining
- Dynamic Node Allocation (DNA)

4.23.16.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1086-2	X20 interface module, 1 POWERLINK interface, managing or controlled node, PRC function, 1 fiber optic connection	

Table 500: X20IF1086-2 - Order data

4.23.16.3 Technical data

Product ID	X20IF1086-2
Short description	
Communication module	1x POWERLINK (V1/V2) managing or controlled node
General information	
B&R ID code	0xB455
Status indicators	Module status, bus function
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED and software
Power consumption	1.8 W (Rev. <D0: 2 W)
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - X1	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Fieldbus	POWERLINK (V1/V2) managing or controlled node
Type	Type 4 2)
Standard (compliance)	ANSI/IEEE 802.3
Design	1x duplex LC
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100 BASE-FX
Half-duplex	Yes
Full-duplex	POWERLINK mode: No / Ethernet mode: Yes
Autonegotiation	No
Auto-MDI / MDIX	No
Controller	POWERLINK MAC
Wave length	1300 nm
Cable fiber type	Multimode fiber with 62.5/125 µm or 50/125 µm core diameter LC connector on both sides
Optical power budget	
Optical fiber 62.5/125 µm, NA = 0.275	11 dB
Optical fiber 50/125 µm, NA = 0.200	7.5 dB
Cable length	
Ethernet TCP/IP	Max. 400 m between 2 stations (segment length)
POWERLINK	Max. 2 km between 2 stations (segment length)
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In X20 CPU

Table 501: X20IF1086-2 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) See the POWERLINK help system under "General information, Hardware - IF/LS".

4.23.16.4 LED status indicators

Figure	LED	Color	Status	Description
	S/E	Green/Red		Status/Error LED. The LED indicators are described in section 4.12.3.4.1 ""S/E" LED".
	L/A X1	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus

4.23.16.5 "S/E" LED

The Status/Error LED is a green/red dual LED. The LED status can have different meanings depending on the operating mode.

4.23.16.5.1 Ethernet mode

In this mode, the interface is operated as an Ethernet interface.

Green - Status	Description
On	Interface being operated as an Ethernet interface

Table 502: Status/Error LED - Ethernet operating mode

4.23.16.5.2 POWERLINK V1

Status LED		Status of the POWERLINK node
Green	Red	
On	Off	The POWERLINK node is running with no errors.
Off	On	A system error has occurred. The error type can be read using the PLC logbook. An irreparable problem has occurred. The system cannot properly carry out its tasks. This state can only be changed by resetting the module.
Blinking alternately		The POWERLINK managing node has failed. This error code can only occur when operated as a controlled node. This means that the configured node number lies within the range 0x01 - 0xFD.
Off	Blinking	System failure. The red blinking LED signals an error code (see section 4.12.2.4.2 "System failure error codes").
Off	Off	Module is: • Off • Starting up • Not configured correctly in Automation Studio • Defective

Table 503: Status/Error LED - POWERLINK V1 operating mode

4.23.16.5.3 POWERLINK

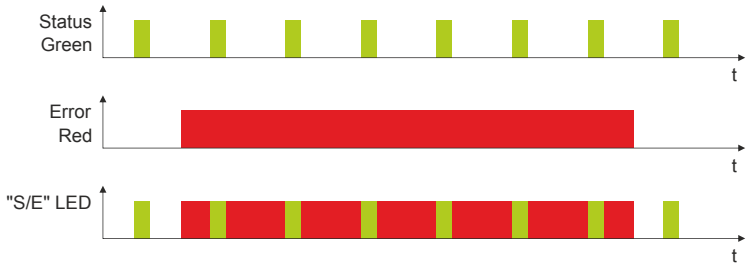
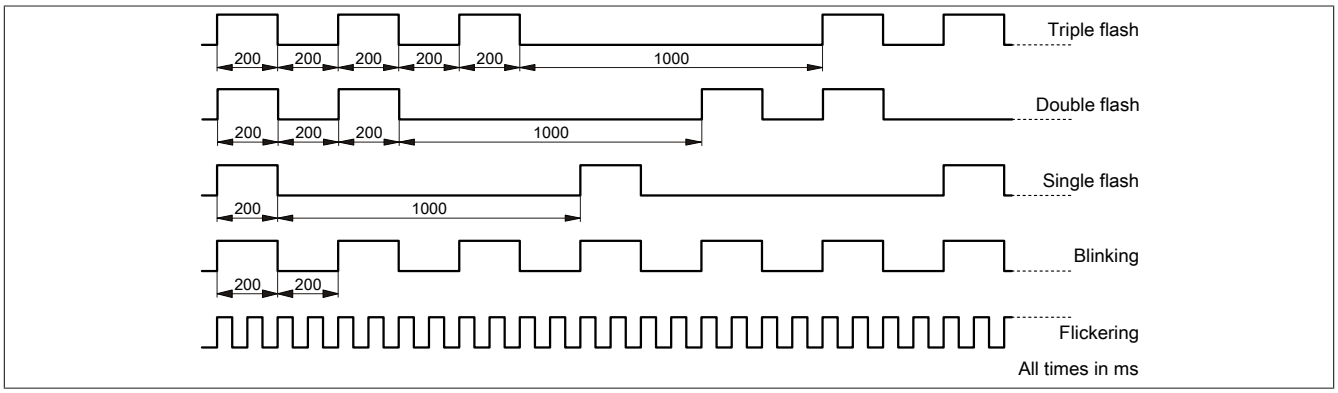
Red - Error	Description
On	The module is in an error mode (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: The LED blinks red several times immediately after startup. This is not an error.

Table 504: Status/Error LED as Error LED - POWERLINK operating mode

Green - Status	Description
Off	**Mode** The module is in NOT_ACTIVE mode or: • Switched off • Starting up • Not configured correctly in Automation Studio • Defective **Managing node (MN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to PRE_OPERATIONAL_1 mode. If POWERLINK communication is detected before the time expires, however, then the MN will not be started. **Controlled node (CN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to BASIC_ETHERNET mode. If POWERLINK communication is detected before this time expires, however, the module switches immediately to PRE_OPERATIONAL_1 mode.
Green flickering (approx. 10 Hz)	**Mode** The module is in BASIC_ETHERNET mode. The interface is being operated as an Ethernet TCP/IP interface. **Managing node (MN)** This state can only be changed by resetting the module. **Controlled node (CN)** If POWERLINK communication is detected while in this state, the module will transition to the PRE_OPERATIONAL_1 state.
Single flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_1 mode. **Managing node (MN)** The MN starts "reduced cycle" operation. Cyclic communication is not yet taking place. **Controlled node (CN)** The module can be configured by the MN in this state. The CN waits until it receives an SoC frame and then switches to the PRE_OPERATIONAL_2 mode. An LED lit red in this state indicates failure of the MN.
Double flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_2 mode. **Managing node (MN)** The MN begins cyclic communication (cyclic input data is not yet being evaluated). The CNs are configured in this state. **Controlled node (CN)** The module can be configured by the MN in this state. A command then switches the module to READY_TO_OPERATE mode. An LED lit red in this mode indicates failure of the MN.
Triple flash (approx. 1 Hz)	**Mode** The module is in the READY_TO_OPERATE state. **Managing node (MN)** Cyclic and asynchronous communication is taking place. Any received PDO data is ignored. **Controlled node (CN)** The configuration of the module is completed. Normal cyclic and asynchronous communication is taking place. The PDO data sent corresponds to the PDO mapping. Cyclic data is not yet being evaluated, however. An LED lit red in this mode indicates failure of the MN.
On	**Mode** The module is in PRE_OPERATIONAL_2 mode. PDO mapping is active and cyclic data is being evaluated.
Blinking (approx. 2.5 Hz)	**Mode** The module is in STOPPED mode. **Managing node (MN)** This status is not possible for the MN. **Controlled node (CN)** No output data is produced or input data supplied. It is only possible to enter or leave this mode after the MN has given the appropriate command.

Table 505: Status/Error LED as Status LED - POWERLINK operating mode

Status LEDs - Blinking patterns



4.23.16.5.4 System failure error codes

Incorrect configuration or defective hardware can cause a system stop error.

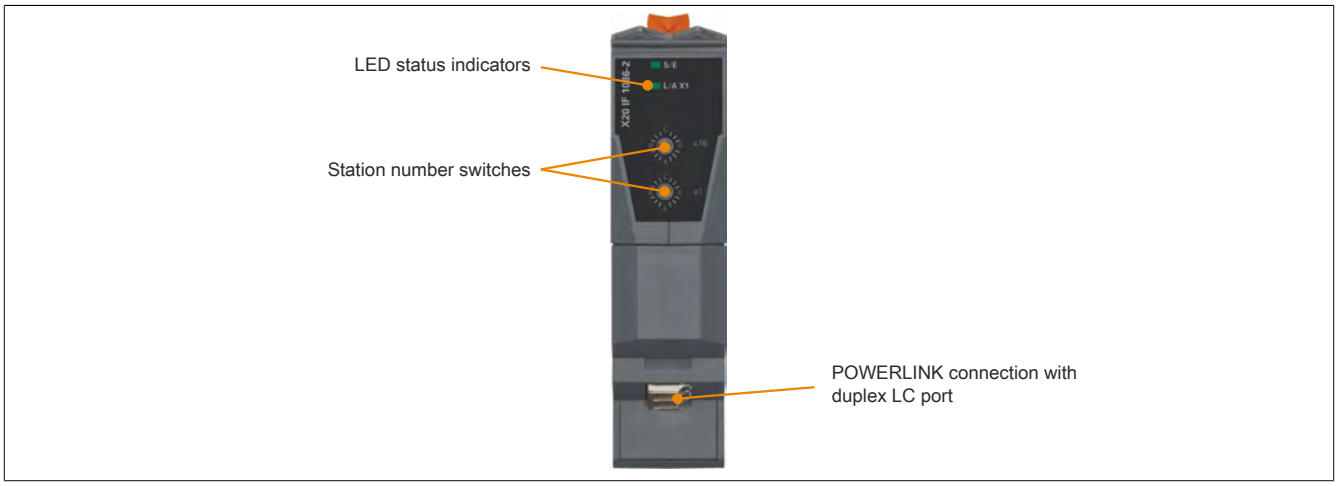
The error code is indicated by the red Error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. The error code is output cyclically every 2 seconds.

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	•	•	•	-	Pause	•	•	•	-	Pause
Hardware error: The module or a system component is defective and must be replaced.	-	•	•	-	Pause	-	•	•	-	Pause

Table 506: Status/Error ("S/E") LED - System failure error codes

Key:
- • ... 150 ms
- - ... 600 ms
- Pause ... 2 second delay

4.23.16.6 Operating and connection elements



4.23.16.7 POWERLINK node number

The node number for the POWERLINK station is set using the two number switches. The node number can also be directly configured using Automation Studio.

4.23.16.7.1 POWERLINK V1

Switch position	Description
0x00	Operation as managing node.
0x01 - 0xFD	Node number of the POWERLINK node. Operation as controlled node.
0xFE - 0xFF	Reserved, switch position not permitted

Table 507: POWERLINK V1 - Node numbers

4.23.16.7.2 POWERLINK

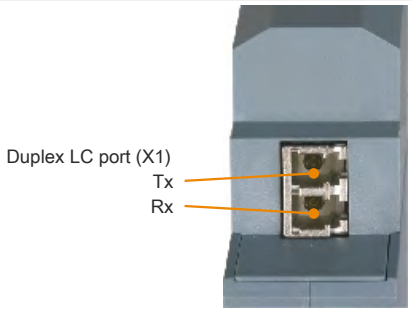
Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node.
0xF0	Operation as a managing node.
0xF1 - 0xFF	Reserved, switch position not permitted

Table 508: POWERLINK node number

4.23.16.7.3 Ethernet mode

In this mode, the interface is operated as an Ethernet interface. The INA2000 station number can be set using the B&R Automation Studio software.

4.23.16.8 Duplex LC port

Figure	Description
	100 Base FX port, Duplex LC socket

4.23.16.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.16.10 Wiring guidelines for X20 modules with fiber optic cable

The following wiring guidelines must be observed:

- Cable fiber type: Multimode fiber with 62.5/125 µm or 50/125 µm core diameter
- On both sides: Duplex LC male connector
- Observe minimum cable flex radius (see data sheet for the cable)

4.23.17 X20IF1091

4.23.17.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with an X2X Link master interface.

- X2X Link connection

4.23.17.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF1091	X20 interface module, 1 X2X Link master interface, electrically isolated, order 1x TB704 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB704.9	Accessory terminal block, 4-pin, screw clamps 2.5 mm²	
0TB704.91	Accessory terminal block, 4-pin, cage clamp terminal block 2.5 mm²	

Table 509: X20IF1091 - Order data

4.23.17.3 Technical data

Product ID	X20IF1091
Short description	
Communication module	1x X2X Link master
General information	
B&R ID code	0x1F24
Status indicators	Module status, data transfer
Diagnostics	
Module status	Yes, using status LED
Data transfer	Yes, using status LED
Power consumption	0.97 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	X2X Link master
Design	4-pin male multipoint connector
Number of stations	Max. 253
Bus terminating resistor	Internal
Internal bus supply	No
Network topology	Line
Distance between 2 stations	Max. 100 m
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB704 terminal block separately
Slot	In X20 CPU

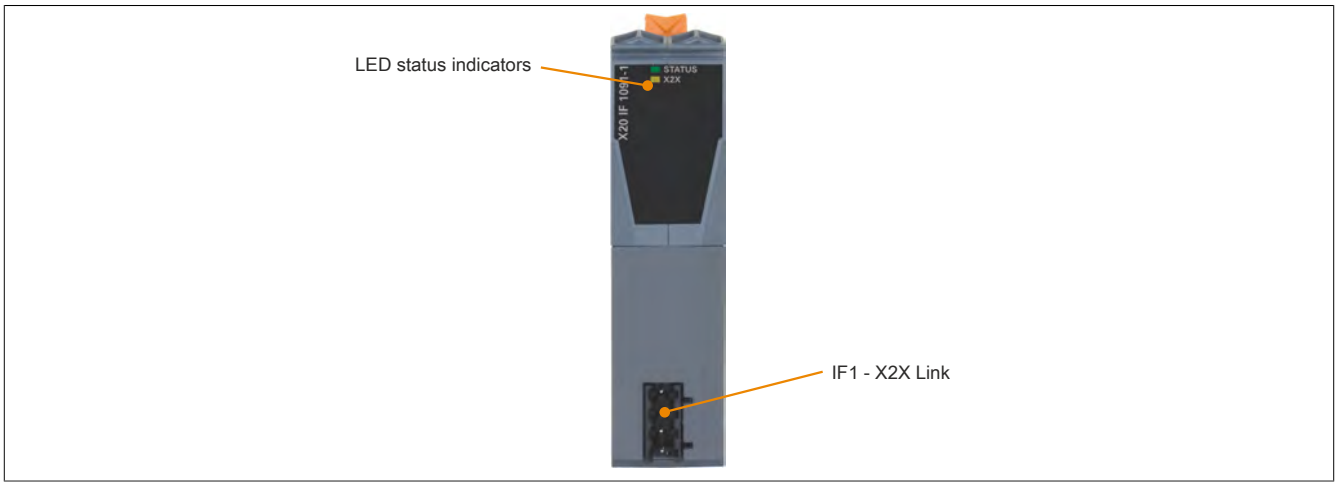
Table 510: X20IF1091 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

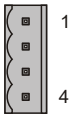
4.23.17.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	X2X	Yellow	On	Module sending data via the X2X Link interface

4.23.17.5 Operating and connection elements



4.23.17.6 X2X Link interface (IF1)

Interface	Pinout		
	Terminal	Function	
	1	X2X	
	2	X2X⊥	
	3	X2X\	
	4	SHLD	Shield
4-pin male multipoint connector			

4.23.17.7 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.18 X20IF10A1-1

4.23.18.1 General information

The interface module is equipped with an AS master interface. It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

AS-i stands for actuator-sensor interface and is a bus system for the lowest field level of automation technology. Using AS-i bus systems provides an easy and affordable way to connect, operate and service sensors and actuators.

This eliminates the need for parallel wiring, where each individual sensor or actuator was connected to the input or output module via a separate wire. A dual-core wire is used instead, which transfers both power and information at the same time.

- AS interface master
- Electrically isolated
- 4-pin bus connector

4.23.18.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF10A1-1	X20 interface module, for DTM configuration, 1 ASi master interface, electrically isolated, order 1x TB704 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB704.9	Accessory terminal block, 4-pin, screw clamps 2.5 mm²	
0TB704.91	Accessory terminal block, 4-pin, cage clamp terminal block 2.5 mm²	

Table 511: X20IF10A1-1 - Order data

4.23.18.3 Technical data

Product ID	X20IF10A1-1
Short description	
Communication module	AS interface master
General information	
B&R ID code	0xA718
Status indicators	Module status, network status, data transfer
Diagnostics	
Module status	Yes, using status LED and software
Network status	Yes, using status LED and software
Data transfer	Yes, using status LED
Fieldbus current consumption	Max. 27 mA
Power consumption	
Bus	1.1 W
Fieldbus	0.85 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	AS interface master
Design	4-pin male multipoint connector
Power supply	ASi power supply
Voltage range	24 to 32 V
Controller	netX100
Max. number of slaves	62
Max. distance	
Standard	100 m
With additional components	500 m
Max. cycle time	5 ms
Response time	Typ. 3 ms
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB704 terminal block separately
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller

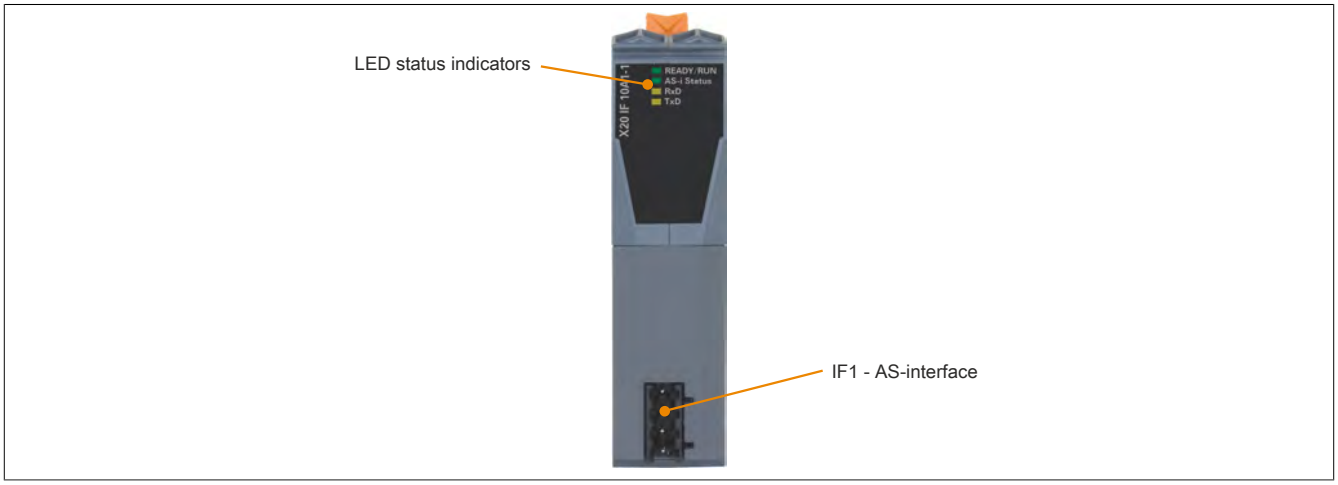
Table 512: X20IF10A1-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.18.4 LED status indicators

Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	Blinking	Error when booting
			On	Communication on the PCI bus has not yet been started
	AS-i status	Green/red	Off	Configuration not found for this channel
			Blinking	Configuration mode is active
		Green	Blinking quickly	Communication has stopped
			Blinking	Configuration error, data exchange is active
			On	Configuration error-free, data exchange is active
		Red	Blinking	AS-interface power loss
			On	Fatal system error or hardware error
	RxD	Yellow	Flickering or on	The module is receiving data via the AS-interface
	TxD	Yellow	Flickering or on	The module is sending data via the AS-interface

4.23.18.5 Operating and connection elements



4.23.18.6 AS-interface (IF1)

Interface	Pinout	
	Terminal	Function
	1	ASi+
	2	ASi+
	3	ASi-
	4	ASi-
4-pin male multipoint connector		

4.23.18.7 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.18.7.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.18.8 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.19 X20IF10D1-1

4.23.19.1 General information

The interface module functions as an EtherNet/IP scanner (master). It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

The interface has two RJ45 sockets. Both connections lead to an integrated switch. This makes it easy to create daisy-chain connections using EtherNet/IP.

- EtherNet/IP Scanner
- Integrated switch for efficient cabling

4.23.19.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF10D1-1	X20 interface module, for DTM configuration, 1 EtherNet/IP scanner (master) interface, electrically isolated	

Table 513: X20IF10D1-1 - Order data

Optional accessories

Model number	Short description
X20CA0E61.xxxxx	POWERLINK connection cable RJ45 to RJ45, 0.2 to 20 m
X20CA0E61.0500	POWERLINK connection cable RJ45 to RJ45, 50 m

4.23.19.3 Technical data

Product ID	X20IF10D1-1
Short description	
Communication module	EtherNet/IP scanner (master)
General information	
B&R ID code	0xA71B
Status indicators	Module status, network status, data transfer
Diagnostics	
Module status	Yes, using status LED and software
Network status	Yes, using status LED and software
Data transfer	Yes, using status LED
Power consumption	2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
PLC - IF2	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Fieldbus	EtherNet/IP scanner (master)
Design	2x shielded RJ45 (switch)
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	10/100 Mbit/s
Transmission	
Physical layer	10 BASE-T/100 BASE-TX
Half-duplex	Yes
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Controller	netX100
Memory	8 MB SDRAM
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller

Table 514: X20IF10D1-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.19.4 LED status indicators

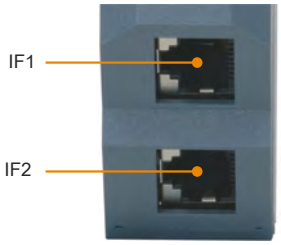
Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	Blinking	Boot error
			On	Communication on the PCI bus has not yet been started
	Mod status[1)]	Green	Blinking	Interface module not yet configured
			On	Scanner (Master) is operational
		Red	Blinking	Recoverable hardware error
			On	Irrecoverable hardware error
		Green/red	Blinking	Initialization / Self-test
			Off	No power to module
	Net status[1)]	Green	Blinking	No active connection
			On	Indicates at least one active connection
		Red	Blinking	Timeout occurred on at least one connection
			On	An IP address has been used repeatedly
		Green/red	Off	No IP address assigned or module not supplied
			Blinking	Initialization / Self-test
	L/A IF1/IF2	Green	Off	No link to remote station
			Flickering	A link to the remote station has been established. The LED blinks when Ethernet activity is taking place on the bus.
			On	A link to the remote station has been established.

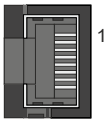
1) This LED is a green/red dual LED.

4.23.19.5 Operating and connection elements

4.23.19.6 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.23.19.7 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.19.7.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.19.8 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.20 X20(c)IF10D3-1

4.23.20.1 General information

The interface module functions as an EtherNet/IP adapter (slave). It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

The interface has two RJ45 sockets. Both connections lead to an integrated switch. This makes it easy to create daisy-chain connections using EtherNet/IP.

- EtherNet/IP adapter (slave)
- Integrated switch for efficient cabling

4.23.20.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.20.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF10D3-1	X20 interface module, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated	
X20cIF10D3-1	X20 interface module, coated, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated	

Table 515: X20IF10D3-1, X20cIF10D3-1 - Order data

Optional accessories

Model number	Short description
X20CA0E61.xxxxx	POWERLINK connection cable RJ45 to RJ45, 0.2 to 20 m
X20CA0E61.0500	POWERLINK connection cable RJ45 to RJ45, 50 m

4.23.20.4 Technical data

Product ID	X20IF10D3-1	X20cIF10D3-1
Short description		
Communication module	EtherNet/IP Adapter (slave)	
General information		
B&R ID code	0xA71C	0xE237
Status indicators	Module status, network status, data transfer	
Diagnostics		
Module status	Yes, using status LED and software	
Network status	Yes, using status LED and software	
Data transfer	Yes, using status LED	
Power consumption	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - IF1	Yes	
PLC - IF2	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Fieldbus	EtherNet/IP Adapter (slave)	
Design	2x shielded RJ45 (switch)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	10/100 Mbit/s	
Transmission		
Physical layer	10 BASE-T/100 BASE-TX	
Half-duplex	Yes	
Full-duplex	Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Controller	netX100	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller	In the X20c CPU and in the X20cBC1083 expandable bus controller

Table 516: X20IF10D3-1, X20cIF10D3-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.20.5 LED status indicators

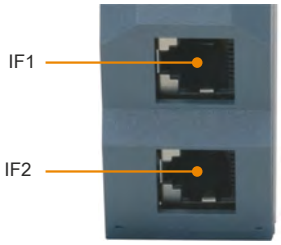
Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Green	On	PCI bus communication in progress
		Red	Blinking	Boot error
			On	Communication on the PCI bus has not yet been started
	Mod status[1)]	Green	Blinking	Interface module not yet configured
			On	Adapter (Slave) is operational
		Red	Blinking	Recoverable hardware error
			On	Irrecoverable hardware error
		Green/red	Blinking	Initialization / Self-test
			Off	No power to module
	Net status[1)]	Green	Blinking	No active connection
			On	Indicates at least one active connection
		Red	Blinking	Timeout occurred on at least one connection
			On	An IP address has been used repeatedly
		Green/red	Blinking	Initialization / Self-test
			Off	No IP address assigned or module not supplied
	L/A IF1/IF2	Green	Off	No link to remote station
			Flickering	A link to the remote station has been established. The LED blinks when Ethernet activity is taking place on the bus.
			On	A link to the remote station has been established.

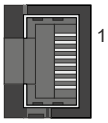
1) This LED is a green/red dual LED.

4.23.20.6 Operating and connection elements

4.23.20.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.23.20.8 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.20.8.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.20.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.20.10 Minimum DTM version for coated modules

Information:

The minimum DTM version required by coated modules is 1.0370.140220.12186. This version is included beginning with Automation Studio upgrade packs V4.0.18.x and V3.0.90.29.

4.23.21 X20IF10E1-1

4.23.21.1 General information

The interface module functions as a PROFINET RT controller (master). It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

The interface has two RJ45 sockets. Both connections lead to an integrated switch. This makes it easy to create daisy-chain connections using PROFINET RT.

- PROFINET RT controller
- Integrated switch for efficient cabling

4.23.21.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF10E1-1	X20 interface module for DTM configuration, 1 PROFINET RT controller (master) interface, electrically isolated	

Table 517: X20IF10E1-1 - Order data

Optional accessories

Model number	Short description
X20CA0E61.xxxxx	POWERLINK connection cable RJ45 to RJ45, 0.2 to 20 m
X20CA0E61.0500	POWERLINK connection cable RJ45 to RJ45, 50 m

4.23.21.3 Technical data

Product ID	X20IF10E1-1
Short description	
Communication module	PROFINET RT controller (master)
General information	
B&R ID code	0xA71D
Status indicators	Module status, network status, data transfer
Diagnostics	
Module status	Yes, using status LED and software
Network status	Yes, using status LED and software
Data transfer	Yes, using status LED
Power consumption	2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
PLC - IF2	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Fieldbus	PROFINET RT controller (master)
Design	2x shielded RJ45 (switch)
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100BASE-TX
Half-duplex	Yes
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Controller	netX100
Memory	8 MB SDRAM
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller

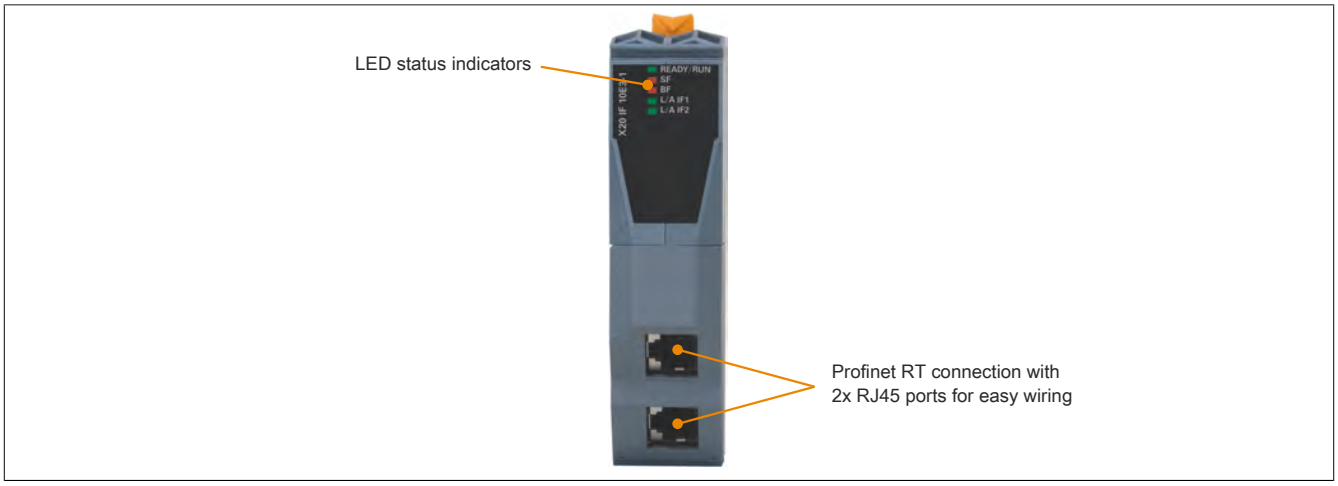
Table 518: X20IF10E1-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.21.4 LED status indicators

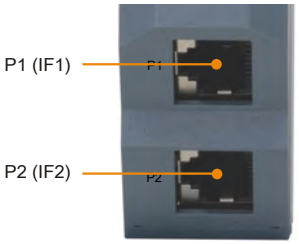
Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Red	Blinking	Boot error
			On	Communication on the PCI bus has not yet been started
		Green	On	PCI bus communication in progress
	SF	Red	Off	No error
			Blinking	Invalid configuration
			On	System errors
	BF	Red	Off	No error
			Blinking	Configuration error: Not all configured I/O modules are connected
			On	No link to remote station
	L/A IF1/IF2	Green	Off	No link to remote station
			Flickering	A link to the remote station has been established. The LED blinks when Ethernet activity is taking place on the bus.
			On	A link to the remote station has been established.

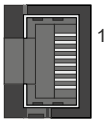
4.23.21.5 Operating and connection elements



4.23.21.6 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.23.21.7 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.21.7.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.21.8 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.22 X20(c)IF10E3-1

4.23.22.1 General information

The interface module functions as a PROFINET RT device (slave). It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

The interface has two RJ45 sockets. Both connections lead to an integrated switch. This makes it easy to create daisy-chain connections using PROFINET RT.

- PROFINET RT device
- Integrated switch for efficient cabling

4.23.22.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.22.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF10E3-1	X20 interface module, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated	
X20cIF10E3-1	X20 interface module, coated, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated	

Table 519: X20IF10E3-1, X20cIF10E3-1 - Order data

Optional accessories

Model number	Short description
X20CA0E61.xxxxx	POWERLINK connection cable RJ45 to RJ45, 0.2 to 20 m
X20CA0E61.0500	POWERLINK connection cable RJ45 to RJ45, 50 m

4.23.22.4 Technical data

Product ID	X20IF10E3-1	X20cIF10E3-1
Short description		
Communication module	PROFINET RT device (slave)	
General information		
B&R ID code	0xA71E	0xE238
Status indicators	Module status, network status, data transfer	
Diagnostics		
Module status	Yes, using status LED and software	
Network status	Yes, using status LED and software	
Data transfer	Yes, using status LED	
Power consumption	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - IF1	Yes	
PLC - IF2	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 1)	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Fieldbus	PROFINET RT device (slave)	
Design	2x shielded RJ45 (switch)	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100 BASE-TX	
Half-duplex	Yes	
Full-duplex	Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Controller	netX100	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller	In the X20c CPU and in the X20cBC1083 expandable bus controller

Table 520: X20IF10E3-1, X20cIF10E3-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.22.5 LED status indicators

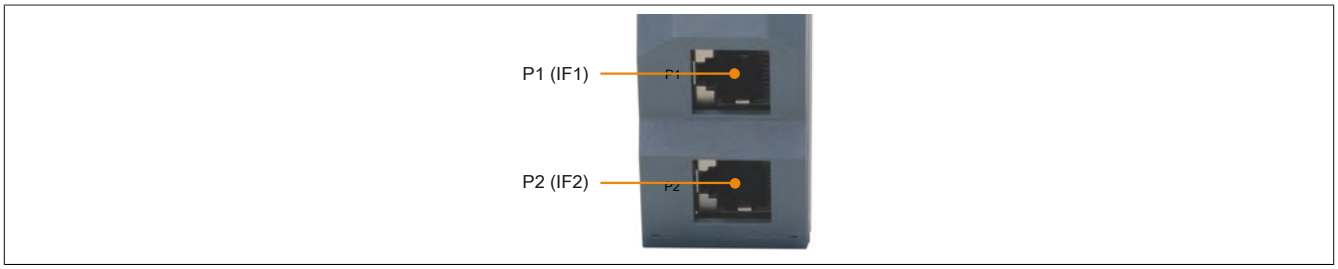
Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Red	Blinking	Boot error
			On	Communication on the PCI bus has not yet been started
		Green	On	PCI bus communication in progress
	SF	Red	Off	No error
			Cyc. Blinking[1)]	DCP signal service triggered via bus
			On	System errors
	BF	Red	Off	No error
			Blinking	No data exchange
			On	No configuration or physical connection error
	L/A IF1/IF2	Green	Off	No link to remote station
			Flickering	A link to the remote station has been established. The LED blinks when Ethernet activity is taking place on the bus.
			On	A link to the remote station has been established.

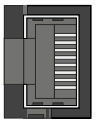
1) Blinks cyclically at 2 Hz, duration 3 s.

4.23.22.6 Operating and connection elements

4.23.22.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.23.22.8 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.22.8.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.22.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.22.10 Recognizing an invalid connection

All cyclic data is set to zero in the event of an invalid connection between the master and slave.
An invalid connection may be caused by the following:

- No connection between the master and the slave
- Interface card initialization is not yet complete.
- The master is in error mode.
- Data is marked as invalid (IOPS = Bad).

It cannot be determined whether the data is valid or invalid based on the transmitted data. In order to be able to reliably recognize an invalid connection, it is necessary to evaluate the master's IOPS data additionally in the application.

Forwarding IOPS data to the application can be enabled via the interface card's DTM ("I/O state information" in AS).

4.23.22.11 Minimum DTM version for coated modules

Information:

The minimum DTM version required by coated modules is 1.0370.140220.12186. This version is included beginning with Automation Studio upgrade packs V4.0.18.x and V3.0.90.29.

4.23.23 X20IF10G3-1

4.23.23.1 General information

The interface module functions as an EtherCAT slave. It can be operated in X20 CPUs or in the expandable X20BC1083 POWERLINK bus controller.

The interface has two RJ45 sockets. Both connections lead to an integrated switch. This simplifies daisy-chain connections with EtherCAT.

- EtherCAT slave
- Integrated switch for efficient cabling

4.23.23.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF10G3-1	X20 interface module for DTM configuration, 1 EtherCAT slave interface, electrically isolated	

Table 521: X20IF10G3-1 - Order data

Optional accessories

Model number	Short description
X20CA0E61.xxxxx	POWERLINK connection cable RJ45 to RJ45, 0.2 to 20.0 m
X20CA0E61.0500	POWERLINK connection cable RJ45 to RJ45, 50.0 m

4.23.23.3 Technical data

Product ID	X20IF10G3-1
Short description	
Communication module	EtherCAT slave
General information	
B&R ID code	0xA72C
Status indicators	Module status, network status, data transfer
Diagnostics	
Module status	Yes, using status LED and software
Network status	Yes, using status LED and software
Data transfer	Yes, using status LED
Power consumption	2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
PLC - IF1	Yes
PLC - IF2	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Fieldbus	EtherCAT (slave)
Design	2x shielded RJ45
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100BASE-TX
Half-duplex	No
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Controller	netX100
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	In the X20 CPU and in the X20BC1083 expandable bus controller

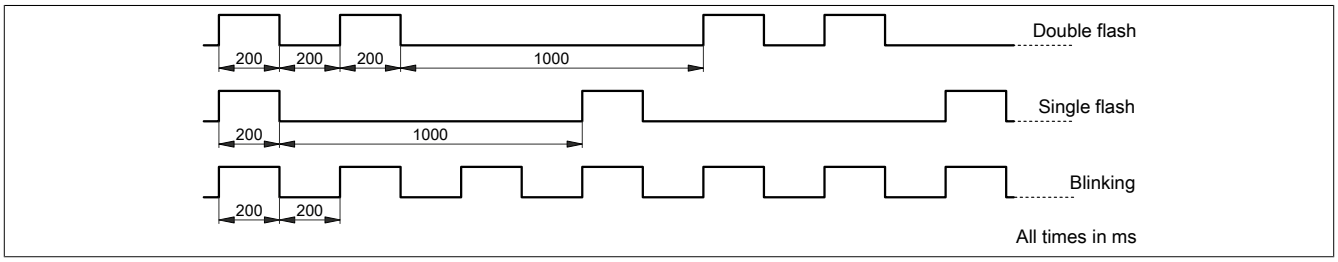
Table 522: X20IF10G3-1 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

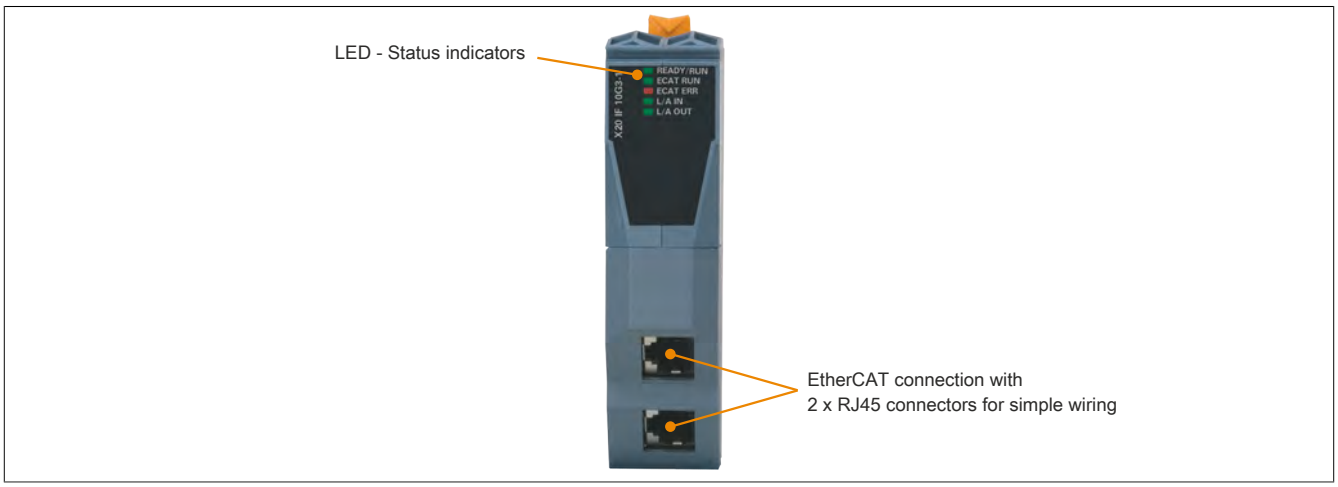
4.23.23.4 LED status indicators

Figure	LED	Color	Status	Description
	READY/RUN	Green/red	Off	No power to module
		Red	Blinking	Boot error
			On	Communication on the PCI bus has not yet been started
		Green	On	PCI bus communication in progress
	ECAT RUN	Green	Off	INIT status
			Single flash	SAFE-OPERATIONAL status
			Blinking	PREOPERATIONAL status
			On	Status OPERATIONAL
	ECAT ERR	Red	Off	No error
			Single flash	The module has an internal error and changed the EtherCAT status on its own
			Double flash	Watchdog timeout (process data watchdog or EtherCAT watchdog)
			Blinking	Invalid configuration data
			On	A critical communication or application error has occurred.
	L/A IN L/A OUT	Green	Off	No physical Ethernet connection exists (PORT CLOSED).
			Blinking	The respective LED blinks when Ethernet activity is present (PORT OPEN) on the corresponding RJ45 port (IN, OUT).
			On	Connection (link) established, however no communication (PORT OPEN).

Status LEDs - Blinking patterns

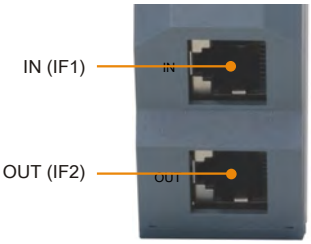


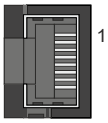
4.23.23.5 Operating and connection elements



4.23.23.6 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.23.23.7 Use with POWERLINK bus controllers

When this module is connected to the expandable POWERLINK bus controller, the amount of cyclic data is limited by the POWERLINK frame to 1488 bytes in each direction (input and output).
When using multiple IF10xx-1 interfaces or other X2X modules with a POWERLINK bus controller, the 1488 bytes are divided between all connected modules.

4.23.23.7.1 Operating netX modules with the X20BC1083 bus controller

The following must be taken into account to operate netX modules with the bus controller without problems:

- A minimum revision ≥E0 is required for the bus controller.
- NetX modules can only be operated with POWERLINK V2. V1 is not permitted.

4.23.23.8 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.24 X20(c)IF10X0

4.23.24.1 General information

Interface module for the operation of redundant CPUs.

- CPU-CPU data synchronization module for redundant CPU systems

4.23.24.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.24.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF10X0	X20 interface module, 1 redundancy link interface 1000BASE-SX, CPU-CPU data synchronization module for controller redundancy	
X20cIF10X0	X20 interface module, coated, 1 redundancy link interface 1000 Base-FX, CPU-CPU data synchronization for controller redundancy	

Table 523: X20IF10X0, X20cIF10X0 - Order data

4.23.24.4 Technical data

Product ID	X20IF10X0	X20cIF10X0
Short description		
Communication module	CPU redundancy link module	
General information		
B&R ID code	0xC3B4	0xE239
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Data transfer	Yes, using status LED and software	
Power consumption	1.93 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Fieldbus	Redundancy link	
Standard (compliance)	IEEE Std 802.3, 2002 Edition, Clause 38	
Design	1x duplex LC	
Transfer rate	1 Gbit/s	
Transmission		
Physical layer	1000BASE-SX	
Wave length	850 nm	
Cable fiber type	Multimode fiber with 62.5/125 µm or 50/125 µm core diameter LC connector on both sides	
Cable length		
MMF 50/125 µm	Min: 2 m, max: up to 500 m	
MMF 625/125 µm	Min: 2 m, max: up to 300 m	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 85%, non-condensing	Up to 100%, condensing
Storage	5 to 85%, non-condensing	
Transport	5 to 85%, non-condensing	
Mechanical characteristics		
Slot	Left IF slot on X20CP358x CPUs	Left IF slot on X20cCP358x CPUs

Table 524: X20IF10X0, X20cIF10X0 - Technical data

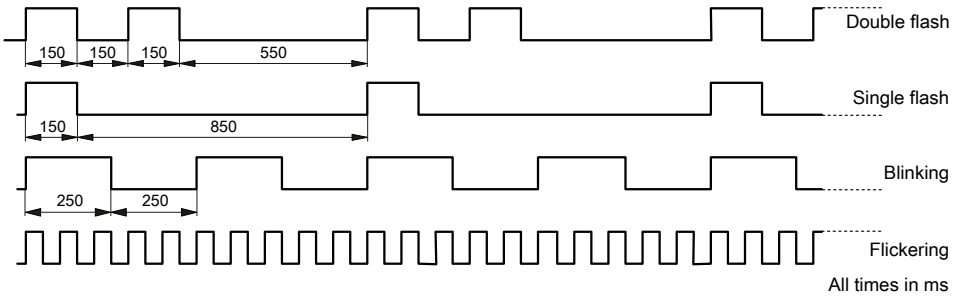
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.23.24.5 LED status indicators

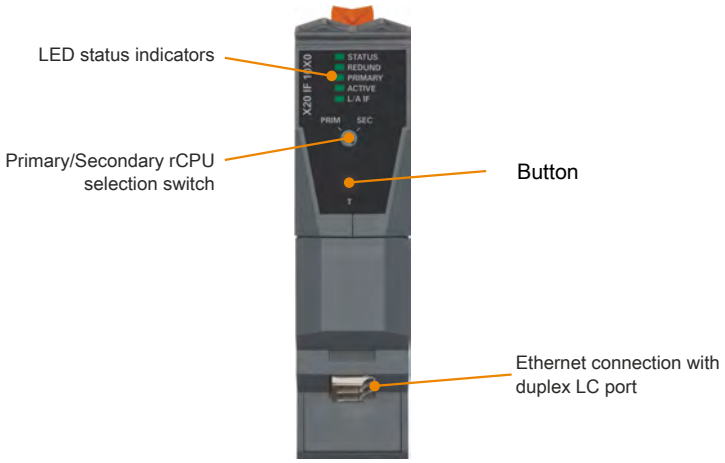
Figure	LED	Color	Status	Description
	STATUS[1)]	Green	On	Interface module active
		Red	Blinking	CPU starting up
	REDUND[1)]	Green	On	Possible to failover CPU with hot redundancy
			Blinking	Possible to failover CPU with warm redundancy
			Double flash	Possible to failover CPU with cold redundancy
			Flickering	Application synchronization in progress
		Red	On	Not possible to failover CPU. No distinction is made here between whether failover is temporarily or permanently not supported.
	PRIMARY[1)]	Green	On	rCPU = Primary CPU
			Off	rCPU = Secondary CPU
		Red	On	Invalid use of the selection switch. One rCPU must be configured as primary, the other as secondary. It is not permitted to change the switch position during operation.
	ACTIVE	Green	On	rCPU actively executing the application
			Off	rCPU inactive
	LA/IF[1)]	Green	On	Connection established to the redundancy partner
			Blinking	Redundancy link active. Data is being transferred for synchronization purposes.
		Red	On	No connection to the redundancy partner

1) This is a green/red dual LED.

LEDs - Blinking patterns



4.23.24.6 Operating and connection elements



4.23.24.7 Switch positions

The CPU can be set to primary or secondary using the "PRIM/SEC" selection switch.

During configuration, make sure that one rCPU is set as primary and the other rCPU as secondary.

Information:

It is not permitted to change the switch position during operation.

The "T" button is used for redundancy switchovers and manually synchronizing the application.

4.23.24.8 Derating

The temperatures listed in the technical data are valid when the unit is operated in the left IF slot of the X20CP358x CPUs.
When operated in the IF slot of the X20CP158x CPUs, the maximum temperature values are reduced by 5°C

4.23.24.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.25 X20(c)IF2181-2

4.23.25.1 General information

The interface module is used to expand the X20 CPU for specific applications. It is equipped with an POWERLINK interface.

POWERLINK is a standard protocol for Fast Ethernet with hard real-time properties. The Ethernet POWERLINK Standardization Group (EPSG) (see www.ethernet-powerlink.org).

Systems with redundant cabling can be implemented easily using POWERLINK. Unlike ring redundancy, cable redundancy does not require cable looping, which can sometimes be problematic. This allows the creation of all types of tree structures. When using a device with the link selector function, data is always transferred via the highest quality network lines. The link selector function is integrated in the X20IF2181-2 module.

- POWERLINK V2 for real-time Ethernet communication
- Integrated link selector function (preconfigured)
- Redundant Managing Node for CPU redundancy
- Integrated hub for efficient cabling (configurable)
- Configurable ring redundancy
- Poll response chaining
- Dynamic Node Allocation (DNA)

4.23.25.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.23.25.3 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF2181-2	X20 interface module, 1x link selector for POWERLINK cable redundancy, POWERLINK functions: - Managing node - Controlled node for iCN operation - Redundant managing node for controller redundancy - Ring redundancy - 2x hub - Multi ASend - PRC function 2x RJ45	
X20cIF2181-2	X20 interface module, coated, 1x link selector for POWERLINK cable redundancy, POWERLINK functions: - Managing node - Controlled node for iCN operation - Redundant managing node for controller redundancy - Ring redundancy - 2x hub - Multi ASend - PRC function 2x RJ45	

Table 525: X20IF2181-2, X20cIF2181-2 - Order data

Optional accessories

Model number	Short description
X20CA0E61.xxxxx	POWERLINK connection cable RJ45 to RJ45, 0.2 to 20 m
X20CA0E61.0500	POWERLINK connection cable RJ45 to RJ45, 50 m

4.23.25.4 Technical data

Product ID	X20IF2181-2	X20cIF2181-2
Short description		
Communication module	1x POWERLINK managing or controlled node	
General information		
B&R ID code	0xC3B3	0xE23A
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
POWERLINK cable redundancy system	Configurable	
Controller redundancy	Configurable	
Power consumption	2 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
PLC - X1	Yes	
PLC - X2	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Fieldbus	POWERLINK managing or controlled node	
Type	Type 5 [2]	
Design	2x shielded RJ45	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Controller	POWERLINK MAC	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	In X20 CPU	In X20c CPU

Table 526: X20IF2181-2, X20cIF2181-2 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) See the POWERLINK help system under "General information, Hardware - IF/LS".

4.23.25.5 LED status indicators

Figure	LED	Color	Status	Description
	S/E	Green/Red		Status/Error LED. The LED indicators are described in section 4.12.3.4.1 ""S/E" LED".
	RS	Green	On	Both cable connections are OK.
		Red	On	At least one cable connection is faulty.
	L/A X1/X2	Green	On	A link to the POWERLINK remote station has been established.
			Blinking	A link to the POWERLINK remote station has been established. Indicates Ethernet activity is taking place on the bus

4.23.25.5.1 "S/E" LED

The Status/Error LED is a green/red dual LED. The LED status can have different meanings depending on the operating mode.

4.23.25.5.1.1 Ethernet mode

In this mode, the interface is operated as an Ethernet interface.

Green - Status	Description
On	Interface being operated as an Ethernet interface

Table 527: Status/Error LED - Ethernet operating mode

4.23.25.5.1.2 POWERLINK

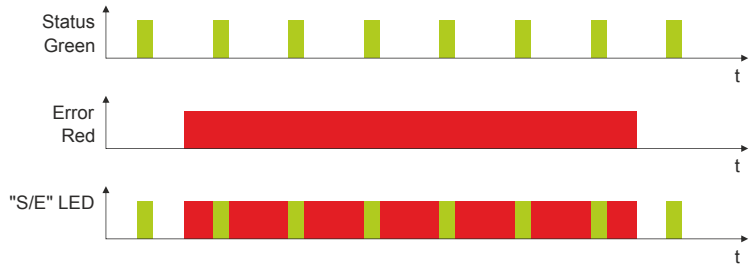
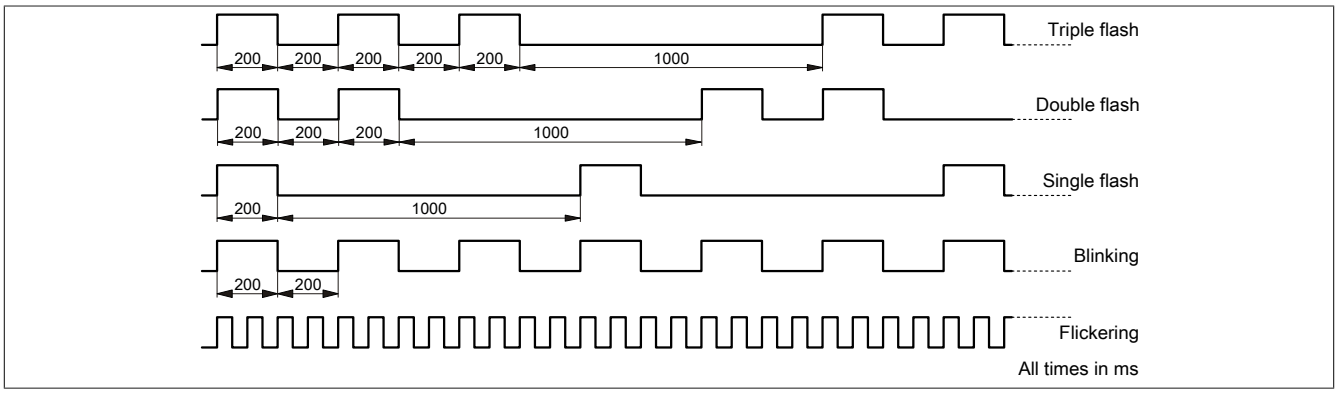
Red - Error	Description
On	The module is in an error mode (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: The LED blinks red several times immediately after startup. This is not an error.

Table 528: Status/Error LED as Error LED - POWERLINK operating mode

Green - Status	Description
Off	**Mode** The module is in NOT_ACTIVE mode or: • Switched off • Starting up • Not configured correctly in Automation Studio • Defective **Managing node (MN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to PRE_OPERATIONAL_1 mode. If POWERLINK communication is detected before the time expires, however, then the MN will not be started. **Controlled node (CN)** The bus is being monitored for POWERLINK frames. If a corresponding frame is not received within the defined time frame (timeout), then the module switches immediately to BASIC_ETHERNET mode. If POWERLINK communication is detected before this time expires, however, the module switches immediately to PRE_OPERATIONAL_1 mode.
Green flickering (approx. 10 Hz)	**Mode** The module is in BASIC_ETHERNET mode. The interface is being operated as an Ethernet TCP/IP interface. **Managing node (MN)** This state can only be changed by resetting the module. **Controlled node (CN)** If POWERLINK communication is detected while in this state, the module will transition to the PRE_OPERATIONAL_1 state.
Single flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_1 mode. **Managing node (MN)** The MN starts "reduced cycle" operation. Cyclic communication is not yet taking place. **Controlled node (CN)** The module can be configured by the MN in this state. The CN waits until it receives an SoC frame and then switches to the PRE_OPERATIONAL_2 mode. An LED lit red in this state indicates failure of the MN.
Double flash (approx. 1 Hz)	**Mode** The module is in PRE_OPERATIONAL_2 mode. **Managing node (MN)** The MN begins cyclic communication (cyclic input data is not yet being evaluated). The CNs are configured in this state. **Controlled node (CN)** The module can be configured by the MN in this state. A command then switches the module to READY_TO_OPERATE mode. An LED lit red in this mode indicates failure of the MN.
Triple flash (approx. 1 Hz)	**Mode** The module is in the READY_TO_OPERATE state. **Managing node (MN)** Cyclic and asynchronous communication is taking place. Any received PDO data is ignored. **Controlled node (CN)** The configuration of the module is completed. Normal cyclic and asynchronous communication is taking place. The PDO data sent corresponds to the PDO mapping. Cyclic data is not yet being evaluated, however. An LED lit red in this mode indicates failure of the MN.
On	**Mode** The module is in PRE_OPERATIONAL_2 mode. PDO mapping is active and cyclic data is being evaluated.
Blinking (approx. 2.5 Hz)	**Mode** The module is in STOPPED mode. **Managing node (MN)** This status is not possible for the MN. **Controlled node (CN)** No output data is produced or input data supplied. It is only possible to enter or leave this mode after the MN has given the appropriate command.

Table 529: Status/Error LED as Status LED - POWERLINK operating mode

Status LEDs - Blinking patterns



4.23.25.5.2 System failure error codes

Incorrect configuration or defective hardware can cause a system stop error.

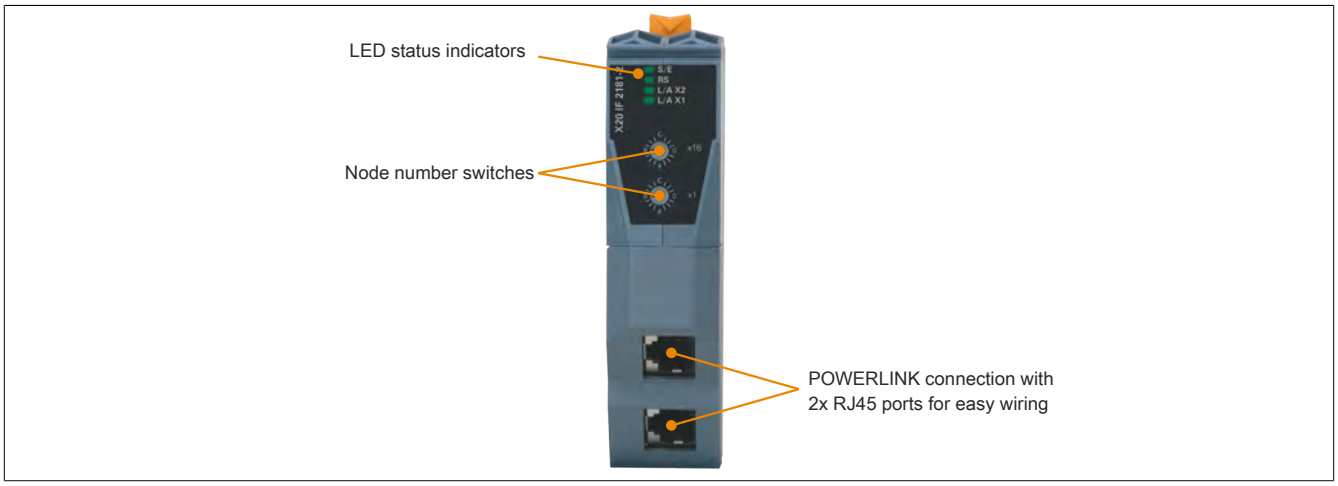
The error code is indicated by the red Error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. The error code is output cyclically every 2 seconds.

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	•	•	•	-	Pause	•	•	•	-	Pause
Hardware error: The module or a system component is defective and must be replaced.	-	•	•	-	Pause	-	•	•	-	Pause

Table 530: Status/Error ("S/E") LED - System failure error codes

Key:
- • ... 150 ms
- - ... 600 ms
- Pause ... 2 second delay

4.23.25.6 Operating and connection elements



4.23.25.7 POWERLINK node number

The node number for the POWERLINK station is set using the two number switches. The node number can also be directly configured using Automation Studio.

4.23.25.7.1 POWERLINK V2

Switch position	Description
0x00	Reserved, switch position not permitted.
0x01 - 0xEF	Node number of POWERLINK station. Operation as controlled node.
0xF0	Operation as managing node.
0xF1 - 0xF7	Reserved, switch position not permitted.
0xF8	CPU redundancy: Function as primary CPU
0xF9	CPU redundancy: Function as secondary CPU
0xFA - 0xFF	Reserved, switch position not permitted.

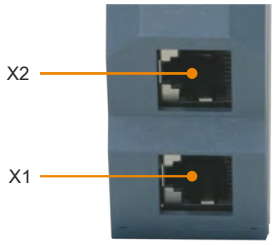
Table 531: POWERLINK V2 - Node numbers

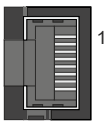
4.23.25.7.2 Ethernet mode

In this mode, the interface is operated as an Ethernet interface. The INA2000 station number can be set using the B&R Automation Studio software.

4.23.25.8 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.23.25.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.25.10 POWERLINK cable redundancy system

It is often indispensable to have redundant network cabling, especially in systems that handle technical processes. The potential for danger, especially to the lines that run through the system, is disproportionately high in relation to the need to keep communication active in all operating situations. This risk is effectively reduced with double cabling that is routed separately.

The POWERLINK cable redundancy system is based on the principle of doubling the transfer routing as well as providing continual and simultaneous monitoring. That means data is simultaneously fed into two cable lines using a corresponding mechanism. The same mechanisms are used to receive these telegrams from the redundant network.

Details about the structure of a redundancy system can be found in the "Redundancy for control systems" user's manual. The user's manual is available in the Downloads section of the B&R website www.br-automation.com.

4.23.26 X20IF2772

4.23.26.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with 2 CAN bus interfaces.

- Dual CAN bus connection
- Integrated terminating resistors

4.23.26.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF2772	X20 interface module, 2 CAN bus interfaces, max. 1 Mbit/s, electrically isolated, order 2x TB2105 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	

Table 532: X20IF2772 - Order data

4.23.26.3 Technical data

Product ID	X20IF2772
Short description	
Communication module	2x CAN bus
General information	
B&R ID code	0x1F25
Status indicators	Module status, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	1.2 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
IF1 - IF2	Yes
PLC - IF1	Yes
PLC - IF2	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Signal	CAN bus 2)
Design	5-pin male multipoint connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Terminating resistor	Integrated in the module
Controller	SJA 1000
IF2 interface	
Signal	CAN bus 2)
Design	5-pin male multipoint connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Terminating resistor	Integrated in the module
Controller	SJA 1000
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 2x TB2105 terminal blocks separately
Slot	In X20 CPU

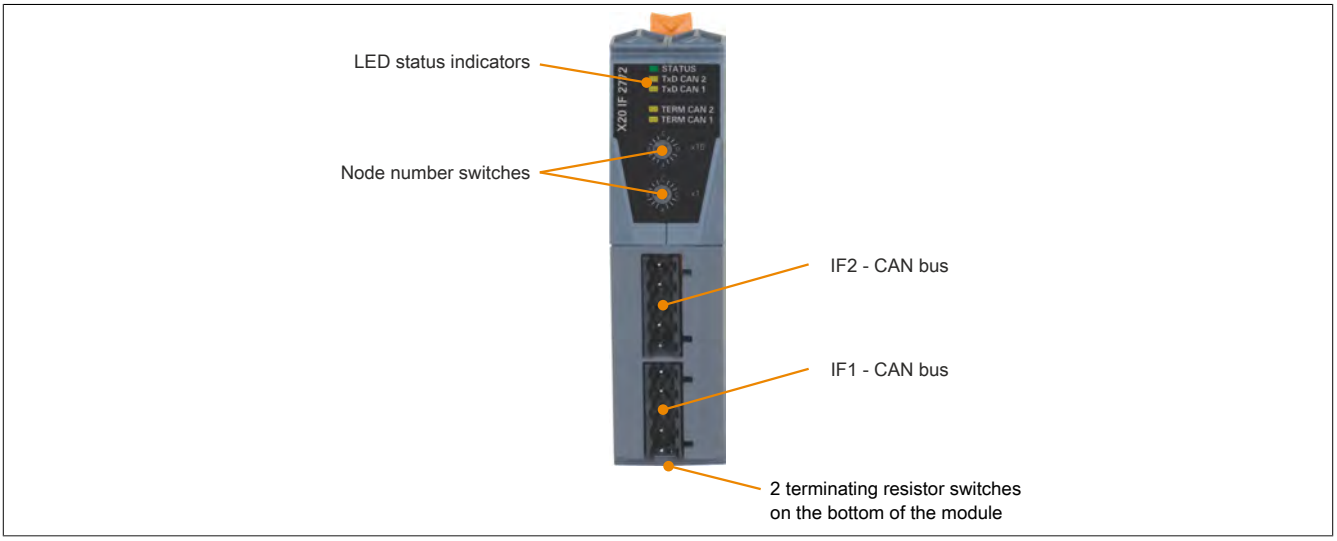
Table 533: X20IF2772 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) This CAN bus interface can be configured as a CANopen master in Automation Studio 3.0 and higher.

4.23.26.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	TxD CAN 1	Yellow	On	The module is sending data via the CAN bus interface (IF1)
	TxD CAN 2	Yellow	On	The module is sending data via the CAN bus interface (IF2)
	TERM CAN 1	Yellow	On	The integrated terminating resistor for the CAN bus interface (IF1) is turned on
	TERM CAN 2	Yellow	On	The integrated terminating resistor for the CAN bus interface (IF2) is turned on

4.23.26.5 Operating and connection elements

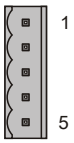


4.23.26.6 CAN bus node number

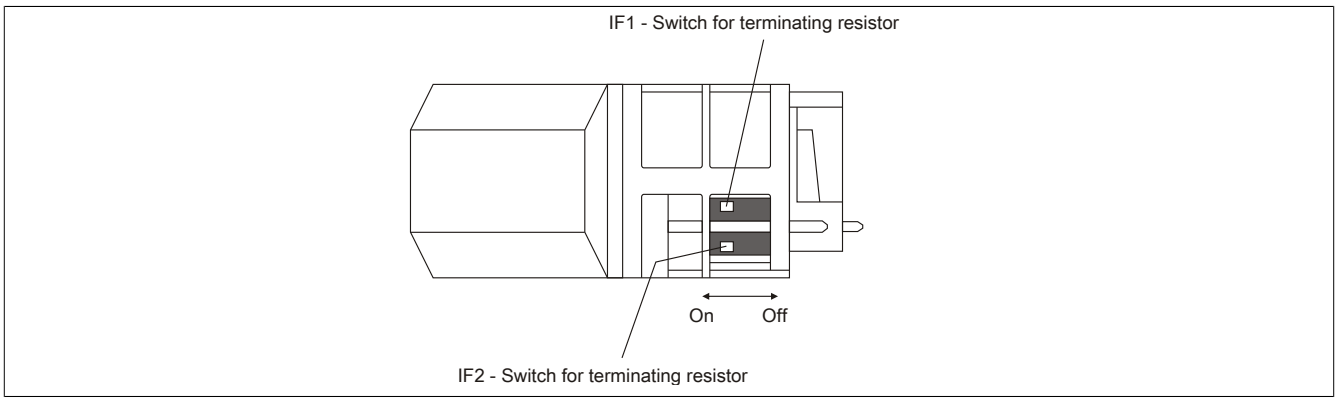
The node number for the CAN bus interfaces is set with the two hex switches.

4.23.26.7 Interfaces CAN bus 1 and CAN bus 2 (IF1 and IF2)

Both interfaces feature a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
 5-pin male multipoint connector	**Terminal**	**Function**	
	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	

4.23.26.8 Terminating resistor



Two terminating resistors are integrated in the interface module. The respective resistor can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM CAN 1" or "TERM CAN 2".

4.23.26.9 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.23.27 X20IF2792

4.23.27.1 General information

The interface module can be used to expand the X20 CPU for specific applications. It is equipped with both an X2X Link interface and a CAN bus interface.

- X2X Link connection
- CAN bus connection
- Integrated terminating resistor

4.23.27.2 Order data

Model number	Short description	Figure
	X20 interface module communication	
X20IF2792	X20 interface module, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, 1 X2X Link master interface, electrically isolated, order 1x TB2105 and 1x TB704 terminal block separately	
	Required accessories	
	Terminal blocks	
0TB2105.9010	Accessory terminal block, 5-pin, screw clamps 2.5 mm²	
0TB2105.9110	Accessory terminal block, 5-pin, cage clamp terminal block 2.5 mm²	
0TB704.9	Accessory terminal block, 4-pin, screw clamps 2.5 mm²	
0TB704.91	Accessory terminal block, 4-pin, cage clamp terminal block 2.5 mm²	

Table 534: X20IF2792 - Order data

4.23.27.3 Technical data

Product ID	X20IF2792
Short description	
Communication module	1x X2X Link master, 1x CAN bus
General information	
B&R ID code	0x1F26
Status indicators	Module status, data transfer, terminating resistor
Diagnostics	
Module status	Yes, using status LED
Data transfer	Yes, using status LED
Terminating resistor	Yes, using status LED
Power consumption	1.51 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
IF1 - IF2	Yes
PLC - IF1	Yes
PLC - IF2	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1]	Yes
KC	Yes
GOST-R	Yes
Interfaces	
IF1 interface	
Fieldbus	X2X Link master
Design	4-pin male multipoint connector
Number of stations	Max. 253
Bus terminating resistor	Internal
Internal bus supply	No
Network topology	Line
Distance between 2 stations	Max. 100 m
IF2 interface	
Signal	CAN bus [2]
Design	5-pin male multipoint connector
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Terminating resistor	Integrated in the module
Controller	SJA 1000
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x TB704 and 1x TB2105 terminal block separately
Slot	In X20 CPU

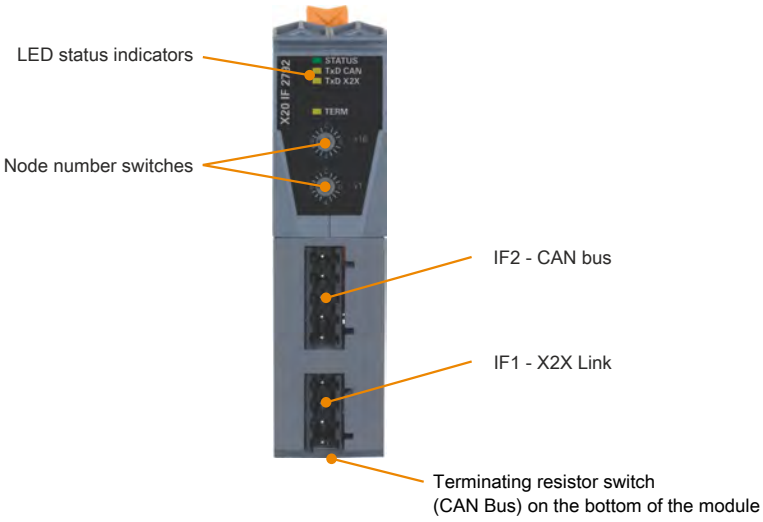
Table 535: X20IF2792 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) This CAN bus interface can be configured as a CANopen master in Automation Studio 3.0 and higher.

4.23.27.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS	Green	On	Interface module active
		Red	On	CPU starting up
	TxD CAN	Yellow	On	The module is sending data via the CAN bus interface
	TxD X2X	Yellow	On	Module sending data via the X2X Link interface
	TERM	Yellow	On	The integrated terminating resistor for the CAN bus interface is turned on

4.23.27.5 Operating and connection elements



4.23.27.6 X2X Link interface (IF1)

Interface	Pinout		
	Terminal	Function	
	1	X2X	
	2	X2X⊥	
	3	X2X\	
	4	SHLD	Shield
4-pin male multipoint connector			

4.23.27.7 CAN bus node number

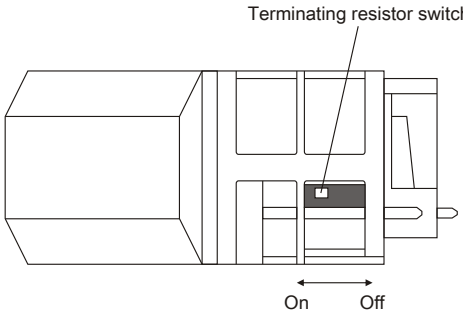
The node number for the CAN bus interface (IF2) is set with the two hex switches.

4.23.27.8 CAN bus interface

The interface is a 5-pin multipoint plug. The 0TB2105 terminal block must be ordered separately.

Interface	Pinout		
	Terminal	Function	
 5-pin male multipoint connector	1	CAN⊥	CAN ground
	2	CAN_L	CAN low
	3	SHLD	Shield
	4	CAN_H	CAN high
	5	NC	

4.23.27.9 Terminating resistor



The interface module has an integrated terminating resistor for the CAN bus interface. It can be turned on and off with a switch on the bottom of the housing. An active terminating resistor is indicated by the "TERM" LED.

4.23.27.10 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

4.24 Hub system

The X20HB8880 hub is a device that can be used universally in standard Ethernet networks or POWERLINK networks. It is suitable for 100 Mbit/s (Fast Ethernet) networks. Due to its modular structure, the hub can be configured as 2/4/6x Fast Ethernet hub as needed.

The X20BC8083 bus controller makes it possible to connect X2X Link I/O nodes to POWERLINK. The bus modules expanded to the left allow connection of up to 2 hub expansion modules in addition to the bus controller. This means that a 2/4/6x Fast Ethernet hub is also available on the bus controller depending on the degree of expansion.

4.24.1 Brief information

Product ID	Short description	on page
X20ET8819	X20 Ethernet analysis tool, can be expanded with active hub modules, 2x RJ45	2289
X20HB8815	X20 POWERLINK - TCP/IP gateway, can be expanded with active hub modules, 2x RJ45	2301
X20HB8880	X20 base hub module, integrated 2-port hub, 2x RJ45	2309
X20HB88G0	X20 EtherCAT junction base module integr. 2x EtherCAT junction, 2x RJ45 connection	2313
X20cHB8815	X20 POWERLINK - TCP/IP gateway, coated, can be expanded with active hub modules, 2x RJ45	2301
X20cHB8880	X20 base hub module, coated, integrated 2-port hub, 2x RJ45	2309

4.24.2 X20ET8819

4.24.2.1 General information

Analyzing POWERLINK

POWERLINK has proven itself in the field for years and rarely has problems during commissioning and production. Nonetheless, it is still possible for communication disturbances to occur due to damaged or poor quality cables. If an error occurs, localizing and correcting it is usually very easy thanks to the heterogeneous structure of this flat network type (all data is always visible throughout the network). What's problematic are errors that occur sporadically. This is where tools such as Omnipeek™ or Wireshark come in.

These tools (or more likely the standard PC technology being used) reach their limits, however, when dealing with machines that have short network cycles. Either not all frames can be recorded, or some telegrams are lost altogether. In these cases, what's needed is a special hardware tool that can work very quickly, record and save every bit of traffic and then pass it on to a laptop.

Ethernet analysis tool X20ET8819

This module provides different operating modes. For example, it can work passively on the network, in which case the real-time behavior remains unchanged. The device listens in and selectively takes in data when certain defined trigger conditions are met. It can read all of the data, mark it with a timestamp, store it temporarily and ultimately pass it on to a PC. The data is then analyzed in the familiar PC environment.

- NetTime time stamp has a resolution of 20 ns
- Recording and analysis of CRC and frame errors
- Triggers can also be activated using external digital signals
- Analysis of both half-duplex and full-duplex networks
- Able to record two networks simultaneously

4.24.2.2 Order data

Model number	Short description	Figure
	X20 hub system	
X20ET8819	X20 Ethernet analysis tool, can be expanded with active hub modules, 2x RJ45	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20PS9400	X20 power supply module, for bus controller and internal I/O supply, X2X Link supply	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Digital inputs	
X20DI9371	X20 digital input module, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections	
	Digital outputs	
X20DO9322	X20 digital output module, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections	
	System modules for the X20 hub system	
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45	
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable	

Table 536: X20ET8819 - Order data

4.24.2.3 Technical data

Product ID	X20ET8819
Short description	
Ethernet analysis tool	Ethernet analysis tool with up to 2 slots for hub expansion modules
General information	
Status indicators	Module status, bus function
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED and software
Power consumption	2 W
Electrical isolation	
Fieldbus - Supply	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1]	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Type	Ethernet analysis tool
Design	2x shielded RJ45
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100BASE-TX
Half-duplex	Yes
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS9400 power supply module separately Order 1x X20BB8x bus base separately
Spacing [2]	
X20BB80	37.5 $^{+0.2}$ mm
X20BB81	62.5$^{+0.2}$ mm
X20BB82	87.5$^{+0.2}$ mm

Table 537: X20ET8819 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

2) Spacing is based on the width of the X20BB80 bus base. Up to two X20HB2880 or X20HB2881 hub expansion modules and one X20PS9400 power supply module are also always required for the Ethernet analysis tool.

4.24.2.4 LED status indicators

Figure	LED	Color	Status	Description
	S/E[1]	Green/red		Status/Error LED. The statuses of this LED are described in section 4.24.2.5 "S/E LED".
	L/A IF1	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus
	L/A IF2	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus

1) The Status/Error LED is a green/red dual LED.

4.24.2.5 S/E LED

The Status/Error LED is a green and red dual LED.

Red - Error	Description
On	This error can occur only in Analysis mode. If packets are lost when in Analysis mode, the red Status LED lights up. Remedy: Use the "MODE" switch to reduce the number of bytes in the received packets (see 4.24.2.14 "Analysis mode" on page 2297). As soon as no packets are lost for longer than 1 s, it switches back to green.

Table 538: Status/error LED is red: LED indicates error

Green - Status	Description
Off	The Ethernet analysis tool is either booting or not receiving power.
Green flickering (approx. 10 Hz)	The analysis tool is in Service mode: Analysis tool disabled, go to website to update firmware (see 4.24.2.13 "Firmware update" on page 2296)
Single flash (approx. 1 Hz)	The external trigger is active. No data is currently being recorded. No data has been recorded since turned on.
Double flash (approx. 1 Hz)	The external trigger is active. No data is currently being recorded. However, the analysis tool has recorded data at least once. This means that the trigger has been triggered at least once.
On	The analysis tool is active, and is recording all received packets.

Table 539: Status/error LED is green: LED indicates operation

System failure error codes

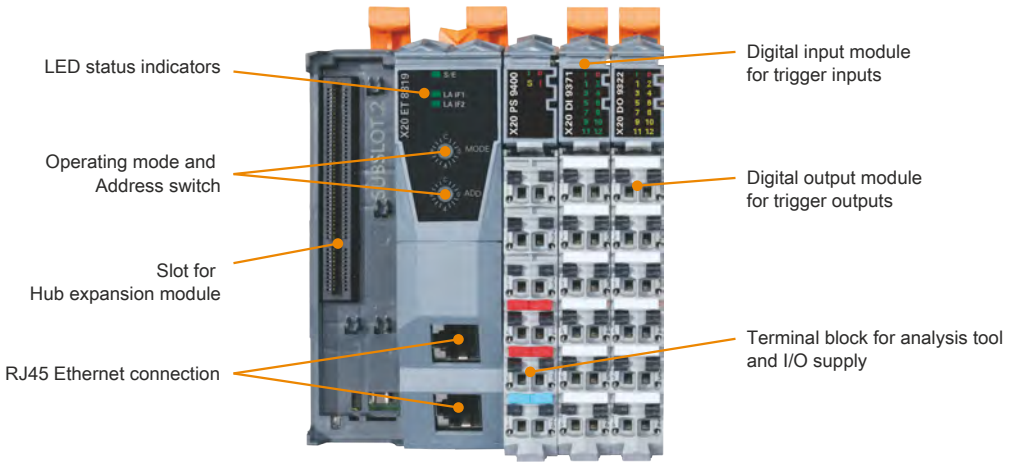
Incorrect node number or defective hardware can cause a system failure error. The error code is indicated by the red error LED using four switch-on phases. The switch-on phases have a duration of either 150 ms or 600 ms. Error code output is repeated cyclically after 2 seconds.

Key: • ... 150 ms
− ... 600 ms
Delay ... 2 sec. delay

Error description	Error code indicated by red status LED									
RAM error: The module is defective and must be replaced.	•	•	•	−	Pause	•	•	•	−	Pause
Wrong node number	•	−	−	−	Pause	•	−	−	−	Pause
Hardware errors: The module or a system component is defective and must be replaced.	−	•	•	−	Pause	−	•	•	−	Pause

Table 540: Status/Error LED as Error LED - System failure error codes

4.24.2.6 Operating and connection elements

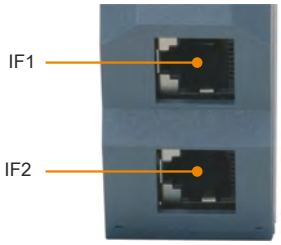


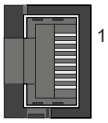
4.24.2.7 Operating mode and address switch

switches	Description
MODE	Specifies the mode in which the analysis tool is run (see 4.24.2.14 "Analysis mode" on page 2297)
ADD	The following addresses are derived from the position of the ADD switch: • Own IP address (192.168.0.ADD) • Analysis mode: Destination MAC (01:00:5 e: 00:00: ADD) • Analysis mode: MulticastIP 239.0.0.ADD Note: Position 0 is not permitted

4.24.2.8 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.24.2.9 Hardware configuration 1

If the Ethernet analysis tool is run without additional hub expansion modules, then recording is only possible on port T0. The analysis tool must be connected to an available hub port in the system.

Information:

An X20HB288x module is not permitted in this hardware configuration.

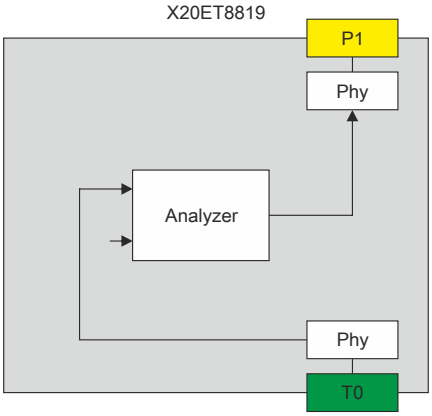


Figure 371: Diagram of hardware configuration 1

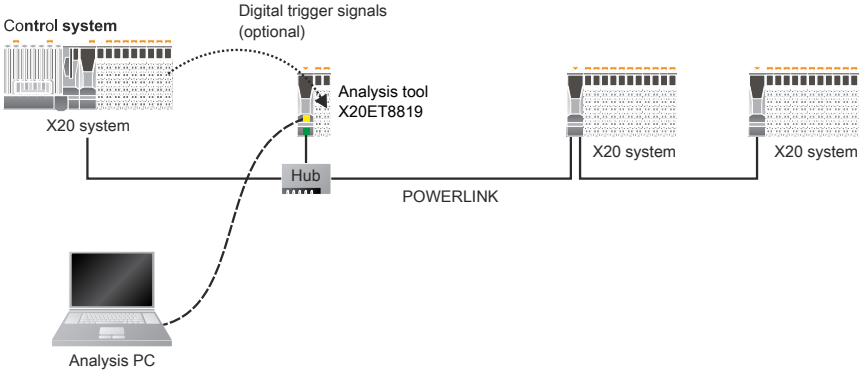


Figure 372: Example application of hardware configuration 1

4.24.2.10 Hardware configuration 2

Extending the Ethernet analysis tool with an X20HB2880 or X20HB2881 allows even full-duplex lines to be recorded as well. In this case ports T1 and T2 are analyzed.

Information:

Only the required X20HB288x module is permitted in this hardware configuration. A second X20HB288x module would produce different behavior (see Hardware configuration 3).

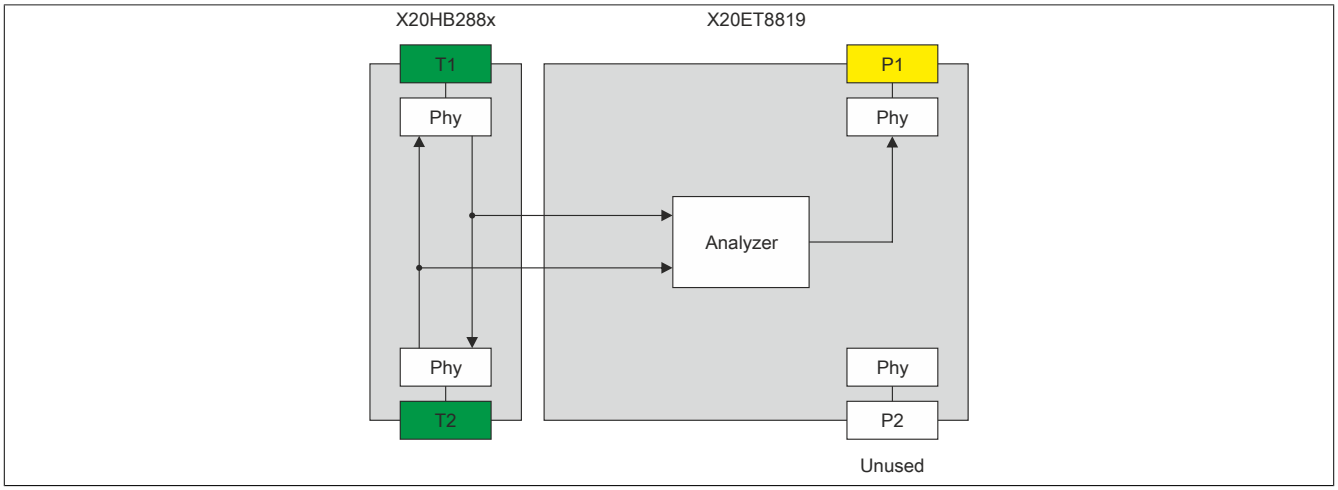


Figure 373: Diagram of hardware configuration 2

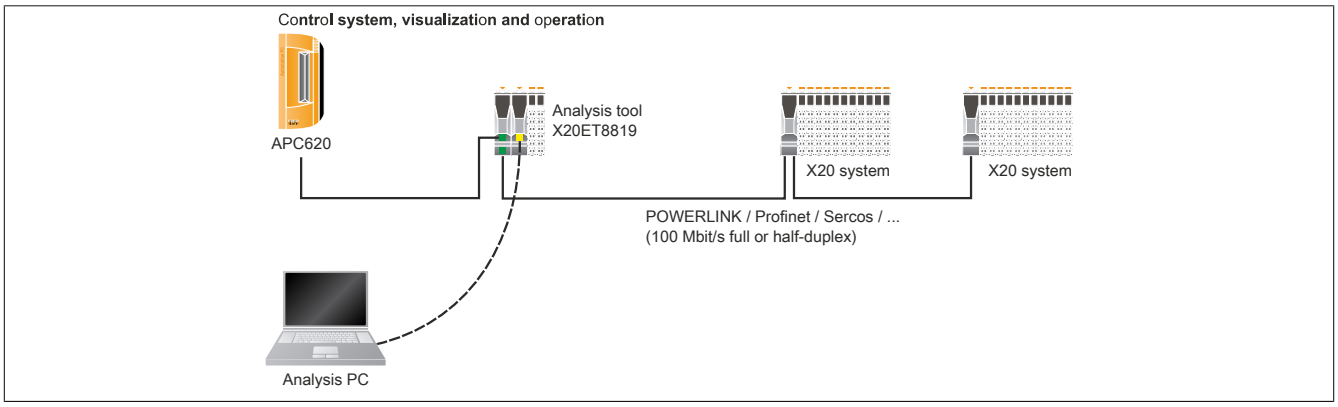


Figure 374: Example application of hardware configuration 2

4.24.2.11 Hardware configuration 3a

Simultaneous data recording at two locations in the network is possible by using two X20HB2880 or X20HB2881. **Only** data from T1 and T3 is analyzed.

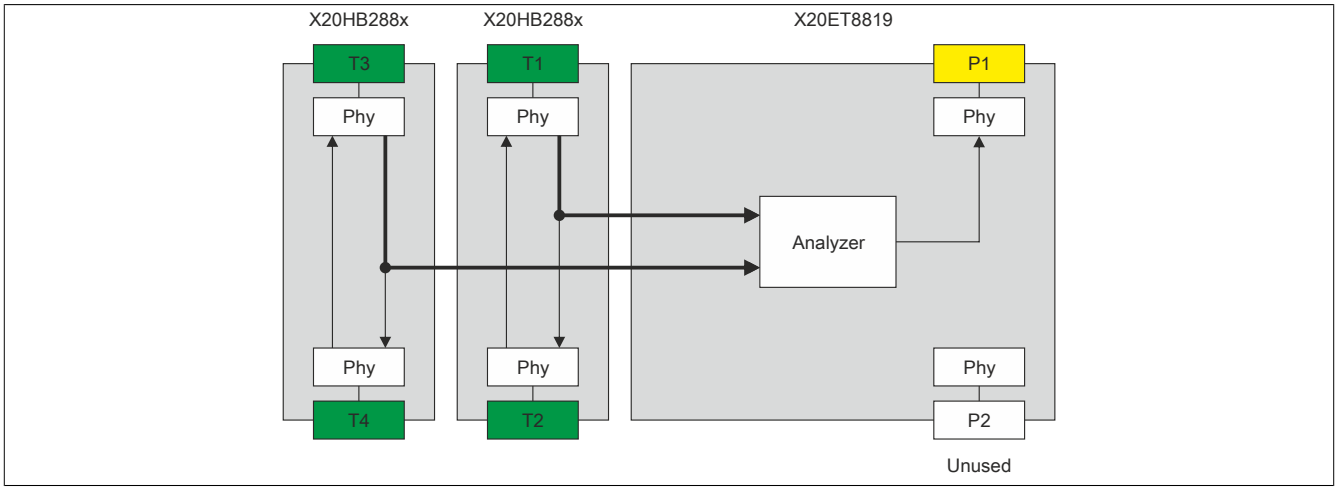


Figure 375: Diagram of hardware configuration 3a

Example application 1 shows data being recorded simultaneously from two hubs.

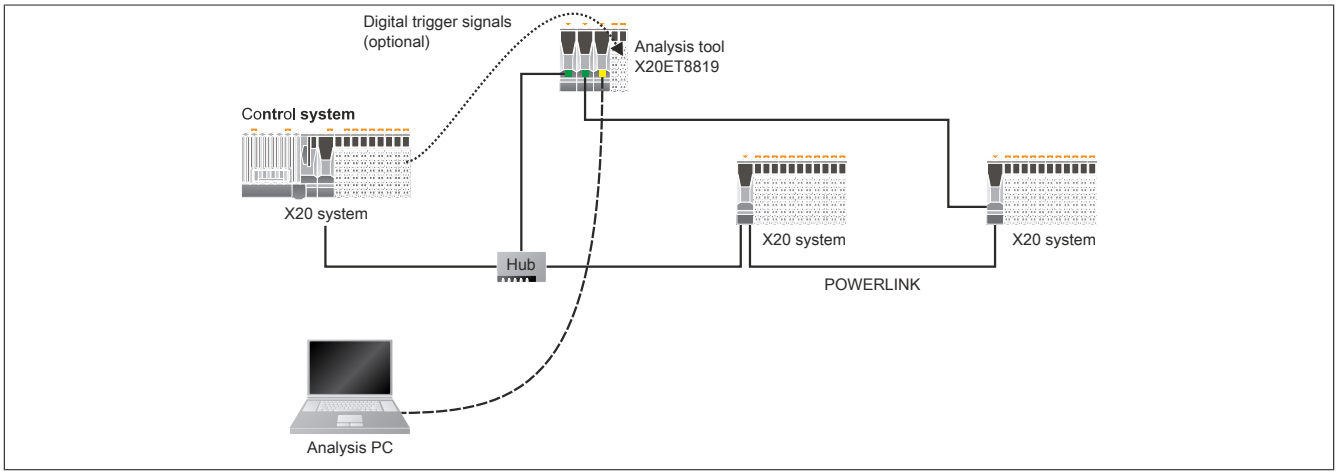


Figure 376: Example application 1 of hardware configuration 3, connection via hubs

The two hub expansion modules can also be inserted in series in the network. It should be noted that in this case data recording is only possible in one direction at a time.

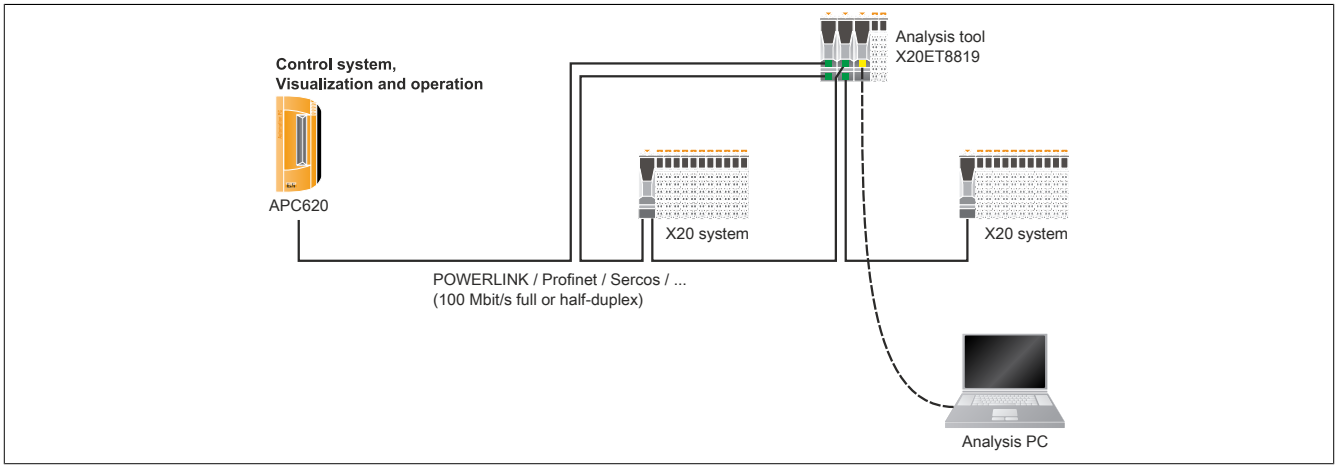


Figure 377: Example application 2 of hardware configuration 3, connection in line

4.24.2.12 Hardware configuration 3b

With firmware V 1.03 and higher, data traffic in half-duplex networks (e.g. POWERLINK) is recorded in both directions.

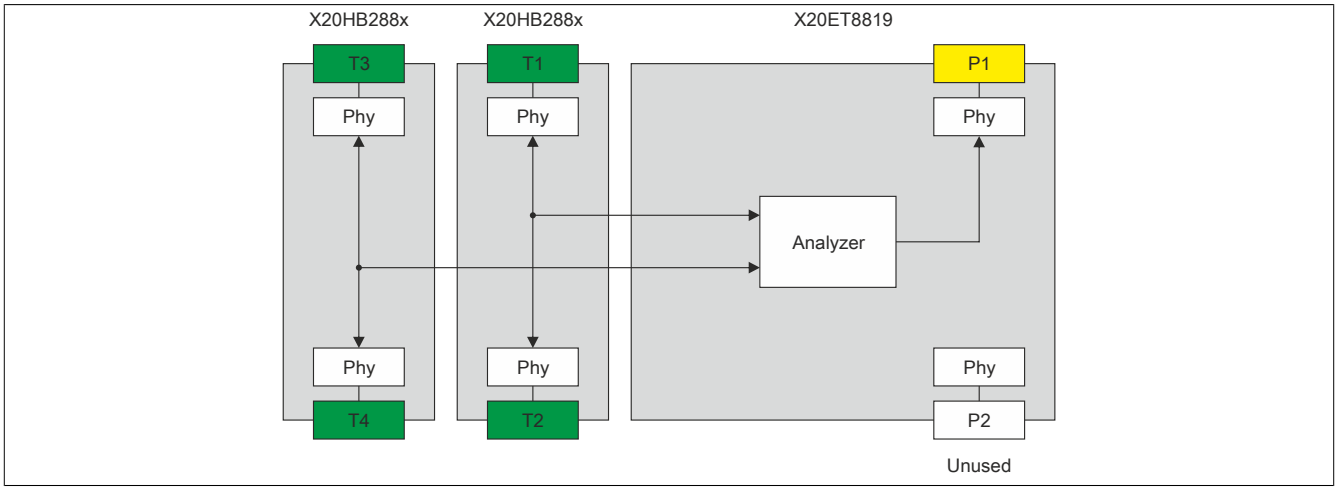


Figure 378: Diagram of hardware configuration 3b

4.24.2.13 Firmware update

To update the firmware, the webpage of the X20ET8819 module must be opened when in service mode. To do this, set the MODE switch to 0 and ADD to a value between 0x1 and 0xF. When the hardware is restarted now, the module will enter service mode. A connection can be established to the webpage using a web browser via the interface IF1 (P1) and the IP address 192.168.0.ADD. The update is started by selecting "Firmware Download".

Figure 379: Start firmware update

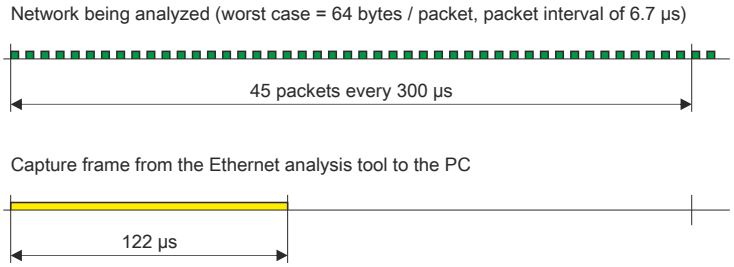
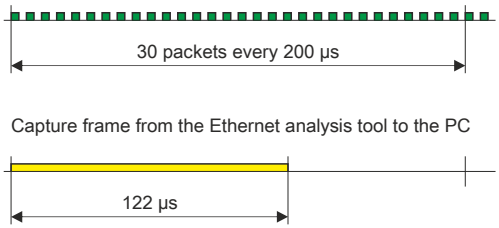
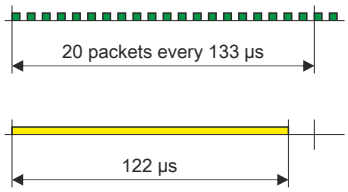
4.24.2.13.1 Firmware history

Version	Comment
1.05	Continuous product improvement for analysis mode A with frame lengths >1016 bytes.
1.04	• New analysis mode: In this mode, every package is recorded in its original size. • If two X20HB288x modules are used, data traffic on half-duplex networks can be recorded in both directions.
1.02	Support for trigger outputs: The X20DO9322 can now be used as the second I/O module.
1.00	First version

4.24.2.14 Analysis mode

Each time an incoming packet is analyzed, (see hardware configurations 1 to 3), the analysis tool saves the reception timestamp, various flags and the first 'n' bytes of data from the received packet in capture frames. These frames are sent via IF 1 (P1).

The number of recorded data bytes, 'n', is set with the operating mode switch MODE. This defines the number of packets that are sent for each capture frame.

MODE	n	p/s	Description
0	-	-	Service mode
1	24	148800	45 packets fit in a capture frame: (1514-64) / (24+8) = 45 packets 
2	40	148800	
3	64	148800	This is the first setting at which complete packets fit in the capture frame (minimum packet with 60 byte payload). 20 packets can fit in one capture frame, however this setting could cause problems on the analysis PC because there is not much idle time between the capture frames. 
4	80	128000	
5	120	88000	
6	196	56000	
7	280	40000	
8	716	16000	2 packets fit in a capture frame: (716+8)*2 + 64 = 1512 bytes A setting 'n' > 716 has the disadvantage that a network with full capacity would not be able to be analyzed.
9	24 to 1440	-	The analysis tool selects the largest possible value for 'n' itself due to the packet volume of the last capture frame that was sent. This means that each capture frame can be assigned a different 'n' value. 'n' is always a multiple of 4 and can assume values between 24 and 1440.
A	-	-	Up to a size of 1440 bytes every packet is recorded in its original size.
B - F	-	-	Reserved

Note:

- A change in the position of the MODE switch from 1 to A will be applied online during operation.
- If the S/E LED is red, then the number of bytes to be recorded should be reduced.

4.24.2.15 Using trigger inputs

The Ethernet analysis tool launches the first connected I/O module in the standard function model. The X2X link is configured with a fixed cycle of 1 ms. If this configuration contains digital input data (digital input module X20DI9371), the first 4 digital inputs will be included in the packet header.

4.24.2.15.1 Background

When looking for very complicated errors, it is usually not possible to find a trigger condition on the network. It is often difficult to discern whether the cause of the problem is even associated with the Ethernet communication or somewhere else. The fact that such errors are extremely rare makes finding them that much harder.
A permanent record of network frames through the module X20ET8819 would exceed storage capabilities of the recording software due to the large amount of data. The trigger inputs on the X20ET8819 offer an additional way to circumvent this problem. Analysis of the network can be started or stopped when a specific event occurs.

In most cases, the problem can be indicated using a digital signal. The CPU can detect errors or irregularities (e.g. failure of a network slave), for example, and then set a digital output on the local I/O bus. If this signal is connected to a digital input on the Ethernet analysis tool, then the module is able to evaluate this information and trigger a response such as pausing an active recording.

4.24.2.15.2 Evaluation of the inputs on the analysis tool X20ET8819

Input 1 - 4

The first 4 inputs will be inserted only in the packet header by the X20ET8819. The recording software from B&R (OmniPeek full version and plugin) can determine how the signals are interpreted.

Input 5 - 7

If the recording software is unable to evaluate the first 4 inputs (Wireshark, OmniPeek, various other capture tools), then inputs 5 - 7 are used to control the Ethernet analysis tool X20ET8819 directly.

Input	Name	Description
5	ExternActivate	Recording will not start automatically if this input is set to HIGH when the analysis tool is turned on. The module waits for a positive edge on input 6.
6	ExternStart	Recording begins when a positive edge occurs on this input. The value in 'captureId', offset 49 in the capture frame header is incremented to indicate to the receiving tool that a new recording has been started. When recording using the recording software from B&R, this information can be used to switch to a new ring buffer and to store the last one.
7	ExternStop	Recording stops when a negative edge occurs on this input.
8 - 12	-	Reserved

Table 541: Evaluation of inputs 5 - 7 on the analysis tool

Example 1

A drive is started one time each minute. After 10 to 30 hours, a problem arises on a network station shortly after starting the drive. To analyze the error, the Ethernet communication is recorded between when the start command is issued and when the error occurs.

Problems:

Due to the large amount of data it is not possible to record the entire 30 hours. Someone would have to stay on the analysis PC the whole time to stop recording when the error occurs.

Solution:

Input	Description
ExternActivate	Input permanently wired to 24 VDC = Activates the external trigger function
ExternStart / ExternStop	Connect both inputs to the same digital output that the master uses to notify the X20ET8819 when to start and stop recording. The master can, for example, always set the output before the drive start command and reset it as soon as the startup has been completed. When the master detects an error, it only has stop setting the output. This would mean that after 30 hours the recording is certain to contain the time period in which the error occurred and as well as a few prior recordings of proper startups for comparison.

Table 542: Function of the inputs in Example 1

Example 2

A system containing multiple X20 I/O systems on the POWERLINK network is experiencing sporadic failures. An I/O slave suddenly fails for no apparent reason after running properly for a long time. To analyze whether the failure is network related, the time before the failure must be recorded.

Problems:

The master has no indication as to when and why the problem occurs. That means there is no start condition for the recording. Someone would have to stay on the analysis PC the whole time to stop recording when the error occurs.

Solution:

Input	Description
ExternActivate	Input permanently wired to 24 VDC = Activates the external trigger function
ExternStart	Input permanently wired to 24 VDC = Ensures that the recording starts immediately when the X20ET8819 is turned on
ExternStop	Connect input to a digital output on the affected I/O slave, which is permanently set to 1 by the program. As soon as the slave fails the first time and resets the digital outputs, recording is stopped by the negative edge on ExternStop and is not started again.

Table 543: Function of the inputs in Example 2

4.24.2.16 Using trigger outputs

Output	Name	Description
1	FrameError	As soon as a frame error (CRC, Oversize, Preamble, Noise or Alignment) occurs, this output is set for 10 ms.
2 - 12	-	Reserved

Table 544: Using trigger outputs in the event of an error

4.24.2.17 B&R recording software

The recording plug-in (for WildPackets OmniPeek™) to decode the capture frames is available for download in the Download section on the B&R homepage.

B&R provides the following free recording software for the module in the Downloads section of the B&R website:

- Ethernet Analyzer Plugin for Wildpackets OmniPeek™
- B&R Network Analyzer (stand-alone solution)

4.24.3 X20(c)HB8815

4.24.3.1 General information

The POWERLINK TCP/IP gateway enables the exchange of all types of application data (HMI, diagnostics, parameter data, etc.) between a POWERLINK V2 network and a TCP/IP network. It functions like a layer 2 switch, with the exception that cyclic POWERLINK packets are not routed to the ETH port.

With respect to the functionality of layer 2 switches, it should be mentioned that the gateway uses the store-and-forward principle. Gateway functionality doesn't need to be configured separately.
When the gateway receives a frame, it saves the MAC address of the sender and the corresponding interface in the source address table (SAT). If the destination address is found in the SAT, the gateway routes the frame to the corresponding interface. Frames with a broadcast or multicast address are always routed to all interfaces.

When IP packets are received at the "ETH" port that are larger than the MTU configured for POWERLINK, they are fragmented, if permitted.

- "ETH" port: Interface for TCP/IP network
- "PLK" port: Interface for POWERLINK network

> **Information:**
>
> **I/O modules cannot be operated with the X20HB8815.**
> **POWERLINK V1 is not supported.**

POWERLINK is a standard protocol for Fast Ethernet with hard real-time properties. The Ethernet POWERLINK Standardization Group (EPSG) (see www.ethernet-powerlink.org).

The bus modules expanded to the left allow connection of up to 2 hub expansion modules in addition to the gateway. This means that a basic device provides up to 2 POWERLINK ports.

- POWERLINK
- Up to 2 slots for hub expansion modules
- 3x / 5x POWERLINK hub

4.24.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

> **For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.**

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.24.3.3 Order data

Model number	Short description	Figure
	X20 hub system	
X20HB8815	X20 POWERLINK - TCP/IP gateway, can be expanded with active hub modules, 2x RJ45	
X20cHB8815	X20 POWERLINK - TCP/IP gateway, coated, can be expanded with active hub modules, 2x RJ45	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for the X20 hub system	
X20PS8002	X20 power supply module for standalone hub and compact link selector	
X20cPS8002	X20 power supply module, coated, for standalone hub and compact link selector	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	System modules for the X20 hub system	
X20HB1881	X20 hub expansion module, integrated 1-port hub, for fiber optic cable	
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45	
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable	
X20cHB1881	X20 hub expansion module, coated, integrated 1-port hub, for fiber optic cable	
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45	
X20cHB2881	X20 hub expansion module, coated, integrated 2-port hub, for fiber optic cable	

Table 545: X20HB8815, X20cHB8815 - Order data

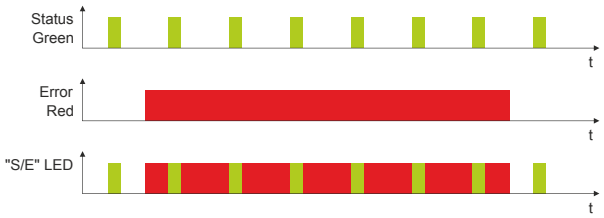
4.24.3.4 Technical data

Product ID	X20HB8815	X20cHB8815
Short description		
Gateway	POWERLINK controlled node with up to 2 slots for hub expansion modules	
General information		
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED and software	
Bus function	Yes, using status LED and software	
Power consumption	2 W	
Electrical isolation		
Fieldbus - Supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Type	POWERLINK gateway	
Design	2x RJ45, shielded	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate		
POWERLINK	100 Mbit/s	
TCP/IP	10/100 Mbit/s	
Transmission		
POWERLINK		
Physical layer	100 BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
TCP/IP		
Physical layer	10 BASE-T/100 BASE-TX	
Half-duplex	Yes	
Full-duplex	Yes	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS8002 supply module separately Order 1x X20BB8x bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS8002 power supply module separately Order 1x X20cBB8x bus base separately
Spacing [2]		
X20BB80	37.5 $^{+0.2}$ mm	
X20BB81	62.5 $^{+0.2}$ mm	
X20BB82	87.5 $^{+0.2}$ mm	

Table 546: X20HB8815, X20cHB8815 - Technical data

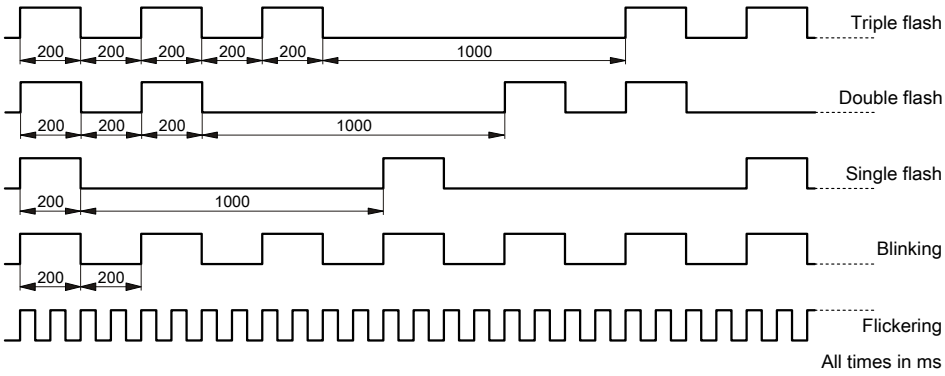
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Spacing is based on the width of the X20BB80 bus base. Up to two X20HB2880 or X20HB2881 hub expansion modules and one X20PS8002 supply module are also always required for the gateway.

4.24.3.5 LED status indicators

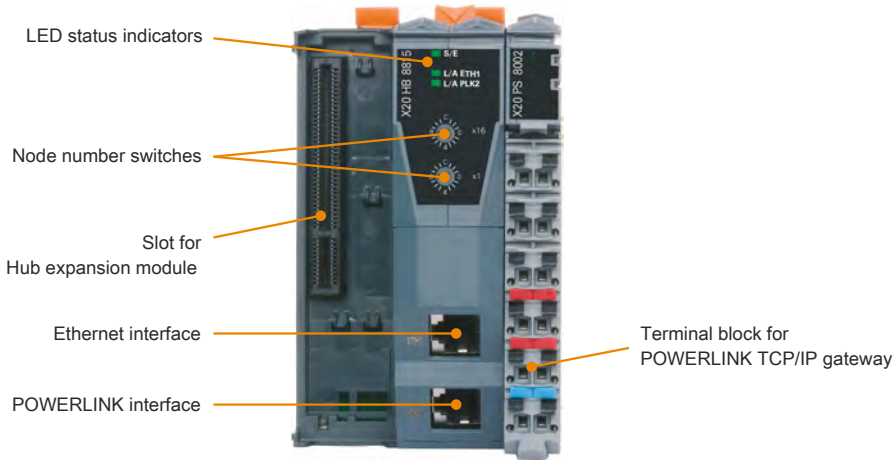
Figure	LED	Color	Status	Description
	S/E[1]	Green	Off	No power supply or mode is NOT_ACTIVE. The controlled node (CN) is either not getting power, or it is in the NOT_ACTIVE state. The CN waits in this state for about 5 seconds after a restart. Communication is not possible with the module. If no POWERLINK communication is detected during these 5 seconds, the CN goes into the BASIC_ETHERNET state (flickering). If POWERLINK communication is detected before this time passes, however, the CN goes directly into the PRE_OPERATIONAL_1 state.
			Flickering	BASIC_ETHERNET mode. The CN has not detected any POWERLINK communication. It is possible to communicate directly with the CN in this state (e.g. with UDP, IP, etc.). If POWERLINK communication is detected while in this state, the CN goes into the PRE_OPERATIONAL_1 state.
			Single flash	PRE_OPERATIONAL_1 mode. When operated on a POWERLINK V1 manager, the CN goes directly into the PRE_OPERATIONAL_2 state. When operated on a POWERLINK V2 manager, the CN waits until an SoC frame is received and then goes into the PRE_OPERATIONAL_2 state.
			Double flash	PRE_OPERATIONAL_2 mode. The CN is normally configured by the manager in this state. Issuing a command (POWERLINK V2) or setting the data valid flag in the output data (POWERLINK V1) then switches to the READY_TO_OPERATE state.
			Triple flash	READY_TO_OPERATE mode. In a POWERLINK V1 network, the CN automatically switches to the OPERATIONAL state as soon as input data is present. In a POWERLINK V2 network, the manager switches to the OPERATIONAL state by issuing a command.
			On	OPERATIONAL mode. PDO mapping is active and cyclic data is being evaluated.
			Blinking	STOPPED mode. No output data is produced or input data supplied. It is only possible to enter or leave this state after the manager has given the appropriate command.
		Red	On	The controlled node (CN) is in an error state (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, then the green LED blinks over the red LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: • The LED blinks red several times immediately after startup. This is not an error. • The LED is lit red for CNs with configured physical node number 0 but that have not yet been assigned a node number via Dynamic Node Allocation (DNA).
	L/A IFx	Green	On	A link to the peer station has been established (TCP/IP network).
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus
	L/A PLK2	Green	On	A link to the peer station has been established (POWERLINK network).
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus

1) The Status/Error LED "S/E" is a green/red dual LED.

Status LED - Blinking patterns



4.24.3.6 Operating and connection elements



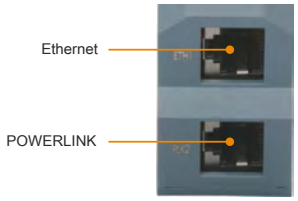
4.24.3.7 POWERLINK node number switches

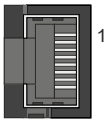
The node number for a POWERLINK station is set using its two number switches.

Switch position	Description
0x00	Reserved, switch position not permitted
0x01 - 0xEF	Node number of the POWERLINK node. Operation as controlled node.
0xF0 - 0xFF	Reserved, switch position not permitted

4.24.3.8 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

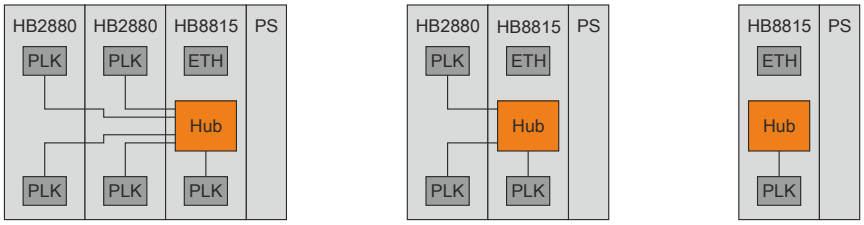
4.24.3.9 Slot for hub expansion modules

Depending on the bus base, up to 2 hub expansion modules can be installed on the left side of the module:

Bus base	Slots for hub expansion modules
X20BB81	1
X20BB82	2

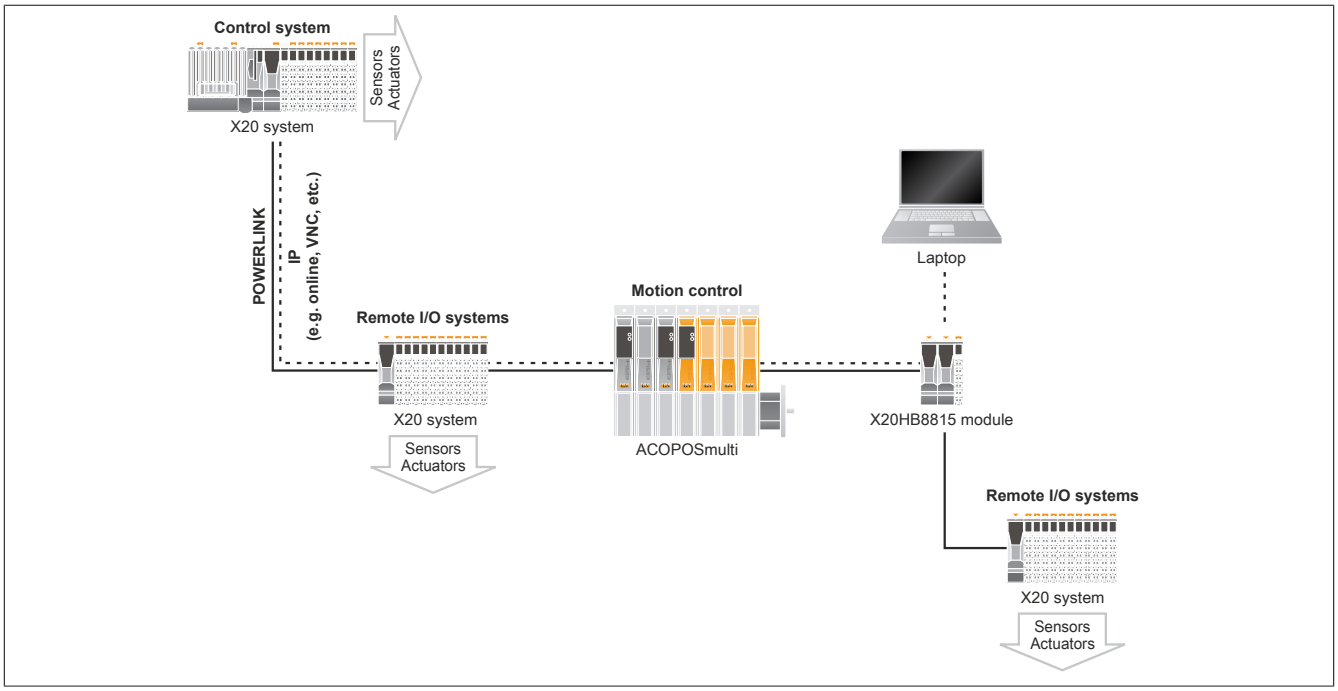
Table 547: Slots for hub expansion modules for various bus bases

The hub expansion module for the gateway is a 2x hub, which allows the gateway to be expanded into a 5x POWERLINK hub.

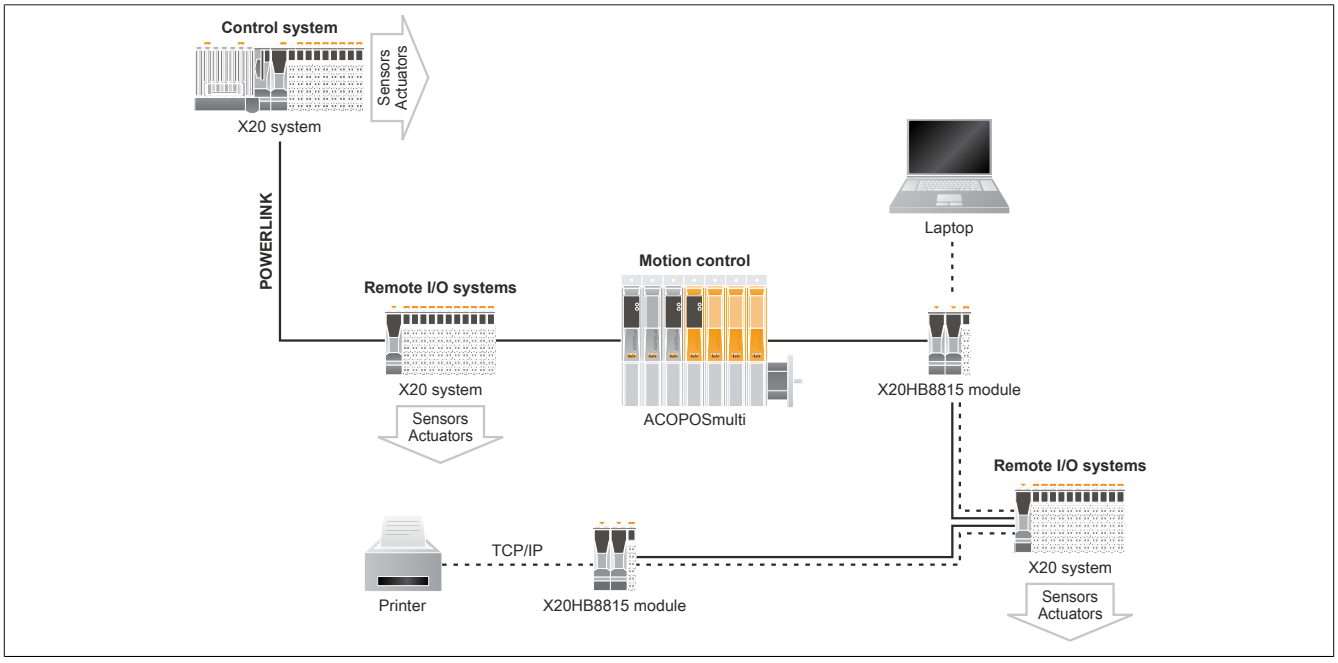


4.24.3.10 Usage examples

Example 1: Online connection with Automation Studio via POWERLINK



Example 2: Use the POWERLINK network for TCP/IP services



4.24.3.11 SG3

This module is not supported on SG3 targets.

4.24.3.12 Firmware

This module comes with preinstalled firmware. The firmware is a component of Automation Studio. The module is automatically updated to this version.

To update the firmware included in Automation Studio, the hardware must be upgraded (see "Project management" / "Automation Studio upgrade" in the help system).

When using a 3rd-party device as a POWERLINK manager, the firmware update can be performed via the integrated Web server.

4.24.3.13 MTU size

Automatic MTU configuration is currently not supported. The MTU size is set to 300 (default value).

The MTU can be set manually under "Asynchronous Optimization" -> "Local ASnd MTU" in the I/O configuration of the module.

4.24.3.14 Asynchronous send priority

If needed, a higher asynchronous send priority can be assigned to the module. The setting for this is made in the I/O configuration of the module under "Asynchronous Optimization" -> "Asynchronous Send Priority".

Information:

If the priority is set too high, it is possible in some circumstances that other POWERLINK stations cannot send their asynchronous data on time.

4.24.4 X20(c)HB8880

4.24.4.1 General information

The X20 hub is a device that can be used universally in standard Ethernet networks or POWERLINK networks. It is suitable for 100 Mbit/s (Fast Ethernet) networks.

The bus modules expanded to the left allow connection of up to 2 hub expansion modules in addition to the hub base module. This means that a single base device provides up to 6 hub interfaces.

- 2x / 4x / 6x Fast Ethernet hub
- Modular construction
- Easily expandable

4.24.4.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.24.4.3 Order data

Model number	Short description	Figure
	X20 hub system	
X20HB8880	X20 base hub module, integrated 2-port hub, 2x RJ45	
X20cHB8880	X20 base hub module, coated, integrated 2-port hub, 2x RJ45	
	Required accessories	
	System modules for bus controllers	
X20BB80	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included	
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for the X20 hub system	
X20PS8002	X20 power supply module for standalone hub and compact link selector	
X20cHB1881	X20 hub expansion module, coated, integrated 1-port hub, for fiber optic cable	
X20cPS8002	X20 power supply module, coated, for standalone hub and compact link selector	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	System modules for the X20 hub system	
X20HB1881	X20 hub expansion module, integrated 1-port hub, for fiber optic cable	
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45	
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable	
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45	
X20cHB2881	X20 hub expansion module, coated, integrated 2-port hub, for fiber optic cable	

Table 548: X20HB8880, X20cHB8880 - Order data

4.24.4.4 Technical data

Product ID	X20HB8880	X20cHB8880
Short description		
Hub	Modular X20 hub with up to 2 slots for hub expansion modules:	
General information		
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED	
Bus function	Yes, using status LED	
Power consumption	2 W	
Electrical isolation		
Fieldbus - Supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Interfaces		
Type	Hub base module	
Design	2x shielded RJ45	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100 BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS8002 power supply module separately Order 1x X20BB8x bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS8002 supply module separately Order 1x X20cBB8x bus base separately
Spacing [2]		
X20BB80	37.5 $^{+0.2}$ mm	
X20BB81	62.5 $^{+.02}$ mm	
X20BB82	87.5 $^{+0.2}$ mm	

Table 549: X20HB8880, X20cHB8880 - Technical data

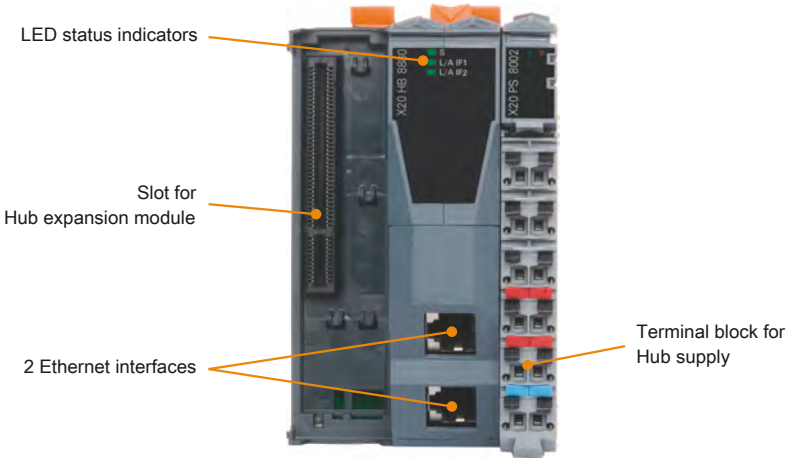
1) Ta min.: 0°C
Ta max.: See environmental conditions

2) Spacing is based on the width of the X20BB80 bus base. Up to two X20HB2880 hub expansion modules and one X20PS8002 supply module are also always required for the hub.

4.24.4.5 LED status indicators

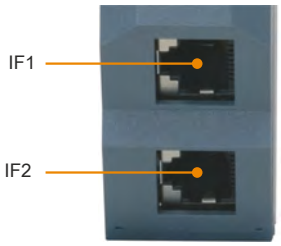
Figure	LED	Color	Status	Description
	S	Green	On	Hub is active
	L/A IFx	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus.

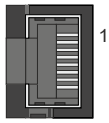
4.24.4.6 Operating and connection elements



4.24.4.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



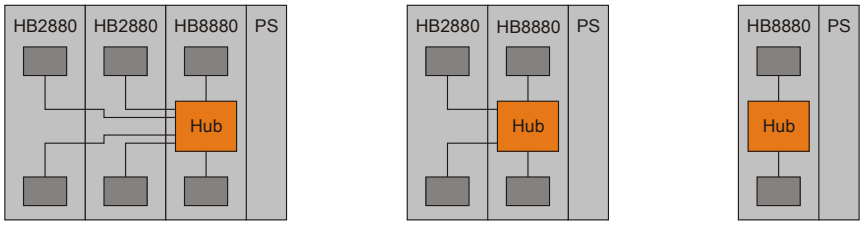
Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.24.4.8 Slot for hub expansion modules

Depending on the bus base, up to 2 hub expansion modules can be installed on the left side of the X20 hub:

Bus base	Slots for hub expansion modules
X20BB81	1
X20BB82	2

The hub expansion module is a 2x hub, which allows the hub base module to be expanded into a 6x hub.



6x with X20BB82 4x with X20BB81 2x with X20BB80

4.24.5 X20HB88G0

4.24.5.1 General information

The X20BB81 bus module has an expansion slot on the left side, and therefore the X20HB88G0 junction base module has an additional slot available for an X20HB28G0 EtherCAT junction module. This means that a single base device provides 4 interfaces.

- 4x EtherCAT junction base module

4.24.5.2 Order data

Model number	Short description	Figure
	X20 hub system	
X20HB88G0	X20 EtherCAT junction base module integr. 2x EtherCAT junction, 2x RJ45 connection	
	Required accessories	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for the X20 hub system	
X20HB28G0	X20 EtherCAT junction module, integrated 2-port EtherCAT junction, 2x RJ45	
X20PS8002	X20 power supply module for standalone hub and compact link selector	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 550: X20HB88G0 - Order data

4.24.5.3 Technical data

Product ID	X20HB88G0
Short description	
Junction module	X20 EtherCAT junction base module with one slot for 1 junction module
General information	
Status indicators	Module status, bus function
Diagnostics	
Module status	Yes, using status LED and software
Bus function	Yes, using status LED and software
Power consumption	1.79 W
Electrical isolation	
Fieldbus - Supply	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Type	EtherCAT junction base module
Design	2x RJ45, shielded
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100 BASE-TX
Half-duplex	Yes
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Hub runtime	750 ns 2)
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS8002 supply module separately Order 1x X20BB81 bus base separately
Spacing 3)	62.5 $^{+0.2}$ mm

Table 551: X20HB88G0 - Technical data

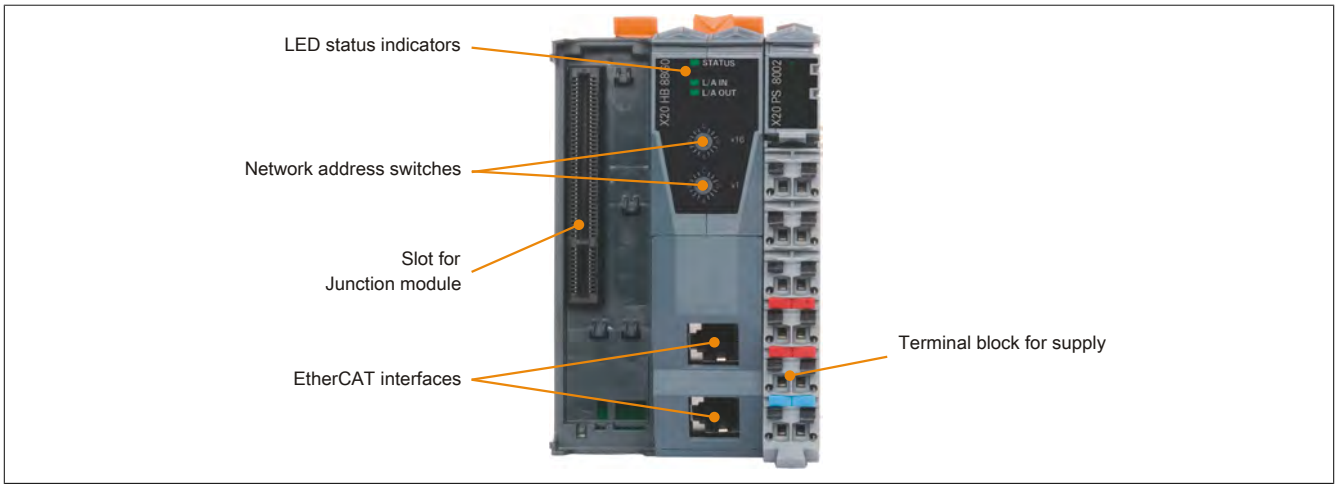
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) For the interfaces on the X20HB28G0 EtherCAT junction module, the hub runtime is 1.1 µs instead of 750 ns.
3) Spacing is based on the width of the X20BB80 bus base. One X20HB28G0 junction module and one X20PS8002 supply module are also always required for the base module.

4.24.5.4 LED status indicators

Figure	LED	Color	Status	Description
	STATUS[1]	Green	On	Junction base module is in OPERATIONAL mode.
			Blinking	PREOPERATIONAL mode
			1 pulse	SAFE OPERATIONAL mode
			Flickering	The junction base module has started and is not yet in INIT mode or it is in BOOTSTRAP mode (e.g. while downloading firmware).
			Off	INIT mode
		Red	On	A critical communication or application error has occurred.
			Blinking	Invalid configuration data
			1 pulse	The junction base module has an internal error and changed the EtherCAT status on its own
			2 pulses	Watchdog timeout (process data watchdog or EtherCAT watchdog)
			Flickering	Error in the start procedure (INIT mode has been achieved, but the error indicator bit in the AL status register is set)
			Off	No error
	L/A IN L/A OUT	Green	Blinking	The respective LED blinks when Ethernet activity is present (PORT OPEN) on the corresponding interface.
			On	Connection (link) established, however no communication (PORT OPEN).
			Off	No physical Ethernet connection exists (PORT CLOSED).

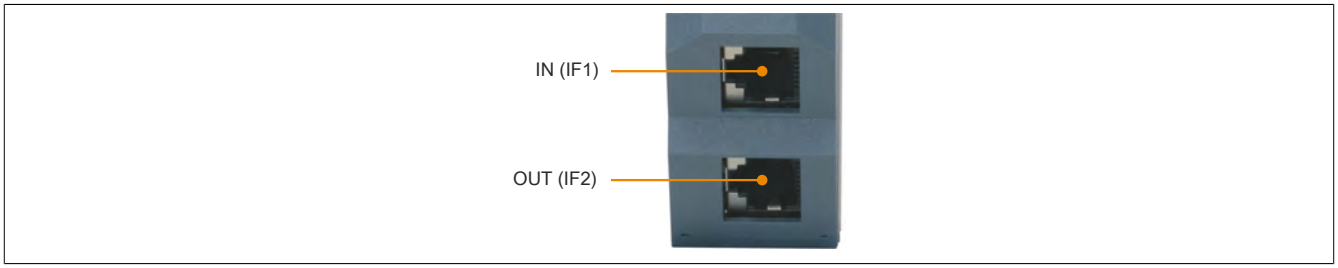
1) The Status LED is a green/red dual LED.

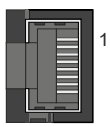
4.24.5.5 Operating and connection elements



4.24.5.6 EtherCAT interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	TXD	Transmit data
	2	TXD\	Transmit data\
	3	RXD	Receive data
	4	Termination	
	5	Termination	
	6	RXD\	Receive data\
	7	Termination	
	8	Termination	

4.24.5.7 Network address switch

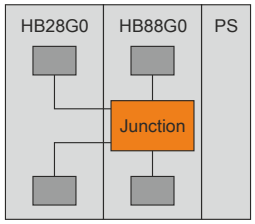
A slave alias address can be set using the two network address switches on the base module. During the initialization phase (during startup), the base module writes the value of the address switch to the ESC register 0x12 or 0x13. However, the value is only accepted in the register if the value of the switch value is between 0x00 and 0xFA (decimal 250).

Switch position	Description
0x00 to 0xFA	Writes the address switch value to the "Station Alias" register.
0xFB to 0xFE	Address switch value not used. ESC Alias registers not changed.
0xFF	Address switch value not used. ESC Alias registers not changed. The base module boots with the default values if the address switch is set to the value "0xFF" before a restart. All set parameters remain unchanged in flash memory.

The master determines whether the alias address is used for the slave addressing by setting the corresponding bit in the ESC DL control register (bit 24).

4.24.5.8 Slot for EtherCAT junction module

The junction base module is equipped with an additional slot. The X20HB28G0 EtherCAT junction module is operated on this slot, providing 4 additional interfaces.



4x with X20BB81

4.25 Motor controllers

The motor controllers offer extensive possibilities for controlling motors, valves or resistive loads and are particularly well suited for controlling brush DC motors. Each output is assigned a status LED.

4.25.1 Brief information

Product ID	Short description	on page
X20MM2436	X20 PWM motor module, 24 to 39 VDC ±25%, 2 PWM motor bridges, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, configurable as incremental encoder	2318
X20MM3332	X20 digital motor module, 24 VDC, 3 digital outputs, full bridge (H bridge), 3 A continuous current, 5 A peak current	2338
X20MM4331	X20 digital motor module, 24 VDC, 4 digital outputs, half bridge, 3 A continuous current, 5 A peak current	2353
X20MM4456	X20 PWM motor module, 24 to 48 VDC ±25%, 4 PWM motor bridges, 6 A continuous current, 10 A peak current, 4x 4 digital inputs 24 VDC, sink, configurable as incremental encoder	2366
X20SM1426	X20 stepper motor module, 1 motor connection, 1 A continuous current, 1.2 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder	2387
X20SM1436	X20 stepper motor module, module supply 24-39 VDC ±25%, 1 motor connection, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder	2432

4.25.2 X20MM2436

4.25.2.1 General information

The motor bridge module is used to control 2 DC motors with a nominal voltage of 24 to 39 VDC ±25% at a nominal current up to 3 A. The module can be reconfigured and used in current controller mode for controlling inductive loads. The module is also equipped with 4 digital inputs, which can be used as incremental counters. Each motor is controlled with a full-bridge (H-bridge). This enables the motors to be moved in both directions.

- 2x outputs (H bridge) with PWM control and 24 to 39 VDC ±25% supply
- 3 A nominal current (3.5 A max current)
- 15 Hz to 50 kHz frequency, 16-bit
- Frequency mode with 10 to 6553.5 Hz or 1 to 655.35 Hz resolution.
- PWM resolution, 15-bit + sign, minimum 10 ns
- Configurable dither
- 2x 2 inputs 24V, can be configured as AB
- Sink connection
- 1-wire connections

4.25.2.2 Order data

Model number	Short description	Figure
	Motor controllers	
X20MM2436	X20 PWM motor module, 24 to 39 VDC ±25%, 2 PWM motor bridges, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, configurable as incremental encoder	
	Required accessories	
	Bus modules	
X20BM31	X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 552: X20MM2436 - Order data

4.25.2.3 Technical data

Product ID	X20MM2436
Short description	
I/O module	2-channel PWM motor bridge, 2 AB incremental encoders
General information	
B&R ID code	0x26B5
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Output	Yes, using status LED and software
I/O supply	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	-
External I/O	
24 VDC	2.45 W
48 VDC	3.15 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Digital inputs	
Quantity	4
Nominal voltage	24 VDC
Input voltage	24 VDC (-15% / +20%)
Input current at 24 VDC	Approx. 1.3 mA
Input filter	
Hardware	<5 µs
Software	-
Connection type	1-wire connections
Input circuit	Sink
Additional functions	2x AB incremental encoder, 1x ABR counter, 2x event counter, 2x period duration/gate measurement
Input resistance	Typ. 18 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
AB incremental encoder	
Quantity	2
Encoder inputs	24 V, asymmetrical
Counter size	16-bit
Input frequency	Max. 50 kHz
Evaluation	4x
Signal form	Square wave pulse
PWM output	
Quantity	2
Nominal voltage	24 to 39 VDC ±25%
Nominal current	3 A
Maximum current	3.5 A (2 s)
PWM frequency	
Standard operating mode (PWM/current)	15 Hz to 50 kHz
Frequency operating mode	1 Hz to 6553.5 Hz
Actuator supply	
Supply	External
Fuse	Required line fuse: Max. 10 A, slow-blow
Output protection	Thermal cutoff for overcurrent and short circuit
Design	H bridge
Configurable dither	Amplitude, frequency
Period duration resolution (PWM/current operating mode)	16-bit, min. 20 µs
Frequency resolution (frequency operating mode)	
0.1 Hz scaling	<3000Hz: 0.1 Hz; 3000 Hz to 6553.5 Hz: 0.1 Hz to 0.4 Hz
0.01 Hz scaling	<300 Hz: 0.01 Hz; 300 Hz to 655.35 Hz: 0.01 to 0.04 Hz
Phase shift PWM1 to PWM2	180° - if possible (according to operating mode)
DC bus capacitance	100 µF

Table 553: X20MM2436 - Technical data

Product ID	X20MM2436
PWM pulse width	
PWM mode	15-bit + sign ≥10 ns
Current mode	15-bit + sign ≥10 ns
Frequency mode	15-bit + sign ≥10 ns
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 50°C
Vertical installation	Not permitted
Derating	See section "Derating"
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM31 bus module separately
Spacing	$25^{+0.2}$ mm

Table 553: X20MM2436 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.25.2.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green		Input state of the corresponding digital input
	M1, M2	Orange	On	Output 1 or 2 is active

1) Depending on the configuration, a firmware update can take up to several minutes.

4.25.2.5 Pinout

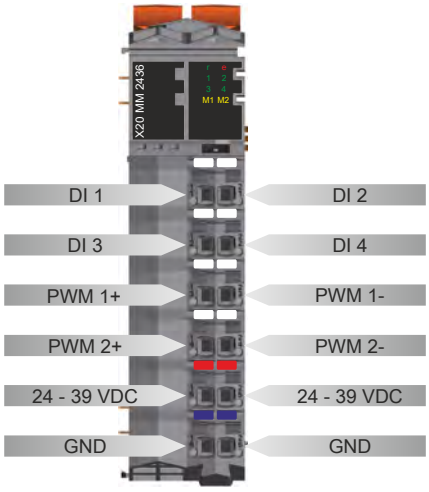
In accordance with the EN60204-1 standard, a cable cross section of 0.75 mm² or larger must be used for the motor outputs in order to handle the maximum motor current of 3.5 A. To ensure full motor power, voltage drops that could result from the cable length and the electrical connections must also be taken into consideration when selecting the attachment cable.

Warning!

The terminal block is not permitted to be plugged in or unplugged during operation.

Information:

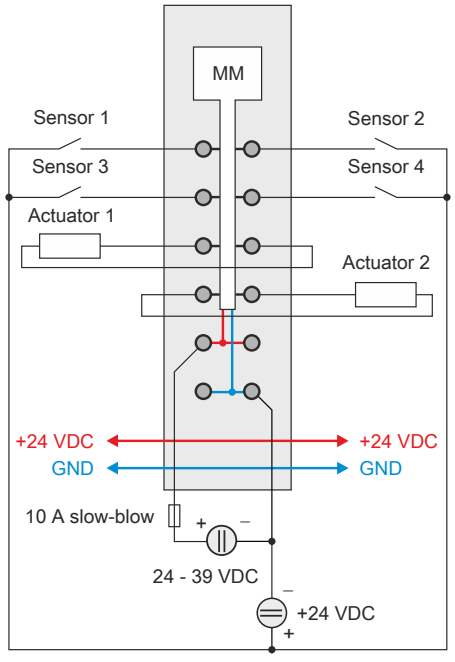
Shielded motor cables must be used in order to meet the limits according to the EN55011 standard (emissions).



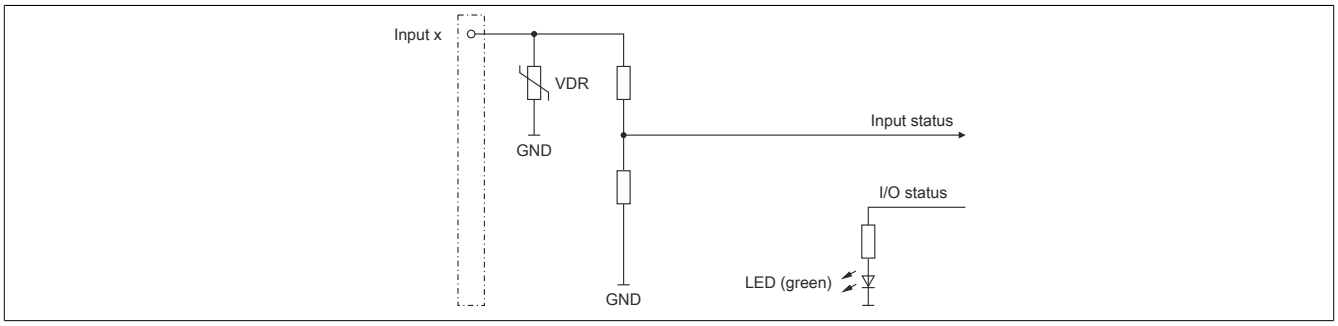
4.25.2.6 Connection example

Information:

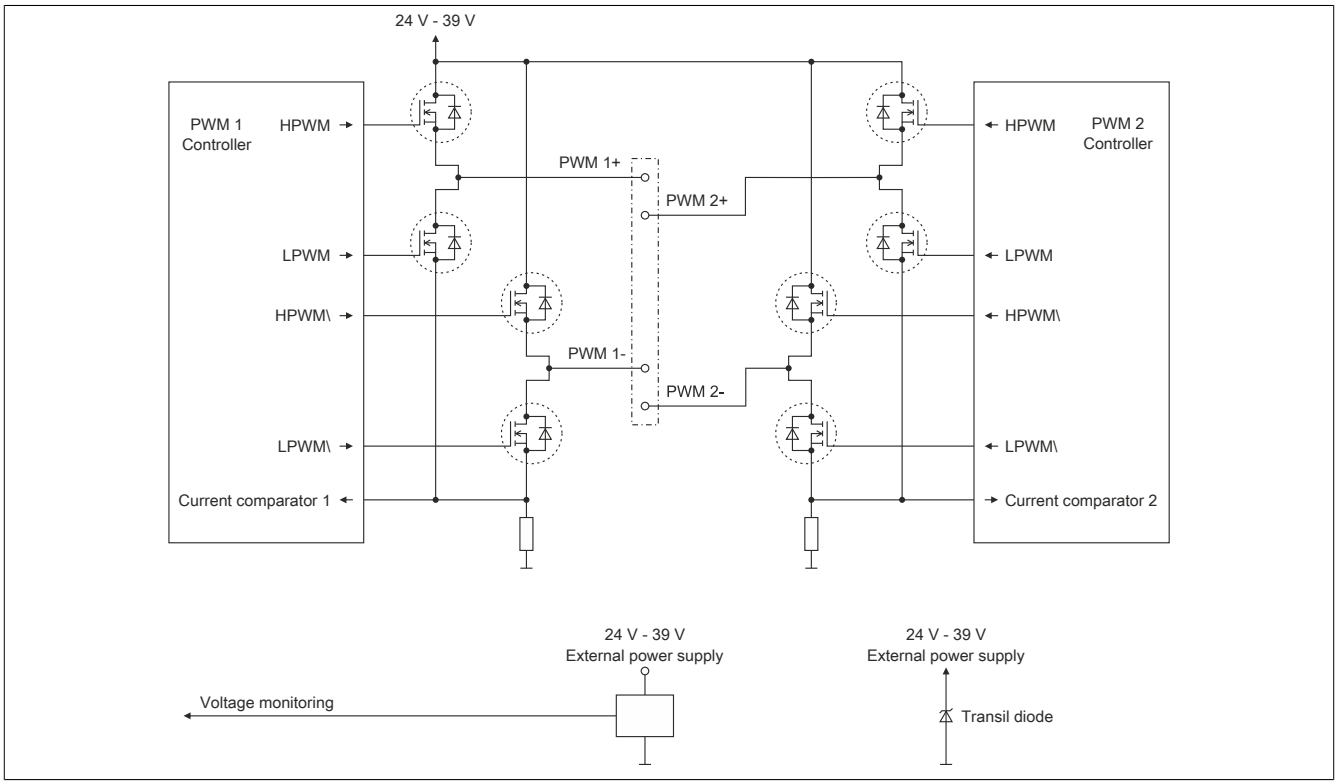
This module can only be operated if supplied with power via the terminal block.



4.25.2.7 Input circuit diagram



4.25.2.8 Output circuit diagram



4.25.2.9 Protection

The power supply line should be protected by a circuit breaker or a fuse. In general, dimensioning the supply line and overcurrent protection depends on the structure of the power supply (modules can be connected individually or in groups).

Information:

The effective current for the power supply depends on the load but is always less than the motor current. Make sure the maximum nominal current of 7 A is not exceeded on the power supply terminals of the power element.

When choosing a suitable fuse, the user must also account for characteristics such as aging effects, temperature derating, overcurrent capacity and the definition of the rated current, which can vary by manufacturer and type. In addition, the fuse that is selected must also be able to handle application-specific characteristics (e.g. overcurrent that occurs in acceleration cycles).

The cross section of the power mains and the rated current of the overcurrent protection used are chosen according to the current load so that the maximum current load for the cable cross section selected (based on the type of wiring, see table) is greater than or equal to the current load in the power mains. The rated current of the overcurrent protection must be less than or equal to the maximum current load for the cable cross section selected (based on the type of wiring, see table):

I_{Mains}	≤	I_b	≤	I_Z
Mains	≤	Fuse	≤	Line/cable

Wire cross section [mm²]	Maximum current load for cable cross section I_Z / rated current for overcurrent protection I_b [A] depending on the type of wiring at an ambient air temperature of 40°C in accordance with IEC 60204-1			
	B1	B2	C	E
1.5	13.5 / 13	13.1 / 10	15.2 / 13	16.1 / 16
2.5	18.3 / 16	16.5 / 16	21 / 20	22 / 20

Table 554: Cable cross section of the mains supply line depending on the type of wiring

The tripping current of the fuse must not exceed the rated current for overcurrent protection I_b.

Type of wiring	Description
B1	Wires in conduit or cable duct
B2	Cables in conduit or cable duct
C	Cables or wires on walls
E	Cables or wires on open-ended cable tray

Table 555: Type of wiring used for the mains supply line

4.25.2.10 Derating

To ensure proper operation, the following items must be taken into consideration:

- The sum of the square of both effective currents (I_N , peak value must not exceed 3 A) must not exceed 9 A². The boost current of 3.5 A for 2 seconds is an exception.
- Modules next to the motor module can have a maximum power consumption of 1.0 W.
- The derating values listed below must be taken into consideration

Example calculations

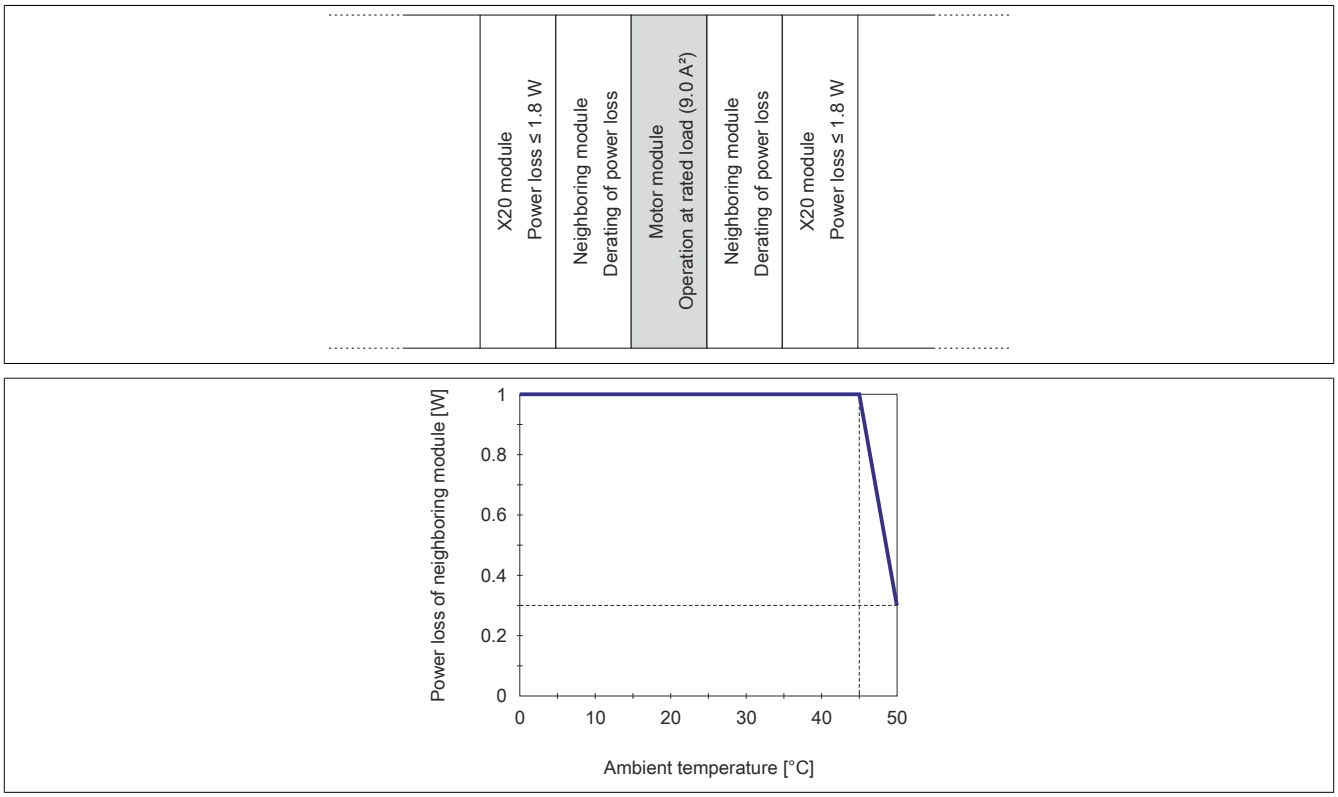
In the following examples, the calculation of I_N^2 is used to check if the current operating state is permitted.

Output current		I_N^2	Operating state permitted
PWM 1	PWM 2		
3.0 A	0 A	$I_N^2 = 3\ A \cdot 3\ A + 0\ A \cdot 0A = 9\ A^2$	Yes
2.1 A	2.1 A	$I_N^2 = 2.1\ A \cdot 2.1\ A + 2.1\ A \cdot 2.1\ A = 8.82\ A^2$	Yes
2.8 A	2.0 A	$I_N^2 = 2.8\ A \cdot 2.8\ A + 2\ A \cdot 2\ A = 11.84\ A^2$	for max. 2 s[1)]

1) The cooling time, which means operation <9 A², must be at least 5 times as long as the time of the overload.

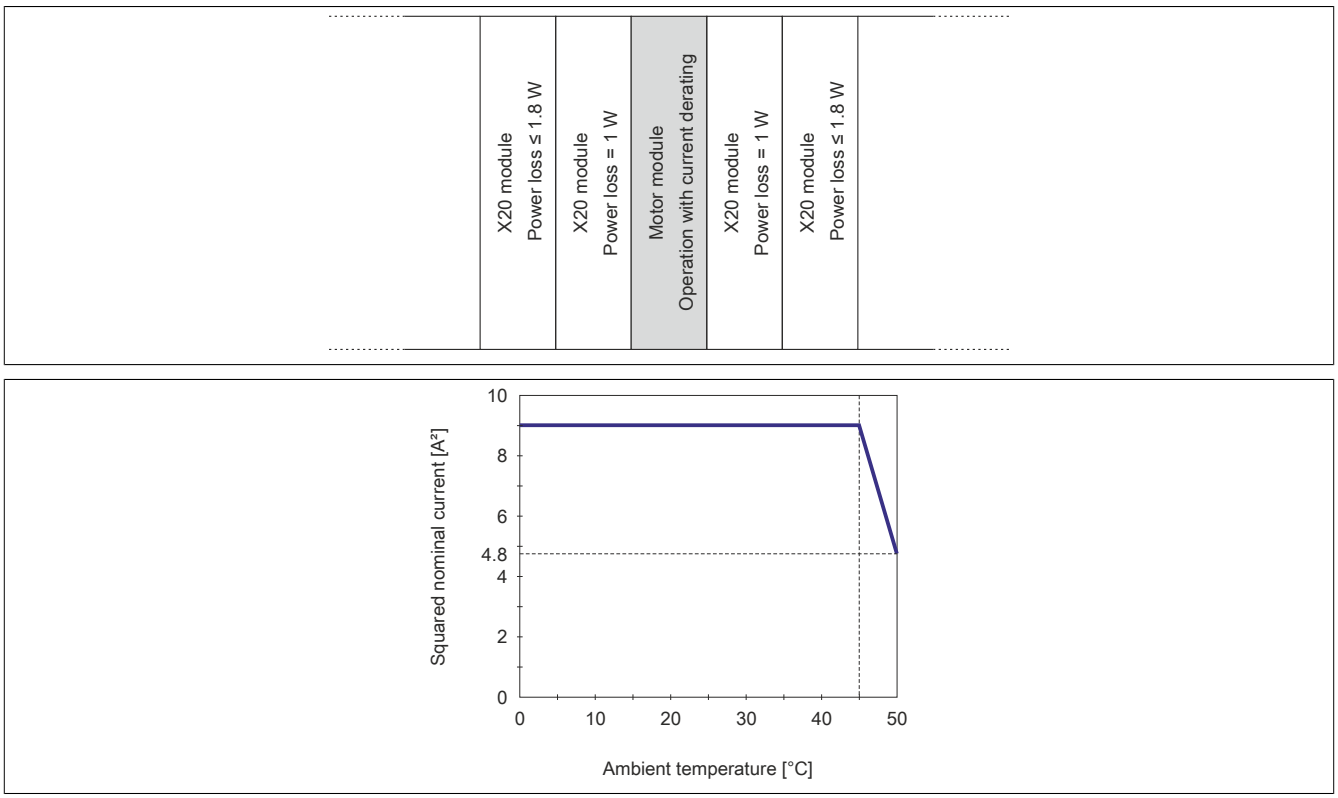
Power loss derating for neighboring modules

Modules directly next to the motor module can have a power loss of 1.0 W. If the motor module is operated with the rated load over the entire temperature range (9.0 A²), a derating for power loss of the neighboring modules must be adhered to starting at 45°C.



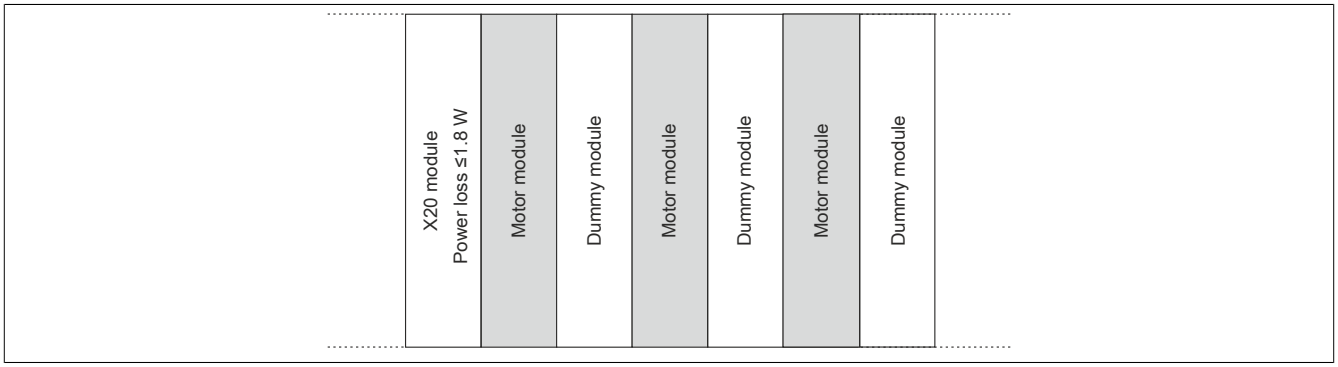
Current derating of the motor module

If the power loss of the neighboring modules to the motor module is 1.0 W, then the current of the motor module must be derated starting at 45°C.



Hardware configuration for multiple motor modules

If three or more motor modules are operated in a cluster, a dummy module must be inserted between the motor modules. There is no derating in this configuration.



4.25.2.11 Monitoring the module supply

The module supply is continually monitored (with firmware Version 3 or higher). If the following limits are exceeded in either direction, an error bit is set.

Upper limit:	>50 V
Lower limit:	<18 V

4.25.2.12 Overvoltage cutoff

If the supply voltage on the module exceeds 50V (e.g. through feedback during generator operation), then both PWM outputs are disabled (PWM output pins are shorted). The outputs are reactivated as soon as the supply voltage is back in the valid range. Switching the outputs on again can cause an open load error in current mode (depending on the current setpoint and load inductance) as well as with any other abrupt change to the current setpoint value.

4.25.2.13 Overtemperature cutoff (at 85°C)

If the module temperature reaches or exceeds the limit value of 85°C, then the module executes the following actions:

- Setting the "overtemperature" error bit
- The PWM outputs are disabled (short-circuited)

Once the module temperature sinks to 83°C, the error bit is automatically cleared by the module and the outputs become operational again.

4.25.2.14 Register description

4.25.2.14.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.25.2.14.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
"Standard PWM/current mode" operating mode only						
12	PeriodDurationPWM01PWM02	UINT			●	
14	PulseWidthCurrentPWM01	INT			●	
16	PulseWidthCurrentPWM02	INT			●	
18	ConfigOutput01	USINT				●
20	ConfigOutput02	USINT				●
31	DecayConfig[1]	USINT				●
"Frequency mode 1 and 2" operating mode only[2]						
12	FrequencyPWM01PWM02	UINT			●	
	DutyCyclePWM01PWM02	INT				
14	DutyCyclePWM01	INT			●	
	FrequencyPWM01	UINT				
16	DutyCyclePWM02	INT			●	
	FrequencyPWM02	UINT				
All operating modes						
30	ConfigOutput03	USINT				●
38	CounterConfig01[3]	USINT				●
39	CounterConfig02[3]	USINT				●
Communication						
All operating modes						
0	Counter01	INT	●			
2	Counter02	INT	●			
10	Input status[3]	USINT	●			
	StatusInput01	Bit 0				
	...	...				
	StatusInput04	Bit 3				
	CounterOverflow01	Bit 4				
	CounterOverflow02	Bit 5				
	RefToggle01	Bit 6				
32	Error status	USINT	●			
	UnderVoltageError	Bit 0				
	OverVoltageError	Bit 1				
	OvertemperaturError	Bit 2				
	OperatingError	Bit 3				
	CurrentError01	Bit 4				
	OverCurrentError01	Bit 5				
	CurrentError02	Bit 6				
	OverCurrentError02	Bit 7				
34	Error acknowledgment, dither switch-off[3] and FrequencyPrescale[2]	USINT			●	
	ClearError01	Bit 0				
	ClearError02	Bit 1				
	CounterOverflowDetectEnable01	Bit 2				
	CounterOverflowDetectEnable02	Bit 3				
	CounterReset01	Bit 4				
	CounterReset02	Bit 5				
	DitherDisable01 FrequencyPrescale01	Bit 6				
	DitherDisable02 FrequencyPrescale02	Bit 7				
36	Temperature01	SINT		●		

1) Firmware version 3 or higher.
2) Firmware version 7.00 or higher.
3) Firmware version 4 or higher.

4.25.2.14.3 Function model 254 - Bus controller

Register	Offset[1]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
"Standard PWM/current mode" operating mode only							
12	0	PeriodDurationPWM01PWM02	UINT			●	
14	2	PulseWidthCurrentPWM01	INT			●	
16	4	PulseWidthCurrentPWM02	INT			●	
18	-	ConfigOutput01	USINT				●
20	-	ConfigOutput02	USINT				●
31	-	DecayConfig[2]	USINT				●
"Frequency mode 1 and 2" operating mode only[3]							
12	0	FrequencyPWM01PWM02	UINT			●	
		DutyCyclePWM01PWM02	INT				
14	2	DutyCyclePWM01	INT			●	
		FrequencyPWM01	UINT				
16	4	DutyCyclePWM02	INT			●	
		FrequencyPWM02	UINT				
All operating modes							
30	-	ConfigOutput03	USINT				●
38	-	CounterConfig01[4]	USINT				●
39	-	CounterConfig02[4]	USINT				●
Communication							
All operating modes							
0	0	Counter01	INT	●			
2	2	Counter02	INT	●			
10	4	Input status[4]	USINT	●			
		StatusInput01	Bit 0				
		...	...				
		StatusInput04	Bit 3				
		CounterOverflow01	Bit 4				
		CounterOverflow02	Bit 5				
		RefToggle01	Bit 6				
32	6	Error status	USINT	●			
		UnderVoltageError	Bit 0				
		OverVoltageError	Bit 1				
		OvertemperaturError	Bit 2				
		OperatingError	Bit 3				
		CurrentError01	Bit 4				
		OverCurrentError01	Bit 5				
		CurrentError02	Bit 6				
		OverCurrentError02	Bit 7				
34	6	Error acknowledgment, dither switch-off[4] and FrequencyPrescale[3]	USINT			●	
		ClearError01	Bit 0				
		ClearError02	Bit 1				
		CounterOverflowDetectEnable01	Bit 2				
		CounterOverflowDetectEnable02	Bit 3				
		CounterReset01	Bit 4				
		CounterReset02	Bit 5				
		DitherDisable01 FrequencyPrescaled01	Bit 6				
		DitherDisable02 FrequencyPrescaled02	Bit 7				
36	-	Temperature01	SINT		●		

1) The offset specifies the position of the register within the CAN object.
2) Firmware version 3 or higher.
3) Firmware version 7.00 or higher.
4) Firmware version 4 or higher.

4.25.2.14.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.25.2.14.4 Operating mode description

Beginning with firmware version 7.00, the module is equipped with the "Frequency mode 1" and "Frequency mode 2" operating modes in addition to "Standard PWM/current mode".
The following table lists the differences between the different operating modes:

	Operating mode		
	Standard PWM/current mode	Frequency mode 1	Frequency mode 2
Frequency setting	1x period duration in µs (see register "PWM period duration")	2x In 1/10 or 1/100 Hz (see register "Frequency")	1x In 1/10 or 1/100 Hz (see register "Frequency")
Duty cycle / Current setting	2x -100 to 100% (see register "PWM pulse width")	1x -100 to 100% (see register "Duty cycle")	2x -100 to 100% (see register "Duty cycle")
Dithering	Yes	No	No
Decay mode setting	Yes	No	No
PWM/current mode selection	Yes	No	No
Other	PWM start from channel 2 offset 180° compared to channel 1	Due to a different frequency, a fixed phase relationship between channel 1 and channel 2 is not possible.	PWM start from channel 2 offset 180° compared to channel 1
	3.5 A per channel	1 A per channel	3.5 A per channel

4.25.2.14.5 Configuration

4.25.2.14.5.1 Counter configuration 1

Name:
CounterConfig01

This register can be used to configure counter 1.

This function is available beginning with firmware Version 4.

Data type	Value
SINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Sets the type of counter.	000	AB counter with 4x evaluation (A = DI 1, B = DI 2)
		001	Event counter (DI 1)
		010	Period measurement (DI 1)
		011	Gate measurement (DI 1)
		100	ABR counter with 4x evaluation (A = DI 1, B = DI 2, R = DI 3, Reference enable = DI 4). Copies counter 1 to counter 2 on a reference pulse. Counter 2 is shown in the I/O map, even if it is disabled in counter configuration 2.
		101 to 111	No counter. Counter is disabled and not shown in the I/O map.
3	Measurement starts	0	At rising edge on DI 1 Referencing at rising edge on DI 3 (only for ABR counters)
		1	At falling edge on DI 1 Referencing at falling edge on DI 3 (only for ABR counters)
4 - 5	Set the counter frequency for gate or period measurement	00	4 MHz
		01	External via DI 2
		10	31.25 kHz
		11	Reserved
6 - 7	Set the reference input	00	Reference input always enabled (DI 3)
		01	Reserved
		10	Enable for reference input (DI 3) if DI 4 = 0
		11	Enable for reference input (DI 3) if DI 4 = 1

4.25.2.14.5.2 Counter configuration 2

Name:
CounterConfig02

This register can be used to configure counter 2. Unlike counter 1, this counter cannot be configured as an ABR counter.

This function is available beginning with firmware Version 4.

Data type	Value
SINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Sets the type of counter.	000	AB counter with 4x evaluation (A = DI 3, B = DI 4)
		001	Event counter (DI 3)
		010	Period measurement (DI 3)
		011	Gate measurement (DI 3)
		100 to 111	No counter. Counter is disabled and not shown in the I/O map.
3	Measurement starts	0	At rising edge on DI 3
		1	At falling edge on DI 3
4 - 5	Set the counter frequency for gate or period measurement	00	4 MHz
		01	External via DI 4
		10	31.25 kHz
		11	Reserved
6 - 7	Reserved	-	

4.25.2.14.5.3 Module configuration

Name:
ConfigOutput03

The output control for each motor can be configured separately in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Output 1	0	PWM control
		1	Current control
1	Output 2	0	PWM control
		1	Current control
2 - 3	Operating mode[1)]	00	Standard PWM/current mode
		01	Frequency mode 1 (bit 0 to 1 ignored)
		10	Frequency mode 2 (bit 0 to 1 ignored)
		11	Reserved
4 - 7	Reserved	-	

1) Firmware version 7.00 or higher.

Information:

After switching on or resetting, only one switchover from the default "Standard PWM/current mode" is allowed after "Frequency mode 1" or "Frequency mode 2". Later reconfigurations into another mode are ignored by the module's firmware.

4.25.2.14.5.4 Registers for "Standard PWM/current mode" operating mode

PWM period duration

Name:
PeriodDurationPWM01PWM02

This register can be used to set the period duration between 20 µs (50 kHz) and 65535 µs (15 Hz).

Data type	Value	Information
UINT	20 to 65535	Time in µs

PWM pulse width

Name:
PulseWidthCurrentPWM01 to PulseWidthCurrentPWM02

The PWM pulse width (PWM mode) or current setting (in current mode) is entered in this register according to the setting in the module configuration register. A negative value changes the output polarity.

Information:

This module uses the same scaling as the X67MM2436 module to maintain software compatibility. Current values larger than 3.5 A are limited to 3.5 A.

Derating must also be taken into consideration when using both channels (see section 4.25.2.10 "Derating").

PWM mode

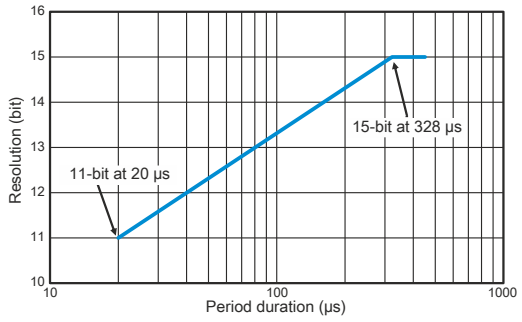
Data type	Value	Output +	Output -
INT	32767	High	Low
	16384	PWM 50/50	Low
	0	Low	Low
	-16384	Low	PWM 50/50
	-32767	Low	High

Current mode

Data type	Value	Current mode	Note
INT	22937 to 32767	+3.5 A (max. 2 s)	Limited internally, check derating
	22936	3.5 A (max. 2 s)	Derating must be taken into consideration.
	19660	+3 A	
	0	0 A	
	-19660	-3 A	
	-22936	-3.5 A (max. 2 s)	Derating must be taken into consideration.
	-22937 to -32767	-3.5 A (max. 2 s)	Limited internally, check derating

Resolution/Derating

As mentioned earlier in the technical data, the PWM resolution is 15-bit (+ sign). This value is derated for a period duration of less than 328 µs because of the minimal PWM timing resolution (10 ns) (see following diagram). With the minimum PWM period duration of 20 µs, the PWM has 11-bit resolution (+ sign):



Decay configuration

Name:
DecayConfig

The decay configuration determines the method and dynamics of current reduction for inductive loads or motors.

"Slow decay" is configured by default. In this mode, the current is automatically reduced relatively slowly with resistance in the load. No energy is regenerated into the module.

"Mixed decay" mode is recommended for applications that require a dynamic and linear reduction of current. In this mode, energy is regenerated into the module during part of the PWM cycle (fast decay).

This function is available beginning with firmware Version 3.

Data type	Value
USINT	See bit structure.

Bit structure:

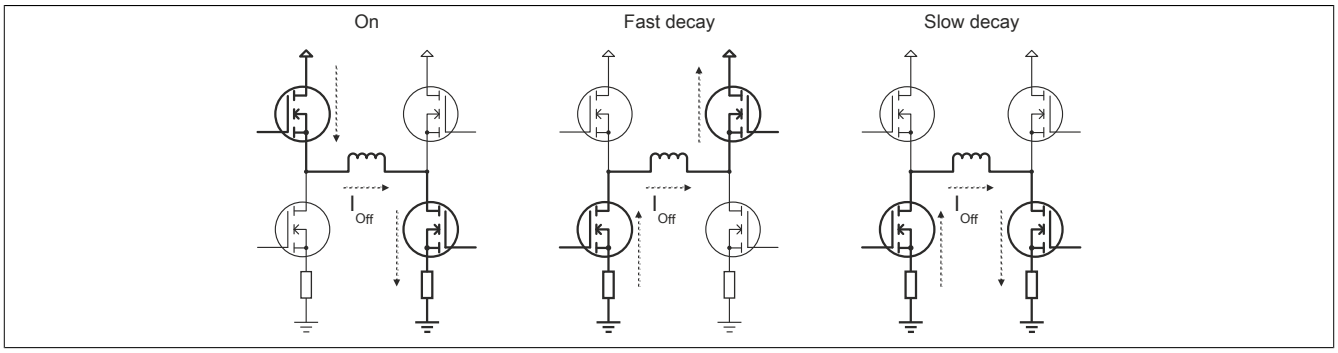
Bit	Description	Value	Information
0 - 1	PWM 1	00	Slow decay (default setting)
		01	Mixed decay
		10 to 11	Reserved
2 - 3	Reserved	0	
4 - 5	PWM 2	00	Slow decay (default setting)
		01	Mixed decay
		10 to 11	Reserved
6 - 7	Reserved	0	

Mixed decay

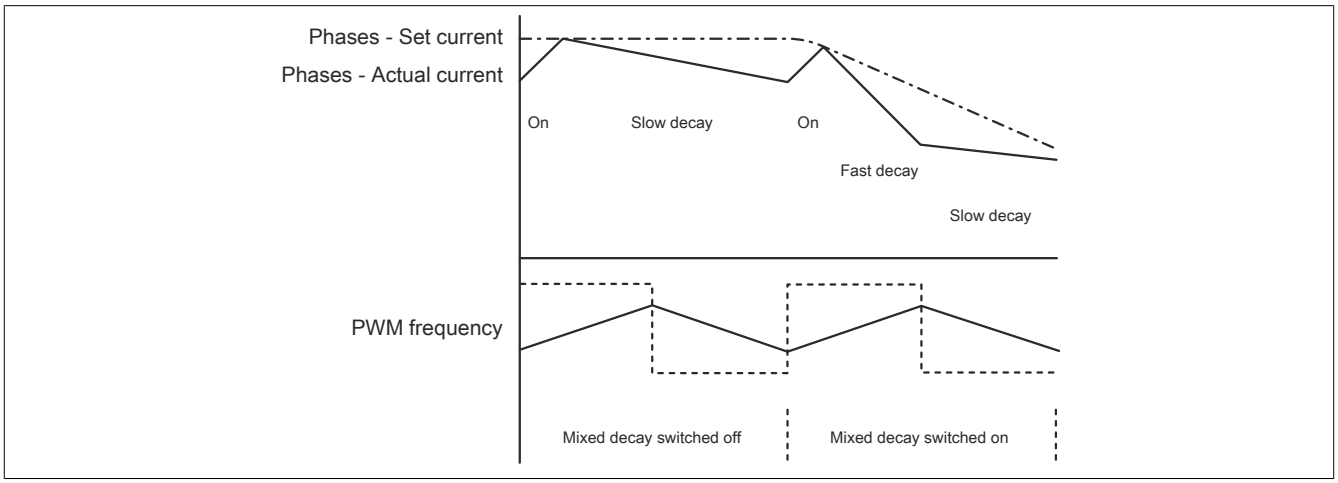
As its name suggests, mixed decay mode is a mix of "slow decay" and "fast decay". This occurs as follows:

A check is made at the beginning of each PWM cycle to determine if the actual current for the phases is below the current setpoint. If this is the case, PWM is enabled (On) until the set current is reached. The system switches to fast decay mode for the rest of the first half of the PWM cycle. If the current setpoint has already been exceeded at the beginning of the PWM cycle (generator operation), the system immediately switches to fast decay mode. The second half of the PWM cycle always takes place in slow decay mode.

This also permits generator operation as long as the valid range for the supply voltage has not been exceeded due to the regeneration into the DC circuit.



Mixed decay - Set / actual current, PWM frequency



Operating DC motors

In PWM mode, the motor current is limited to the maximum current (3.5 A), independent of the supply voltage.

However, the motor switches to generator operation when braking. Because of the counter EMF, which is dependent on the rotary speed, a current is generated in the module that is only limited by the internal resistance of the motor. This is not permitted to exceed 7 A (maximum 2 seconds).

The counter EMF closely corresponds to the voltage needed to achieve this speed. Therefore, the maximum brake current is very easy to calculate with the following formula.

$$I_{Brake} = U_e.Pulse\ width(in\ \%)/100.\frac{1}{R_{Motor}}$$

Example:

Module supply	42 V
Pulse width	16364 (equal to 50%)
Internal resistance of motor	3.5 Ω

$$I_{Brake} = 42V.50/100.\frac{1}{3.5\Omega} = 6A$$

Dither

A dither is used to prevent valves from sticking. This function is supported in both PWM mode and in current mode. The pulse width or current is adjusted according to the dither amplitude and dither frequency.

By default, the dither is active for both outputs as soon as the dither amplitude and dither frequency are set to a value >0. If necessary, the dither can be deactivated for each output individually or simultaneously (see 4.25.2.14.6.5 "Error acknowledgment, dither switch-off and FrequencyPrescale").

Dither amplitude

Name:
ConfigOutput01

This register can be used to configure the amplitude value or pulse width.
0 to 255 corresponds with an amplitude value from 0.0 to 25.5% of the nominal current or the maximum pulse width of 32767.

Data type	Value	Information
USINT	0 to 255	Amplitude value or pulse width

Dither frequency

Name:
ConfigOutput02

This register can be used to set the frequency in 2 Hz steps.

Data type	Value	Information
USINT	0 to 255	Corresponds to 0 to 510 Hz

Dither example

Valve specification	20 to 35% peak to peak of the valve current at 2 A²
	This corresponds to a dither amplitude of ±6.67 to ±11.67% at 3 A. A midrange dither amplitude of 9% at 3 A is selected. This corresponds to a setting of 90.
Dither frequency specification	**40 to 70 Hz**
	A setting of 28 is selected. This corresponds to a frequency of 56 Hz.

4.25.2.14.5.5 Registers for "Frequency mode 1 and 2" operating mode

Frequency

Name:
FrequencyPWM01 to FrequencyPWM02 (frequency mode 1)
FrequencyPWM01PWM02 (frequency mode 2)

The frequency for PWM01 or PWM02 (depends on the frequency mode) can be set individually or together in these registers. The unit is 1/10 or 1/100 Hz depending on how the "FrequencyPrescale" settings are configured. For more information, see the 4.25.2.14.6.5 "Error acknowledgment, dither switch-off and FrequencyPrescale" registers.

Data type	Value	Information
DINT	0	Disabled
	1 to 99	FrequencyPrescale 1/10: 10 Hz FrequencyPrescale 1/100: 1 Hz
	100 to 65535	FrequencyPrescale 1/10: 1/10 * Value = 10 to 6553.5 Hz FrequencyPrescale 1/100: 1/100 * Value = 1 to 655.35 Hz

Duty cycle

Name:
DutyCyclePWM01PWM02 (frequency mode 1)
DutyCyclePWM01 to DutyCyclePWM02 (frequency mode 2)

The duty cycle for the PWM outputs is set individually or separately depending on the frequency mode.

For information about scaling, derating, etc. see the "PWM pulse width" registers (PWM mode).

Important!

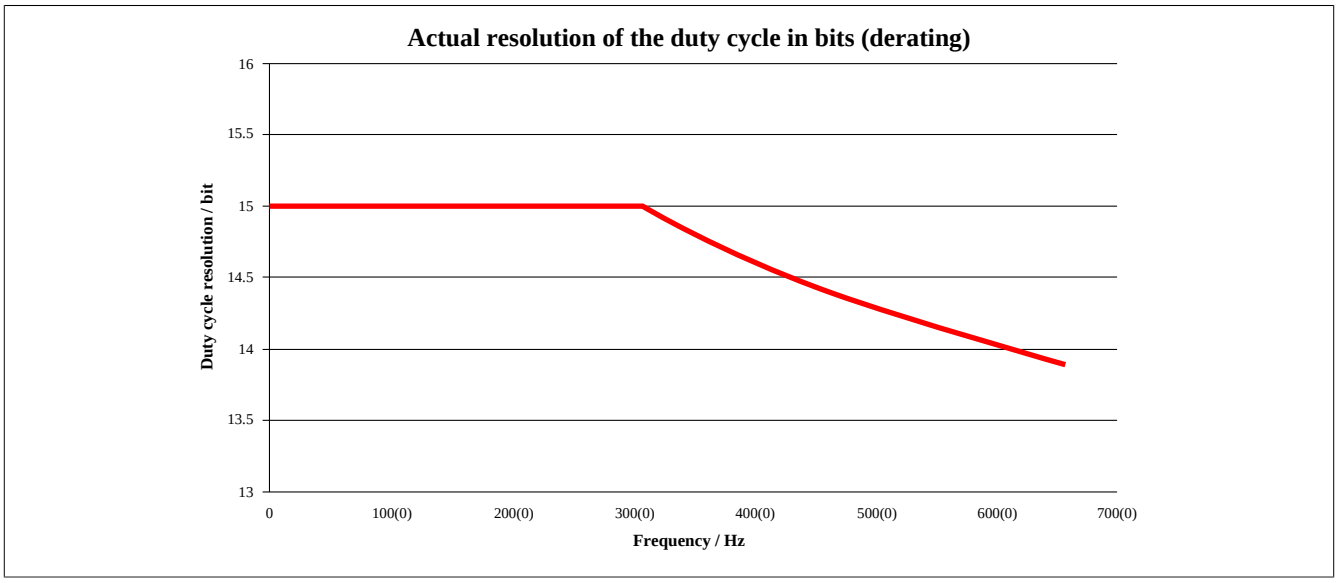
A negative duty cycle can also be configured. In this case, the frequency is output to "PWM1/2" (identical to "Standard PWM/current mode") instead of the "PWM1/2+" output. It is especially important to take this into consideration with actuators that are only able to process positive input values.

Data type	Value
INT	-32768 to 32767

Derating the duty cycle

As with "Standard PWM/current mode", the predefined duty cycle in the frequency modes cannot be implemented over the entire frequency domain with full 15-bit resolution; instead, it is subject to derating.

It is possible to achieve the full 15-bit resolution until about 305 (frequency domain 1) or 3050 Hz (frequency domain 2).



4.25.2.14.6 Communication

4.25.2.14.6.1 Numerator

Name:
Counter01 to Counter02

This register indicates the status of counters 1 and 2. Configuration of the counters is described in sections 4.25.2.14.5.1 "Counter configuration 1" and 4.25.2.14.5.2 "Counter configuration 2". The following counter types or measurements can be configured:

- AB counter
- ABR counter
- Event counter
- Period measurement
- Gate measurement

If counter 1 is configured as an ABR counter, then the register for counter 2 is assigned the current value of counter 1 when the reference pulse occurs.

Data type	Value
INT	-32768 to 32767

Counter function - Assignment of the digital inputs:

Counter function	Counter number	A	B	R	Enable reference	Counter input	Period duration and gate signal	External measuring frequency
Incremental counter	1	DI 1	DI 2	DI 3	DI 4			
	2	DI 3	DI 4					
Event counter	1					DI 1		
	2					DI 3		
Period duration and gate measurement	1						DI 1	DI 2
	2						DI 3	DI 4

4.25.2.14.6.2 Input status

Name:
StatusInput01 to StatusInput04
CounterOverflow01 to CounterOverflow02
RefToggle01

The status of the inputs and counters is mapped in this register.

This function is available beginning with firmware Version 4.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusInput01	0 or 1	Logical state of input 1
...		...	
3	StatusInput0	0 or 1	Logical state of input 4
4	CounterOverflow01	0	Period duration or gate measurements of counter 1 are within the valid range (0x0 - 0xFFFF). The bit is only valid if overflow detection is enabled (bit 2 = 1 in the 4.25.2.14.6.5 "Error acknowledgment, dither switch-off and FrequencyPrescale" register).
		1	Overflow during period duration or gate measurement (reset with bit 2 = 0 in the 4.25.2.14.6.5 "Error acknowledgment, dither switch-off and FrequencyPrescale" register).
5	CounterOverflow02	0	Period duration or gate measurements of counter 2 are within the valid range (0x0 - 0xFFFF). The bit is only valid if overflow detection is enabled (bit 3 = 1 in the 4.25.2.14.6.5 "Error acknowledgment, dither switch-off and FrequencyPrescale" register).
		1	Overflow during period duration or gate measurement (reset with bit 3 = 0 in the 4.25.2.14.6.5 "Error acknowledgment, dither switch-off and FrequencyPrescale" register).
6	RefToggle01	x	Bit 6 changes value each time the counter state is latched from counter 1 to counter 2. After the module boots, bit 6 = 0.
7	Reserved	-	

4.25.2.14.6.3 Temperature

Name:
Temperature01

The module temperature is displayed in this register.

Data type	Value	Information
SINT	-40 to 125	Module temperature in °C

4.25.2.14.6.4 Error status

Name:
UnderVoltageError
OverVoltageError
OvertemperatureError
OperatingError
CurrentError01 to CurrentError02
OverCurrentError01 to OverCurrentError02

If an error is detected, the corresponding error bit remains set in this register until the error is acknowledged (see 4.25.2.14.6.5 "Error acknowledgment, dither switch-off and FrequencyPrescale").

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	UnderVoltageError	0	No error
		1	Module supply lower limit <18 V
1	OverVoltageError	0	No error
		1	Module supply upper limit >50 V
2	OvertemperatureError	0	No error
		1	Overtemperature
3	OperatingError[1)]	0	No error
		1	Faulty operation
4	CurrentError01	0	No error
		1	Open load error Output 1
5	OverCurrentError01	0	No error
		1	Overcurrent error Output 1
6	CurrentError02	0	No error
		1	Open load error Output 2
7	OverCurrentError02	0	No error
		1	Overcurrent error Output 2

1) Firmware version 7.00 or higher.

Faulty operation

This warning indicates faulty operation of the module. The following table lists possible causes, the module's reaction and how to correct/acknowledge the error.

Cause	Reaction	Correction/Acknowledgment
Default value for "PeriodDuration" or "Frequency" outside of specified range	Default value limited to the specified range	Automatic acknowledgment as soon as the default value is back within specifications
Later reconfiguration of the operating mode (see bits 2 to 3 of the "Module configuration" register)	The new configuration is ignored. The module continues to work in the original operating mode.	The original configuration is restored.

Overcurrent error

An overcurrent error is registered if one of the following conditions is met:

- ≥3.5 or 1 A (frequency mode 1) flow from a PWM output for at least 2 seconds
- ≥5 A flow for 3 consecutive PWM cycles

In both cases, the affected PWM output is deactivated by the firmware (i.e. the pins on the PWM output are short-circuited). The user must acknowledge the error (see 4.25.2.14.6.5 "Error acknowledgment, dither switch-off and FrequencyPrescale") before a PWM output disabled in this manner can be made operational again.

Open load error

An open load error is only registered in current control mode (see 4.25.2.14.5.3 "configuration register") if the current setpoint is not reached. In some cases this can be caused by an open line, although usually the impedance of the load is too high.

4.25.2.14.6.5 Error acknowledgment, dither switch-off and FrequencyPrescale

Name:
ClearError01 to ClearError02
CounterOverflowDetectEnable01 to CounterOverflowDetectEnable02
CounterReset01 to CounterReset02
DitherDisable01 to DitherDisable02
FrequencyPrescale01 to FrequencyPrescale02

This register can be used to acknowledge errors; to enable/disable overflow detection, counters and dither; and to set a prescaler for the frequency domains.

This function is available beginning with firmware Version 4.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ClearError01	0	No effect
		1	Error acknowledgment on output 1 (overcurrent or open load) or acknowledgment from limit switch 1
1	ClearError02	0	No effect
		1	Error acknowledgment on output 2 (overcurrent or open load) or acknowledgment from limit switch 2
2	CounterOverflowDetectEnable01	0	Overflow detection disabled. Bit 4 in the counter status register is reset (see section 4.25.2.14.6.2 "Input status")
		1	Counter 1: Overflow detection enabled.
3	CounterOverflowDetectEnable02	0	Overflow detection disabled. Bit 5 in the counter status register is reset (see section 4.25.2.14.6.2 "Input status")
		1	Counter 2: Overflow detection enabled.
4	CounterReset01	0	Counter 1 is enabled (default).
		1	Counter 1 is set to 0 and disabled. If counter 1 is configured as an ABR counter (see 4.25.2.14.5.1 "Counter configuration 1"), then latch 2 is also set to 0. In this mode, the latched value from counter 1 is stored in counter 2.
5	CounterReset02	0	Counter 2 is enabled (default).
		1	Counter 2 is set to 0 and disabled (no effects if counter 1 is configured as an ABR counter)
6	DitherDisable01	0	Dither for PWM output 1 is enabled (default). The dither frequency and dither amplitude must be >0 (see "Dither").
		1	Dither for PWM output 1 is disabled.
	FrequencyPrescale01[1)]	0	Unit in 1/10 Hz, frequency domain: 10 to 6553.5 Hz
		1	Unit in 1 Hz, frequency domain: 1 to 655.35 Hz
7	DitherDisable02	0	Dither for PWM output 2 is enabled (default). The dither frequency and dither amplitude must be >0 (see "Dither").
		1	Dither for PWM output 2 is disabled.
	FrequencyPrescale02[1)]	0	Unit in 1/10 Hz, frequency domain: 10 to 6553.5 Hz
		1	Unit in 1 Hz, frequency domain: 1 to 655.35 Hz

1) Firmware version 7.00 or higher.

FrequencyPrescale

Beginning with firmware version 7.00, bits 6 to 7 in the "Frequency mode 1 and 2" operating mode have a different meaning.

Instead of enabling/disabling dithering for channel 1 or 2, it toggles the prescaler for the frequency setting between 1/10 and 1/100 Hz.

In "Frequency mode 2" operating mode, only bit 6 (FrequencyPrescale01) is used since both channels are operated with the same frequency.

Information:

The frequency domain can be toggled at any time, but it also results in the frequency jumping by a factor of 10. If this frequency jump is not tolerated in the application, then the value set in the "Frequency" register must be adjusted accordingly.

4.25.2.14.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

4.25.2.14.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
250 µs

4.25.3 X20MM3332

4.25.3.1 General information

The 3 outputs on the motor module are designed as full-bridge outputs. The continuous current per channel is 3 A at a peak current of up to 5 A. Integrated diagnostics offer the possibility to read back the output current for each channel using the application.

The module offers extensive possibilities for controlling motors, valves or resistive loads and is particularly well suited for controlling brush DC motors. Because the outputs are designed as full-bridge outputs, the motors can be moved in both directions.

- 3 full-bridge outputs (H-bridges)
- High component density
- 3 A continuous current
- 5 A peak current
- Readable current

4.25.3.2 Order data

Model number	Short description	Figure
	Motor controllers	
X20MM3332	X20 digital motor module, 24 VDC, 3 digital outputs, full bridge (H bridge), 3 A continuous current, 5 A peak current	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 556: X20MM3332 - Order data

4.25.3.3 Technical data

Product ID	X20MM3332
Short description	
I/O module	3 full-bridge outputs
General information	
B&R ID code	0xA982
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Output	Yes, using status LED and software
I/O supply	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.8 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
External I/O supply bus	Yes
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GOST-R	Yes
Motor bridge - Power unit	
Quantity	3
Design	H bridge
Type	Full bridge High-side driver Low-side driver
Nominal voltage	24 VDC
Switching voltage	24 VDC (-15% / +20%)
Nominal current	3 A
Maximum current	5 A (250 ms)
Total nominal current	10 A
Current value measurement	
Resolution	100 mA
Data collection	In the driver
Output protection	Thermal cutoff for overcurrent and short circuit
Supply voltage	No reverse polarity protection
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 50°C
Vertical installation	Not permitted
Derating	See section "Derating"
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%
Storage	5 to 95%
Transport	5 to 95%
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 557: X20MM3332 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.25.3.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

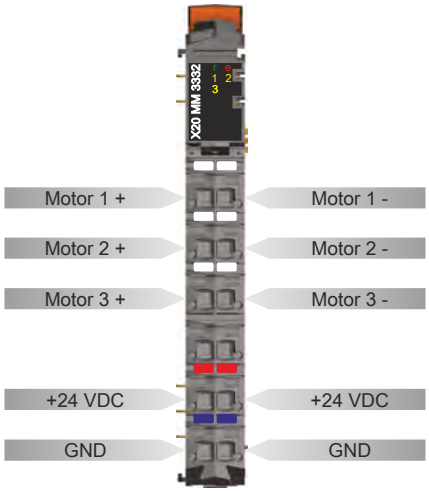
Figure	LED	Color	Color	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 3	Orange	On	The corresponding output is active
			Blinking	Error on the corresponding output
			Off	The corresponding output is switched off

4.25.3.5 Pinout

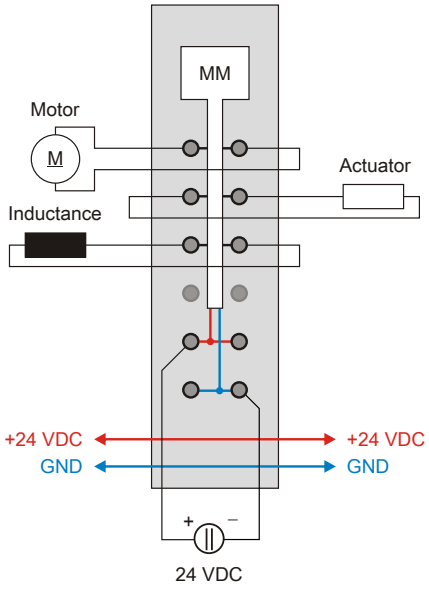
Lines with a cross section between a minimum of 0.75 mm² and a maximum of 2.5 mm² are recommended for the outputs.

Warning!

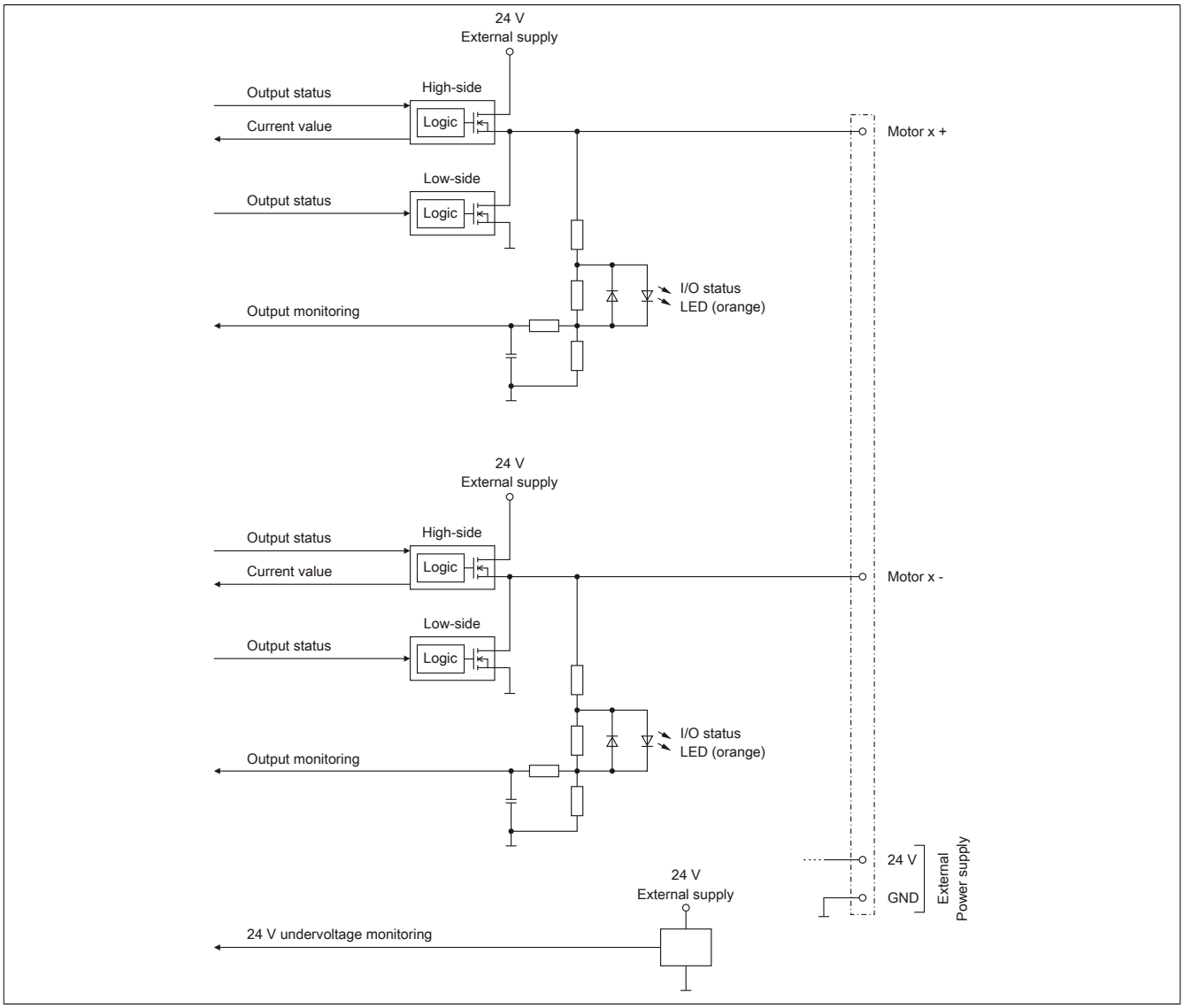
The terminal block is not permitted to be plugged in or unplugged during operation.



4.25.3.6 Connection example

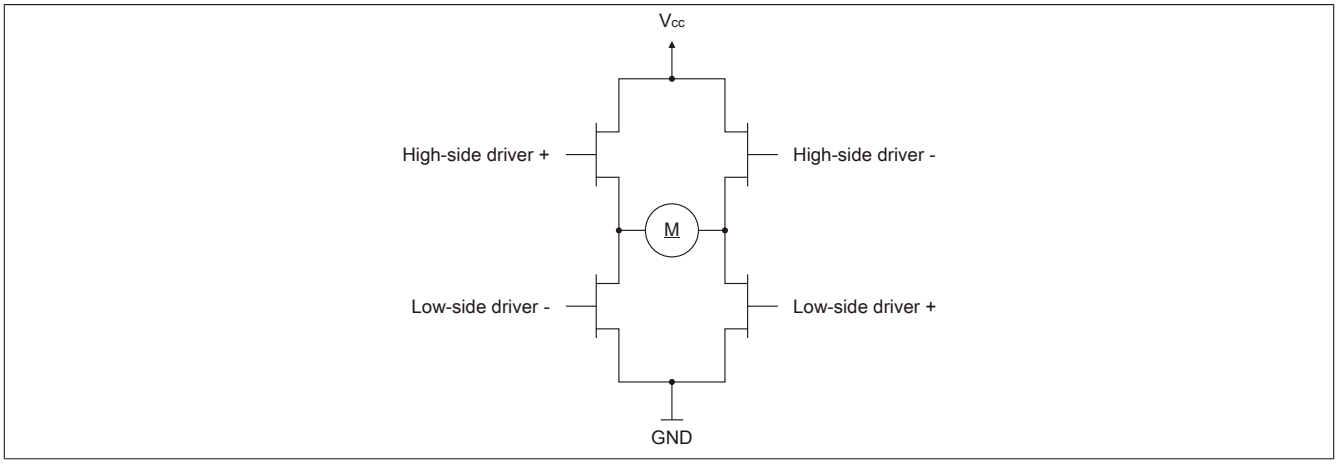


4.25.3.7 Output circuit diagram



4.25.3.8 Function description - Motor operation

Three DC motors can be operated with the module. Each output is designed as a full-bridge output, therefore the motors can be moved in both directions.



Description of the operating modes using the basic circuit diagram shown above:

Operating mode	Description
Rotational direction 1	If the high-side driver + and the low-side driver + are active, the direction of rotation on the motor is from + to -.
Rotational direction 2	If the high-side driver - and the low-side driver - are active, the direction of rotation on the motor is from - to +.
Brakes	If both low-side drivers are active, the motor is short-circuited. This functions as a motor brake.

4.25.3.9 Protection

The power supply line should be protected by a circuit breaker or a fuse. In general, dimensioning the supply line and overcurrent protection depends on the structure of the power supply (modules can be connected individually or in groups).

Information:

The effective current for the power supply depends on the load, but is always less than the sum of the output currents. Make sure that the maximum nominal current of 31 A per pin is not exceeded on the power supply terminals of the power unit.

When choosing a suitable fuse, the user must also account for characteristics such as aging effects, temperature derating, overcurrent capacity and the definition of the rated current, which can vary by manufacturer and type. In addition, the fuse that is selected must also be able to handle application-specific characteristics (e.g. overcurrent that occurs in acceleration cycles).

The cross section of the power mains and the rated current of the overcurrent protection used are chosen according to the current load so that the maximum current load for the cable cross section selected (based on the type of layout, see table) is greater than or equal to the current load in the power mains. The rated current of the overcurrent protection must be less than or equal to the maximum current load for the cable cross section selected (based on the type of layout, see table):

I_{Mains}	≤	I_b	≤	I_Z
Mains	≤	Fuse	≤	Line/cable

Wire cross section [mm²]	Current load of the cable cross section I_Z / rated current of the over current protection I_b [A] according to type of installation in an ambient air temperature of 40°C in accordance to IEC 60204-1			
	B1	B2	C	E
1.5	13.5 / 13	13.1 / 10	15.2 / 13	16.1 / 16
2.5	18.3 / 16	16.5 / 16	21 / 20	22 / 20
4.0	24.0 / 24.0	23.0 / 20.0	28.0 / 25.0	30.0 / 25.0
6.0	32.0 / 32.0	29.0 / 25.0	36.0 / 32.0	37.0 / 32.0

Table 558: Cable cross section of the mains supply line depending on the type of layout

The tripping current of the fuse cannot exceed the rated current of fuse I_b.

Type of layout	Description
B1	Wires in conduit or cable duct
B2	Cables in conduit or cable duct
C	Cables or wires on walls
E	Cables or wires on open cable tray

Table 559: Type of layout for the mains supply line

4.25.3.10 Derating

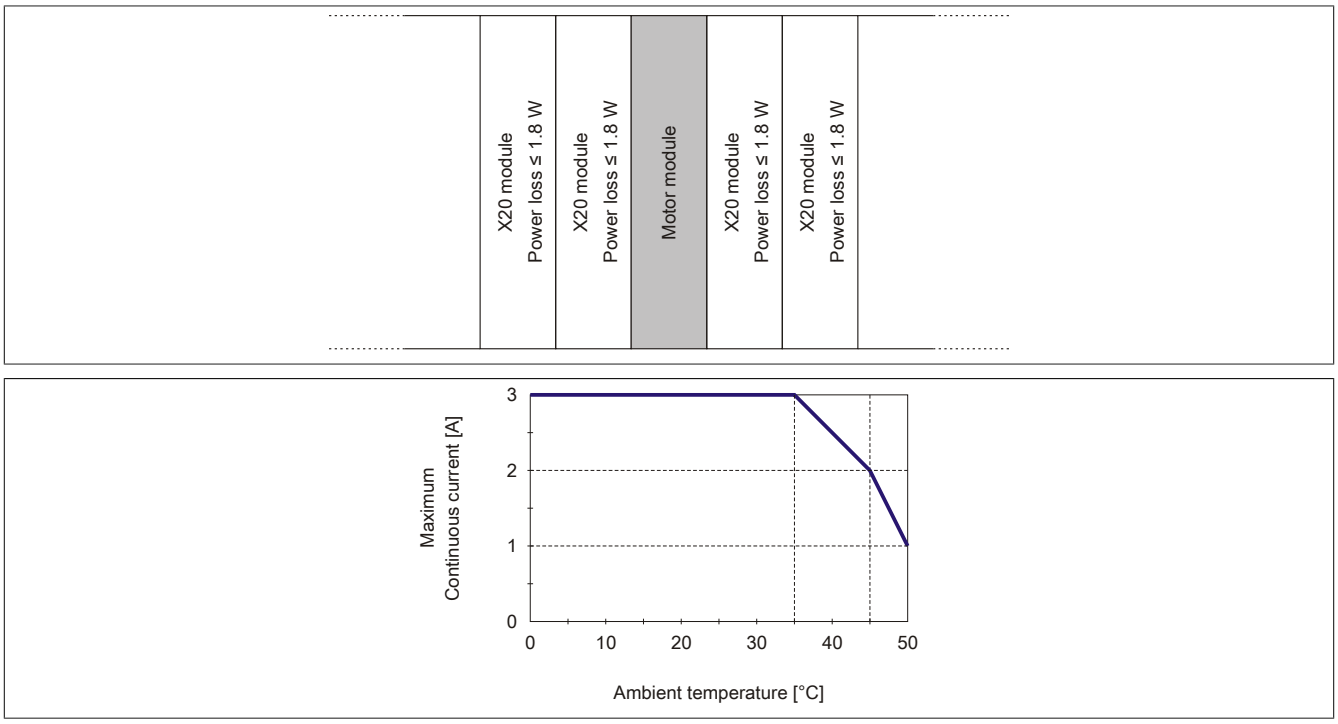
In order to be able to operate the motor module over the entire temperature range, only modules with a maximum power loss of of 0.5 W can be installed next to the motor module or respective turn-off times must be implemented.

If the neighboring modules have a higher power loss and all channels are operated continuously, the motor current must be derated.

When a motor is switched on, the current is increased for a short time. This behavior has no influence on the derating.

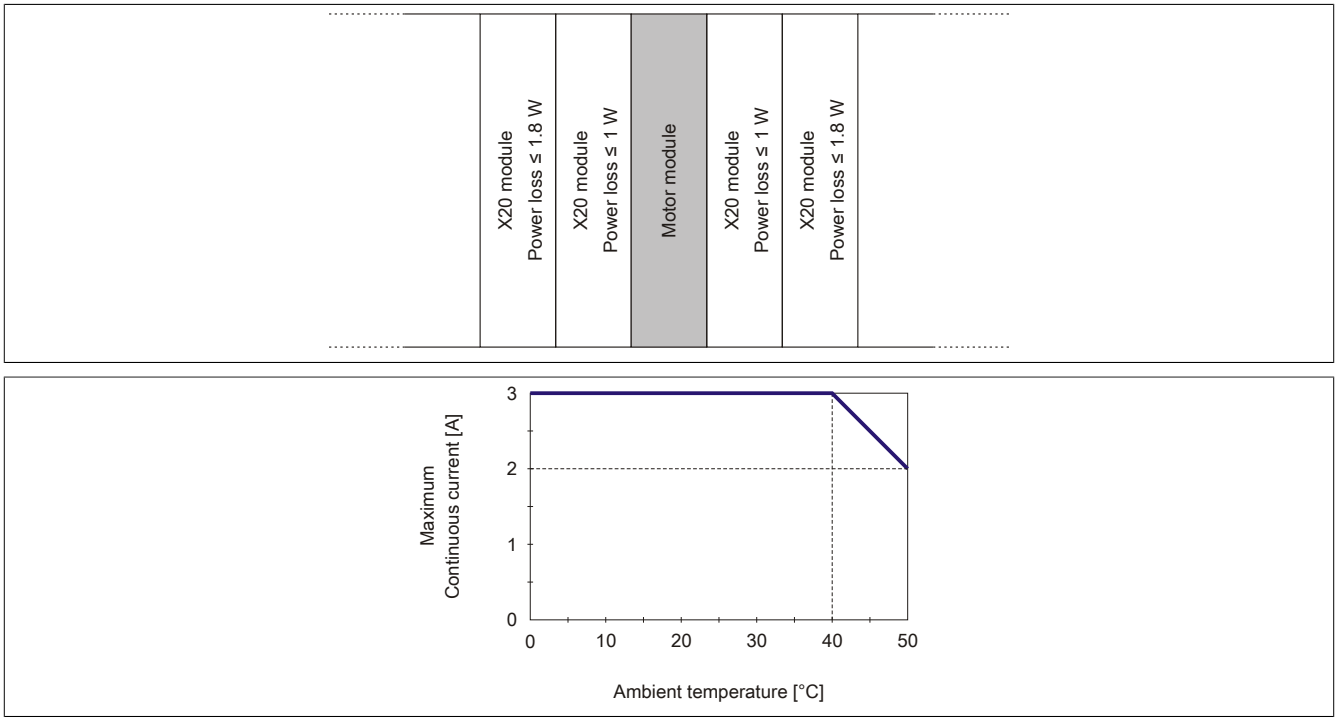
Current derating 1 of the motor module

Current derating for the motor module for neighboring modules with ≤1.8 W thermal power loss.



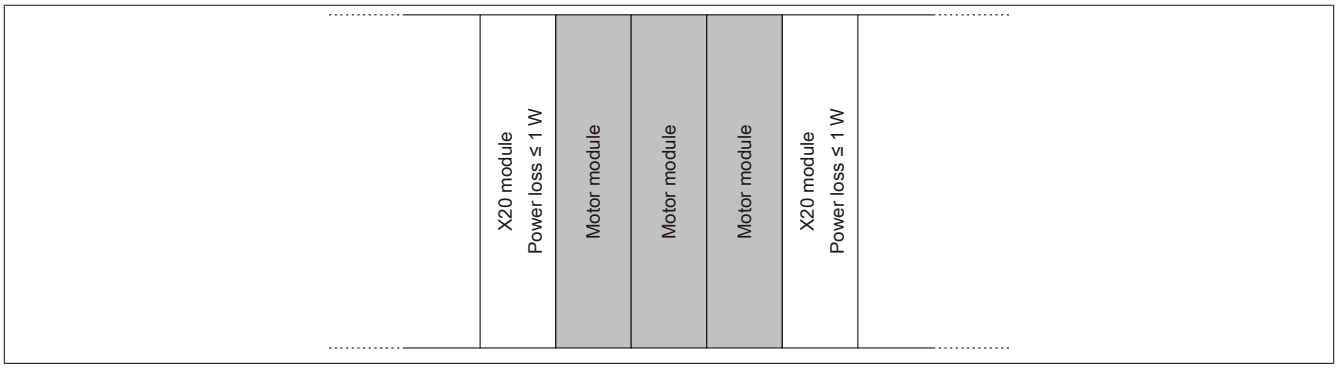
Current derating 2 of the motor module

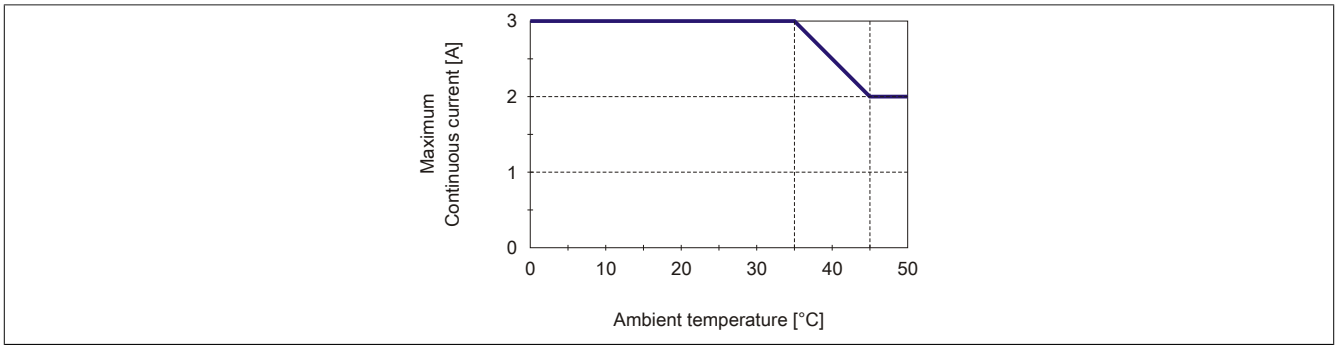
Current derating for the motor module for neighboring modules with ≤1 W thermal power loss.



Current derating 3 of the motor module

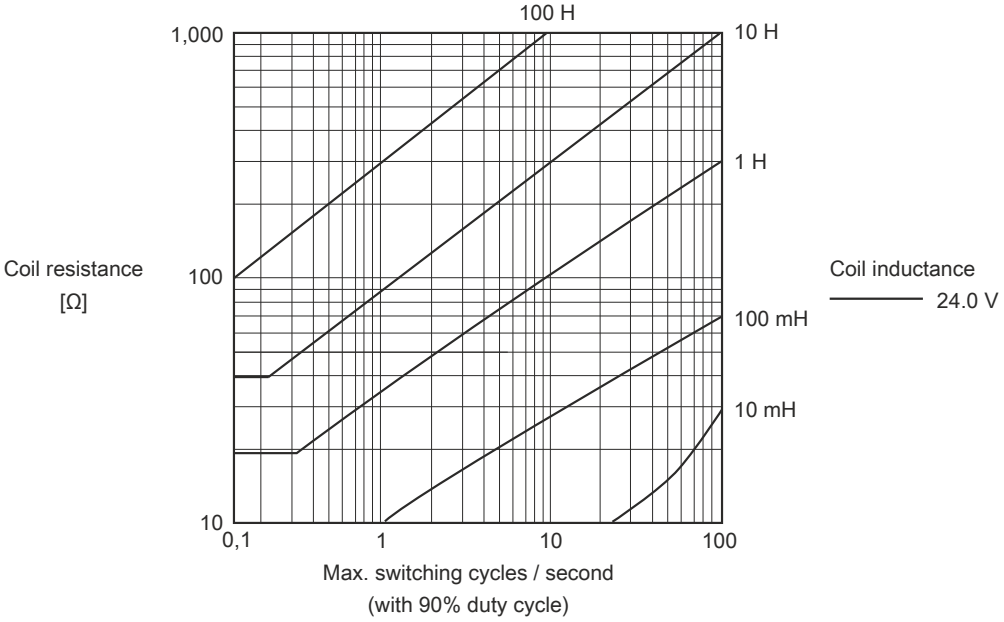
Current derating with multiple motor modules next to each other.



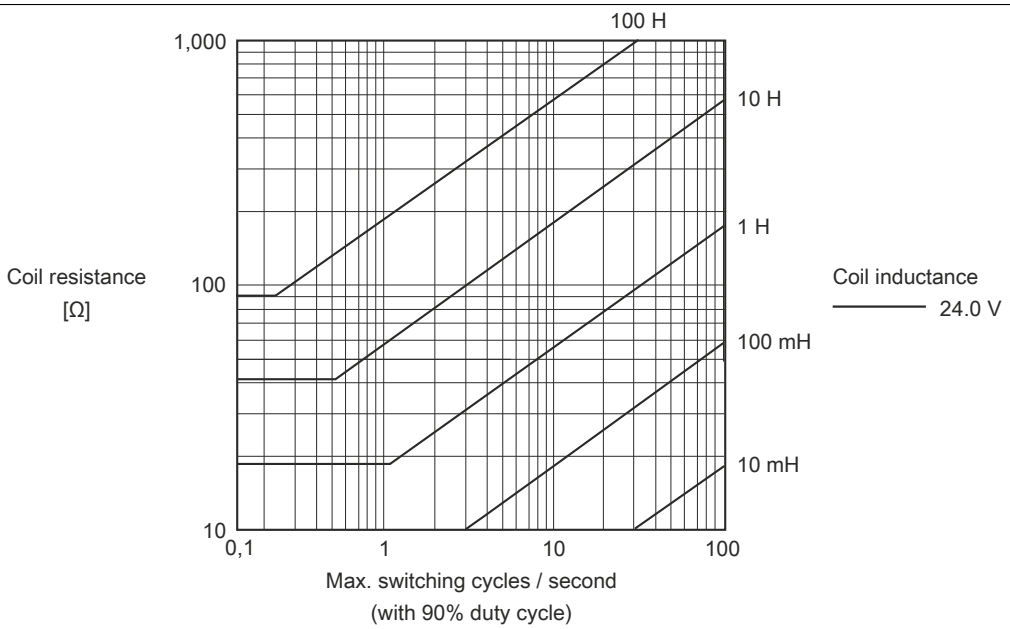


4.25.3.11 Switching inductive loads (e.g. valves)

With enabled short circuit channel - All outputs with same load



With disabled short circuit channel - All outputs with same load



4.25.3.12 Monitoring the module supply

The module supply is continually monitored. If the supply voltage drops below 18V, all channels are switched off and an error bit is set.

Information:

The undervoltage must be present for longer than 250 ms, before all channels are switched off. Power dips can occur when starting motors or capacitive loads!

4.25.3.13 Monitoring the module current

The module current is continually monitored. If an overcurrent occurs, the respective channel is switched off and an error bit is set.

Information:

The overcurrent must be present for longer than 250 ms, before the channel is switched off. High starting currents occur when starting motors or capacitive loads!

4.25.3.14 Channel monitoring

After each switching process, the status inputs are checked with a 2 ms delay to ensure they are correct. This is done so that faulty status signals are not generated when switching motors or capacitive loads.

If the status of the output does not correspond to the status that is expected (e.g. short circuit or motor spin-out), a warning bit is set.

Information:

When channel monitoring is triggered, a warning is given. The output remains switched even if there is a short circuit and is cycled to the output by the internal protective circuit.

If the motor is still spinning out, the voltage drops slowly. That means the warning bit StatusDigitalOutput can show a warning while the motor is spinning out.

If the motor is moved externally, voltage is induced into the module, which results in StatusDigitalOutput being set and the red LED being lit (warning).

4.25.3.15 Overtemperature cutoff (at 85°C)

If the module temperature reaches or exceeds the limit value of 85°C, then the module executes the following actions:

- Setting the "overtemperature" error bit
- The outputs are switched off (short-circuited)

As soon as the temperature sinks back down below 85°C, the error must be acknowledged with OvertemperatureAcknowledge so that the channels can be switched on again.

4.25.3.16 Register description

4.25.3.16.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.25.3.16.2 Function model 0 - Standard

In this function model, control of full bridges takes place using 3 bits per channel.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
0	Motor configuration 1 - Default	USINT			•	
	StartChannel01	Bit 0				
	ShortCircuitChannel01	Bit 1				
	DirectionChannel01	Bit 2				
	StartChannel02	Bit 4				
	ShortCircuitChannel02	Bit 5				
	DirectionChannel02	Bit 6				
1	Motor configuration 2 - Default	USINT			•	
	StartChannel03	Bit 0				
	ShortCircuitChannel03	Bit 1				
	DirectionChannel03	Bit 2				
18	Error acknowledged	USINT			•	
	OvercurrentAcknowledge01	Bit 0				
	OvercurrentAcknowledge02	Bit 1				
	OvercurrentAcknowledge03	Bit 2				
	OvertemperatureAcknowledge	Bit 6				
	UndervoltageAcknowledge	Bit 7				
Communication						
4	CurrentInput01	USINT	•			
6	CurrentInput02	USINT	•			
8	CurrentInput03	USINT	•			
20	Module and channel status	USINT	•			
	OvercurrentError01	Bit 0				
	OvercurrentError02	Bit 1				
	OvercurrentError03	Bit 2				
	StatusDigitalOutput01	Bit 3				
	StatusDigitalOutput02	Bit 4				
	StatusDigitalOutput03	Bit 5				
	OvertemperatureError	Bit 6				
	UndervoltageError	Bit 7				

4.25.3.16.3 Function model 1 - Byte control and Function model 254 - bus controller

Control of the half bridges takes place using one byte (two bits per channel). All other registers are the same as in Function model 0 - Standard.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
0	0	Motor configuration - Byte control	USINT			●	
18	4	Error acknowledged	USINT			●	
		OvercurrentAcknowledge01	Bit 0				
		OvercurrentAcknowledge02	Bit 1				
		OvercurrentAcknowledge03	Bit 2				
		OvertemperatureAcknowledge	Bit 6				
		UndervoltageAcknowledge	Bit 7				
Communication							
4	0	CurrentInput01	USINT	●			
6	2	CurrentInput02	USINT	●			
8	4	CurrentInput03	USINT	●			
20	6	Module and channel status	USINT	●			
		OvercurrentError01	Bit 0				
		OvercurrentError02	Bit 1				
		OvercurrentError03	Bit 2				
		StatusDigitalOutput01	Bit 3				
		StatusDigitalOutput02	Bit 4				
		StatusDigitalOutput03	Bit 5				
		OvertemperatureError	Bit 6				
		UndervoltageError	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.25.3.16.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.25.3.16.4 Configuration

4.25.3.16.4.1 Motor configuration 1 - Default

Name:
StartChannel01 to StartChannel02
ShortCircuitChannel01 to ShortCircuitChannel02
DirectionChannel01 to DirectionChannel02

This register contains the control bits for the first two channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0	StartChannel01	0	Switch off channel 1
		1	Channel 1 is started (bridge control)
1	ShortCircuitChannel01	0	Do not short circuit channel 1.
		1	Short circuit channel 1.
2	DirectionChannel01	0	Rotational direction 1
		1	Rotational direction 2: The polarity of the connections for motor 1 are reversed internally.[1)]
3	Reserved	-	Reserved
4	StartChannel02	0	Switch off channel 2
		1	Channel 2 is started (bridge control)
5	ShortCircuitChannel02	0	Do not short circuit channel 2.
		1	Short circuit channel 2.
6	DirectionChannel02	0	Rotational direction 1
		1	Rotational direction 2: The polarity of the connections for motor 2 are reversed internally.[1)]
7	Reserved	-	

1) The direction of rotation on the motor is changed by internally reversing the polarity of the connections.

Information:

StartChannel 1 to 2 and ShortCircuitChannel 1 to 2:

To avoid internal bridge shorts, the outputs are delayed by 200 µs when switching to another state or a short circuit.

Information:

When the direction of the motor is changed, the polarity is reversed. If the direction of rotation on the motor is changed during operation, the motor immediately brakes and turns in the other direction. This can result in very high current values. Therefore, we recommend short-circuiting the motor first (braking) and then changing to the other direction.

4.25.3.16.4.2 Motor configuration 2 - Default

Name:
StartChannel03
ShortCircuitChannel03
DirectionChannel03

This register contains the control bits for the third channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0	StartChannel03	0	Switch off channel 3
		1	Switch on channel 3
1	ShortCircuitChannel03	0	Do not short circuit channel 3.
		1	Short circuit channel 3.
2	DirectionChannel03	0	Rotational direction 1
		1	Rotational direction 2: The polarity of the connections for motor 3 are reversed internally.[1)]
3 - 7	Reserved	-	

1) The direction of rotation on the motor is changed by internally reversing the polarity of the connections.

Information:

StartChannel 3 and ShortCircuitChannel 3:

To avoid internal bridge shorts, the outputs are delayed by 200 µs when switching to another state or a short circuit.

Information:

When the direction of the motor is changed, the polarity is reversed. If the direction of rotation on the motor is changed during operation, the motor immediately brakes and turns in the other direction. This can result in very high current values. Therefore, we recommend short-circuiting the motor first (braking) and then changing to the other direction.

4.25.3.16.4.3 Motor configuration - Byte control

Name:
ControlByte01

This register is used to control all 3 channels. Two bits per channels are always grouped together. This register is only used in Function model 1 - Byte control and Function model 254 - bus controller.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0 - 1	Channel 1	00	No-load operation
		01	Rotational direction 1
		10	Rotational direction 2: The polarity of the connections for motor 1 are reversed internally.[1)]
		11	Short circuit
...		...	
4 - 5	Channel 3	00	No-load operation
		01	Rotational direction 1
		10	Rotational direction 2: The polarity of the connections for motor 3 are reversed internally.[1)]
		11	Short circuit
6 - 7	Reserved	-	

1) The direction of rotation on the motor is changed by internally reversing the polarity of the connections.

Information:

When the direction of the motor is changed, the polarity is reversed. If the direction of rotation on the motor is changed during operation, the motor immediately brakes and turns in the other direction. This can result in very high current values. Therefore, we recommend short-circuiting the motor first (braking) and then changing to the other direction.

4.25.3.16.4.4 Error acknowledged

Name:
OvercurrentAcknowledge01 to OvercurrentAcknowledge03
OvertemperatureAcknowledge
UndervoltageAcknowledge

This register contains bits used to acknowledge an overcurrent error, an undervoltage error and an overtemperature error.

The errors are acknowledged with a rising edge. An existing error can only be acknowledged if the cause of the error has been corrected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0	OvercurrentAcknowledge01	1	With a rising edge, the overcurrent error shown on channel 1 is acknowledged.
1	OvercurrentAcknowledge02	1	With a rising edge, the overcurrent error shown on channel 2 is acknowledged.
2	OvercurrentAcknowledge03	1	With a rising edge, the overcurrent error shown on channel 3 is acknowledged.
3 - 5	Reserved	-	
6	OvertemperatureAcknowledge	1	With a rising edge, the overtemperature error shown is acknowledged.
7	UndervoltageAcknowledge	1	With a rising edge, the undervoltage error shown is acknowledged.

4.25.3.16.5 Communication

4.25.3.16.5.1 Voltage of the channels

Name:
CurrentInput01 to CurrentInput03

Every 700 µs, the current that flows through a channel is measured with a resolution of 8 bits. The value measured is stored in these registers.

Data type	Value	Information
USINT	0 to 255	0 to 5 A

4.25.3.16.5.2 Module and channel status

Name:
OvercurrentError01 to OvercurrentError03
StatusDigitalOutput01 to StatusDigitalOutput03
OvertemperatureError
UndervoltageError

Some operating states are monitored by the module. They are:

- Module supply
- Module current
- Status channels
- Module temperature

The states are stored in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0	OvercurrentError01	0	No overcurrent on channel 1
		1	Overcurrent on channel 1
1	OvercurrentError02	0	No overcurrent on channel 2
		1	Overcurrent on channel 2
2	OvercurrentError03	0	No overcurrent on channel 3
		1	Overcurrent on channel 3
3	StatusDigitalOutput01	0	Channel 1 output status OK
		1	Channel 1 output warning: Short-circuit or invalid output status
4	StatusDigitalOutput02	0	Channel 2 output status OK
		1	Channel 2 output warning: Short-circuit or invalid output status
5	StatusDigitalOutput03	0	Channel 3 output status OK
		1	Channel 3 output warning: Short-circuit or invalid output status
6	OvertemperatureError	0	Module temperature within permitted range
		1	Module overtemperature error
7	UndervoltageError	0	Supply voltage within permitted range
		1	Supply voltage has dropped below 18V

4.25.3.16.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
400 µs

4.25.3.16.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
400 µs

4.25.4 X20MM4331

4.25.4.1 General information

The 4 outputs on the motor module are designed as half-bridge outputs. The continuous current per channel is 3 A at a peak current of up to 5 A. Integrated diagnostics offer the possibility to read back the output current for each channel using the application.

The module offers extensive possibilities for controlling motors, valves or resistive loads and is particularly well suited for controlling brush DC motors. The outputs can be switched on/off and short-circuited.

- 4 half-bridge outputs
- High component density
- 3 A continuous current
- 5 A peak current
- Readable current

4.25.4.2 Order data

Model number	Short description	Figure
	Motor controllers	
X20MM4331	X20 digital motor module, 24 VDC, 4 digital outputs, half bridge, 3 A continuous current, 5 A peak current	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 560: X20MM4331 - Order data

4.25.4.3 Technical data

Product ID	X20MM4331
Short description	
I/O module	4 half-bridge outputs
General information	
B&R ID code	0xA976
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Output	Yes, using status LED and software
I/O supply	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.8 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
External I/O supply bus	Yes
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Motor bridge - Power unit	
Quantity	4
Type	Half bridge High-side driver Low-side driver

Table 561: X20MM4331 - Technical data

Product ID	X20MM4331
Nominal voltage	24 VDC
Switching voltage	24 VDC (-15% / +20%)
Nominal current	3 A
Maximum current	5 A (250 ms)
Total nominal current	10 A
Current value measurement	
Resolution	100 mA
Data collection	On the high-side branch
Output protection	Thermal cutoff for overcurrent and short circuit
Supply voltage	No reverse polarity protection
Isolation voltage between channel and bus	500 V_{eff}
Digital outputs	
Quantity	4
Nominal voltage	24 VDC
Output protection	Thermal cutoff for overcurrent and short circuit
Type	Half bridge High-side driver (Source) Low-side driver (Sink)
Max. continuous current per output	3 A
Max. module current	10 A
Recording the current value on the high branch	
Resolution	100 mA
Operating conditions	
Mounting orientation	
Horizontal	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 50°C
Vertical installation	Not permitted
Derating	See section "Derating"
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 561: X20MM4331 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.25.4.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

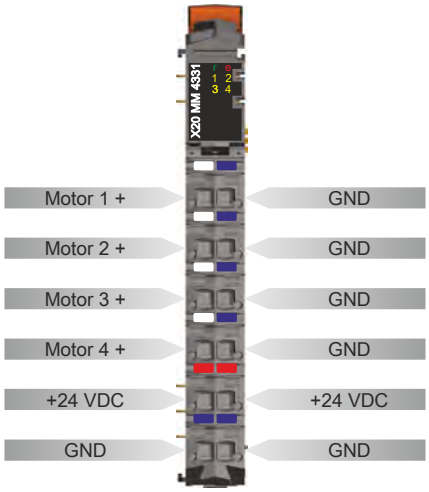
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Off	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange	On	The corresponding output is active
			Blinking	Error on the corresponding output
			Off	The corresponding output is switched off

4.25.4.5 Pinout

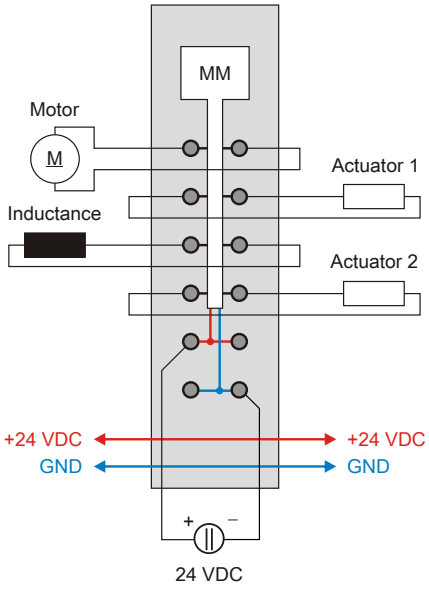
Lines with a cross section between a minimum of 0.75 mm² and a maximum of 2.5 mm² are recommended for the outputs.

Warning!

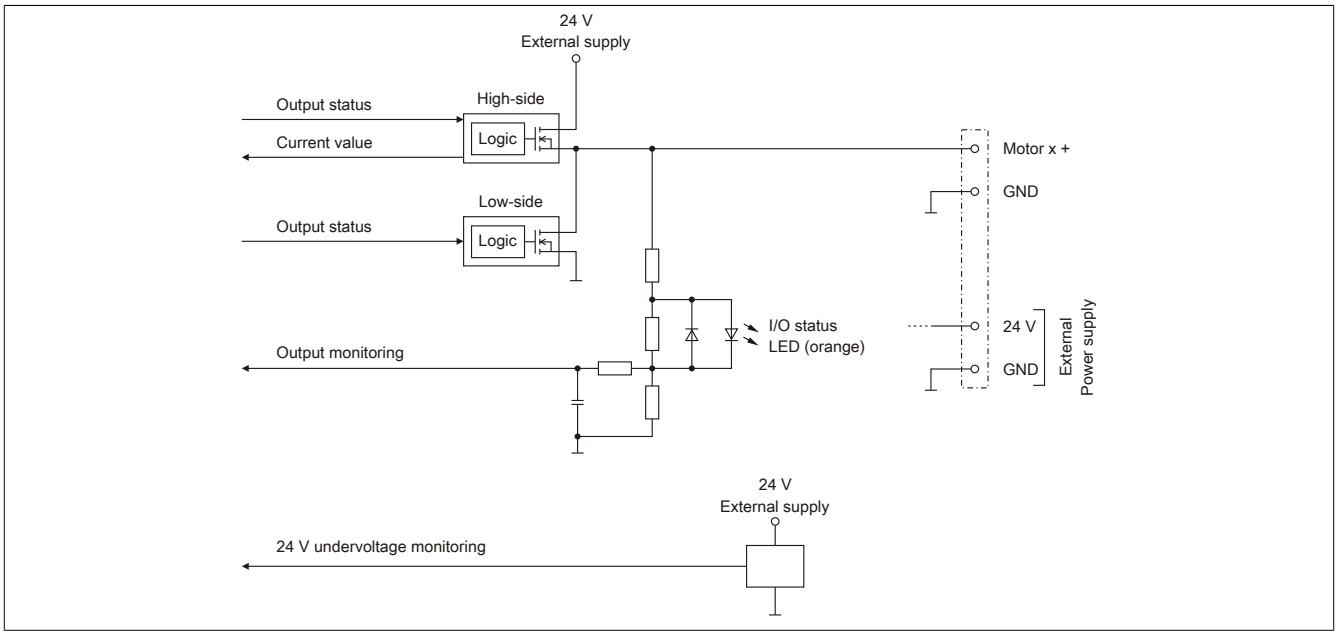
The terminal block is not permitted to be plugged in or unplugged during operation.



4.25.4.6 Connection example

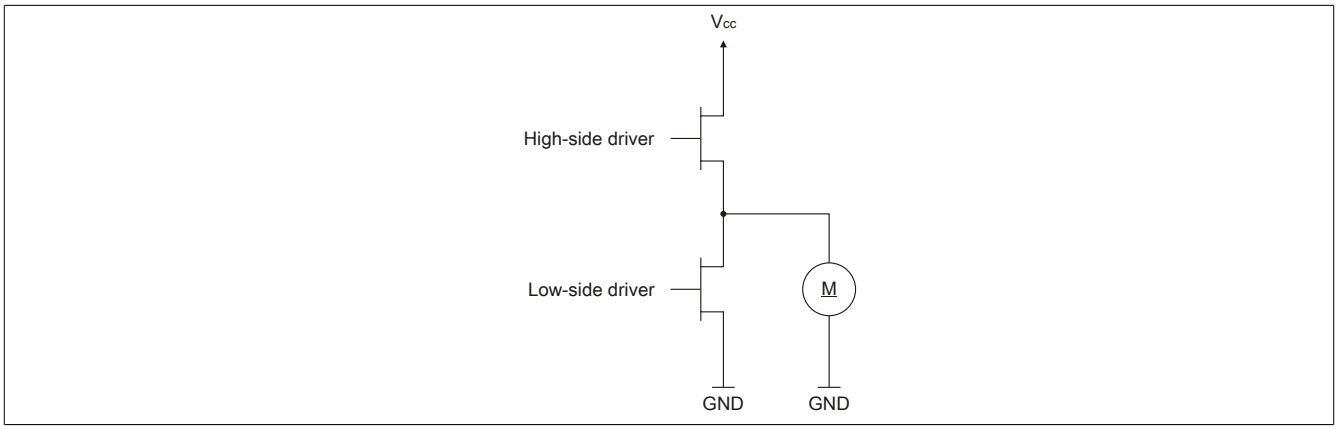


4.25.4.7 Output circuit diagram



4.25.4.8 Function description - Motor operation

Four DC motors can be operated with the module. Each output is designed as a half-bridge.



Description of the operating modes using the basic circuit diagram shown above:

Operating mode	Description
Motor is running	If the high-side driver is active, the motor is switched on.
Brakes	If motor braking should take place, the high-side driver is first switched off and then the low-side driver is activated. In this way, the motor windings are short-circuited and the motor braking takes place.

4.25.4.9 Protection

The power supply line should be protected by a circuit breaker or a fuse. In general, dimensioning the supply line and overcurrent protection depends on the structure of the power supply (modules can be connected individually or in groups).

Information:

The effective current for the power supply depends on the load, but is always less than the sum of the output currents. Make sure that the maximum nominal current of 31 A per pin is not exceeded on the power supply terminals of the power unit.

When choosing a suitable fuse, the user must also account for characteristics such as aging effects, temperature derating, overcurrent capacity and the definition of the rated current, which can vary by manufacturer and type. In addition, the fuse that is selected must also be able to handle application-specific characteristics (e.g. overcurrent that occurs in acceleration cycles).

The cross section of the power mains and the rated current of the overcurrent protection used are chosen according to the current load so that the maximum current load for the cable cross section selected (based on the type of layout, see table) is greater than or equal to the current load in the power mains. The rated current of the overcurrent protection must be less than or equal to the maximum current load for the cable cross section selected (based on the type of layout, see table):

I_{Mains}	≤	I_b	≤	I_Z
Mains	≤	Fuse	≤	Line/cable

Wire cross section [mm²]	Current load of the cable cross section I_Z / rated current of the over current protection I_b [A] according to type of installation in an ambient air temperature of 40°C in accordance to IEC 60204-1			
	B1	**B2**	**C**	**E**
1.5	13.5 / 13	13.1 / 10	15.2 / 13	16.1 / 16
2.5	18.3 / 16	16.5 / 16	21 / 20	22 / 20
4.0	24.0 / 24.0	23.0 / 20.0	28.0 / 25.0	30.0 / 25.0
6.0	32.0 / 32.0	29.0 / 25.0	36.0 / 32.0	37.0 / 32.0

Table 562: Cable cross section of the mains supply line depending on the type of layout

The tripping current of the fuse cannot exceed the rated current of fuse I_b.

Type of layout	Description
B1	Wires in conduit or cable duct
B2	Cables in conduit or cable duct
C	Cables or wires on walls
E	Cables or wires on open cable tray

Table 563: Type of layout for the mains supply line

4.25.4.10 Derating

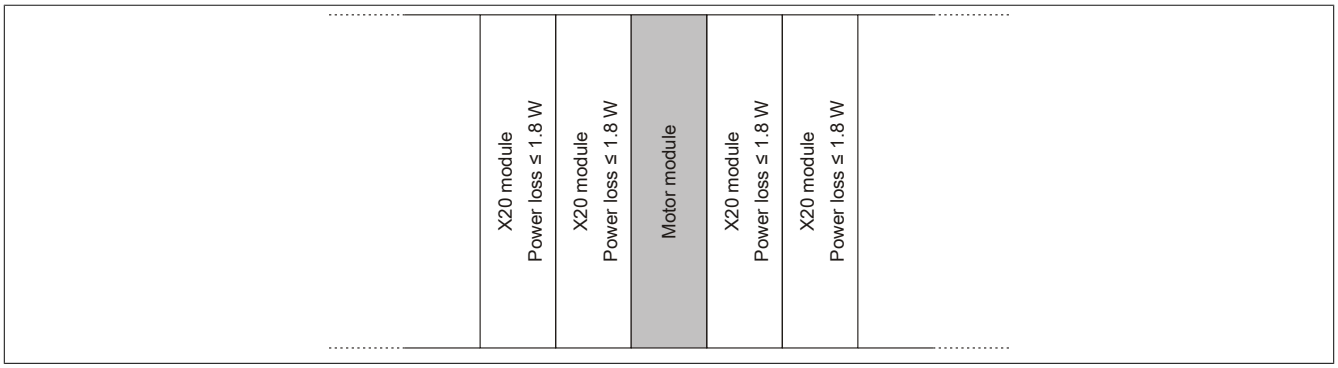
In order to be able to operate the motor module over the entire temperature range, only modules with a maximum power loss of of 0.5 W can be installed next to the motor module or respective turn-off times must be implemented.

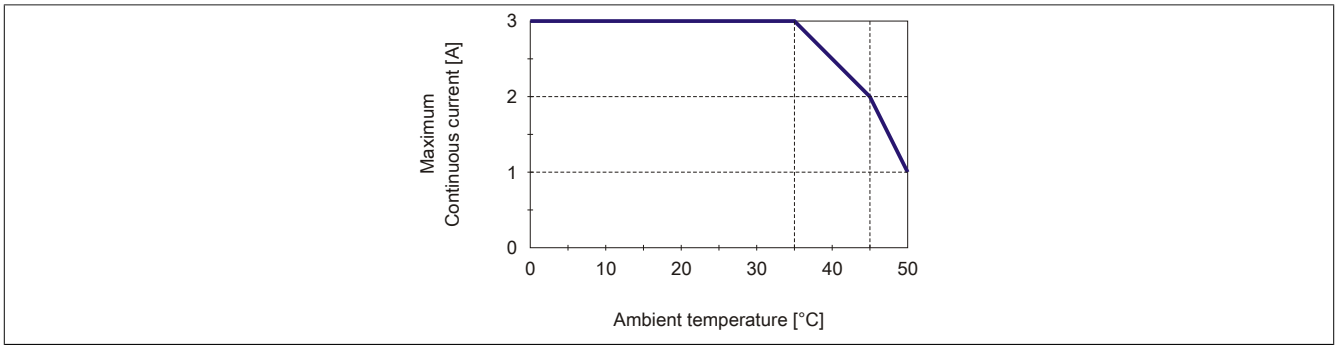
If the neighboring modules have a higher power loss and all channels are operated continuously, the motor current must be derated.

When a motor is switched on, the current is increased for a short time. This behavior has no influence on the derating.

Current derating 1 of the motor module

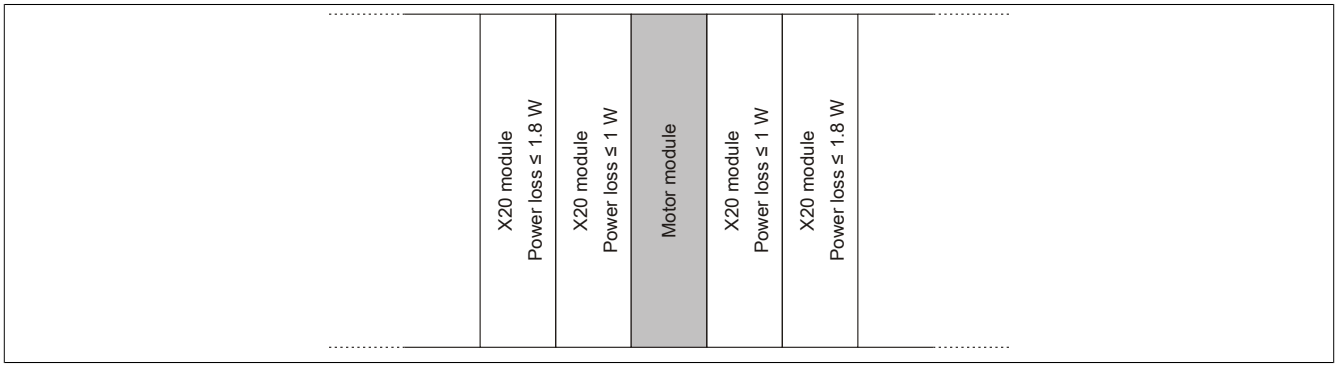
Current derating for the motor module for neighboring modules with ≤1.8 W thermal power loss.

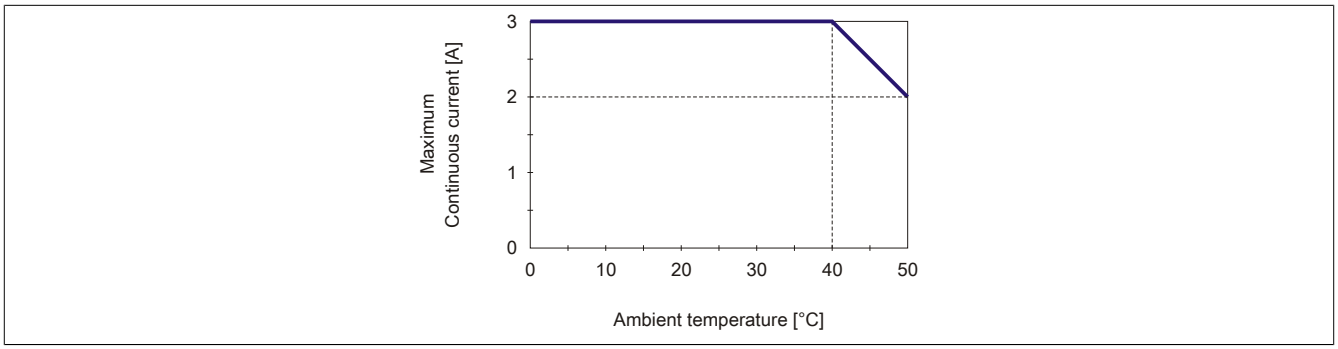




Current derating 2 of the motor module

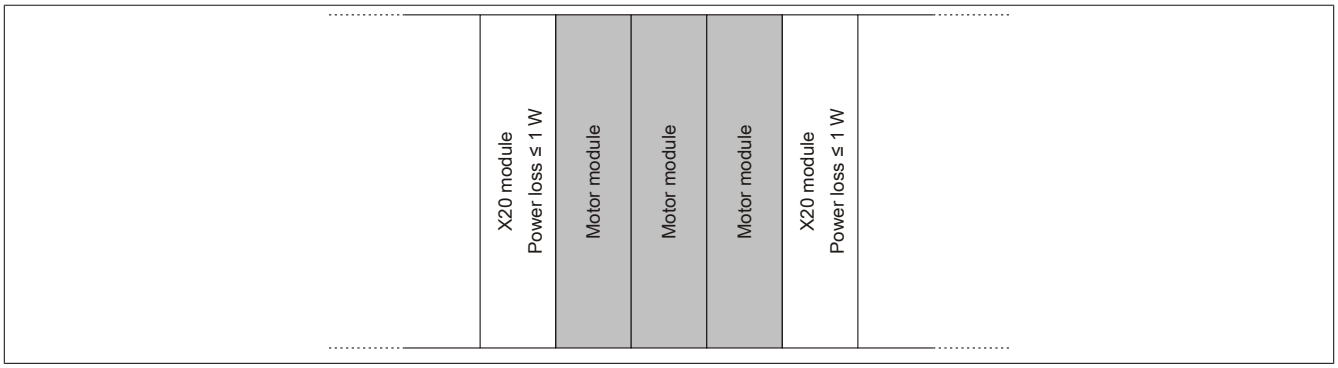
Current derating for the motor module for neighboring modules with ≤1 W thermal power loss.

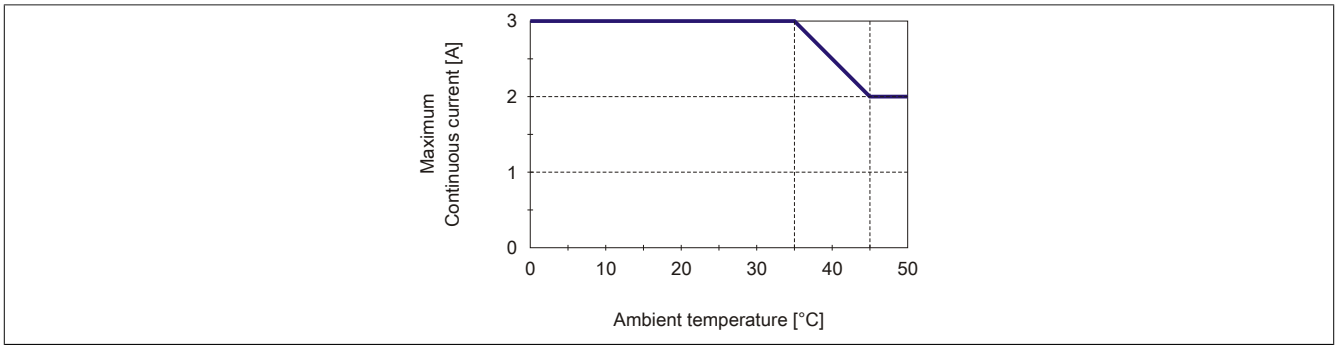




Current derating 3 of the motor module

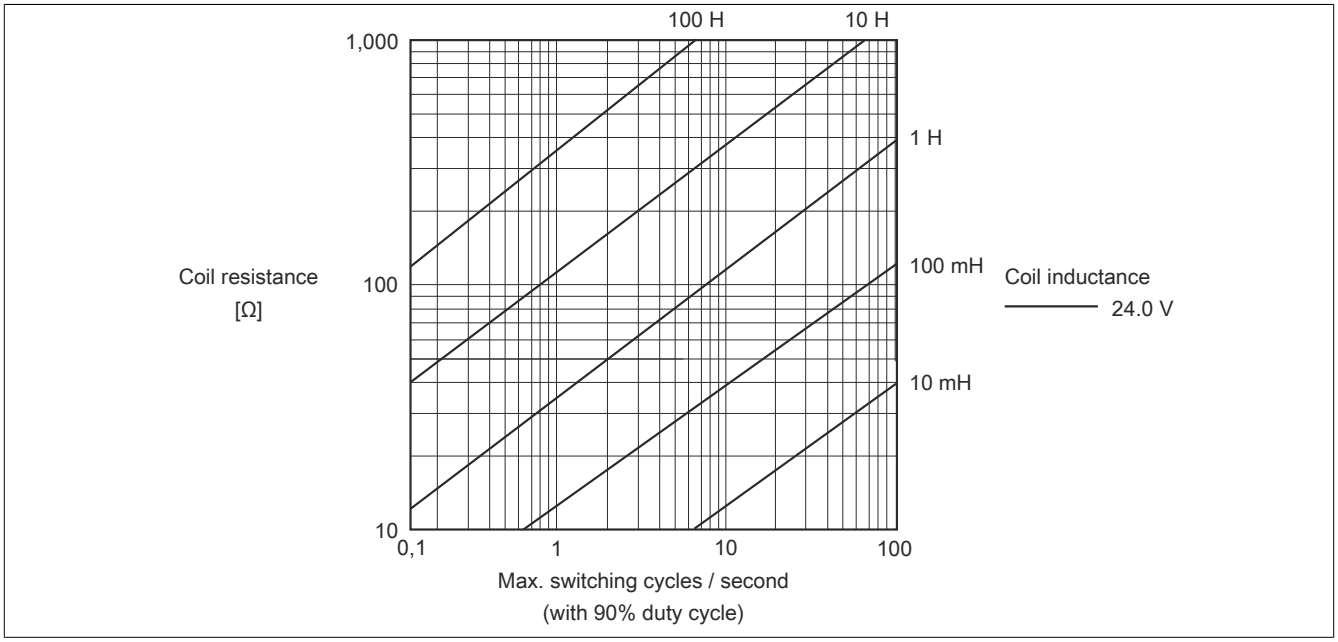
Current derating with multiple motor modules next to each other.





4.25.4.11 Switching inductive loads (e.g. valves)

All outputs with the same load.



4.25.4.12 Monitoring the module supply

The module supply is continually monitored. If the supply voltage drops below 18V, all channels are switched off and an error bit is set.

Information:

The undervoltage must be present for longer than 250 ms, before all channels are switched off. Power dips can occur when starting motors or capacitive loads!

4.25.4.13 Monitoring the module current

The module current is continually monitored. If an overcurrent occurs, the respective channel is switched off and an error bit is set.

Information:

The overcurrent must be present for longer than 250 ms, before the channel is switched off. High starting currents occur when starting motors or capacitive loads!

4.25.4.14 Channel monitoring

After each switching process, the status inputs are checked with a 2 ms delay to ensure they are correct. This is done so that faulty status signals are not generated when switching motors or capacitive loads.

If the status of the output does not correspond to the status that is expected (e.g. short circuit or motor spin-out), a warning bit is set.

Information:

When channel monitoring is triggered, a warning is given. The output remains switched even if there is a short circuit and is cycled to the output by the internal protective circuit.

If the motor is still spinning out, the voltage drops slowly. That means the warning bit StatusDigitalOutput can show a warning while the motor is spinning out.

If the motor is moved externally, voltage is induced into the module, which results in StatusDigitalOutput being set and the red LED being lit (warning).

4.25.4.15 Overtemperature cutoff (at 85°C)

If the module temperature reaches or exceeds the limit value of 85°C, then the module executes the following actions:

- Setting the "overtemperature" error bit
- The outputs are switched off (short-circuited)

As soon as the temperature sinks back down below 85°C, the error must be acknowledged with OvertemperatureAcknowledge so that the channels can be switched on again.

4.25.4.16 Register description

4.25.4.16.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.25.4.16.2 Function model 0 - Standard

In this function model, control of full bridges takes place using 3 bits per channel.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
0	Motor configuration - Default	USINT			•	
	StartChannel01	Bit 0				
	ShortCircuitChannel01	Bit 1				
	StartChannel02	Bit 2				
	ShortCircuitChannel02	Bit 3				
	StartChannel03	Bit 4				
	ShortCircuitChannel03	Bit 5				
	StartChannel04	Bit 6				
	ShortCircuitChannel04	Bit 7				
18	Error acknowledged	USINT			•	
	OvercurrentAcknowledge01	Bit 0				
	...	...				
	OvercurrentAcknowledge04	Bit 3				
	OvertemperatureAcknowledge	Bit 5				
	UndervoltageAcknowledge	Bit 6				
Communication						
2 + N * 2	CurrentInput0N (Index N = 1 to 4)	USINT	•			
20	Status of current and channels	USINT	•			
	OvercurrentError01	Bit 0				
	...	...				
	OvercurrentError04	Bit 3				
	StatusDigitalOutput01	Bit 4				
	...	...				
	StatusDigitalOutput04	Bit 7				
21	Module status	USINT	•			
	OvertemperatureError	Bit 0				
	UndervoltageError	Bit 1				

4.25.4.16.3 Function model 1 - Byte control and Function model 254 - bus controller

Control of the half bridges takes place using one byte (two bits per channel). All other registers are the same as in Function model 0 - Standard.

This function model supports all of the module's functions. Control of the half bridges takes place using one byte (2 bits per channel). All other registers are the same as the standard function model.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
0	0	Motor configuration - Byte control	USINT			•	
18	12	Error acknowledged	USINT			•	
		OvercurrentAcknowledge01	Bit 0				
		...	...				
		OvercurrentAcknowledge04	Bit 3				
		OvertemperatureAcknowledge	Bit 5				
		UndervoltageAcknowledge	Bit 6				
Communication							
2 + N * 2	2 + N * 2	CurrentInput0N (Index N = 1 to 4)	USINT	•			
20	8	Status of current and channels	USINT	•			
		OvercurrentError01	Bit 0				
		...	...				
		OvercurrentError04	Bit 3				
		StatusDigitalOutput01	Bit 4				
		...	...				
		StatusDigitalOutput04	Bit 7				
21	10	Module status	USINT	•			
		OvertemperatureError	Bit 0				
		UndervoltageError	Bit 1				

1) The offset specifies the position of the register within the CAN object.

4.25.4.16.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.25.4.16.4 Configuration

4.25.4.16.4.1 Motor configuration - Default

Name:
StartChannel01 to StartChannel04
ShortCircuitChannel01 to ShortCircuitChannel04

This register contains the control bits for all channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0	StartChannel01	0	Switch off channel 1
		1	Channel 1 is started (bridge control)
1	ShortCircuitChannel01	0	Do not short circuit channel 1.
		1	Short circuit channel 1.
2	StartChannel02	0	Switch off channel 2
		1	Channel 2 is started (bridge control)
3	ShortCircuitChannel02	0	Do not short circuit channel 2.
		1	Short circuit channel 2.
4	StartChannel03	0	Switch off channel 3
		1	Channel 3 is started (bridge control)
5	ShortCircuitChannel03	0	Do not short circuit channel 3.
		1	Short circuit channel 3.
6	StartChannel04	0	Switch off channel 4
		1	Channel 4 is started (bridge control)
7	ShortCircuitChannel04	0	Do not short circuit channel 4.
		1	Short circuit channel 4.

Information:

To avoid internal bridge shorts, the outputs are delayed by 200 µs when switching to another state or a short circuit.

4.25.4.16.4.2 Motor configuration - Byte control

Name:
ControlByte01

This register is used to control all four channels. Two bits per channels are always grouped together. This register is only used in Function model 1 - Byte control and Function model 254 - bus controller.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0 - 1	Channel 1	00	Off
		01	On
		10	Off
		11	Short circuit
...		...	
6 - 7	Channel 4	00	Off
		01	On
		10	Off
		11	Short circuit

4.25.4.16.4.3 Error acknowledged

Name:
OvercurrentAcknowledge01 to OvercurrentAcknowledge04
OvertemperatureAcknowledge
UndervoltageAcknowledge

This register contains bits used to acknowledge an overcurrent error, an undervoltage error and an overtemperature error.

The errors are acknowledged with a rising edge. An existing error can only be acknowledged if the cause of the error has been corrected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0	OvercurrentAcknowledge01	1	With a rising edge, the overcurrent error shown on channel 1 is acknowledged.
...		...	
3	OvercurrentAcknowledge04	1	With a rising edge, the overcurrent error shown on channel 4 is acknowledged.
4 - 5	Reserved	-	
6	OvertemperatureAcknowledge	1	With a rising edge, the overtemperature error shown is acknowledged.
7	UndervoltageAcknowledge	1	With a rising edge, the undervoltage error shown is acknowledged.

4.25.4.16.5 Communication

4.25.4.16.5.1 Voltage of the channels

Name:
CurrentInput01 to CurrentInput04

Every 500 µs, the current that flows through a channel is measured with a resolution of 8 bits. The value measured is stored in these registers.

Data type	Value	Information
USINT	0 to 255	0 to 5 A

4.25.4.16.5.2 Status of current and channels

Name:
OvercurrentError01 to OvercurrentError04
StatusDigitalOutput01 to StatusDigitalOutput04

Some operating states are monitored by the module. They are:

- Module current
- Status channels

The states are stored in this register. For other operating modes, see 4.25.4.16.5.3 "Module status"

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0	OvercurrentError0	0	No overcurrent on channel 1
		1	Overcurrent on channel 1
...		...	
3	OvercurrentError04	0	No overcurrent on channel 4
		1	Overcurrent on channel 4
4	StatusDigitalOutput01	0	Channel 1 output status OK
		1	Channel 1 output warning: Short-circuit or invalid output status
...		...	
7	StatusDigitalOutput04	0	Channel 4 output status OK
		1	Channel 4 output warning: Short-circuit or invalid output status

4.25.4.16.5.3 Module status

Name:
OvertemperatureError
UndervoltageError

Some operating states are monitored by the module. They are:

- Module supply
- Module temperature

The states are stored in this register. For other operating modes, see 4.25.4.16.5.2 "Status of current and channels"

Data type	Value
USINT	See bit structure.

Bit structure:

Bit			Description
0	OvertemperatureError	0	Module temperature within permitted range
		1	Module overtemperature error
1	UndervoltageError	0	Supply voltage within permitted range
		1	Supply voltage has dropped below 18V
2 - 7	Reserved	-	

4.25.4.16.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
400 µs

4.25.4.16.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
400 µs

4.25.5 X20MM4456

4.25.5.1 General information

The PWM motor bridge module is used to control 4 DC motors with a nominal voltage of 24 to 48 VDC ±25% at a nominal current up to 6 A. The module can be reconfigured and used in current controller mode for controlling inductive loads. The module is also equipped with 16 digital inputs, which can be used as incremental counters. The 4 motors are controlled with a full-bridge (H-bridge). This enables the motors to be moved in both directions.

- 4x outputs (H bridge) with PWM control and 24 to 48 VDC ±25% supply
- 6 A nominal current (10 A max current)
- 15 Hz to 50 kHz frequency, 16-bit
- PWM resolution, 15-bit, + sign, minimum 10 ns
- Configurable dither
- 4x 4 inputs 24V, can be configured as ABR
- Sink connection
- 1-wire connections

4.25.5.2 Order data

Model number	Short description	Figure
	Motor controllers	
X20MM4456	X20 PWM motor module, 24 to 48 VDC ±25%, 4 PWM motor bridges, 6 A continuous current, 10 A peak current, 4x 4 digital inputs 24 VDC, sink, configurable as incremental encoder	
	Required accessories	
	Terminal blocks	
0TB3103-7020	Accessory terminal block, 3-pin, screw clamps 6 mm²	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 564: X20MM4456 - Order data

4.25.5.3 Technical data

Product ID	X20MM4456
Short description	
I/O module	4-channel PWM motor bridge, 4 ABR incremental encoders
General information	
B&R ID code	0xA177
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Output	Yes, using status LED and software
I/O supply	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	2.4 W
External I/O 50 kHz	
24 VDC	3.3 W / channel
48 VDC	4.7 W / channel
60 VDC	5.4 W / channel
External I/O 10 kHz	
24 VDC	2.1 W / channel
48 VDC	2.4 W / channel
60 VDC	2.6 W / channel
External I/O 5 kHz	
24 VDC	2 W / channel
48 VDC	2.1 W / channel
60 VDC	2.2 W / channel
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
KC	Yes
GOST-R	Yes
Digital inputs	
Quantity	16
Nominal voltage	24 VDC
Input voltage	24 VDC (-15% / +20%)
Input current at 24 VDC	Approx. 4 mA
Input filter	
Hardware	<5 µs
Software	-
Connection type	1-wire connections
Input circuit	Sink
Additional functions	4x ABR incremental encoder
Input resistance	Typ. 6 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
ABR incremental encoder	
Quantity	4
Encoder inputs	24 V, asymmetrical
Counter size	16-bit
Input frequency	Max. 50 kHz
Evaluation	4x
Signal form	Square wave pulse
PWM output	
Quantity	4
Nominal voltage	24 to 48 VDC ±25%
Nominal current	6 A
Maximum current	10 A (2 s)
PWM frequency	15 Hz to 50 kHz
Actuator supply	
Supply	External
Fuse	Required line fuse: Max. 32 A slow-blow (see "Overcurrent protection")
Output protection	Thermal cutoff for overcurrent and short circuit
Design	H bridge
Configurable dither	Amplitude, frequency
Period resolution	16-bit, min. 20 µs
Phase shift PWM1, 2, 3, 4	each 90°
DC bus capacitance	680 µF

Table 565: X20MM4456 - Technical data

Product ID	X20MM4456
PWM pulse width	
PWM mode	15-bit + sign ≥10 ns
Current mode	15-bit + sign ≥10 ns
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 50°C
Vertical installation	Not permitted
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 2x X20TB12 terminal block separately Order 1x 0TB3103-7020 terminal block separately
Spacing	87.5$^{+0.2}$ mm

Table 565: X20MM4456 - Technical data

4.25.5.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Status LED, left

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Green		Input state of the corresponding digital input
	M1 + M2	Orange	On	The corresponding output is active

1) Depending on the configuration, a firmware update can take up to several minutes.

Status LED, right

Figure	LED	Color	Status	Description
	9 - 16	Green		Input state of the corresponding digital input
	M3 + M4	Orange	On	The corresponding output is active

4.25.5.5 Connection elements

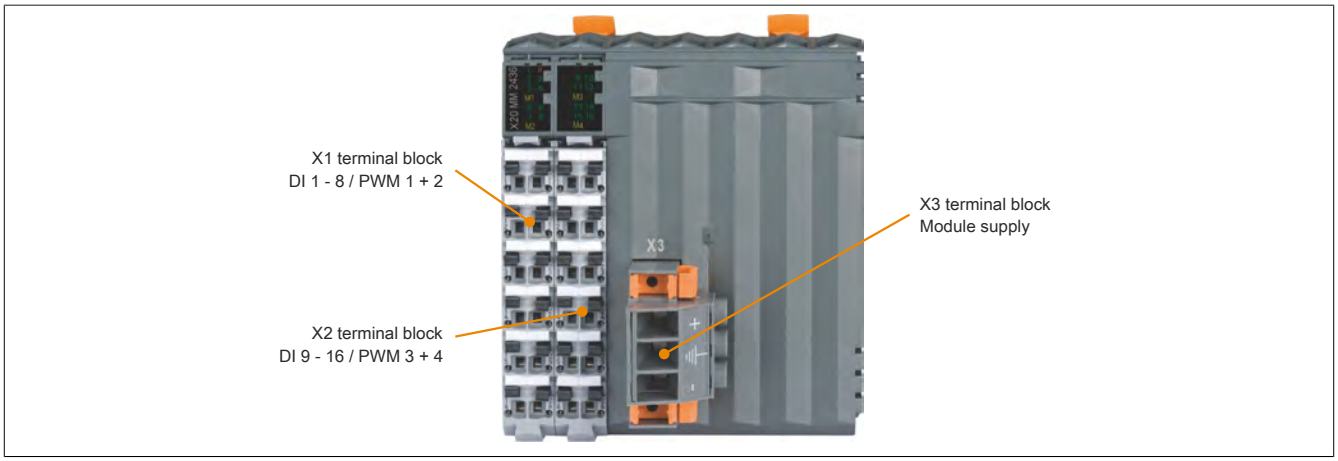
In accordance with the EN60204-1 standard, a cable cross section of 1.5 mm² or larger must be used for the motor outputs in order to handle the maximum motor current of 10 A. To ensure full motor power, voltage drops that could result from the cable length and the electrical connections must also be taken into consideration when selecting the attachment cable.

Warning!

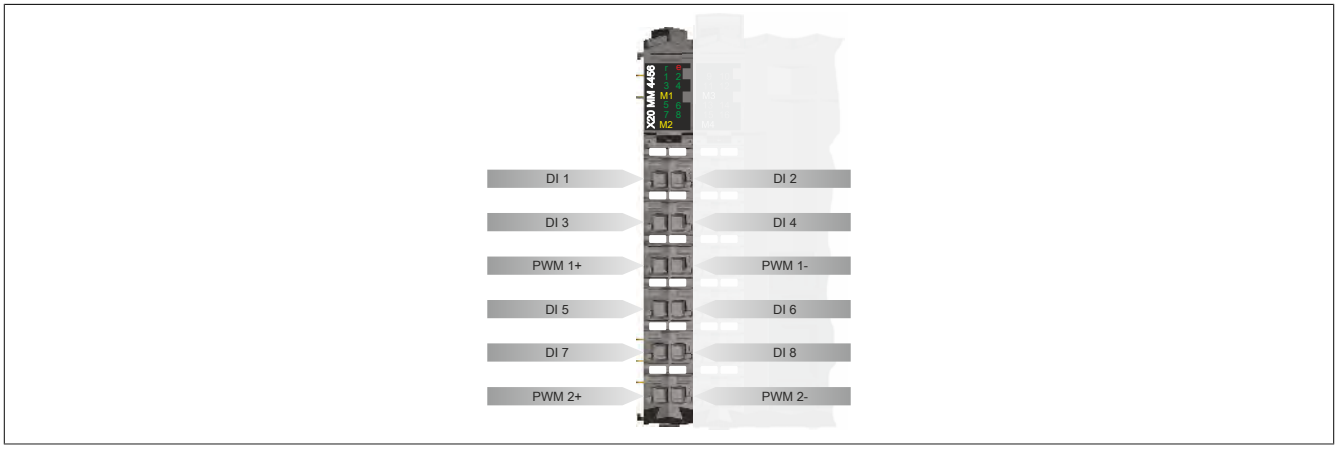
The terminal block is not permitted to be plugged in or unplugged during operation.

Information:

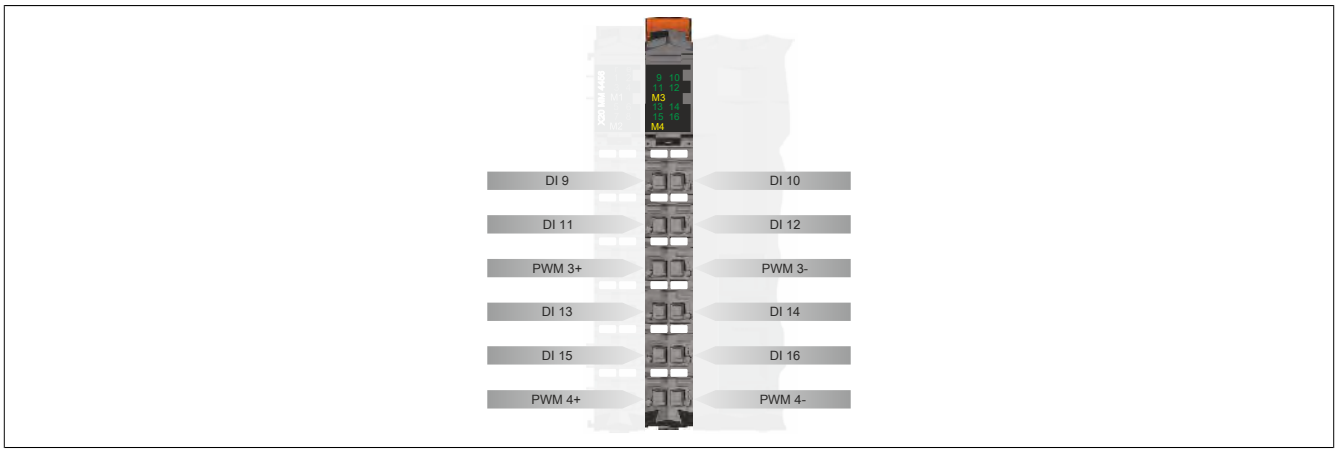
Shielded motor cables must be used in order to meet the limits according to the EN55011 standard (emissions).



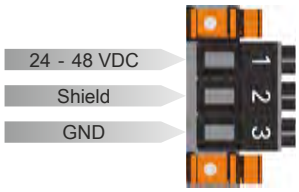
4.25.5.5.1 Terminal block X1 - DI 1 - 8 / PWM 1 + 2



4.25.5.5.2 Terminal block X2 - DI 9 - 16 / PWM 3 + 4



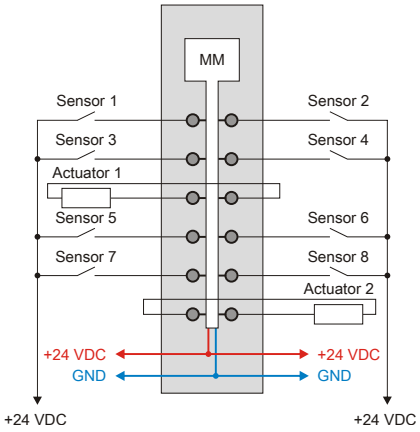
4.25.5.5.3 X3 terminal block - Module supply



4.25.5.6 Connection examples

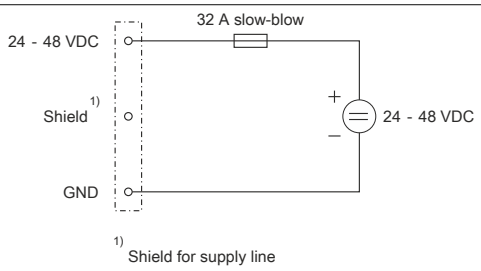
X1 and X2 terminal blocks

The following image shows a connection example for the X1 terminal block. The connection example also applies to the X2 terminal block.



X3 terminal block

For information on the fuse used, see 4.25.3.9 "Protection"



4.25.5.7 Possible uses for digital inputs

Digital input channels 1 to 16 can be used as follows:

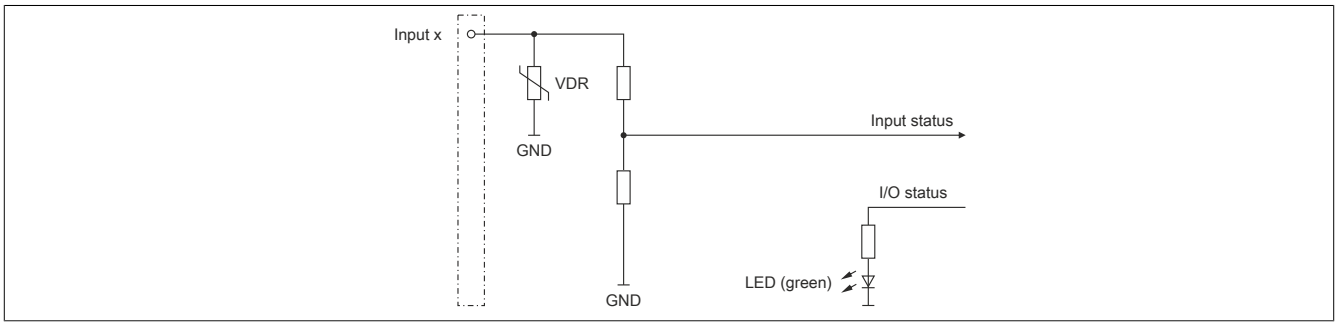
Channel	Function	Special functions
DI 1	Digital input	A
DI 2	Digital input	B
DI 3	Digital input	Limit switch, trigger, reference pulse
DI 4	Digital input	Limit switch, trigger, reference enable
DI 5	Digital input	A
DI 6	Digital input	B
DI 7	Digital input	Limit switch, trigger, reference pulse
DI 8	Digital input	Limit switch, trigger, reference enable
DI 9	Digital input	A
DI 10	Digital input	B
DI 11	Digital input	Limit switch, trigger, reference pulse
DI 12	Digital input	Limit switch, trigger, reference enable
DI 13	Digital input	A
DI 14	Digital input	B
DI 15	Digital input	Limit switch, trigger, reference pulse
DI 16	Digital input	Limit switch, trigger, reference enable

The functions can also be mixed:

Example 1	
Channel	**Function**
DI 1	Digital input
DI 2	Digital input
DI 3	Digital input
DI 4	Digital input
DI 5	Digital input
DI 6	Digital input
DI 7	Digital input
DI 8	Digital input
DI 9	A
DI 10	B
DI 11	R
DI 12	
DI 13	A
DI 14	B
DI 15	R
DI 16	

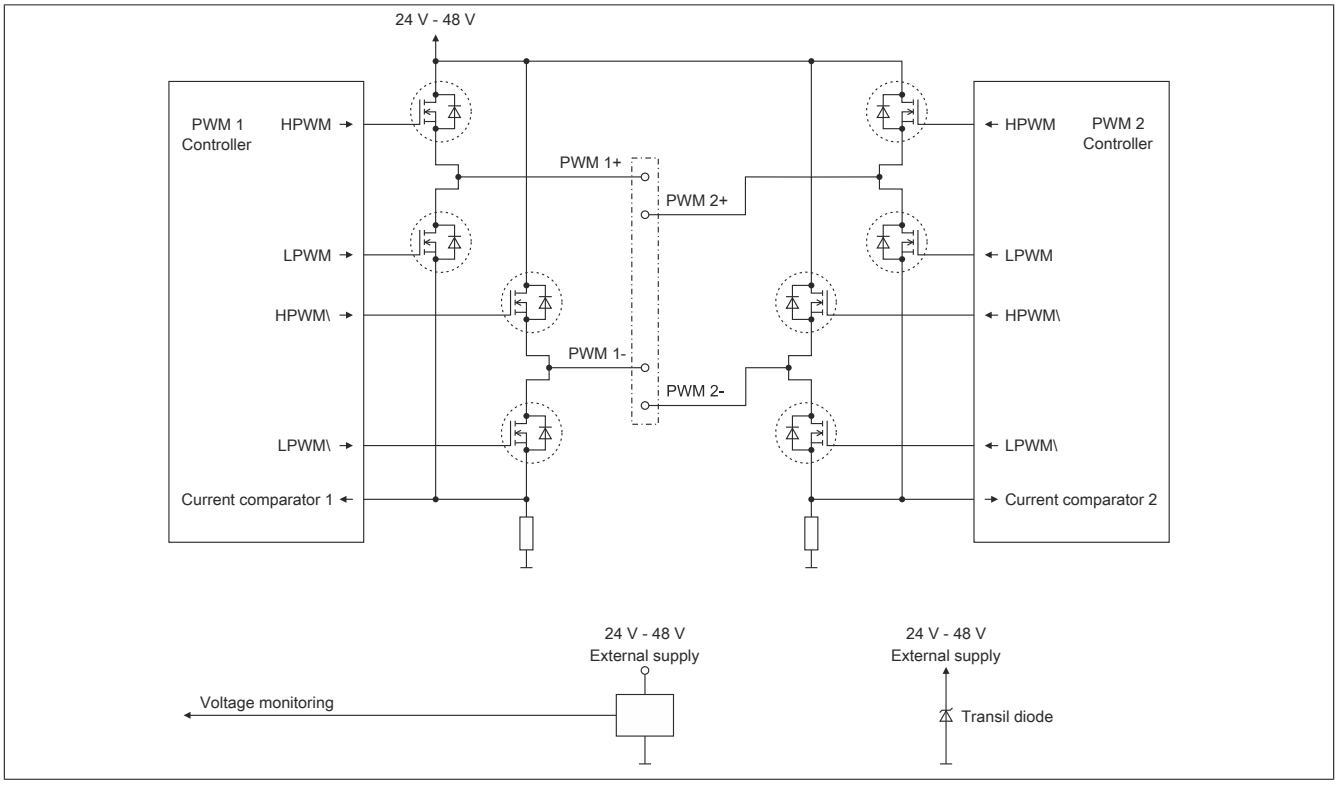
Example 2	
Channel	**Function**
DI 1	A
DI 2	B
DI 3	R
DI 4	
DI 5	Digital input
DI 6	Digital input
DI 7	Digital input
DI 8	Digital input
DI 8	Digital input
DI 10	Digital input
DI 11	Digital input
DI 12	Digital input
DI 13	A
DI 14	B
DI 15	R
DI 16	

4.25.5.8 Input circuit diagram



4.25.5.9 Output circuit diagram

The following image shows the output circuit diagram for the outputs 1 and 2. The diagram also applies to the outputs 3 and 4.



4.25.5.10 Protection

The power supply line should be protected by a circuit breaker or a fuse. In general, dimensioning the supply line and overcurrent protection depends on the structure of the power supply (modules can be connected individually or in groups).

Information:

The effective current for the power supply depends on the load, but is always less than the sum of the output currents. Make sure that the maximum nominal current of 31 A per pin is not exceeded on the power supply terminals of the power unit.

When choosing a suitable fuse, the user must also account for characteristics such as aging effects, temperature derating, overcurrent capacity and the definition of the rated current, which can vary by manufacturer and type. In addition, the fuse that is selected must also be able to handle application-specific characteristics (e.g. overcurrent that occurs in acceleration cycles).

The cross section of the power mains and the rated current of the overcurrent protection used are chosen according to the current load so that the maximum current load for the cable cross section selected (based on the type of layout, see table) is greater than or equal to the current load in the power mains. The rated current of the overcurrent protection must be less than or equal to the maximum current load for the cable cross section selected (based on the type of layout, see table):

I_{Mains}	≤	I_b	≤	I_Z
Mains	≤	Fuse	≤	Line/cable

Wire cross section [mm²]	Current load of the cable cross section I_Z / rated current of the over current protection I_b [A] according to type of installation in an ambient air temperature of 40°C in accordance to IEC 60204-1			
	B1	**B2**	**C**	**E**
1.5	13.5 / 13	13.1 / 10	15.2 / 13	16.1 / 16
2.5	18.3 / 16	16.5 / 16	21 / 20	22 / 20
4.0	24.0 / 24.0	23.0 / 20.0	28.0 / 25.0	30.0 / 25.0
6.0	32.0 / 32.0	29.0 / 25.0	36.0 / 32.0	37.0 / 32.0

Table 566: Cable cross section of the mains supply line depending on the type of layout

The tripping current of the fuse cannot exceed the rated current of fuse I_b.

Type of layout	Description
B1	Wires in conduit or cable duct
B2	Cables in conduit or cable duct
C	Cables or wires on walls
E	Cables or wires on open cable tray

Table 567: Type of layout for the mains supply line

4.25.5.11 Monitoring the module supply

The module supply is continually monitored. If the following limits are exceeded in either direction, an error bit is set.

Upper limit:	>80 V
Warning stage:	>60 V
Lower limit:	<18 V

4.25.5.12 Overvoltage cutoff

If the supply voltage on the module exceeds 80V (e.g. through feedback during generator operation), then all PWM outputs are disabled (PWM output pins are short-circuited). The outputs are reactivated as soon as the supply voltage is back in the valid range. Switching the outputs on again can cause an open load error in current mode (depending on the current setpoint and load inductance) as well as with any other abrupt change to the current setpoint value.

4.25.5.13 Overtemperature cutoff (at 85°C)

If the module temperature reaches or exceeds the limit value of 85°C, then the module executes the following actions:

- Setting the "overtemperature" error bit
- The PWM outputs are disabled (short-circuited)

Once the module temperature sinks to 83°C, the error bit is automatically cleared by the module and the outputs become operational again.

4.25.5.14 Measurement of effective current

In current controller mode (see bit 12 in the configuration register), there is an apparent deviation between the current setpoint and the measured effective current.

This is due to how the module operates. The PWM output remains "On" or in "Fast Decay" as long as needed to reach the current setpoint. Therefore, the current setpoint is the maximum or minimum current in a specified PWM cycle. This is why the effective current of this cycle (average current of this cycle) is lower (PWM = "On") or higher (PWM = "Fast Decay") than the current setpoint.

The size of the deviation depends on the load impedance.

4.25.5.15 Register description

4.25.5.15.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.25.5.15.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
0 + (N-1) * 8	PulseWidthCurrentPWM0N (Index N = 1 to 4)	INT			•	
4	PeriodDurationPWM	UINT			•	
2 + (N-1) * 8	Control	USINT			•	
	TriggerEdge0N	Bit 0				
	StartTrigger0N	Bit 1				
	StartLatch0N	Bit 2				
	DitherDisable0N	Bit 3				
	ClearError0N	Bit 4				
	ShowMeanCurrent0N	Bit 5				
	ResetCounter0N	Bit 6				
64	ConfigOutput01	USINT				•
65	ConfigOutput02	USINT				•
72 + (N-1) * 8	Configuration0N (Index N = 1 to 4)	UINT				•
Communication						
0 + (N-1) * 8	Counter0N (Index N = 1 to 4)	INT	•			
2 + (N-1) * 8	CounterLatch0N (Index N = 1 to 4)	INT	•			
4 + (N-1) * 8	usSinceTrigger0N (Index N = 1 to 4)	UINT	•			
6 + (N-1) * 8	Status0N (Index N = 1 to 4)	USINT	•			
	StatusInput(N-1)*4 + 1	Bit 0				
	...	...				
	StatusInput(N-1)*4 + 4	Bit 3				
	nLatchPending0N	Bit 4				
	LatchDone0N	Bit 5				
	EndswitchReached0N	Bit 6				
	PWMError0N	Bit 7				
7	Global error	USINT	•			
	OverVoltageError	Bit 4				
	UnderVoltageError	Bit 5				
	VoltageWarning	Bit 6				
	OvertemperatureError	Bit 7				
15	Channel errors	USINT	•			
	CurrentError01	Bit 0				
	OverCurrentError01	Bit 1				
	CurrentError02	Bit 2				
	OverCurrentError02	Bit 3				
	CurrentError03	Bit 4				
	OverCurrentError03	Bit 5				
	CurrentError04	Bit 6				
	OverCurrentError04	Bit 7				
128	ModuleTemperature	SINT		•		

4.25.5.15.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
0 + (N-1) * 8	0 + (N-1) * 8	PulseWidthCurrentPWM0N (Index N = 1 to 4)	INT			●	
4	4	PeriodDurationPWM	UINT			●	
2 + (N-1) * 8	2 + (N-1) * 8	Control	USINT			●	
		TriggerEdge0N	Bit 0				
		StartTrigger0N	Bit 1				
		StartLatch0N	Bit 2				
		DitherDisable0N	Bit 3				
		ClearError0N	Bit 4				
		ShowMeanCurrent0N	Bit 5				
		ResetCounter0N	Bit 6				
64	-	ConfigOutput01	USINT				●
65	-	ConfigOutput02	USINT				●
72 + (N-1) * 8	-	Configuration0N (Index N = 1 to 4)	UINT				●
Communication							
0 + (N-1) * 8	72 + (N-1) * 8	Counter0N (Index N = 1 to 4)	INT	●			
2 + (N-1) * 8	2 + (N-1) * 8	CounterLatch0N (Index N = 1 to 4)	INT	●			
4 + (N-1) * 8	4 + (N-1) * 8	usSinceTrigger0N (Index N = 1 to 4)	UINT	●			
6 + (N-1) * 8	6 + (N-1) * 8	Status of inputs	U(S)INT	●			
		StatusInput(N-1)*4 + 1	Bit 0				
		...	...				
		StatusInput(N-1)*4 + 4	Bit 3				
		nLatchPending0N	Bit 4				
		LatchDone0N	Bit 5				
		EndswitchReached0N	Bit 6				
		PWMError0N	Bit 7				
		CurrentError01	Bit 8				
		OverCurrentError01	Bit 9				
		CurrentError02	Bit 10				
		OverCurrentError02	Bit 11				
		CurrentError03 OverVoltageError	Bit 12				
		OverCurrentError03 UnderVoltageError	Bit 13				
		CurrentError04 VoltageWarning	Bit 14				
		OverCurrentError04 OvertemperatureError	Bit 15				
128	-	Temperature	SINT		●		

1) The offset specifies the position of the register within the CAN object.

4.25.5.15.3.1 CAN I/O bus controller

The module occupies 4 analog logical slots on CAN-I/O.

4.25.5.15.4 Configuration

4.25.5.15.4.1 Configuration

Name:
Configuration01 to Configuration04

These registers can be used to configure the four DC motors.

The following placeholders are used in the configuration table:

Register	[x]	In1	In2
Configuration01	1	DI3	DI4
Configuration02	2	DI7	DI8
Configuration03	3	DI11	DI12
Configuration04	4	DI15	DI16

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Configuration of latch function for ABR counter **[x]**. Activation of the latch function is described in the control register (bit 2):	00	ABR counter **[x]** is latched unconditionally (default setting). The reference enable input is ignored.
		01	ABR counter **[x]** is latched if a rising edge occurs on digital input **In1** and the reference enable input **In2** is "1". The reference enable input must be activated to do this (see bit 2).
		10	ABR counter 1 is latched if a rising edge occurs on digital input **In1** and the reference enable input **In2** is "1". The reference enable input must be activated to do this (see bit 2).
		11	The latch function is disabled.
2	Reference enable input:	0	No reference enable input
		1	Digital input **In2** is used as a reference enable input
3	Active level of the reference enable for ABR counter **[x]**:	0	Active level = High
		1	Active level = Low
4 - 5	Reserved	0	
6 - 7	Definition of the limit switch **[x]** (see also Limit switch function):	00	Limit switch 1 is disabled
		01	Digital input **In1** is used as the limit switch
		10	Digital input **In2** is used as the limit switch
		11	Digital inputs **In1** and **In2** are used as left and right limit switches
8	Active level for limit switch **[x]**:	0	Active level = High
		1	Active level = Low
9 - 10	Trigger input for trigger counter "µs Since Trigger **[x]**":	00	Trigger counter disabled
		01	Digital input **In1** is used as trigger input
		10	Digital input **In2** is used as trigger input
		11	Reserved
11	Displays the current average for output **[x]**:	0	If the corresponding setting has been activated, then the average current value is shown in the 4.25.5.15.5.2 "ABR counter**[x]** register (see bit 5 in the control register)
		1	If the corresponding setting has been activated, then the average current value is shown in the 4.25.5.15.5.3 "us_since_Trigger**[x]** register (see bit 5 in the control register).
12	Type of control for output **[x]**:	0	PWM control
		1	Current control
13 - 14	Decay configuration PWM **[x]** (see also 4.25.5.15.6 "Decay configuration"):	00	Slow decay (default setting)
		01	Mixed decay
		10 - 11	Reserved
15	Reserved	0	

Limit switch function

The limit switch function serves to quickly shut off the PWM outputs when a limit position is reached.

The limit switch is activated and the disable edge (rising or falling) on the limit switch input is selected using bits 6 to 8.

A PWM output is deactivated as soon as the configured disable edge is reached on the corresponding input of the limit switch. It remains deactivated until either the limit switch function is deactivated or the limit switch is acknowledged with bit 4 in the respective control register.

4.25.5.15.4.2 Control

Name:
TriggerEdge01 to TriggerEdge04
StartTrigger01 to StartTrigger04
StartLatch01 to StartLatch04
DitherDisable01 to DitherDisable04
ClearError01 to ClearError04
ShowMeanCurrent01 to ShowMeanCurrent04
ResetCounter01 to ResetCounter04

These registers can be used to configure the behavior of the trigger, the ABR counter and the dither.

[x] represents the corresponding control number.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	TriggerEdge**[x]** Configuration of trigger edge for "µs Since Trigger":	0	Counting starts at rising edge
		1	Counting starts at falling edge
1	StartTrigger**[x]** Status change of bit 1 enables the "µs Since Trigger"	x	Counting starts at the next trigger edge (see bit 0). For more information about trigger functionality, see "Trigger function procedure".
2	StartLatch**[x]** Latching and referencing ABR counter:	0	Disabled
		1	Enabled
3	DitherDisable **[x]**	0	Dither for PWM output **[x]** is enabled (default setting). The dither frequency and dither amplitude must be >0 (see 4.25.5.15.4.5 "Dither").
		1	Dither for PWM output **[x]** is disabled.
4	ClearError**[x]** Acknowledge error or limit switch:	0	No effect
		1	Error acknowledgment on output **[x]** (overcurrent or open load) or acknowledgment from limit switch **[x]**
5	ShowMeanCurrent**[x]** Configuration of registers ABR counter latch and us_since_Trigger	0	The register ABR counter latch **[x]** contains the latched counter value. The register µs Since Trigger **[x]** contains the trigger counter.
		1	Both registers contain the current PWM output current
6	ResetCounter[x] Reset ABR counter	0	Enable ABR counter (default)
		1	Reset ABR counter
7	Reserved	0	

Trigger function procedure

The following points must be taken into consideration when configuring or activating the trigger function:

- Select the desired trigger edge using bit 0
- Enable the trigger function by changing the state of StartTrigger (bit 1). This edge clears the register us_since_Trigger (µs counter).
- When the trigger event occurs, the µs counter "µs Since Trigger" is started
- The "µs Since Trigger" counter cannot overrun, i.e. the counter is stopped at 2^{16}-1 and retains this value until the next time the trigger function is activated
- The trigger function can be re-activated at any time by changing the state of StartTrigger (bit 1) regardless of if a trigger event has occurred or if "µs Since Trigger" has reached its maximum value.

Reset ABR counter

Bit 6 sets the following counters and status bits to 0:

- ABR counter
- Latch value of the ABR counter
- Latching started on the ABR counter (bit 4 of the status register)
- ABR counter successfully latched (bit 5 of the status register)

Please note that a started latch procedure is no longer active after the ABR counter has been reset. This means that latching must be restarted by a rising edge on bit 2.

4.25.5.15.4.3 PWM period duration

Name:
PeriodDurationPWM

This register can be used to set the period duration between 20 µs (50 kHz) and 65535 µs (15 Hz).

Data type	Value	Information
UINT	20 to 65535	Time in µs

4.25.5.15.4.4 PWM pulse width

Name:
PulseWidthCurrentPWM01 to PulseWidthCurrentPWM04

The PWM pulse width (PWM mode) or current setting (in current mode) is entered in this register according to the setting in the module configuration register. A negative value changes the output polarity.

PWM mode

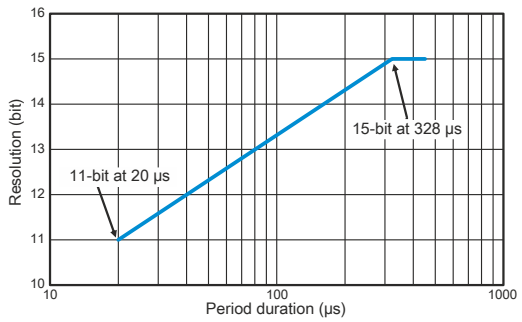
Data type	Value	Output +	Output -
INT	32767	High	Low
	16384	PWM 50/50	Low
	0	Low	Low
	-16384	Low	PWM 50/50
	-32767	Low	High

Current mode

Data type	Value	Current mode
INT	19661 to 32767	6 to 10 A (max. 2 s)
	19660	6 A
	0	0 A
	-19660	-6 A
	-19661 to -32767	-6 to -10 A (max. 2 s)

Resolution/Derating

As mentioned earlier in the technical data, the PWM resolution is 15-bit (+ sign). This value is derated for a period duration of less than 328 µs because of the minimal PWM timing resolution (10 ns) (see following diagram). With the minimum PWM period duration of 20 µs, the PWM has 11-bit resolution (+ sign):



4.25.5.15.4.5 Dither

A dither is used to prevent valves from sticking. This function is supported in both PWM mode and in current mode. The pulse width or current is adjusted according to the dither amplitude and dither frequency.

By default, the dither is active for both outputs as soon as the dither amplitude and dither frequency are set to a value >0. If necessary, the dither can be deactivated for each output individually or simultaneously (see bit 3 in the respective control register).

Dither amplitude

Name:
ConfigOutput01

This register can be used to configure the amplitude value or pulse width.
0 to 255 corresponds with an amplitude value from 0.0 to 25.5% of the nominal current or the maximum pulse width of 32767.

Data type	Value	Information
USINT	0 to 255	Amplitude value or pulse width

Dither frequency

Name:
ConfigOutput02

This register can be used to set the frequency in 2 Hz steps.

Data type	Value	Information
USINT	0 to 255	Corresponds to 0 to 510 Hz

Dither example

Valve specification	Valve specification is 20 to 35% peak to peak of the valve current at 5 A.
	This corresponds to a dither amplitude of ±5 to ±9% at 10 A. A midrange dither amplitude of 7% at 10 A is selected. This corresponds to a setting of 70.
Dither frequency specification	**40 to 70 Hz**
	A setting of 28 is selected. This corresponds to a frequency of 56 Hz.

4.25.5.15.5 Communication

4.25.5.15.5.1 ABR counter

Name:
Counter01 to Counter04

These registers are 16-bit AB(R) counters.

Data type	Value
INT	-32768 to 32767

4.25.5.15.5.2 ABR counter latch

Name:
CounterLatch01 to CounterLatch04

When a latch event occurs, the current counter values are saved in these registers. For additional features, see bit 5 in the respective control register.

Data type	Value
INT	-32768 to 32767

4.25.5.15.5.3 us_since_Trigger

Name:
usSinceTrigger01 to usSinceTrigger04

This register shows either the time in µs since the last trigger event or the average current value.

- The "µs Since Trigger" counter cannot overrun, i.e. the counter is stopped at 2^{16}-1 and retains this value until the next time the trigger function is activated
- If the average current is displayed in this register (bit 11 in the respective configuration register), then the data type of µs Since Trigger in Automation Studio must be unsigned integer (UINT). The average current value, on the other hand, is an Integer (INT). This means that negative currents are displayed between 32,769 and 65,535.

Counting mode

Data type	Value
UINT	0 to 65535

Measurement of average current value

Data type	Value	Information
INT	19,661 to 32,767	6 to 10 A
	19,660	6 A
	1	305 µA (= 10 A / 32,767)
	0	0 A
	65,535	-305 µA (= -10 A / 32,767)
	45,876	-6 A
	45,875 to 32,769	-6 to -10 A

4.25.5.15.5.4 Status of inputs

Name:
StatusInput01 to StatusInput16
nLatchPending01 to nLatchPending04
LatchDone01 to LatchDone04
EndswitchReached01 to EndswitchReached04
PWMError01 to PWMError0

These registers indicate the status of the inputs and outputs for each DC motor.

The following placeholders are used in the status table.

Register	[x]	In1	In2	In3	In4
Status of input 1	1	DI1	DI2	DI3	DI4
Status of input 2	2	DI5	DI6	DI7	DI8
Status of input 3	3	DI9	DI10	DI11	DI12
Status of input 4	4	DI13	DI14	DI15	DI16

Data type	Value
USINT[1)]	See bit structure.
UINT[2)]	See bit structure.

1) Function model 0 and function model 254 → Register "Status of input 3" and "Status of input 4"
2) Only function model 254 → Register "Status of input 1" and "Status of input 2"

Bit structure:

Bit	Description	Value	Information
0	StatusInput **[In1]**	x	**In1** is used for the encoder signal A of ABR counter **[x]**.
1	StatusInput **[In2]**	x	**In2** is used for the encoder signal B of ABR counter **[x]**.
2	StatusInput **[In3]**	0	Possible uses for the digital input • Trigger input **[x]** • Reference pulse for ABR counter **[x]** • Limit switch **[x]** (left)
3	StatusInput **[In4]**	0	Possible uses for the digital input • Reference enable **[x]** • Trigger input **[x]** • Limit switch **[x]** (right)
4	nLatchPending **[x]**	00	Latching started
		01	ABR counter latch **[x]** ready. Latch not yet started.
5	LatchDone **[x]**	0	The status of this bit is changed each time ABR counter **[x]** is successfully latched
6	EndswitchReached **[x]**	00	No effect on PWM output **[x]**
		01	Endswitch **[x]** reached. PWM output **[x]** disabled.
7	PWMError **[x]**	0	Error free operation
		1	An error has occurred. The error can be determined by evaluating the two error registers 4.25.5.15.5.6 "Global errors" and 4.25.5.15.5.5 "Channel errors".
8 - 15	**Only Function model 254**		
	Status of input 1	x	With "Status of inputs 1", bits 12 to 15 contain error bits 4 to 7 from the 4.25.5.15.5.6 "Global error" register.
	Status of input 2	x	With "Status of inputs 2", bits 8 to 15 contain error bits 0 to 7 from the 4.25.5.15.5.5 "Channel errors" register

4.25.5.15.5.5 Channel errors

Name:
CurrentError01 to CurrentError04
OverCurrentError01 to OverCurrentError04

If an error is detected, the corresponding error bit in this register remains set until the error is acknowledged using bit 4 in the respective "control register".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	CurrentError01	0	No error
		1	Open load error
1	OverCurrentError01	0	No error
		1	Overcurrent errorOutput deactivated.
2	CurrentError02	0	No error
		1	Open load error
3	OverCurrentError02	0	No error
		1	Overcurrent errorOutput deactivated.
4	CurrentError03	0	No error
		1	Open load error
5	OverCurrentError03	0	No error
		1	Overcurrent errorOutput deactivated.
6	CurrentError04	0	No error
		1	Open load error
7	OverCurrentError04	0	No error
		1	Overcurrent errorOutput deactivated.

Overcurrent error

An overcurrent error is registered if one of the following conditions is met:

- ≥10 A flow from a PWM output for at least 2 seconds
- ≥16 A flow for 3 consecutive PWM cycles
- All PWM outputs together consume more than 32 A on the X3 connector

In all three cases, the affected PWM output is deactivated by the firmware (i.e. the pins on the PWM output are short-circuited). The user must acknowledge the error using bit 4 in the respective control register before a PWM output deactivated in this manner can be made operational again.

Open load error

An open load error is only registered in current control mode (see bit 12 in the respective configuration register) if the current setpoint is not reached. In some cases this can be caused by an open line, although usually the impedance of the load is too high.

4.25.5.15.5.6 Global error

Name:
OverVoltageError
UnderVoltageError
VoltageWarning
OvertemperatureError

This register indicates overtemperature and errors in the module supply. The error bits are automatically acknowledged by the module as soon as the values are back within the permissible limits.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	0	
4	OverVoltageError	0	No error
		1	Voltage >80 V. All outputs are deactivated.
5	UnderVoltageError	0	No error
		1	Voltage <18 V
6	VoltageWarning	0	No error
		1	Voltage >60 V
7	OvertemperatureError	0	No error
		1	Module overtemperature; all outputs are deactivated.

4.25.5.15.5.7 Temperature

Name:
ModuleTemperature

The module temperature is displayed in this register.

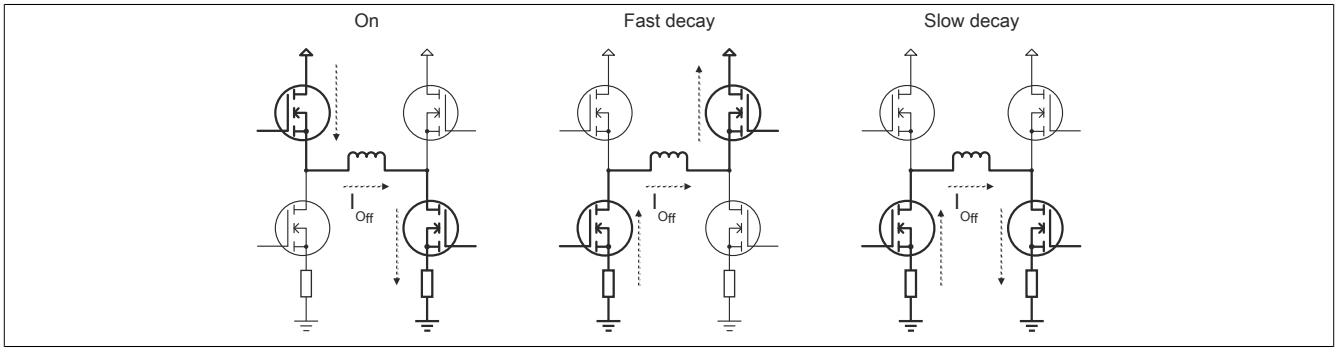
Data type	Value	Information
SINT	-40 to 125	Module temperature in °C

4.25.5.15.6 Decay configuration

The decay configuration determines the method and dynamics of current reduction for inductive loads or motors.

"Slow decay" is configured by default. In this mode, the current is automatically reduced relatively slowly with resistance in the load. No energy is regenerated into the module.

"Mixed decay" mode is recommended for applications that require a dynamic and linear reduction of current. In this mode, energy is regenerated into the module during part of the PWM cycle (fast decay).



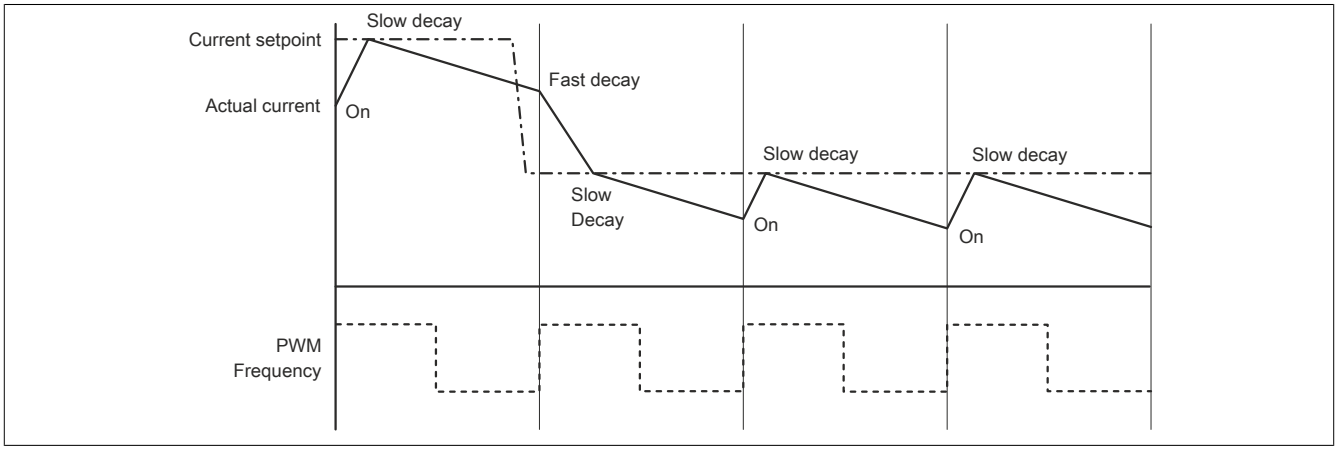
4.25.5.15.6.1 Current control

As its name suggests, mixed decay mode is a mix of "slow decay" and "fast decay". This occurs as follows:

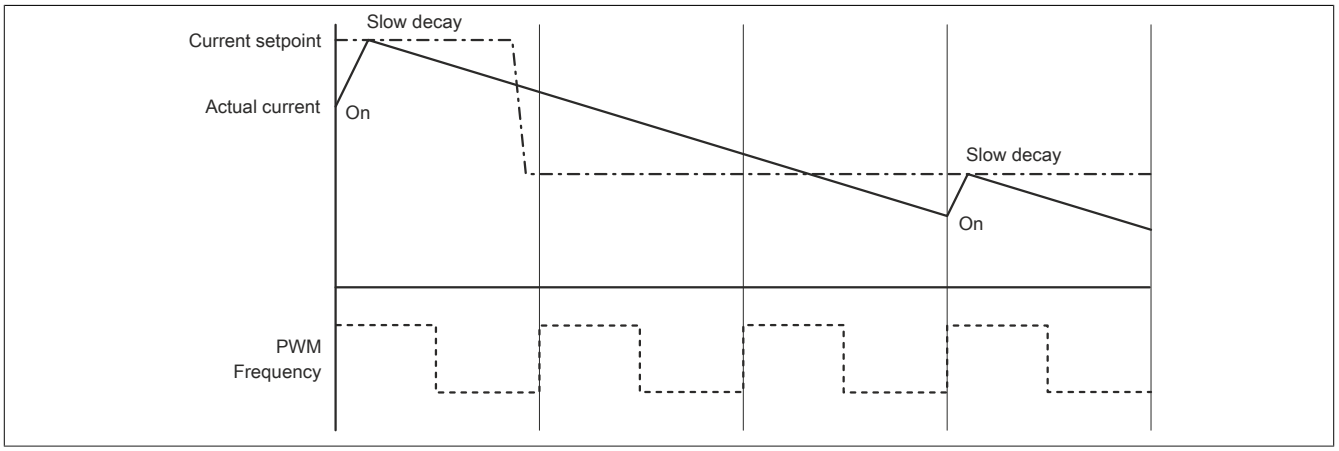
A check is made at the beginning of each PWM cycle to determine if the actual current for the phases is below the set current. If this is the case, PWM is enabled (On) until the current setpoint is reached. If the current setpoint has already been exceeded at the beginning of the PWM cycle (generator operation), the system immediately switches to fast decay mode until the current setpoint is exceeded. The rest of the PWM cycle always takes place in slow decay mode.

This also permits generator operation as long as the valid range for the supply voltage has not been exceeded due to the regeneration into the DC circuit.

Current control in Mixed Decay mode



Current control in Slow Decay mode

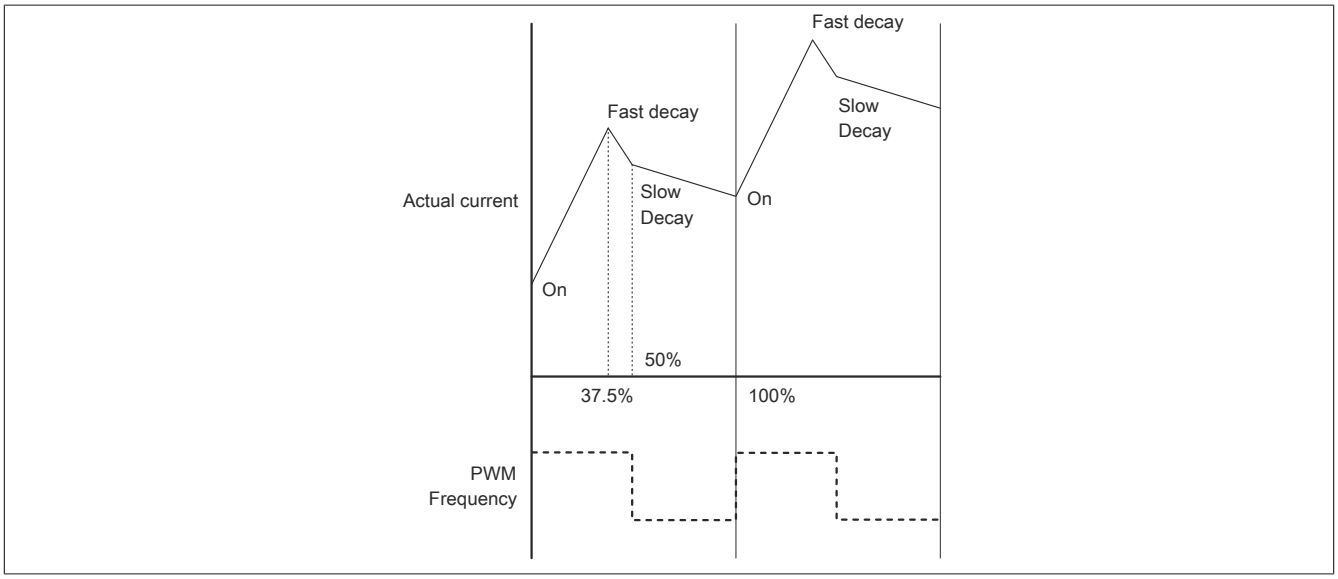


4.25.5.15.6.2 PWM control

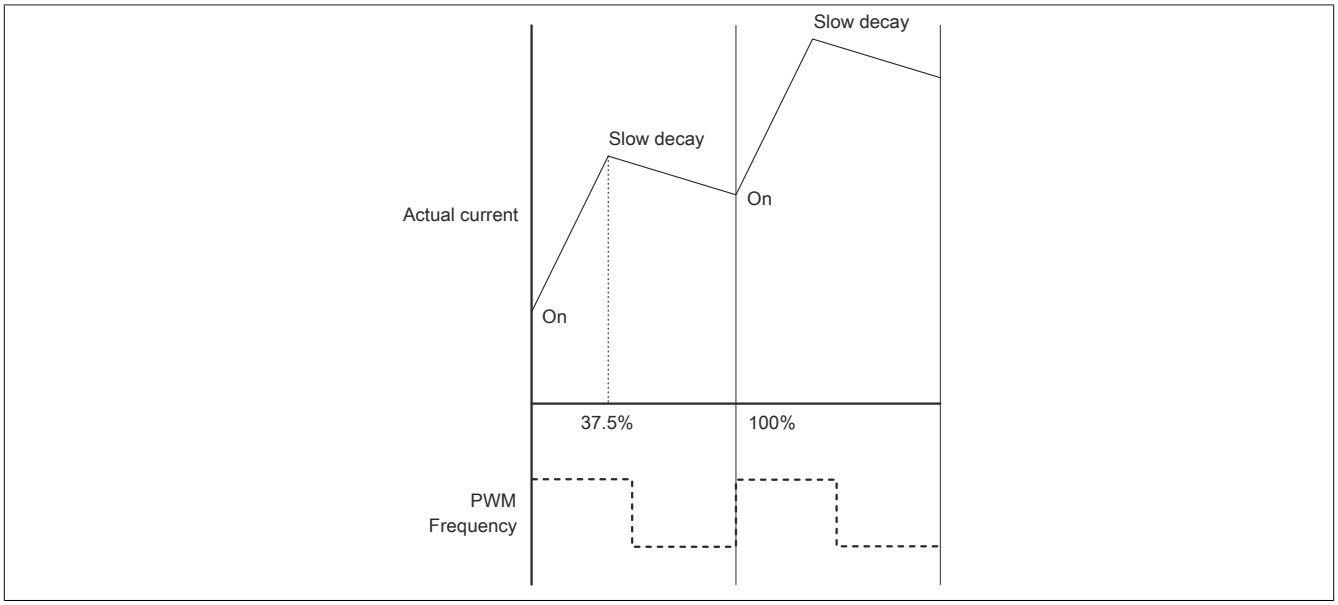
When Mixed Decay mode is enabled, the outputs are driven in Fast Decay mode up until 50% of the period and in Slow Decay mode for the remainder of the switch-off phase.

When Slow Decay mode is used, it is immediately enabled during the switch-off phase.

PWM control in Mixed Decay mode (pulse duty factor = 37.5%)



PWM control in Slow Decay mode (pulse duty factor = 37.5%)



Operating DC motors

In PWM mode, the motor current is limited to the maximum current (10 A), independent of the supply voltage.

However, the motor switches to generator operation when braking. Because of the counter EMF, which is dependent on the rotary speed, a current is generated in the module that is only limited by the internal resistance of the motor. This is not permitted to exceed 15 A (maximum 2 seconds).

The counter EMF closely corresponds to the voltage needed to achieve this speed. Therefore, the maximum brake current is very easy to calculate with the following formula.

$$I_{Brake} = U_e.Pulse\ width(in\ \%)/100.\frac{1}{R_{Motor}}$$

Example:

Module supply	42 V
Pulse width	16364 (equal to 50%)
Internal resistance of motor	3.5 Ω

$$I_{Brake} = 42V.50/100.\frac{1}{3.5\Omega} = 6A$$

4.25.5.15.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
400 µs

4.25.5.15.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
400 µs

4.25.6 X20SM1426

4.25.6.1 General information

The stepper motor module is used to control stepper motors with a rated voltage of 24 VDC at a motor current up to 1 A (1.2 A peak). Additionally, this module has four digital inputs that can be used as limit switches or as encoder inputs.

By individually adjusting the coil currents, the motor is only operated with the current it actually needs. This simplifies the selection of the available motors and prevents unnecessary heating. Because the latter reduces energy consumption and thermal load, the effects are positive on the lifespan of the complete system. Complete flexibility is achieved by using the values for holding current, maximum current and rated current, which are completely independent of each other. The current for the microsteps is automatically adjusted to the configured current values.

The automatic motor identification system is an enormous help during standstills. The stepper motor modules can identify the connected motors using their coil characteristics and generate feedback in the form of an analog value. This makes it possible to detect not only wiring errors, but also incorrect motor types being used mistakenly. A stall detection mechanism is integrated to analyze the motor load. The stall is recognized using a configurable threshold. This allows an overload or motor standstill to be detected precisely in many different types of applications.

- 1 stepper motor, 24 VDC, 1 A (1.2 A peak)
- Resolution of current values at 1%
- Maximum, rated and holding current configured independent of each other
- 38.5 kHz PWM frequency
- Integrated motor detection
- 256 micro-steps
- Stall detection
- Complete integration in Automation Studio and CNC applications
- 4 inputs, 24 VDC, can be configured as ABR
- Ramp function model based on the CANopen communication profile DS402

4.25.6.2 Order data

Model number	Short description	Figure
	Motor controllers	
X20SM1426	X20 stepper motor module, 1 motor connection, 1 A continuous current, 1.2 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 568: X20SM1426 - Order data

4.25.6.3 Technical data

Product ID	X20SM1426
Short description	
I/O module	1 full bridge for controlling stepper motors
General information	
B&R ID code	0x2681
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Output	Yes, using status LED and software
I/O supply	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.8 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - I/O supply	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Motor bridge - Power unit	
Quantity	1
Type	2-phase bipolar stepper motor (full bridge)
Nominal voltage	24 VDC
Nominal current	1 A
Maximum current	1,2 A for 2 s (after a recovery time of at least 10 s at maximal 1 A)
Controller frequency	38.4 kHz
DC bus capacitance	57 µF
Step resolution	Max. 256 microsteps per step
Digital inputs	
Quantity	4
Nominal voltage	24 VDC
Input filter	
Hardware	<5 µs
Software	-
Connection type	1-wire connections
Input circuit	Sink
Additional functions	1x ABR incremental encoder
Input resistance	Typ. 18.2 kΩ
ABR incremental encoder	
Quantity	1
Encoder inputs	24 V, asymmetrical
Counter size	16-bit
Input frequency	Max. 50 kHz
Evaluation	4x
Operating conditions	
Mounting orientation	
Horizontal	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 50°C
Vertical installation	Not allowed
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C

Table 569: X20SM1426 - Technical data

Product ID	X20SM1426
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 569: X20SM1426 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.25.6.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset state
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green		Input state of the corresponding digital input
	M	Orange	On	Motor is active

1) Depending on the configuration, a firmware update can take up to several minutes.

4.25.6.5 Pinout

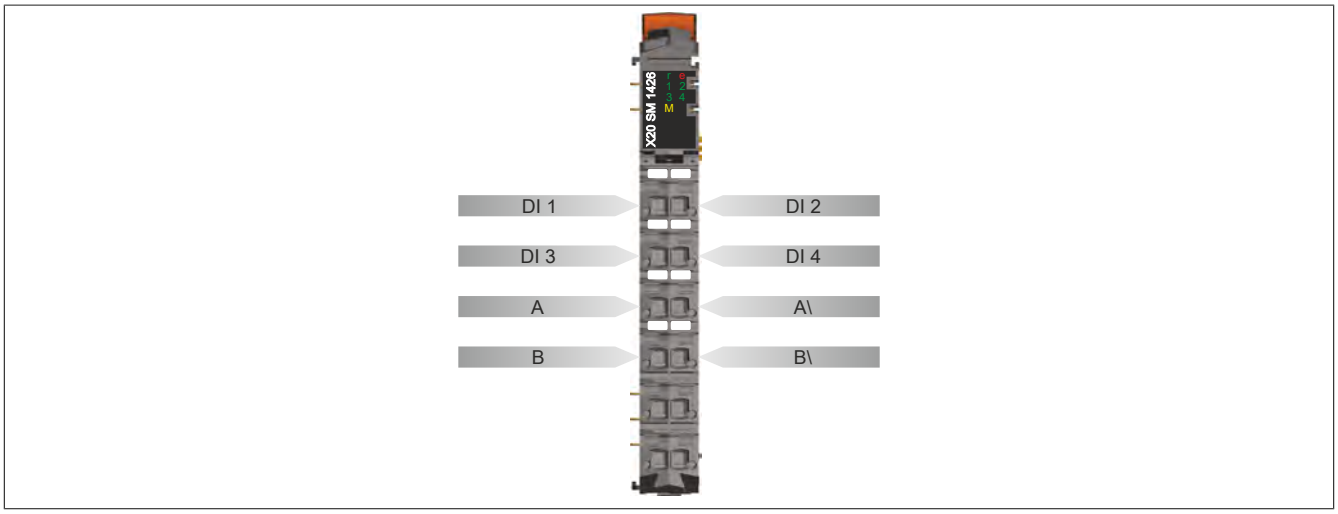
In accordance with the EN60204-1 standard, a cable cross section of 0.75 mm² or larger must be used for the motor outputs in order to handle the maximum motor current of 1.2 A. To ensure full motor power, voltage drops that could result from the cable length and the electrical connections must also be taken into consideration when selecting the attachment cable.

Warning!

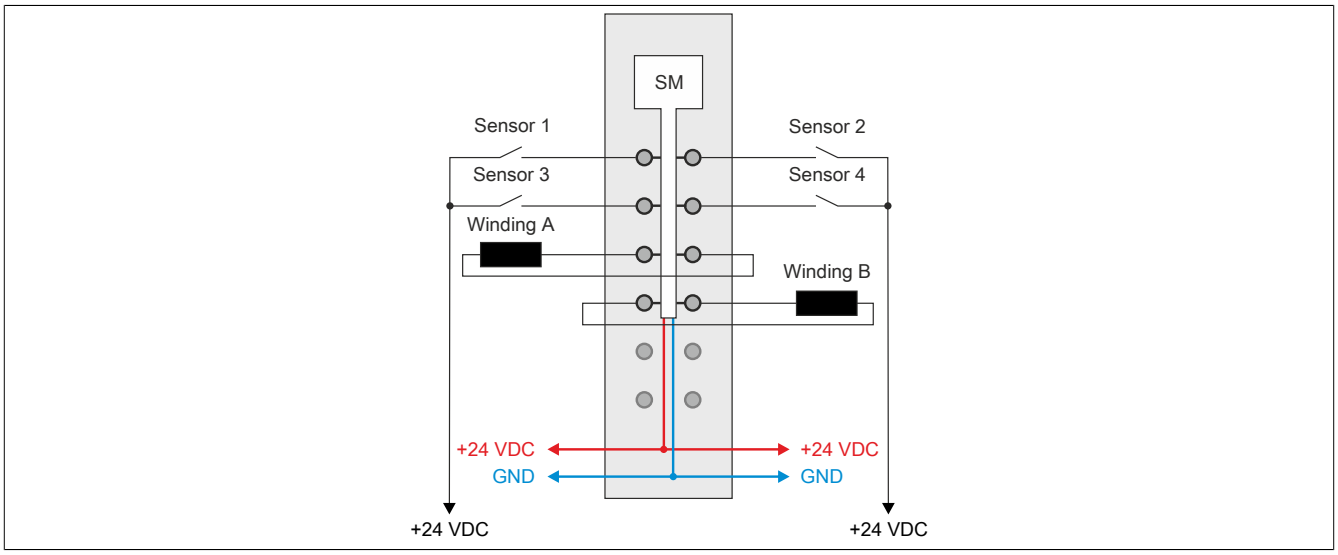
The terminal block is not permitted to be plugged in or unplugged during operation.

Information:

Shielded motor cables must be used in order to meet the limits according to the EN55011 standard (emissions).



4.25.6.6 Connection example



4.25.6.7 Connection options for digital inputs

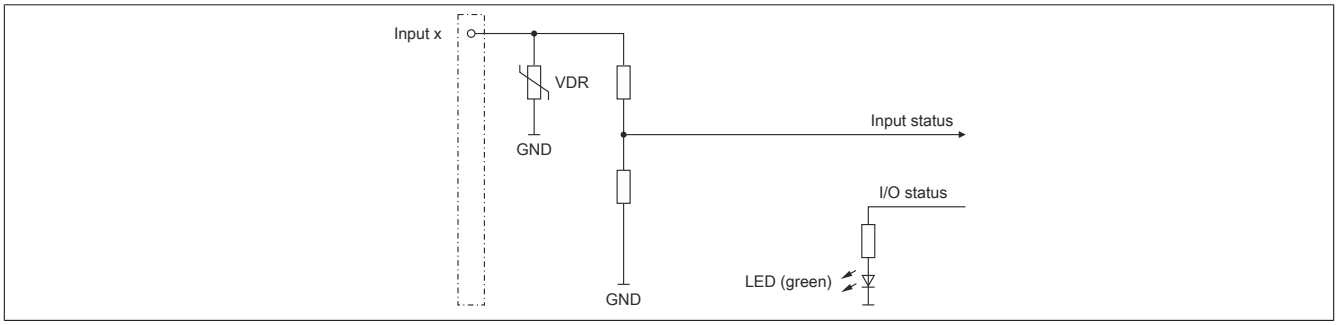
Standard function model

Channel	Function	
DI 1	Digital input	A
DI 2	Digital input	B
DI 3	Digital input	R
DI 4	Digital input	Trigger input

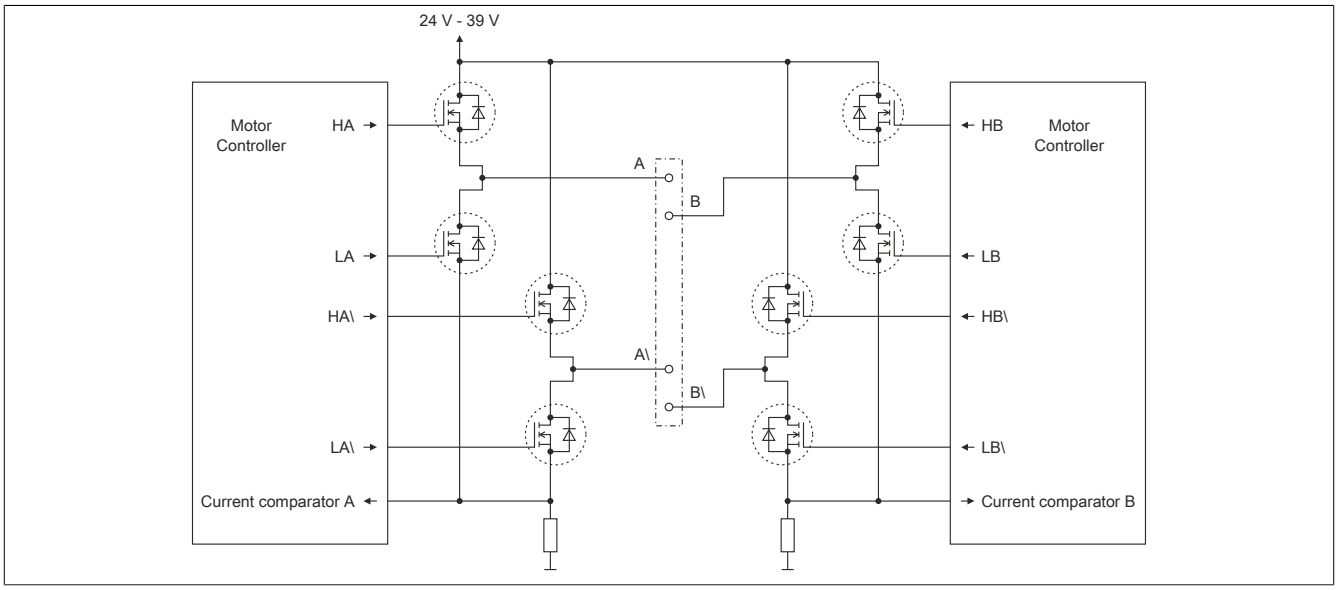
Ramp function model

Channel	Function		
DI 1	Digital input	A	A
DI 2	Digital input	B	B
DI 3	Digital input	R	Negative limit switch
DI 4	Digital input	Digital input	Positive limit switch

4.25.6.8 Input circuit diagram



4.25.6.9 Output circuit diagram



4.25.6.10 Overvoltage cutoff

The module supply voltage is continually monitored. Its status can be read. The error "Module power supply error" occurs when the voltage is above or below the limits.

If the supply voltage on the module rises or falls outside the limit values (e.g. due to regeneration), then the motor output is switched off. The outputs are reactivated as soon as the supply voltage is back in the valid range and the error bit is reset.

Supply voltage limit values

	Drive is switched off	Drive is switched back on
Lower limit	<17.5 V	>19.5 V
Upper limit	>30 V	<29.0 V

4.25.6.11 Overtemperature cutoff (at 85°C)

If the module temperature reaches or exceeds the limit value of 85°C, then the module executes the following actions:

- Setting the "overtemperature" error bit
- The outputs are switched off (short-circuited)

As soon as the temperature sinks back down below 85°C, the error must be acknowledged with OvertemperatureAcknowledge so that the channels can be switched on again.

4.25.6.12 Derating

Modules next to the SM module can have a maximum power consumption of 1 W. To ensure proper operation, the derating values listed below must be adhered to:

Power loss derating for neighboring modules

Modules directly next to the SM module can have a power loss of 1 W. If the SM module is operated at the rated load over the entire temperature range (1 A rated current), the power loss of neighboring modules must be derated starting at 45°C.

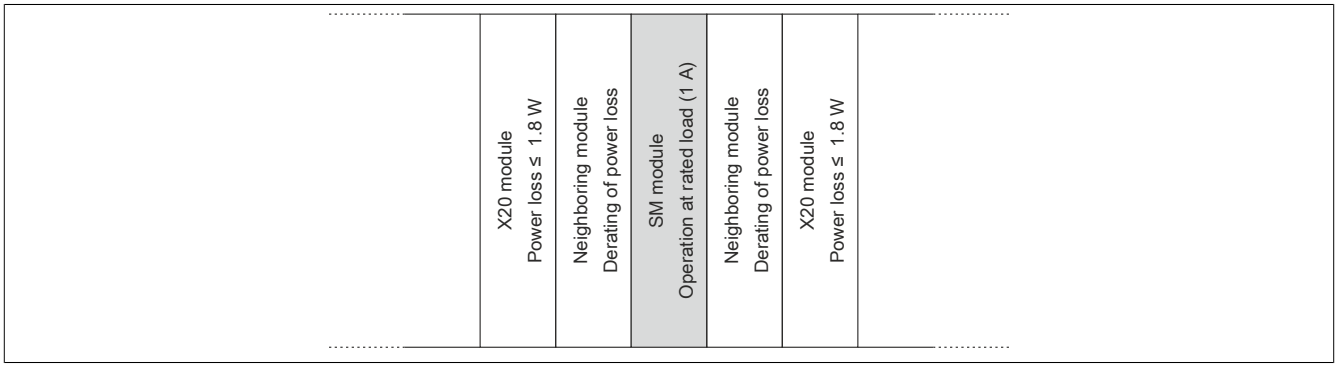


Figure 380: Operating the SM module over the entire temperature range at 1 A rated current

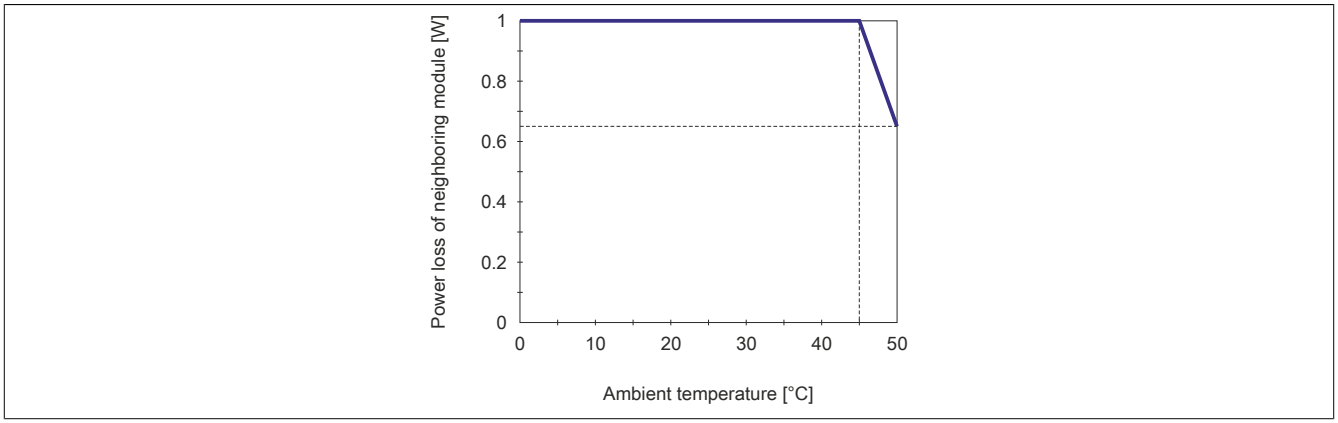


Figure 381: Power loss derating for directly neighboring modules

Current derating of the SM module

If the power loss of the neighboring modules to the SM module is 1 W, then the current of the SM module must be derated starting at 45°C.

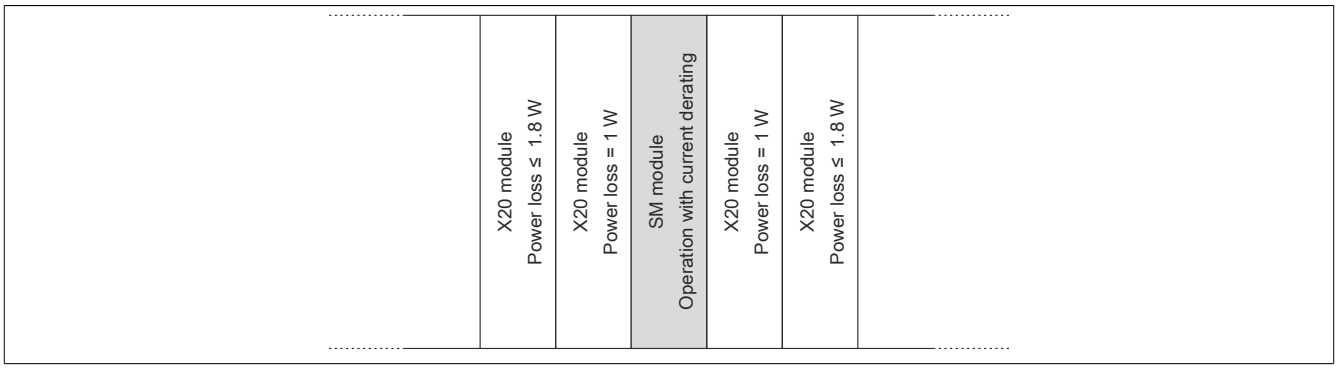


Figure 382: Neighboring modules to the SM module have a power loss of 1 W

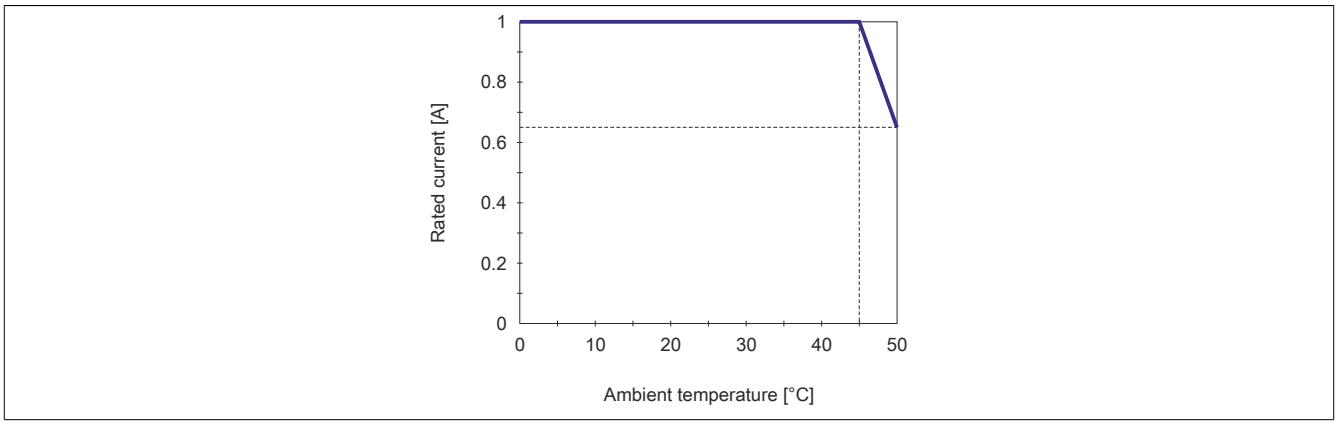


Figure 383: Current derating

Current derating for multiple SM modules

If three or more SM modules are operated in a cluster, the current of the SM modules must be derated as follows starting at 40°C.

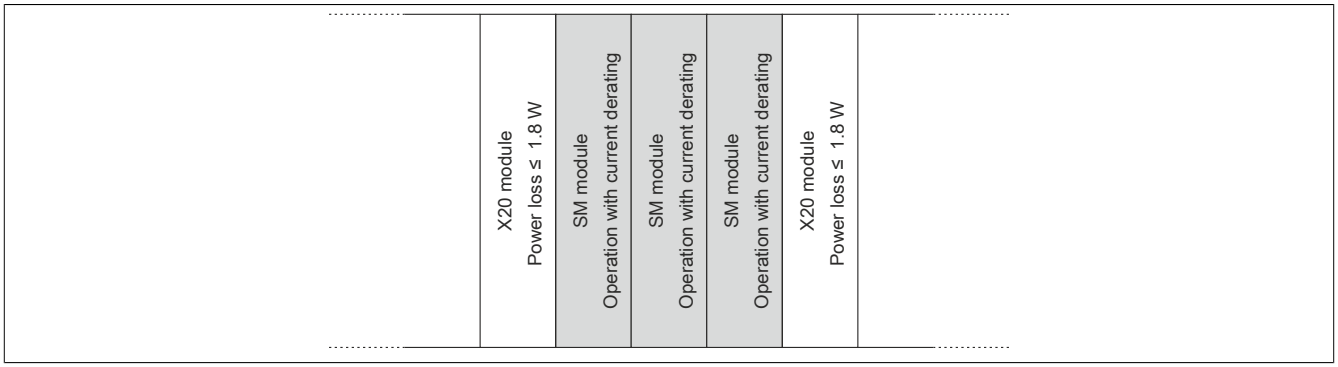


Figure 384: Operating three or more SM modules in a cluster

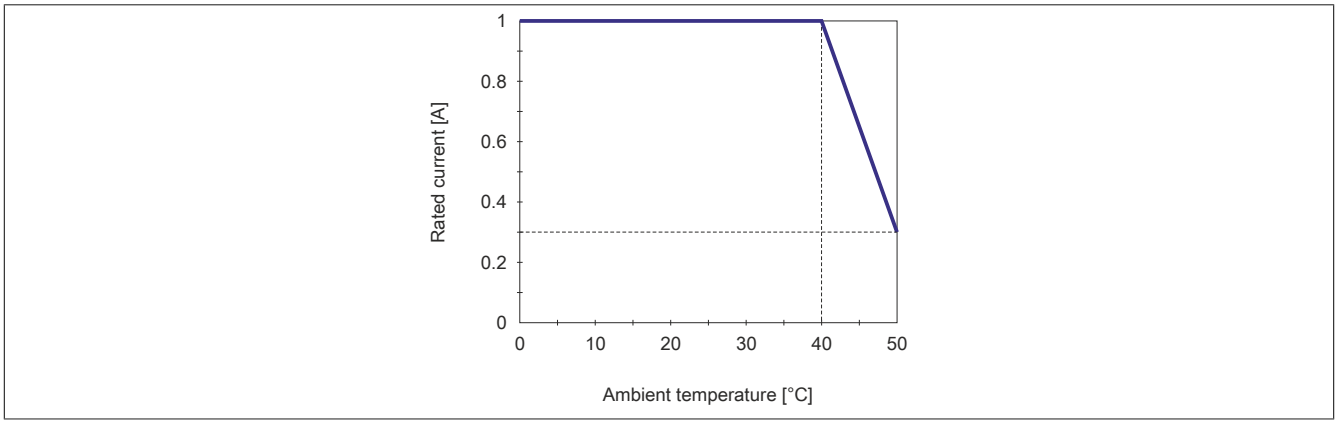


Figure 385: Current derating

4.25.6.13 Register description

4.25.6.13.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.25.6.13.2 Function model 0 - Standard without SDC

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
44	Stall threshold	UINT				•
46	Module configuration 1	UINT				•
33	Holding current	USINT				•
34	Nominal current	USINT				•
35	Maximum current	USINT				•
32	Counter configuration	USINT				•
52	Mixed decay threshold	UINT				•
81	Motor ID trigger	USINT				•
84	Full step threshold	UINT				•
92	Minimum speed for stall detection	UINT				•
Reads the configuration						
33	Holding current	USINT		•		
34	Nominal current	USINT		•		
35	Maximum current	USINT		•		
Communication						
6	Position sync/async	UINT		•		
64	Position latched sync/async	INT		•		
12	Motor ID	UINT		•		
Index* 2 + 16	MotorStepN (Index N = 0 to 3)	UINT			•	
0	Position sync/async	INT	•			
86	Position sync 2	INT	•			
4	Input counter state	USINT	•			
	ModulePowerSupplyError	Bit 0				
	StatusInput01	Bit 2				
	StatusInput02	Bit 3				
	StatusInput03	Bit 4				
	StatusInput04	Bit 5				
10	Error status	USINT	•			
	StallError	Bit 0				
	OvertemperatureError	Bit 1				
	CurrentError	Bit 2				
	OvercurrentError	Bit 3				
60	Position latched sync/async	INT	•			
68	usSinceTrigger	UINT	•			
54	Module configuration 2	USINT			•	
	StartLatch	Bit 0				
	TriggerEdgePos	Bit 1				
	TriggerEdgeNeg	Bit 2				
	TriggerEdge	Bit 3				
	StartTrigger	Bit 4				
	ClearError	Bit 5				
72	Stepper latch trigger status	USINT	•			
	LatchInput	Bit 0				
	LatchDone	Bit 1				
	TriggerInput	Bit 4				
74	Measuring motor load	USINT	•			

4.25.6.13.3 Function model 0 - Standard with SDC

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
44	Stall threshold	UINT				●
-	Module configuration 1	UINT				●
33	Holding current	USINT				●
34	Nominal current	USINT				●
35	Maximum current	USINT				●
32	Counter configuration	USINT				●
52	Mixed decay threshold	UINT				●
81	Motor ID trigger	USINT				●
84	Full step threshold	UINT				●
92	Minimum speed for stall detection	UINT				●
102	SDC configuration	USINT				●
103	Motor settling time	USINT				●
107	Turn-off delay	USINT				●
Reads the configuration						
33	Holding current	USINT		●		
34	Nominal current	USINT		●		
35	Maximum current	USINT		●		
Communication						
6	Position sync/async	UINT		●		
12	Motor ID	UINT		●		
112	SDC life sign monitoring	INT			●	
100	Motor current	USINT			●	
	DriveEnable01	Bit 0				
	BoostCurrent01	Bit 1				
	StandstillCurrent01	Bit 2				
74	Measuring motor load	USINT	●			
73	Life cycle counter	SINT	●			
0	Position sync/async	INT	●			
4	Input counter value	USINT	●			
	ModulePowerSupplyError	Bit 0				
	StatusInput01	Bit 2				
	StatusInput02	Bit 3				
	StatusInput03	Bit 4				
	StatusInput04	Bit 5				
10	Error status	USINT	●			
	StallError01	Bit 0				
	OvertemperatureError01	Bit 1				
	CurrentError01	Bit 2				
	OvercurrentError01	Bit 3				
	DrvOk01	Bit 4				
54	Error acknowledgment	USINT		●		
	ClearError01	Bit 5				
16	Motor1Step0	INT		●		
200 204	Home position Home position	INT	●			
212 214	Reference pulse counter Reference pulse counter	SNT	●			
220	Net time of the position value	INT	●			
208	Trigger timestamp	INT	●			
216	Trigger counter	SINT	●			

4.25.6.13.4 Function model 254 - Bus controller and function model 3 - Ramp

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration							
48	-	Holding current	USINT				●
49	-	Nominal current	USINT				●
50	-	Maximum current	USINT				●
72	-	Full step threshold	UINT				●
52	-	Maximum speed	UINT				●
54	-	Maximum acceleration	UINT				●
56	-	Maximum deceleration	UINT				●
58	-	Reversing loop	INT				●
60	-	Fixed position A	DINT				●
64	-	Fixed position B	DINT				●
68	-	Homing speed	UINT				●
74	-	Stall recognition delay	USINT				●
75	-	Jolt time	USINT				●
78	-	Minimum speed for stall detection	UINT				●
70	-	Homing configuration	SINT				●
51	-	Stall detection configuration / Mixed decay	USINT				●
306	-	General configuration	USINT				●
308	-	Limit switch configuration	USINT				●
344	-	Software limit	DINT				●
348	-	Software limit	DINT				●
Reads the configuration							
48	-	Holding current	USINT		●		
49	-	Nominal current	USINT		●		
50	-	Maximum current	USINT		●		
Communication							
0	0	Set position/speed	DINT			●	
4	4	Control word	UINT			●	
6	6	Mode	SINT			●	
0	0	Current position (cyclic)	DINT	●			
4	4	Status word	UINT	●			
6	6	Input status	USINT	●			
84	-	Motor ID	UINT		●		
86	-	Homed zero position	DINT		●		
94	-	Homed zero position	DINT		●		
90	-	Current position (acyclic)	DINT		●		
80	-	Reads the extended control word	UINT		●		
82	-	Read back mode	SINT		●		
98	-	Error code	UINT		●		

1) The offset specifies the position of the register within the CAN object.

4.25.6.13.4.1 Operation with bus controller

The following function model can be used when the SM module is used together with a bus controller.

Bus controller	Function model
X20BC0083, X20BC1083, X20BC8083, X20BC8084	All function models
All others	Function model 254 - Bus controller (identical to Ramp function model)

4.25.6.13.4.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.25.6.13.5 Register description: Standard functional model, shared registers

4.25.6.13.5.1 Configuration registers

Stall threshold

Name:
ConfigOutput01

The SM module features integrated sensorless load measurement for the motor axis. This is especially useful for detecting a "stall condition" (e.g. if the motor moves to the end point during a homing procedure). It cannot be used for torque monitoring during dynamic movements.

With the "stall threshold" register, a threshold can be defined according to the motor load, and the module detects a stall condition started at this threshold (see "Error status").

This threshold value must be determined on a case-by-case basis, since the results of load measurement are influenced by a variety of factors.

- Motor speed: A higher speed results in higher measurement values
- Speeds that cause motor resonances (which interfere with load measurement) are to be avoided
- Motor accelerations that create a dynamic load (and also affect the measurement) should also be avoided
- It is especially important to be aware that mixed decay mode must be optimized for reliable stall detection (see "Mixed decay threshold")

The higher the load measurement value, the lower the load. This means that a stall condition is detected if the load measurement value drops below the trigger threshold for stall detection.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Trigger threshold for stall detection	0	Stall detection is disabled
		1	Minimum sensitivity for stall detection
		2 to 6	Setting the sensitivity of stall detection
		7	Maximum sensitivity for stall detection
3 - 15	Reserved	0	

Mixed decay threshold

Name:
ConfigOutput16

The mixed decay threshold is configured in this register. This value must be adjusted according to the motor being used, current and voltage when using stall detection. Otherwise, the default value 15 will be used.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Mixed Decay Threshold	0	Mixed decay disabled
		1 to 14	Setting for mixed decay threshold
		15	Mixed decay always enabled
4 - 15	Reserved	-	

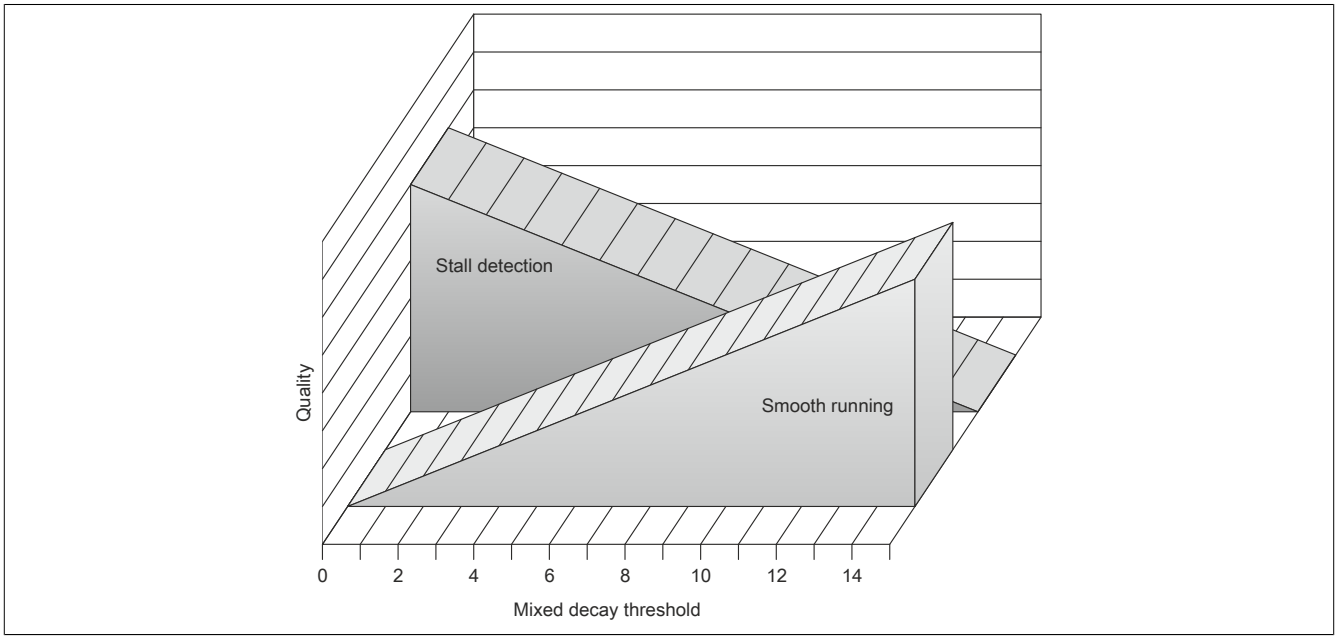
Mixed decay modules provide a greatly optimized sinusoidal current profile in the individual phases of the stepper motor, especially for fast current changes and low current values.

Mixed decay interferes with reliable stall detection, however. For this reason, mixed decay mode can be disabled during stall detection (motor load measurement) using the mixed decay threshold. The smaller the configured mixed decay threshold, the larger the range in which mixed decay is disabled while motor load measurement takes place.

Mixed decay mode is always enabled if the mixed decay threshold is set to 15.

Relationship between stall detection and mixed decay

Depending on the application and the motor used, satisfactorily smooth operation can be achieved while using stall detection by setting the mixed decay threshold to a value between 1 and 14. This is a compromise between smooth operation and stall detection quality and must be fine tuned during commissioning.



Minimum speed for stall detection

Name:
StallDetectMinSpeed01

If the motor speed exceeds the value set in this register, then stall detection is enabled and the configured mixed decay threshold is used. The value 15 is always used for the mixed decay threshold below this threshold value, and no stall error is reported. This means that mixed decay mode is always enabled at low speeds where stall detection principally does not work.

Data type	Value	Information
UINT	0 to 65535	Minimum speed in steps per second.

Full step threshold

Name:
FullStepThreshold01

This register is used to configure a rotational speed. When this defined speed has been reached, the drive will automatically change from microsteps to full step mode. This makes it possible to optimize the torque at higher speeds, while microstep mode ensures optimum concentricity at lower speeds.

It does not make sense to change to full step mode when at a standstill because fine positioning would then no longer be possible. This is why the value "0" does not make sense in the full step threshold register and is interpreted as disabling full step mode (i.e. the motor will always be operated in microstep mode).

Data type	Value	Information
UINT	0	Full step mode disabled
	1 to 65,535	steps/second

Example

Microstep mode should change to full step mode at 500 steps/second. On a motor with 200 steps per revolution, this would be equal to a speed of:

$$T^{-1} = \frac{500\ steps/second}{200\ steps/round} = 2.5\ \frac{rounds}{second} = 150\ \mathrm{min}^{-1}$$

Holding current, rated current and maximum current

Name:
ConfigOutput03 (holding current)
ConfigOutput04 (rated current)
ConfigOutput05 (maximum current)

The holding current, nominal current and maximum current registers are used to configure the desired motor current.

Reasonable values are:

- Holding current < Nominal current < Maximum current

The motor's nominal current is entered in the nominal current register according to the motor's data sheet.

Register	Description
Nominal current	Current during normal operation
Maximum current	Should be selected if a higher motor torque is required briefly during acceleration phases.
Holding current	The holding current should be used in situations when less torque is required (e.g. at a standstill). This reduces the amount of heat generated by the motor.

Switching between preset current values (holding current, rated current, maximum current):

Function model	Switching between preset current values at runtime
Default	Using bits 14 and 15 in the registers Motor StepX
Standard with enabled SDC information	Using the register Motor current

Data type	Value	Unit
USINT	0 to 117	Percent of the module's rated current • 100% corresponds to the rated current of the motor bridge power unit listed in the technical data • 117% corresponds to the maximum current of the motor bridge power unit listed in the technical data

Counter configuration

Name:
ConfigOutput09

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ABR latch function	0	Negative edge: Disable ABR latch function.
		1	Positive edge: Enable latch ABR latch function. After a latch event has occurred, the latch function can be started again with a new rising edge.
1 - 2	Definition of the latch mode	00	Latch ABR counter state unconditionally
		01	Latch ABR counter state at a positive edge on the R input
		10	Latch ABR counter state at a negative edge on the R input
		11	Reserved
3		0	• Position sync: Internal position counter • Position async: ABR counter state • Position latched sync: Internal position counter • Position latched async: ABR counter state
		1	• Position sync: ABR counter state • Position async: Internal position counter • Position latched sync: ABR counter state • Position latched async: Internal position counter
4 - 7	Reserved		

1) These registers are not available in the standard function model with SDC information enabled.

Motor ID trigger

Name:
MotorIdentTrigger

This register can be used to trigger acyclic motor identification (see "Motor ID"). The application must ensure that the conditions for reading the motor ID are fulfilled (see "Notes" under).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0		0	No effect
		1	Rising edge triggers motor identifier measurement
1 - 7	Reserved	0	

4.25.6.13.5.2 Register for reading back the configuration

Read ing the holding current, rated current and maximum current

ConfigOutput03Read (holding current)
ConfigOutput04Read (rated current)
ConfigOutput05Read (maximum current)

These registers are used to read the respective current values in percent.

Register	Description
Nominal current	Current during operation at constant speed
Maximum current	Current during acceleration phases
Holding current	Current when motor is at standstill

Data type	Value	Unit
USINT	0 to 255	Percent of the module's rated current (100% corresponds to the rated current of the motor bridge power unit listed in the technical data)

4.25.6.13.5.3 Communication registers

Measuring motor load

Name:
MotorLoad

This register contains the current measured load value for stall detection. This can be used to tune stall detection.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Motor	0 to 7	Motor load value
3 - 8	Reserved	-	

Module configuration 1

Name:
ConfigOutput02

The number of transfer values and the resolution of microsteps for the drive can be configured in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	The setting for these two bits determines the meaning of bits 2 and 3 in the "Input counter state" register.	x	
1 - 2	Reserved	0	
3 - 4	Number of transfer values per X2X cycle (See "Motor StepX".)	00	1 x Δs / Δt (transfer values: MotorStep0)
		01	2 x Δs / Δt (transfer values: MotorStep0 - MotorStep1
		10	4 x Δs / Δt (transfer values: MotorStep0 - MotorStep3
		11	Reserved
5 - 6	Resolution of microsteps for the following registers: • "Motor StepX" • "Position sync/async"	00	Resolution: 5 bits (bit 0 - 4) microsteps; 8 bits (bit 5 - 13) full steps
		01	Resolution: 6 bits (bit 0 - 5) microsteps; 7 bits (bit 6 - 13) full steps
		10	Resolution: 7 bits (bit 0 - 6) microsteps; 6 bits (bit 7 - 13) full steps
		11	Resolution: 8 bits (bit 0 - 7) microsteps; 5 bits (bit 8 - 13) full steps
7 - 15	Reserved	0	

Position sync/async

Name:
PositionSync
Positionasync

Depending on the Counter configuration, these registers can be used to read either the internal position counter or the counter state of the ABR input.

Data type	Value
INT	-32768 to 32767

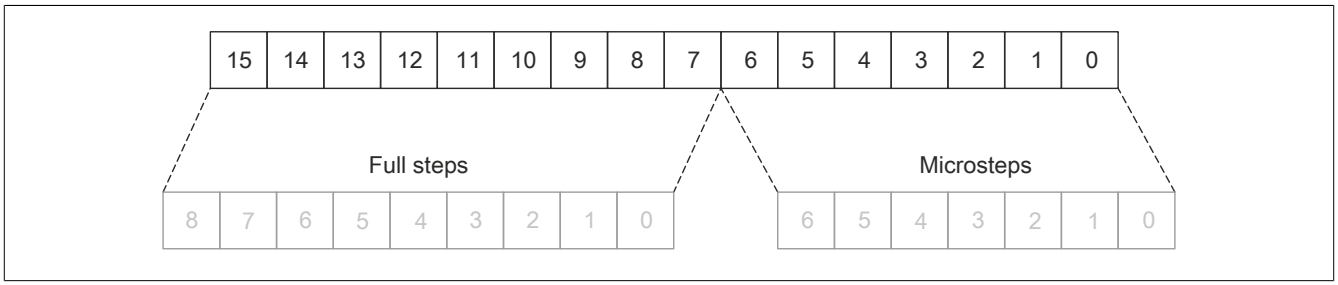
Register	Counter configuration	
	Bit 3 … 0	Bit 3 … 1
Position sync	Internal position counter	ABR counter
Position async	ABR counter	Internal position counter

Internal position counter

The internal position counter is the position calculated by the SM module (set position). This is a cyclic 16-bit counter.

The lowest 5 to 8 bits represent microsteps, while the highest 8 to 11 bits represent full steps (depending on bits 5 and 6 of the register Module configuration 1). In the standard function model with SDC, this value is set to "8-bit microsteps" and can not be changed.

Example of the internal position counter format (7-bit micro steps, i.e. set bit 5 and 6 of the module configuration to binary 10):



ABR counter

This counter is a cyclic 16-bit counter. The relationship between this counter and the internal position counter depends on the resolution of the ABR encoder and the microsteps defined for the internal position counter.

Motor ID

Name:
Motoridentification01

This register is used to identify the connected motor type for service purposes and to differentiate between motors in the application. Following measurement, this register contains the time [µs] needed to apply a current increase of ΔI = 1 A to a motor winding.

This depends on:

- Operating voltage
- The inductance and resistance of the motor winding

Notes		
1)	To achieve reproducible results, the measurement must be made under the following defined conditions:	
	a)	Motor is at standstill
	b)	The motor must be in a half-step position (phase A fully powered, phase B not powered). This means the internal position counter on the SM module must have a value that fulfills the following conditions: • Full steps are divisible by 4 • Microsteps = 0
2)	Condition 1b) is fulfilled after a the SM module is reset or powered on. Immediately afterwards, when the holding current is applied to the motor for the first time (at standstill), the duration for applying the current is measured. This is therefore a suitable time to read the motor identification register in the application.	
3)	The current range from approximately 1/3 of the rated current up to the rated current is used as operating range for determining the motor identifier.	

Data type	Motor ID values	Function
UINT	0	No motor identifier available (after turning on for as long as the measurement conditions are not met)
	1 to 32767	Valid range of values for the motor ID register (in µs)
	65504 to 65519	Ground fault: Motor identification not possible
	65528	Motor ID trigger not possible • Motor has no power applied • Motor in movement • Rated current is set to 0A • Ground fault present
	65529	Invalid value: Underflow
	65530	Overtemperature: Measurement not possible
	65532	Open line: Measurement not possible
	65533	Motor position incorrect: Measurement not possible
	65534	Invalid value: Overrun
	65535	Measurement in progress

Ground fault detection

When the motor is powered on, a ground fault check is performed before motor identification. Error numbers have been added in the motor identification register for the event of a ground fault error (values 65504 to 65519 in the table above).

Error status

Name: The names of the bits are different depending on whether SDC information is enabled or disabled.

Without SDC	With SDC
StallError	StallError01
Overtemperature	Overtemperature01
ErrorCurrentError	ErrorCurrentError01
OvercurrentError	OvercurrentError01
-	DrvOK01

The current error status of the drive is indicated in this register. Each bit indicates a certain error or status. If an error is registered in bits 0 to 3, then the corresponding bit remains set until the error has been acknowledged (see "Module configuration 2" and "Error acknowledgment").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StallError(01)	0	No stall
		1	Stall
1	Overtemperature error OvertemperatureError(01)	0	No overtemperature
		1	Overtemperature
2	Current error CurrentError(01)	0	No current error
		1	Current error
3	Overcurrent error OvercurrentError(01)	0	No overcurrent
		1	Overcurrent
4	Status of the drive DrvOk0[1)]	0	An error was triggered for the motor axis
		1	The drive is running error-free
5 - 15	Reserved	0	

1) Only when SDC information is enabled

Overtemperature error

The "Overtemperature" error bit can be set for the following reasons:

- A specific temperature was exceeded near the channel due to overload
- Module temperature exceeds 85°C

Current error

This error bit occurs whenever the required current cannot be supplied to the motor windings. This can be (but is not necessarily) caused by an open line. At higher speeds (depending on the motor), this error can also occur without an open line. In this case it is simply no longer possible to supply the desired current to the motor windings. Because of the Back-EMF on the motor, this bit is set at slightly lower speeds if the motor is operated with no load compared with full or partial loads.

Overcurrent error

Overcurrent occurs if the motor current measured in the motor windings is twice as high as it should be (e.g. short circuit).

Status of the drive

The status of the drive is only shown when SDC information is enabled. The drive bit is 1 when the following conditions are met:

- Motor turned on (see "Motor current")
- Ground fault detection is completed and OK
- MotorID measurement is completed
- Motor is supplied with current
- Motor settling time has passed
- Supply voltage is in the valid range
- No overtemperature fault
- Preset position value is valid (see "SDC life sign monitoring")

4.25.6.13.6 Register description: Standard functional model without SDC information

4.25.6.13.6.1 Communication registers

Input counter state

Name:
ModulePowerSupplyError
StatusInput01 to StatusInput04

This register is used to indicate the status of the digital inputs and counters.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ModulePowerSupplyError	0	OK
		1	Module supply error
1	Reserved	0	
2	StatusInput01	**When bit 0 in Module configuration 1 = 0**	
		0 or 1	Input state - Digital input 1
		When bit 0 in Module configuration 1 = 1	
		x	Ref toggle bit for counter 1: The state of this bit is changed after the homing procedure is complete.
3	StatusInput02	**When bit 0 in Module configuration 1 = 0**	
		0 or 1	Input state - Digital input 2
		When bit 0 in Module configuration 1 = 1	
		0	Homing of ABR counter active
		1	Homing of ABR counter complete
4	StatusInput03	0 or 1	Input state - Digital input 3
5	StatusInput04	0 or 1	Input state - Digital input 4
6 - 7	Reserved	0	

Motor StepX

Name:
MotorStep0 to MotorStep3

These registers are used to specify the number and direction of steps that must be carried out by the module during the next X2X cycle, and to select the motor current (see also "Holding current, rated current and maximum current").

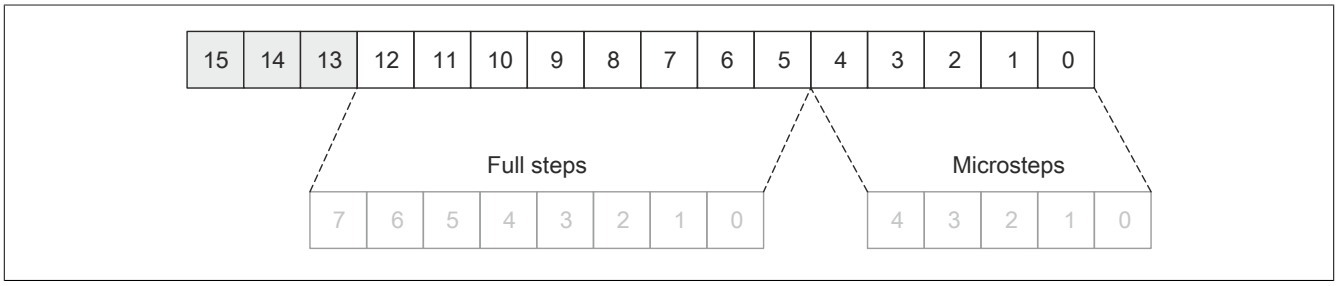
Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 12	Number of steps for the module to move during the next X2X cycle	x	
13	Direction of movement	0	Positive
		1	Negative
14 - 15	Selection of motor current	00	Motor not powered
		01	Holding current
		10	Rated current
		11	Maximum current

Depending on the required resolution and maximum configurable speed, "Module configuration 1" can be used to specify which bit position is used as the 1's position for full steps (see bits 5 and 6 of Module configuration 1).

Example for 5-bit microsteps (set bits 5 and 6 of the module configuration to binary 00):



The number of transfer values per X2X cycle is specified by bits 3 and 4 in "Module configuration 1" (see "Module configuration 1"). If only one transfer value (bits 3 and 4 = 00) is specified, then the motor is advanced by MotorStep0 until the next X2X cycle. If 2 or 4 transfer values are specified, then the X2X cycle is divided accordingly.

Example: X2X cycle = 1 ms (1000 µs)

Time	Number of transfer values (see Module configuration 1)		
	1 (bits 3 - 4 = 00)	2 (bits 3 - 4 = 01)	4 (bits 3 - 4 = 10)
0 - 250 µs)	MotorStep0	MotorStep0	MotorStep0
250 - 500 µs)			MotorStep1
500 - 750 µs)		MotorStep1	MotorStep2
750 - 1000 µs)			MotorStep3

Position latched sync/async

Name:
PositionLatchedSync
PositionLatchedASync

The position counter (internal position counter or ABR counter) is applied at the latch event (see "Module configuration 2"). Bits 3 and 7 of the Counter configuration register are used to determine which counter state (internal position counter or ABR encoder) should be saved in the registers "Position latched sync" and "Position latched async".

Data type	Value
INT	-32768 to 32767

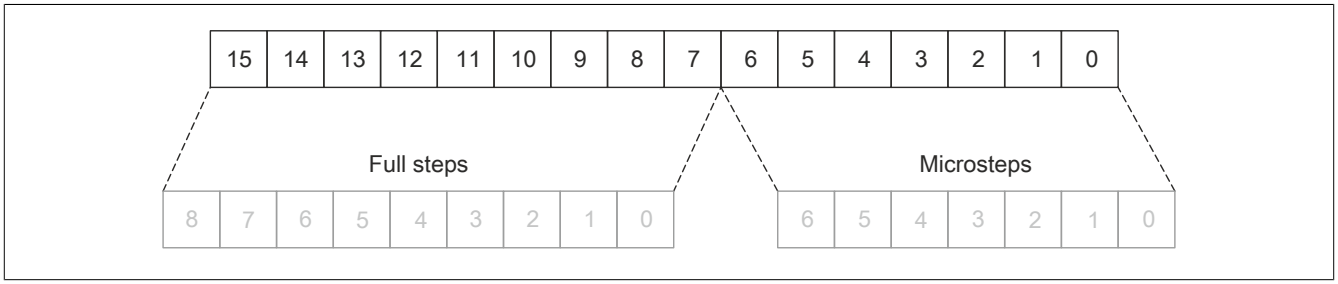
Register	Counter configuration	
	Bit 3 … 0	Bit 3 … 1
Position sync	Internal position counter	ABR counter
Position async	ABR counter	Internal position counter

Internal position counter

The internal position counter is the position calculated by the SM module (set position). This is a cyclic 16-bit counter.

The lowest 5 to 8 bits represent microsteps, while the highest 8 to 11 bits represent full steps (depending on bits 5 and 6 of the register Module configuration 1).

Example of the internal position counter format (7-bit micro steps, i.e. set bit 5 and 6 of the module configuration to binary 10):



ABR counter

This counter is a cyclic 16-bit counter. The relationship between this counter and the internal position counter depends on the resolution of the ABR encoder and the microsteps defined for the internal position counter.

usSinceTrigger

Name:
usSinceTrigger

This register indicates the time (in µs) that has passed since the trigger event occurred (see "Module configuration 2").

Data type	Value
UINT	0 to 65535

Stepper latch trigger status

Name:
LatchInput
LatchDone
TriggerInput

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Latch input:	x	Digital input for the latch event (level)
1	LatchDone	x	State changes each time the counter state is successfully latched (reset value = 0)
2 - 3	Reserved	-	
4	TriggerInput	x	Trigger input (level)
5 - 7	Reserved	0	

4.25.6.13.6.2 Configuration registers

Module configuration 2

Name:
StartLatch
TriggerEdgePos
TriggerEdgeNeg
StartTrigger
TriggerEdge
ClearError

The trigger functions for the stepper motor can be configured with this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Latch function for stepper motor Latch byte	0	The latch function for stepper motor position is deactivated at the negative edge of this bit
		1	The latch function for stepper motor position is deactivated at the positive edge of this bit
1 - 2	Latch mode for stepper motor TriggerEdgePos (Bit 1) TriggerEdgeNeg (Bit 2)	00	Latch position of stepper motor, unconditional
		01	Latch position of stepper motor at positive edge on input DI 3
		10	Latch position of stepper motor at negative edge on input DI 3
		11	Reserved
3	TriggerEdge	0	Trigger edge (input DI 4) = positive
		1	Trigger edge (input DI 4) = negative
4	Enable trigger (when changes occur) StartTrigger	x	
5	ClearError	0	No effect
		1	Error acknowledgment for the motor (for more info, see "Error status")
6 - 7	Reserved	-	

Trigger function procedure:

- Select the desired trigger edge using bit 3
- Enable the trigger function by changing the state of bit 4. When this bit changes, usSinceTrigger (µs counter) is cleared.
- When the trigger event occurs, usSinceTrigger (µs counter) is started.
- The usSinceTrigger counter cannot overrun, i.e. it is stopped at 2^{16} and retains this value until the next time the trigger function is activated.

The trigger function can be re-activated at any time by changing the state of bit 4, regardless of whether a trigger event has occurred or if usSinceTrigger has reached the maximum value.

Position sync 2

Name:
PositionSync02

Depending on Counter configuration (bit 3), this register contains the state of either the position counter or the ABR counter. It's an exact complement to the Position sync register.

If the position sync register contains the position counter, then the PositionSync02 register contains the ABR counter state and vice versa.

By default, the register cannot be seen in the I/O map; instead, it has to first be activated in the I/O configuration.

Data type	Value
INT	-32768 to 32767

4.25.6.13.7 Register description: Standard functional model with SDC information

4.25.6.13.7.1 Configuration registers

SDC configuration

Name:
SDCConfig01

This register can be used to enable/disable additional SDC information.

The additional cyclic registers are hidden or shown depending on whether SDC information is disabled or enabled. It is comparable to the two variants of the standard function model with and without SDC information.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Trigger edge	0	Rising trigger edge
		1	Falling trigger edge
1 - 5	Reserved	0	
6	SDC life sign monitoring	0	Disabled
		1	Enabled
7	SDC information[1)]	0	Disabled
		1	Enabled

1) When the "SDC information" bit is enabled, the "EncOK01" bit is shown in the Automation Studio I/O mapping. This bit is linked to the ModulOK bit and always indicates its value.

Note:

Neither SDC information nor SDC life sign monitoring is permitted to be changed at runtime.

Module configuration 1 with SDC

The Module configuration 1 register is ignored in the standard function model with SDC information enabled. The module behaves as if the module configuration were described as follows:

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Meaning of bits 2 and 3 in the register "Input counter value"		
1 - 2	Reserved	0	
3 - 4	Number of transfer values per X2X cycle	00	1x Δs / Δt (transfer values: Motor settings Motor1Step0)
5 - 6	Resolution of microsteps	11	8-bit microsteps
7 - 15	Reserved	0	

Motor settling time

Name:
MotorSettlingTime01

This register determines the motor setting time. The motor settling time determines the minimum time between when the motor is powered on to when the DrvOk bit is set (see "Error status"). The setting is made in steps of 10 ms.

Data type	Value	Information
USINT	1 to 255	10 ms to 2.55 s, default: 10 ms

Turn-off delay

Name:
DelayedCurrentSwitchOff01

When the SDC life sign monitoring is triggered (i.e. the net time timestamp is in the past) the motor is decelerated at nominal current with speed setpoint = 0.

Then the motor is switched off after the delay configured with this register.

Data type	Value	Information
USINT	0 to 255	0 to 25.5 ms in steps of 100 ms (default: 100 ms)

4.25.6.13.7.2 Communication registers

SDC life sign monitoring

Name:
SetTime01

The module uses SDC life sign monitoring to check whether valid values have been received for the speed setpoint. SDC life sign monitoring is activated in the SDC configuration register by setting bit 6 (SDCSetTime = on).

If the specified NetTime timestamp is in the past, then an error is triggered for the motor axis (only when the motor is switched on). The module performs the following steps:

1) The CPU is informed of the error using the Drive bit (DrvOk) = 0

2) Braking at configured rated current with speed setpoint = 0

3) Wait for configured turn-off delay to expire

4) Power off motor

When the timestamp is back in the valid range, the motor can be powered on again by a rising edge on the DriveEnable bit (see "Motor current").

Data type	Value
INT	-32768 to 32767

Motor current

Name:
DriveEnable01
BoostCurrent01
StandstillCurrent01

Bits 0 to 2 of this register can be used to control the motor's current supply.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DriveEnable01	x	Motor powered
1	BoostCurrent01	x	Maximum current
2	StandstillCurrent01	x	Holding current
3 - 7	Reserved	0	

The possible status of bits 0 to 2

StandstillCurrent01	BoostCurrent01	DriveEnable01	Description
x	x	0	Motor not supplied with current
0	0	1	Rated current supplied to motor
0	1	1	Maximum current supplied to motor
1	0	1	Holding current supplied to motor
1	1	1	Holding current supplied to motor

Life cycle counter

Name:
LifeCnt

This register is incremented by one with each X2X Link cycle.

Data type	Value
SINT	-128 to 127

Input counter value

Name:
ModulePowerSupplyError
StatusInput01 to StatusInput04

This register is used to indicate the status of the digital inputs and the counter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ModulePowerSupplyError	0	OK
		1	Module supply error
1	Reserved	0	
2	StatusInput01	0 or 1	Input state - Digital input 1
...		...	
5	StatusInput04	0 or 1	Input state - Digital input 4
6 - 7	Reserved	0	

Error acknowledgment

Name:
ClearError01

This register can be used to acknowledge errors that have occurred on the motor.

For more info, see "Error status".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 4	Reserved	0	
5	ClearError01	0	No effect
		1	Error acknowledgment for motor
6 - 7	Reserved	0	

Motor1Step0

Name:
Motor1Step0

This registers is used to specify the number and direction of steps that should be carried out by the module during the next X2X cycle.

The value is specified with a resolution of 1/256 of a full step (corresponds to 8-bit microsteps).

The direction of movement is derived from the value's sign:

Data type	Value	Information
INT	>0	Movement in positive direction in 1/256 full steps
	<0	Movement in negative direction in 1/256 full steps

Unlike the standard function model without enabled SDC information, the motor current is selected using a separate register (see Motor current).

Home position

Name:
RefPulsePos01

These 2 registers contain the following:

Register	Description
Home position of the internal position counter	This register indicates the home position of the internal position counter.
Home position for the ABR counter	This register indicates the home position of the ABR counter.

Data type	Value
INT	-32768 to 32767

The "Position Sync" setting in the Automation Studio I/O configuration can be used to select which of the two registers is be addressed by the variable RefPulsePos01.

Variables in Automation Studio	I/O configuration, Counter 01, "Position Sync" option	
	Stepper counter 01 shown at ActPos01	ABR counter 01 shown at ActPos01
RefPulsePos01	Home position of internal position counter	Home position of ABR counter
The "Position Sync" option also sets bit 3 in the Counter configuration register for Counter 1:		
Bit 3 (counter 1)	0	1

Reference pulse counter

Name:
RefPulseCnt01

These 2 registers contain the following:

Register	Description
Reference pulse counter for the internal position counter	The reference pulses of the internal position counter are counted in this register.
Reference pulse counter for the ABR counter	The reference pulses of the ABR counter are counted in this register.

Data type	Value
SINT	-128 to 127

The "Position Sync" setting in the Automation Studio I/O configuration can be used to select which of the two registers is addressed by the variable RefPulseCnt01.

Variables in Automation Studio	I/O configuration, Counter 01, "Position Sync" option	
	Stepper counter 01 shown at ActPos01	ABR counter 01 shown at ActPos01
RefPulseCnt01	Reference pulse counter for internal position counter	Reference pulse counter of ABR counter
The "Position Sync" option also sets bit 3 in the Counter configuration register for Counter 1:		
Bit 3 (counter 1)	0	1

Net time of the position value

Name:
ActTime01

This register contains the net time of the most recent valid position value.

Data type	Value
INT	-32768 to 32767

Trigger counter

Name:
TriggerCnt01

This register contains a cyclic counter that is incremented with each trigger event.

Data type	Value
SINT	-128 to 127

Trigger timestamp

Name:
TriggerTime01

This register indicates the point in time (net time) of the most recent trigger event. The trigger edge must be configured in the "SDC configuration" register.

Data type	Value
INT	-32768 to 32767

4.25.6.13.8 Register description: Function model 254 - Bus controller and function model 3 - Ramp

4.25.6.13.8.1 Configuration registers

Holding current, rated current and maximum current

Name:
ConfigOutput03a (holding current)
ConfigOutput04a (rated current)
ConfigOutput05a (maximum current)

The holding current, nominal current and maximum current registers are used to configure the desired motor current.

Reasonable values are:

- Holding current < Nominal current < Maximum current

The motor's nominal current is entered in the nominal current register according to the motor's data sheet.

Register	Description
Nominal current	Current during operation at constant speed
Maximum current	Current during acceleration phases. In the mode "Homing during stall", the rated current is always used instead of the maximum current, even in acceleration phases.
Holding current	Current when motor is at standstill

When the current changes to a weaker value (e.g. when transitioning from the acceleration phase to the constant speed mode), the stronger current is maintained for an additional 100 ms. This is done according to the following priority regardless of the actual defined values: maximum current before nominal current before holding current.

Data type	Value	Unit
USINT	0 to 117	Percent of the module's rated current • 100% corresponds to the rated current of the motor bridge power unit listed in the technical data • 117% corresponds to the maximum current of the motor bridge power unit listed in the technical data

Full step threshold

Name:
FullStepThreshold01

This register defines the threshold speed, above which the motor is operated in full step mode, and below which it is operated in microstep mode.

Data type	Value	Information
UINT	1 to 65534	Speed in microsteps / cycle
	65535	Motor is always operated in microstep mode

Maximum speed

Name:
MaxSpeed01pos

This register defines the maximum speed for the absolute positioning modes (1, -123, -124, -125, -126).

Information:

The setting does not apply to the speed and homing modes (2, -127, -128).

Data type	Value	Information
UNIT	0 to 65,535	Speed in microsteps / cycle

Maximum acceleration

Name:
MaxAcc01

This register defines the maximum acceleration (also applies for homing modes).

Data type	Value	Information
UINT	0 to 65,535	Acceleration in microsteps / cycle²

Maximum deceleration

Name:
MaxDec01

This register defines the maximum deceleration (also applies for homing modes).

Data type	Value	Information
UINT	0 to 65,535	Deceleration in microsteps / cycle²

Reversing loop

Name:
RevLoop01

This parameter is only used in mode 1, -123, -124, -125, -126 (absolute positioning modes).

If the value for the reversing loop is not equal to 0, the position setpoint is approached directly when coming from one direction; when coming from the other direction, the position setpoint is initially exceeded by the configured number of steps before finally moving to the position setpoint. This ensures that the position setpoint is always approached from the same direction (to avoid mechanical backlash).

The sign of the defined value determines the direction in which the reversing loop runs.

Sign	Effective direction
Positive	Reversing loop in positive direction of movement
Negative	Reversing loop in negative direction of movement

Data type	Value
INT	-32768 to 32767

Fixed position A

Name:
FixedPos01a

This register defines the position to move to in modes -124 (when 1 is set at the digital input) and -125.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Fixed position B

Name:
FixedPos01b

This register defines the position to move to in modes -124 (when 0 is set at the digital input) and -126.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Homing speed

Name:
RefSpeed01

This register sets the speed for homing modes -127 and -128.

Data type	Value	Information
UINT	0 to 65,535	Speed in microsteps / cycle

Stall recognition delay

Name:
StallRecognitionDelay01

The value in this register is only relevant for "Homing during stall".

A stall is only detected after the time specified here has expired and after the homing procedure has started.

For example, a setting of 4 (and a cycle time of 25 ms) means that a stall will not be detected until 100 ms after the motor starts moving (start of the homing procedure).

Set to 0 to eliminate delay.

Data type	Value	Information
USINT	0 to 255	in cycles, see "General configuration"

Minimum speed for stall detection

Name:
StallDetectMinSpeed01

If the motor speed exceeds the value set in this register, then stall detection is enabled and the configured mixed decay threshold is used. The value 15 is always used for the mixed decay threshold below this threshold value, and no stall error is reported. This means that mixed decay mode is always enabled at low speeds where stall detection principally does not work.

Data type	Value	Information
UINT	0 to 65535	Minimum speed in microsteps per cycle.

Jolt time

Name:
JoltTime01

If a value other than 0 is assigned to this register, then jolt limitation is performed. This is done by averaging the values for the steps to be carried out (speed setpoint) in each cycle using FIFO memory. The jolt time corresponds to the number of FIFO elements (0 to 80). If a value greater than 80 is entered, then it will be limited internally to 80.

Changes made while a motor is running will be applied as soon as ...

- the motor has reached the position setpoint (positioning modes only)
- the motor has stopped (all modes)

Data type	Value	Information
USINT	0	No jolt time limitation
	1 to 80[1)]	Number of FIFO elements

1) Starting with upgrade 1.4.1.0 (firmware version 14); For older versions: 16

Homing configuration

Name:
RefConfig01

The homing mode can be set with this register.

Data type	Value	Information
SINT	-120	Set home position
	-121	Homing at positive edge on input DI 4
	-122	Homing at negative edge on input DI 4
	-125	Homing at positive edge on input DI 3 (R pulse)
	-126	Homing at negative edge on input DI 3 (R pulse)
	-127	Homing during stall detection
	-128	Immediate homing
	Everything else	No effect

Stall detection configuration / Mixed decay

Name:
StallDetectConfig01

The mixed decay threshold and stall detection sensitivity can be configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Mixed decay threshold	0	Mixed decay disabled
		1 to 14	Setting for mixed decay threshold
		15	Mixed decay always enabled
4 - 6	Stall threshold	0	Stall detection is disabled
		1 to 6	Steps involved in setting stall detection sensitivity
		7	Maximum sensitivity for stall detection
7	Motor load	0	Motor load value not shown
		1	Show value in register Status word[1)]

1) If this bit is 1, then the motor load value is shown in bits 13 to 15 of the status word register (otherwise these bits are 0). This value can help when testing the stall detection and the Home during stall mode.

Stall threshold

The SM module features integrated sensorless load measurement for the motor axis. This is especially useful for detecting a "stall condition" (e.g. if the motor moves to the end point during a homing procedure). It cannot be used for torque monitoring during dynamic movements.

The "stall threshold" (bits 4 to 6 of this register) can be used to define a threshold value for each axis individually according to the motor load, beyond which the motor will detect a stall condition.

This threshold value must be determined on a case-by-case basis, since the results of load measurement are influenced by a variety of factors.

- Motor speed: A higher speed results in higher measurement values
- Speeds that cause motor resonances (which interfere with load measurement) are to be avoided
- Motor accelerations that create a dynamic load (and also affect the measurement) should also be avoided
- It is especially important to be aware that mixed decay mode must be optimized for reliable stall detection.

The higher the load measurement value, the lower the load. This means that a stall condition is detected if the load measurement value drops below the trigger threshold for stall detection.

Mixed decay threshold

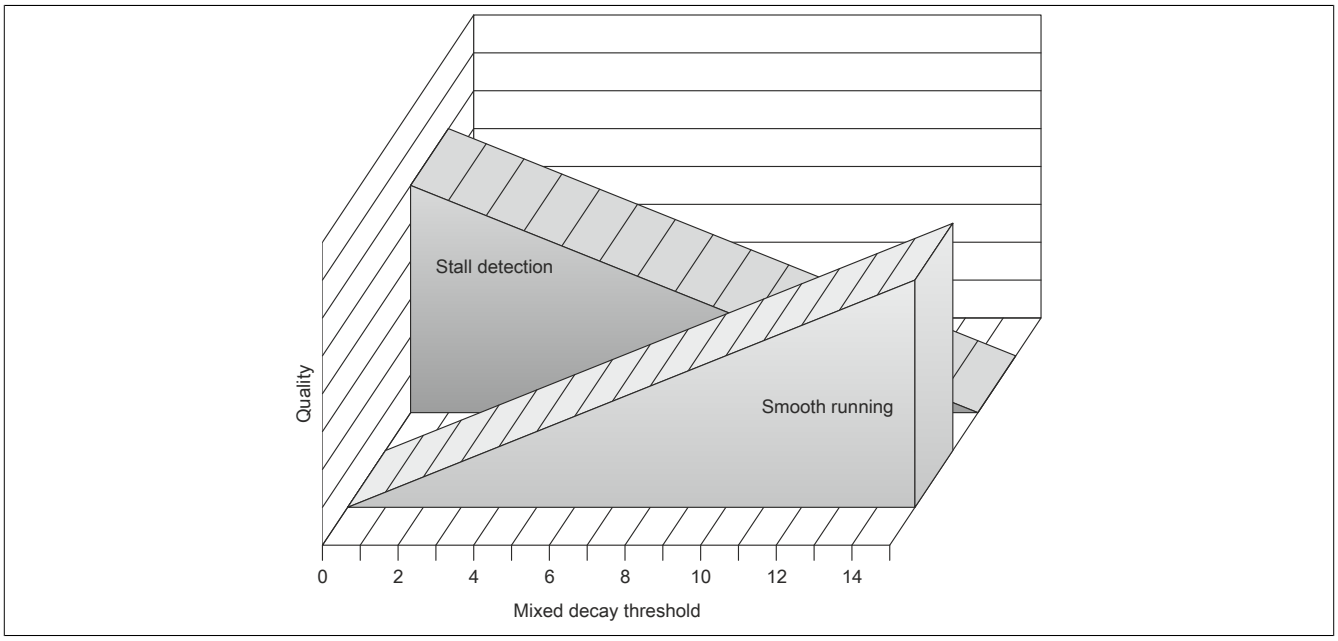
Mixed decay modules provide a greatly optimized sinusoidal current profile in the individual phases of the stepper motor, especially for fast current changes and low current values.

Mixed decay interferes with reliable stall detection, however. For this reason, mixed decay mode can be disabled during stall detection (motor load measurement) using the mixed decay threshold. The smaller the configured mixed decay threshold, the larger the range in which mixed decay is disabled while motor load measurement takes place.

Mixed decay mode is always enabled if the mixed decay threshold is set to 15.

Relationship between stall detection and mixed decay

Depending on the application and the motor used, satisfactorily smooth operation can be achieved while using stall detection by setting the mixed decay threshold to a value between 1 and 14. This is a compromise between smooth operation and stall detection quality and must be fine tuned during commissioning.



General configuration

Name:
GeneralConfig01

Bit 0 of this register can be used to switch the positioning mode. This register can also be used to configure the cycle time of the motion profile generator.

- 0: "Mode 1: Position mode" without extended control word
- 1: "Mode 1: Position mode with extended control word"

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Position mode	0	Without extended control word
		1	With extended control word
1 - 2	Cycle time of the motion profile generator[1)]	00	25 ms
		01	10 ms
		10	5 ms
		11	Reserved
3 - 7	Reserved	0	

1) This parameter is supported starting with upgrade 1.4.1.0 (firmware version 14).

Limit switch configuration

Name:
LimitSwitchConfig01

This register can be used to configure the behavior of the limit switch.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Negative limit switch	00	Off
		01	Active if low
		10	Reserved
		11	Active if high
2 - 3	Positive limit switch	00	Off
		01	Active if low
		10	Reserved
		11	Active if high
4 - 6	Reserved	0	
7	Direction monitoring	0	Off (default)
		1	On

Negative/positive limit switch

When one of the limit switches is reached, a warning is triggered and the speed is decelerated to 0. The "Device Control State Machine" state is not changed. This keeps current flowing to the motor.

The error that occurred can be read from the Error code register. Normal operation can be resumed by acknowledging the warning. This will not restrict motor movement to a specific direction and the limit switch will not be triggered until the next active edge.

Exceeding the limit switch while braking

The limit switches are not linked with the corresponding direction of movement. If the limit switch is exceeded, another error will be triggered when reversing after acknowledging the initial error.

Direction monitoring

If this function is enabled, then the two limit switches will be linked with the respective direction of movement. This means that the negative limit switch is only triggered in the negative direction and the positive limit switch only in the positive direction of movement (specified direction).

This prevents specifying a movement in the wrong direction when direction monitoring is enabled and limit switches are active.

Warning!

If the motor is wired incorrectly with this configuration (wrong direction of movement), then the limit switch will not be triggered and the actual correct direction of movement will be denied. This will also be the case when the limit switch connections are reversed.

Software limit

Name:
PositionLimitMin01
PositionLimitMax01

This register configures software limits. The function is active if at least one of the two registers is unequal to zero.

These limits are effective in all positioning modes. Position overrun is not possible when this function is enabled. Movement is always contained within the two limits.

If a position is specified that violates the minimum/maximum software limit, the "Internal limit active" bit will be set in the Status word register. The motor movement will be stopped until a position is specified within the limits.

The "Internal limit active" bit will also be set in the "Status word" register if there is a configuration error (minimum > maximum).

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Information:

The software limits will only be monitored in connection with the following CANopen bus controllers:

- **X20BC0043-10**
- **X20BC0143-10**
- **X67BC4321-10**
- **X67BC4321.L08-10**
- **X67BC4321.L12-10**

4.25.6.13.8.2 Reading back the configuration

Read ing the holding current, rated current and maximum current

ConfigOutput03aRead (holding current)
ConfigOutput04aRead (rated current)
ConfigOutput05aRead (maximum current)

These registers are used to read the respective current values in percent.

Register	Description
Nominal current	Current during operation at constant speed
Maximum current	Current during acceleration phases
Holding current	Current when motor is at standstill

Data type	Value	Unit
USINT	0 to 255	Percent of the module's rated current (100% corresponds to the rated current of the motor bridge power unit listed in the technical data)

4.25.6.13.8.3 Communication registers

Set position/speed

Name:
AbsPos01

This register is used to set position or speed, depending on the operating mode.

- Position mode (see "Mode"): Cyclic setting of the position setpoint in microsteps. In this mode, one micro-step is always 1/256 full-step.
- Speed mode (see "Mode"): In this mode, this register is used as a signed speed setpoint.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Control word

Name:
MpGenControl01

This register can be used to issue commands based on the module's state (see 4.25.6.13.8.4 "Ramp function model operation").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Switch on	x	
1	Enable voltage	x	
2	Quick stop	x	
3	Enable operation	x	
4 - 6	Mode-specific	x	
7	Fault reset	x	
8	Halt (stop)[1)]	x	
9 - 10	Reserved	0	
11	Motor ID trigger	0	No effect
		1	Rising edge: Motor ID trigger[2)]
12	Warning reset	0	No effect
		1	Rising edge: Reset warnings
13	Undercurrent detection	0	Disable current error detection (default)
		1	Enable current error detection
14	ABR counter sync/async	0	Default: • Internal position counter, cyclic • ABR counter, non-cyclic
		1	• Internal position counter, non-cyclic • ABR counter, cyclic
15	Stall detection	0	Disable stall detection (default)
		1	Enable stall detection

1) The "Halt" bit is only evaluated when the extended control word is enabled (see "General configuration").
2) This bit can be used to trigger a measurement of the motor ID. Keep in mind that the application must ensure that the conditions for measurement are fulfilled (see table in the "Motor ID" register).

Mode

Name:
MpGenMode01

Data type	Value	Information
SINT	0	No mode selected
	1	Depending on bit 0 in the General configuration register, the position mode will behave as follows: • Position mode without extended control word: Move to position setpoint as soon as position setpoint is changed • Position mode with extended control word: Move to position setpoint as described in "Mode 1 - Position mode with extended control word"
	2	Speed mode: Constant speed
	-120	Set home position
	-121	Remaining distance mode
	-122	Set the actual position
	-123	Move to position setpoint when external input is set
	-124	Two-position module
	-125	Move to fixed position A (position set asynchronously)
	-126	Move to fixed position B (position set asynchronously)
	-127	Positive homing (see also "Homing configuration")
	-128	Negative homing (see also "Homing configuration")

Information:

For all modes: The "Target reached" bit is set in the Status word register when the current action is finished (i.e. when the position or speed is reached, depending on the mode).

A new position or speed can be specified even before the current action is finished.

Mode 1 - Position mode

The position setpoint is specified in the Set position/speed register. The motor is then moved to this new position. This is done with a ramp function that accounts for the defined maximum speed and acceleration values.

The position setpoint can also be changed during an active positioning procedure.

The position setpoint is specified in microsteps (1/256 of a full step).

If bit 0 in the General configuration register is 0 (no extended control word), then the position setpoint will be applied as soon as it is different from the current position. The new position is then moved to.

However, if bit 0 in the General configuration register is set to 1 (extended control word), then the position setpoint will be applied as described under "Mode 1 - Position mode with extended control word".

Mode 1 - Position mode with extended control word

The position mode with extended control word behaves like the previously described Position mode 1 (without extended control word) except that the new position setpoint (Position/speed register) is applied according to the extended control word.

Extended control word

This register can be used to issue commands based on the module's state (see 4.25.6.13.8.4 "Ramp function model operation").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Corresponds to the default Control word	x	
4	New setpoint	0	Do not apply position setpoint
		1	Apply position setpoint
5	Change set immediately	0	Complete current positioning movement and then start next positioning movement
		1	Interrupt current positioning movement and then start next positioning movement
6	abs / rel	0	Position setpoint is an absolute value
		1	Position setpoint is a relative value
7	Corresponds to the defaultControl word	x	
8	stop[1)]	0	Execute positioning
		1	Stop axis with deceleration
9 - 15	Corresponds to the defaultControl word	x	

1) This bit applies to all modes.

Extended status word

The bits in the status word reflect the status of the state machine (for a detailed description, see "Status word" and "State machine").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 9	Corresponds to the defaultStatus word	x	
10	Target reached, depending on bit 8 (Halt) in the register Control word		**If Halt = 0**
		0	Position setpoint not reached
		1	Position setpoint reached
			If Halt = 1
		0	Axis decelerating
		1	Axis speed = 0
11	Corresponds to the defaultStatus word	x	
12	Setpoint acknowledge	0	Ramp generator did not apply the position value
		1	Ramp generator applied the position value
13 - 15	Corresponds to the defaultStatus word	x	

Position setting

The position setpoint can be defined in two different ways:

Type of setpoint definition	Description
Single setpoint	Once the position setpoint is reached, the *Target reached* bit in the Status word register is set. Then a new position setpoint is defined. The drive stops at each position setpoint before starting the movement to the next position setpoint.
Set of setpoints	Once a setpoint has been reached, the movement to the next setpoint is started immediately without stopping the drive. It is therefore not possible to initiate a new positioning movement by transferring a new position setpoint during an active positioning movement.

Table 570: Types of position setpoint definition

The two modes "Single setpoint" and "Set of setpoints" are controlled by the timing of the bits *New setpoint* and *Change set immediately* in the *extended control word* and *Setpoint acknowledge* in the *Extended control word* register.

These bits can be used to create a Request-Response mechanism. This makes it possible to specify a position setpoint while previous setpoint is still being processed.

Transferring the position setpoint

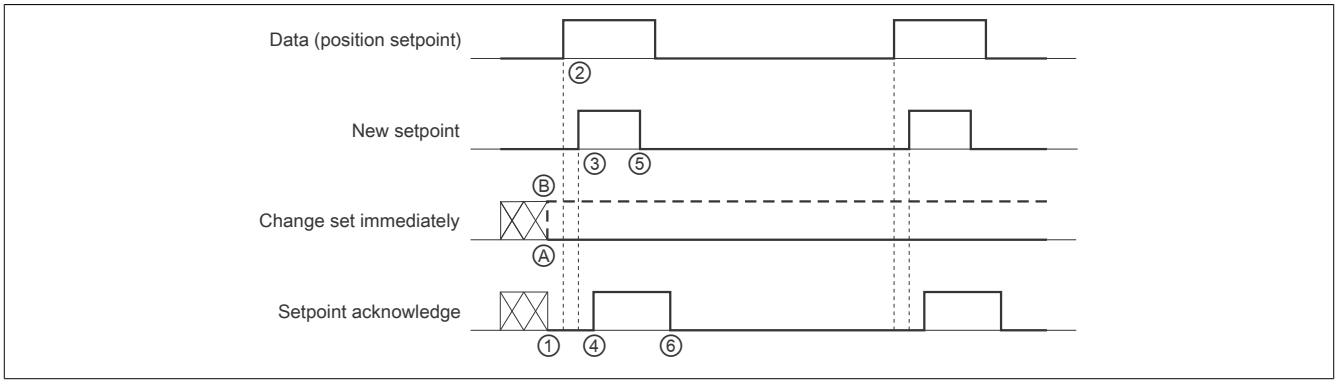


Figure 386: Principle for applying the setpoint

Transferring a new setpoint:

1. When the *Setpoint acknowledge* bit in the Extended status word register is 0, the module will accept a new position setpoint.
2. The new position setpoint is specified in the *Set position/speed*.
3. A rising edge of the *New setpoint* bit in the Extended control word register signalizes that the new position setpoint in the *Set position/speed* register is valid and can be used for the next positioning movement.
4. Once the module has received and saved the new position setpoint, the *Setpoint acknowledge* bit in the *Status word* register is set to 1.
5. Now the controller can reset the *New setpoint* bit to 0.
6. Then the module resets the *Setpoint acknowledge* bit to 0 to signal when a new position setpoint is accepted.

"Single setpoint" mode

When the *Change set immediately* bit is set to 0 (Ⓐ in figure "Principle for applying the setpoint"), then the module is operating in *Single setpoint* mode. This mechanism results in a speed of 0 when the motor reaches position setpoint x_1 at time t_1. After the controller has been notified that the setpoint has been reached, the next setpoint x_2 will be processed at time t_2 and reached at t_3.

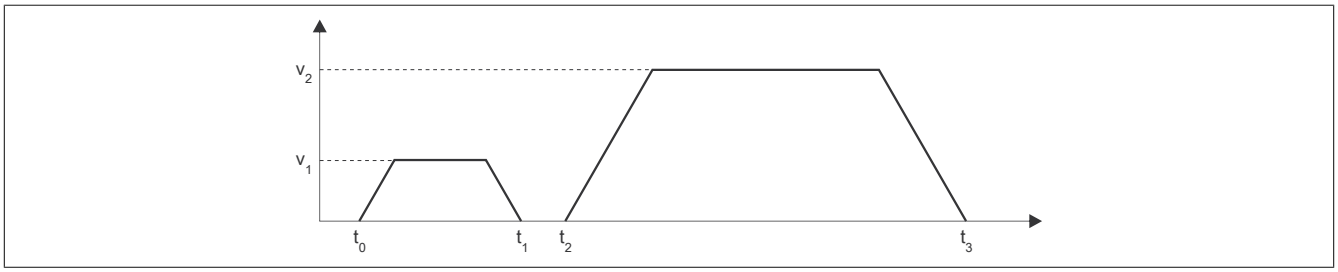


Figure 387: Ramp in *Single setpoint mode*

"Set of setpoints" mode

When the *Change set immediately* bit is set to 1 (Ⓑ in figure "Principle for applying the setpoint"), then the module is operating in *Single setpoint* mode. This means that the module receives the first position setpoint at t_0. A second position setpoint is received at the time t_1. The drive immediately adapts the current movement to the new setpoint.

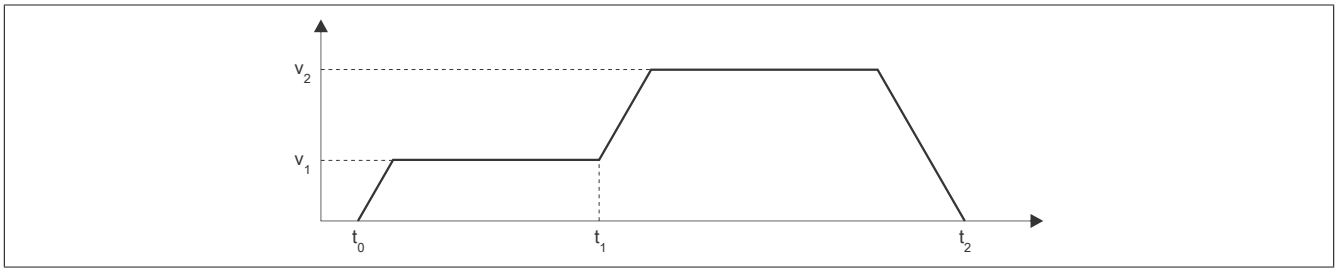


Figure 388: Ramp in *Set of setpoints mode*

Relative position setting

When the *abs / rel* bit in the Extended control word register is set, then the position setpoint is interpreted as a relative value. At each *New setpoint* trigger, the position setpoint will be increased by this value (or decreased if the value is negative).

If the mode changes between the position settings, relative movement will then proceed starting at the last specified position. The position setpoint mode is initialized with 0 when the module is started.

Mode 2: Speed mode - Constant speed (pos./neg.)

The value in the Position/speed register is now interpreted as the speed setpoint (microsteps/ cycle).

Observing the maximum permissible acceleration, the motor moves with a ramp to the desired speed setpoint and maintains this speed until a new speed setpoint is specified.

Values are allowed within the range -65535 to 65535. When a value is entered outside of this range, it is readjusted to these limits.

Mode -120: Set home position

This mode is supported starting with upgrade 1.4.1.0 (firmware version 14).

The current actual position is modified so that the position specified by the Position/speed register is at the home position. If you subsequently move to this position, the motor is at the home position.

The home position in the "Home position" register is also set to this value.

Before this mode is called, the motor must be at a standstill and the home position must have been determined using the "Positive / negative homing" mode. In order to set the position, the State machine must be in the state "Operation Enable".

Mode -121: Remaining distance mode (like Modus 1)

The number of steps defined in the "Fixed position A" register are added to the current position and the resulting position is approached at a rising/falling edge on digital input 3.

Note:

Steps are not added to the position setpoint, but rather to the current position at the moment the trigger occurs.

Negative values are also allowed for the offset defined in "Fixed position A".

New position setpoints are no longer accepted in the Position/speed register after the trigger event. There must first be a switch made to mode 0 and then back to mode -121.

The "Target reached" bit in the Status word register is not set to 1 until the end position (after the trigger event) has been reached.

The Homing configuration determines whether a rising or falling edge of the digital input is used as a trigger.

The Reversing loop is not enabled in this mode (i.e. any configured values not equal to 0 are ignored).

Mode -122: Set the actual position

The position setpoint set in the "Position/speed" register is accepted as the current actual position in the internal position counter when the state machine is in the "Operation Enable" state.

Before this mode is started, the motor must be at a standstill and physically located at the point for which the position being set should be applied.

Mode -123: Move to the position setpoint when the external input is set

The set position defined in the "Position/speed" is moved to when a rising edge occurs on the corresponding digital input.

A new position setpoint is not accepted until another rising edge occurs on the corresponding digital input. This can also occur during the active positioning procedure and will be applied immediately.

Mode -124: Two position mode

The positions "Fixed position A" and "Fixed position B" are defined in the non-cyclic registers.

The value 1 on digital input 3 moves to fixed position A. The value 0 moves to fixed position B. It is also possible to switch between the two during an active positioning movement.

Mode -125/-126: Move to fixed position X

The purpose of these modes is to enable a virtual switch from speed mode to position mode, which otherwise isn't possible because of the double use of the register for position and speed setpoints.

- Mode -125: Fixed position A
- Mode -126: Fixed position B

Mode -127/-128: Homing (positive/negative)

Mode -127 and -128 are used to select which direction to move in.

The motor must be at a standstill before switching from another mode to one of the homing modes.

If the homing condition occurs, then the motor stops and the values of the position counter and ABR counter valid at the moment when the homing condition occurs are written to the Homed zero position register.

You must specify in the Homing configuration whether homing should occur at low/high level on the digital input, during stall or unconditionally.

Homing via digital input

Case 1: Active homing level not yet reached → Motor not yet at end position:

Movement continues at homing speed in the homing direction until the active level for "homing-stop" is on the digital input.

Case 2: Active homing level already reached → Motor at end position:

Movement continues at the homing speed, counter to the homing direction, until the active level for "homing-stop" is no longer on the digital input. Movement continues at homing speed in the homing direction until the active level for "homing-stop" is on the digital input again.

Homing during stall

Movement continues in the homing direction until a stall is detected. When a stall is detected, the value of the position counter is entered in the Homed zero position register within one millisecond. The motor is then stopped abruptly (not using the deceleration ramp). However, it can take up to 25 ms to stop the motor because the ramp generator runs with a configurable internal cycle of up to 25 ms.

In this mode, the rated current is always used instead of the maximum current, even in acceleration phases.

To test the response behavior of this homing mode, the motor load value used for identifying a stall can be made visible in the status word (see "Stall detection configuration / Mixed decay").

Homing unconditional (immediate)

Immediate homing: The current values of the position counter and ABR counter are immediately entered in the Homed zero position register (no motor movement).

Current position (cyclic)

Name:
AbsPos01ActVal

This cyclic register contains the current position.

Default: Value of the internal position counter, can be changed to ABR counter

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Status word

Name:
MpGenStatus01

The bits in this register reflect the state of the state machine. For a more detailed description, see "Status word" and "State machine".

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Ready to switch on	x	
1	Switched on	x	
2	Operation enabled	x	
3	Fault (error bit)	x	
4	Voltage enabled	x	
5	Quick stop	x	
6	Switch on disabled	x	
7	Warning	x	
8	Reserved	0	
9	Remote	1	Always 1 because there is no local mode for the SM module
10	Target reached	x	
11	Internal limit active	0	No limit violation
		1	Internal limit is active (upper/lower software limit violated)
12	Mode-specific	x	
13 - 15	Reserved / Motor load value	0	Always 0 when bit 7 in the Stall detection configuration / Mixed decay register is set to 0.
		x	Returned motor load value

Input status

Name:
InputStatus

This register indicates the logical states of digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Digital input 1	0 or 1	Input state - Digital input 1
...		...	
3	Digital input 4	0 or 1	Input state - Digital input 4
4 - 15	Reserved	0	

Motor ID

Name:
Motoridentification01

This register is used to identify the connected motor type for service purposes and to differentiate between motors in the application. Following measurement, this register contains the time [µs] needed to apply a current increase of ΔI = 1 A to a motor winding.

This depends on:

- Operating voltage
- The inductance and resistance of the motor winding

Notes		
1)	To achieve reproducible results, the measurement must be made under the following defined conditions:	
	a)	Motor is at standstill
	b)	The motor must be in a half-step position (phase A fully powered, phase B not powered). This means the internal position counter on the SM module must have a value that fulfills the following conditions: • Full steps are divisible by 4 • Microsteps = 0
2)	Condition 1b) is fulfilled after a the SM module is reset or powered on. Immediately afterwards, when the holding current is applied to the motor for the first time (at standstill), the duration for applying the current is measured. This is therefore a suitable time to read the motor identification register in the application.	
3)	The current range from approximately 1/3 of the rated current up to the rated current is used as operating range for determining the motor identifier.	

Data type	Motor ID values	Function
UINT	0	No motor identifier available (after turning on for as long as the measurement conditions are not met)
	1 to 32767	Valid range of values for the motor ID register (in µs)
	65504 to 65519	Ground fault: Motor identification not possible
	65528	Motor ID trigger not possible • Motor has no power applied • Motor in movement • Rated current is set to 0A • Ground fault present
	65529	Invalid value: Underflow
	65530	Overtemperature: Measurement not possible
	65532	Open line: Measurement not possible
	65533	Motor position incorrect: Measurement not possible
	65534	Invalid value: Overrun
	65535	Measurement in progress

Ground fault detection

When the motor is powered on, a ground fault check is performed before motor identification. Error numbers have been added in the motor identification register for the event of a ground fault error (values 65504 to 65519 in the table above).

Homed zero position

Name:
RefPos01CyclicCounter
RefPos01AcyclicCounter

After a homing procedure, the homing position for the cyclic and non-cyclic position counter can be read using these registers (either the internal position counter or ABR counter depending on bit 14 of the "Control word" register).

The following two registers are provided for the motor:

- Homed zero position for cyclic counter
- Homed zero position for non-cyclic counter

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Current position (acyclic)

Name:
AbsPos1ActValAcyclic

This acyclic register contains the current position.

Default: Value of the ABR counter, can be changed to internal position counter

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Reads the extended control word

Name:
ControlReadback01

This register can be used to read the content of the Control word register.

Data type	Value
UINT	0 to 65535

Read back mode

Name:
ModeReadback01

This register can be used to read the content of the Mode register.

Data type	Value
SINT	-128 to 127

Error code

Name:
ErrorCode01

The cause of an error or warning can be read in this register.

Data type	Error code	Error type	Priority	Description
UINT	0x0000	-	-	No error
	0x3000	Error	High	Voltage
	0x4200	Error	:	Overtemperature
	0xFF20	Warning	:	Negative limit switch
	0xFF21	Warning	:	Positive limit switch
	0x2300	Warning	:	Overcurrent
	0xFF00	Warning	:	Current error[1)]
	0xFF01	Warning	Low	Stall [2)]

1) A current error is only detected if bit 13 = 1 in the control word (current error detection enabled).
2) Stall is only detected if bit 15 = 1 in the control word (stall detection enabled).

Information regarding the handling of errors and warnings:

- Bit 3 (Fault) and bit 7 (Warning) in the status word can be used to query whether an error or a warning was reported in the error code register.
- Bit 7 (Fault Reset) and bit 12 (Warning Reset) in the control word are used to acknowledge pending errors and warnings.
- If two or more errors/warnings are pending, the one with the highest priority (the order in the table above) will be displayed in the error code register.

4.25.6.13.8.4 Ramp function model operation

Control for this model has been based on the CANopen communication profile DS402.

Commands for controlling the modules are written to the "Control word". The current module state is returned to the "Status word" register. The function mode (absolute position, constant speed, homing, etc.) is set in the "Mode" register.

Control word

Control word bits and their state for the commands of the state machine:

Command	Reserved	ABR counter sync/async	Current error detection	Warning reset	Motor ID trigger	Reserved	Reserved	Halt 2)	Fault reset	Mode specific	Mode specific	Mode specific	Enable operation	Quick stop	Enable voltage	Switch on
Bit[1]	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Shutdown	x	x	x	x	x	0	0	x	0	x	x	x	x	1	1	0
Switch on	x	x	x	x	x	0	0	x	0	x	x	x	0	1	1	1
Disable voltage	x	x	x	x	x	0	0	x	0	x	x	x	x	x	0	x
Quick stop	x	x	x	x	x	0	0	x	0	x	x	x	x	0	1	x
Disable operation	x	x	x	x	x	0	0	x	0	x	x	x	0	1	1	1
Enable operation	x	x	x	x	x	0	0	x	0	x	x	x	1	1	1	1
Fault reset	x	x	x	x	x	0	0	x	↑	x	x	x	x	x	x	x

1) x ... Any; ↑ ... Rising edge
2) Bit 8 (Halt) is only evaluated if the extended control word is enabled in the "General configuration" register.

Bits 0, 1, 2, 3 and 7 (light gray in the previous table)	These bits control the state of the "State machine" according to the commands in the table above.
stop	0 ... Perform motor movement 1 ... Stop axis with deceleration This bit is only evaluated when the extended control word is activated in the "General configuration" register.
Motor ID trigger	A rising edge enables the motor ID measurement.
Warning reset	A rising edge resets warnings (no effect on errors, which are reset using "Fault Reset"; the state machine is not affected by this bit)
Fault reset	A rising edge resets errors and warnings (see "State machine" on page 2429)
Current error detection	0 ... Current error detection disabled 1 ... Current error detection enabled
ABR counter sync/async	0 ... Value of the ABR counter on the "Current position (non-cyclic)" register. Internal position counter of the ramp generator on the "Current position (cyclic)" register. 1 ... Value of the ABR counter on the "Current position (cyclic)" register. Internal position counter of the ramp generator on the "Current position (non-cyclic)" register.
Stall detection	0 ... Stall detection disabled 1 ... Stall detection enabled

Status word

The individual bits of this register and its states depend on the current state of the state machine:

Status	Reserviert / MotorLoadBit 2 [1]	Reserviert / MotorLoadBit 1 [1]	Reserviert / MotorLoadBit 0 [1]	Mode-specific	Int. limit active	Target reached	Remote	Reserved	Warning	Switch on disabled	Quick stop	Voltage enabled	Fault	Operation enabled	Switched on	Ready to switch on
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not ready to switch on	x	x	x	x	x	x	1	0	x	0	x	0	0	0	0	0
Switch on disabled	x	x	x	x	x	x	1	0	x	1	x	0	0	0	0	0
Ready to switch on	x	x	x	x	x	x	1	0	x	0	1	0	0	0	0	1
Switched on	x	x	x	x	x	x	1	0	x	0	1	1	0	0	1	1
Operation enable	x	x	x	x	x	x	1	0	x	0	1	1	0	1	1	1
Quick stop active	x	x	x	x	x	x	1	0	x	0	0	1	0	1	1	1
Fault reaction active	x	x	x	x	x	x	1	0	x	0	x	0	1	1	1	1
Fault	x	x	x	x	x	x	1	0	x	0	x	0	1	0	0	0

1) If bit 7 is set to 1 in the Mixed decay / Stall detection register, then the motor load value is returned in bits 13-15 of the status word. Otherwise these bits are always 0.

Information about the status word:

Bits 0,1,2,3,5 and 6 (light gray in the previous table)	These bits are set according to the current state of the "State machine".	
Voltage enabled	Becomes 1 as soon as the motor is powered	
Warning	Becomes 1 if a warning is detected ("Overcurrent", "Undercurrent"). The type of warning is indicated in the "Error code" register. The highest priority error / warning is shown in each case, with the priority corresponding to the order in the respective table. Warnings can be reset with a rising edge on the "Warning reset" bit in the control word.	
Remote	Always 1 since there is no local mode on the SM module	
Target reached[1], depending on bit 8 (Halt) in the register Control word	**If Halt = 0**	**If Halt = 1**
	In modes 1, -123, -124, -125 and -126 (absolute positioning): 0 ... Positioning begins 1 ... Target has been reached **In mode 2 (constant speed):** 0 ... Motor accelerates/brakes 1 ... Speed setpoint reached **In modes -127 and -128 (homing):** 0 ... Homing started 1 ... Homing ended **In mode -122 (set actual position):** The bit briefly becomes 0 and immediately becomes 1 again as soon as the position is set.	**In all modes:** 0 ... Axis decelerating 1 ... Axis speed = 0
Internal limit active	0 ... No limit violation 1 ... Internal limit is active (upper/lower software limit violated)	

Table 571: Information about the status word

1) If Halt has not been activated in the "General configuration" register, then "Target Reached" behaves the same as when Halt = 0.

State machine

The motor is controlled according to the state machine illustrated below. After the module is started, the state machine automatically changes to the state "*Not ready to switch on*". The application then operates the state machine by writing commands to the "Control word".

The state machine successively reaches the states "*Ready to switch on*", "*Switched on*" and "*Operation enable*" by writing the consecutive commands "*Shutdown*", "*Switch on*" and "*Enable operation*".

Information:

Motor movements are not performed until the "*Operation enable*" state, according to the setting in the Mode register.

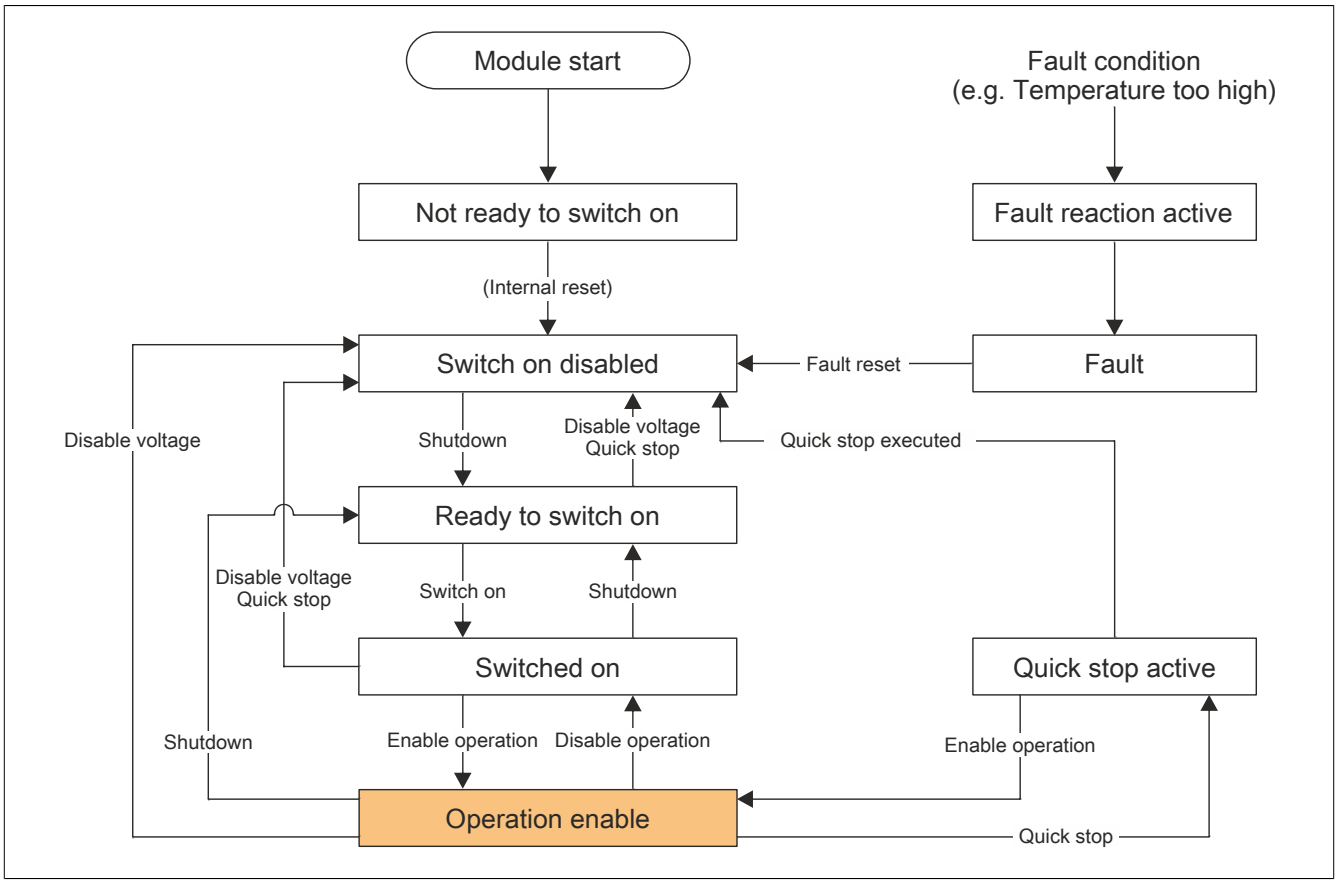


Figure 389: State machine - Flow chart

State change	Description
Not ready to switch on → Switch On Disabled	This state change occurs automatically after starting the module and internal initialization has taken place.
Switch on disabled → Ready to Switch On	This state change is brought on by the *Shutdown* command. No others actions are performed.
Ready to switch on → Switch On Disabled	This state change is brought on by the command *Disable voltage* or *Quick stop*. No others actions are performed.
Switched on → Switch On Disabled	This state change is brought on by the command *Disable voltage* or *Quick stop*. The motor voltage is switched off immediately.
Ready to switch on → Switched On	This state change is brought on by the *Switch on* command. The motor voltage is switched on. When this state change occurs for the first time since the module is started, the motor ID measurement is performed before the *Switched on* state is achieved. This can take approximately 1 second.
Switched on → Ready to Switch On	This state change is brought on by the *Shutdown* command. The motor voltage is switched off immediately.
Switched on → Operation Enable	This state change is brought on by the *Enable operation* command. Motor movements are now performed depending on the defined mode.
Operation enable → Switched On	This state change is brought on by the *Disable operation* command. If in motion, the motor is decelerated with the configured deceleration. Motor voltage remains on in the *Switched on* state.
Operation enable → Ready to Switch On	This state change is brought on by the *Shutdown* command. The motor voltage is switched off immediately.
Operation enable → Switch On Disabled	This state change is brought on by the *Disable voltage* command. Motor voltage switched off. It is strongly recommended to only make this state change on a stopped motor since regeneration on a motor running at no load can cause an overvoltage error on the DC bus (0x3210).
Operation enable → Quick Stop Active	This state change is brought on by the *Quick stop* command. If in motion, the motor is decelerated with the configured deceleration. During the deceleration, the state machine remains in the *Quick stop active* state. Once the motor is at standstill, the state automatically changes to the *Switch on disabled* state. While the state machine is in the *Quick stop active* state, the *Enable operation* command can be used to switch it back to the *Operation enable* state.
→ Fault reaction active	This state change is brought on when an error occurs and cannot be triggered by a command from the user. It can be triggered by error types classified as an "Error" (see "Error code"). (Other error types listed as "Warning" only cause the "Warning" bit to be set in the status word and do not cause a state change in the state machine.) Motor voltage is switched off and the state machine then changes immediately to the *Fault* state. The type of error is listed in the error code register (see the table under "Error code"). The highest priority error is shown. The priority corresponds to the order in the error code table.
Fault → Switch On Disabled	This state change is brought on by the *Fault reset* command. However, the state only changes if no more errors are present when the command is written. All errors and warnings are reset. The error code register contains 0 or the warning code if a warning is still present.

Table 572: State machine - State change

4.25.6.13.9 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Standard function model	250 µs
Ramp function model	250 µs

4.25.6.13.10 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Standard function model	250 µs
Ramp function model	
Inputs	250 µs
Outputs[1)]	25 ms

1) Depending on the configuration of the motion profile generator

4.25.7 X20SM1436

4.25.7.1 General information

The stepper motor module is used to control stepper motors with a rated voltage of 24 to 39 VDC (±25%) at a motor current up to 3 A (3.5 A peak). Additionally, this module has four digital inputs that can be used as limit switches or as encoder inputs.

By individually adjusting the coil currents, the motor is only operated with the current it actually needs. This simplifies the selection of the available motors and prevents unnecessary heating. Because the latter reduces energy consumption and thermal load, the effects are positive on the lifespan of the complete system. Complete flexibility is achieved by using the values for holding current, maximum current and rated current, which are completely independent of each other. The current for the microsteps is automatically adjusted to the configured current values.

The automatic motor identification system is an enormous help during standstills. The stepper motor modules can identify the connected motors using their coil characteristics and generate feedback in the form of an analog value. This makes it possible to detect not only wiring errors, but also incorrect motor types being used mistakenly. A stall detection mechanism is integrated to analyze the motor load. The stall is recognized using a configurable threshold. This allows an overload or motor standstill to be detected precisely in many different types of applications.

- 1 stepper motor, 24 to 39 VDC ±25%, 3 A (3.5 A peak)
- Resolution of current values at 1%
- Boost, rated and holding current configured independent of each other
- 38.5 kHz PWM frequency
- Integrated motor detection
- 256 micro-steps
- Stall detection
- Complete integration in Automation Studio and CNC applications
- 4 inputs, 24 VDC, can be configured as ABR
- Ramp function model based on the CANopen communication profile DS402

4.25.7.2 Order data

Model number	Short description	Figure
	Motor controllers	
X20SM1436	X20 stepper motor module, module supply 24-39 VDC ±25%, 1 motor connection, 3 A continuous current, 3.5 A peak current, 4 digital inputs 24 VDC, sink, can be configured as incremental encoder	
	Required accessories	
	Bus modules	
X20BM31	X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 573: X20SM1436 - Order data

4.25.7.3 Technical data

Product ID	X20SM1436
Short description	
I/O module	1 full bridge for controlling stepper motors
General information	
B&R ID code	0x2682
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Output	Yes, using status LED and software
I/O supply	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	-
External I/O	
24 VDC	2.45 W
48 VDC	3.15 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - I/O supply	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Motor bridge - Power unit	
Quantity	1
Type	2-phase bipolar stepper motor (full bridge)
Nominal voltage	24 to 39 VDC ±25%
Nominal current	3 A
Maximum current	3,5 A for 2 s (after a recovery time of at least 10 s at maximal 3 A)
Controller frequency	38.4 kHz
DC bus capacitance	100 µF
Step resolution	Max. 256 microsteps per step
Module supply	
Supply	External
Fuse	Required line fuse: Max. 16 A, slow-blow
Output protection	No reverse polarity protection for supply voltage
Digital inputs	
Quantity	4
Nominal voltage	24 VDC
Input filter	
Hardware	<5 µs
Software	-
Connection type	1-wire connections
Input circuit	Sink
Additional functions	1x ABR incremental encoder
Input resistance	Typ. 18.2 kΩ
ABR incremental encoder	
Quantity	1
Encoder inputs	24 V, asymmetrical
Counter size	16-bit
Input frequency	Max. 50 kHz
Evaluation	4x
Operating conditions	
Mounting orientation	
Horizontal	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 50°C
Vertical installation	Not allowed
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C

Table 574: X20SM1436 - Technical data

Product ID	X20SM1436
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM31 bus module separately
Spacing	25 $^{+0.2}$ mm

Table 574: X20SM1436 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

4.25.7.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset state
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green		Input state of the corresponding digital input
	M	Orange	On	Motor is active

1) Depending on the configuration, a firmware update can take up to several minutes.

4.25.7.5 Pinout

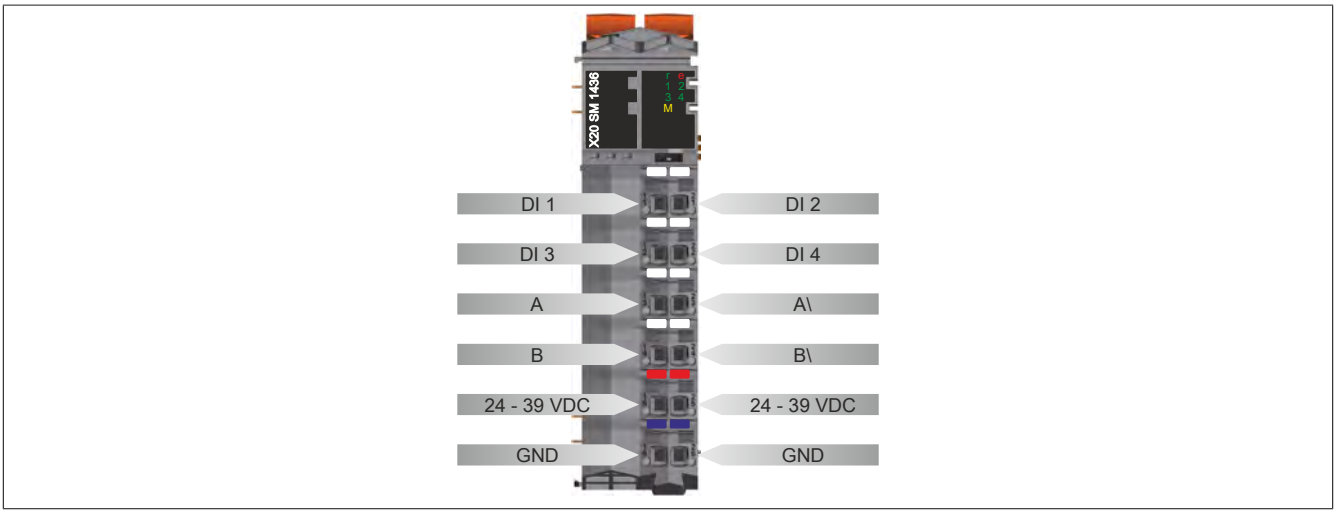
In accordance with the EN60204-1 standard, a cable cross section of 0.75 mm² or larger must be used for the motor outputs in order to handle the maximum motor current of 3.5 A. To ensure full motor power, voltage drops that could result from the cable length and the electrical connections must also be taken into consideration when selecting the attachment cable.

Warning!

The terminal block is not permitted to be plugged in or unplugged during operation.

Information:

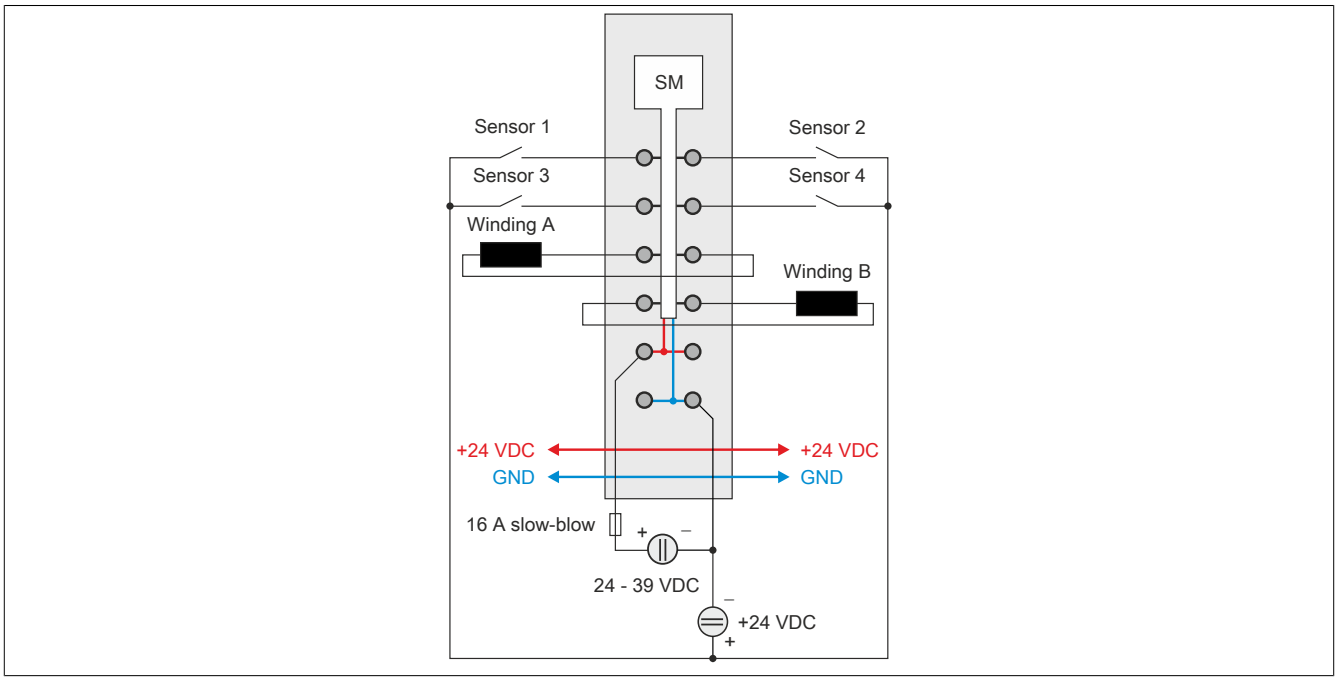
Shielded motor cables must be used in order to meet the limits according to the EN55011 standard (emissions).



4.25.7.6 Connection example

Information:

This module can only be operated if supplied with power via the terminal block.



4.25.7.7 Connection options for digital inputs

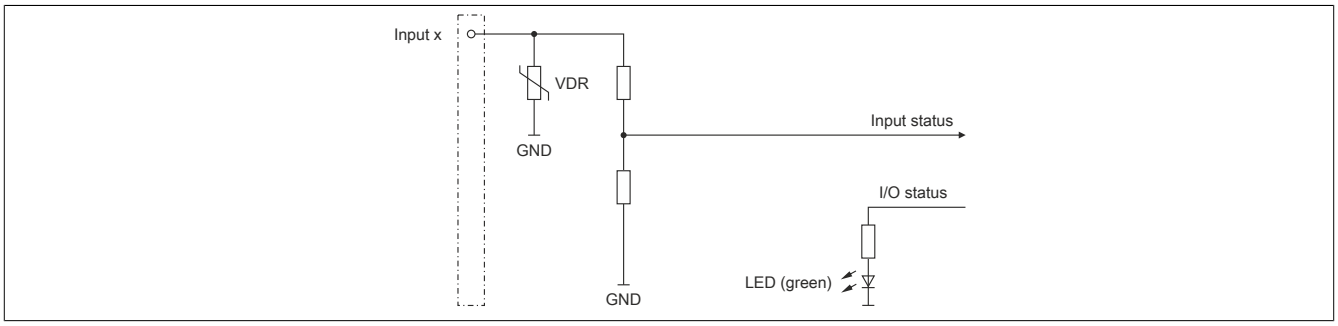
Standard function model

Channel	Function	
DI 1	Digital input	A
DI 2	Digital input	B
DI 3	Digital input	R
DI 4	Digital input	Trigger input

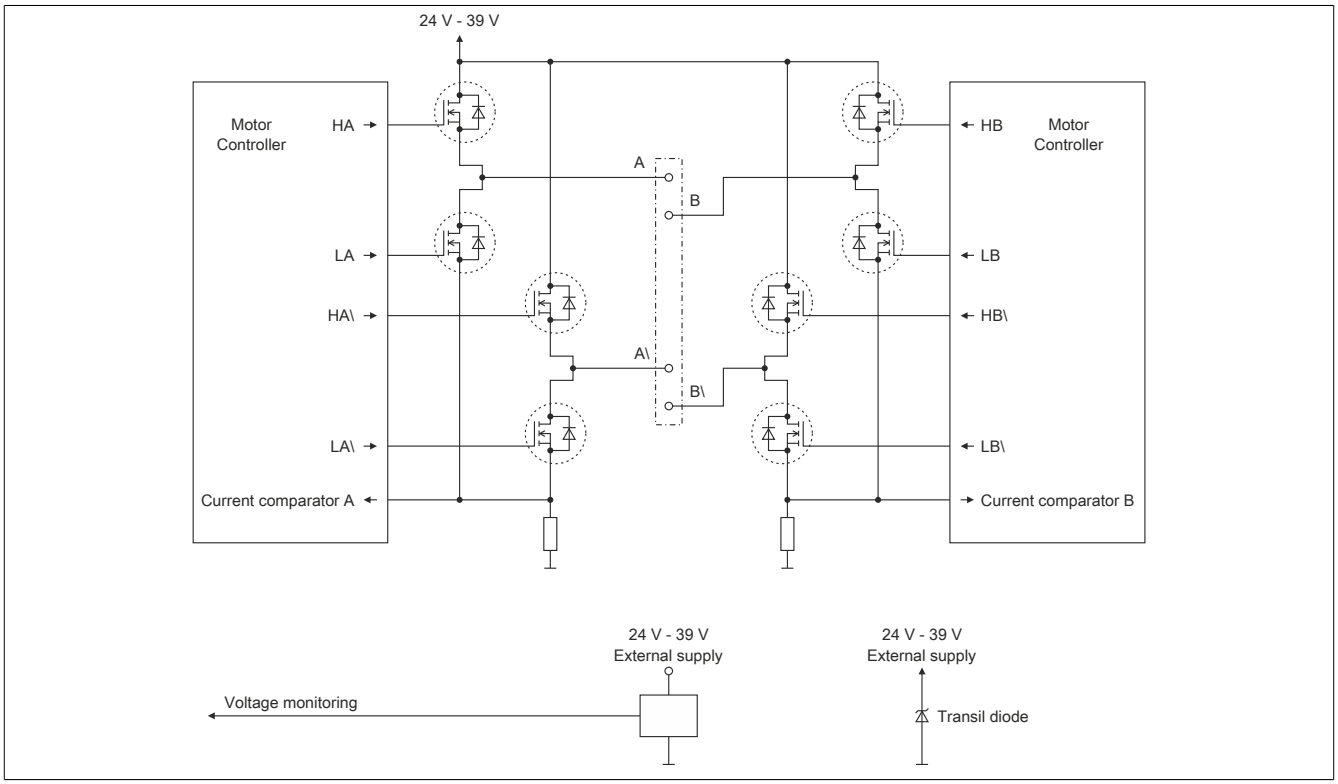
Ramp function model

Channel	Function		
DI 1	Digital input	A	A
DI 2	Digital input	B	B
DI 3	Digital input	R	Negative limit switch
DI 4	Digital input	Digital input	Positive limit switch

4.25.7.8 Input circuit diagram



4.25.7.9 Output circuit diagram



4.25.7.10 Overvoltage motor cutoff

The module supply voltage is continually monitored. Its status can be read. The error "Module power supply error" occurs when the voltage is above or below the limits.

If the supply voltage on the module rises or falls outside the limit values (e.g. due to regeneration), then the motor output is switched off.

The outputs are reactivated as soon as the supply voltage is back in the valid range and the error bit is reset.

Supply voltage limit values

	Drive is switched off	Drive is switched back on
Lower limit	<18 V	>19.5 V
Upper limit	>50 V	<49 V

4.25.7.11 Overtemperature cutoff (at 85°C)

If the module temperature reaches or exceeds the limit value of 85°C, then the module executes the following actions:

- Setting the "overtemperature" error bit
- The outputs are switched off (short-circuited)

As soon as the temperature sinks back down below 85°C, the error must be acknowledged with OvertemperatureAcknowledge so that the channels can be switched on again.

4.25.7.12 Power supply dimensioning

The motor's current consumption depends on the defined motor currents, the available power and the actual motor being used.

Example	
Motor model number	80MPD5.300S000-01
Defined current in the motor module	3 A
Motor module supply voltage	48 VDC
Motor load	1 Nm

Table 575: Power supply dimensioning example - Basic data

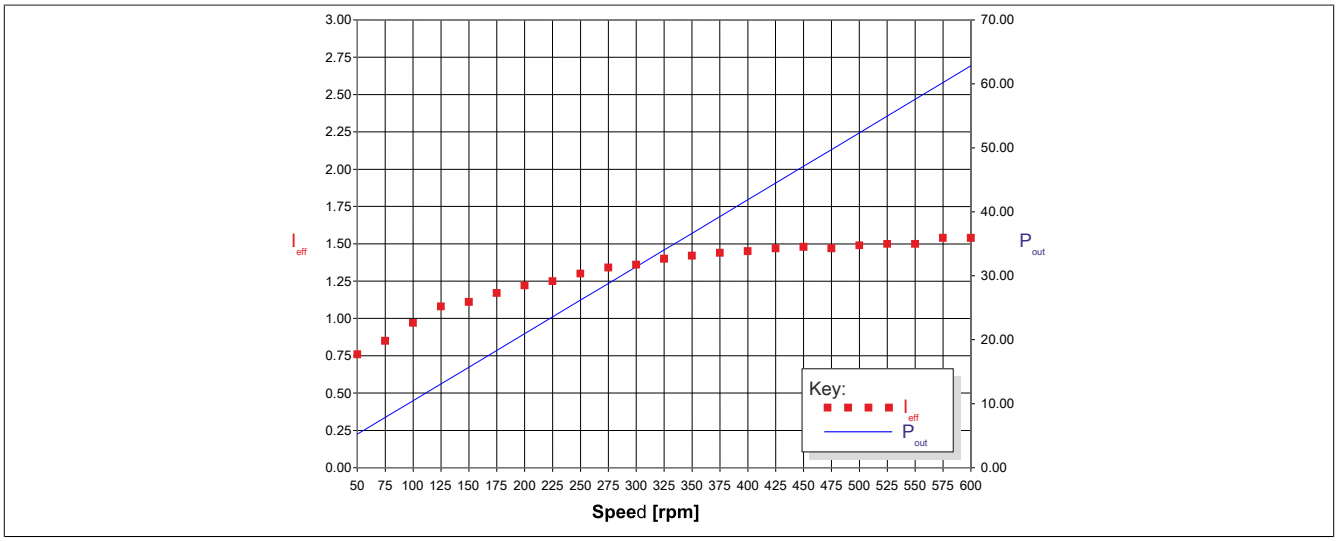


Figure 390: Power supply dimensioning example - Power/speed dependency

The example is based on a constant load throughout the entire speed range.

An increase in the motor load causes an increase in the effective current of the module supply.

4.25.7.13 Protection

The power supply line should be protected by a circuit breaker or a fuse. In general, dimensioning the supply line and overcurrent protection depends on the structure of the power supply (modules can be connected individually or in groups).

Information:

The effective current for the power supply depends on the load but is always less than the motor current. Make sure the maximum nominal current of 10 A is not exceeded on the power supply terminals of the power unit.

When choosing a suitable fuse, the user must also account for characteristics such as aging effects, temperature derating, overcurrent capacity and the definition of the rated current, which can vary by manufacturer and type. In addition, the fuse that is selected must also be able to handle application-specific characteristics (e.g. overcurrent that occurs in acceleration cycles).

The cross section of the power mains and the rated current of the overcurrent protection used are chosen according to the current load so that the maximum current load for the cable cross section selected (based on the type of wiring, see table) is greater than or equal to the current load in the power mains. The rated current of the overcurrent protection must be less than or equal to the maximum current load for the cable cross section selected (based on the type of wiring, see table):

I_{Mains}	≤	I_b	≤	I_Z
Mains	≤	Fuse	≤	Line/cable

	Maximum current load for cable cross section I_Z / rated current for overcurrent protection I_b [A] depending on the type of wiring at an ambient air temperature of 40°C in accordance with IEC 60204-1			
Wire cross section [mm²]	**B1**	**B2**	**C**	**E**
1.5	13.5 / 13	13.1 / 10	15.2 / 13	16.1 / 16
2.5	18.3 / 16	16.5 / 16	21 / 20	22 / 20

Table 576: Cable cross section of the mains supply line depending on the type of wiring

The tripping current of the fuse must not exceed the rated current for overcurrent protection I_b.

Type of wiring	Description
B1	Wires in conduit or cable duct
B2	Cables in conduit or cable duct
C	Cables or wires on walls
E	Cables or wires on open-ended cable tray

Table 577: Type of wiring used for the mains supply line

4.25.7.14 Derating

Modules next to the SM module can have a maximum power consumption of 1 W. To ensure proper operation, the derating values listed below must be adhered to:

Power loss derating for neighboring modules

Modules directly next to the SM module can have a power loss of 1 W. If the SM module is operated at the rated load over the entire temperature range (3 A rated current), the power loss of neighboring modules must be derated starting at 45°C.

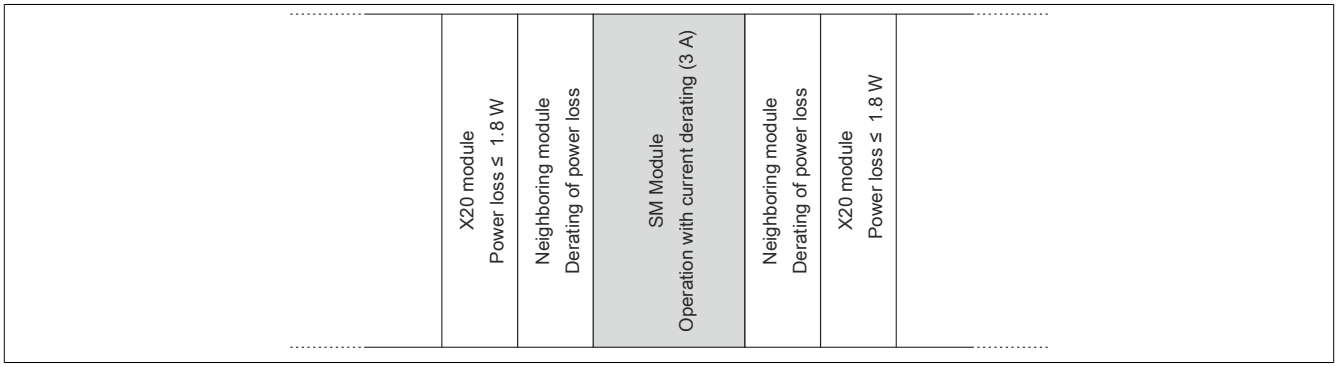


Figure 391: Operating the SM module over the entire temperature range at 3 A rated current

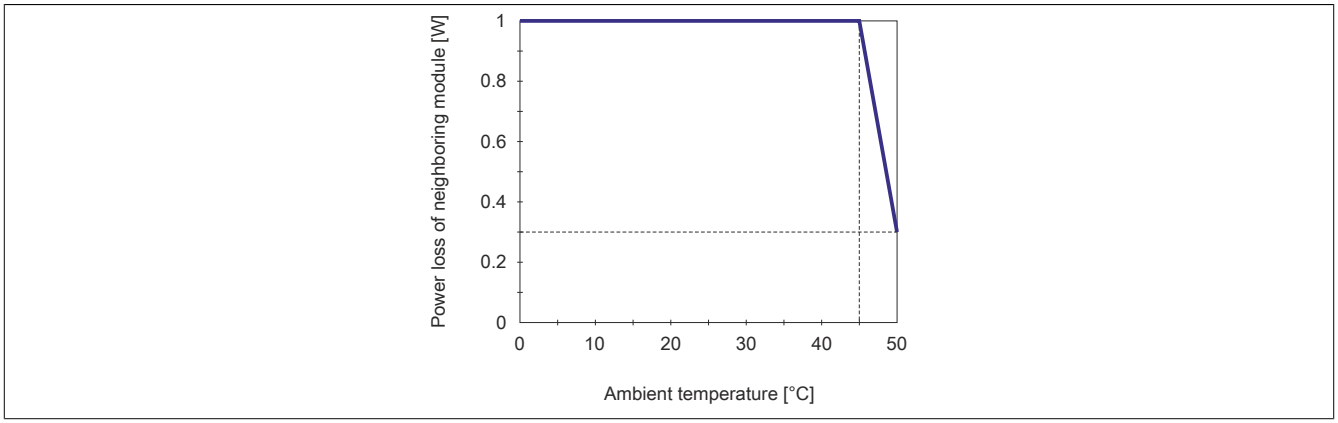


Figure 392: Power loss derating for directly neighboring modules

Current derating of the SM module

If the power loss of the neighboring modules to the SM module is 1 W, then the current of the SM module must be derated starting at 45°C.

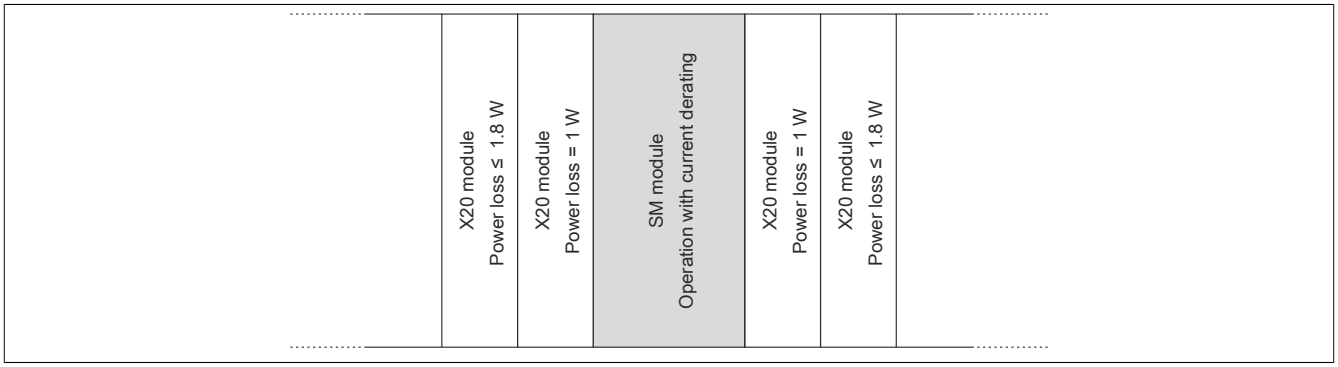


Figure 393: Neighboring modules to the SM module have a power loss of 1 W

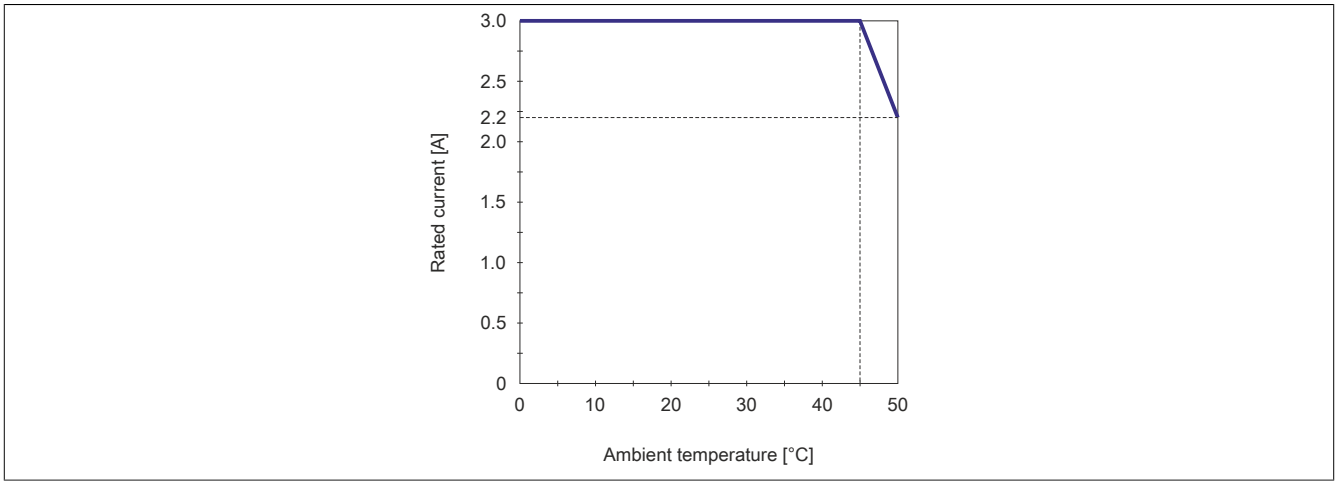


Figure 394: Current derating of the SM module

Hardware configuration for multiple SM modules

If three or more SM modules are operated in a cluster, a dummy module must be inserted between the SM modules. There is no derating in this configuration.

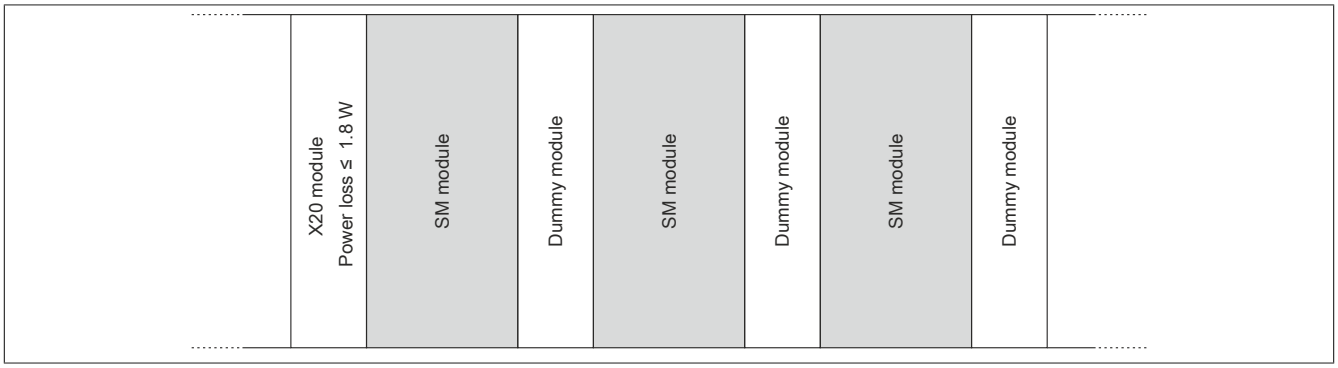


Figure 395: Operating three or more SM modules in a cluster

4.25.7.15 Register description

4.25.7.15.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.25.7.15.2 Function model 0 - Standard without SDC

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
44	Stall threshold	UINT				•
46	Module configuration 1	UINT				•
33	Holding current	USINT				•
34	Nominal current	USINT				•
35	Maximum current	USINT				•
32	Counter configuration	USINT				•
52	Mixed decay threshold	UINT				•
81	Motor ID trigger	USINT				•
84	Full step threshold	UINT				•
92	Minimum speed for stall detection	UINT				•
Reads the configuration						
33	Holding current	USINT		•		
34	Nominal current	USINT		•		
35	Maximum current	USINT		•		
Communication						
6	Position sync/async	UINT		•		
64	Position latched sync/async	INT		•		
12	Motor ID	UINT		•		
Index* 2 + 16	MotorStepN (Index N = 0 to 3)	UINT			•	
0	Position sync/async	INT	•			
86	Position sync 2	INT	•			
4	Input counter state	USINT	•			
	ModulePowerSupplyError	Bit 0				
	StatusInput01	Bit 2				
	StatusInput02	Bit 3				
	StatusInput03	Bit 4				
	StatusInput04	Bit 5				
10	Error status	USINT	•			
	StallError	Bit 0				
	OvertemperatureError	Bit 1				
	CurrentError	Bit 2				
	OvercurrentError	Bit 3				
60	Position latched sync/async	INT	•			
68	usSinceTrigger	UINT	•			
54	Module configuration 2	USINT			•	
	StartLatch	Bit 0				
	TriggerEdgePos	Bit 1				
	TriggerEdgeNeg	Bit 2				
	TriggerEdge	Bit 3				
	StartTrigger	Bit 4				
	ClearError	Bit 5				
72	Stepper latch trigger status	USINT	•			
	LatchInput	Bit 0				
	LatchDone	Bit 1				
	TriggerInput	Bit 4				
74	Measuring motor load	USINT	•			

4.25.7.15.3 Function model 0 - Standard with SDC

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
44	Stall threshold	UINT				●
-	Module configuration 1	UINT				●
33	Holding current	USINT				●
34	Nominal current	USINT				●
35	Maximum current	USINT				●
32	Counter configuration	USINT				●
52	Mixed decay threshold	UINT				●
81	Motor ID trigger	USINT				●
84	Full step threshold	UINT				●
92	Minimum speed for stall detection	UINT				●
102	SDC configuration	USINT				●
103	Motor settling time	USINT				●
107	Turn-off delay	USINT				●
Reads the configuration						
33	Holding current	USINT		●		
34	Nominal current	USINT		●		
35	Maximum current	USINT		●		
Communication						
6	Position sync/async	UINT		●		
12	Motor ID	UINT		●		
112	SDC life sign monitoring	INT			●	
100	Motor current	USINT			●	
	DriveEnable01	Bit 0				
	BoostCurrent01	Bit 1				
	StandstillCurrent01	Bit 2				
74	Measuring motor load	USINT	●			
73	Life cycle counter	SINT	●			
0	Position sync/async	INT	●			
4	Input counter value	USINT	●			
	ModulePowerSupplyError	Bit 0				
	StatusInput01	Bit 2				
	StatusInput02	Bit 3				
	StatusInput03	Bit 4				
	StatusInput04	Bit 5				
10	Error status	USINT	●			
	StallError01	Bit 0				
	OvertemperatureError01	Bit 1				
	CurrentError01	Bit 2				
	OvercurrentError01	Bit 3				
	DrvOk01	Bit 4				
54	Error acknowledgment	USINT		●		
	ClearError01	Bit 5				
16	Motor1Step0	INT		●		
200 204	Home position Home position	INT	●			
212 214	Reference pulse counter Reference pulse counter	SNT	●			
220	Net time of the position value	INT	●			
208	Trigger timestamp	INT	●			
216	Trigger counter	SINT	●			

4.25.7.15.4 Function model 254 - Bus controller and function model 3 - Ramp

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration							
48	-	Holding current	USINT				●
49	-	Nominal current	USINT				●
50	-	Maximum current	USINT				●
72	-	Full step threshold	UINT				●
52	-	Maximum speed	UINT				●
54	-	Maximum acceleration	UINT				●
56	-	Maximum deceleration	UINT				●
58	-	Reversing loop	INT				●
60	-	Fixed position A	DINT				●
64	-	Fixed position B	DINT				●
68	-	Homing speed	UINT				●
74	-	Stall recognition delay	USINT				●
75	-	Jolt time	USINT				●
78	-	Minimum speed for stall detection	UINT				●
70	-	Homing configuration	SINT				●
51	-	Stall detection configuration / Mixed decay	USINT				●
306	-	General configuration	USINT				●
308	-	Limit switch configuration	USINT				●
344	-	Software limit	DINT				●
348	-	Software limit	DINT				●
Reads the configuration							
48	-	Holding current	USINT		●		
49	-	Nominal current	USINT		●		
50	-	Maximum current	USINT		●		
Communication							
0	0	Set position/speed	DINT			●	
4	4	Control word	UINT			●	
6	6	Mode	SINT			●	
0	0	Current position (cyclic)	DINT	●			
4	4	Status word	UINT	●			
6	6	Input status	USINT	●			
84	-	Motor ID	UINT		●		
86	-	Homed zero position	DINT		●		
94	-	Homed zero position	DINT		●		
90	-	Current position (acyclic)	DINT		●		
80	-	Reads the extended control word	UINT		●		
82	-	Read back mode	SINT		●		
98	-	Error code	UINT		●		

1) The offset specifies the position of the register within the CAN object.

4.25.7.15.4.1 Operation with bus controller

The following function model can be used when the SM module is used together with a bus controller.

Bus controller	Function model
X20BC0083, X20BC1083, X20BC8083, X20BC8084	All function models
All others	Function model 254 - Bus controller (identical to Ramp function model)

4.25.7.15.4.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.25.7.15.5 Register description: Standard functional model, shared registers

4.25.7.15.5.1 Configuration registers

Stall threshold

Name:
ConfigOutput01

The SM module features integrated sensorless load measurement for the motor axis. This is especially useful for detecting a "stall condition" (e.g. if the motor moves to the end point during a homing procedure). It cannot be used for torque monitoring during dynamic movements.

With the "stall threshold" register, a threshold can be defined according to the motor load, and the module detects a stall condition started at this threshold (see "Error status").

This threshold value must be determined on a case-by-case basis, since the results of load measurement are influenced by a variety of factors.

- Motor speed: A higher speed results in higher measurement values
- Speeds that cause motor resonances (which interfere with load measurement) are to be avoided
- Motor accelerations that create a dynamic load (and also affect the measurement) should also be avoided
- It is especially important to be aware that mixed decay mode must be optimized for reliable stall detection (see "Mixed decay threshold")

The higher the load measurement value, the lower the load. This means that a stall condition is detected if the load measurement value drops below the trigger threshold for stall detection.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Trigger threshold for stall detection	0	Stall detection is disabled
		1	Minimum sensitivity for stall detection
		2 to 6	Setting the sensitivity of stall detection
		7	Maximum sensitivity for stall detection
3 - 15	Reserved	0	

Mixed decay threshold

Name:
ConfigOutput16

The mixed decay threshold is configured in this register. This value must be adjusted according to the motor being used, current and voltage when using stall detection. Otherwise, the default value 15 will be used.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Mixed Decay Threshold	0	Mixed decay disabled
		1 to 14	Setting for mixed decay threshold
		15	Mixed decay always enabled
4 - 15	Reserved	-	

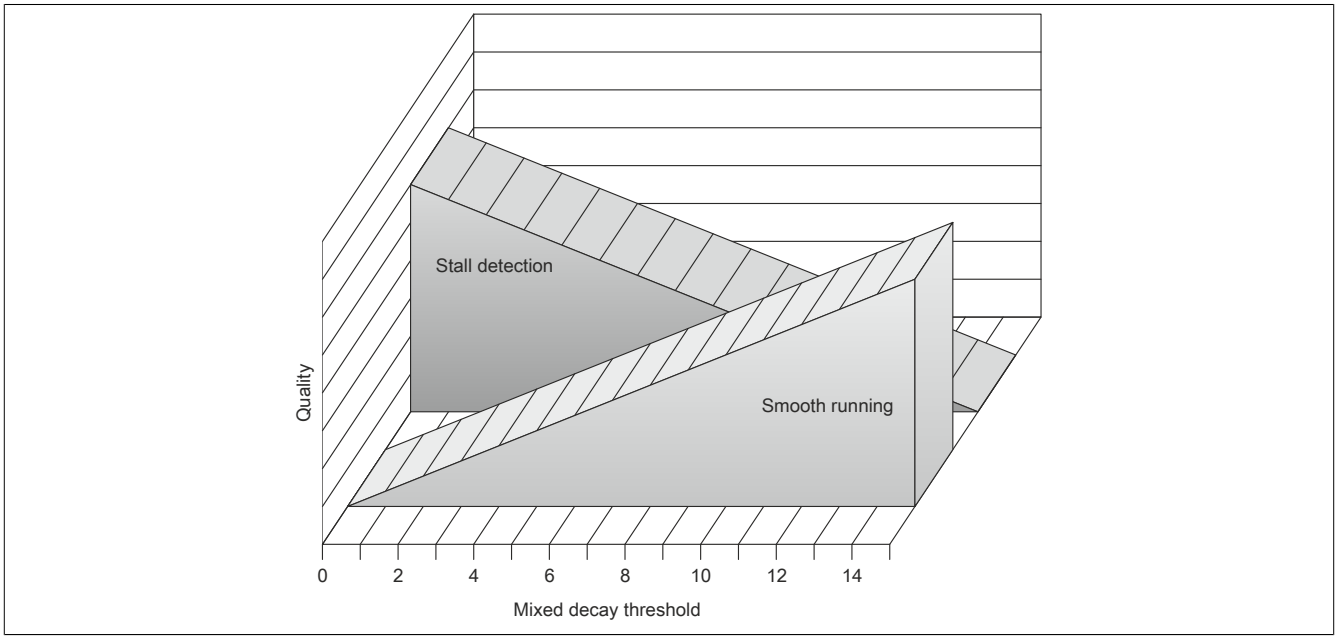
Mixed decay modules provide a greatly optimized sinusoidal current profile in the individual phases of the stepper motor, especially for fast current changes and low current values.

Mixed decay interferes with reliable stall detection, however. For this reason, mixed decay mode can be disabled during stall detection (motor load measurement) using the mixed decay threshold. The smaller the configured mixed decay threshold, the larger the range in which mixed decay is disabled while motor load measurement takes place.

Mixed decay mode is always enabled if the mixed decay threshold is set to 15.

Relationship between stall detection and mixed decay

Depending on the application and the motor used, satisfactorily smooth operation can be achieved while using stall detection by setting the mixed decay threshold to a value between 1 and 14. This is a compromise between smooth operation and stall detection quality and must be fine tuned during commissioning.



Minimum speed for stall detection

Name:
StallDetectMinSpeed01

If the motor speed exceeds the value set in this register, then stall detection is enabled and the configured mixed decay threshold is used. The value 15 is always used for the mixed decay threshold below this threshold value, and no stall error is reported. This means that mixed decay mode is always enabled at low speeds where stall detection principally does not work.

Data type	Value	Information
UINT	0 to 65535	Minimum speed in steps per second.

Full step threshold

Name:
FullStepThreshold01

This register is used to configure a rotational speed. When this defined speed has been reached, the drive will automatically change from microsteps to full step mode. This makes it possible to optimize the torque at higher speeds, while microstep mode ensures optimum concentricity at lower speeds.

It does not make sense to change to full step mode when at a standstill because fine positioning would then no longer be possible. This is why the value "0" does not make sense in the full step threshold register and is interpreted as disabling full step mode (i.e. the motor will always be operated in microstep mode).

Data type	Value	Information
UINT	0	Full step mode disabled
	1 to 65,535	steps/second

Example

Microstep mode should change to full step mode at 500 steps/second. On a motor with 200 steps per revolution, this would be equal to a speed of:

$$T^{-1} = \frac{500\ steps/second}{200\ steps/round} = 2.5\ \frac{rounds}{second} = 150\ \mathrm{min}^{-1}$$

Holding current, rated current and maximum current

Name:
ConfigOutput03 (holding current)
ConfigOutput04 (rated current)
ConfigOutput05 (maximum current)

The holding current, nominal current and maximum current registers are used to configure the desired motor current.

Reasonable values are:

- Holding current < Nominal current < Maximum current

The motor's nominal current is entered in the nominal current register according to the motor's data sheet.

Register	Description
Nominal current	Current during normal operation
Maximum current	Should be selected if a higher motor torque is required briefly during acceleration phases.
Holding current	The holding current should be used in situations when less torque is required (e.g. at a standstill). This reduces the amount of heat generated by the motor.

Switching between preset current values (holding current, rated current, maximum current):

Function model	Switching between preset current values at runtime
Default	Using bits 14 and 15 in the registers Motor StepX
Standard with enabled SDC information	Using the register Motor current

Data type	Value	Unit
USINT	0 to 117	Percent of the module's rated current • 100% corresponds to the rated current of the motor bridge power unit listed in the technical data • 117% corresponds to the maximum current of the motor bridge power unit listed in the technical data

Counter configuration

Name:
ConfigOutput09

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ABR latch function	0	Negative edge: Disable ABR latch function.
		1	Positive edge: Enable latch ABR latch function. After a latch event has occurred, the latch function can be started again with a new rising edge.
1 - 2	Definition of the latch mode	00	Latch ABR counter state unconditionally
		01	Latch ABR counter state at a positive edge on the R input
		10	Latch ABR counter state at a negative edge on the R input
		11	Reserved
3		0	• Position sync: Internal position counter • Position async: ABR counter state • Position latched sync: Internal position counter • Position latched async: ABR counter state
		1	• Position sync: ABR counter state • Position async: Internal position counter • Position latched sync: ABR counter state • Position latched async: Internal position counter
4 - 7	Reserved		

1) These registers are not available in the standard function model with SDC information enabled.

Motor ID trigger

Name:
MotorIdentTrigger

This register can be used to trigger acyclic motor identification (see "Motor ID"). The application must ensure that the conditions for reading the motor ID are fulfilled (see "Notes" under).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0		0	No effect
		1	Rising edge triggers motor identifier measurement
1 - 7	Reserved	0	

4.25.7.15.5.2 Register for reading back the configuration

Read ing the holding current, rated current and maximum current

ConfigOutput03Read (holding current)
ConfigOutput04Read (rated current)
ConfigOutput05Read (maximum current)

These registers are used to read the respective current values in percent.

Register	Description
Nominal current	Current during operation at constant speed
Maximum current	Current during acceleration phases
Holding current	Current when motor is at standstill

Data type	Value	Unit
USINT	0 to 255	Percent of the module's rated current (100% corresponds to the rated current of the motor bridge power unit listed in the technical data)

4.25.7.15.5.3 Communication registers

Measuring motor load

Name:
MotorLoad

This register contains the current measured load value for stall detection. This can be used to tune stall detection.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Motor	0 to 7	Motor load value
3 - 8	Reserved	-	

Module configuration 1

Name:
ConfigOutput02

The number of transfer values and the resolution of microsteps for the drive can be configured in this register.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	The setting for these two bits determines the meaning of bits 2 and 3 in the "Input counter state" register.	x	
1 - 2	Reserved	0	
3 - 4	Number of transfer values per X2X cycle (See "Motor StepX".)	00	1 x Δs / Δt (transfer values: MotorStep0)
		01	2 x Δs / Δt (transfer values: MotorStep0 - MotorStep1
		10	4 x Δs / Δt (transfer values: MotorStep0 - MotorStep3
		11	Reserved
5 - 6	Resolution of microsteps for the following registers: • "Motor StepX" • "Position sync/async"	00	Resolution: 5 bits (bit 0 - 4) microsteps; 8 bits (bit 5 - 13) full steps
		01	Resolution: 6 bits (bit 0 - 5) microsteps; 7 bits (bit 6 - 13) full steps
		10	Resolution: 7 bits (bit 0 - 6) microsteps; 6 bits (bit 7 - 13) full steps
		11	Resolution: 8 bits (bit 0 - 7) microsteps; 5 bits (bit 8 - 13) full steps
7 - 15	Reserved	0	

Position sync/async

Name:
PositionSync
Positionasync

Depending on the Counter configuration, these registers can be used to read either the internal position counter or the counter state of the ABR input.

Data type	Value
INT	-32768 to 32767

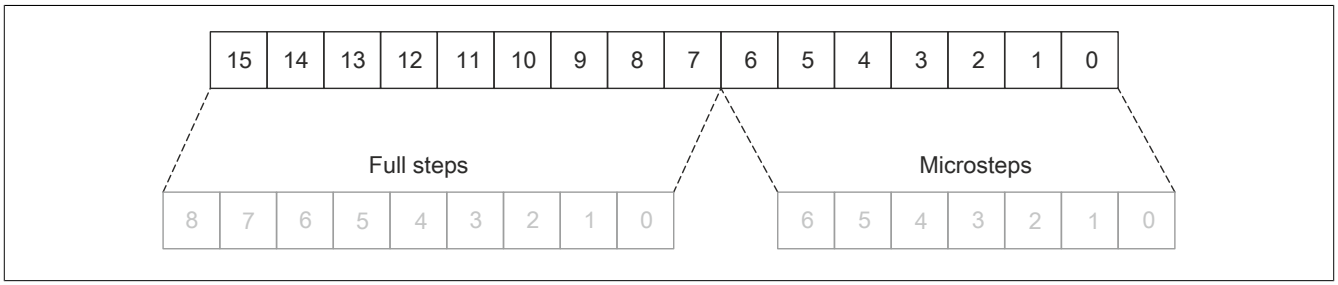
Register	Counter configuration	
	Bit 3 … 0	Bit 3 … 1
Position sync	Internal position counter	ABR counter
Position async	ABR counter	Internal position counter

Internal position counter

The internal position counter is the position calculated by the SM module (set position). This is a cyclic 16-bit counter.

The lowest 5 to 8 bits represent microsteps, while the highest 8 to 11 bits represent full steps (depending on bits 5 and 6 of the register Module configuration 1). In the standard function model with SDC, this value is set to "8-bit microsteps" and can not be changed.

Example of the internal position counter format (7-bit micro steps, i.e. set bit 5 and 6 of the module configuration to binary 10):



ABR counter

This counter is a cyclic 16-bit counter. The relationship between this counter and the internal position counter depends on the resolution of the ABR encoder and the microsteps defined for the internal position counter.

Motor ID

Name:
Motoridentification01

This register is used to identify the connected motor type for service purposes and to differentiate between motors in the application. Following measurement, this register contains the time [µs] needed to apply a current increase of ΔI = 1 A to a motor winding.

This depends on:

- Operating voltage
- The inductance and resistance of the motor winding

Notes		
1)	To achieve reproducible results, the measurement must be made under the following defined conditions:	
	a)	Motor is at standstill
	b)	The motor must be in a half-step position (phase A fully powered, phase B not powered). This means the internal position counter on the SM module must have a value that fulfills the following conditions: • Full steps are divisible by 4 • Microsteps = 0
2)	Condition 1b) is fulfilled after a the SM module is reset or powered on. Immediately afterwards, when the holding current is applied to the motor for the first time (at standstill), the duration for applying the current is measured. This is therefore a suitable time to read the motor identification register in the application.	
3)	The current range from approximately 1/3 of the rated current up to the rated current is used as operating range for determining the motor identifier.	

Data type	Motor ID values	Function
UINT	0	No motor identifier available (after turning on for as long as the measurement conditions are not met)
	1 to 32767	Valid range of values for the motor ID register (in µs)
	65504 to 65519	Ground fault: Motor identification not possible
	65528	Motor ID trigger not possible • Motor has no power applied • Motor in movement • Rated current is set to 0A • Ground fault present
	65529	Invalid value: Underflow
	65530	Overtemperature: Measurement not possible
	65532	Open line: Measurement not possible
	65533	Motor position incorrect: Measurement not possible
	65534	Invalid value: Overrun
	65535	Measurement in progress

Ground fault detection

When the motor is powered on, a ground fault check is performed before motor identification. Error numbers have been added in the motor identification register for the event of a ground fault error (values 65504 to 65519 in the table above).

Error status

Name: The names of the bits are different depending on whether SDC information is enabled or disabled.

Without SDC	With SDC
StallError	StallError01
Overtemperature	Overtemperature01
ErrorCurrentError	ErrorCurrentError01
OvercurrentError	OvercurrentError01
-	DrvOK01

The current error status of the drive is indicated in this register. Each bit indicates a certain error or status. If an error is registered in bits 0 to 3, then the corresponding bit remains set until the error has been acknowledged (see "Module configuration 2" and "Error acknowledgment").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StallError(01)	0	No stall
		1	Stall
1	Overtemperature error OvertemperatureError(01)	0	No overtemperature
		1	Overtemperature
2	Current error CurrentError(01)	0	No current error
		1	Current error
3	Overcurrent error OvercurrentError(01)	0	No overcurrent
		1	Overcurrent
4	Status of the drive DrvOk0[1)]	0	An error was triggered for the motor axis
		1	The drive is running error-free
5 - 15	Reserved	0	

1) Only when SDC information is enabled

Overtemperature error

The "Overtemperature" error bit can be set for the following reasons:

- A specific temperature was exceeded near the channel due to overload
- Module temperature exceeds 85°C

Current error

This error bit occurs whenever the required current cannot be supplied to the motor windings. This can be (but is not necessarily) caused by an open line. At higher speeds (depending on the motor), this error can also occur without an open line. In this case it is simply no longer possible to supply the desired current to the motor windings. Because of the Back-EMF on the motor, this bit is set at slightly lower speeds if the motor is operated with no load compared with full or partial loads.

Overcurrent error

Overcurrent occurs if the motor current measured in the motor windings is twice as high as it should be (e.g. short circuit).

Status of the drive

The status of the drive is only shown when SDC information is enabled. The drive bit is 1 when the following conditions are met:

- Motor turned on (see "Motor current")
- Ground fault detection is completed and OK
- MotorID measurement is completed
- Motor is supplied with current
- Motor settling time has passed
- Supply voltage is in the valid range
- No overtemperature fault
- Preset position value is valid (see "SDC life sign monitoring")

4.25.7.15.6 Register description: Standard functional model without SDC information

4.25.7.15.6.1 Communication registers

Input counter state

Name:
ModulePowerSupplyError
StatusInput01 to StatusInput04

This register is used to indicate the status of the digital inputs and counters.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ModulePowerSupplyError	0	OK
		1	Module supply error
1	Reserved	0	
2	StatusInput01	**When bit 0 in Module configuration 1 = 0**	
		0 or 1	Input state - Digital input 1
		When bit 0 in Module configuration 1 = 1	
		x	Ref toggle bit for counter 1: The state of this bit is changed after the homing procedure is complete.
3	StatusInput02	**When bit 0 in Module configuration 1 = 0**	
		0 or 1	Input state - Digital input 2
		When bit 0 in Module configuration 1 = 1	
		0	Homing of ABR counter active
		1	Homing of ABR counter complete
4	StatusInput03	0 or 1	Input state - Digital input 3
5	StatusInput04	0 or 1	Input state - Digital input 4
6 - 7	Reserved	0	

Motor StepX

Name:
MotorStep0 to MotorStep3

These registers are used to specify the number and direction of steps that must be carried out by the module during the next X2X cycle, and to select the motor current (see also "Holding current, rated current and maximum current").

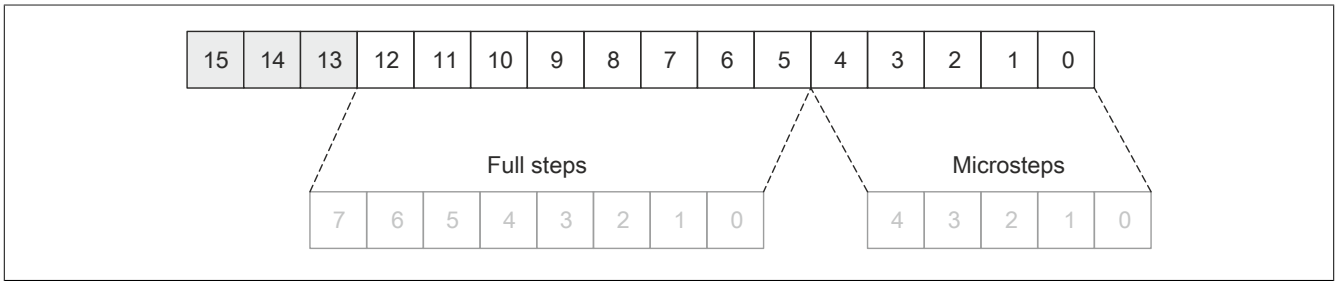
Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 12	Number of steps for the module to move during the next X2X cycle	x	
13	Direction of movement	0	Positive
		1	Negative
14 - 15	Selection of motor current	00	Motor not powered
		01	Holding current
		10	Rated current
		11	Maximum current

Depending on the required resolution and maximum configurable speed, "Module configuration 1" can be used to specify which bit position is used as the 1's position for full steps (see bits 5 and 6 of Module configuration 1).

Example for 5-bit microsteps (set bits 5 and 6 of the module configuration to binary 00):



The number of transfer values per X2X cycle is specified by bits 3 and 4 in "Module configuration 1" (see "Module configuration 1"). If only one transfer value (bits 3 and 4 = 00) is specified, then the motor is advanced by MotorStep0 until the next X2X cycle. If 2 or 4 transfer values are specified, then the X2X cycle is divided accordingly.

Example: X2X cycle = 1 ms (1000 µs)

Time	Number of transfer values (see Module configuration 1)		
	1 (bits 3 - 4 = 00)	2 (bits 3 - 4 = 01)	4 (bits 3 - 4 = 10)
0 - 250 µs)	MotorStep0	MotorStep0	MotorStep0
250 - 500 µs)			MotorStep1
500 - 750 µs)		MotorStep1	MotorStep2
750 - 1000 µs)			MotorStep3

Position latched sync/async

Name:
PositionLatchedSync
PositionLatchedASync

The position counter (internal position counter or ABR counter) is applied at the latch event (see "Module configuration 2"). Bits 3 and 7 of the Counter configuration register are used to determine which counter state (internal position counter or ABR encoder) should be saved in the registers "Position latched sync" and "Position latched async".

Data type	Value
INT	-32768 to 32767

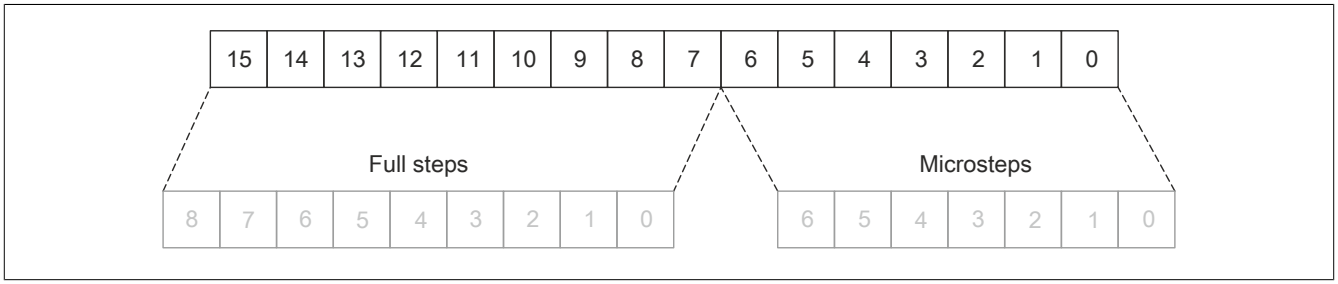
Register	Counter configuration	
	Bit 3 … 0	Bit 3 … 1
Position sync	Internal position counter	ABR counter
Position async	ABR counter	Internal position counter

Internal position counter

The internal position counter is the position calculated by the SM module (set position). This is a cyclic 16-bit counter.

The lowest 5 to 8 bits represent microsteps, while the highest 8 to 11 bits represent full steps (depending on bits 5 and 6 of the register Module configuration 1).

Example of the internal position counter format (7-bit micro steps, i.e. set bit 5 and 6 of the module configuration to binary 10):



ABR counter

This counter is a cyclic 16-bit counter. The relationship between this counter and the internal position counter depends on the resolution of the ABR encoder and the microsteps defined for the internal position counter.

usSinceTrigger

Name:
usSinceTrigger

This register indicates the time (in µs) that has passed since the trigger event occurred (see "Module configuration 2").

Data type	Value
UINT	0 to 65535

Stepper latch trigger status

Name:
LatchInput
LatchDone
TriggerInput

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Latch input:	x	Digital input for the latch event (level)
1	LatchDone	x	State changes each time the counter state is successfully latched (reset value = 0)
2 - 3	Reserved	-	
4	TriggerInput	x	Trigger input (level)
5 - 7	Reserved	0	

4.25.7.15.6.2 Configuration registers

Module configuration 2

Name:
StartLatch
TriggerEdgePos
TriggerEdgeNeg
StartTrigger
TriggerEdge
ClearError

The trigger functions for the stepper motor can be configured with this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Latch function for stepper motor Latch byte	0	The latch function for stepper motor position is deactivated at the negative edge of this bit
		1	The latch function for stepper motor position is deactivated at the positive edge of this bit
1 - 2	Latch mode for stepper motor TriggerEdgePos (Bit 1) TriggerEdgeNeg (Bit 2)	00	Latch position of stepper motor, unconditional
		01	Latch position of stepper motor at positive edge on input DI 3
		10	Latch position of stepper motor at negative edge on input DI 3
		11	Reserved
3	TriggerEdge	0	Trigger edge (input DI 4) = positive
		1	Trigger edge (input DI 4) = negative
4	Enable trigger (when changes occur) StartTrigger	x	
5	ClearError	0	No effect
		1	Error acknowledgment for the motor (for more info, see "Error status")
6 - 7	Reserved	-	

Trigger function procedure:

- Select the desired trigger edge using bit 3
- Enable the trigger function by changing the state of bit 4. When this bit changes, usSinceTrigger (µs counter) is cleared.
- When the trigger event occurs, usSinceTrigger (µs counter) is started.
- The usSinceTrigger counter cannot overrun, i.e. it is stopped at 2^{16} and retains this value until the next time the trigger function is activated.

The trigger function can be re-activated at any time by changing the state of bit 4, regardless of whether a trigger event has occurred or if usSinceTrigger has reached the maximum value.

Position sync 2

Name:
PositionSync02

Depending on Counter configuration (bit 3), this register contains the state of either the position counter or the ABR counter. It's an exact complement to the Position sync register.

If the position sync register contains the position counter, then the PositionSync02 register contains the ABR counter state and vice versa.

By default, the register cannot be seen in the I/O map; instead, it has to first be activated in the I/O configuration.

Data type	Value
INT	-32768 to 32767

4.25.7.15.7 Register description: Standard functional model with SDC information

4.25.7.15.7.1 Configuration registers

SDC configuration

Name:
SDCConfig01

This register can be used to enable/disable additional SDC information.

The additional cyclic registers are hidden or shown depending on whether SDC information is disabled or enabled. It is comparable to the two variants of the standard function model with and without SDC information.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Trigger edge	0	Rising trigger edge
		1	Falling trigger edge
1 - 5	Reserved	0	
6	SDC life sign monitoring	0	Disabled
		1	Enabled
7	SDC information[1)]	0	Disabled
		1	Enabled

1) When the "SDC information" bit is enabled, the "EncOK01" bit is shown in the Automation Studio I/O mapping. This bit is linked to the ModulOK bit and always indicates its value.

Note:

Neither SDC information nor SDC life sign monitoring is permitted to be changed at runtime.

Module configuration 1 with SDC

The Module configuration 1 register is ignored in the standard function model with SDC information enabled. The module behaves as if the module configuration were described as follows:

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Meaning of bits 2 and 3 in the register "Input counter value"		
1 - 2	Reserved	0	
3 - 4	Number of transfer values per X2X cycle	00	1x Δs / Δt (transfer values: Motor settings Motor1Step0)
5 - 6	Resolution of microsteps	11	8-bit microsteps
7 - 15	Reserved	0	

Motor settling time

Name:
MotorSettlingTime01

This register determines the motor setting time. The motor settling time determines the minimum time between when the motor is powered on to when the DrvOk bit is set (see "Error status"). The setting is made in steps of 10 ms.

Data type	Value	Information
USINT	1 to 255	10 ms to 2.55 s, default: 10 ms

Turn-off delay

Name:
DelayedCurrentSwitchOff01

When the SDC life sign monitoring is triggered (i.e. the net time timestamp is in the past) the motor is decelerated at nominal current with speed setpoint = 0.

Then the motor is switched off after the delay configured with this register.

Data type	Value	Information
USINT	0 to 255	0 to 25.5 ms in steps of 100 ms (default: 100 ms)

4.25.7.15.7.2 Communication registers

SDC life sign monitoring

Name:
SetTime01

The module uses SDC life sign monitoring to check whether valid values have been received for the speed setpoint. SDC life sign monitoring is activated in the SDC configuration register by setting bit 6 (SDCSetTime = on).

If the specified NetTime timestamp is in the past, then an error is triggered for the motor axis (only when the motor is switched on). The module performs the following steps:

1) The CPU is informed of the error using the Drive bit (DrvOk) = 0

2) Braking at configured rated current with speed setpoint = 0

3) Wait for configured turn-off delay to expire

4) Power off motor

When the timestamp is back in the valid range, the motor can be powered on again by a rising edge on the DriveEnable bit (see "Motor current").

Data type	Value
INT	-32768 to 32767

Motor current

Name:
DriveEnable01
BoostCurrent01
StandstillCurrent01

Bits 0 to 2 of this register can be used to control the motor's current supply.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DriveEnable01	x	Motor powered
1	BoostCurrent01	x	Maximum current
2	StandstillCurrent01	x	Holding current
3 - 7	Reserved	0	

The possible status of bits 0 to 2

StandstillCurrent01	BoostCurrent01	DriveEnable01	Description
x	x	0	Motor not supplied with current
0	0	1	Rated current supplied to motor
0	1	1	Maximum current supplied to motor
1	0	1	Holding current supplied to motor
1	1	1	Holding current supplied to motor

Life cycle counter

Name:
LifeCnt

This register is incremented by one with each X2X Link cycle.

Data type	Value
SINT	-128 to 127

Input counter value

Name:
ModulePowerSupplyError
StatusInput01 to StatusInput04

This register is used to indicate the status of the digital inputs and the counter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ModulePowerSupplyError	0	OK
		1	Module supply error
1	Reserved	0	
2	StatusInput01	0 or 1	Input state - Digital input 1
...		...	
5	StatusInput04	0 or 1	Input state - Digital input 4
6 - 7	Reserved	0	

Error acknowledgment

Name:
ClearError01

This register can be used to acknowledge errors that have occurred on the motor.

For more info, see "Error status".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 4	Reserved	0	
5	ClearError01	0	No effect
		1	Error acknowledgment for motor
6 - 7	Reserved	0	

Motor1Step0

Name:
Motor1Step0

This registers is used to specify the number and direction of steps that should be carried out by the module during the next X2X cycle.

The value is specified with a resolution of 1/256 of a full step (corresponds to 8-bit microsteps).

The direction of movement is derived from the value's sign:

Data type	Value	Information
INT	>0	Movement in positive direction in 1/256 full steps
	<0	Movement in negative direction in 1/256 full steps

Unlike the standard function model without enabled SDC information, the motor current is selected using a separate register (see Motor current).

Home position

Name:
RefPulsePos01

These 2 registers contain the following:

Register	Description
Home position of the internal position counter	This register indicates the home position of the internal position counter.
Home position for the ABR counter	This register indicates the home position of the ABR counter.

Data type	Value
INT	-32768 to 32767

The "Position Sync" setting in the Automation Studio I/O configuration can be used to select which of the two registers is be addressed by the variable RefPulsePos01.

Variables in Automation Studio	I/O configuration, Counter 01, "Position Sync" option	
	Stepper counter 01 shown at ActPos01	ABR counter 01 shown at ActPos01
RefPulsePos01	Home position of internal position counter	Home position of ABR counter
The "Position Sync" option also sets bit 3 in the Counter configuration register for Counter 1:		
Bit 3 (counter 1)	0	1

Reference pulse counter

Name:
RefPulseCnt01

These 2 registers contain the following:

Register	Description
Reference pulse counter for the internal position counter	The reference pulses of the internal position counter are counted in this register.
Reference pulse counter for the ABR counter	The reference pulses of the ABR counter are counted in this register.

Data type	Value
SINT	-128 to 127

The "Position Sync" setting in the Automation Studio I/O configuration can be used to select which of the two registers is addressed by the variable RefPulseCnt01.

Variables in Automation Studio	I/O configuration, Counter 01, "Position Sync" option	
	Stepper counter 01 shown at ActPos01	ABR counter 01 shown at ActPos01
RefPulseCnt01	Reference pulse counter for internal position counter	Reference pulse counter of ABR counter
The "Position Sync" option also sets bit 3 in the Counter configuration register for Counter 1:		
Bit 3 (counter 1)	0	1

Net time of the position value

Name:
ActTime01

This register contains the net time of the most recent valid position value.

Data type	Value
INT	-32768 to 32767

Trigger counter

Name:
TriggerCnt01

This register contains a cyclic counter that is incremented with each trigger event.

Data type	Value
SINT	-128 to 127

Trigger timestamp

Name:
TriggerTime01

This register indicates the point in time (net time) of the most recent trigger event. The trigger edge must be configured in the "SDC configuration" register.

Data type	Value
INT	-32768 to 32767

4.25.7.15.8 Register description: Function model 254 - Bus controller and function model 3 - Ramp

4.25.7.15.8.1 Configuration registers

Holding current, rated current and maximum current

Name:
ConfigOutput03a (holding current)
ConfigOutput04a (rated current)
ConfigOutput05a (maximum current)

The holding current, nominal current and maximum current registers are used to configure the desired motor current.

Reasonable values are:

- Holding current < Nominal current < Maximum current

The motor's nominal current is entered in the nominal current register according to the motor's data sheet.

Register	Description
Nominal current	Current during operation at constant speed
Maximum current	Current during acceleration phases. In the mode "Homing during stall", the rated current is always used instead of the maximum current, even in acceleration phases.
Holding current	Current when motor is at standstill

When the current changes to a weaker value (e.g. when transitioning from the acceleration phase to the constant speed mode), the stronger current is maintained for an additional 100 ms. This is done according to the following priority regardless of the actual defined values: maximum current before nominal current before holding current.

Data type	Value	Unit
USINT	0 to 117	Percent of the module's rated current • 100% corresponds to the rated current of the motor bridge power unit listed in the technical data • 117% corresponds to the maximum current of the motor bridge power unit listed in the technical data

Full step threshold

Name:
FullStepThreshold01

This register defines the threshold speed, above which the motor is operated in full step mode, and below which it is operated in microstep mode.

Data type	Value	Information
UINT	1 to 65534	Speed in microsteps / cycle
	65535	Motor is always operated in microstep mode

Maximum speed

Name:
MaxSpeed01pos

This register defines the maximum speed for the absolute positioning modes (1, -123, -124, -125, -126).

Information:

The setting does not apply to the speed and homing modes (2, -127, -128).

Data type	Value	Information
UNIT	0 to 65,535	Speed in microsteps / cycle

Maximum acceleration

Name:
MaxAcc01

This register defines the maximum acceleration (also applies for homing modes).

Data type	Value	Information
UINT	0 to 65,535	Acceleration in microsteps / cycle²

Maximum deceleration

Name:
MaxDec01

This register defines the maximum deceleration (also applies for homing modes).

Data type	Value	Information
UINT	0 to 65,535	Deceleration in microsteps / cycle²

Reversing loop

Name:
RevLoop01

This parameter is only used in mode 1, -123, -124, -125, -126 (absolute positioning modes).

If the value for the reversing loop is not equal to 0, the position setpoint is approached directly when coming from one direction; when coming from the other direction, the position setpoint is initially exceeded by the configured number of steps before finally moving to the position setpoint. This ensures that the position setpoint is always approached from the same direction (to avoid mechanical backlash).

The sign of the defined value determines the direction in which the reversing loop runs.

Sign	Effective direction
Positive	Reversing loop in positive direction of movement
Negative	Reversing loop in negative direction of movement

Data type	Value
INT	-32768 to 32767

Fixed position A

Name:
FixedPos01a

This register defines the position to move to in modes -124 (when 1 is set at the digital input) and -125.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Fixed position B

Name:
FixedPos01b

This register defines the position to move to in modes -124 (when 0 is set at the digital input) and -126.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Homing speed

Name:
RefSpeed01

This register sets the speed for homing modes -127 and -128.

Data type	Value	Information
UINT	0 to 65,535	Speed in microsteps / cycle

Stall recognition delay

Name:
StallRecognitionDelay01

The value in this register is only relevant for "Homing during stall".

A stall is only detected after the time specified here has expired and after the homing procedure has started.

For example, a setting of 4 (and a cycle time of 25 ms) means that a stall will not be detected until 100 ms after the motor starts moving (start of the homing procedure).

Set to 0 to eliminate delay.

Data type	Value	Information
USINT	0 to 255	in cycles, see "General configuration"

Minimum speed for stall detection

Name:
StallDetectMinSpeed01

If the motor speed exceeds the value set in this register, then stall detection is enabled and the configured mixed decay threshold is used. The value 15 is always used for the mixed decay threshold below this threshold value, and no stall error is reported. This means that mixed decay mode is always enabled at low speeds where stall detection principally does not work.

Data type	Value	Information
UINT	0 to 65535	Minimum speed in microsteps per cycle.

Jolt time

Name:
JoltTime01

If a value other than 0 is assigned to this register, then jolt limitation is performed. This is done by averaging the values for the steps to be carried out (speed setpoint) in each cycle using FIFO memory. The jolt time corresponds to the number of FIFO elements (0 to 80). If a value greater than 80 is entered, then it will be limited internally to 80.

Changes made while a motor is running will be applied as soon as ...

- the motor has reached the position setpoint (positioning modes only)
- the motor has stopped (all modes)

Data type	Value	Information
USINT	0	No jolt time limitation
	1 to 80[1)]	Number of FIFO elements

1) Starting with upgrade 1.3.1.0 (firmware version 16); For older versions: 16

Homing configuration

Name:
RefConfig01

The homing mode can be set with this register.

Data type	Value	Information
SINT	-120	Set home position
	-121	Homing at positive edge on input DI 4
	-122	Homing at negative edge on input DI 4
	-125	Homing at positive edge on input DI 3 (R pulse)
	-126	Homing at negative edge on input DI 3 (R pulse)
	-127	Homing during stall detection
	-128	Immediate homing
	Everything else	No effect

Stall detection configuration / Mixed decay

Name:
StallDetectConfig01

The mixed decay threshold and stall detection sensitivity can be configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Mixed decay threshold	0	Mixed decay disabled
		1 to 14	Setting for mixed decay threshold
		15	Mixed decay always enabled
4 - 6	Stall threshold	0	Stall detection is disabled
		1 to 6	Steps involved in setting stall detection sensitivity
		7	Maximum sensitivity for stall detection
7	Motor load	0	Motor load value not shown
		1	Show value in register Status word[1)]

1) If this bit is 1, then the motor load value is shown in bits 13 to 15 of the status word register (otherwise these bits are 0). This value can help when testing the stall detection and the Home during stall mode.

Stall threshold

The SM module features integrated sensorless load measurement for the motor axis. This is especially useful for detecting a "stall condition" (e.g. if the motor moves to the end point during a homing procedure). It cannot be used for torque monitoring during dynamic movements.

The "stall threshold" (bits 4 to 6 of this register) can be used to define a threshold value for each axis individually according to the motor load, beyond which the motor will detect a stall condition.

This threshold value must be determined on a case-by-case basis, since the results of load measurement are influenced by a variety of factors.

- Motor speed: A higher speed results in higher measurement values
- Speeds that cause motor resonances (which interfere with load measurement) are to be avoided
- Motor accelerations that create a dynamic load (and also affect the measurement) should also be avoided
- It is especially important to be aware that mixed decay mode must be optimized for reliable stall detection.

The higher the load measurement value, the lower the load. This means that a stall condition is detected if the load measurement value drops below the trigger threshold for stall detection.

Mixed decay threshold

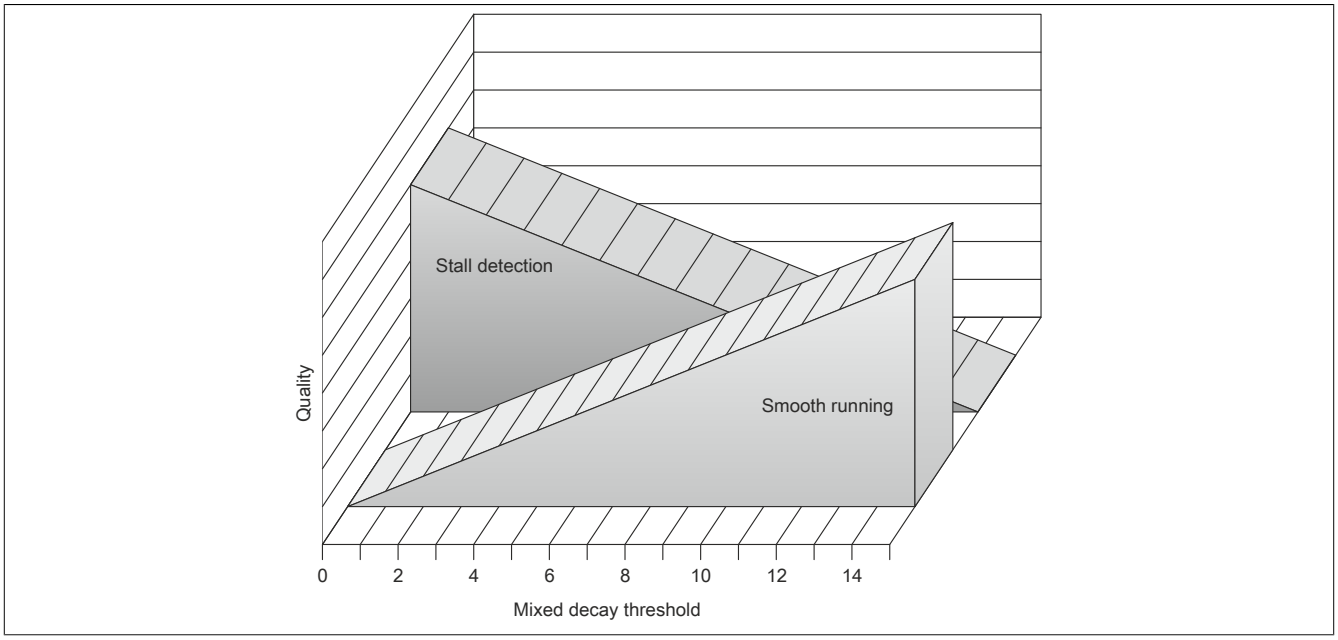
Mixed decay modules provide a greatly optimized sinusoidal current profile in the individual phases of the stepper motor, especially for fast current changes and low current values.

Mixed decay interferes with reliable stall detection, however. For this reason, mixed decay mode can be disabled during stall detection (motor load measurement) using the mixed decay threshold. The smaller the configured mixed decay threshold, the larger the range in which mixed decay is disabled while motor load measurement takes place.

Mixed decay mode is always enabled if the mixed decay threshold is set to 15.

Relationship between stall detection and mixed decay

Depending on the application and the motor used, satisfactorily smooth operation can be achieved while using stall detection by setting the mixed decay threshold to a value between 1 and 14. This is a compromise between smooth operation and stall detection quality and must be fine tuned during commissioning.



General configuration

Name:
GeneralConfig01

Bit 0 of this register can be used to switch the positioning mode. This register can also be used to configure the cycle time of the motion profile generator.

- 0: "Mode 1: Position mode" without extended control word
- 1: "Mode 1: Position mode with extended control word"

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Position mode	0	Without extended control word
		1	With extended control word
1 - 2	Cycle time of the motion profile generator[1)]	00	25 ms
		01	10 ms
		10	5 ms
		11	Reserved
3 - 7	Reserved	0	

1) This parameter is supported starting with upgrade 1.3.1.0 (firmware version 16).

Limit switch configuration

Name:
LimitSwitchConfig01

This register can be used to configure the behavior of the limit switch.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Negative limit switch	00	Off
		01	Active if low
		10	Reserved
		11	Active if high
2 - 3	Positive limit switch	00	Off
		01	Active if low
		10	Reserved
		11	Active if high
4 - 6	Reserved	0	
7	Direction monitoring	0	Off (default)
		1	On

Negative/positive limit switch

When one of the limit switches is reached, a warning is triggered and the speed is decelerated to 0. The "Device Control State Machine" state is not changed. This keeps current flowing to the motor.

The error that occurred can be read from the Error code register. Normal operation can be resumed by acknowledging the warning. This will not restrict motor movement to a specific direction and the limit switch will not be triggered until the next active edge.

Exceeding the limit switch while braking

The limit switches are not linked with the corresponding direction of movement. If the limit switch is exceeded, another error will be triggered when reversing after acknowledging the initial error.

Direction monitoring

If this function is enabled, then the two limit switches will be linked with the respective direction of movement. This means that the negative limit switch is only triggered in the negative direction and the positive limit switch only in the positive direction of movement (specified direction).

This prevents specifying a movement in the wrong direction when direction monitoring is enabled and limit switches are active.

Warning!

If the motor is wired incorrectly with this configuration (wrong direction of movement), then the limit switch will not be triggered and the actual correct direction of movement will be denied. This will also be the case when the limit switch connections are reversed.

Software limit

Name:
PositionLimitMin01
PositionLimitMax01

This register configures software limits. The function is active if at least one of the two registers is unequal to zero.

These limits are effective in all positioning modes. Position overrun is not possible when this function is enabled. Movement is always contained within the two limits.

If a position is specified that violates the minimum/maximum software limit, the "Internal limit active" bit will be set in the Status word register. The motor movement will be stopped until a position is specified within the limits.

The "Internal limit active" bit will also be set in the "Status word" register if there is a configuration error (minimum > maximum).

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Information:

The software limits will only be monitored in connection with the following CANopen bus controllers:

- **X20BC0043-10**
- **X20BC0143-10**
- **X67BC4321-10**
- **X67BC4321.L08-10**
- **X67BC4321.L12-10**

4.25.7.15.8.2 Reading back the configuration

Read ing the holding current, rated current and maximum current

ConfigOutput03aRead (holding current)
ConfigOutput04aRead (rated current)
ConfigOutput05aRead (maximum current)

These registers are used to read the respective current values in percent.

Register	Description
Nominal current	Current during operation at constant speed
Maximum current	Current during acceleration phases
Holding current	Current when motor is at standstill

Data type	Value	Unit
USINT	0 to 255	Percent of the module's rated current (100% corresponds to the rated current of the motor bridge power unit listed in the technical data)

4.25.7.15.8.3 Communication registers

Set position/speed

Name:
AbsPos01

This register is used to set position or speed, depending on the operating mode.

- Position mode (see "Mode"): Cyclic setting of the position setpoint in microsteps. In this mode, one micro-step is always 1/256 full-step.
- Speed mode (see "Mode"): In this mode, this register is used as a signed speed setpoint.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Control word

Name:
MpGenControl01

This register can be used to issue commands based on the module's state (see 4.25.7.15.8.4 "Ramp function model operation").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Switch on	x	
1	Enable voltage	x	
2	Quick stop	x	
3	Enable operation	x	
4 - 6	Mode-specific	x	
7	Fault reset	x	
8	stop[1)]	x	
9 - 10	Reserved	0	
11	Motor ID trigger	0	No effect
		1	Rising edge: Motor ID trigger[2)]
12	Warning reset	0	No effect
		1	Rising edge: Reset warnings
13	Undercurrent detection	0	Disable current error detection (default)
		1	Enable current error detection
14	ABR counter sync/async	0	Default: • Internal position counter, cyclic • ABR counter, non-cyclic
		1	• Internal position counter, non-cyclic • ABR counter, cyclic
15	Stall detection	0	Disable stall detection (default)
		1	Enable stall detection

1) The "Halt" bit is only evaluated when the extended control word is enabled (see "General configuration").
2) This bit can be used to trigger a measurement of the motor ID. Keep in mind that the application must ensure that the conditions for measurement are fulfilled (see table in the "Motor ID" register).

Mode

Name:
MpGenMode01

Data type	Value	Information
SINT	0	No mode selected
	1	Depending on bit 0 in the General configuration register, the position mode will behave as follows: • Position mode without extended control word: Move to position setpoint as soon as position setpoint is changed • Position mode with extended control word: Move to position setpoint as described in "Mode 1 - Position mode with extended control word"
	2	Speed mode: Constant speed
	-120	Set home position
	-121	Remaining distance mode
	-122	Set the actual position
	-123	Move to position setpoint when external input is set
	-124	Two-position module
	-125	Move to fixed position A (position set asynchronously)
	-126	Move to fixed position B (position set asynchronously)
	-127	Positive homing (see also "Homing configuration")
	-128	Negative homing (see also "Homing configuration")

Information:

For all modes: The "Target reached" bit is set in the Status word register when the current action is finished (i.e. when the position or speed is reached, depending on the mode).

A new position or speed can be specified even before the current action is finished.

Mode 1 - Position mode

The position setpoint is specified in the Set position/speed register. The motor is then moved to this new position. This is done with a ramp function that accounts for the defined maximum speed and acceleration values.

The position setpoint can also be changed during an active positioning procedure.

The position setpoint is specified in microsteps (1/256 of a full step).

If bit 0 in the General configuration register is 0 (no extended control word), then the position setpoint will be applied as soon as it is different from the current position. The new position is then moved to.

However, if bit 0 in the General configuration register is set to 1 (extended control word), then the position setpoint will be applied as described under "Mode 1 - Position mode with extended control word".

Mode 1 - Position mode with extended control word

The position mode with extended control word behaves like the previously described Position mode 1 (without extended control word) except that the new position setpoint (Position/speed register) is applied according to the extended control word.

Extended control word

This register can be used to issue commands based on the module's state (see 4.25.7.15.8.4 "Ramp function model operation").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Corresponds to the defaultControl word	x	
4	New setpoint	0	Do not apply position setpoint
		1	Apply position setpoint
5	Change set immediately	0	Complete current positioning movement and then start next positioning movement
		1	Interrupt current positioning movement and then start next positioning movement
6	abs / rel	0	Position setpoint is an absolute value
		1	Position setpoint is a relative value
7	Corresponds to the defaultControl word	x	
8	Halt[1)]	0	Execute positioning
		1	Stop axis with deceleration
9 - 15	Corresponds to the defaultControl word	x	

1) This bit applies to all modes.

Extended status word

The bits in the status word reflect the status of the state machine (for a detailed description, see "Status word" and "State machine").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 9	Corresponds to the defaultStatus word	x	
10	Target reached, depending on bit 8 (Halt) in the register Control word		**If Halt = 0**
		0	Position setpoint not reached
		1	Position setpoint reached
			If Halt = 1
		0	Axis decelerating
		1	Axis speed = 0
11	Corresponds to the defaultStatus word	x	
12	Setpoint acknowledge	0	Ramp generator did not apply the position value
		1	Ramp generator applied the position value
13 - 15	Corresponds to the defaultStatus word	x	

Position setting

The position setpoint can be defined in two different ways:

Type of setpoint definition	Description
Single setpoint	Once the position setpoint is reached, the *Target reached* bit in the Status word register is set. Then a new position setpoint is defined. The drive stops at each position setpoint before starting the movement to the next position setpoint.
Set of setpoints	Once a setpoint has been reached, the movement to the next setpoint is started immediately without stopping the drive. It is therefore not possible to initiate a new positioning movement by transferring a new position setpoint during an active positioning movement.

Table 578: Types of position setpoint definition

The two modes "Single setpoint" and "Set of setpoints" are controlled by the timing of the bits *New setpoint* and *Change set immediately* in the *extended control word* and *Setpoint acknowledge* in the *Extended control word* register.

These bits can be used to create a Request-Response mechanism. This makes it possible to specify a position setpoint while previous setpoint is still being processed.

Transferring the position setpoint

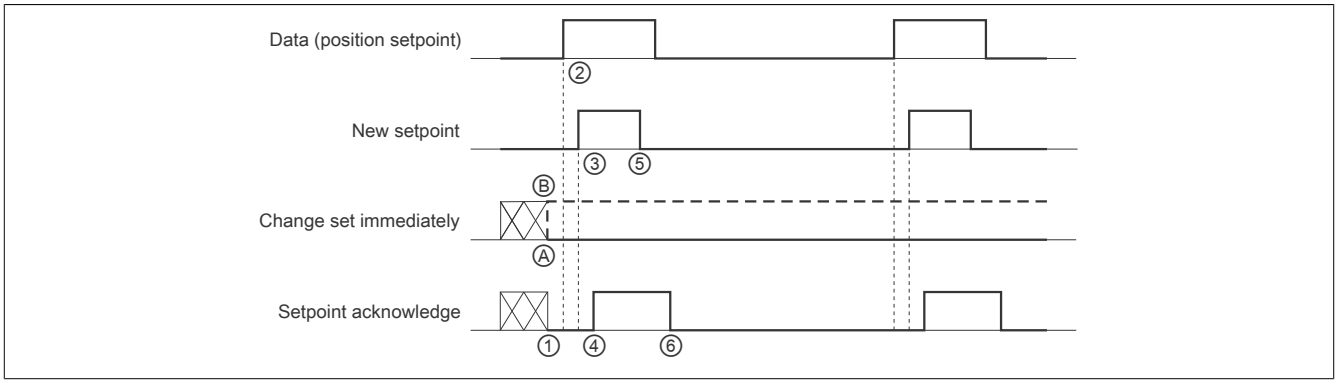


Figure 396: Principle for applying the setpoint

Transferring a new setpoint:

1. When the *Setpoint acknowledge* bit in the Extended status word register is 0, the module will accept a new position setpoint.
2. The new position setpoint is specified in the *Set position/speed*.
3. A rising edge of the *New setpoint* bit in the Extended control word register signalizes that the new position setpoint in the *Set position/speed* register is valid and can be used for the next positioning movement.
4. Once the module has received and saved the new position setpoint, the *Setpoint acknowledge* bit in the *Status word* register is set to 1.
5. Now the controller can reset the *New setpoint* bit to 0.
6. Then the module resets the *Setpoint acknowledge* bit to 0 to signal when a new position setpoint is accepted.

"Single setpoint" mode

When the *Change set immediately* bit is set to 0 (Ⓐ in figure "Principle for applying the setpoint"), then the module is operating in *Single setpoint* mode. This mechanism results in a speed of 0 when the motor reaches position setpoint x_1 at time t_1. After the controller has been notified that the setpoint has been reached, the next setpoint x_2 will be processed at time t_2 and reached at t_3.

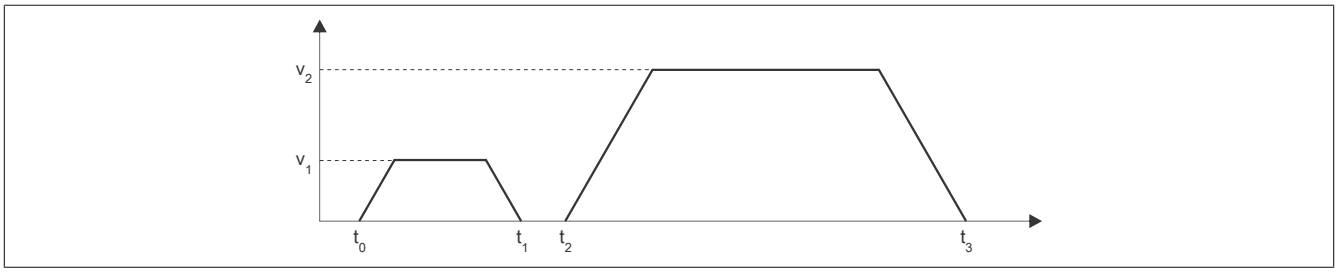


Figure 397: Ramp in *Single setpoint mode*

"Set of setpoints" mode

When the *Change set immediately* bit is set to 1 (Ⓑ in figure "Principle for applying the setpoint"), then the module is operating in *Single setpoint* mode. This means that the module receives the first position setpoint at t_0. A second position setpoint is received at the time t_1. The drive immediately adapts the current movement to the new setpoint.

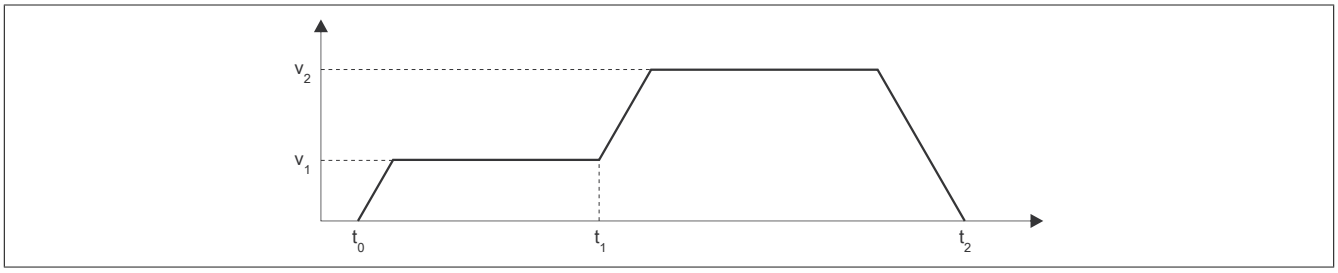


Figure 398: Ramp in *Set of setpoints mode*

Relative position setting

When the *abs / rel* bit in the Extended control word register is set, then the position setpoint is interpreted as a relative value. At each *New setpoint* trigger, the position setpoint will be increased by this value (or decreased if the value is negative).

If the mode changes between the position settings, relative movement will then proceed starting at the last specified position. The position setpoint mode is initialized with 0 when the module is started.

Mode 2: Speed mode - Constant speed (pos./neg.)

The value in the Position/speed register is now interpreted as the speed setpoint (microsteps/ cycle).

Observing the maximum permissible acceleration, the motor moves with a ramp to the desired speed setpoint and maintains this speed until a new speed setpoint is specified.

Values are allowed within the range -65535 to 65535. When a value is entered outside of this range, it is readjusted to these limits.

Mode -120: Set home position

This mode is supported starting with upgrade 1.3.1.0 (firmware version 16).

The current actual position is modified so that the position specified by the Position/speed register is at the home position. If you subsequently move to this position, the motor is at the home position.

The home position in the "Home position" register is also set to this value.

Before this mode is called, the motor must be at a standstill and the home position must have been determined using the "Positive / negative homing" mode. In order to set the position, the State machine must be in the state "Operation Enable".

Mode -121: Remaining distance mode (like Modus 1)

The number of steps defined in the "Fixed position A" register are added to the current position and the resulting position is approached at a rising/falling edge on digital input 3.

Note:

Steps are not added to the position setpoint, but rather to the current position at the moment the trigger occurs.

Negative values are also allowed for the offset defined in "Fixed position A".

New position setpoints are no longer accepted in the Position/speed register after the trigger event. There must first be a switch made to mode 0 and then back to mode -121.

The "Target reached" bit in the Status word register is not set to 1 until the end position (after the trigger event) has been reached.

The Homing configuration determines whether a rising or falling edge of the digital input is used as a trigger.

The Reversing loop is not enabled in this mode (i.e. any configured values not equal to 0 are ignored).

Mode -122: Set the actual position

The position setpoint set in the "Position/speed" register is accepted as the current actual position in the internal position counter when the state machine is in the "Operation Enable" state.

Before this mode is started, the motor must be at a standstill and physically located at the point for which the position being set should be applied.

Mode -123: Move to the position setpoint when the external input is set

The set position defined in the "Position/speed" is moved to when a rising edge occurs on the corresponding digital input.

A new position setpoint is not accepted until another rising edge occurs on the corresponding digital input. This can also occur during the active positioning procedure and will be applied immediately.

Mode -124: Two position mode

The positions "Fixed position A" and "Fixed position B" are defined in the non-cyclic registers.

The value 1 on digital input 3 moves to fixed position A. The value 0 moves to fixed position B. It is also possible to switch between the two during an active positioning movement.

Mode -125/-126: Move to fixed position X

The purpose of these modes is to enable a virtual switch from speed mode to position mode, which otherwise isn't possible because of the double use of the register for position and speed setpoints.

- Mode -125: Fixed position A
- Mode -126: Fixed position B

Mode -127/-128: Homing (positive/negative)

Mode -127 and -128 are used to select which direction to move in.

The motor must be at a standstill before switching from another mode to one of the homing modes.

If the homing condition occurs, then the motor stops and the values of the position counter and ABR counter valid at the moment when the homing condition occurs are written to the Homed zero position register.

You must specify in the Homing configuration whether homing should occur at low/high level on the digital input, during stall or unconditionally.

Homing via digital input

Case 1: Active homing level not yet reached → Motor not yet at end position:

Movement continues at homing speed in the homing direction until the active level for "homing-stop" is on the digital input.

Case 2: Active homing level already reached → Motor at end position:

Movement continues at the homing speed, counter to the homing direction, until the active level for "homing-stop" is no longer on the digital input. Movement continues at homing speed in the homing direction until the active level for "homing-stop" is on the digital input again.

Homing during stall

Movement continues in the homing direction until a stall is detected. When a stall is detected, the value of the position counter is entered in the Homed zero position register within one millisecond. The motor is then stopped abruptly (not using the deceleration ramp). However, it can take up to 25 ms to stop the motor because the ramp generator runs with a configurable internal cycle of up to 25 ms.

In this mode, the rated current is always used instead of the maximum current, even in acceleration phases.

To test the response behavior of this homing mode, the motor load value used for identifying a stall can be made visible in the status word (see "Stall detection configuration / Mixed decay").

Homing unconditional (immediate)

Immediate homing: The current values of the position counter and ABR counter are immediately entered in the Homed zero position register (no motor movement).

Current position (cyclic)

Name:
AbsPos01ActVal

This cyclic register contains the current position.

Default: Value of the internal position counter, can be changed to ABR counter

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Status word

Name:
MpGenStatus01

The bits in this register reflect the state of the state machine. For a more detailed description, see "Status word" and "State machine".

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Ready to switch on	x	
1	Switched on	x	
2	Operation enabled	x	
3	Fault (error bit)	x	
4	Voltage enabled	x	
5	Quick stop	x	
6	Switch on disabled	x	
7	Warning	x	
8	Reserved	0	
9	Remote	1	Always 1 because there is no local mode for the SM module
10	Target reached	x	
11	Internal limit active	0	No limit violation
		1	Internal limit is active (upper/lower software limit violated)
12	Mode-specific	x	
13 - 15	Reserved / Motor load value	0	Always 0 when bit 7 in the Stall detection configuration / Mixed decay register is set to 0.
		x	Returned motor load value

Input status

Name:
InputStatus

This register indicates the logical states of digital inputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Digital input 1	0 or 1	Input state - Digital input 1
...		...	
3	Digital input 4	0 or 1	Input state - Digital input 4
4 - 15	Reserved	0	

Motor ID

Name:
Motoridentification01

This register is used to identify the connected motor type for service purposes and to differentiate between motors in the application. Following measurement, this register contains the time [µs] needed to apply a current increase of ΔI = 1 A to a motor winding.

This depends on:

- Operating voltage
- The inductance and resistance of the motor winding

Notes		
1)	To achieve reproducible results, the measurement must be made under the following defined conditions:	
	a)	Motor is at standstill
	b)	The motor must be in a half-step position (phase A fully powered, phase B not powered). This means the internal position counter on the SM module must have a value that fulfills the following conditions: • Full steps are divisible by 4 • Microsteps = 0
2)	Condition 1b) is fulfilled after a the SM module is reset or powered on. Immediately afterwards, when the holding current is applied to the motor for the first time (at standstill), the duration for applying the current is measured. This is therefore a suitable time to read the motor identification register in the application.	
3)	The current range from approximately 1/3 of the rated current up to the rated current is used as operating range for determining the motor identifier.	

Data type	Motor ID values	Function
UINT	0	No motor identifier available (after turning on for as long as the measurement conditions are not met)
	1 to 32767	Valid range of values for the motor ID register (in µs)
	65504 to 65519	Ground fault: Motor identification not possible
	65528	Motor ID trigger not possible • Motor has no power applied • Motor in movement • Rated current is set to 0A • Ground fault present
	65529	Invalid value: Underflow
	65530	Overtemperature: Measurement not possible
	65532	Open line: Measurement not possible
	65533	Motor position incorrect: Measurement not possible
	65534	Invalid value: Overrun
	65535	Measurement in progress

Ground fault detection

When the motor is powered on, a ground fault check is performed before motor identification. Error numbers have been added in the motor identification register for the event of a ground fault error (values 65504 to 65519 in the table above).

Homed zero position

Name:
RefPos01CyclicCounter
RefPos01AcyclicCounter

After a homing procedure, the homing position for the cyclic and non-cyclic position counter can be read using these registers (either the internal position counter or ABR counter depending on bit 14 of the "Control word" register).

The following two registers are provided for the motor:

- Homed zero position for cyclic counter
- Homed zero position for non-cyclic counter

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Current position (acyclic)

Name:
AbsPos1ActValAcyclic

This acyclic register contains the current position.

Default: Value of the ABR counter, can be changed to internal position counter

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Reads the extended control word

Name:
ControlReadback01

This register can be used to read the content of the Control word register.

Data type	Value
UINT	0 to 65535

Read back mode

Name:
ModeReadback01

This register can be used to read the content of the Mode register.

Data type	Value
SINT	-128 to 127

Error code

Name:
ErrorCode01

The cause of an error or warning can be read in this register.

Data type	Error code	Error type	Priority	Description
UINT	0x0000	-	-	No error
	0x3000	Error	High	Voltage
	0x4200	Error	:	Overtemperature
	0xFF20	Warning	:	Negative limit switch
	0xFF21	Warning	:	Positive limit switch
	0x2300	Warning	:	Overcurrent
	0xFF00	Warning	:	Current error[1)]
	0xFF01	Warning	Low	Stall [2)]

1) A current error is only detected if bit 13 = 1 in the control word (current error detection enabled).
2) Stall is only detected if bit 15 = 1 in the control word (stall detection enabled).

Information regarding the handling of errors and warnings:

- Bit 3 (Fault) and bit 8 (Warning) in the status word can be used to query whether an error or a warning was reported in the error code register.
- Bit 7 (Fault Reset) and bit 8 (Warning Reset) in the control word are used to acknowledge pending errors and warnings.
- If two or more errors/warnings are pending, the one with the highest priority (the order in the table above) will be displayed in the error code register.

4.25.7.15.8.4 Ramp function model operation

Control for this model has been based on the CANopen communication profile DS402.

Commands for controlling the modules are written to the "Control word". The current module state is returned to the "Status word" register. The function mode (absolute position, constant speed, homing, etc.) is set in the "Mode" register.

Control word

Control word bits and their state for the commands of the state machine:

Command	Reserved	ABR counter sync/async	Current error detection	Warning reset	Motor ID trigger	Reserved	Reserved	Halt 2)	Fault reset	Mode specific	Mode specific	Mode specific	Enable operation	Quick stop	Enable voltage	Switch on
Bit[1]	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Shutdown	x	x	x	x	x	0	0	x	0	x	x	x	x	1	1	0
Switch on	x	x	x	x	x	0	0	x	0	x	x	x	0	1	1	1
Disable voltage	x	x	x	x	x	0	0	x	0	x	x	x	x	x	0	x
Quick stop	x	x	x	x	x	0	0	x	0	x	x	x	x	0	1	x
Disable operation	x	x	x	x	x	0	0	x	0	x	x	x	0	1	1	1
Enable operation	x	x	x	x	x	0	0	x	0	x	x	x	1	1	1	1
Fault reset	x	x	x	x	x	0	0	x	↑	x	x	x	x	x	x	x

1) x ... Any; ↑ ... Rising edge
2) Bit 8 (Halt) is only evaluated if the extended control word is enabled in the "General configuration" register.

Bits 0, 1, 2, 3 and 7 (light gray in the previous table)	These bits control the state of the "State machine" according to the commands in the table above.
stop	0 ... Perform motor movement 1 ... Stop axis with deceleration This bit is only evaluated when the extended control word is activated in the "General configuration" register.
Motor ID trigger	A rising edge enables the motor ID measurement.
Warning reset	A rising edge resets warnings (no effect on errors, which are reset using "Fault Reset"; the state machine is not affected by this bit)
Fault reset	A rising edge resets errors and warnings (see "State machine" on page 2476)
Current error detection	0 ... Current error detection disabled 1 ... Current error detection enabled
ABR counter sync/async	0 ... Value of the ABR counter on the "Current position (non-cyclic)" register. Internal position counter of the ramp generator on the "Current position (cyclic)" register. 1 ... Value of the ABR counter on the "Current position (cyclic)" register. Internal position counter of the ramp generator on the "Current position (non-cyclic)" register.
Stall detection	0 ... Stall detection disabled 1 ... Stall detection enabled

Status word

The individual bits of this register and its states depend on the current state of the state machine:

Status	Reserviert / MotorLoadBit 2 [1]	Reserviert / MotorLoadBit 1 [1]	Reserviert / MotorLoadBit 0 [1]	Mode-specific	Int. limit active	Target reached	Remote	Reserved	Warning	Switch on disabled	Quick stop	Voltage enabled	Fault	Operation enabled	Switched on	Ready to switch on
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not ready to switch on	x	x	x	x	x	x	1	0	x	0	x	0	0	0	0	0
Switch on disabled	x	x	x	x	x	x	1	0	x	1	x	0	0	0	0	0
Ready to switch on	x	x	x	x	x	x	1	0	x	0	1	0	0	0	0	1
Switched on	x	x	x	x	x	x	1	0	x	0	1	1	0	0	1	1
Operation enable	x	x	x	x	x	x	1	0	x	0	1	1	0	1	1	1
Quick stop active	x	x	x	x	x	x	1	0	x	0	0	1	0	1	1	1
Fault reaction active	x	x	x	x	x	x	1	0	x	0	x	0	1	1	1	1
Fault	x	x	x	x	x	x	1	0	x	0	x	0	1	0	0	0

1) If bit 7 is set to 1 in the Mixed decay / Stall detection register, then the motor load value is returned in bits 13-15 of the status word. Otherwise these bits are always 0.

Information about the status word:

Bits 0,1,2,3,5 and 6 (light gray in the previous table)	These bits are set according to the current state of the "State machine".	
Voltage enabled	Becomes 1 as soon as the motor is powered	
Warning	Becomes 1 if a warning is detected ("Overcurrent", "Undercurrent"). The type of warning is indicated in the "Error code" register. The highest priority error / warning is shown in each case, with the priority corresponding to the order in the respective table. Warnings can be reset with a rising edge on the "Warning reset" bit in the control word.	
Remote	Always 1 since there is no local mode on the SM module	
Target reached[1], depending on bit 8 (Halt) in the register Control word	**If Halt = 0**	**If Halt = 1**
	In modes 1, -123, -124, -125 and -126 (absolute positioning): 0 ... Positioning begins 1 ... Target has been reached **In mode 2 (constant speed):** 0 ... Motor accelerates/brakes 1 ... Speed setpoint reached **In modes -127 and -128 (homing):** 0 ... Homing started 1 ... Homing ended **In mode -122 (set actual position):** The bit briefly becomes 0 and immediately becomes 1 again as soon as the position is set.	**In all modes:** 0 ... Axis decelerating 1 ... Axis speed = 0
Internal limit active	0 ... No limit violation 1 ... Internal limit is active (upper/lower software limit violated)	

Table 579: Information about the status word

1) If Halt has not been activated in the "General configuration" register, then "Target Reached" behaves the same as when Halt = 0.

State machine

The motor is controlled according to the state machine illustrated below. After the module is started, the state machine automatically changes to the state "*Not ready to switch on*". The application then operates the state machine by writing commands to the "Control word".

The state machine successively reaches the states "*Ready to switch on*", "*Switched on*" and "*Operation enable*" by writing the consecutive commands "*Shutdown*", "*Switch on*" and "*Enable operation*".

Information:

Motor movements are not performed until the "*Operation enable*" state, according to the setting in the Mode register.

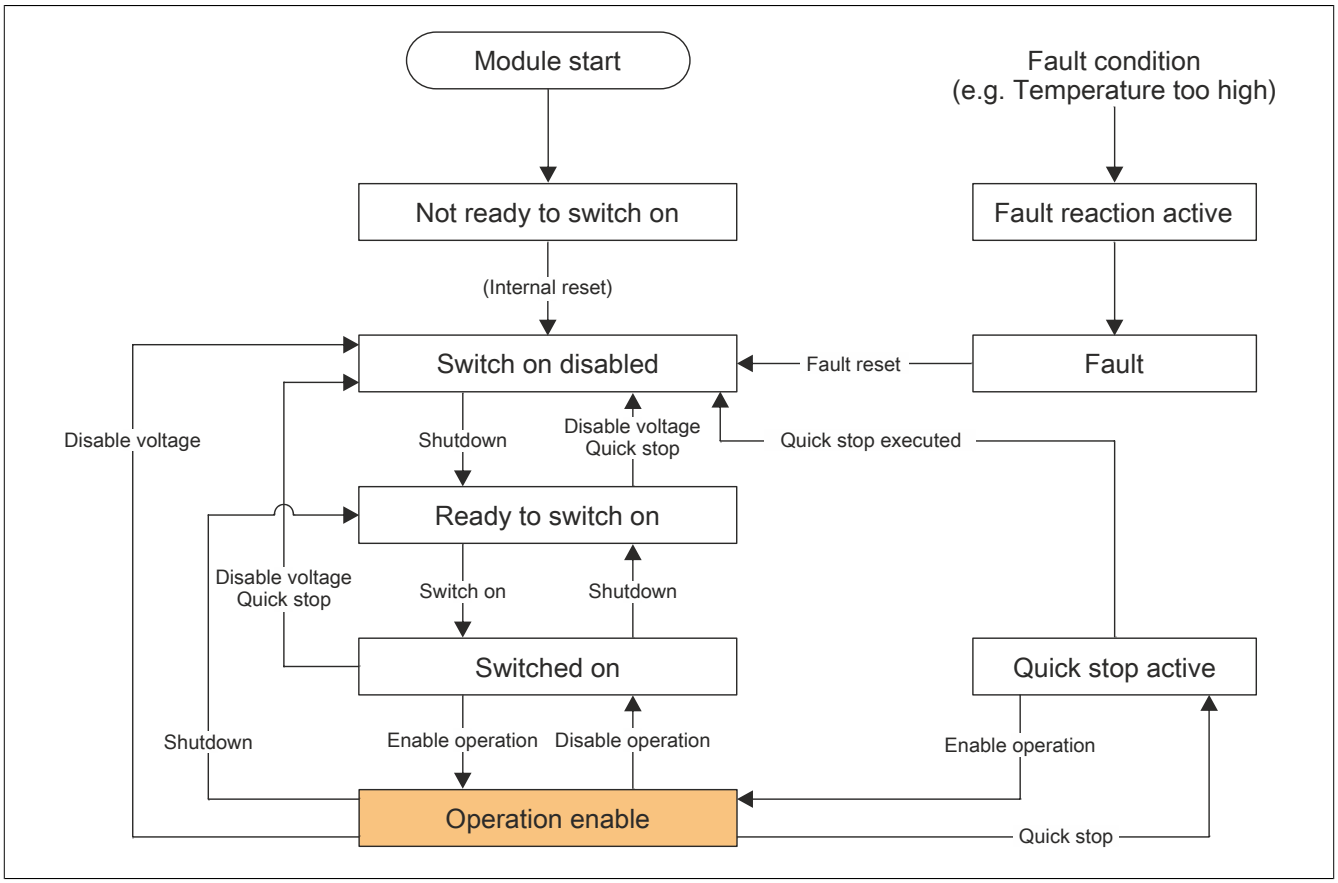


Figure 399: State machine - Flow chart

State change	Description
Not ready to switch on → Switch On Disabled	This state change occurs automatically after starting the module and internal initialization has taken place.
Switch on disabled → Ready to Switch On	This state change is brought on by the *Shutdown* command. No others actions are performed.
Ready to switch on → Switch On Disabled	This state change is brought on by the command *Disable voltage* or *Quick stop*. No others actions are performed.
Switched on → Switch On Disabled	This state change is brought on by the command *Disable voltage* or *Quick stop*. The motor voltage is switched off immediately.
Ready to switch on → Switched On	This state change is brought on by the *Switch on* command. The motor voltage is switched on. When this state change occurs for the first time since the module is started, the motor ID measurement is performed before the *Switched on* state is achieved. This can take approximately 1 second.
Switched on → Ready to Switch On	This state change is brought on by the *Shutdown* command. The motor voltage is switched off immediately.
Switched on → Operation Enable	This state change is brought on by the *Enable operation* command. Motor movements are now performed depending on the defined mode.
Operation enable → Switched On	This state change is brought on by the *Disable operation* command. If in motion, the motor is decelerated with the configured deceleration. Motor voltage remains on in the *Switched on* state.
Operation enable → Ready to Switch On	This state change is brought on by the *Shutdown* command. The motor voltage is switched off immediately.
Operation enable → Switch On Disabled	This state change is brought on by the *Disable voltage* command. Motor voltage switched off. It is strongly recommended to only make this state change on a stopped motor since regeneration on a motor running at no load can cause an overvoltage error on the DC bus (0x3210).
Operation enable → Quick Stop Active	This state change is brought on by the *Quick stop* command. If in motion, the motor is decelerated with the configured deceleration. During the deceleration, the state machine remains in the *Quick stop active* state. Once the motor is at standstill, the state automatically changes to the *Switch on disabled* state. While the state machine is in the *Quick stop active* state, the *Enable operation* command can be used to switch it back to the *Operation enable* state.
→ Fault reaction active	This state change is brought on when an error occurs and cannot be triggered by a command from the user. It can be triggered by error types classified as an "Error" (see "Error code"). (Other error types listed as "Warning" only cause the "Warning" bit to be set in the status word and do not cause a state change in the state machine.) Motor voltage is switched off and the state machine then changes immediately to the *Fault* state. The type of error is listed in the error code register (see the table under "Error code"). The highest priority error is shown. The priority corresponds to the order in the error code table.
Fault → Switch On Disabled	This state change is brought on by the *Fault reset* command. However, the state only changes if no more errors are present when the command is written. All errors and warnings are reset. The error code register contains 0 or the warning code if a warning is still present.

Table 580: State machine - State change

4.25.7.15.9 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Standard function model	250 µs
Ramp function model	250 µs

4.25.7.15.10 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Standard function model	250 µs
Ramp function model	
Inputs	250 µs
Outputs[1)]	25 ms

1) Depending on the configuration of the motion profile generator

4.26 Other functions

The following modules are included in this module group:

- Multi-measurement transformers / synchronization modules
- Universal mixed modules and combination modules
- Diode array modules
- PWM modules
- IO-Link master modules
- Potential distribution modules
- Supply modules for potentiometers
- Condition monitoring modules
- Specialty modules

4.26.1 Brief information

Product ID	Short description	on page
0ACS100A.00-1	Acceleration sensor, nominal sensitivity 100 mV/g, top exit	2731
0ACS100A.90-1	Acceleration sensor, nominal sensitivity 100 mV/g, side exit	2733
X20CM0985	X20 digital and analog mixed module, multi-measurement transducer/ synchronization module, 5 digital outputs, 24 VDC, 0.5 A source, 1 relay, 1 A, changeover contact, 8 analog inputs, ±480 V / 120 V, 16-bit converter resolution, 3 analog inputs 5 A / 1 A AC, 16-bit converter resolution, order terminal blocks 0TB3102-7011, 0TB3104-7011, 0TB3102-7012, 0TB3104-7012 and 2x TB12 separately.	2552
X20CM0985-1	X20 digital and analog mixed module, multi-measurement transducer/ synchronization module, 5 digital outputs, 24 VDC, 0.5 A, source, 1 relay 1 A, 8 analog inputs, ±480 V / 120 V, 16-bit converter resolution, 3 analog inputs 5 A / 1 A AC, 16-bit converter resolution, additional software functions, order terminal blocks 0TB3102-7011, 0TB3104-7011, 0TB3102-7012, 0TB3104-7012 and 2x X20TB12 separately	2481
X20CM4810	X20 analog input module for vibration measurement and analyse of condition monitoring exercises. 4 IEPE analog input 51,5625 kHz sampling frequency 24 bit converter resolution	2594
X20CM6209	X20 diode array module, 1 A, 40 V reverse voltage, no module status data	2737
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement	2740
X20CM8323	X20 PWM module, 8 digital outputs for switching electromechanical loads, 0.6 A continuous current, 2 A peak current, current monitoring, switching time detection	2759
X20DS4387	X20 digital signal module, 4x IO-Link master, 4 digital channels configurable as inputs or outputs, 3-wire connections	2777
X20DS438A	X20 digital signal module, 4x I/O-Link master V1.1, can also be configured as 4x digital input or output channels, 3-wire connections	2794
X20PD0011	X20 potential distributor module, 12x GND, integrated microfuse	2858
X20PD0012	X20 potential distributor module, 12x 24 VDC, integrated microfuse	2862
X20PD0016	X20 potential distributor module, 5x GND, 5x 24 VDC, each with 1x floating feed, integrated microfuse	2866
X20PD2113	X20 potential distributor module, 6x GND, 6x 24 VDC, with feed option, integrated microfuse	2871
X20PS4951	X20 power supply module, for potentiometers, 4x ±10 V for potentiometer supply	2877
X20cPD2113	X20 potential distributor, coated, 6x GND, 6x 24 VDC, with supply option, integrated microfuse	2871

4.26.2 X20CM0985-1

4.26.2.1 General information

The module has a compact size and combines a power measurement module that has special features with a synchronization unit that is able to meet all demands.

The measurement unit's 3 current inputs are suitable for both X: 1 A and X: 5 A current transformers. Overcurrent resistance and the high resolution of the measurement unit round off its features. For the voltage inputs, the value range can be configured between 480 VAC and 120 VAC.

The area of use includes 4-wire AC networks with a phase voltage up to 480 VAC and 3-wire systems, whereas L2 can be grounded (V-connection). The module can also handle Aron measuring circuits.

The resulting measured values include the pure phase current; line-to-line voltage or phase voltage; the effective, reactive and apparent power parts; the mains frequency; the power factor and much more. In addition, peak values and energy meters are stored on the module in nonvolatile memory. Depending on the configuration, it is also possible to use a digital output as a pulse encoder for an external energy meter.

The synchronization unit doesn't just take the phasing and phase voltage into consideration; integrated intelligence also monitors the rate of change and other parameters, allowing them to influence when the synchronization output is switched. It is also possible to monitor a generator using a large number of additional conditions. A total of 4 voltage inputs provide substantial overall flexibility.

Monitoring functions expand the features of the module. Rating-dependent overcurrent monitoring is included, which utilizes the thermal capacity of the motor/generator to allow short overloads while still providing full protection. The dependent, delayed imbalanced load monitoring used to protect three-phase generator and three-phase networks from imbalanced load can be adapted to the characteristics of different generator types using parameters while taking their special thermal time constants into account.

- Energy measurement for 120 to 480 VAC
- Simultaneous measurement of 2 AC mains networks plus 2 additional voltages
- For multifunctional measurement tasks
- Intelligent mains synchronization unit

Information:

Please refer to section 4.26.2.4 "Safety guidelines" before operating the module.

4.26.2.2 Order data

Model number	Short description	Figure
	Other functions	
X20CM0985-1	X20 digital and analog mixed module, multi-measurement transducer/ synchronization module, 5 digital outputs, 24 VDC, 0.5 A, source, 1 relay 1 A, 8 analog inputs, ±480 V / 120 V, 16-bit converter resolution, 3 analog inputs 5 A / 1 A AC, 16-bit converter resolution, additional software functions, order terminal blocks 0TB3102-7011, 0TB3104-7011, 0TB3102-7012, 0TB3104-7012 and 2x X20TB12 separately	
	Required accessories	
	Terminal blocks	
0TB3102-7011	Accessory terminal block, 2-pin, A-keying, screw clamp 6 mm²	
0TB3102-7012	Accessory terminal block, 2-pin, B-keying, screw clamp 6 mm²	
0TB3104-7011	Accessory terminal block, 4-pin, A-keying, screw clamp 6 mm²	
0TB3104-7012	Accessory terminal block, 4-pin, B-keying, screw clamp 6 mm²	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 581: X20CM0985-1 - Order data

4.26.2.3 Technical data

Product ID	X20CM0985-1
Short description	
I/O module	X20 energy measurement and synchronization module
General information	
B&R ID code	0xB768
Status indicators	Channel status, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Analog inputs	Yes, using status LED (measurement range of analog inputs)
Digital outputs	Yes, using status LED and software
Overvoltage category	II [1]
Measurable frequency	15.2 Hz to 2x rated frequency [2]
Power consumption	
Bus	1.05 W
Internal I/O	4 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - I/O supply	Yes
Input/Output - Bus	Yes
Digital outputs - Analog inputs	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [3]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Design	FET positive switching
Quantity	5
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.1 A
Total nominal current	0.5 A
Connection type	1-wire connections
Output circuit	Source
Output protection	Thermal cutoff for overcurrent and short circuit
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
Residual voltage	<0.3 V at 0.1 A rated current
Peak short circuit current	<2 A
Switching on after overload or short circuit cutoff	Approx. 10 ms, depends on the module temperature
Switching delay	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load	Max. 100 Hz
Isolation voltage between channel and bus	500 V_{eff}
Relay outputs	
Quantity	1

Table 582: X20CM0985-1 - Technical data

Product ID	X20CM0985-1
Design	Relay / Changeover contact
Nominal voltage	30 VDC / 240 VAC
Rated frequency	DC / 45 to 63 Hz
Switching capacity	
Min.	10 mA / 5 VDC
Max.	30 W / 240 VAC
Nominal output current	1 A at 30 VDC / 1 A at 240 VAC
Actuator supply	External
Switching voltage	Max. 60 VDC / 250 VAC
Switching delay	
0 -> 1	≤10 ms
1 -> 0	≤10 ms
Service life [4]	
Mechanics	Min. 10 x 10^6 ops.
Electrical	Min. 60 x 10^3 ops. (NC) at 1 A Min. 30 x 10^3 ops. (NO) at 1 A
Contact resistance	Max. 100 mΩ
Protective circuit	
Internal	None
External	None
DC	Inverse diode, RC combination or VDR
AC	RC combination or VDR
Isolation voltage	
Contact - Contact	1000 VAC / 1 min
Contact - Coil	4000 VAC / 1 min
Analog input voltage	
Channels	8
Input	120 VAC / 480 VAC
Input type	Single-ended
Digital converter resolution	±15-bit
Conversion time	
50 Hz	10 ms
60 Hz	8.33 ms
Permitted input signal	Max. 132 VAC / 528 VAC
Output format [5]	
±120 VAC	1 LSB = 0x0001 = 5.707 mV
±480 VAC	1 LSB = 0x0001 = 22.787 mV
Output of the digital value during overload	
Above upper limit	0x7FFF
Below lower limit	0x8001
Conversion method	SAR
Input filter	
Cutoff frequency	10 kHz
Slope	60 dB
Maximum gain drift [6]	0.02% per °C
Maximum offset drift [7]	0.003% per °C
Crosstalk between channels	-70 dB
Nonlinearity [7]	≤0.5% at 45 to 65 Hz
Protection against electrical shock	Protective impedance in accordance with IEC 61131-2
Test voltage between channel and bus (type test)	3700 V_{eff}
Output format	INT
Input impedance in signal range	Approx. 3 MΩ
Max. error at 25°C	
Gain	0.09% [6]
Offset	0.03% [7]
Input protection	Overvoltage protection
Analog input current	
Channels	3
Input	1 A / 5 A AC
Input type	Isolated current transformer according to the compensation principle with a magnetic sensor, for connecting an external transformer
Digital converter resolution	±15-bit
Conversion time	
50 Hz	10 ms
60 Hz	8.33 ms
Permitted input signal	Max. 1.5 A / 7.7 A
Output format [5]	
±1 A	1 LSB = 0x0001 = 189.903 µA
±5 A	1 LSB = 0x0001 = 949.513 µA
Output of the digital value during overload	
Above upper limit	0x7FFF
Below lower limit	0x8001
Conversion method	SAR

Table 582: X20CM0985-1 - Technical data

Product ID	X20CM0985-1
Input filter	
Cutoff frequency	10 kHz
Slope	60 dB
Maximum gain drift [6]	0.07% per °C
Maximum offset drift	Measurement range 2 A: 0.0064% per °C; Measurement range 10 A: 0.00384% per °C
Crosstalk between channels	-70 dB
Nonlinearity [8]	≤0.5% at 45 to 65 Hz
Isolation voltage between channel and bus	500 V_{eff}
Output format	INT
Max. error at 25°C	
Gain	0.2% [6]
Offset	0.05% [8]
Thermal overcurrent [9]	15 x I_{Nom} for 0.2 s [10]
Monitored overcurrent	4 x I_{Nom} [10]
Input impedance [11]	
Measurement range 1 A	Max. 30 mΩ
Measurement range 5 A	Max. 10 mΩ
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 55°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 2x X20TB12 terminal block separately Order 2x TB3102 and 2x TB3104 screw clamps separately
Spacing	$87.5^{+0.2}$ mm

Table 582: X20CM0985-1 - Technical data

1) IEC 61131-2.
2) Rated frequency: 48 to 62 Hz. Synchronization is only possible at the nominal frequency.
3) Ta min.: 0°C
   Ta max.: See environmental conditions
4) See section "Electrical service life"
5) INT, range of values: 0x8001 to 0x7FFF
6) Based on the current measured value.
7) Based on the measurement range 240 VAC / 960 VAC.
8) Based on the measurement range 2 A / 10 A.
9) This can result in the measurement hysteresis being offset in relation to the overcurrent.
10) Based on the measurement range 1 A / 5 A.
11) Including current transformer, circuit path and X20TB12 terminal block (5 mΩ)

4.26.2.4 Safety guidelines

General information

Programmable logic controllers, operating and monitoring devices (e.g. industrial PCs, Power Panels, Mobile Panels etc.) as well as the uninterruptible power supplies have all been designed, developed, and produced by B&R for conventional use in industry. They were not designed, developed and manufactured for any use involving serious risks or hazards that could lead to death, injury, serious physical damage or loss of any kind without the implementation of exceptionally stringent safety precautions. In particular, such risks and hazards include the use of these devices to monitor nuclear reactions in nuclear power plants, their use in flight control or flight safety systems as well as in the control of mass transportation systems, medical life support systems or weapons systems.

When using programmable logic controllers or operating/monitoring devices as control systems together with a Soft PLC (e.g. B&R Automation Runtime or comparable product) or Slot PLC (e.g. B&R LS251 or comparable product), safety precautions relevant to industrial control systems (e.g. the provision of safety devices such as emergency stop circuits, etc.) must be observed in accordance with applicable national and international regulations. The same applies for all other devices connected to the system, e.g. drives.

All tasks such as the installation, commissioning and servicing of devices are only permitted to be carried out by qualified personnel. Qualified personnel are those familiar with the transport, mounting, installation, commissioning and operation of devices who also have the appropriate qualifications (e.g. IEC 60364). National accident prevention regulations must be observed.

The safety notices, connection descriptions (type plate and documentation) and limit values listed in the technical data are to be read carefully before installation and commissioning and must be observed.

Intended use

Danger!

Electronic devices are never completely failsafe. If the multi-measurement and synchronization unit fails, the user is responsible for making sure that the motor or generator is brought to a secure state.

Some errors are detected and prevented in the synchronization unit by the system's internal software monitoring. However, when the device is in operation it is always possible for errors, defective components, software errors or configuration mistakes to occur at any time. B&R emphasizes that the multi-measurement and synchronization unit possesses neither a failsafe function nor a redundancy system. For this reason, independent higher-level safety precautions need to be put in place to ensure that personnel and machines are protected.

Grounding the Mounting Rail

For grounding purposes, a good conductive connection between the mounting rail and the metal back wall is required. The mounting rail is to be connected conductively to the back wall. This is achieved by inserting a contact washer with the fastening screw.

Information:

The control cabinet back wall must be connected with GND

4.26.2.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

LED status indicators - Right

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Orange		Output status of the corresponding digital output

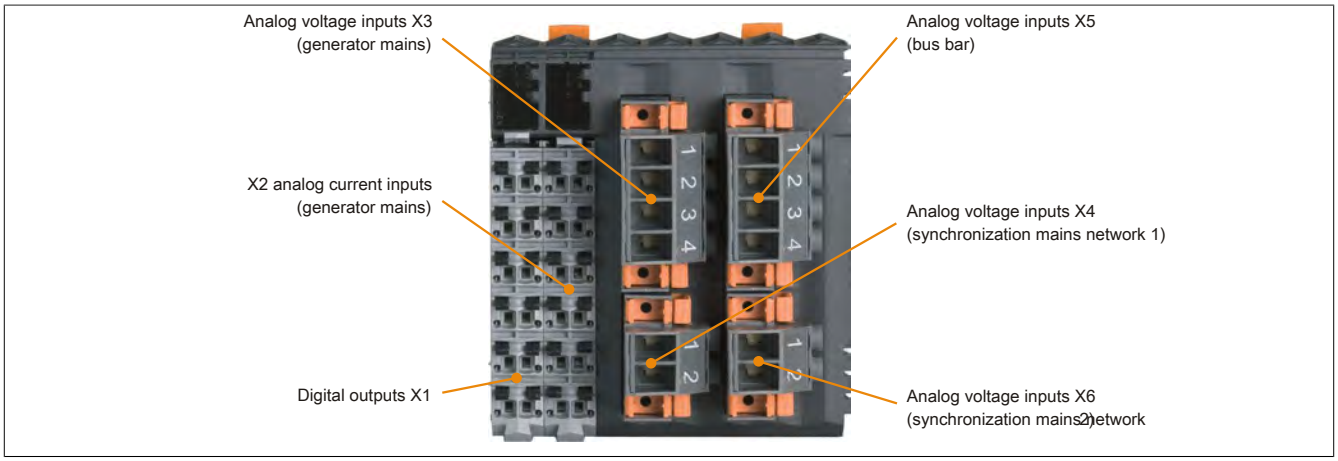
1) Depending on the configuration, a firmware update can take up to several minutes.

Status-LEDs right

Figure	LED[1]	Terminal	Color	Status	Description
	1	X3	Green	On	Measurement range: 120 VAC
			Red	On	Measurement range: 480 VAC
	2	X4	Green	On	Measurement range: 120 VAC
			Red	On	Measurement range: 480 VAC
	3	X5	Green	On	Measurement range: 120 VAC
			Red	On	Measurement range: 480 VAC
	4	X6	Green	On	Measurement range: 120 VAC
			Red	On	Measurement range: 480 VAC
	5	X2	Green	On	Measurement range: 1 A
			Red	On	Measurement range: 5 A

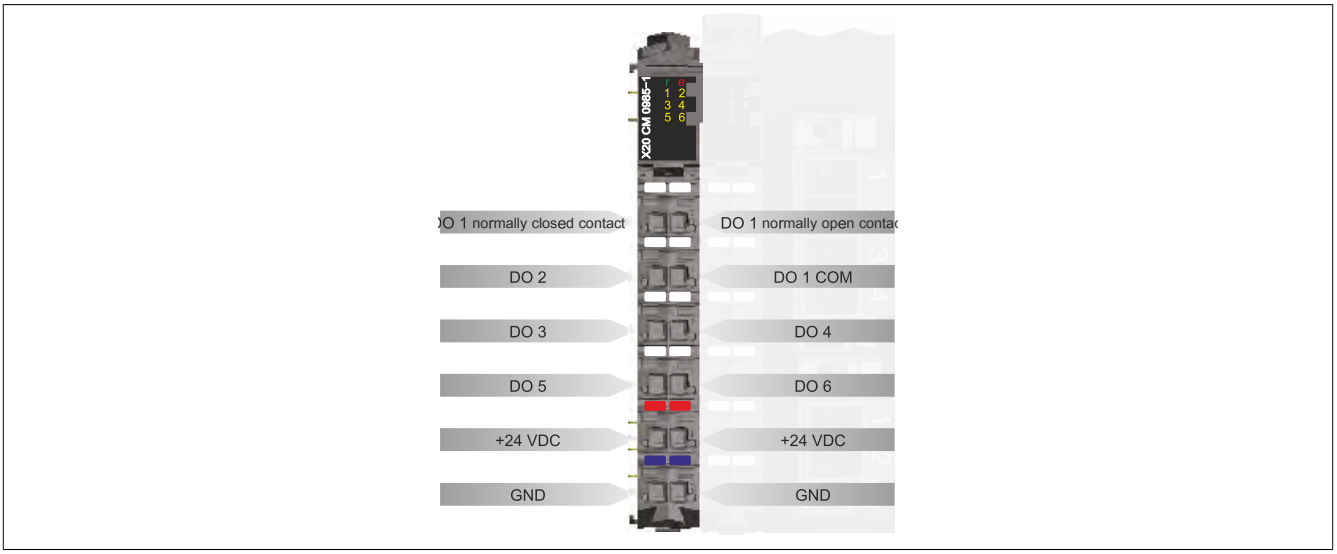
1) LEDs 1 - 5 are green/red dual LEDs.

4.26.2.6 Connection elements



4.26.2.7 Digital outputs X1

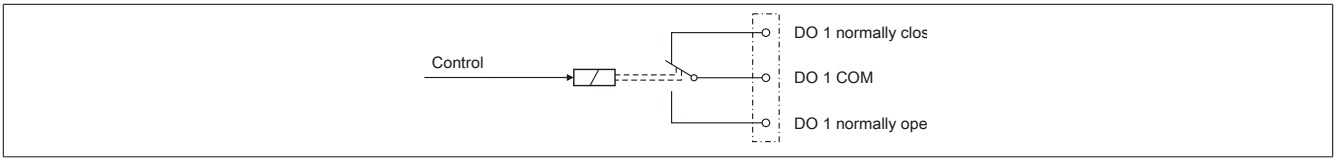
The X1 and X2 terminals can each be keyed differently to prevent them from being inadvertently plugged into the module incorrectly.



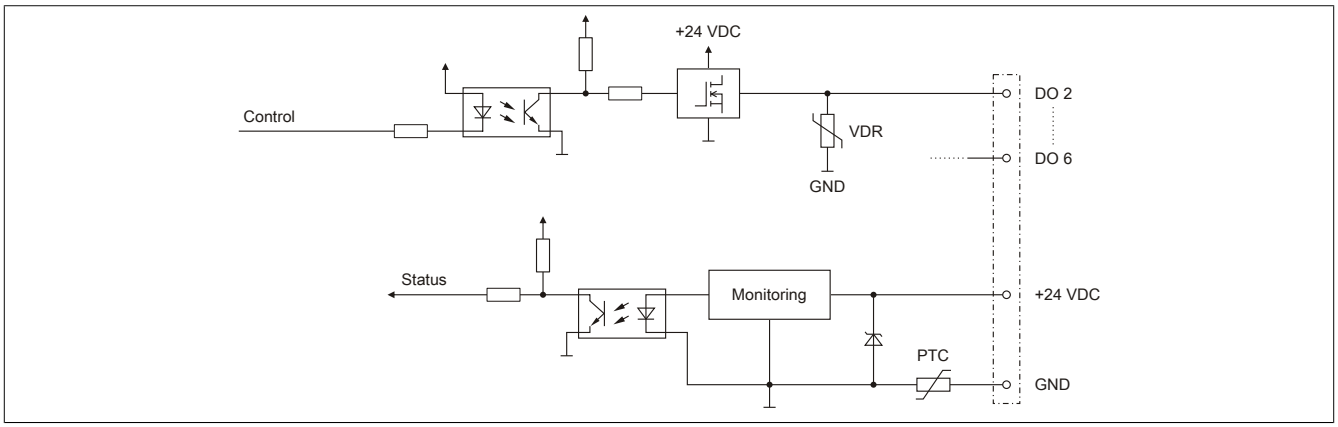
Function description of the digital outputs

Digital output	Description
DO1	This digital output is designed as a changeover contact switch. The monitoring relay allows selected monitoring of the following generator mains network measurement values: • Overvoltage and undervoltage • Overfrequency and underfrequency • Voltage asymmetry • Current asymmetry • Calculated neutral conductor current (maximum) • Short circuit current • Rating-dependent overcurrent • Limit value of the capacitive reactive power (exciter failure) • Generator overload • Generator feedback
DO2	DO2 serves as a meter output. The generated pulses can be recorded by an external energy meter (kWh).
DO3	This output is set when there is no voltage on the bus bar (below the lower limit of the defined parameter). 3-phase monitoring takes place for the bus bar voltage.
DO4	DO4 serves as a synchronization pulse. The power switch is activated by setting this output. The output is deactivated after the configured time has elapsed (**exception:**Synchro check operating mode).
DO5	This output can be configured either as a digital output or monitoring output (see register "ConfigOutput24"). The monitoring function is only available with the "3-phase mains" configuration. When configured as monitoring output, the user can choose between monitoring the following mains measurement values: • Overvoltage and undervoltage • Overfrequency and underfrequency • Voltage asymmetry • Phase shift • Frequency change The monitoring status can be output either normally or inverted. This can be defined using the "DigitalOutput" register. This setting is then disabled when shutting off, resetting, restarting, etc.
DO6	Can be configured as a digital output or synchronization output (see register "ConfigOutput24"). When configured as a synchronization output: DO6 serves as the synchronization pulse. The power switch is activated by setting this output. The output is deactivated after the configured time has elapsed (**exception:**Synchro check operating mode).

DO1 - Output circuit diagram



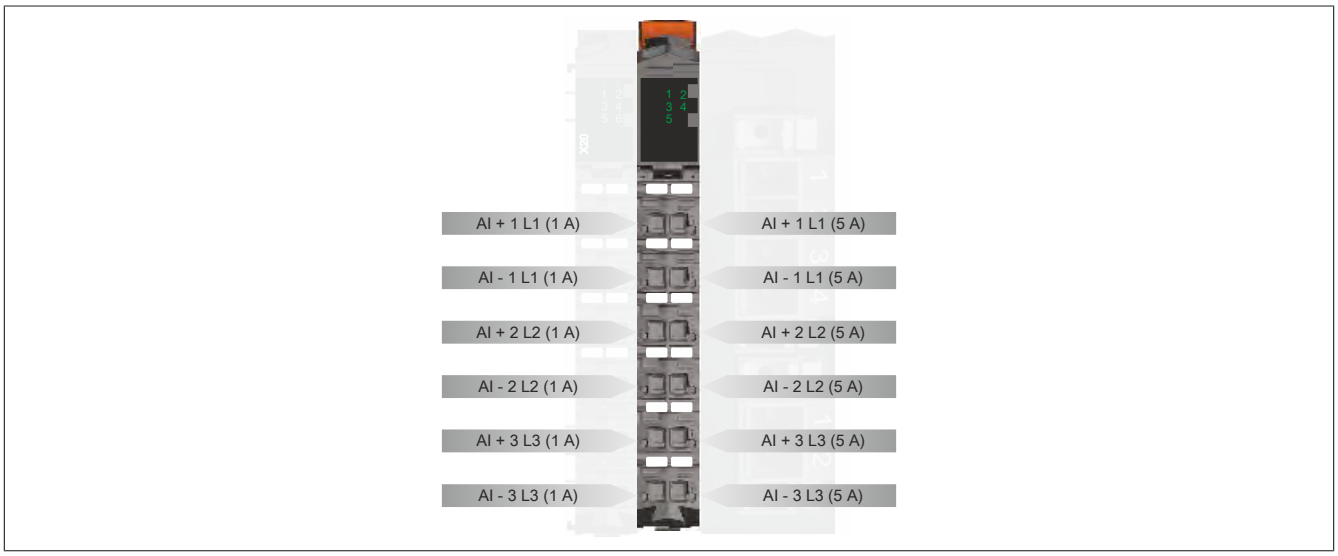
DO2 - DO 6 - Output circuit diagram



4.26.2.8 X2 analog current inputs

The X2 terminal measures the three phase currents of the generator mains using an externally connected current transformer. The measurement range of the current inputs can be configured as 1 A or 5 A.

The X1 and X2 terminals can each be keyed differently to prevent them from being inadvertently plugged into the module incorrectly.

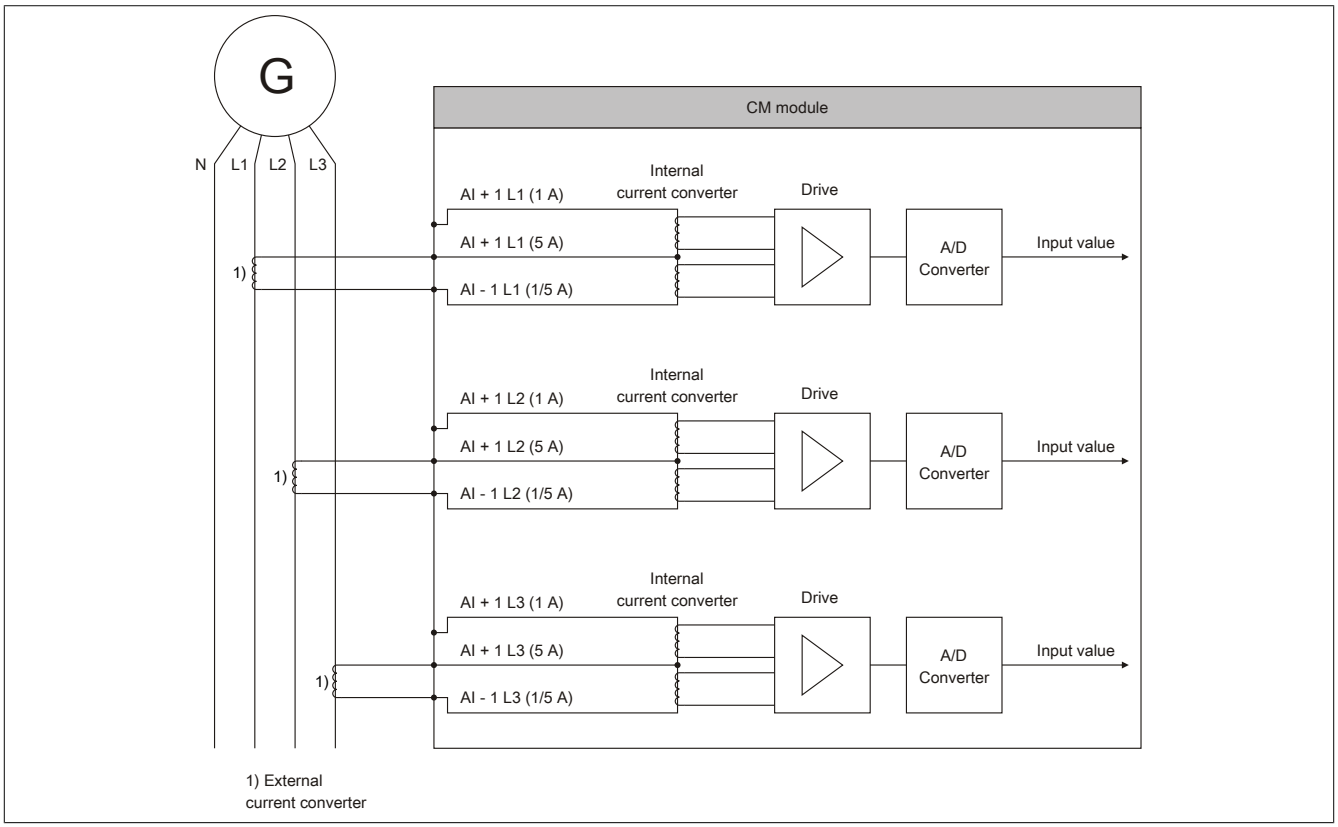


Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

Input circuit diagram - Analog current inputs

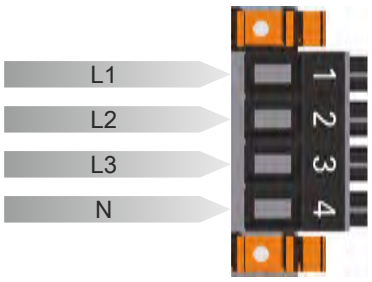


4.26.2.9 X3 and X5 analog voltage inputs

The X3 and X5 terminals are used to measure and monitor the line-to-line and phase voltages of the generator mains and bus bar.

- Terminal X3: Generator mains
- Terminal X5: Bus bar

The X3 and X5 terminals are each keyed differently to prevent them from being inadvertently plugged into the module incorrectly. Section 4.26.2.14 "Releasing the locking clip for terminals X3 - X6" describes how to release the terminal locking clip.



4.26.2.10 X4 and X6 analog voltage inputs

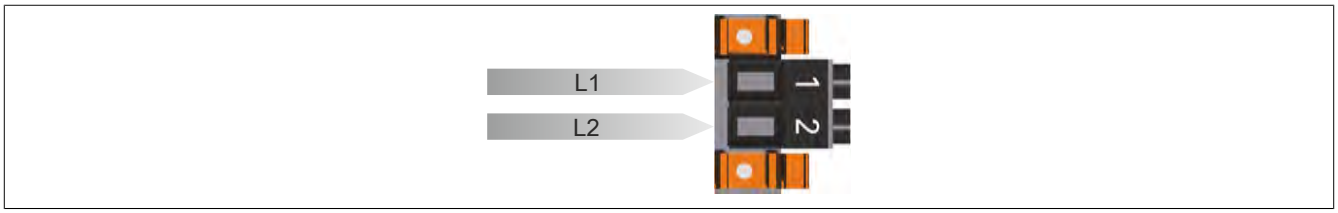
The X4 and X6 terminals are each keyed differently to prevent them from being inadvertently plugged into the module incorrectly. Section 4.26.2.14 "Releasing the locking clip for terminals X3 - X6" describes how to release the terminal locking clip.

The two terminals are connected differently depending on the selected configuration (see register "ConfigOutput68").

Configuration as Sync-mains 1 / Sync-mains 2

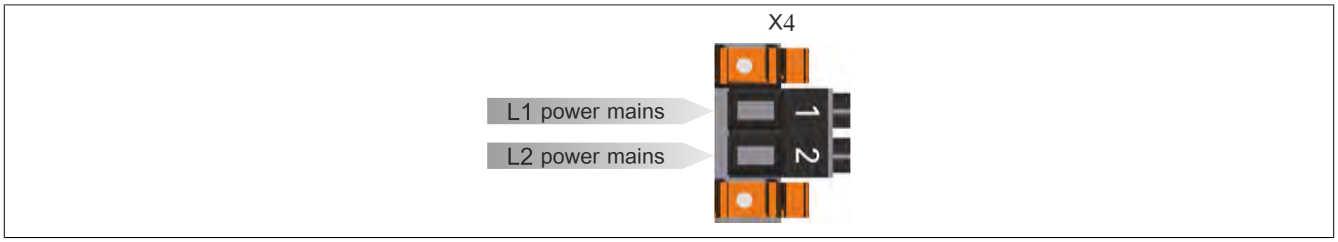
The voltage inputs on the X4 and X6 terminals are used to determine the line-to-line voltages for synchronization between two different mains networks.

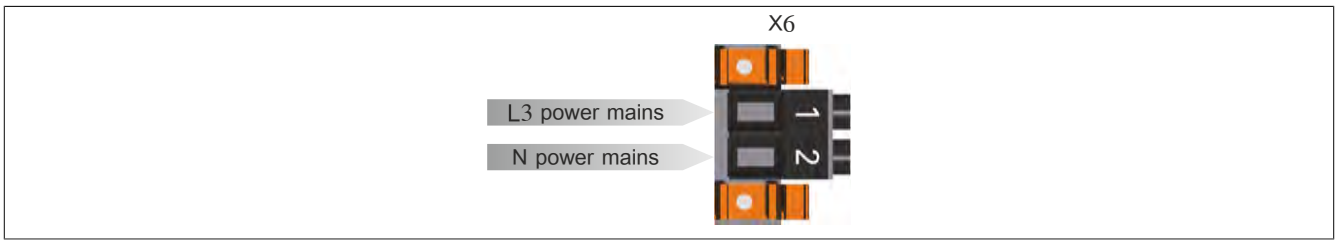
- Terminal X4: Synchronization mains network 1
- Terminal X6: Synchronization mains network 2



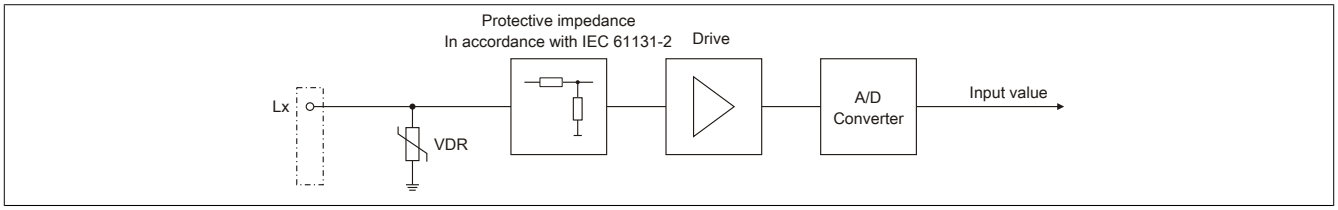
Configuration as 3-phase mains

The terminals X4 and X6 can be combined to form a 3-phase mains. The X4 and X6 terminals are used to measure and monitor the line-to-line voltages and phase voltages of the power mains.



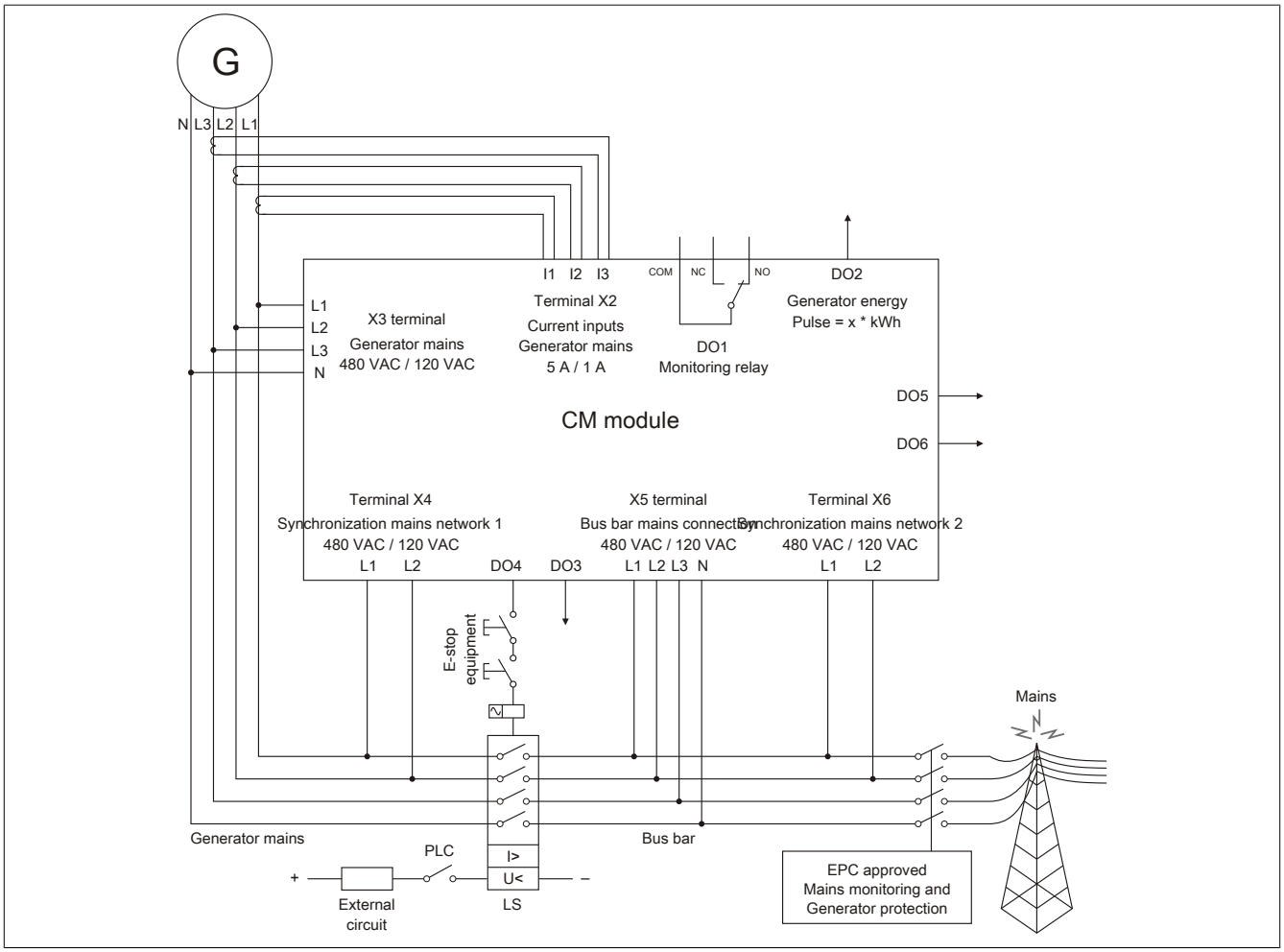


Input circuit diagram, analog voltage inputs

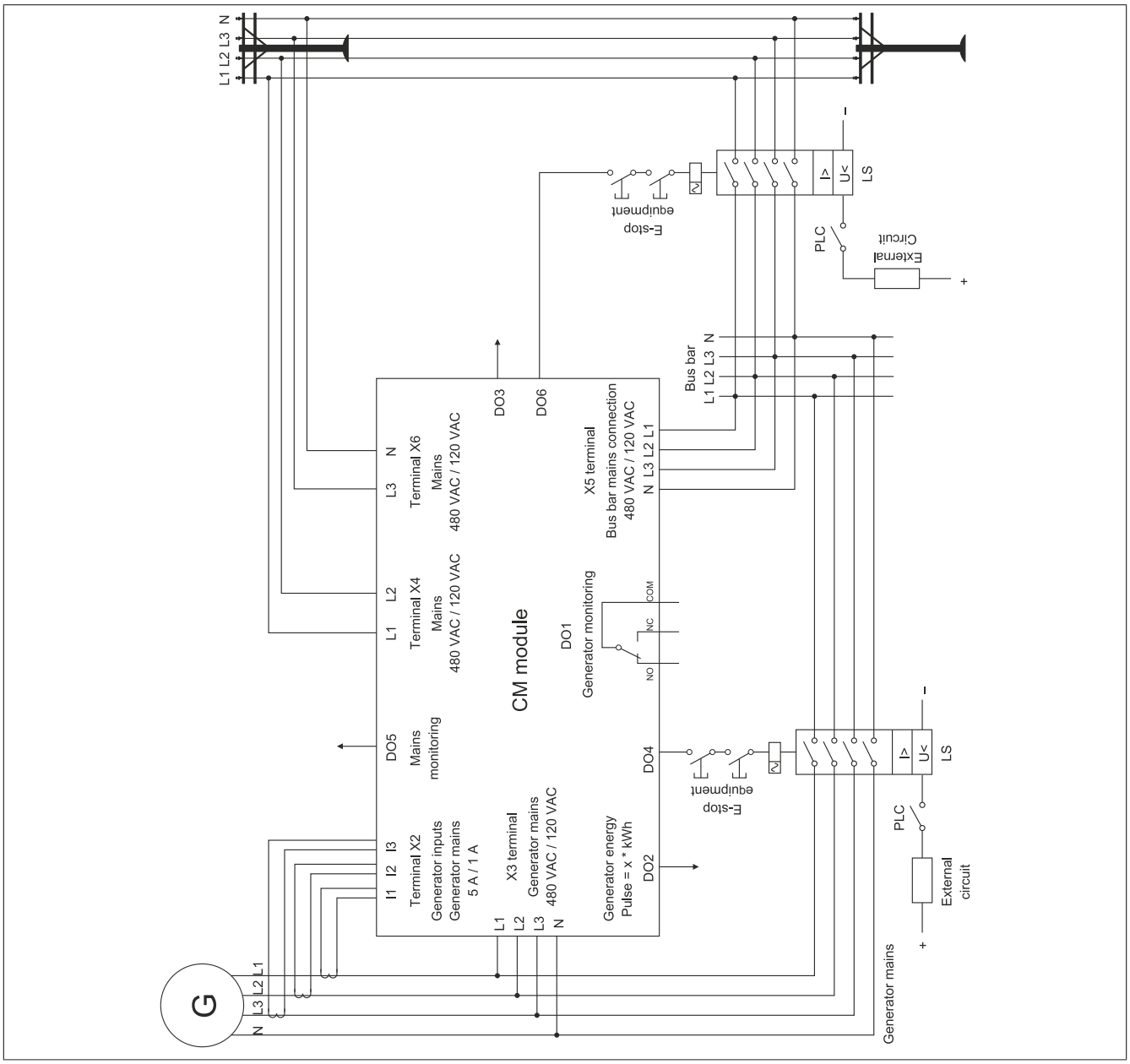


4.26.2.11 Circuit diagram

Example of mains configuration "Sync-mains 1 / Sync-mains 2"



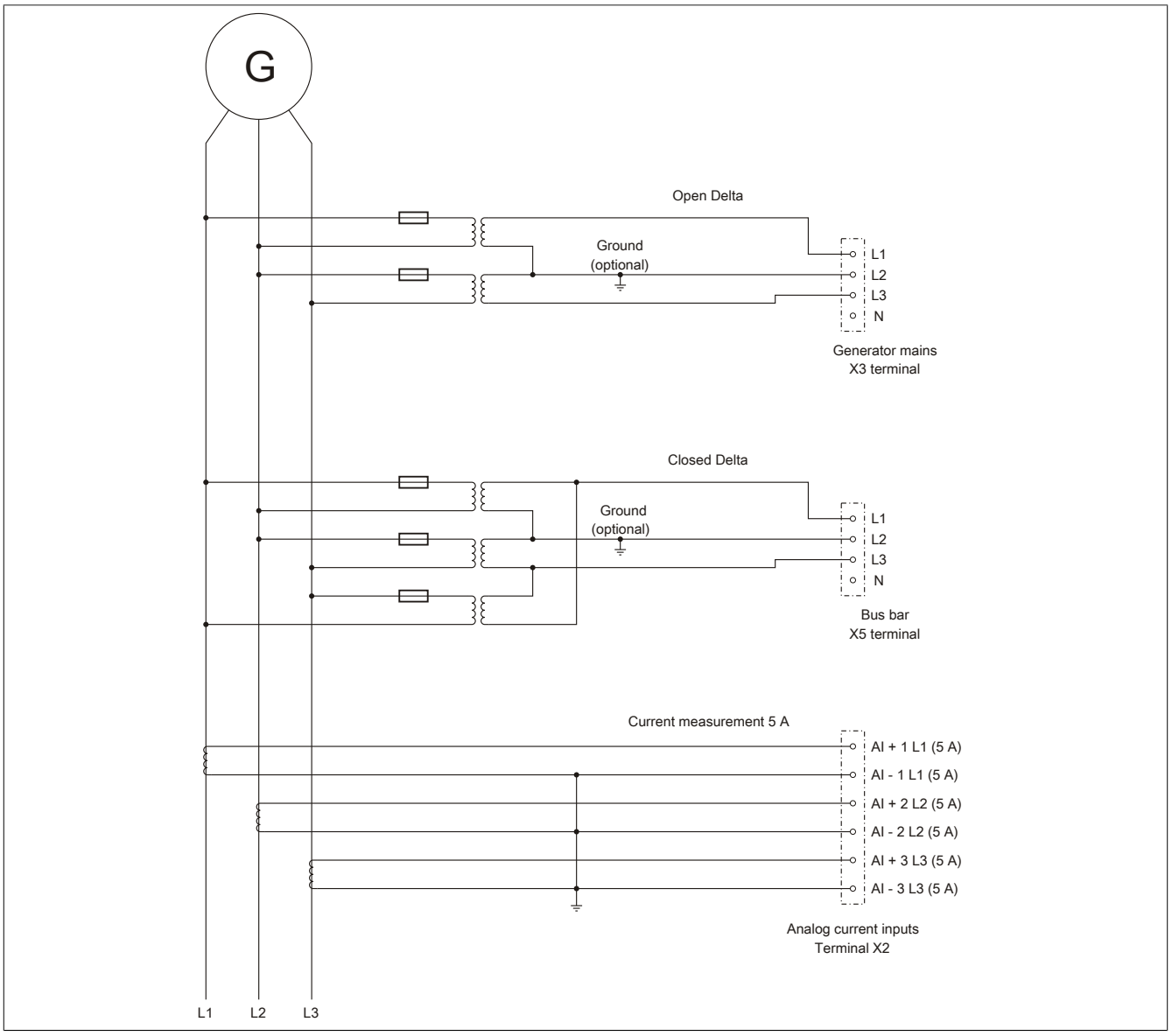
Example of mains configuration "3-phase mains"



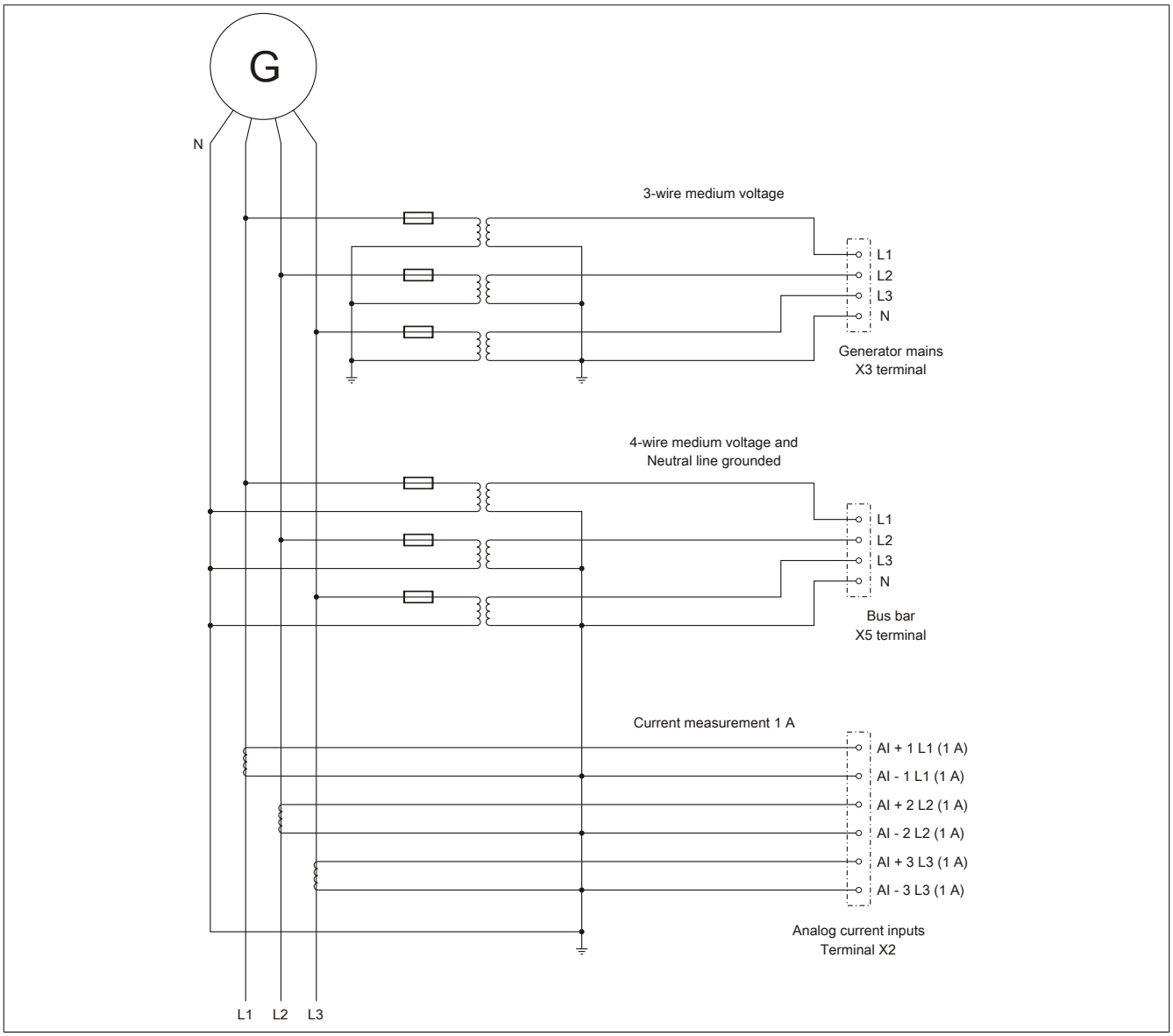
4.26.2.12 Typical connection examples for voltage/current measurement

For power measurement, the X3 terminal must always be used in connection with the X2 terminal! For single-phase measurement, always ensure that current input 1 is used for power measurement if voltage input 1 is being used. Otherwise, accurate power measurement is not possible for this phase!

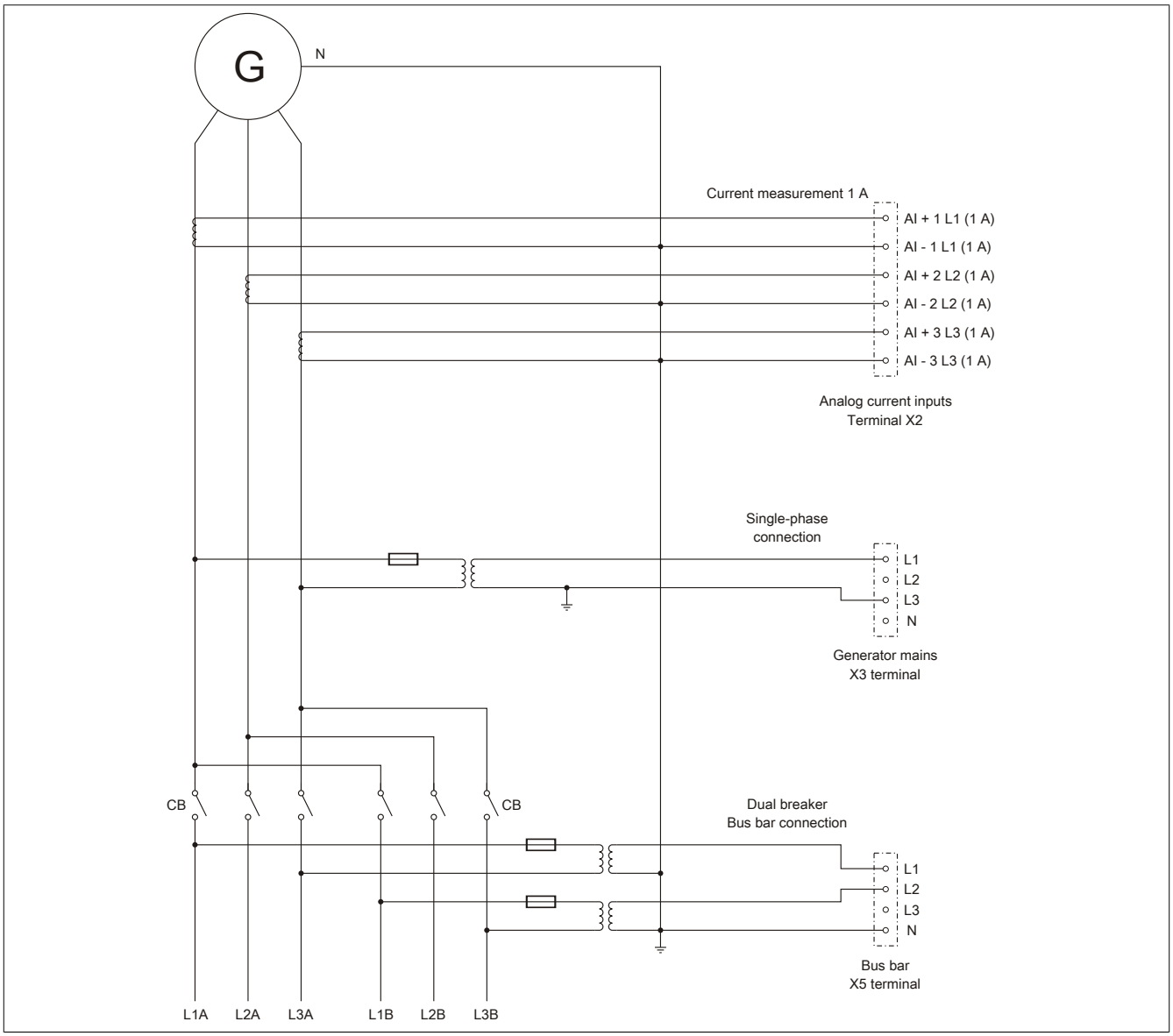
Connection example 1



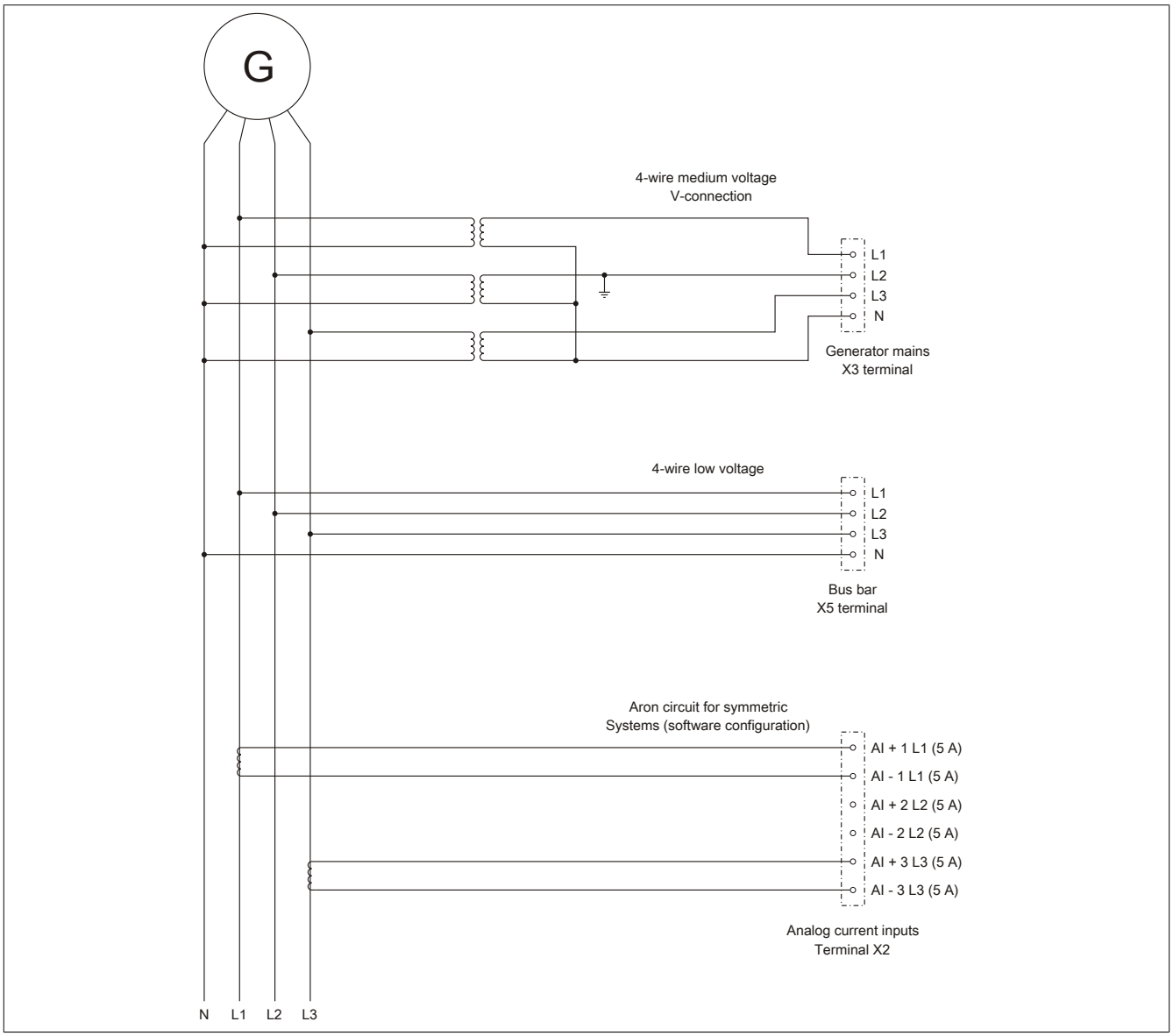
Connection example 2



Connection example 3

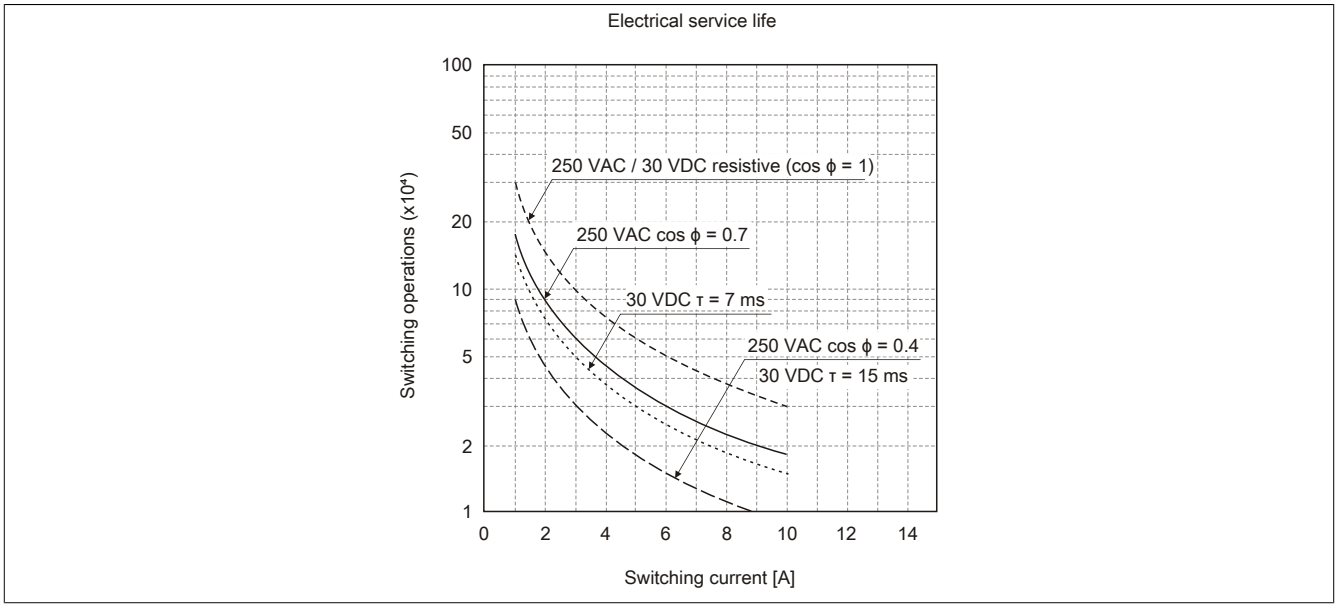


Connection example 4



4.26.2.13 Electrical service life

The electrical service life for the DO1 relay output can be seen in the following diagram.



4.26.2.14 Releasing the locking clip for terminals X3 - X6

Terminals X3 - X6 are equipped with a terminal locking clip. This clip attaches the terminal block securely to the electronic module. This prevents the terminal from accidentally being disconnected.

To release the locking clip, press inwards on the corrugated part of the lever with your fingertip (1) and then slide outwards (2). No additional tools are required for removing the terminal.

Terminals X5 and X6 must be removed first before terminals X3 and X4 can be removed.

4.26.2.15 Synchronization functions

The following three synchronization functions are available on the module:

- Synchronization with slip
- Synchro check
- Switching to voltage-free "dead bus"

Synchronization with slip

The following is valid for synchronization mains 1 and synchronization mains 2:

- 50% < U < 125% of the nominal voltage U_N
- 80% < f < 110% of the nominal frequency f_N

The generator voltage is adjusted to the synchronization voltage with regard to amplitude and frequency. Taking into account the configured phase angle (Δα), a defined transformer vector group and the switching response time, the switch-on command is calculated and transmitted in advance so that the main contacts of the power switch are closed at the point of synchronicity.

Synchronization occurs under the following conditions:

- Synchronization mode "Slip" is set using software.
- The device is ready.
- The phase sequences of the mains networks being synchronized are OK (phase sequence detection).
- The configured limit for voltage difference is not exceeded (ΔU_{max}).
- The configured limits for frequency difference are not exceeded (Δf_{max} and Δf_{min}).
- The configured limit for the phase angle (including vector group transformer Δα) is not exceeded (j_{max}).

When the synchronization mode is set to "Slip", synchronization is not activated until the value of the differential angle between the two synchronized mains networks is >5° for at least 100 ms.

In other words, if the phase difference happens to be within ±5° at the time of the synchronization request, the synchronization won't be activated unless/until the phase difference is larger for 100 ms.

Resetting the mode "Synchronization with slip" cancels the synchronization.

In order to receive a synchronization pulse, the synchronization window must be entered from any phase direction after the synchronization command has been authorized and all of the synchronization conditions specified above are observed.
The switch is not engaged immediately after reaching the phase window. The switch is only engaged if synchronization is possible at the synchronization point while observing the switch lead time.

With very low frequency differences or equivalent frequencies and in adherence to the conditions described above, synchronization will also take place at a phase angle = 0°.

The synchronization output changes its state from Low to High when all conditions are met. It changes back from High to Low after the configured pulse duration has elapsed.

Synchro check

In this operating mode, the device can be used to check the synchronization. The DO4 output remains set as long as the following conditions are met:

- The "-Check" command is set using software.
- The device is ready.
- The phase sequences of the mains networks being synchronized are OK (phase sequence detection).
- The configured limit for voltage difference is not exceeded (ΔU_{max}).
- The configured limits for frequency difference are not exceeded (Δf_{max} and Δf_{min}).
- The defined limit for the phase angle is not exceeded (ϕ_{max}).

DO4 stays at High as long as all conditions are met.

Switching to voltage-free "dead bus"

The switch-on command for the power switch is output without synchronization if the following conditions have been met:

- The "Dead Bus" command is set using software.
- The device is ready.
- The bus bar does not have voltage applied: $U_B < U_{BminSync}$ as a percentage of U_{NomBus}

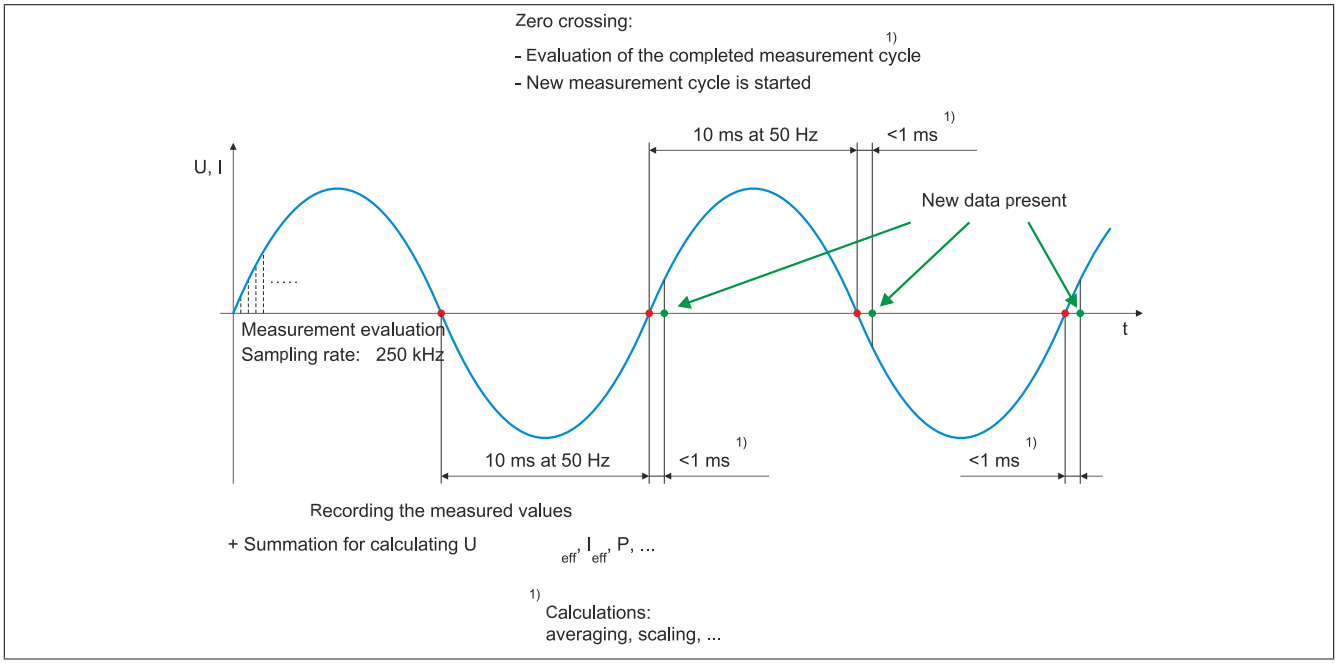
U_B ...	Bus bar phase voltage
$U_{BminSync}$ ...	Dead bus voltage
U_{NomBus} ...	Bus bar nominal voltage

- Frequency measurement of Sync Mains 1 must result in a valid value.

DO4 changes its state from Low to High when all conditions are met. It changes back from High to Low after the configured pulse duration has elapsed.

4.26.2.16 Measurement functions

Timing diagram



Measured parameters for generator mains (X3)

- Phase currents
- Current average
- Dynamic current average
- Neutral current
- Line-to-line voltages
- Phase voltages
- Voltage average
- Total apparent power
- Total reactive power
- Total active power
- Active power factor
- Frequency

Measured parameters between synchronization mains networks

- Differential angle
- Differential voltage

Rating-dependent overcurrent

Rating-dependent overcurrent monitoring is in accordance with the specifications of IEC 255-8 "Electrical relay; Relay for protecting against thermal overload (overload relay)" and IEC 255-17 "Electrical relay; Relay for protecting against the thermal overload of motors (overload relay for motors).

Dependent delayed imbalanced load monitoring

Dependent delayed imbalanced load monitoring protects against imbalanced loads in three-phase generators and three-phase mains. Parameters can be changed to make it possible to match the trigger characteristics to different generator types while taking their special thermal time constants into consideration.

An imbalanced load can be caused by uneven current distribution in the mains due to imbalanced load, asymmetrical short circuits, line interruptions or switching operations. Imbalanced loads result in reverse system currents in the stator, which causes harmonics with an uneven ordinal number in the stator winding and harmonics with an even ordinal number in the rotor winding. The rotor is at particular risk here because the harmonic waves place an additional load on the rotor winding and induce eddy currents in the rotor's solid iron, which may melt the metal or destroy the metallic structure.

An imbalanced load can be permissible within certain limits, however, when accounting for the thermal load limit of the generator. To avoid premature failure of the generator when an imbalanced load occurs, the characteristics that trigger imbalanced load protection should be adapted to the thermal characteristics of the generator. Imbalanced load protection can also be triggered by external errors in the mains caused by asymmetric short circuits.

Short circuit current monitoring

If overcurrent or a short circuit occurs and the limit value is exceeded, the error message "Short circuit current" is signaled after the configured time delay has passed.

Voltage asymmetry monitoring

This trigger value, specified as a percentage, is based on the nominal voltage of the generator. If the difference between the three line-to-line voltages of the generator mains exceeds the set limit value, then the error message "Voltage asymmetry" is signaled after the response time has passed. For this to happen, only one of these voltages has to exceed the respective limit value (in either the positive or negative direction).

Bus bar voltage measurement and zero voltage monitoring

3-phase monitoring takes place for the bus bar voltage. The measured values are represented as phase-to-phase and phase-to-neutral values. The D03 output is set when there is no voltage (below the lower limit of the defined limit bus bar voltage minimum U_{Bmin}) on the bus bar (X5 terminal).

This monitoring can be used to determine which synchronization function should be used.

Synchronization function	Bus bar voltage measurement
Dead bus	No voltage is being supplied to the bus bar or the value is below the lower limit parameter. Output DO3 is set.
Synchronization with slip	The voltage measured on the bus bar is above the defined parameter value. Output DO3 is not set.

Exciter failure

The reactive power monitoring can be used to protect a generator against operating in the impermissible range. The capacitive reactive power monitor offers protection against under-excitation (exciter failure). If the lower limit is exceeded (in the negative direction), the error message "Capacitive reactive power" is signaled after the configured time delay has passed.

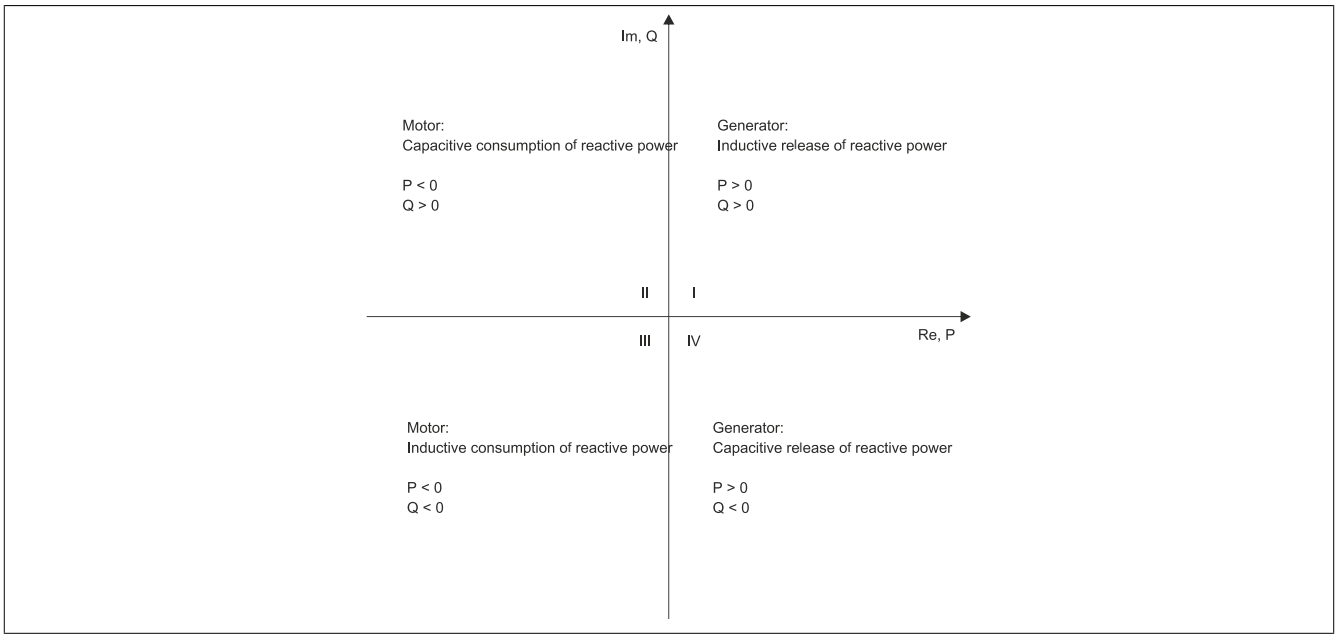
Phase sequence detection

Phase sequence detection is used to detect incorrectly wired voltage and current inputs or if the generator is rotating in the wrong direction (for information about configuration, see register "ConfigOutput24").

Phase sequence L1, L2 and L3 is monitored for this. If not correct, then an error message is output (see register "StatusDigitalOutput") and synchronization cannot take place.

4.26.2.17 Generator operating modes

The operating modes possible for the generator are illustrated in this 4 quadrant diagram.

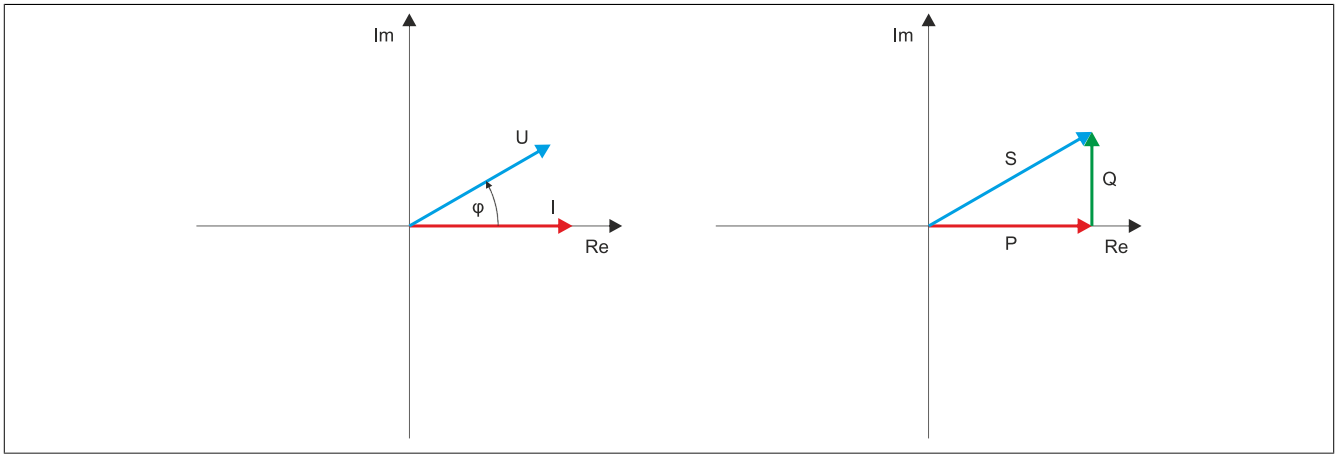


Quadrant I

Generator operation, inductive release of reactive power:

- The active power P and the reactive power Q are greater than 0.
- The phase angle ϕ is between 0 and 90°. This means that U keeps ahead of I.

Example: ϕ = 30°

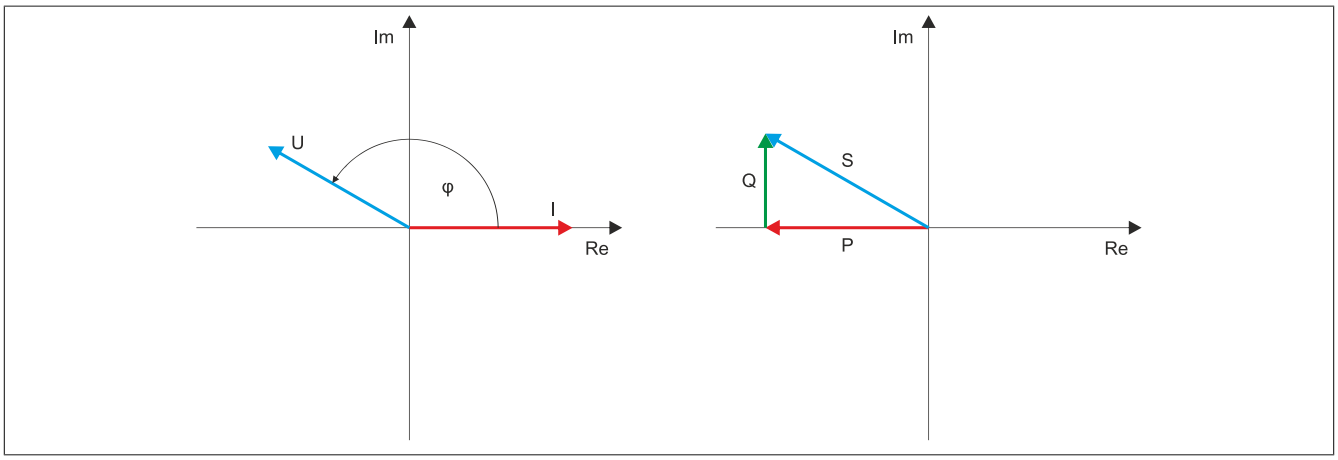


Quadrant II

Motor operation, capacitive reactive power consumption:

- The active power P is less than 0 while the reactive power Q is greater than 0.
- The phase angle ϕ is between 90 and 180°. This means that U keeps ahead of I.

Example: ϕ = 150°

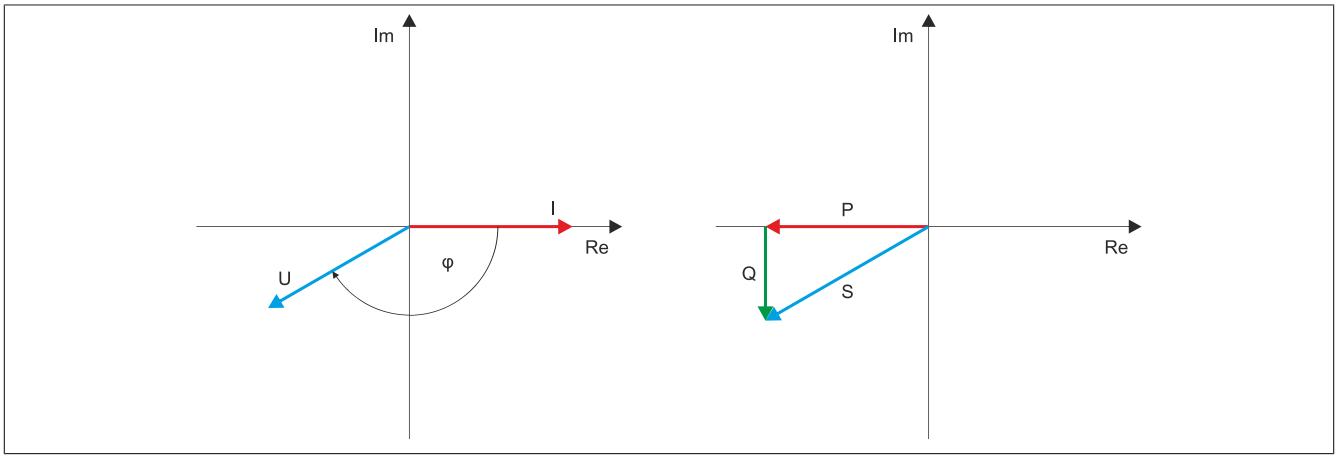


Quadrant III

Motor operation, inductive reactive power consumption:

- The active power P and the reactive power Q are less than 0.
- The phase angle ϕ is between -90 and -180°. This means that U lags behind I.

Example: ϕ = -150°

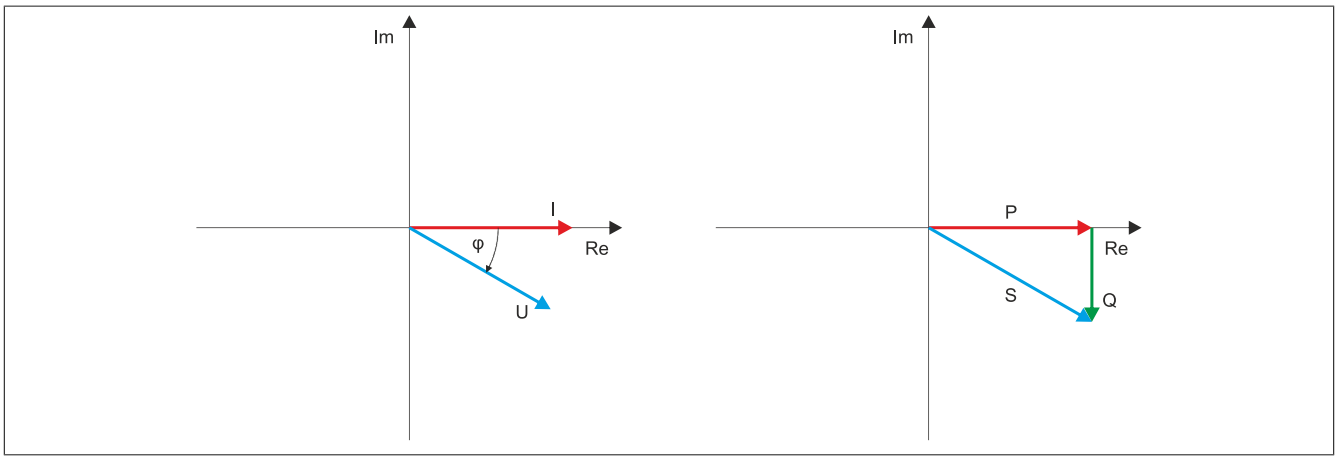


Quadrant IV

Generator operation, capacitive release of reactive power:

- The active power P is greater than 0 while the reactive power Q is less than 0.
- The phase angle ϕ is between 0 and -90°. This means that U lags behind I.

Example: ϕ = -30°



Power factor of the generator

The power factor is a product of the ratio between the active power P and apparent power S. With sinusoidal values, this corresponds to the cosine of the phase shift angle ϕ.

$$\left|Leistungsfaktor\right| = \left|\frac{P}{S}\right|$$

The module derives the sign used for the power factor from the signs used with the P and Q values. In this way, it depends on the generator's operating mode:

Sign	Description
Positive	• Quadrant I or III, P and Q positive or P and Q negative • Inductive release of reactive power or inductive reactive power consumption
Negative	• Quadrant II or IV, P negative and Q positive or P positive and Q negative • Capacitive release of reactive power or capacitive reactive power consumption

4.26.2.18 Register description

4.26.2.18.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.2.18.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
General registers - Configuration						
2762	ConfigOutput68 (Read) Mains settings	UINT		(●)[1)]		●
2561	ConfigOutput20 (Read) Nominal voltage range, nominal current range and Aron circuit	USINT		(●)[1)]		●
2614	ConfigOutput10 (Read) Nominal frequency (f_{Nom})	UINT		(●)[1)]		●
2569	ConfigOutput24 (Read) General configuration register	USINT		(●)[1)]		●
2567	ConfigOutput23 (Read) Trigger bits	USINT		(●)[1)]		●
Generator mains - Configuration						
2582	ConfigOutput02 (Read) Nominal voltage of generator mains (U_{NomGen})	UINT		(●)[1)]		●
2598	ConfigOutput06 (Read) Multiplier for generator mains	UINT		(●)[1)]		●
2590	ConfigOutput04 (Read) Nominal current of generator mains (I_{Nom})	UINT		(●)[1)]		●
2610	ConfigOutput09 (Read) Multiplier for current transformer	UINT		(●)[1)]		●
2563	ConfigOutput21 (Read) Turns generator mains functions on/off	UINT		(●)[1)]		●
2746	ConfigOutput41 (Read) Low-pass filter for total power ratings	UINT		(●)[1)]		●
Generator monitoring functions - Configuration						
2658	ConfigOutput16 (Read) Overvoltage limit of the generator mains (U_{maxGen})	UINT		(●)[1)]		●
2938	ConfigOutput118 (Read) Overvoltage limit 2 of the generator mains (U_{maxGen})	UINT		(●)[1)]		●
2706	ConfigOutput26 (Read) Response time for generator overvoltage (U_{maxGen})	UINT		(●)[1)]		●
2942	ConfigOutput119 (Read) Response time 2 for generator overvoltage (U_{maxGen})	UINT		(●)[1)]		●
2662	ConfigOutput27 (Read) Undervoltage limit of generator mains (U_{minGen})	UINT		(●)[1)]		●
2702	ConfigOutput59 (Read) Undervoltage limit of generator mains 2 ($U_{min2Gen}$)	UINT		(●)[1)]		●
2710	ConfigOutput28 (Read) Response time for generator undervoltage (U_{minGen})	UINT		(●)[1)]		●
2734	ConfigOutput65 (Read) Response time for generator undervoltage 2 ($U_{min2Gen}$)	UINT		(●)[1)]		●
2666	ConfigOutput29 (Read) Generator over-frequency (f_{maxGen})	UINT		(●)[1)]		●
2954	ConfigOutput122 (Read) Generator over-frequency 2 (f_{maxGen})	UINT		(●)[1)]		●
2714	ConfigOutput30 (Read) Response time for generator over-frequency (f_{maxGen})	UINT		(●)[1)]		●
2958	ConfigOutput123 (Read) Response time 2 for generator over-frequency (f_{maxGen})	UINT		(●)[1)]		●
2670	ConfigOutput31 (Read) Generator under-frequency (f_{minGen})	UINT		(●)[1)]		●
2946	ConfigOutput120 (Read) Generator under-frequency 2 (f_{minGen})	UINT		(●)[1)]		●
2718	ConfigOutput32 (Read) Response time for generator under-frequency (f_{minGen})	UINT		(●)[1)]		●
2950	ConfigOutput121 (Read) Response time 2 for generator under-frequency (f_{minGen})	UINT		(●)[1)]		●
2674	ConfigOutput33 (Read) Generator voltage asymmetry (U_{asGen})	UINT		(●)[1)]		●
2722	ConfigOutput34 (Read) Response time for the generator voltage asymmetry (U_{asGen})	UINT		(●)[1)]		●
2742	ConfigOutput35 (Read) Load time constant for current asymmetry	UINT		(●)[1)]		●

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2902	ConfigOutput109 (Read) Unbalanced load constant	UINT		(●)[1)]		●
2962	ConfigOutput124 (Read) Nominal current on generator mains for unbalanced load protection	UINT		(●)[1)]		●
2678	ConfigOutput36 (Read) Maximum limit of neutral conductor current	UINT		(●)[1)]		●
2726	ConfigOutput37 (Read) Response time for neutral conductor current monitoring	UINT		(●)[1)]		●
2682	ConfigOutput38 (Read) Short circuit current	UINT		(●)[1)]		●
2730	ConfigOutput39 (Read) Response time for short circuit current	UINT		(●)[1)]		●
2686	ConfigOutput42 (Read) Rating-dependent overcurrent	UINT		(●)[1)]		●
2690	ConfigOutput43 (Read) Integration coefficient for rating-dependent overcurrent (iths)	UINT		(●)[1)]		●
2694	ConfigOutput44 (Read) Capacitive reactive power	UINT		(●)[1)]		●
2738	ConfigOutput45 (Read) Response time for reactive power monitoring	UINT		(●)[1)]		●
2830	ConfigOutput89 (Read) Generator overload	UINT		(●)[1)]		●
2834	ConfigOutput90 (Read) Response time for generator overload	UINT		(●)[1)]		●
2838	ConfigOutput91 (Read) Generator feedback	UINT		(●)[1)]		●
2842	ConfigOutput92 (Read) Response time for generator feedback	UINT		(●)[1)]		●
	DO1 function					
2698	ConfigOutput57 (Read) Monitoring functions - 1	UINT		(●)[1)]		●
2854	ConfigOutput97 (Read) Monitoring functions - 2	UINT		(●)[1)]		●
Synchronization mains (for mains configuration "Sync mains 1 / Sync mains 2") - Configuration						
2578	ConfigOutput01 (Read) Nominal voltage of synchronization mains (U_{NomSyn})	UINT		(●)[1)]		●
2602	ConfigOutput07 (Read) Multiplier for synchronization mains 1	UINT		(●)[1)]		●
2606	ConfigOutput08 (Read) Multiplier for synchronization mains 2	UINT		(●)[1)]		●
Mains (for mains configuration "3-phase mains") - Configuration						
2578	ConfigOutput01 (Read) Nominal voltage of mains ($U_{NomMains}$)	UINT		(●)[1)]		●
2602	ConfigOutput07 (Read) Multiplier for mains	UINT		(●)[1)]		●
2565	ConfigOutput22 (Read) Enable/disable mains functions	UINT		(●)[1)]		●
Mains monitoring functions (for mains configuration "3-phase mains") - Configuration						
	Mains voltage monitoring					
2766	ConfigOutput73 (Read) Overvoltage limit of the mains ($U_{maxMains}$)	UINT		(●)[1)]		●
2858	ConfigOutput98 (Read) Overvoltage limit 2 of the mains ($U_{maxMains}$)	UINT		(●)[1)]		●
2802	ConfigOutput82 (Read) Response time for mains overvoltage ($U_{maxMains}$)	UINT		(●)[1)]		●
2862	ConfigOutput99 (Read) Response time 2 for mains overvoltage ($U_{maxMains}$)	UINT		(●)[1)]		●
2774	ConfigOutput75 (Read) Mains over-frequency ($f_{maxMains}$)	UINT		(●)[1)]		●
2874	ConfigOutput102 (Read) Mains over-frequency 2 ($f_{maxMains}$)	UINT		(●)[1)]		●
2810	ConfigOutput84 (Read) Response time for mains over-frequency ($f_{maxMains}$)	UINT		(●)[1)]		●
2878	ConfigOutput103 (Read) Response time 2 for mains over-frequency ($f_{maxMains}$)	UINT		(●)[1)]		●
2778	ConfigOutput76 (Read) Mains under-frequency ($f_{minMains}$)	UINT		(●)[1)]		●
2882	ConfigOutput104 (Read) Mains under-frequency 2 ($f_{minMains}$)	UINT		(●)[1)]		●
2814	ConfigOutput85 (Read) Response time for mains under-frequency ($f_{minMains}$)	UINT		(●)[1)]		●
2886	ConfigOutput105 (Read) Response time 2 for mains under-frequency ($f_{minMains}$)	UINT		(●)[1)]		●
2782	ConfigOutput77 (Read) Mains voltage asymmetry ($U_{asMains}$)			(●)[1)]		●
2818	ConfigOutput86 (Read) Response time for the mains voltage asymmetry ($U_{asMains}$)			(●)[1)]		●

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
	Undervoltage monitoring in 2-point mode					
2770	ConfigOutput74 (Read) Undervoltage limit of the mains ($U_{minMains}$)			(●)[1]		●
2866	ConfigOutput100 (Read) Undervoltage limit 2 of the mains ($U_{minMains}$)			(●)[1]		●
2806	ConfigOutput83 (Read) Response time for mains undervoltage ($U_{minMains}$)			(●)[1]		●
2870	ConfigOutput101 (Read) Response time 2 for mains undervoltage ($U_{minMains}$)			(●)[1]		●
	Undervoltage monitoring in 6-point mode					
2770	ConfigOutput74 (Read) Undervoltage limit ($U_{minMains}$) (1st mains)			(●)[1]		●
2866	ConfigOutput100 (Read) Undervoltage limit ($U_{minMains}$) (2nd mains)			(●)[1]		●
2906	ConfigOutput110 (Read) Undervoltage limit ($U_{minMains}$) (3rd mains)			(●)[1]		●
2914	ConfigOutput112 (Read) Undervoltage limit ($U_{minMains}$) (4th mains)			(●)[1]		●
2922	ConfigOutput114 (Read) Undervoltage limit ($U_{minMains}$) (5th mains)			(●)[1]		●
2930	ConfigOutput116 (Read) Undervoltage limit ($U_{minMains}$) (6th mains)			(●)[1]		●
2806	ConfigOutput83 (Read) Response time for mains undervoltage ($U_{minMains}$) (1st mains)			(●)[1]		●
2870	ConfigOutput101 (Read) Response time for mains undervoltage ($U_{minMains}$) (2nd mains)			(●)[1]		●
2910	ConfigOutput111 (Read) Response time for mains undervoltage ($U_{minMains}$) (3rd mains)			(●)[1]		●
2918	ConfigOutput113 (Read) Response time for mains undervoltage ($U_{minMains}$) (4th mains)			(●)[1]		●
2926	ConfigOutput115 (Read) Response time for mains undervoltage ($U_{minMains}$) (5th mains)			(●)[1]		●
2934	ConfigOutput117 (Read) Response time for mains undervoltage ($U_{minMains}$) (6th mains)			(●)[1]		●
	Microgrid monitoring					
2890	ConfigOutput106 (Read) Overvoltage limit of the microgrid ($U_{maxMains}$)	UINT		(●)[1]		●
2894	ConfigOutput107 (Read) Undervoltage limit of the microgrid ($U_{minMains}$)	UINT		(●)[1]		●
2898	ConfigOutput108 (Read) Response time for microgrid limit	UINT		(●)[1]		●
	Phase shift monitoring					
2786	ConfigOutput78 (Read) Maximum phase difference for a single phase	UINT		(●)[1]		●
2790	ConfigOutput79 (Read) Maximum phase difference for three phases	UINT		(●)[1]		●
2826	ConfigOutput88 (Read) Minimum voltage for phase shift monitoring	UINT		(●)[1]		●
	Mains frequency chance					
2794	ConfigOutput80 (Read) Response value for mains frequency change (df/dt)	UINT		(●)[1]		●
2822	ConfigOutput87 (Read) Number of periods for mains frequency change (df/dt)	UINT		(●)[1]		●
	DO5 function					
2798	ConfigOutput81 (Read) DO5 function	UINT		(●)[1]		●
Busbar - Configuration						
2586	ConfigOutput03 (Read) Busbar nominal voltage (U_{NomBus})	UINT		(●)[1]		●
2594	ConfigOutput05 (Read) Multiplier for busbar	UINT		(●)[1]		●
2650	ConfigOutput40 (Read) Minimum busbar voltage (U_{Bmin})	UINT		(●)[1]		●
Synchronization - Configuration						
3	ConfigOutputPacked01 Synchronization mode	USINT			●	
2654	ConfigOutput56 (Read) Synchronization configuration	UINT		(●)[1]		●
2654	ConfigOutput11 (Read) Max. permissible difference frequency (df_{max})	UINT		(●)[1]		●
2630	ConfigOutput12 (Read) Min. permissible difference frequency (df_{min})	UINT		(●)[1]		●
2634	ConfigOutput13 (Read) Max. permissible differential voltage (dU_{max})	UINT		(●)[1]		●
2638	ConfigOutput14 (Read) Max. permissible differential angle (ϕ_{max})	UINT		(●)[1]		●

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2618	ConfigOutput15 (Read) Phase shift of sync mains 1 (dα)	UINT		(●)[1)]		●
2754	ConfigOutput47 (Read) Pulse duration of switch-on relay on DO4	UINT		(●)[1)]		●
2758	ConfigOutput48 (Read) Switching response time of power switch on DO4	UINT		(●)[1)]		●
2642	ConfigOutput95 (Read) Pulse duration of switch-on relay on DO6	UINT		(●)[1)]		●
2646	ConfigOutput96 (Read) Switching response time of power switch on DO6	UINT		(●)[1)]		●
2622	ConfigOutput58 (Read) Dead bus voltage ($U_{BminSync}$)	UINT		(●)[1)]		●
2846	ConfigOutput93 (Read) 2-phase synchronization for commissioning tests	UINT		(●)[1)]		●
Maximum value buffer and power meter - Configuration						
2750	ConfigOutput46 (Read) Pulse value of energy meter output	UINT		(●)[1)]		●
2850	ConfigOutput94 (Read) Count value for active energy meter and reactive energy meter	UINT		(●)[1)]		●
3074	ConfigOutput49 Maximum phase current of generator I1	INT		●		
	ConfigOutput60 Reset maximum phase current I1	INT				●
3078	ConfigOutput50 Maximum phase current I2	INT		●		
	ConfigOutput61 Reset maximum phase current I2	INT				●
3082	ConfigOutput51 Maximum phase current I3	INT		●		
	ConfigOutput62 Reset maximum phase current I3	INT				●
3086	ConfigOutput52 Maximum total active power	INT		●		
	ConfigOutput63 Resets maximum total active power	INT				●
3090	ConfigOutput53 Maximum neutral conductor current	INT		●		
	ConfigOutput64 Resets maximum neutral conductor current	INT				●
3108	ConfigOutput54 Active energy meter for supply	DINT		●		
	ConfigOutput66 Write to active energy meter for supply	DINT				●
3124	ConfigOutput55 Reactive energy meter for supply	DINT		●		
	ConfigOutput67 Write to reactive energy meter for supply	DINT				●
3116	ConfigOutput71 Active energy meter for reference	DINT		●		
	ConfigOutput69 Write to active energy meter for reference	DINT				●
3132	ConfigOutput72 Reactive energy meter for reference	DINT		●		
	ConfigOutput70 Write to reactive energy meter for reference	DINT				●
General registers - Communication						
1	DigitalOutputPacked01 Digital outputs 05 - 06 and various control bits	USINT			●	
	DigitalOutput05	Bit 0				
	DigitalOutput06	Bit 1				
	ResetGeneratorErrors	Bit 2				
	ResetMainsErrors	Bit 3				
	InvertDO5	Bit 4				
165	StatusDigitalOutputPacked01 Status of digital outputs	USINT	●			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput06	Bit 5				
	StatusInput17	Bit 6				
	StatusInput16	Bit 7				
162	StatusInputPacked01 Generator mains error registers	UINT	●			
	StatusInput01	Bit 0				
	...	...				
	StatusInput11	Bit 10				
	StatusInput31	Bit 11				
	StatusInput32	Bit 12				
	StatusInput18	Bit 15				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
167	StatusInputPacked02 Power mains error registers	USINT	•			
	StatusInput24	Bit 0				
	...	...				
	StatusInput30	Bit 6				
	StatusInput33	Bit 7				
186	StatusInputPacked03 General error registers	UINT	•			
	StatusInput12	Bit 0				
	...	...				
	StatusInput15	Bit 3				
	StatusInput19	Bit 4				
	...	...				
	StatusInput23	Bit 7				
190	StatusInputPacked04 Power mains error registers (continued)	UINT	•			
	StatusInput34	Bit 0				
	...	...				
	StatusInput37	Bit 4				
194	StatusInputPacked05 Generator mains error registers (continued)	UINT	•			
	StatusInput38	Bit 0				
	...	...				
	StatusInput40	Bit 2				
Generator mains measured values - Communication						
30	AnalogInput01 Phase current I1	INT	•			
34	AnalogInput02 Phase current I2	INT	•			
38	AnalogInput03 Phase current I3	INT	•			
42	AnalogInput04 Current average I1, I2, I3	INT	•			
46	AnalogInput05 Neutral conductor current In	INT	•			
170	AnalogInput06 Current average, dynamic (Im_dyn)	UINT	•			
2	AnalogInput07 Line-to-line voltage UG12	INT	•			
6	AnalogInput08 Line-to-line voltage UG23	INT	•			
10	AnalogInput09 Line-to-line voltage UG31	INT	•			
18	AnalogInput10 Phase voltage UG1	INT	•			
22	AnalogInput11 Phase voltage UG2	INT	•			
26	AnalogInput12 Phase voltage UG3	INT	•			
14	AnalogInput22 Voltage average UG12, UG23, UG31	INT	•			
174	AnalogInput19 Total active power filtered P/P_H1	INT	•			
178	AnalogInput20 Total reactive power filtered Q/Q_H1	INT	•			
182	AnalogInput21 Total apparent power filtered Q/S_H1	INT	•			
54	AnalogInput23 Power factor of generator/cos ϕ	INT	•			
50	AnalogInput24 Frequency of the generator mains	UINT	•			
	Timestamp for generator voltages and currents					
772	AnalogInput38 Timestamp of pos. zero crossing of phase voltage UG1	DINT	•			
780	AnalogInput39 Timestamp of pos. zero crossing of phase voltage UG2	DINT	•			
788	AnalogInput40 Timestamp of pos. zero crossing of phase voltage UG3	DINT	•			
796	AnalogInput41 Timestamp of pos. zero crossing of phase current I1	DINT	•			
804	AnalogInput42 Timestamp of pos. zero crossing of phase current I2	DINT	•			
812	AnalogInput43 Timestamp of pos. zero crossing of phase current I3	DINT	•			
Generator monitoring functions - Communication						
3330	AnalogInput36 Read unbalanced load meter	UINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
3334	AnalogInput37 Read unbalanced load current I2	INT		•		
Measured values for busbar - Communication						
82	AnalogInput13 Line-to-line voltage of busbar UB12	INT	•			
86	AnalogInput14 Line-to-line voltage of busbar UB23	INT	•			
90	AnalogInput15 Line-to-line voltage of busbar UB31	INT	•			
94	AnalogInput16 Phase voltage of busbar UB1	INT	•			
98	AnalogInput17 Phase voltage of busbar UB2	INT	•			
102	AnalogInput18 Phase voltage of busbar UB3	INT	•			
106	AnalogInput35 Frequency of busbar	UINT	•			
Measured values for synchronization mains (for "Sync mains 1 / Sync mains 2" mains configuration) - Communication						
114	AnalogInput25 Line-to-line voltage of sync mains 1 US1	INT	•			
134	AnalogInput26 Line-to-line voltage of sync mains 2 US2	INT	•			
138	AnalogInput27 Frequency of sync mains 1	UINT	•			
142	AnalogInput28 Frequency of sync mains 2	UINT	•			
Power mains measured values (for "3-phase mains" configuration)						
114	AnalogInput25 Line-to-line voltage of power mains UN12	INT	•			
118	AnalogInput31 Line-to-line voltage of power mains UN23	INT	•			
122	AnalogInput32 Line-to-line voltage of power mains UN31	INT	•			
126	AnalogInput33 Phase voltage of power mains UN1	INT	•			
130	AnalogInput34 Phase voltage of power mains UN2	INT	•			
134	AnalogInput26 Phase voltage of power mains UN3	INT	•			
138	AnalogInput27 Frequency of power mains	UINT	•			
Synchronization - Communication						
146	AnalogInput29 Differential angle between sync mains	INT	•			
150	AnalogInput30 Differential voltage between sync mains	INT	•			

1) This configuration register has a dual design. The register with "Read" in the name allows the configured value to be read back.

4.26.2.18.3 Configuration registers

4.26.2.18.3.1 General registers

Mains settings

Name:
ConfigOutput68
ConfigOutput68Read

This register is used to configure the module on the connected mains.

The value of this register can be read back.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Generator mains configuration	00	3-phase mains with neutral conductor (default)
		01	3-phase mains without neutral conductor
		10 to 11	Reserved
2 - 3	Busbar configuration	00	3-phase mains with neutral conductor (default)
		01	3-phase mains without neutral conductor
		10 to 11	Reserved
4 - 5	Mains configuration	00	3-phase mains with neutral conductor (default)
		01	3-phase mains without neutral conductor
		10	Sync Mains 1 / Sync Mains 2 (default)
		11	Reserved
6 - 7	Reserved	0	
8 - 9	Generator mains ground	00	No phases grounded
		01	L1 grounded
		10	L2 grounded
		11	L3 grounded
10 - 11	Busbar ground	00	No phases grounded
		01	L1 grounded
		10	L2 grounded
		11	L3 grounded
12 - 13	Sync Mains 1 ground	00	No phases grounded
		01	L1 grounded
		10	L2 grounded
		11	L3 grounded
14 - 15	Sync Mains 2 ground	00	No phases grounded
		01	L1 grounded
		10	L2 grounded
		11	L3 grounded

Mains without neutral conductor

If configured as "3-phase mains without neutral conductor", the potential of the neutral conductor is calculated from the 3 phases ("virtual neutral point").

The phase voltages are then measured in relation to this "virtual neutral point".

Mains with ground

If one of the phases of a mains system is grounded, then it must be configured as such. Otherwise, it is possible that the module will report a phase failure that blocks the mains synchronization function.

Monitoring functions disabled:

- Phase failure monitoring is not carried out for the phase configured as "grounded".
- Phase sequence monitoring is not performed on 2-phase mains that are grounded.

Mains configuration

The mains can be used as two 2-phase synchronization mains or combined into a 3-phase mains.

If the mains configuration is set to "3-phase mains" then the monitoring functions will be enabled for these combined mains.

Nominal voltage range, nominal current range and Aron circuit

Name:
ConfigOutput20
ConfigOutput20Read

The value of this register can be read back.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Nominal voltage range of generator mains	0	Voltage 100 V
		1	Voltage 400 V
1	Nominal voltage range of busbar	0	Voltage 100 V
		1	Voltage 400 V
2	Nominal voltage range of Sync Mains 1	0	Voltage 100 V
		1	Voltage 400 V
3	Nominal voltage range of Sync Mains 2	0	Voltage 100 V
		1	Voltage 400 V
4	Nominal current range of the generator mains	0	Current range 1 A
		1	Current range 5 A
5	Switch to power measurement principle of Aron circuit	0	Aron circuit disabled: Three-phase supply with neutral line
		1	Aron circuit enabled: Three-phase supply without neutral line
6 - 7	Reserved	0	

Nominal frequency (f_{Nom})

Name:
ConfigOutput10
ConfigOutput10Read

This is needed for converting the percentages based on this nominal value into physical units.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	4800 to 6200	corresponds to 48 to 62 Hz.	0.01 Hz

General configuration register

Name:
ConfigOutput24
ConfigOutput24Read

The value of this register can be read back.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	DO5 function	00	DO5 is freely available to the user
		01	Monitoring output of the mains
		10	DO5 is freely available to the user or can be used as a mains monitoring output (the two signals are linked with an OR)
		11	Reserved
2 - 3	DO6 function	00	DO6 is freely available to the user
		01	Synchronization output (control of power switch)
		10 to 11	Reserved
4	Definition of rotational direction monitoring of all mains	0	Right rotating field
		1	Left rotating field
5 - 7	Reserved	0	

Trigger bits

Name:
ConfigOutput23
ConfigOutput23Read

The value of this register can be read back.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reset unbalanced load meter	0	Unbalanced load meter not set to 0
		1	On rising edge: Unbalanced load meter set to 0
1 - 7	Reserved	0	

4.26.2.18.3.2 Generator mains

Nominal voltage of generator mains (U_{NomGen})

Name:
ConfigOutput02
ConfigOutput02Read

This is needed for converting the percentages based on this nominal value into physical units.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	70 to 65000	Corresponds to 70 to 65000 V	1 V

Multiplier for generator mains

Name:
ConfigOutput06
ConfigOutput06Read

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

The value 100 corresponds to a multiplication factor of 1 (measured value not changed).

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 65535	Corresponds to 0.01 to 655.35	0.01

Nominal current of generator mains (I_{Nom})

Name:
ConfigOutput04
ConfigOutput04Read

This is needed for converting the percentages based on this nominal value into physical units.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 65000	Corresponds to 0 to 65000 A	1 A

Multiplier for current transformer

Name:
ConfigOutput09
ConfigOutput09Read

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 65535	Corresponds to 1 to 65535	1

Turns generator mains functions on/off

Name:
ConfigOutput21
ConfigOutput21Read

The value of this register can be read back.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Error acknowledgment mode	0	Error bits are reset by the module
		1	Error bits are reset by the user
2 - 3	Check all overvoltages and undervoltages[1)]	00	3 line-to-line voltages (default)
		01	3 phase voltages
		10	3 line-to-line and 3 phase voltages
		11	Reserved
4 - 5	Reserved	0	
6	Power measurement mode[2)]	0	Total output - Including the harmonic component (default)
		1	Fundamental power - 1st harmonic only
7	Reserved	0	

1) This parameter is supported starting with upgrade 1.6.0.0 (firmware version 102). For information about configuring limit values, see section 4.26.2.18.3.3 "Generator monitoring".
2) This parameter is supported starting with upgrade 1.5.0.0 (firmware version 101).

Power measurement mode

In real transmission networks, neither the voltages nor the currents are strictly sinusoidal. This means: The fundamental frequencies are generally subject to strong harmonics.

By default, the module always accounts for the contributions of the fundamental frequency as well as the harmonics. In addition to the voltage and current measured values, this also affects the power measurements.

When controlling with reactive power in applications, the part of the reactive power coming from the harmonic frequencies (distortion reactive power) can have negative effects. Only the displacement reactive power should be controlled (i.e. the reactive power component of the fundamental frequency). In particular, this can make a control to displacement reactive power = 0 (cos φ = 1) impossible.

This is why the module offers the possibility of accounting for only the fundamental frequency (1st harmonic) for power measurement, when necessary. This primarily serves to filter out the distortion reactive power. However, all other measured values associated with the power measurement as well as the corresponding generator protection functions are affected when re-configuring the power measurement to the fundamental frequency.

The voltage and current measured values from the generator mains are **not** affected. Just as before (as with the other voltage supply systems), they also always include the contribution of harmonics regardless of the mode being used for power measurement.

Measured value / Functionality	Corresponding data point	Corresponding output	Remarks/Details
Active power	AnalogInput19		P → P_H1
Reactive power	AnalogInput20		Q → Q_H1
Apparent power	AnalogInput21		S → S_H1
Power factor	AnalogInput23		Power factor -> cos φ |cos φ| = cos(arctan(Q_H1/P_H1)) The signs for cos φ are described in section 4.26.2.17 "Generator operating modes". "I" and "U" must be replaced by the respective 1st harmonics "I_H1" and "U_H1".
Maximum total active power	ConfigOutput52		Changing the parameter "Power measurement mode" during runtime has no immediate effect on any of these registers or the internal energy meters (e.g. meter reset). It only determines the summands or comparison value that is effective immediately (total output / fundamental frequency power).
Active energy meter for supply	ConfigOutput54		
Reactive energy meter for supply	ConfigOutput55		
Active energy meter for reference	ConfigOutput71		
Reactive energy meter for reference	ConfigOutput72		
Energy meter output		DO 2	
Generator monitoring function: Capacitive reactive power	StatusInput10	DO 1	
Generator monitoring function: Generator overload	StatusInput31	DO 1	
Generator monitoring function: Generator feedback	StatusInput32	DO 1	

Low-pass filter for total power ratings

Name:
ConfigOutput41
ConfigOutput41Read

Parameter for delay time of the low-pass filter of the total power values P, Q and S or P_H1, Q_H1 and S_H1 (see "Power measurement mode"). The maximum total power values are recorded independently of this without being filtered.

This parameter is used as a delay element so that current or voltage fluctuations have less effect on how the calculated power values are represented. The damping behavior of the low-pass filter acts in accordance with the configurable time constant of a decaying e-function.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 300	Corresponds to 0 to 300 ms	1 ms

4.26.2.18.3.3 Generator monitoring

Overvoltage limit of generator mains (Umax)

Name:
ConfigOutput16 (1st value)
ConfigOutput118 (2nd value)
ConfigOutput16Read (1st value)
ConfigOutput118Read (2nd value)

If the value of one of the generator voltages configured in the "ConfigOutput21" register exceeds the value set here, then the "Overvoltage" error message (register "StatusInputPacked01") or "Overvoltage2" (register "StatusInput-Packed05") is indicated after the delay time has expired and, if configured, the DO1 monitoring relay is switched.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	Corresponds to 0 to 200% of U_{NomGen}	0.1%

Response time for generator overvoltage (U_{max})

Name:
ConfigOutput26 (1st time)
ConfigOutput119 (2nd time)
ConfigOutput26Read (1st time)
ConfigOutput119Read (2nd time)

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	Corresponds to 0.5 to 10 s	0.1 s

Undervoltage limit of generator mains (U_{min})

Name:
ConfigOutput27 (1st value)
ConfigOutput59 (2nd value)
ConfigOutput27Read (1st value)
ConfigOutput59Read (2nd value)

If the value of one of the generator voltages configured in the "ConfigOutput21" register falls below the value set here, then the "Undervoltage" or "Undervoltage2" error message (register "StatusInputPacked01") is indicated after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	Corresponds to 0 to 200% of U_{NomGen}	0.1%

Response time for generator undervoltage (U_{min})

Name:
ConfigOutput28 (1st time)
ConfigOutput65 (2nd time)
ConfigOutput28Read (1st time)
ConfigOutput65Read (2nd time)

The error is only triggered if the response value is exceeded in the negative direction without interruption for as long as is specified in this register.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	Corresponds to 0.5 to 10 s	0.1 s

Generator over-frequency (f_{max})

Name:
ConfigOutput29 (1st frequency)
ConfigOutput122 (2nd frequency)
ConfigOutput29Read (1st frequency)
ConfigOutput122Read (2nd frequency)

If the value of the generator frequency exceeds the percent value set here in relation to the nominal frequency, then the error message "Overfrequency" (register "StatusInputPacked01") or "Overfrequency 2" (register "StatusPacked05") is indicated after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of f_{Nom}	0.1%

Response time for generator over-frequency (f_{max})

Name:
ConfigOutput30 (1st time)
ConfigOutput123 (2nd time)
ConfigOutput30Read (1st time)
ConfigOutput123Read (2nd time)

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 for 10 s	0.1 s

Generator under-frequency (f_{min})

Name:
ConfigOutput31 (1st frequency)
ConfigOutput120 (2nd frequency)
ConfigOutput31Read (1st frequency)
ConfigOutput120Read (2nd frequency)

If the value of the generator frequency falls below the percent value set here in relation to the nominal frequency, then the error message "Underfrequency" (register "StatusInputPacked01") or "Underfrequency 2" (register "StatusInputPacked05") is indicated after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of f_{Nom}	0.1%

Response time for generator under-frequency (f_{min})

Name:
ConfigOutput32 (1st time)
ConfigOutput121 (2nd time)
ConfigOutput32Read (1st time)
ConfigOutput121Read (2nd time)

The error is only triggered if the response value is exceeded in the negative direction without interruption for as long as is specified in this register.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

Generator voltage asymmetry (U_{as})

Name:
ConfigOutput33
ConfigOutput33Read

This trigger value, specified as a percentage, is based on the nominal voltage of the generator. If the difference between the three line-to-line voltages of the generator mains exceeds the configured limit value, then the error message "Voltage asymmetry" is indicated (register "StatusInputPacked01") after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

For this to happen, only one of these voltages has to exceed the respective limit value (in either the positive or negative direction).

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 300	For 0 to 30% of U_{NomGen}	0.1%

Response time for generator voltage asymmetry (U_{as})

Name:
ConfigOutput34
ConfigOutput34Read

This error is triggered only if the response value is exceeded without interruption (in either the positive or negative direction) for as long as is specified in this register.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

Load time constant for current asymmetry (K1)

Name:
ConfigOutput35
ConfigOutput35Read

The dependent delayed unbalanced load monitoring function (see "Dependent delayed unbalanced load monitoring") continually monitors the AC currents coming from the main current converters and continually calculates the present unbalanced load current. This is compared with the threshold value, which is calculated using the load time constants. If this threshold value is exceeded, the error message "Current asymmetry" is indicated (register "StatusInputPacked01") and, if configured, the DO1 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 65535	For 0.1 to 6553.5 s	0.1 s

Unbalanced load constant (K2)

Name:
ConfigOutput109
ConfigOutput109Read

The boundary between continuous operation and short-term operation is defined by the unbalanced load constant K2 (see "Dependent delayed unbalanced load monitoring").

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	8 to 15	For 0.08 to 0.15 (default: 0.08)	0.01

Dependent delayed unbalanced load monitoring

Unbalanced load monitoring protects against unbalanced load in three-phase generators and three-phase mains. Parameters can be changed to make it possible to match the trigger characteristics to different generator types while taking their special thermal time constants into consideration.

An unbalanced load can be caused by uneven current distribution in the mains due to unbalanced load, asymmetrical short circuits, line interruptions or switching operations. Unbalanced loads result in reverse system currents in the stator, which causes harmonics with an uneven ordinal number in the stator winding and harmonics with an even ordinal number in the rotor winding. The rotor is at particular risk here because the harmonic waves place an additional load on the rotor winding and induce eddy currents in the rotor's solid iron, which may melt the metal or destroy the metallic structure.

An unbalanced load can be permissible within certain limits, however, when accounting for the thermal load limit of the generator. To avoid premature failure of the generator when an unbalanced load occurs, the characteristics that trigger unbalanced load protection should be adapted to the thermal characteristics of the generator. Unbalanced load protection can also be triggered by external errors in the mains caused by asymmetric short circuits.

When unbalanced load protection is tripped can be calculated using the following formula:

Operating mode	Formula
Short-term operation	$t = \frac{K1}{(\frac{I_2}{I_{Nom}})^2 - K2^2}$
Continuous operation	$\frac{I_2}{I_{Nom}} \leq K2 \rightarrow t = \infty$

Key	
t	Calculated tripping time
K1	Valid load time constant for the generator [s]
K2	Unbalanced load constant
I_2	Calculated inverse current / unbalanced load current [A]
I_{Nom}	Nominal current for the generator [A]

To calculate the tripping time instant, the scan duration of the measurement system (i.e. 20 ms for 50 Hz voltage) is divided by the calculated trigger time, and the results are continually added up. With short-term operation, the value of the summands increases; with continuous operation, it decreases. If the summand reaches the value 1 (100%), then the max. permitted value has been reached. The summand is limited between 0 and 1.

The boundary between continuous operation and short-term operation is defined by the unbalanced load constant K2.

Information:

When the generator is at a standstill, the summand is neither reset nor is its value reduced.

Nominal current on generator mains for unbalanced load protection

Name:
ConfigOutput124
ConfigOutput124Read

The nominal current for unbalanced load protection can be set separately. If the value is set to 0 (default), the normal nominal current is used for calculations.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 65000	For 0 to 65000 A	1 A

Maximum limit of neutral conductor current

Name:
ConfigOutput36
ConfigOutput36Read

Configurable limit for the neutral conductor current. If the value is exceeded, then the error message "Maximum neutral conductor current" is indicated (register "StatusInputPacked01") after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 1000	For 0 to 100% of I_{Nom}	0.1%

Response time for neutral conductor current monitor

Name:
ConfigOutput37
ConfigOutput37Read

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

Short circuit current

Name:
ConfigOutput38
ConfigOutput38Read

If the value of the generator current exceeds the percentage based on the converter's nominal current set here, then the error message "Short circuit current" is indicated (register "StatusInputPacked01") and, if configured, the DO1 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1000 to 5000	For 100 to 500% of I_{Nom}	0.1%

Response time for short circuit current

Name:
ConfigOutput39
ConfigOutput39Read

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	4 to 500	For 0.04 to 5 s	0.01 s

Rating-dependent overcurrent

Name:
ConfigOutput42
ConfigOutput42Read

The response value percentage is based on the nominal current of the generator. If the response value is exceeded, then the error message "Rating-dependent overcurrent" is indicated (register "StatusInputPacked01") and, if configured, the DO1 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1000 to 2000	For 100 to 200% of I_{Nom}	0.1%

Rating-dependent overcurrent monitoring

A generator that is operated at its nominal current I_{Nom} normally reaches about half of its maximum thermal load. Operating it above the rated current I_{Nom} result in additional warming, which is permitted until the maximum temperature is reached. The highest permissible continuous temperature is determined by the class of the insulation material used in the generator.

Based on the settings and the current measurement, the device forms an internal model based on an I^2t characteristic curve of the generator temperature. This allows the heat capacity of the generator to be completely utilized for short overloads while at the same time providing full protection. The configurable parameters for determining the machine model include the nominal current I_{Nom} of the generator and the time multiplier.

Integration coefficient for rating-dependent overcurrent (iths)

Name:
ConfigOutput43
ConfigOutput43Read

To calculate the tripping time instant, the sampling duration of the measurement system is divided by the calculated trigger time (t). The results are continually added up. If the summand reaches the value 1 (100%), then the max. permitted value has been reached. The summand is limited between 0 and 1.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 20	For 0.1 to 2	0.1

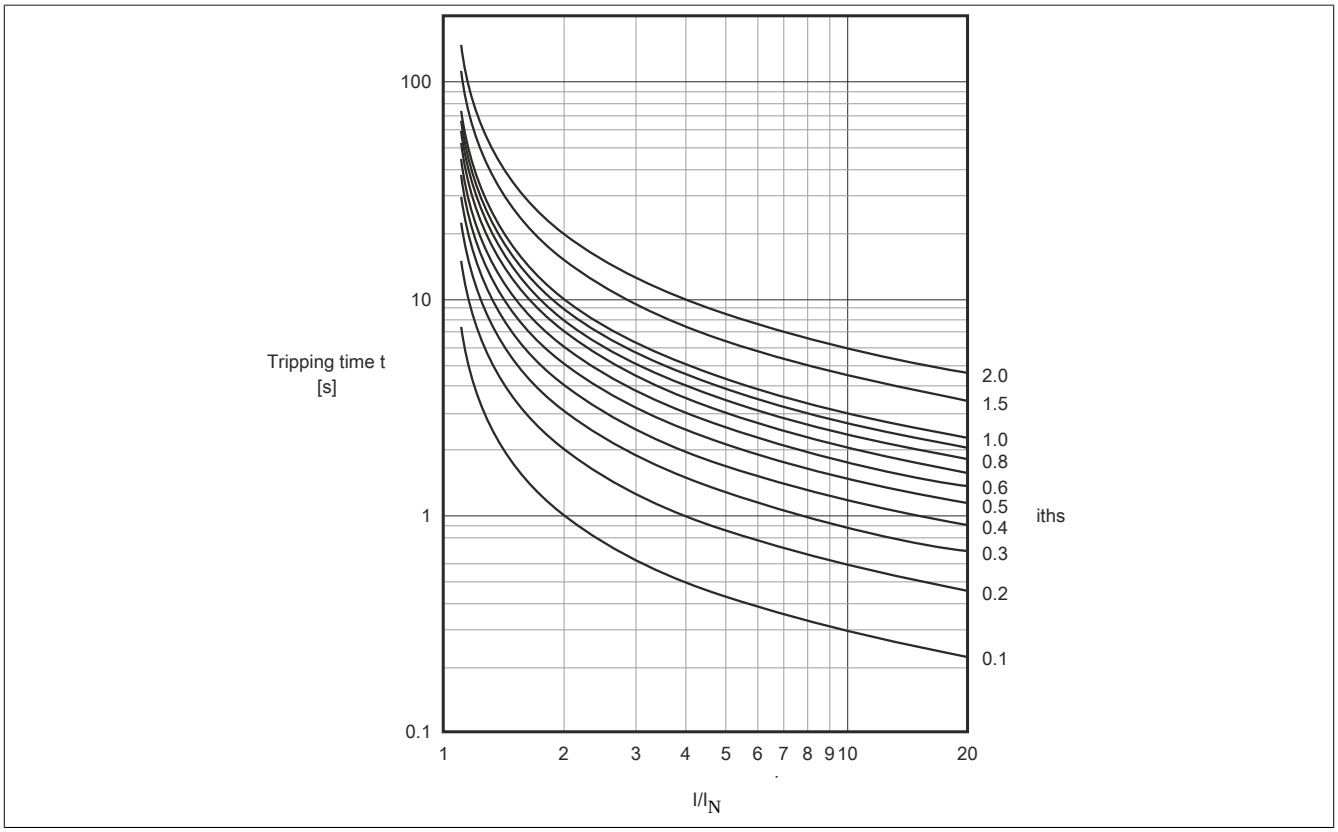
For a constant overcurrent, the trigger characteristic curve can be calculated based on the following formula:

$$t = \frac{0.14}{\left(\frac{I}{I_N}\right)^{0.02} - 1} * iths$$

Key:

t	Tripping time [s]
I	The highest value of the 3 phase currents [A]
I_N	Rating-dependent overcurrent [A]
iths	Integration coefficient

Trigger characteristic curve in accordance with IEC 255-4 (normal, inverse)



The monitor function can be reset by restarting the module or by falling below the overcurrent value so that the results of the continuous addition decrease according to the formula.

Capacitive reactive power

Name:
ConfigOutput44
ConfigOutput44Read

The capacitive reactive power for the generator is monitored to determine if it falls below the defined response value. In this way, monitoring the capacitive reactive power can be used to detect exciter failure. If the response value is fallen below, then the error message "Capacitive reactive power" is indicated (register "StatusInputPacked01") after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

Depending on how the "Power measurement mode" parameter is set in the "ConfigOutput21" register, either the total reactive power or the fundamental frequency reactive power (displacement reactive power) is compared with the response value.

The value of this register can be read back.

Data type	Value	Information	Resolution
INT	-32768 to 32767	For -32768 to 32767 kvar	1 kvar

Response time for reactive power monitoring

Name:
ConfigOutput45
ConfigOutput45Read

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

Generator overload

Name:
ConfigOutput89
ConfigOutput89Read

If the value of the active power of the generator exceeds the percentage of the generator's nominal power set here, then the error message "Generator overload" is indicated (register "StatusInputPacked01") after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

Depending on how the "Power measurement mode" parameter is set in the "ConfigOutput21" register, either the total active power or the fundamental frequency active power is compared with the response value.

The nominal power is calculated as follows:

$P_{NomGen} = U_{NomGen} * I_{NomGen} * \sqrt{3}$

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of P_{NomGen}	0.1%

Response time for generator overload

Name:
ConfigOutput90
ConfigOutput90Read

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

Generator feedback

Name:
ConfigOutput91
ConfigOutput91Read

If the value of the negative active power of the generator falls below the percentage of the generator's nominal power set here, then the error message "Generator feedback" is indicated (register "StatusInputPacked01") after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

Depending on how the "Power measurement mode" parameter is set in the "ConfigOutput21" register, either the total active power or the fundamental frequency active power is compared with the response value.

The nominal power is calculated as follows:

$P_{NomGen} = U_{NomGen} * I_{NomGen} * \sqrt{3}$

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	0 to 200% of P_{NomGen}	0.1%

Response time for generator feedback

Name:
ConfigOutput92
ConfigOutput92Read

The error is only triggered if the response value is exceeded in the negative direction without interruption for as long as is specified in this register.

The values of this register can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

DO1 function

This digital output can be set after the defined response time has elapsed depending on the assignment of the generator mains' monitoring variables (X3). Assignments are made using the "ConfigOutput57" and "ConfigOutput97" registers.

The monitoring variables can be assigned to this input either individually or with additional monitoring variables using an OR connective. This makes it possible to set the relay when there are multiple monitoring variables.

Assigning monitoring functions - 1

Name:
ConfigOutput57
ConfigOutput57Read

The following monitoring functions can be assigned to the monitoring relay using this register:

The value of this register can be read back.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Overvoltage (of a phase)	0	Do not assign function
		1	Assign function
1	Undervoltage (or a phase)	0	Do not assign function
		1	Assign function
2	Overfrequency	0	Do not assign function
		1	Assign function
3	Underfrequency	0	Do not assign function
		1	Assign function
4	Voltage asymmetry	0	Do not assign function
		1	Assign function
5	Current asymmetry (unbalanced load)	0	Do not assign function
		1	Assign function
6	Neutral conductor current, maximum	0	Do not assign function
		1	Assign function
7	Short circuit current	0	Do not assign function
		1	Assign function
8	Rating-dependent overcurrent	0	Do not assign function
		1	Assign function
9	Capacitive reactive power (exciter failure)	0	Do not assign function
		1	Assign function
10	Ready	0	Do not assign function
		1	Assign function
11	Generator overload	0	Do not assign function
		1	Assign function
12	Generator feedback	0	Do not assign function
		1	Assign function
13 - 14	Reserved	0	
15	Undervoltage 2 (one phase)	0	Do not assign function
		1	Assign function

Information:

The minimum pulse duration when addressing a monitoring function on the error bit via X2X as well as on the relay is 500 ms.

Assigning monitoring functions - 2

Name:
ConfigOutput97

The following additional monitoring functions can be assigned to the monitoring relay using this register:

The value of this register can be read back.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Overvoltage 2 (one phase)	0	Do not assign function
		1	Assign function
1	Underfrequency 2	0	Do not assign function
		1	Assign function
2	Overfrequency	0	Do not assign function
		1	Assign function
3 - 15	Reserved	0	

Information:

The minimum pulse duration when addressing a monitoring function on the error bit via X2X as well as on the relay is 500 ms.

4.26.2.18.3.4 Synchronization mains

(for mains configuration "Sync mains 1 / Sync mains 2")

Nominal voltage of synchronization mains (U_{NomSyn})

Name:
ConfigOutput01
ConfigOutput01Read

This is needed for converting the percentages based on this nominal value into physical units.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	70 to 65000	For 70 to 65000 V	1 V

Multiplier for synchronization mains

Name:
ConfigOutput07 (mains 1)
ConfigOutput08 (mains 2)
ConfigOutput07Read (mains 1)
ConfigOutput08Read (mains 2)

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

100 means a multiplier factor of 1 (measured value not changed).

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 65535	For 0.01 to 655.35	0.01

4.26.2.18.3.5 Mains

Mains (for mains configuration "3-phase mains")

Nominal voltage of mains ($U_{NomMains}$)

Name:
ConfigOutput01
ConfigOutput01Read

This is needed for converting the percentages based on this nominal value into physical units.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	70 to 65000	For 70 to 65000 V	1 V

Multiplier for mains

Name:
ConfigOutput07
ConfigOutput07Read

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

100 means a multiplier factor of 1 (measured value not changed).

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 65535	For 0.01 to 655.35	0.01

Enable/disable mains functions

Name:
ConfigOutput22
ConfigOutput22Read

The value of this register can be read back.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Error acknowledgment mode	0	Mains error bits are reset by the module
		1	Mains error bits are reset by the user
1	Phase shift measurement	0	Three-phase only
		1	Single- or three-phase
2 - 3	Check all overvoltages and undervoltages	00	3 line-to-line voltages (default)
		01	3 phase voltages
		10	3 line-to-line and 3 phase voltages
		11	Reserved
4	Configuration of undervoltage monitoring	0	2-point mode
		1	6-point mode
5 - 7	Reserved	0	

1) This parameter is supported starting with upgrade 1.6.0.0 (firmware version 102). For information about configuring limit values, see section "Mains voltage monitoring".

4.26.2.18.3.6 Mains monitoring functions

(for "3-phase mains" configuration)

The following mains monitoring functions are available if the network configuration is set to a 3-phase mains (see register "Mains settings").

Mains voltage monitoring

Overvoltage limit of the mains ($U_{maxMains}$)

Name:
ConfigOutput73 (1st value)
ConfigOutput98 (2nd value)
ConfigOutput73Read (1st value)
ConfigOutput98Read (2nd value)

If the value of one of the mains voltages configured in the "ConfigOutput22" register exceeds the value set here, then the "Overvoltage" error message (register "StatusInputPacked02") or "Overvoltage 2" (register "StatusInput-Packed04") is indicated after the delay time has expired and, if configured, the DO5 monitoring relay is switched.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of $U_{NomMains}$	0.1%

Response time for mains overvoltage ($U_{MaxMains}$)

Name:
ConfigOutput82 (1st time)
ConfigOutput99 (2nd time)
ConfigOutput82Read (1st time)
ConfigOutput99Read (2nd time)

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 60000	For 0.005 to 60 s	0.001 s

Mains over-frequency ($f_{maxMains}$)

Name:
ConfigOutput75 (1st frequency)
ConfigOutput102 (2nd frequency)
ConfigOutput75Read (1st frequency)
ConfigOutput102Read (2nd frequency)

If the value of the mains frequency exceeds the percent value set here in relation to the nominal frequency, then the error message "Overfrequency" (register "StatusInputPacked02") or "Overfrequency 2" (register "StatusInput-Packed04") is indicated after the delay time has passed and, if configured, the DO5 monitoring relay is switched.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of f_{Nom}	0.1%

Response time for mains over-frequency ($f_{maxMains}$)

Name:
ConfigOutput84 (1st time)
ConfigOutput103 (2nd time)
ConfigOutput84Read (1st time)
ConfigOutput103Read (2nd time)

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 60000	For 0.005 to 60 s	0.001 s

Mains under-frequency ($f_{minMains}$)

Name:
ConfigOutput76 (1st frequency)
ConfigOutput104 (2nd frequency)
ConfigOutput76Read (1st frequency)
ConfigOutput104Read (2nd frequency)

If the value of the mains frequency falls below the percent value set here in relation to the nominal frequency, then the error message "Underfrequency" (register "StatusInputPacked02") or "Underfrequency 2" (register "StatusInputPacked04") is indicated after the delay time has passed and, if configured, the DO5 monitoring relay is switched.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of f_{Nom}	0.1%

Response time for mains under-frequency ($f_{minMains}$)

Name:
ConfigOutput85 (1st time)
ConfigOutput105 (2nd time)
ConfigOutput85Read (1st time)
ConfigOutput105Read (2nd time)

The error is only triggered if the response value is exceeded in the negative direction without interruption for as long as is specified in this register.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 60000	For 0.005 to 60 s	0.001 s

Mains voltage asymmetry ($U_{asMains}$)

Name:
ConfigOutput77
ConfigOutput77Read

This trigger value, specified as a percentage, is based on the nominal voltage of the mains. If the difference between the 3 line-to-line voltages of the mains exceeds the configured limit value, then the error message "Voltage asymmetry" is indicated (register "StatusInputPacked02") after the delay time has passed and, if configured, the DO5 monitoring relay is switched.

For this to happen, only one of these voltages has to exceed the respective limit value (in either the positive or negative direction).

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 300	For 0 to 30% of $U_{NomMains}$	0.1%

Response time for the mains voltage asymmetry ($U_{asMains}$)

Name:
ConfigOutput86
ConfigOutput86Read

This error is triggered only if the response value is exceeded without interruption (in either the positive or negative direction) for as long as is specified in this register.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.005 to 0.1 s	0.001 s

Undervoltage monitoring in 2-point mode

2 independent limit values and response times can be defined for undervoltage monitoring.

Undervoltage limit of the mains ($U_{minMains}$)

Name:
ConfigOutput74
ConfigOutput74Read

If the value of one of the mains voltages configured in the "ConfigOutput22" register falls below the value set here, then the "Undervoltage" error message (register "StatusInputPacked02") is indicated after the delay time has passed and, if configured, the DO5 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of $U_{NomMains}$	0.1%

Undervoltage limit 2 of the mains ($U_{minMains}$)

Name:
ConfigOutput100
ConfigOutput100Read

If the value of one of the linked mains voltages falls below the value set here, then the "Undervoltage" error message (register "StatusInputPacked02") is indicated after the delay time has passed and, if configured, the DO5 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	0 to 200% of $U_{NomMains}$	0.1%

Response time for mains undervoltage ($U_{minMains}$)

Name:
ConfigOutput83 (1st time)
ConfigOutput101 (2nd time)
ConfigOutput83Read (1st time)
ConfigOutput101Read (2nd time)

The error is only triggered if the response value is exceeded in the negative direction without interruption for as long as is specified in this register.

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 60000	For 0.005 to 60 s	0.001 s

Undervoltage monitoring in 6-point mode

Up to 6 limit values and response times can be set for undervoltage monitoring. If not all 6 points are required, then unused limit values and response times should be set to 0.
Note that for each point, the specified limit value and response time must be greater than or equal to the preceding point (P1 ≤ P2 ≤ P3, etc.).

The defined points are used to create a limit value curve. If the voltage drops below the curve and a response time has expired, the error message "Undervoltage" is signaled ("StatusInputPacked02" register). If configured, the D05 monitoring relay is also switched.

A faulty undervoltage monitoring configuration also triggers the "Undervoltage" error message, and monitor relay DO5 is switched if configured to do so (e.g. P1 > P2 and P2 not equal to (0% / 0 ms)).

The types of voltages to be monitored are specified in the mains configuration ("ConfigOutput22" register):

- Line-to-line voltages
- Phase voltages
- Line-to-line and phase voltages

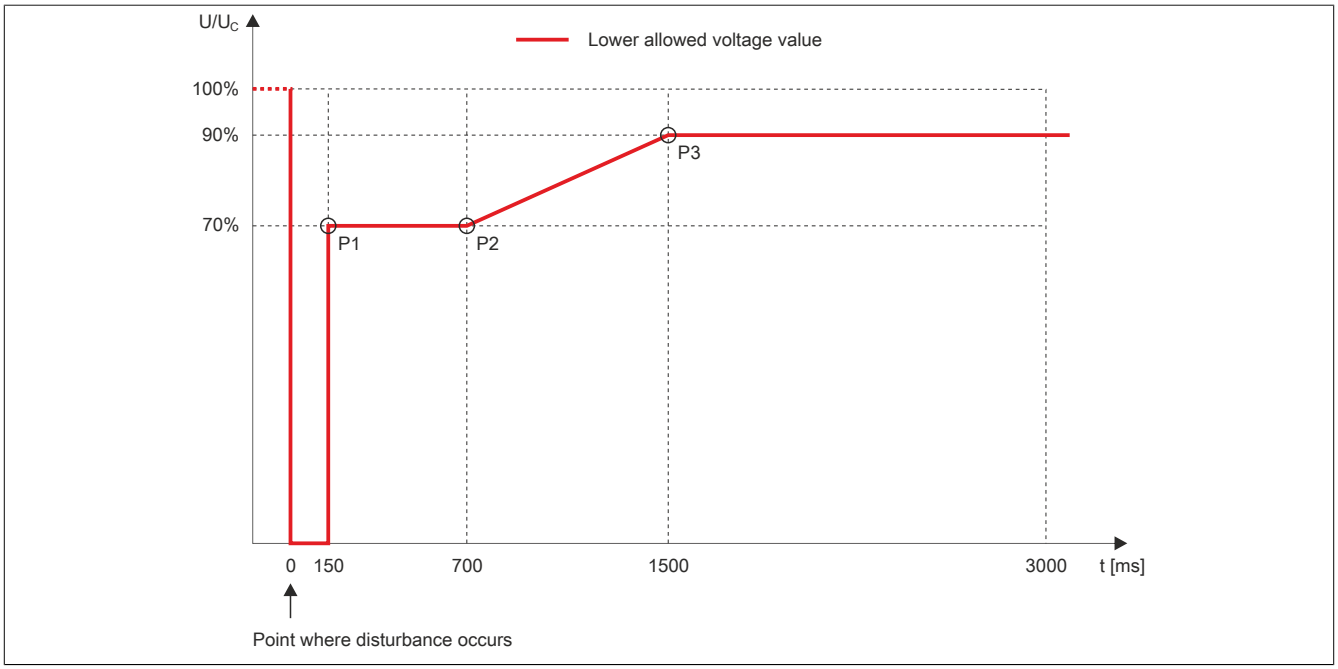
As soon as one of the monitored voltages drops below the limit curve, the corresponding time counter begins counting. The time counter is reset when all voltages are once again equal to or higher than the defined value.

The "Undervoltage" error message is generated when one of the time counters crosses over the limit curve.

Example 1 with 3 points:

In this example, 3 limit values are defined, along with the corresponding response times:

- P1 (70% / 150 ms)
- P2 (70% / 700 ms)
- P3 (90% / 1500 ms)
- P4 (0% / 0 ms)
- P5 (0% / 0 ms)
- P6 (0% / 0 ms)



Notes regarding limit curve

- The red line marks the lowest permitted value for monitored voltages.
- If 2 consecutive points have the same limit value, then the response time of the first point is applied. In the example above, this situation is shown with points 1 and 2.
- Between points 2 and 3 the curve has a positive linear slope. If one of the monitored voltages drops in this area, the module calculates the appropriate response time.

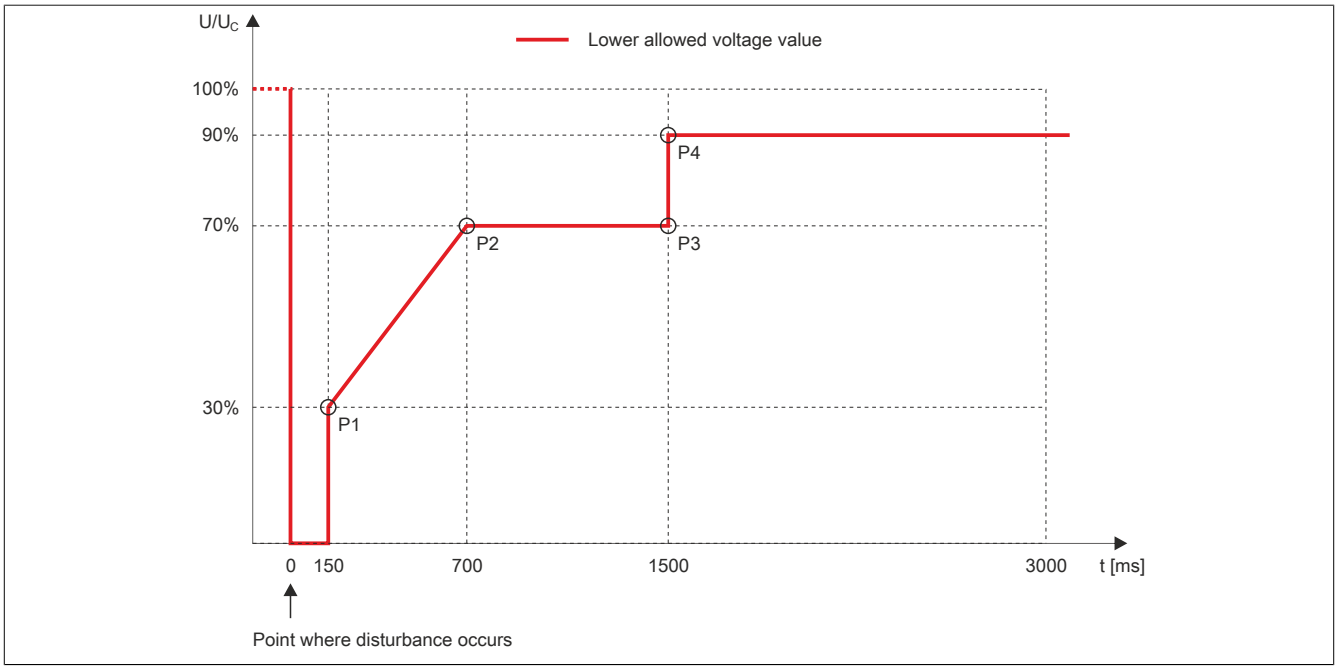
Determining the response time

1 Find voltage value on Y axis
2 Locate intersection on curve
3 Read the response time on the X axis

Example 2 with 4 points:

In this example, 4 limit values are defined, along with the corresponding response times:

- P1 (30% / 150 ms)
- P2 (70% / 700 ms)
- P3 (70% / 1500 ms)
- P4 (90% / 1500 ms)
- P5 (0% / 0 ms)
- P6 (0% / 0 ms)



Notes regarding limit curve

- The red line marks the lowest permitted value for monitored voltages.
- Between points 1 and 2 the curve has a positive linear slope. If one of the monitored voltages drops in this area, the module calculates the appropriate response time.
- If 2 consecutive points have the same limit value, then the response time of the first point is applied. In the example, this situation is shown with points 2 and 3.
- Points 1 and 2 are connected directly by a line with a positive slope. To avoid a direct connection between points 2 and 4, one would have to define another point between them with the same limit as point 2 and the same response time as point 4. In this case, that is point 3.

Determining the response time

1 Find voltage value on Y axis
2 Locate intersection on curve
3 Read the response time on the X axis

Undervoltage limit of the microgrid ($U_{MinMains}$)

Name:
ConfigOutput74 (1st mains)
ConfigOutput100 (2nd mains)
ConfigOutput110 (3rd mains)
ConfigOutput112 (4th mains)
ConfigOutput114 (5th mains)
ConfigOutput116 (6th mains)
ConfigOutput74Read (1st mains)
ConfigOutput100Read (2nd mains)
ConfigOutput110Read (3rd mains)
ConfigOutput112Read (4th mains)
ConfigOutput114Read (5th mains)
ConfigOutput115Read (6th mains)

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	0 to 200% of $U_{NomMains}$	0.1%

Response time for mains undervoltage ($U_{minMains}$)

Name:
ConfigOutput83 (1st mains)
ConfigOutput101 (2nd mains)
ConfigOutput111 (3rd mains)
ConfigOutput113 (4th mains)
ConfigOutput115 (5th mains)
ConfigOutput117 (6th mains)
ConfigOutput83Read (1st mains)
ConfigOutput101Read (2nd mains)
ConfigOutput111Read (3rd mains)
ConfigOutput113Read (4th mains)
ConfigOutput115Read (5th mains)
ConfigOutput117Read (6th mains)

The values of these registers can be read back.

Data type	Value	Information	Resolution
UINT	5 to 60000	For 0.005 to 60 s	0.001 s

Microgrid monitoring

A microgrid is a small mains power grid that only supplies a limited area and generally is not connected to other mains grids, which means it can function autonomously. This is in contrast to a synchronous grid, in which multiple smaller mains grids are connected together and synchronized.

With microgrid monitoring, the mains is monitored for over/undervoltage. After a defined response time elapses, a corresponding error message is generated. Microgrid monitoring always checks the line-to-line voltages independently of the configuration in the "ConfigOutput22" register.

Overvoltage limit of the mains ($U_{maxMains}$)

Name:
ConfigOutput106
ConfigOutput106Read

If the value of one of the linked mains voltages exceeds the value set here, then the "Microgrid monitoring" error message (register "StatusInputPacked04") is indicated after the delay time has passed and, if configured, the DO5 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	0 to 200% of $U_{NomMains}$	0.1%

Undervoltage limit of the mains ($U_{minMains}$)

Name:
ConfigOutput107
ConfigOutput107Read

If the value of one of the linked mains voltages falls below the value set here, then the "Microgrid monitoring" error message (register "StatusInputPacked04") is indicated after the delay time has passed and, if configured, the DO5 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of $U_{NomMains}$	0.1%

Response time for microgrid limit

Name:
ConfigOutput108
ConfigOutput108Read

An error is triggered only if the response value is exceeded without interruption (in either the positive or negative direction) for as long as is specified in this register.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	5 to 200	For 0.005 to 0.2 s	0.001 s

Phase shift monitoring

A phase shift is an abrupt change to the voltage curve that can be caused by a significant change to the load.

In this case, the device recognizes a single change to the period duration. This changed period duration is compared with the calculated average value from past measurements. Monitoring takes place for three phases and if desired also for a single phase. The phase shift monitoring function is only active if the mains voltage is higher than the set percentage value based on the nominal voltage for the converter.

If the response value is exceeded, the error message "Phase shift" is indicated (register "StatusInputPacked02") and, if configured, the DO5 monitoring relay is switched.

Phase shift monitoring response time

A phase shift is indicated on output DO5 within 2 ms after detection of the phase shift (i.e. after zero crossing of the extended/shortened period), as long as this is configured accordingly.

Phase shift detection

Phase shift detection is configured in the "ConfigOutput22" register.

Type of monitoring	Description
Only three-phase monitoring	Triggering takes place if the limit value for three-phase monitoring was exceeded on all 3 phases within 2 periods.
Single-phase or three-phase monitoring	Triggering takes place: • If the limit value for single-phase monitoring is exceeded on at least one of the 3 phases • If the limit value for three-phase monitoring was exceeded on all 3 phases within 2 periods.

Phase shift monitoring detects an abrupt change to the period duration of the mains voltage.

The period duration of the current period is compared with the average value for the period duration over the past 4 periods. If the difference exceeds the set limit value, then triggering takes place immediately.

Limit value

Setting of the limit value takes place in 0.1° steps. The internal limit value in µs is calculated as follows:

t_{hres}[µs] = t_{hres}[0.1°] * Period duration / 3600

When do this, the period duration for the set nominal frequency is used.

Example

Calculation of t_{hres}[µs] at 50 Hz (period duration = 20000 µs) and limit value of 7°:

t_{hres}[µs] = 70 * 20000 µs / 3600 = 388.88 µs (rounded to 389 µs)

If the period duration thus changes abruptly by more than +389 µs, triggering takes place.

Maximum phase difference for a single phase

Name:
ConfigOutput78
ConfigOutput78Read

Triggering occurs if the electrical angle of the voltage curve shifts by more than the set angle on at least one phase.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 990	For 0 to 99°	0.1°

Maximum phase difference for three phases

Name:
ConfigOutput79
ConfigOutput79Read

Triggering occurs if the electrical angle of the voltage curve shifts by more than the set angle on all 3 phases.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 990	For 0 to 99°	0.1°

Minimum voltage for phase shift monitoring

Name:
ConfigOutput88
ConfigOutput88Read

A minimum voltage can be set. Phase shift monitoring is only active if the voltage on all 3 phases exceeds this value.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of $U_{NomMains}$	0.1%

Mains frequency chance

Response value for mains frequency change (df/dt)

Name:
ConfigOutput80
ConfigOutput80Read

For df/dt monitoring, the frequency change in each period is compared to the previous period.

If this value exceeds the configured limit value in each of the periods for the specified number of periods and the sign for the frequency change is always the same, the error message "Df/dt (mains frequency change)" is indicated (register "StatusInputPacked02")and, if configured, the DO5 monitoring relay is switched.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 1000	For 0 to 100 Hz/s	0.1 Hz/s

Number of periods for mains frequency change (df/dt)

Name:
ConfigOutput87
ConfigOutput87Read

This register is used to define the number of periods for monitoring the mains frequency change. For activation, the response value must be continually exceeded at least for as many periods as specified in this register. The display of the error message on output DO5 takes place max. 2 ms after internal detection.

The value of this register can be read back.

Example

The maximum tripping time at 4 periods and 50 Hz mains frequency is calculated as follows:

Max. tripping time = 4 x 20 ms + 2 ms = 82 ms

The change in period duration caused by the frequency gradients must also be accounted for.

Data type	Value	Information	Resolution
UINT	1 to 250	-	-

DO5 function

DO5 function

Name:
ConfigOutput81
ConfigOutput81Read

This digital output can be set after the defined response time has elapsed depending on the assignment of the mains' monitoring variables.

The monitoring variables can be assigned to this input either individually or with additional monitoring variables using an OR connective. This makes it possible to set the output when there are multiple monitoring variables.

The following table is an overview of the monitoring functions that can be assigned to the monitoring output:

The value of this register can be read back.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Error notification
0	Overvoltage (of a phase)	0	Do not assign function
		1	Assign function
1	Undervoltage (or a phase)	0	Do not assign function
		1	Assign function
2	Overfrequency	0	Do not assign function
		1	Assign function
3	Underfrequency	0	Do not assign function
		1	Assign function
4	Voltage asymmetry	0	Do not assign function
		1	Assign function
5	Phase shift- 1/3 of a phase	0	Do not assign function
		1	Assign function
6	Df/dt exceeded	0	Do not assign function
		1	Assign function
7	Undervoltage 2 (one phase)	0	Do not assign function
		1	Assign function
8	Overvoltage 2 (one phase)	0	Do not assign function
		1	Assign function
9	Underfrequency 2	0	Do not assign function
		1	Assign function
10	Overfrequency 2	0	Do not assign function
		1	Assign function
11	Microgrid monitoring	0	Do not assign function
		1	Assign function
12 - 15	Reserved	-	

Information:

The minimum pulse duration when addressing a monitoring function on the error bit via X2X as well as on the output is 500 ms.

4.26.2.18.3.7 Busbar

Busbar nominal voltage (U_{NomBus})

Name:
ConfigOutput03
ConfigOutput03Read

This is needed for converting the percentages based on this nominal value into physical units.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	70 to 65000	For 70 to 65000 V	1 V

Multiplier for busbar

Name:
ConfigOutput05
ConfigOutput05Read

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

100 thus means a multiplier factor of 1 (measured value not changed).

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 65535	For 0.01 to 655.35	0.01

Minimum busbar voltage (U_{Bmin})

Name:
ConfigOutput40
ConfigOutput40Read

Configurable threshold for zero voltage monitoring of the busbar based on its nominal voltage. DO3 is set if the value falls below the configured threshold.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 1000	For 0 to 100% of U_{NomBus}	0.1%

4.26.2.18.3.8 Synchronization

Synchronization mode

Name:
ConfigOutputPacked01
ConfigOutput17 to ConfigOutput19

If multiple mode bits are set at the same time, then no mode will be selected (type BOOL).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ConfigOutput17	0	Sync mode ≠ Slip
		1	Sync mode = Slip
1	ConfigOutput18	0	Sync mode ≠ Check
		1	Sync mode = Check
2	ConfigOutput19	0	Sync mode ≠ Dead bus
		1	Sync Mode = Dead bus
3 - 7	Reserved	-	

Synchronization configuration

Name:
ConfigOutput56
ConfigOutput56Read

This register contains parameters for configuring which mains or voltages should be synchronized with each other.

The value of this register can be read back.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Synchronization configuration (synchronization mains - mains being synchronized)	00	X4 - X6: Synchronization mains 1 - Synchronization mains 2 **The configuration X4 - X6 is only possible if "Sync mains 1 / Sync mains 2" is configured in the "ConfigOutput68" register.**
		01	X4 - X5: Synchronization mains 1 - Busbar
		10	X4 - X3: Synchronization mains 1 - Generator
		11	X5 - X3: Busbar - Generator
2 - 7	Reserved	0	
8	Synchronization output	0	Digital output 4
		1	Digital output 6 - Output must be configured as a synchronization output (see register "ConfigOutput24")
9 - 15	Reserved	0	

Max. differential frequency (df_{max})

Name:
ConfigOutput11
ConfigOutput11Read

A switch-on command on DO4 is only output if this configured differential frequency is not exceeded. This value specifies the upper frequency (positive value corresponds to positive slip → generator frequency is greater than the busbar frequency when synchronizing).

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	2 to 49	For 0.02 to 0.49 Hz	0.01 Hz

Min. differential frequency (df_{min})

Name:
ConfigOutput12
ConfigOutput12Read

A switch-on command on DO4 is only output if this configured differential frequency is not exceeded in the negative direction. This value specifies the lower frequency (negative value corresponds to negative slip → generator frequency is less than the busbar frequency when synchronizing).

The value of this register can be read back.

Data type	Value	Information	Resolution
INT	-49 to 0	For -0.49 to 0 Hz	0.01 Hz

Max. differential voltage (dU_{max})

Name:
ConfigOutput13
ConfigOutput13Read

A switch-on command on DO4 is only output if this configured differential voltage percentage based on the synchronization mains' nominal voltage is not exceeded.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 300	For 0.1 to 30% of U_{NomSyn}	0.1%

Max. permitted differential angle (Φ_{Max})

Name:
ConfigOutput14
ConfigOutput14Read

A switch-on command on DO4 is only output if the configured differential angle between the two synchronization mains is not exceeded.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	1 to 600	For 0.1 to 60°	0.1°

Phase rotation of sync mains 1 (dα)

Name:
ConfigOutput15
ConfigOutput15Read

This parameter is used for correcting any phase shifting from upstream transformer vector groups before reaching the mains being synchronized.

This parameter specifies how many degrees the synchronization mains lags behind the mains being synchronized.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 3600	For 0 to 360°	0.1°

Pulse duration of the turn-on delay

Name:
ConfigOutput47 (DO4)
ConfigOutput95 (DO6)
ConfigOutput47Read (DO4)
ConfigOutput95Read (DO6)

The duration of the switch-on pulse can be adjusted for the following switching units.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	40 to 1000	For 0.04 to 1 s	0.001 s

Switching response time of the power switch

Name:
ConfigOutput48 (DO4)
ConfigOutput96 (DO6)
ConfigOutput48Read (DO4)
ConfigOutput96Read (DO6)

The actuation time of the generator power switch corresponds to the lead time of the switch-on command. The switch-on command is executed before the point of synchronization according to the amount of time defined here.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	40 to 300	For 0.04 to 0.3 s	0.001 s

Dead bus voltage ($U_{BminSync}$)

Name:
ConfigOutput58
ConfigOutput58Read

Configurable threshold for dead bus synchronization based on the nominal voltage of the busbar.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 1000	For 0 to 100% of U_{NomBus}	0.1%

2-phase synchronization for commissioning tests

Name:
ConfigOutput93
ConfigOutput93Read

2-phase synchronization for commissioning tests.

The value of this register can be read back.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Synchronization	0	Default: 3-phase synchronization (normal operation)
		1	2-phase synchronization with L1 and L2 (commissioning tests with 2-phase simulation design)
1 - 7	Reserved	0	

Information:

It is only possible to set 2-phase synchronization for commissioning tests with a 2-phase simulation design.

If only 2 phases are connected, then the respective mains must be configured with neutral conductors since a network with a "virtual neutral point" is not possible with 2 phases (see register "ConfigOutput68").

4.26.2.18.3.9 Maximum value buffer and power meter

Pulse value of energy meter output

Name:
ConfigOutput46
ConfigOutput46Read

Output DO2 outputs pulses that occur at a frequency proportional to the measured energy. The frequency of the pulses can be specified. The length of the pulse is 400 ms. The frequency at which the pulses occur should be set so that the duration between two pulses does not exceed 400 ms at the highest possible power. The pulse output's internal meter starts at 0 kWh after a restart. This register has no effect on the "ConfigOutput54" and "ConfigOutput55" registers.

When set to 0, meter output is disabled.

Depending on how the "Power measurement mode" parameter is set in the "ConfigOutput21" register, either the total active power or the active power of the fundamental wave is added together. Changing the parameter "Power measurement mode" during runtime does not cause the internal energy meter to restart.

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 65535	For 0 to 65535 kWh/pulse	1 kWh/pulse

Count value for active energy meter and reactive energy meter

Name:
ConfigOutput94
ConfigOutput94Read

This parameter is used to configure the resolution of the active energy meter and reactive energy meter (default: 100 kWh).

The value of this register can be read back.

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	1 kWh

Maximum value buffer and meter buffer

These registers are used for nonvolatile storage of the maximum value and meter level values. After restarting, the stored maximum values and meter states are loaded back into their registers and the module's internal work meter is reset. It is possible to reset or write to the stored maximum values and meter states using an acyclic register.

The maximum values are recorded by the effective measured values before reaching the configurable filter. The maximum values can be read or written to as acyclic registers.

Maximum phase current

Name:
Reading: ConfigOutput49 (generator I1)
Reading: ConfigOutput50 (generator I2)
Reading: ConfigOutput51 (generator I3)
Writing: ConfigOutput60 (generator I1)
Writing: ConfigOutput61 (generator I2)
Writing: ConfigOutput62 (generator I3)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Maximum total active power (supplied power)

Name:
Reading: ConfigOutput52
Writing: ConfigOutput63

Depending on the status of the "Power measurement mode" parameter in the "ConfigOutput21" register, either the total power or the fundamental power is added together or compared.

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 kW

Maximum neutral conductor current

Name:
Reading: ConfigOutput53
Writing: ConfigOutput64

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Active energy counter

Name:
Reading: ConfigOutput54 (delivered (producing))
Reading: ConfigOutput71 (drawn (consuming))
Writing: ConfigOutput66 (delivered (producing))
Writing: ConfigOutput69 (drawn (consuming))

Depending on the status of the "Power measurement mode" parameter in the "ConfigOutput21" register, either the total power or the fundamental power is added together or compared.

The resolution can be configured (see register "ConfigOutput94").

Data type	Value	Information	Resolution
DINT	-2,147,483,648 to 2,147,483,647	-	Default: 100 kWh

Reactive energy counter

Name:
Reading: ConfigOutput55 (reactive energy meter delivered (producing))
Reading: ConfigOutput72 (reactive energy meter drawn (consuming))
Writing: ConfigOutput67 (reactive energy meter delivered (producing))
Writing: ConfigOutput70 (reactive energy meter drawn (consuming))

Depending on the status of the "Power measurement mode" parameter in the "ConfigOutput21" register, either the total power or the fundamental power is added together or compared.

The resolution can be configured (see register "ConfigOutput94").

Data type	Value	Information	Resolution
DINT	-2,147,483,648 to 2,147,483,647	-	Default: 100 kvarh

4.26.2.18.4 Communication registers

4.26.2.18.4.1 General registers

DigitalOutputPacked01

Name:
DigitalOutputPacked01
DigitalOutput05
DigitalOutput06
ResetGeneratorErrors
ResetMainsErrors
InvertDO5

The module's default configuration is that the generator and mains error bits are reset by the module. If this should be done by the user, then the module needs to be configured accordingly using the following registers.

- Generator error: "ConfigOutput21"
- Network error: "ConfigOutput22"

(data point applied as BOOL)

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput05	0	Reset output 5
		1	Set output 5
1	DigitalOutput06	0	Reset output 6
		1	Set output 6
2	ResetGeneratorErrors	0	Does not reset generator error bits
		1	Resets generator error bits
3	ResetMainsErrors	0	Do not reset mains error bits
		1	Reset mains error bits
4	InvertDO5	0	Do not invert Output 5
		1	Invert output 5 of the mains monitoring function
5 - 7	Reserved	0	

StatusDigitalOutputPacked01

Name:
StatusDigitalOutputPacked01
StatusDigitalOutput01 to StatusDigitalOutput06
StatusInput16 to StatusInput17

(data point applied as BOOL)

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusDigitalOutput01	0	Current state of output 1 = LOW
		1	Current state of output 1 = HIGH
...		...	
5	StatusDigitalOutput06	0	Current state of output 6 = LOW
		1	Current state of output 6 = HIGH
6	StatusInput17	0	Status DO OK
		1	Status DO overload
7	StatusInput16	0	Status 24 V output supply OK
		1	Status 24 V output supply undervoltage

StatusInputPacked01

Name:
StatusInputPacked01
StatusInput01 to StatusInput11
StatusInput31 to StatusInput32
StatusInput18

This register is the error register for the generator mains (error bits are of type BOOL). With regard to bits 9, 11 and 12, please also observe the description of the "Power measurement mode" parameter in the register "ConfigOutput21".

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusInput01	0	Overvoltage (one phase), OK
		1	Overvoltage (one phase), present
1	StatusInput02	0	Undervoltage (one phase), OK
		1	Undervoltage (one phase), present
2	StatusInput03	0	Over-frequency, OK
		1	Over-frequency, present
3	StatusInput04	0	Under-frequency, OK
		1	Under-frequency, present
4	StatusInput05	0	Voltage asymmetry, OK
		1	Voltage asymmetry, present
5	StatusInput06	0	Current asymmetry, OK
		1	Current asymmetry, present
6	StatusInput07	0	Maximum neutral conductor current, OK
		1	Maximum neutral conductor current exceeded
7	StatusInput08	0	Short circuit-current, OK
		1	Short circuit-current, present
8	StatusInput09	0	Rating-dependent overcurrent OK
		1	Rating-dependent overcurrent occurring
9	StatusInput10	0	Capacitive reactive power (exciter failure), OK
		1	Capacitive reactive power (exciter failure), present
10	StatusInput11	0	Ready, OK
		1	Not ready
11	StatusInput31	0	No generator overload
		1	Generator overload
12	StatusInput32	0	No generator feedback
		1	Generator feedback
13 - 14	Reserved	-	
15	StatusInput18	0	Undervoltage 2 (of a phase) OK
		1	Undervoltage 2 (of a phase) occurring

StatusInput11

The error message "Not ready" is triggered if the X20 I/O supply drops below 18 VDC.

StatusInputPacked02

Name:
StatusInputPacked02
StatusInput24 to StatusInput30
StatusInput33

This register is the error register for the mains (error bits are of type BOOL).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusInput24	0	Overvoltage (one phase), OK
		1	Overvoltage (one phase), present
1	StatusInput25	0	Undervoltage (one phase), OK
		1	Undervoltage (one phase), present
2	StatusInput26	0	Over-frequency, OK
		1	Over-frequency, present
3	StatusInput27	0	Under-frequency, OK
		1	Under-frequency, present
4	StatusInput28	0	Voltage asymmetry, OK
		1	Voltage asymmetry, present
5	StatusInput29	0	Phase shift monitoring OK
		1	Phase shift error (1/3 of a phase)
6	StatusInput30	0	Df/dt OK
		1	Df/dt error
7	StatusInput33	0	Undervoltage 2 (of a phase) OK
		1	Undervoltage 2 (of a phase) occurring

StatusInput33

The data point is only valid if 2-point mode is configured (see register "ConfigOutput22"). This bit only appears in the I/O mapping in Automation Studio if the corresponding status information is enabled in the I/O configuration ("Mains configuration / Additional status information" menu option).

StatusInputPacked03

Name:
StatusInputPacked03
StatusInput12 to StatusInput15
StatusInput19 to StatusInput23

This register is the error register for general error messages (error bits are of type BOOL).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusInput12	0	All phases of the generator mains OK
		1	Failure of at least one phase of the generator mains
1	StatusInput13	0	All phases of the busbar OK
		1	Failure of at least one phase of the busbar
2	StatusInput14	0	All phases of Sync Mains 1 OK
		1	Failure of at least one phase of Sync Mains 1
3	StatusInput15	0	All phases of Sync Mains 2 OK
		1	Failure of at least one phase of Sync Mains 2
4	StatusInput19	0	Phase sequence of generator voltage OK
		1	Phase sequence of generator voltage incorrect
5	StatusInput20	0	Phase sequence of generator current OK
		1	Phase sequence of generator current incorrect
6	StatusInput21	0	Phase sequence of busbar OK
		1	Phase sequence of busbar incorrect
7	StatusInput22	0	Phase sequence of Sync Mains 1 OK
		1	Phase sequence of Sync Mains 1 incorrect
8	StatusInput23	0	Phase sequence of Sync Mains 2 OK
		1	Phase sequence of Sync Mains 2 incorrect
9 - 15	Reserved	-	

StatusInput12 to StatusInput15: Phase failure is detected if at least one of the phases of the respective terminal fails.

StatusInput19 to StatusInput23 are status bits for detecting a change of rotation.

StatusInputPacked04

Name:
StatusInputPacked04
StatusInput34 to StatusInput37

This register is the error register for the mains (error bits are of type BOOL). These bits only appear in the I/O mapping in Automation Studio if the corresponding status information is enabled in the I/O configuration ("Mains configuration / Additional status information" menu option).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusInput34	0	Overvoltage 2 (of a phase) OK
		1	Overvoltage 2 (of a phase) occurring
1	StatusInput35	0	Underfrequency 2 OK
		1	Underfrequency 2 occurring
2	StatusInput36	0	Overfrequency 2 OK
		1	Overfrequency 2 occurring
3	StatusInput37	0	Microgrid monitoring OK
		1	Microgrid monitoring tripped
4 - 15	Reserved	-	

StatusInputPacked05

Name:
StatusInputPacked05
StatusInput38 to StatusInput40

This register is the error register for the generator mains (error bits are of type BOOL). These bits only appear in the I/O mapping in Automation Studio if the corresponding status information is enabled in the I/O configuration ("Generator mains / Additional status information" menu option).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusInput38	0	Overvoltage 2 (of a phase) OK
		1	Overvoltage 2 (of a phase) occurring
1	StatusInput39	0	Underfrequency 2 OK
		1	Underfrequency 2 occurring
2	StatusInput40	0	Overfrequency 2 OK
		1	Overfrequency 2 occurring
3 - 15	Reserved	-	

4.26.2.18.4.2 Generator mains measured values

Phase currents of the generator

Name:
AnalogInput01 (I1)
AnalogInput02 (I2)
AnalogInput03 (I3)

Phase currents of the generator

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Neutral conductor current of generator I_n

Name:
AnalogInput05

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Current average of generator I1, I2, I3

Name:
AnalogInput04

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Dynamic current average of generator (I_{m_dyn})

Name:
AnalogInput06

Describes the change to the current average.

The dynamic average is the amount of change (I_{m_diff}) of the current average (sampling time: 10 ms).

This value decays in an e-function.

$I_{m\_diff} > I_{m\_dyn} \rightarrow I_{m\_dyn} = I_{m\_diff}$

$I_{m\_diff} \leq I_{m\_dyn} \rightarrow I_{m\_dyn} = I_{m\_dyn} * 0.98$

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	1 A

Line-to-line voltages of the generator

Name:
AnalogInput07 (UG12)
AnalogInput08 (UG23)
AnalogInput09 (UG31)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Phase voltages of the generator

Name:
AnalogInput10 (UG 1)
AnalogInput11 (UG 2)
AnalogInput12 (UG 3)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Voltage average of the generator

Name:
AnalogInput22

Voltage average of the generator UG12, UG23, UG31 (U~3 average)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Filtered generator power values:

Name:
AnalogInput19
AnalogInput20
AnalogInput21

Filtered generator power values:

- Total output (sum of all harmonic frequencies)
- Fundamental frequency power (_H1)

Configuration is explained in the "ConfigOutput21" register.

Data type	Value	Information	Resolution
INT	-32768 to 32767	Total active power P/P_H1	1 kW
	-32768 to 32767	Total reactive power Q/Q_H1	1 kvar
	-32768 to 32767	Total apparent power S/S_H1	1 kVA

Power factor of generator/cos ϕ

Name:
AnalogInput23

The factor is described in the section 4.26.2.17 "Power factor of the generator" and the section for the register "ConfigOutput21".

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	0.001

Frequency of the generator mains

Name:
AnalogInput24

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	0.01 Hz

Timestamp for generator voltages and currents

These timestamps mark the last positive zero crossing of the generator voltages (L1-N, L2-N, L3-N) and generator currents (I1, I2, I3). They can be used to calculate all the necessary phase ratios.

Calculation of the phase ratios and error handling for the calculations are to be implemented by the user (e.g. period duration monitoring or verification that the voltages are high enough, etc.).

These timestamps only appear in the I/O mapping in Automation Studio if they are enabled in the I/O configuration ("Enable timestamps for generator voltage and current" menu option).

Timestamp of pos. zero crossing of phase voltage

Name:
AnalogInput38 (UG1)
AnalogInput39 (UG2)
AnalogInput40 (UG3)

Time stamp of pos. zero crossing of phase voltage of the respective generator

Data type	Value	Information	Resolution
DINT	-2,147,483,648 to 2,147,483,647	-	1/4096 µs

Timestamp of pos. zero crossing of phase current

Name:
AnalogInput41 (I1)
AnalogInput42 (I2)
AnalogInput43 (I3)

Time stamp of pos. zero crossing of phase current of the respective generator

Data type	Value	Information	Resolution
DINT	-2,147,483,648 to 2,147,483,647	-	1/4096 µs

4.26.2.18.4.3 Busbar measured values

Line-to-line voltages of the busbar

Name:
AnalogInput13 (UB12)
AnalogInput14 (UB23)
AnalogInput15 (UB31)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Phase voltages of the busbar

Name:
AnalogInput16 (UB1)
AnalogInput17 (UB2)
AnalogInput18 (UB3)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Frequency of busbar

Name:
AnalogInput35

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	0.01 Hz

4.26.2.18.4.4 Measured value of synchronization mains

(for mains configuration "Sync mains 1 / Sync mains 2")

Line-to-line voltages

Name:
AnalogInput25 (sync mains 1 US1)
AnalogInput26 (sync mains 2 US2)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Frequencies

Name:
AnalogInput27 (sync mains 1)
AnalogInput28 (sync mains 2)

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	0.01 Hz

4.26.2.18.4.5 Measured value of mains

(for "3-phase mains" configuration)

Line-to-line voltages of mains

Name:
AnalogInput25 (UN12)
AnalogInput31 (UN23)
AnalogInput32 (UN31)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Phase voltages of the generator

Name:
AnalogInput33 (UN1)
AnalogInput34 (UN2)
AnalogInput26 (UN3)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Frequency of power mains

Name:
AnalogInput27

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	0.01 Hz

4.26.2.18.4.6 Generator monitoring

Read unbalanced load meter

Name:
AnalogInput36

This register can be used to track the current state of the unbalanced load meter (see section "Dependent delayed unbalanced load monitoring"). The unbalanced load meter can be reset with an acyclic trigger bit (see register "ConfigOutput23").

Data type	Value	Information	Resolution
UINT	0 to 65535	For 0 to 100%	

Reads the unbalanced load current (I_2)

Name:
AnalogInput37

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

4.26.2.18.4.7 Synchronization

Differential angle between synchronization mains

Name:
AnalogInput29

Angular difference between the mains being synchronized

Specifies how many degrees the sync mains are ahead of the mains being synchronized.

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	0.1°

Differential voltage between synchronization mains

Name:
AnalogInput30

Voltage difference between the mains being synchronized

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

4.26.2.18.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

4.26.2.18.6 Minimum I/O update time

The minimum I/O update time for the analog inputs depends on the respective period duration of the measurement signal frequency.

Minimum I/O update time	
At 50 Hz	10 ms

4.26.3 X20CM0985

4.26.3.1 General information

The module has a compact size and combines a power measurement module that has special features with a synchronization unit that is able to meet all demands.

The measurement unit's 3 current inputs are suitable for both X: 1 A and X: 5 A current transformers. Overcurrent resistance and the high resolution of the measurement unit round off its features. For the voltage inputs, the value range can be configured between 480 VAC and 120 VAC.

The area of use includes 4-wire AC networks with a phase voltage up to 480 VAC and 3-wire systems, whereas L2 can be grounded (V-connection). The module can also handle Aron measuring circuits.

The resulting measured values include the pure phase current; line-to-line voltage or phase voltage; the effective, reactive and apparent power parts; the mains frequency; the power factor and much more. In addition, peak values and energy meters are stored on the module in nonvolatile memory. Depending on the configuration, it is also possible to use a digital output as a pulse encoder for an external energy meter.

The synchronization unit doesn't just take the phasing and phase voltage into consideration; integrated intelligence also monitors the rate of change and other parameters, allowing them to influence when the synchronization output is switched. It is also possible to monitor a generator using a large number of additional conditions. A total of 4 voltage inputs provide substantial overall flexibility.

Monitoring functions expand the features of the module. Rating-dependent overcurrent monitoring is included, which utilizes the thermal capacity of the motor/generator to allow short overloads while still providing full protection. The dependent, delayed imbalanced load monitoring used to protect three-phase generator and three-phase networks from imbalanced load can be adapted to the characteristics of different generator types using parameters while taking their special thermal time constants into account.

- Energy measurement for 120 to 480 VAC
- Simultaneous measurement of 2 AC mains networks plus 2 additional voltages
- For multifunctional measurement tasks
- Intelligent mains synchronization unit

Information:

Please refer to section 4.26.2.4 "Safety guidelines" before operating the module.

4.26.3.2 Order data

Model number	Short description	Figure
	Other functions	
X20CM0985	X20 digital and analog mixed module, multi-measurement transducer/ synchronization module, 5 digital outputs, 24 VDC, 0.5 A source, 1 relay, 1 A, changeover contact, 8 analog inputs, ±480 V / 120 V, 16-bit converter resolution, 3 analog inputs 5 A / 1 A AC, 16-bit converter resolution, order terminal blocks 0TB3102-7011, 0TB3104-7011, 0TB3102-7012, 0TB3104-7012 and 2x TB12 separately.	
	Required accessories	
	Terminal blocks	
0TB3102-7011	Accessory terminal block, 2-pin, A-keying, screw clamp 6 mm²	
0TB3102-7012	Accessory terminal block, 2-pin, B-keying, screw clamp 6 mm²	
0TB3104-7011	Accessory terminal block, 4-pin, A-keying, screw clamp 6 mm²	
0TB3104-7012	Accessory terminal block, 4-pin, B-keying, screw clamp 6 mm²	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 583: X20CM0985 - Order data

4.26.3.3 Technical data

Product ID	X20CM0985
Short description	
I/O module	X20 energy measurement and synchronization module
General information	
B&R ID code	0x2433
Status indicators	Channel status, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Analog inputs	Yes, using status LED (measurement range of analog inputs)
Digital outputs	Yes, using status LED and software
Overvoltage category	II [1]
Power consumption	
Bus	1.4 W
Internal I/O	4 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - I/O supply	Yes
Input/Output - Bus	Yes
Digital outputs - Analog inputs	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Design	FET positive switching
Quantity	5
Nominal voltage	24 VDC
Switching voltage	24 VDC -15% / +20%
Nominal output current	0.1 A
Total nominal current	0.5 A
Connection type	1-wire connections
Output circuit	Source
Output protection	Thermal cutoff for overcurrent and short circuit
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
Residual voltage	<0.3 V at 0.1 A rated current
Peak short circuit current	<2 A
Switching on after overload or short circuit cutoff	Approx. 10 ms, depends on the module temperature
Switching delay	
0 -> 1	<300 µs
1 -> 0	<300 µs
Switching frequency	
Resistive load	Max. 100 Hz
Isolation voltage between channel and bus	500 V_{eff}
Relay outputs	
Quantity	1
Design	Relay / Changeover contact

Table 584: X20CM0985 - Technical data

Product ID	X20CM0985
Nominal voltage	30 VDC / 240 VAC
Rated frequency	DC / 45 to 63 Hz
Switching capacity	
Min.	10 mA / 5 VDC
Max.	30 W / 240 VAC
Nominal output current	1 A at 30 VDC / 1 A at 240 VAC
Actuator supply	External
Switching voltage	Max. 60 VDC / 250 VAC
Switching delay	
0 -> 1	≤10 ms
1 -> 0	≤10 ms
Service life [3]	
Mechanics	Min. 10 x 10^6 ops.
Electrical	Min. 60 x 10^3 ops. (NC) at 1 A Min. 30 x 10^3 ops. (NO) at 1 A
Contact resistance	Max. 100 mΩ
Protective circuit	
Internal	None
External	None
DC	Inverse diode, RC combination or VDR
AC	RC combination or VDR
Isolation voltage	
Contact - Contact	1000 VAC / 1 min
Contact - Coil	4000 VAC / 1 min
Analog input voltage	
Channels	8
Input	120 VAC / 480 VAC
Input type	Single-ended
Digital converter resolution	±15-bit
Conversion time	
50 Hz	20 ms
60 Hz	16.67 ms
Permitted input signal	Max. 132 VAC / 528 VAC
Output format [4]	
±120 VAC	1 LSB = 0x0001 = 5.707 mV
±480 VAC	1 LSB = 0x0001 = 22.787 mV
Output of the digital value during overload	
Above upper limit	0x7FFF
Below lower limit	0x8001
Conversion method	SAR
Input filter	
Cutoff frequency	10 kHz
Slope	60 dB
Maximum gain drift [5]	0.02% per °C
Maximum offset drift [6]	0.003% per °C
Crosstalk between channels	-70 dB
Nonlinearity [6]	≤0.5% at 45 to 65 Hz
Protection against electrical shock	Protective impedance in accordance with IEC 61131-2
Test voltage between channel and bus (type test)	3700 V_{eff}
Output format	INT
Input impedance in signal range	Approx. 3 MΩ
Max. error at 25°C	
Gain	0.09% [5]
Offset	0.03% [6]
Input protection	Overvoltage protection
Analog input current	
Channels	3
Input	1 A / 5 A AC
Input type	Isolated current transformer according to the compensation principle with a magnetic sensor, for connecting an external transformer
Digital converter resolution	±15-bit
Conversion time	
50 Hz	20 ms
60 Hz	16.67 ms
Permitted input signal	Max. 1.5 A / 7.7 A
Output format [4]	
±1 A	1 LSB = 0x0001 = 189.903 µA
±5 A	1 LSB = 0x0001 = 949.513 µA
Output of the digital value during overload	
Above upper limit	0x7FFF
Below lower limit	0x8001
Conversion method	SAR

Table 584: X20CM0985 - Technical data

Product ID	X20CM0985
Input filter	
Cutoff frequency	10 kHz
Slope	60 dB
Maximum gain drift [5]	0.07% per °C
Maximum offset drift [7]	0.003% per °C
Crosstalk between channels	-70 dB
Nonlinearity [7]	≤0.5% at 45 to 65 Hz
Isolation voltage between channel and bus	500 V_{eff}
Output format	INT
Max. error at 25°C	
Gain	0.2% [5]
Offset	0.05% [7]
Thermal overcurrent	15 x I_{Nom} for 0.2 s [8]
Monitored overcurrent	4 x I_{Nom} [8]
Input impedance [9]	
Measurement range 1 A	Max. 30 mΩ
Measurement range 5 A	Max. 10 mΩ
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 2x X20TB12 terminal block separately Order 2x TB3102 and 2x TB3104 screw clamps separately
Spacing	$87.5^{+0.2}$ mm

Table 584: X20CM0985 - Technical data

1) IEC 61131-2.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) See section "Electrical service life"
4) INT, range of values: 0x8001 to 0x7FFF
5) Based on the current measured value.
6) Based on the measurement range 240 VAC / 960 VAC.
7) Based on the measurement range 2 A / 10 A.
8) Based on the measurement range 1 A / 5 A.
9) Including current transformer, circuit path and X20TB12 terminal block (5 mΩ)

4.26.3.4 Safety guidelines

General information

Programmable logic controllers, operating and monitoring devices (e.g. industrial PCs, Power Panels, Mobile Panels etc.) as well as the uninterruptible power supplies have all been designed, developed, and produced by B&R for conventional use in industry. They were not designed, developed and manufactured for any use involving serious risks or hazards that could lead to death, injury, serious physical damage or loss of any kind without the implementation of exceptionally stringent safety precautions. In particular, such risks and hazards include the use of these devices to monitor nuclear reactions in nuclear power plants, their use in flight control or flight safety systems as well as in the control of mass transportation systems, medical life support systems or weapons systems.

When using programmable logic controllers or operating/monitoring devices as control systems together with a Soft PLC (e.g. B&R Automation Runtime or comparable product) or Slot PLC (e.g. B&R LS251 or comparable product), safety precautions relevant to industrial control systems (e.g. the provision of safety devices such as emergency stop circuits, etc.) must be observed in accordance with applicable national and international regulations. The same applies for all other devices connected to the system, e.g. drives.

All tasks such as the installation, commissioning and servicing of devices are only permitted to be carried out by qualified personnel. Qualified personnel are those familiar with the transport, mounting, installation, commissioning and operation of devices who also have the appropriate qualifications (e.g. IEC 60364). National accident prevention regulations must be observed.

The safety notices, connection descriptions (type plate and documentation) and limit values listed in the technical data are to be read carefully before installation and commissioning and must be observed.

Intended use

Danger!

Electronic devices are never completely failsafe. If the multi-measurement and synchronization unit fails, the user is responsible for making sure that the motor or generator is brought to a secure state.

Some errors are detected and prevented in the synchronization unit by the system's internal software monitoring. However, when the device is in operation it is always possible for errors, defective components, software errors or configuration mistakes to occur at any time. B&R emphasizes that the multi-measurement and synchronization unit possesses neither a failsafe function nor a redundancy system. For this reason, independent higher-level safety precautions need to be put in place to ensure that personnel and machines are protected.

Grounding the Mounting Rail

For grounding purposes, a good conductive connection between the mounting rail and the metal back wall is required. The mounting rail is to be connected conductively to the back wall. This is achieved by inserting a contact washer with the fastening screw.

Information:

The control cabinet back wall must be connected with GND

4.26.3.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

LED status indicators - Right

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Orange		Output status of the corresponding digital output

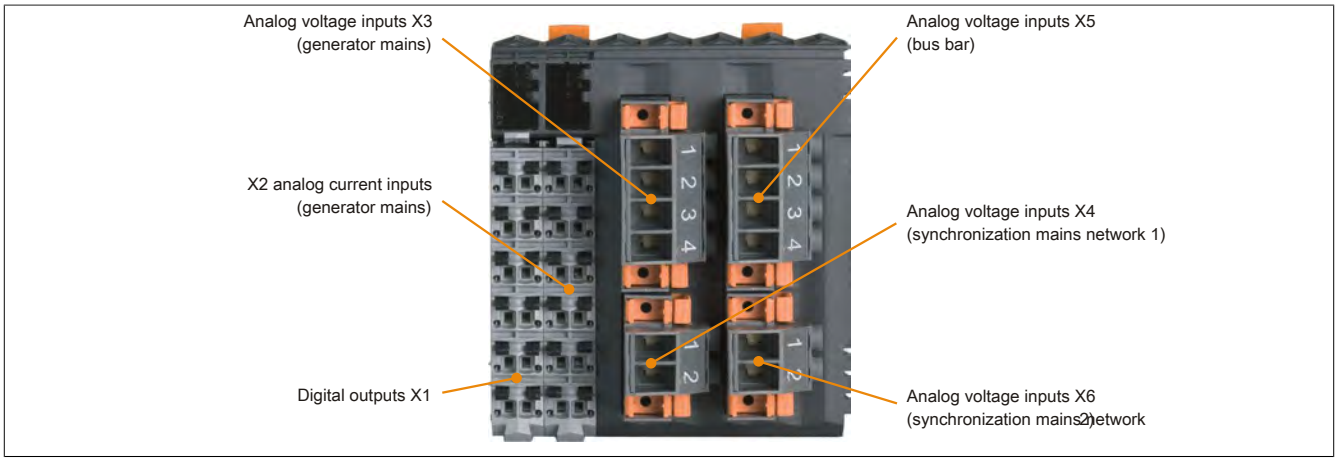
1) Depending on the configuration, a firmware update can take up to several minutes.

Status-LEDs right

Figure	LED[1]	Terminal	Color	Status	Description
	1	X3	Green	On	Measurement range: 120 VAC
			Red	On	Measurement range: 480 VAC
	2	X4	Green	On	Measurement range: 120 VAC
			Red	On	Measurement range: 480 VAC
	3	X5	Green	On	Measurement range: 120 VAC
			Red	On	Measurement range: 480 VAC
	4	X6	Green	On	Measurement range: 120 VAC
			Red	On	Measurement range: 480 VAC
	5	X2	Green	On	Measurement range: 1 A
			Red	On	Measurement range: 5 A

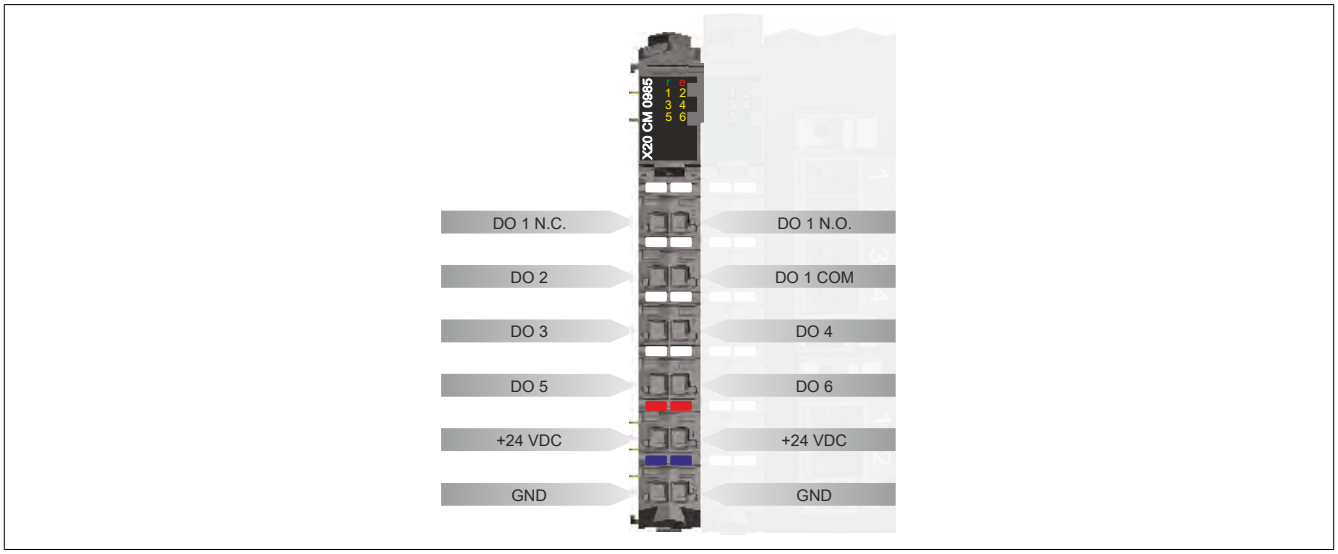
1) LEDs 1 - 5 are green/red dual LEDs.

4.26.3.6 Connection elements



4.26.3.7 Digital outputs X1

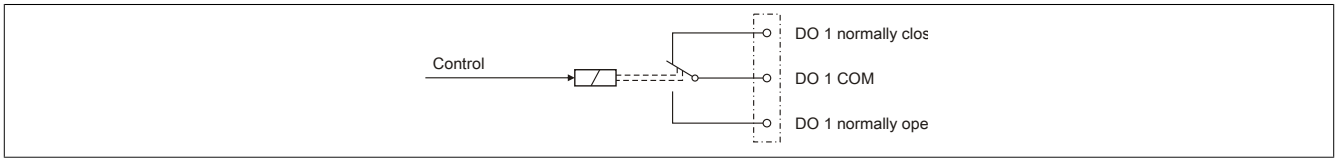
The X1 and X2 terminals can each be keyed differently to prevent them from being inadvertently plugged into the module incorrectly.



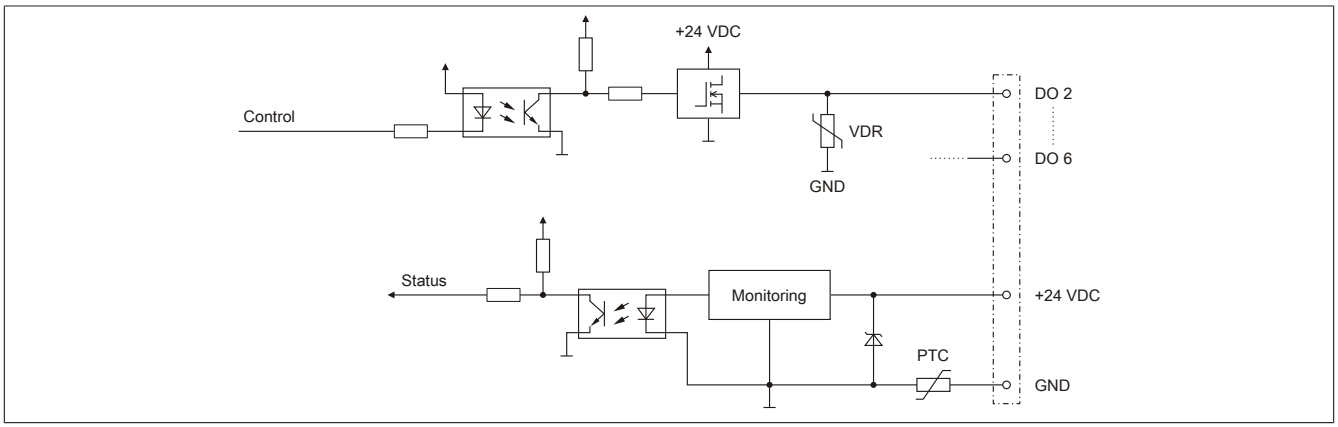
Function description of the digital outputs

Digital output	Description
DO1	This digital output is designed as a changeover contact switch. The monitoring relay allows selective monitoring of: • Overvoltage and undervoltage • Overfrequency and underfrequency • Voltage asymmetry • Current asymmetry • Calculated neutral conductor current (maximum) • Short circuit current • Rating-dependent overcurrent • Limit value of the capacitive reactive power (exciter failure)
DO2	DO2 serves as a meter output. The generated pulses can be recorded by an external energy meter (kWh).
DO3	This output is set when there is no voltage on the bus bar (below the lower limit of the defined parameter). 3-phase monitoring takes place for the bus bar voltage.
DO4	DO4 serves as a synchronization pulse. The power switch is activated by setting this output. The output is deactivated after the configured time has elapsed (exception: "Synchro check" operating mode).
DO5 and DO6	These outputs are freely available to the user.

DO1 - Output circuit diagram



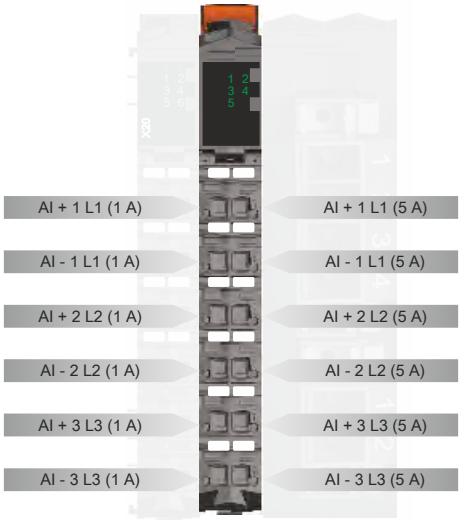
DO2 - DO 6 - Output circuit diagram



4.26.3.8 X2 analog current inputs

The X2 terminal measures the three phase currents of the generator mains using an externally connected current transformer. The measurement range of the current inputs can be configured as 1 A or 5 A.

The X1 and X2 terminals can each be keyed differently to prevent them from being inadvertently plugged into the module incorrectly.

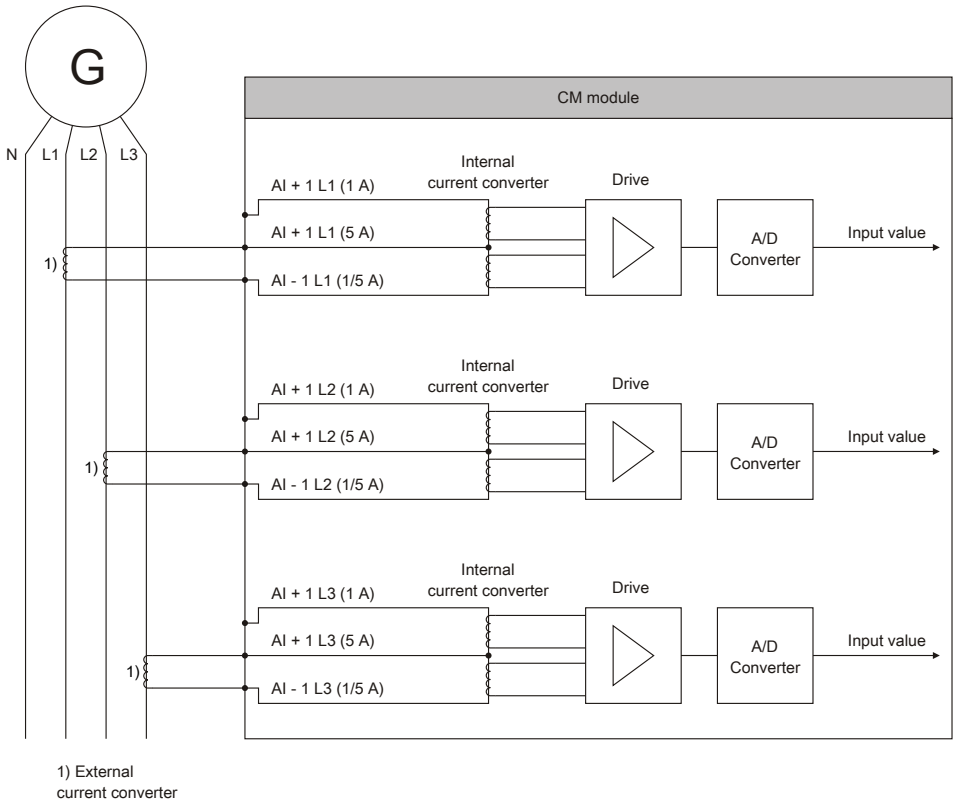


Danger!

Risk of electric shock!

The terminal block must only be allowed to conduct voltage when it is inserted. It must not under any circumstances be removed or inserted when voltage is applied or have voltage applied to it when it is removed.

Input circuit diagram - Analog current inputs

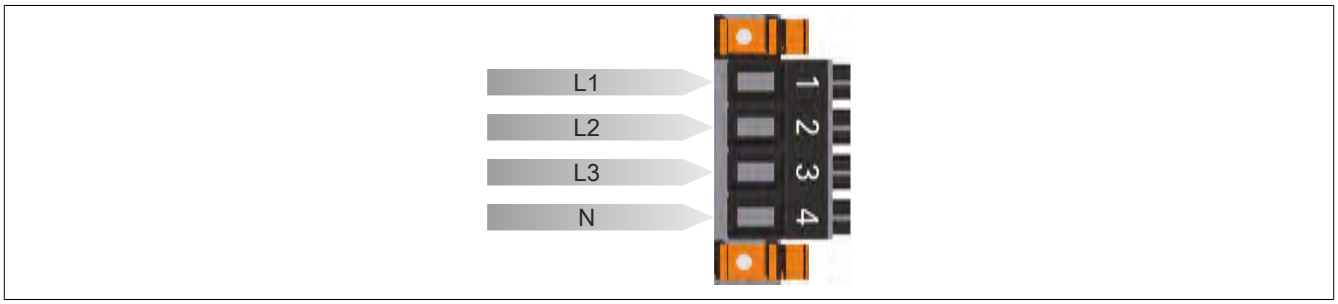


4.26.3.9 X3 and X5 analog voltage inputs

The X3 and X5 terminals are used to measure and monitor the line-to-line and phase voltages of the generator mains and bus bar.

- Terminal X3: Generator mains
- Terminal X5: Bus bar

The X3 and X5 terminals are each keyed differently to prevent them from being inadvertently plugged into the module incorrectly. Section 4.26.2.14 "Releasing the locking clip for terminals X3 - X6" describes how to release the terminal locking clip.

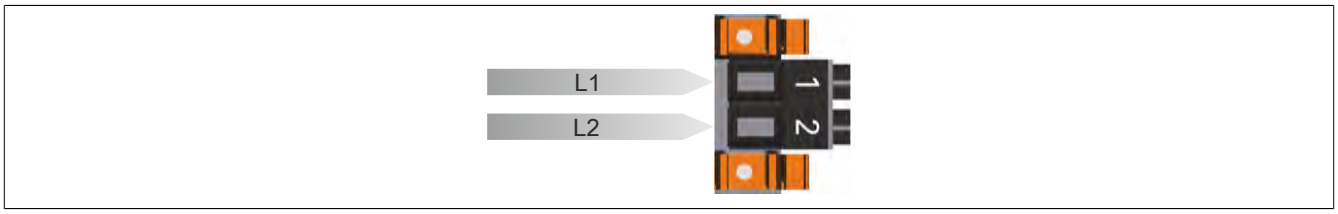


4.26.3.10 X4 and X6 analog voltage inputs

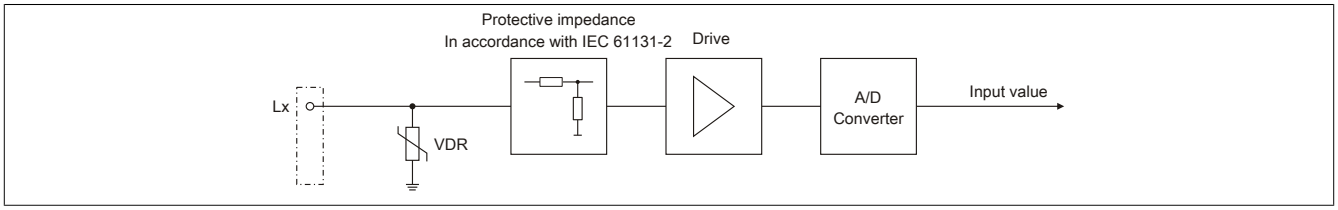
The voltage inputs on the X4 and X6 terminals are used to determine the line-to-line voltages for synchronization between two different mains networks.

- Terminal X4: Synchronization mains network 1
- Terminal X6: Synchronization mains network 2

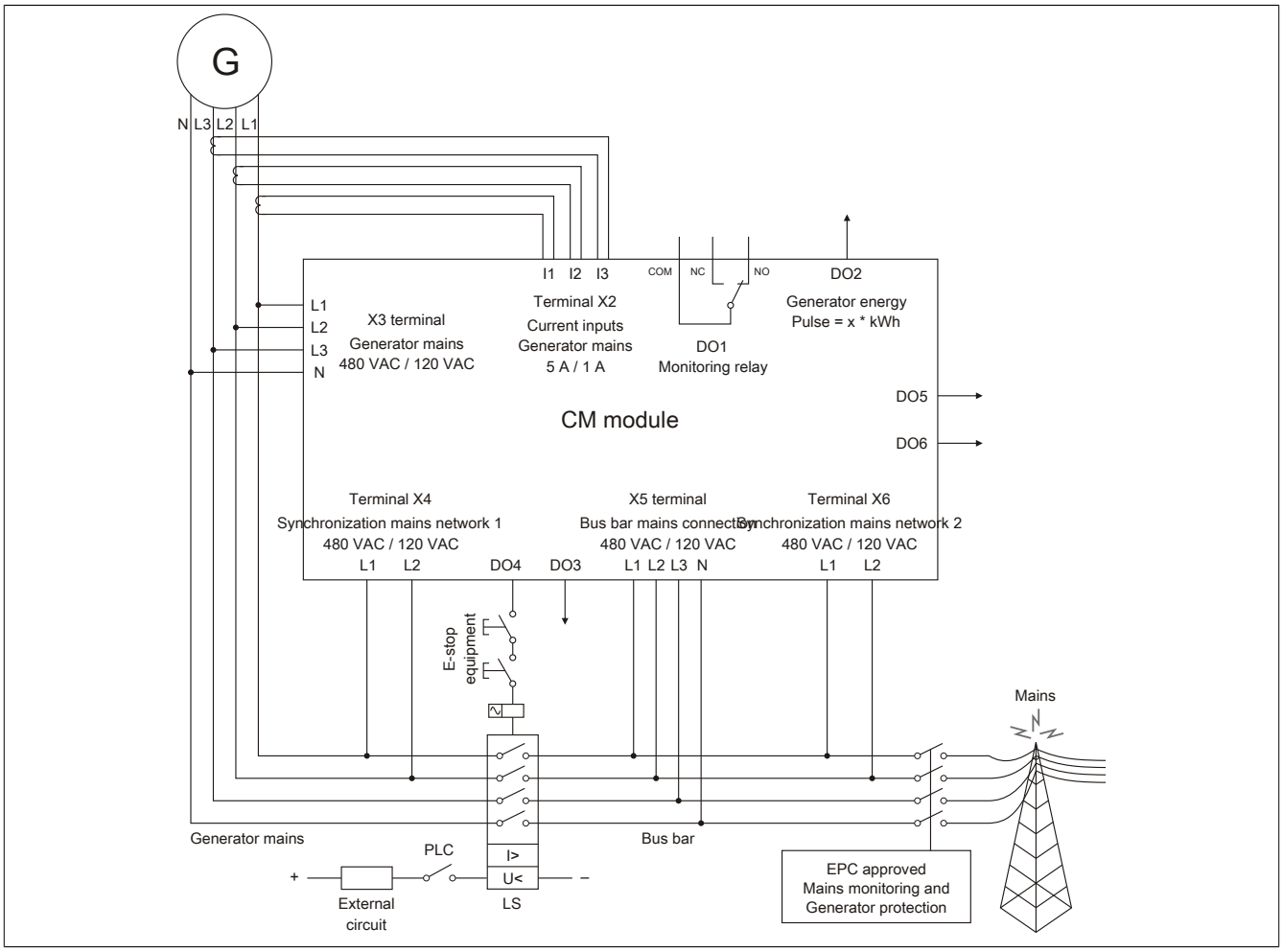
The X4 and X6 terminals are each keyed differently to prevent them from being inadvertently plugged into the module incorrectly. Section 4.26.2.14 "Releasing the locking clip for terminals X3 - X6" describes how to release the terminal locking clip.



Input circuit diagram, analog voltage inputs



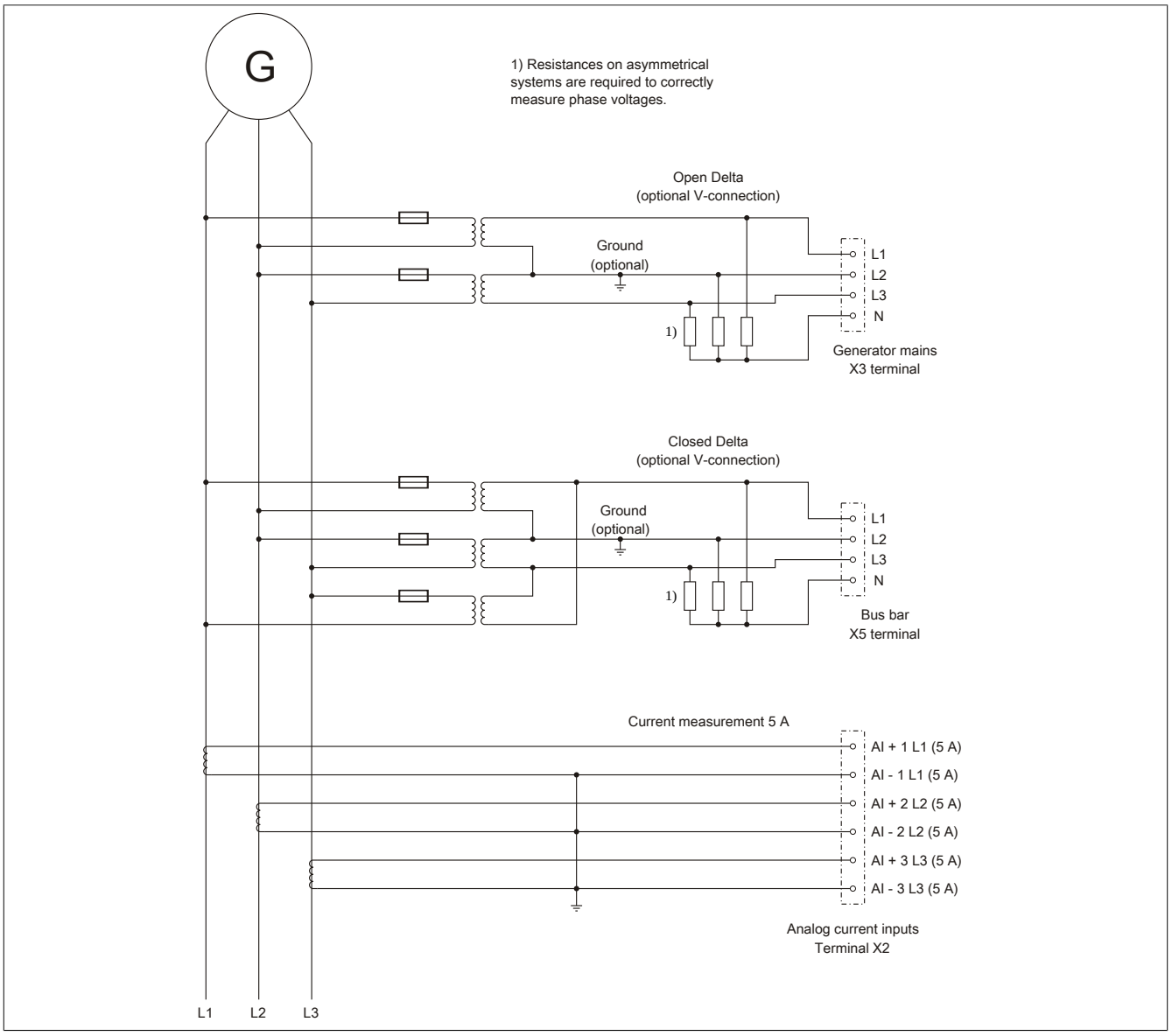
4.26.3.11 Circuit diagram



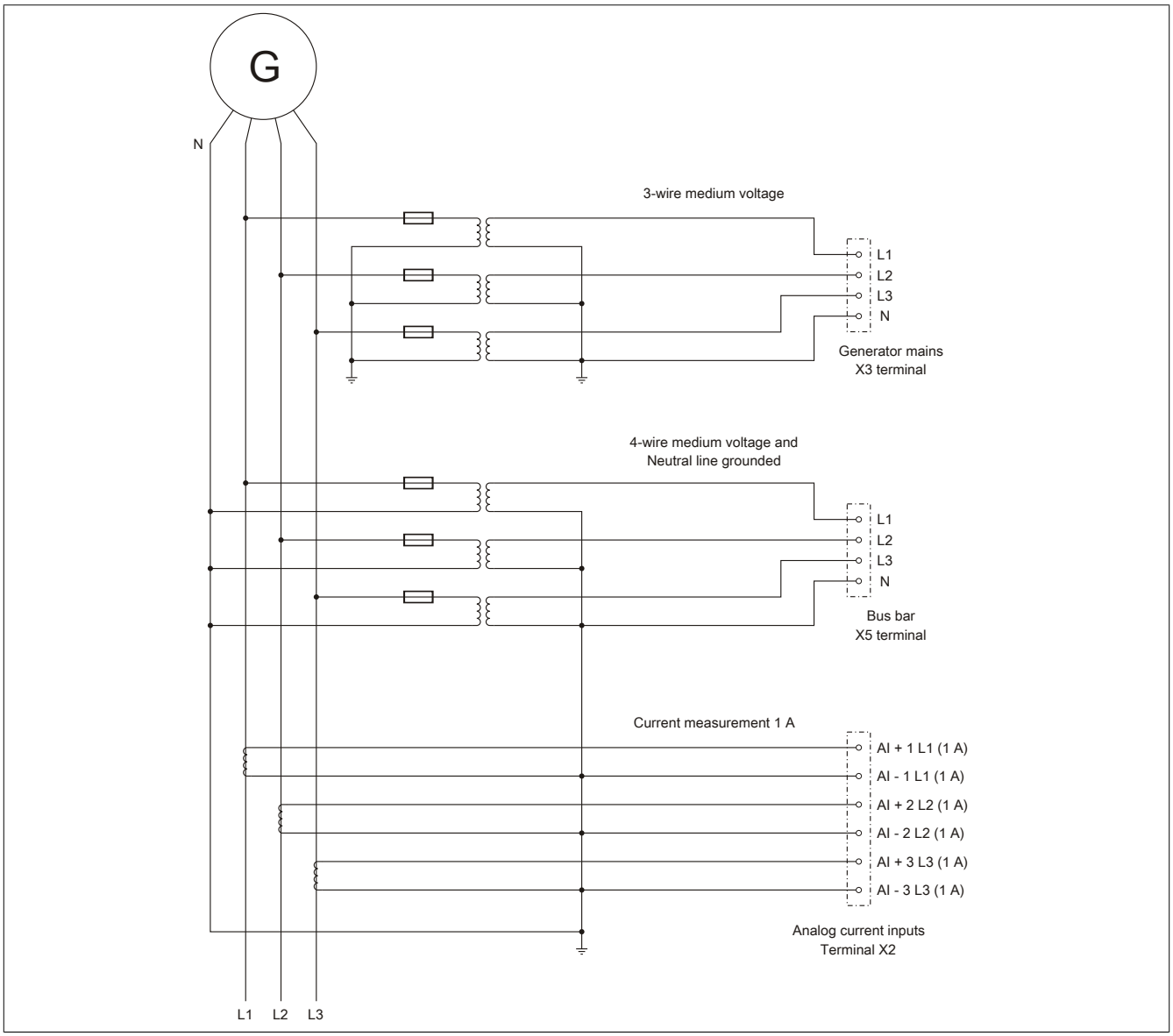
4.26.3.12 Typical connection examples for voltage/current measurement

For power measurement, the X3 terminal must always be used in connection with the X2 terminal! For single-phase measurement, always ensure that current input 1 is used for power measurement if voltage input 1 is being used. Otherwise, accurate power measurement is not possible for this phase!

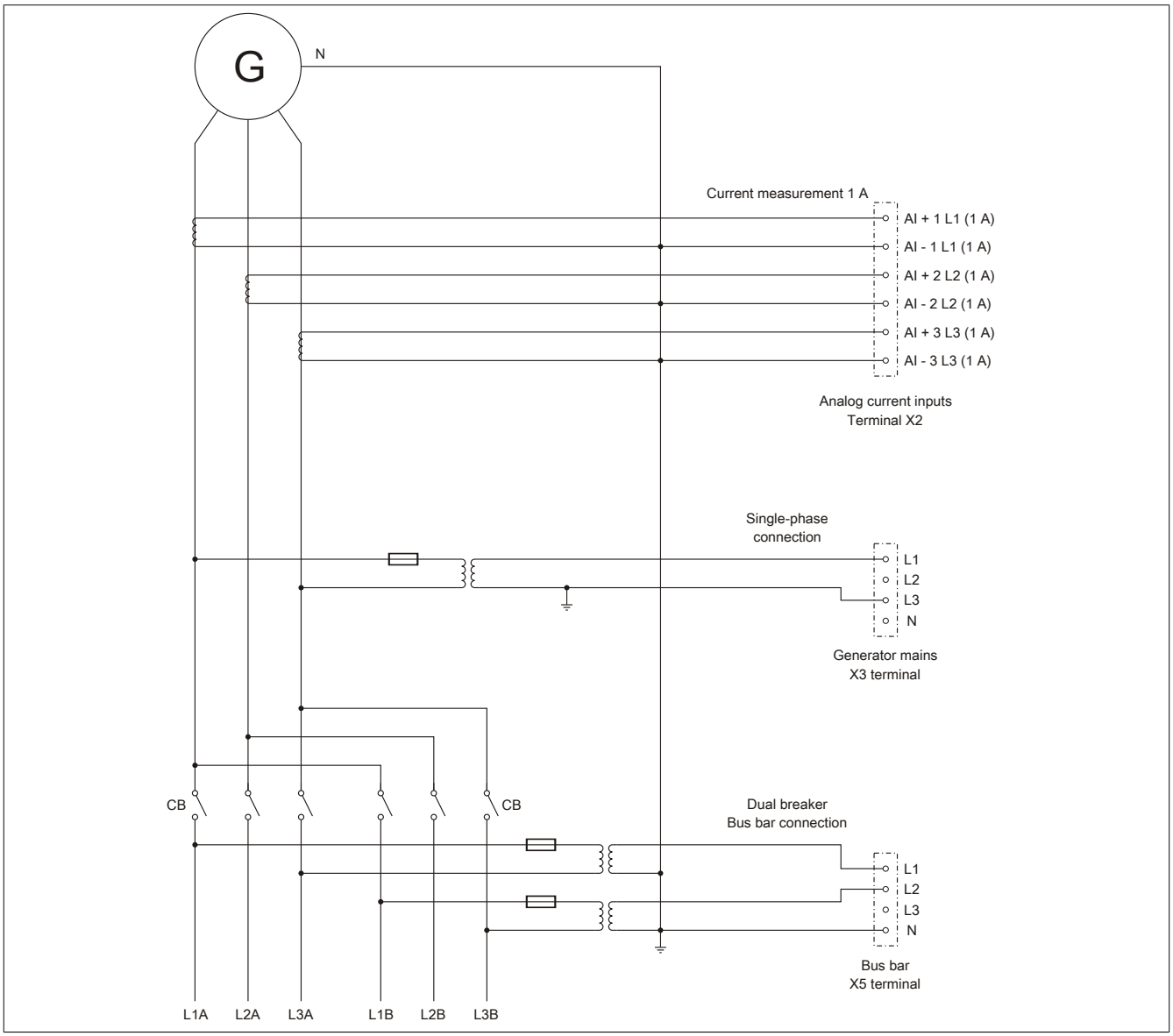
Connection example 1



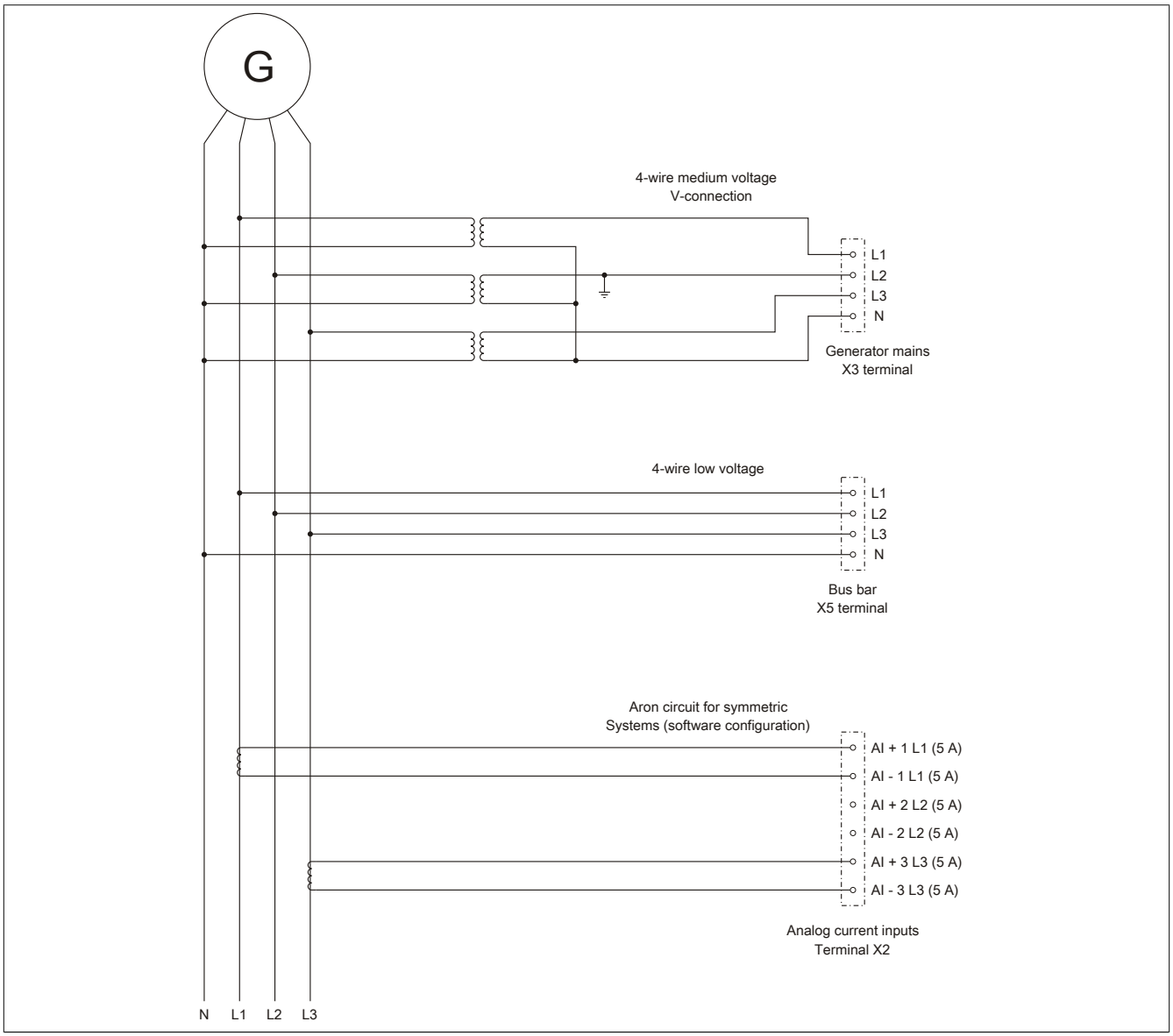
Connection example 2



Connection example 3

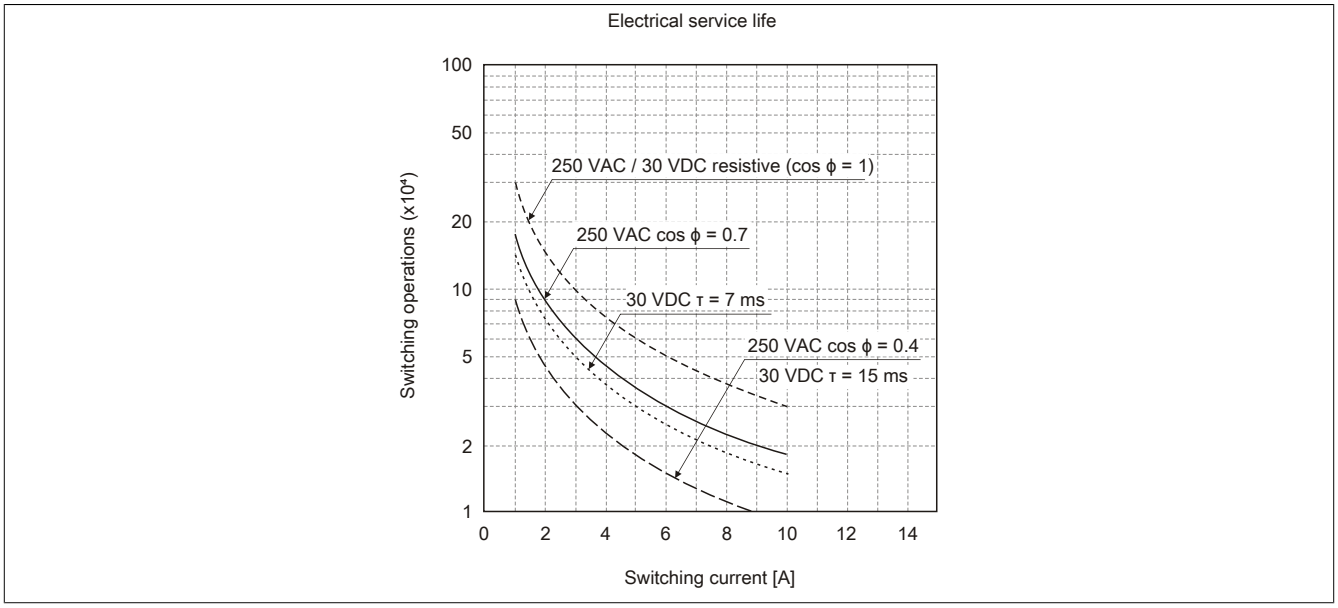


Connection example 4



4.26.3.13 Electrical service life

The electrical service life for the DO1 relay output can be seen in the following diagram.



4.26.3.14 Releasing the locking clip for terminals X3 - X6

Terminals X3 - X6 are equipped with a terminal locking clip. This clip attaches the terminal block securely to the electronic module. This prevents the terminal from accidentally being disconnected.

To release the locking clip, press inwards on the corrugated part of the lever with your fingertip (1) and then slide outwards (2). No additional tools are required for removing the terminal.

Terminals X5 and X6 must be removed first before terminals X3 and X4 can be removed.

4.26.3.15 Synchronization functions

The following three synchronization functions are available on the module:

- Synchronization with slip
- Synchro check
- Switching to voltage-free "dead bus"

Synchronization with slip

The following is valid for synchronization mains 1 and synchronization mains 2:

- 50% < U < 125% of the nominal voltage U_N
- 80% < f < 110% of the nominal frequency f_N

The generator voltage is adjusted to the synchronization voltage with regard to amplitude and frequency. Taking into account the configured phase angle (Δα), a defined transformer vector group and the switching response time, the switch-on command is calculated and transmitted in advance so that the main contacts of the power switch are closed at the point of synchronicity.

Synchronization occurs under the following conditions:

- The "Synchronization selection" command is set using a software application
- The device is ready.
- The configured limit for voltage difference is not exceeded (ΔU_{max}).
- The configured limits for frequency difference are not exceeded (Δf_{max} and Δf_{min}).
- The configured limit for the phase angle (including vector group transformer Δα) is not exceeded (j_{max}).

The actual synchronization is "authorized" if the condition for the phase angle is met the first time and the phase window is exited once. It should be noted that the conditions for voltage and frequency difference do not yet have to be fulfilled this first time.

This means that if the phase difference happens to lie within the phase window when the request is made, it is not necessary to re-enter the window for this "authorization" to take place. In order to abort synchronization when in an "authorized" state, the "Synchronization with slip" command must be reset.

After the synchronization command has been authorized, the synchronization window of all the aforementioned synchronization conditions must be entered again from any phase angle in order to obtain a synchronization impulse in accordance with the switch lead time.

At very low frequencies or equivalent frequencies and in adherence to the conditions described above, synchronization will also take place when entering the synchronization window a second time. The synchronization impulse is only issued at a phase angle = 0°, however.

At low differential frequencies, the switch is not immediately engaged when the phase window is reached. This only occurs when synchronization is possible at the point of synchronicity.

DO4 changes its state from Low to High when all conditions are met. It changes back from High to Low after the configured pulse duration has elapsed.

Synchro check

In this operating mode, the device can be used to check the synchronization. The DO4 output remains set as long as the following conditions are met:

- The "Enable Synchro Check" command is set using software.
- The device is ready.
- The configured limit for voltage difference is not exceeded (ΔU_{max}).
- The configured limits for frequency difference are not exceeded (Δf_{max} and Δf_{min}).
- The defined limit for the phase angle is not exceeded (ϕ_{max}).

DO4 stays at High as long as all conditions are met.

Switching to voltage-free "dead bus"

The switch-on command for the power switch is output without synchronization if the following conditions have been met:

- The "Enable Dead Bus" command is set using software.
- The device is ready.
- The bus bar does not have voltage applied: $U_B < U_{Bmin}$ as a percentage of U_{NomBus}

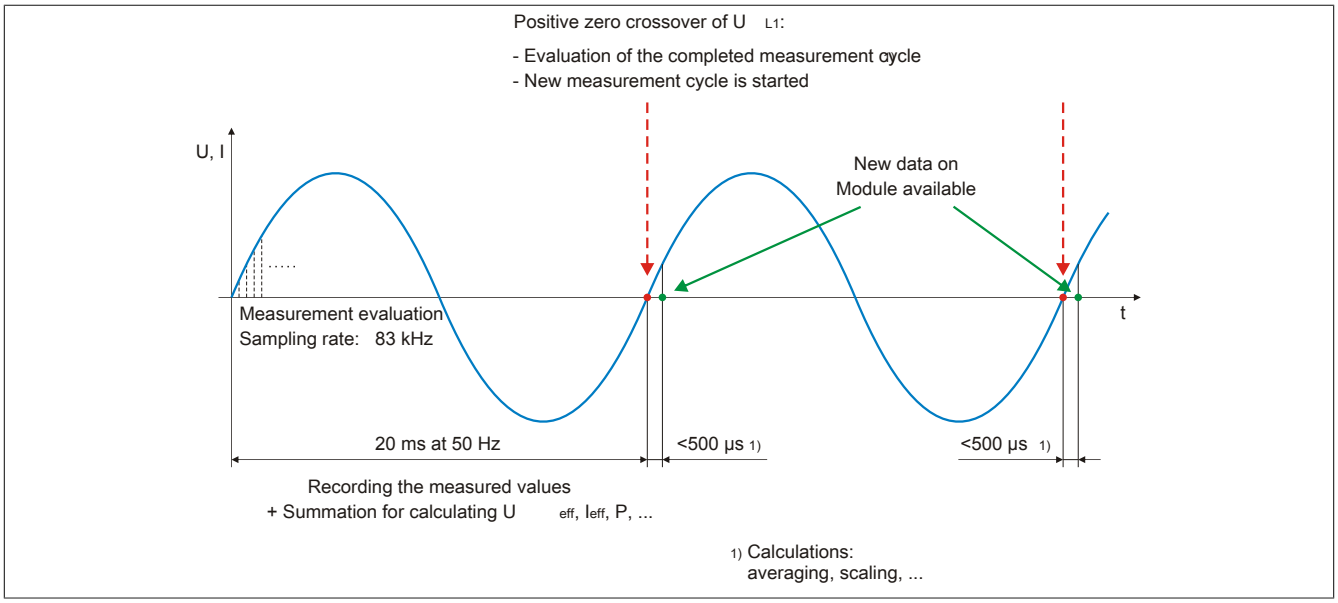
U_B ...	Bus bar phase voltage
U_{Bmin} ...	Minimum bus bar voltage
U_{NomBus} ...	Bus bar nominal voltage

- The generator voltage and frequency can be any valid value.

DO4 changes its state from Low to High when all conditions are met. It changes back from High to Low after the configured pulse duration has elapsed.

4.26.3.16 Measurement functions

Timing diagram



Measured parameters for generator mains (X3)

- Phase currents
- Current average
- Dynamic current average
- Neutral current
- Line-to-line voltages
- Phase voltages
- Voltage average
- Total apparent power
- Total reactive power
- Total active power
- Active power factor
- Frequency

Measured parameters between synchronization mains networks

- Differential angle
- Differential voltage

Rating-dependent overcurrent

Rating-dependent overcurrent monitoring is in accordance with the specifications of IEC 255-8 "Electrical relay; Relay for protecting against thermal overload (overload relay)" and IEC 255-17 "Electrical relay; Relay for protecting against the thermal overload of motors (overload relay for motors).

Dependent delayed imbalanced load monitoring

Dependent delayed imbalanced load monitoring protects against imbalanced loads in three-phase generators and three-phase mains. Parameters can be changed to make it possible to match the trigger characteristics to different generator types while taking their special thermal time constants into consideration.

An imbalanced load can be caused by uneven current distribution in the mains due to imbalanced load, asymmetrical short circuits, line interruptions or switching operations. Imbalanced loads result in reverse system currents in the stator, which causes harmonics with an uneven ordinal number in the stator winding and harmonics with an even ordinal number in the rotor winding. The rotor is at particular risk here because the harmonic waves place an additional load on the rotor winding and induce eddy currents in the rotor's solid iron, which may melt the metal or destroy the metallic structure.

An imbalanced load can be permissible within certain limits, however, when accounting for the thermal load limit of the generator. To avoid premature failure of the generator when an imbalanced load occurs, the characteristics that trigger imbalanced load protection should be adapted to the thermal characteristics of the generator. Imbalanced load protection can also be triggered by external errors in the mains caused by asymmetric short circuits.

Short circuit current monitoring

If overcurrent or a short circuit occurs and the limit value is exceeded, the error message "Overcurrent / Short circuit" is signaled after the configured time delay has passed.

Voltage asymmetry monitoring

The trigger value, which is adjustable by percentage, is always based on the respective average voltage of the linked generator voltages. This value defines the maximum permitted deviation of one of the three differential voltages between the three monitored, interlinked phase voltages.

If this value is exceeded in either direction, the error notification "Asymmetrical voltage" is indicated after the configured time delay has passed.

Bus bar voltage measurement and zero voltage monitoring

3-phase monitoring takes place for the bus bar voltage. The measured values are represented as phase-to-phase and phase-to-neutral values. The D03 output is set when there is no voltage (below the lower dead bus limit) on the bus bar (X5 terminal).

This monitoring can be used to determine which synchronization function should be used.

Synchronization function	Bus bar voltage measurement
Dead bus	No voltage is being supplied to the bus bar or the value is below the lower limit parameter. Output DO3 is set.
Synchronization with slip	The voltage measured on the bus bar is above the defined parameter value. Output DO3 is not set.

Exciter failure

The reactive power monitoring can be used to protect a generator against operating in the impermissible range. The capacitive reactive power monitor offers protection against under-excitation (exciter failure). If the lower limit is exceeded (in the negative direction), the error message "Exciter failure" is signaled after the configured time delay has passed.

4.26.3.17 Register description

4.26.3.17.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.3.17.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Generator mains - Configuration						
2582	ConfigOutput02 Nominal voltage of generator mains (U_{NomGen})	UINT				•
2590	ConfigOutput04 Nominal current of generator mains (I_{Nom})	UINT				•
2598	ConfigOutput06 Multiplier for generator mains	UINT				•
2610	ConfigOutput09 Multiplier for current transformer	UINT				•
2658	ConfigOutput16 Overvoltage limit of generator mains (U_{max})	UINT				•
2561	ConfigOutput20 Nominal voltage range of generator mains	USINT				•
2569	ConfigOutput24 Nominal current range of the generator mains	USINT				•
2571	ConfigOutput25 Aron circuit	USINT				•
2662	ConfigOutput27 Undervoltage limit of generator mains (U_{min})	UINT				•
2782	ConfigOutput41 Low-pass filter for total power ratings	UINT				•
Generator monitoring functions - Configuration						
2614	ConfigOutput10 Nominal frequency (f_{Nom})	UINT				•
2710	ConfigOutput26 Response time for generator overvoltage (U_{max})	UINT				•
2718	ConfigOutput28 Response time for generator undervoltage (U_{min})	UINT				•
2666	ConfigOutput29 Generator over-frequency (f_{max})	UINT				•
2726	ConfigOutput30 Response time for generator over-frequency (f_{max})	UINT				•
2670	ConfigOutput31 Generator under-frequency (f_{min})	UINT				•
2734	ConfigOutput32 Response time for generator under-frequency (f_{min})	UINT				•
2674	ConfigOutput33 Generator voltage asymmetry (U_{as})	UINT				•
2742	ConfigOutput34 Response time for generator voltage asymmetry (U_{as})	UINT				•
2774	ConfigOutput35 Load time constant for current asymmetry	UINT				•
2678	ConfigOutput36 Maximum limit of neutral conductor current	UINT				•
2750	ConfigOutput37 Response time for neutral conductor current monitor	UINT				•
2682	ConfigOutput38 Short circuit current	UINT				•
2758	ConfigOutput39 Response time for short circuit current	UINT				•
2686	ConfigOutput42 Rating-dependent overcurrent	UINT				•
2690	ConfigOutput43 Integration coefficient for rating-dependent overcurrent (iths)	UINT				•
2694	ConfigOutput44 Capacitive reactive power	INT				•
2766	ConfigOutput45 Response time for reactive power monitoring	UINT				•
2698	ConfigOutput57 DO1 function	UINT				•
Busbar - Configuration						
2586	ConfigOutput03 Busbar nominal voltage (U_{NomBus})	UINT				•

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2594	ConfigOutput05 Multiplier for busbar	UINT				•
2563	ConfigOutput21 Nominal voltage range of busbar	USINT				•
2650	ConfigOutput40 Minimum busbar voltage (U_{Bmin})	UINT				•
Synchronization - Configuration						
518	ConfigOutput Synchronization mode	USINT			•	
2578	ConfigOutput01 Nominal voltage of synchronization mains (U_{NomSyn})	UINT				•
2602	ConfigOutput07 Multiplier for synchronization mains	UINT				•
2606	ConfigOutput08 Multiplier for synchronization mains	UINT				•
2626	ConfigOutput11 Max. differential frequency (df_{max})	UINT				•
2630	ConfigOutput12 Min. differential frequency (df_{min})	INT				•
2634	ConfigOutput13 Max. differential voltage (dU_{max})	UINT				•
2638	ConfigOutput14 Max. permitted differential angle (ϕ_{Max})	UINT				•
2618	ConfigOutput15 Phase rotation of sync mains 1 (dα)	UINT				•
2565	ConfigOutput22 Nominal voltage range of synchronization mains	USINT				•
2567	ConfigOutput23 Nominal voltage range of synchronization mains	USINT				•
2794	ConfigOutput47 Pulse duration of the turn-on delay	UINT				•
2798	ConfigOutput48 Switching response time of the power switch	UINT				•
2654	ConfigOutput56 Synchronization configuration	UINT				•
2622	ConfigOutput58 Dead bus voltage	UINT				•
Maximum value buffer and power meter - Configuration						
2790	ConfigOutput46 Pulse value of energy meter output	UINT				•
2950	ConfigOutput49 Maximum phase current I1	INT		•		
2054	ConfigOutput50 Maximum phase current I2	INT		•		
2058	ConfigOutput51 Maximum phase current I3	INT		•		
2062	ConfigOutput52 Maximum total active power	INT		•		
2066	ConfigOutput53 Maximum neutral conductor current	INT		•		
2076	ConfigOutput54 Active energy counter	DINT		•		
2084	ConfigOutput55 Reactive energy counter	DINT		•		
2834	ConfigOutput60 Reset maximum phase current I1	INT				•
2838	ConfigOutput61 Reset maximum phase current I2	INT				•
2842	ConfigOutput62 Reset maximum phase current I3	INT				•
2846	ConfigOutput63 Resets maximum total active power	INT				•
2850	ConfigOutput64 Resets maximum neutral conductor current	INT				•
2860	ConfigOutput66 Reset active energy meter	DINT				•
2868	ConfigOutput67 Write to reactive energy meter	DINT				•
General registers - Communication						
514	DigitalOutput Digital outputs 05 to 06	USINT			•	
	DigitalOutput05	Bit 0				
	DigitalOutput06	Bit 1				
126	Status of digital outputs Status of digital outputs	UINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput06	Bit 5				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
	StatusInput17	Bit 6				
	StatusInput16	Bit 7				
122	Error registers Error registers	UINT	•			
	StatusInput01	Bit 0				
	...	...				
	StatusInput15	Bit 14				
Generator mains measured values - Communication						
2	AnalogInput01 Phase current I1	INT	•			
6	AnalogInput02 Phase current I2	INT	•			
10	AnalogInput03 Phase current I3	INT	•			
14	AnalogInput04 Current average I1, I2, I3	INT	•			
18	AnalogInput05 Neutral conductor current In	INT	•			
22	AnalogInput06 Current average, dynamic (Im_dyn)	UINT	•			
26	AnalogInput07 Line-to-line voltage UG12	INT	•			
30	AnalogInput08 Line-to-line voltage UG23	INT	•			
34	AnalogInput09 Line-to-line voltage UG31	INT	•			
38	AnalogInput10 Phase voltage UG1	INT	•			
42	AnalogInput11 Phase voltage UG2	INT	•			
46	AnalogInput12 Phase voltage UG3	INT	•			
74	AnalogInput19 Total active power filtered P/P_H1	INT	•			
78	AnalogInput20 Total reactive power filtered Q/Q_H1	INT	•			
82	AnalogInput21 Total apparent power filtered Q/S_H1	INT	•			
86	AnalogInput22 Voltage average UG12, UG23, UG31	INT	•			
90	AnalogInput23 Power factor of generator/cos ϕ	INT	•			
94	AnalogInput24 Frequency of the generator mains	UINT	•			
Measured values for busbar - Communication						
50	AnalogInput13 Line-to-line voltage of busbar UB12	INT	•			
54	AnalogInput14 Line-to-line voltage of busbar UB23	INT	•			
58	AnalogInput15 Line-to-line voltage of busbar UB31	INT	•			
62	AnalogInput16 Phase voltage of busbar UB1	INT	•			
66	AnalogInput17 Phase voltage of busbar UB2	INT	•			
70	AnalogInput18 Phase voltage of busbar UB3	INT	•			
Measured values of synchronization mains - Communication						
98	AnalogInput25 Line-to-line voltage of sync mains 1 US1	INT	•			
102	AnalogInput26 Line-to-line voltage of sync mains 2 US2	INT	•			
106	AnalogInput27 Frequency of sync mains 1	UINT	•			
110	AnalogInput28 Frequency of sync mains 2	UINT	•			
114	AnalogInput29 Differential angle between sync mains	INT	•			
118	AnalogInput30 Differential voltage between sync mains	INT	•			

4.26.3.17.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Generator mains - Configuration							
2582	-	ConfigOutput02 Nominal voltage of generator mains	UINT				●
2590	-	ConfigOutput04 Nominal current of generator mains	UINT				●
2598	-	ConfigOutput06 Multiplier for generator mains	UINT				●
2610	-	ConfigOutput09 Multiplier for current transformer	UINT				●
2658	-	ConfigOutput16 Overvoltage limit of generator mains	UINT				●
2561	-	ConfigOutput20 Nominal voltage range of generator mains	USINT				●
2569	-	ConfigOutput24 Nominal current range of the generator mains	USINT				●
2571	-	ConfigOutput25 Aron circuit	USINT				●
2662	-	ConfigOutput27 Undervoltage limit of generator mains	UINT				●
2782	-	ConfigOutput41 Low-pass filter for total power ratings	UINT				●
Generator monitoring functions - Configuration							
2614	-	ConfigOutput10 Rated frequency	UINT				●
2710	-	ConfigOutput26 Response time for generator overvoltage	UINT				●
2718	-	ConfigOutput28 Response time for generator undervoltage	UINT				●
2666	-	ConfigOutput29 Generator overfrequency	UINT				●
2726	-	ConfigOutput30 Response time for generator overfrequency	UINT				●
2670	-	ConfigOutput31 Generator underfrequency	UINT				●
2734	-	ConfigOutput32 Response time for generator underfrequency	UINT				●
2674	-	ConfigOutput33 Generator voltage asymmetry	UINT				●
2742	-	ConfigOutput34 Response time for generator asymmetry	UINT				●
2774	-	ConfigOutput35 Load time constant for current asymmetry	UINT				●
2678	-	ConfigOutput36 Maximum limit of neutral conductor current	UINT				●
2750	-	ConfigOutput37 Response time for neutral conductor current monitor	UINT				●
2682	-	ConfigOutput38 Short circuit current	UINT				●
2758	-	ConfigOutput39 Response time for short circuit current	UINT				●
2686	-	ConfigOutput42 Rating-dependent overcurrent	UINT				●
2690	-	ConfigOutput43 Integration coefficient Overcurrent	UINT				●
2694	-	ConfigOutput44 Capacitive reactive power	INT				●
2766	-	ConfigOutput45 Response time for reactive power monitoring	UINT				●
2698	-	ConfigOutput57 DO1 function	UINT				●
Busbar - Configuration							
2586	-	ConfigOutput03 Nominal voltage of busbar	UINT				●
2594	-	ConfigOutput05 Multiplier for busbar	UINT				●
2563	-	ConfigOutput21 Nominal voltage range of busbar	USINT				●
2650	-	ConfigOutput40 Minimum busbar voltage	UINT				●
Synchronization - Configuration							
518	2	ConfigOutput Synchronization mode	USINT			●	
2578	-	ConfigOutput01 Nominal voltage range of sync mains 1	UINT				●
2602	-	ConfigOutput07 Multiplier for sync mains 2	UINT				●

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
2606	-	ConfigOutput08 Multiplier for sync mains	UINT				•
2626	-	ConfigOutput11 Maximum permitted difference frequency	UINT				•
2630	-	ConfigOutput12 Minimum permitted difference frequency	INT				•
2634	-	ConfigOutput13 Maximum permitted differential voltage	UINT				•
2638	-	ConfigOutput14 Maximum permitted differential angle	UINT				•
2618	-	ConfigOutput15 Phase rotation of sync mains 1	UINT				•
2565	-	ConfigOutput22 Nominal voltage of sync mains 1	USINT				•
2567	-	ConfigOutput23 Nominal voltage of sync mains 2	USINT				•
2794	-	ConfigOutput47 Pulse duration of the turn-on delay	UINT				•
2798	-	ConfigOutput48 Switching response time of the power switch	UINT				•
2654	-	ConfigOutput56 Synchronization configuration	UINT				•
2622	-	ConfigOutput58 Dead bus voltage	UINT				•
Maximum value buffer and power meter - Configuration							
2790	-	ConfigOutput46 Pulse value of energy meter output	UINT				•
2950	-	ConfigOutput49 Maximum phase current I1	INT		•		
2054	-	ConfigOutput50 Maximum phase current I2	INT		•		
2058	-	ConfigOutput51 Maximum phase current I3	INT		•		
2062	-	ConfigOutput52 Maximum total active power	INT		•		
2066	-	ConfigOutput53 Maximum neutral conductor current	INT		•		
2076	-	ConfigOutput54 Active energy counter	DINT		•		
2084	-	ConfigOutput55 Reactive energy counter	DINT		•		
2834	-	ConfigOutput60 Reset maximum phase current I1	INT				•
2838	-	ConfigOutput61 Reset maximum phase current I2	INT				•
2842	-	ConfigOutput62 Reset maximum phase current I3	INT				•
2846	-	ConfigOutput63 Resets maximum total active power	INT				•
2850	-	ConfigOutput64 Resets maximum neutral conductor current	INT				•
2860	-	ConfigOutput66 Reset active energy meter	DINT				•
2868	-	ConfigOutput67 Write to reactive energy meter	DINT				•
General registers - Communication							
514	0	DigitalOutput Digital outputs 05 to 06	USINT			•	
		DigitalOutput05	Bit 0				
		DigitalOutput06	Bit 1				
126	62	Status of digital outputs Status of digital outputs	UINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput06	Bit 5				
		StatusInput17	Bit 6				
		StatusInput16	Bit 7				
122	60	Error registers Error registers	UINT	•			
		StatusInput01	Bit 0				
		...	...				
		StatusInput15	Bit 14				
Generator mains measured values - Communication							
2	16	AnalogInput01 Phase current I1	INT	•			
6	18	AnalogInput02 Phase current I2	INT	•			

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
10	20	AnalogInput03 Phase current I3	INT	●			
14	46	AnalogInput04 Current average I1, I2, I3	INT	●			
18	22	AnalogInput05 Neutral conductor current In	INT	●			
22	38	AnalogInput06 Current average, dynamic	UINT	●			
26	0	AnalogInput07 Line-to-line voltage UG12	INT	●			
30	2	AnalogInput08 Line-to-line voltage UG23	INT	●			
34	4	AnalogInput09 Line-to-line voltage UG31	INT	●			
38	8	AnalogInput10 Phase voltage UG1	INT	●			
42	10	AnalogInput11 Phase voltage UG2	INT	●			
46	12	AnalogInput12 Phase voltage UG3	INT	●			
74	40	AnalogInput19 Total active power filtered P/P_H1	INT	●			
78	42	AnalogInput20 Total reactive power filtered Q/Q_H1	INT	●			
82	44	AnalogInput21 Total apparent power filtered Q/S_H1	INT	●			
86	14	AnalogInput22 Voltage average UG12, UG23, UG31	INT	●			
90	30	AnalogInput23 Power factor of generator/cos ϕ	INT	●			
94	6	AnalogInput24 Frequency of the generator mains	UINT	●			
Measured values for busbar - Communication							
50	32	AnalogInput13 Line-to-line voltage of busbar UB12	INT	●			
54	34	AnalogInput14 Line-to-line voltage of busbar UB23	INT	●			
58	36	AnalogInput15 Line-to-line voltage of busbar UB31	INT	●			
62	24	AnalogInput16 Phase voltage of busbar UB1	INT	●			
66	26	AnalogInput17 Phase voltage of busbar UB2	INT	●			
70	28	AnalogInput18 Phase voltage of busbar UB3	INT	●			
Measured values of synchronization mains - Communication							
98	48	AnalogInput25 Line-to-line voltage of sync mains 1 US1	INT	●			
102	50	AnalogInput26 Line-to-line voltage of sync mains 2 US2	INT	●			
106	52	AnalogInput27 Frequency of sync mains 1	UINT	●			
110	54	AnalogInput28 Frequency of sync mains 2	UINT	●			
114	56	AnalogInput29 Differential angle between sync mains	INT	●			
118	58	AnalogInput30 Differential voltage between sync mains	INT	●			

1) The offset specifies the position of the register within the CAN object.

4.26.3.17.3.1 CAN I/O bus controller

The module occupies 8 analog logical slots on CAN-I/O.

4.26.3.17.4 Configuration registers

4.26.3.17.4.1 Generator mains

Nominal voltage of generator mains (U_{NomGen})

Name:
ConfigOutput02

This is needed for converting the percentages based on this nominal value into physical units.

Data type	Value	Information	Resolution
UINT	70 to 65000	Corresponds to 70 to 65000 V	1 V

Nominal current of generator mains (I_{Nom})

Name:
ConfigOutput04

This is needed for converting the percentages based on this nominal value into physical units.

Data type	Value	Information	Resolution
UINT	0 to 65000	Corresponds to 0 to 65000 A	1 A

Multiplier for generator mains

Name:
ConfigOutput06

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

The value 100 corresponds to a multiplication factor of 1 (measured value not changed).

Data type	Value	Information	Resolution
UINT	1 to 65535	Corresponds to 0.01 to 655.35	0.01

Multiplier for current transformer

Name:
ConfigOutput09

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

Data type	Value	Information	Resolution
UINT	1 to 65535	Corresponds to 1 to 65535	1

Overvoltage limit of generator mains (U_{max})

Name:
ConfigOutput16

If the value of one of the linked generator voltages exceeds the value set here, then the "Overvoltage" error message (register "StatusInputPacked04") is indicated after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	0 to 2000	Corresponds to 0 to 200% of U_{NomGen}	0.1%

Nominal voltage range of generator mains

Name:
ConfigOutput20

Can be toggled between 100 and 400 V.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Voltage	0	100 V
		1	400 V
1 - 7	Reserved	-	

Nominal current range of the generator mains

Name:
ConfigOutput24

Can be toggled between 1 and 5 A.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Current range	0	1 A
		1	5 A
1 - 7	Reserved	-	

Aron circuit

Name:
ConfigOutput25

Switch to power measurement principle of Aron circuit.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Aron circuit	0	Disabled: Three-phase supply with neutral line
		1	Enabled: Three-phase supply without neutral line
1 - 7	Reserved	-	

Undervoltage limit of generator mains (U_{min})

Name:
ConfigOutput27

If the value of one of the linked generator voltages falls below the value set here, then the "Undervoltage" error message (register "Error register") is indicated after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	0 to 2000	Corresponds to 0 to 200% of U_{NomGen}	0.1%

Low-pass filter for total power ratings

Name:
ConfigOutput41

Parameter for the response time of the low-pass filter of the total power values P, Q and S. The maximum total power values are recorded independently of this without being filtered.

This parameter is used as a delay element so that current or voltage fluctuations have less effect on how the calculated power values are represented. The damping behavior of the low-pass filter acts in accordance with the configurable time constant of a decaying e-function.

Data type	Value	Information	Resolution
UINT	0 to 300	Corresponds to 0 to 300 ms	1 ms

4.26.3.17.4.2 Generator monitoring

Nominal frequency (f_{Nom})

Name:
ConfigOutput10

This is needed for converting the percentages based on this nominal value into physical units.

Data type	Value	Information	Resolution
UINT	480 to 620	corresponds to 48 to 62 Hz.	0.1 Hz

Response time for generator overvoltage (U_{max})

Name:
ConfigOutput26

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

Data type	Value	Information	Resolution
UINT	5 to 100	Corresponds to 0.5 to 10 s	0.1 s

Response time for generator undervoltage (U_{min})

Name:
ConfigOutput28

The error is only triggered if the response value is exceeded in the negative direction without interruption for as long as is specified in this register.

Data type	Value	Information	Resolution
UINT	5 to 100	Corresponds to 0.5 to 10 s	0.1 s

Generator over-frequency (f_{max})

Name:
ConfigOutput29

If the value of the generator frequency exceeds the percentage of the nominal frequency set here, then the error message "Overfrequency" is indicated (register "Error register") and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of f_{Nom}	0.1%

Response time for generator over-frequency (f_{max})

Name:
ConfigOutput30

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 for 10 s	0.1 s

Generator under-frequency (f_{min})

Name:
ConfigOutput31

If the value of the generator frequency falls below the percentage of the nominal frequency set here, then the error message "Underfrequency" is indicated (register "Error register") and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	0 to 2000	For 0 to 200% of f_{Nom}	0.1%

Response time for generator under-frequency (f_{min})

Name:
ConfigOutput32

The error is only triggered if the response value is exceeded in the negative direction without interruption for as long as is specified in this register.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

Generator voltage asymmetry (U_{as})

Name:
ConfigOutput33

The trigger value, which is adjustable by percentage, is always based on the respective average voltage of the linked generator voltages. If the value of the voltage difference exceeds or falls below the value set here, then the "Voltage asymmetry" error message is indicated (register "Error register") after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	0 to 300	For 0 to 30% of U~3average	0.1%

Response time for generator voltage asymmetry (U_{as})

Name:
ConfigOutput34

This error is triggered only if the response value is exceeded without interruption (in either the positive or negative direction) for as long as is specified in this register.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

Load time constant for current asymmetry

Name:
ConfigOutput35

The dependent delayed unbalanced load monitoring function continually monitors the AC currents coming from the main current converters and continually calculates the present unbalanced load current. This is compared with the threshold value, which is calculated using the load time constants. If this threshold value is exceeded, the error message "Current asymmetry" is indicated (register "Error register") and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	1 to 65535	For 0.1 to 6553.5 s	0.1 s

Dependent delayed unbalanced load monitoring

Unbalanced load monitoring protects against unbalanced load in three-phase generators and three-phase mains. Parameters can be changed to make it possible to match the trigger characteristics to different generator types while taking their special thermal time constants into consideration.

An unbalanced load can be caused by uneven current distribution in the mains due to unbalanced load, asymmetrical short circuits, line interruptions or switching operations. Unbalanced loads result in reverse system currents in the stator, which causes harmonics with an uneven ordinal number in the stator winding and harmonics with an even ordinal number in the rotor winding. The rotor is at particular risk here because the harmonic waves place an additional load on the rotor winding and induce eddy currents in the rotor's solid iron, which may melt the metal or destroy the metallic structure.

An unbalanced load can be permissible within certain limits, however, when accounting for the thermal load limit of the generator. To avoid premature failure of the generator when an unbalanced load occurs, the characteristics that trigger unbalanced load protection should be adapted to the thermal characteristics of the generator. Unbalanced load protection can also be triggered by external errors in the mains caused by asymmetric short circuits.

When unbalanced load protection is tripped can be calculated using the following formula:

Operating mode	Formula
Short-term operation	$t = \frac{K1}{\frac{2}{(\frac{I_2}{I_{Nom}}) - 0.08^2}}$
Continuous operation	$\frac{I_2}{I_{Nom}} \leq 0.08 \rightarrow t = \infty$

Key	
t	Calculated tripping time
K1	Valid load time constant for the generator [s]
I_2	Calculated inverse current / unbalanced load current [A]
I_{Nom}	Nominal current for the generator [A]

To calculate the tripping time instant, the scan duration of the measurement system (i.e. 20 ms for 50 Hz voltage) is divided by the calculated trigger time, and the results are continually added up. With short-term operation, the value of the summands increases; with continuous operation, it decreases. If the summand reaches the value 1 (100%), then the max. permitted value has been reached. The summand is limited between 0 and 1.

Information:

The boundary between continuous operation and short-term operation is always 0.08 for calculations.

When the generator is at a standstill, the summand is neither reset nor is its value reduced.

Maximum limit of neutral conductor current

Name:
ConfigOutput36

Configurable limit for the neutral conductor current. If the value is exceeded, then the error message "Maximum neutral conductor current" is indicated (register "Error register") after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	0 to 1000	For 0 to 100% of I_{Nom}	0.1%

Response time for neutral conductor current monitor

Name:
ConfigOutput37

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

Short circuit current

Name:
ConfigOutput38

If the value of the generator current exceeds the percentage based on the converter's nominal current set here, then the error message "Short circuit current" is indicated (register "Error register") and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	1000 to 5000	For 100 to 500% of I_{Nom}	0.1%

Response time for short circuit current

Name:
ConfigOutput39

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

Data type	Value	Information	Resolution
UINT	4 to 30	For 0.04 to 0.3 s	0.01 s

Rating-dependent overcurrent

Name:
ConfigOutput42

The response value percentage is based on the nominal current of the generator. If the response value is exceeded, then the error message "Rating-dependent overcurrent" is indicated (register "Error register") and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
UINT	1000 to 2000	For 100 to 200% of I_{Nom}	0.1%

Rating-dependent overcurrent monitoring

A generator that is operated at its nominal current I_{Nom} normally reaches about half of its maximum thermal load. Operating it above the rated current I_{Nom} result in additional warming, which is permitted until the maximum temperature is reached. The highest permissible continuous temperature is determined by the class of the insulation material used in the generator.

Based on the settings and the current measurement, the device forms an internal model based on an I^2t characteristic curve of the generator temperature. This allows the heat capacity of the generator to be completely utilized for short overloads while at the same time providing full protection. The configurable parameters for determining the machine model include the nominal current I_{Nom} of the generator and the time multiplier.

Integration coefficient for rating-dependent overcurrent (iths)

Name:
ConfigOutput43

To calculate the tripping time instant, the sampling duration of the measurement system is divided by the calculated trigger time (t). The results are continually added up. If the summand reaches the value 1 (100%), then the max. permitted value has been reached. The summand is limited between 0 and 1.

Data type	Value	Information	Resolution
UINT	1 to 20	For 0.1 to 2	0.1

For a constant overcurrent, the trigger characteristic curve can be calculated based on the following formula:

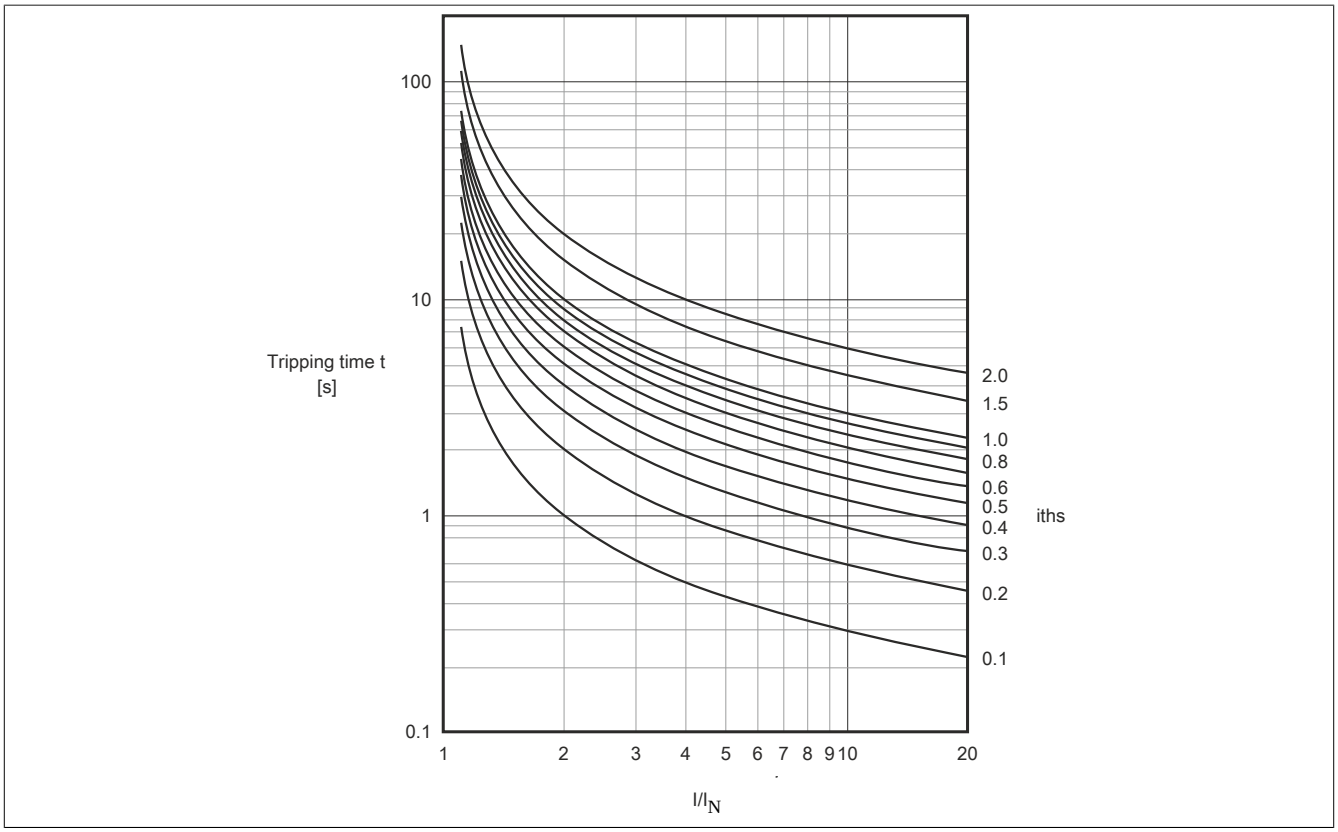
$$t = \frac{0.14}{(\frac{I}{I_N})^{0.02} - 1} * iths$$

Key:

t	Tripping time [s]
I	The highest value of the 3 phase currents [A]
I_N	Rating-dependent overcurrent [A] (0.5 to 2 * I_{Nom})
iths	Integration coefficient (0.1 to 2)

The monitor function can be reset by restarting the module or by falling below the overcurrent value so that the results of the continuous addition decrease according to the formula.

Trigger characteristic curve in accordance with IEC 255-4 (normal, inverse)



The monitor function can be reset by restarting the module or by falling below the overcurrent value so that the results of the continuous addition decrease according to the formula.

Capacitive reactive power

Name:
ConfigOutput44

The capacitive reactive power for the generator is monitored to determine if it falls below the defined response value. In this way, monitoring the capacitive reactive power can be used to detect exciter failure. If the response value is fallen below, then the error message "Capacitive reactive power" is indicated (register "Error register") after the delay time has passed and, if configured, the DO1 monitoring relay is switched.

Data type	Value	Information	Resolution
INT	-32768 to 32767	For -32768 to 32767 kvar	1 kvar

Response time for reactive power monitoring

Name:
ConfigOutput45

The error is only triggered if the response value is exceeded in the positive direction without interruption for as long as is specified in this register.

Data type	Value	Information	Resolution
UINT	5 to 100	For 0.5 to 10 s	0.1 s

DO1 function

Name:
ConfigOutput57

This digital output can be set after the defined response time has elapsed depending on the assignment of the generator mains' monitoring variables (X3).

The monitoring variables can be assigned to this input either individually or with additional monitoring variables using an OR connective. This makes it possible to set the relay when there are multiple monitoring variables.

The following monitoring functions can be assigned to the monitoring relay using this register:

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Overvoltage (of a phase)	0	Do not assign function
		1	Assign function
1	Undervoltage (or a phase)	0	Do not assign function
		1	Assign function
2	Overfrequency	0	Do not assign function
		1	Assign function
3	Underfrequency	0	Do not assign function
		1	Assign function
4	Voltage asymmetry	0	Do not assign function
		1	Assign function
5	Current asymmetry (unbalanced load)	0	Do not assign function
		1	Assign function
6	Neutral conductor current, maximum	0	Do not assign function
		1	Assign function
7	Short circuit current	0	Do not assign function
		1	Assign function
8	Rating-dependent overcurrent	0	Do not assign function
		1	Assign function
9	Capacitive reactive power (exciter failure)	0	Do not assign function
		1	Assign function
10	Ready	0	Do not assign function
		1	Assign function
11 - 15	Reserved	0	

Information:

The minimum pulse duration when addressing a monitoring function on the error bit via X2X as well as on the relay is 500 ms.

4.26.3.17.4.3 Busbar

Busbar nominal voltage (U_{NomBus})

Name:
ConfigOutput03

This is needed for converting the percentages based on this nominal value into physical units.

Data type	Value	Information	Resolution
UINT	70 to 65000	For 70 to 65000 V	1 V

Multiplier for busbar

Name:
ConfigOutput05

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

100 thus means a multiplier factor of 1 (measured value not changed).

Data type	Value	Information	Resolution
UINT	1 to 65535	For 0.01 to 655.35	0.01

Nominal voltage range of busbar

Name:
ConfigOutput21

Can be toggled between 100 and 400 V.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Voltage	0	100 V
		1	400 V
1 - 7	Reserved	-	

Minimum busbar voltage (U_{Bmin})

Name:
ConfigOutput40

Configurable threshold for zero voltage monitoring of the busbar based on its nominal voltage. DO3 is set if the value falls below the configured threshold.

Data type	Value	Information	Resolution
UINT	0 to 1000	For 0 to 100% of U_{NomBus}	0.1%

4.26.3.17.4.4 Synchronization

Synchronization mode

Name:
ConfigOutput
ConfigOutput17 to ConfigOutput19

If multiple mode bits are set at the same time, then no mode will be selected (type BOOL).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	ConfigOutput17	0	Sync mode ≠ Slip
		1	Sync mode = Slip
1	ConfigOutput18	0	Sync mode ≠ Check
		1	Sync mode = Check
2	ConfigOutput19	0	Sync mode ≠ Dead bus
		1	Sync Mode = Dead bus
3 - 7	Reserved	-	

Nominal voltage of synchronization mains (U_{NomSyn})

Name:
ConfigOutput01

This is needed for converting the percentages based on this nominal value into physical units.

Data type	Value	Information	Resolution
UINT	70 to 65000	For 70 to 65000 V	1 V

Multiplier for synchronization mains

Name:
ConfigOutput07 (mains 1)
ConfigOutput08 (mains 2)

This is used for converting the measured value into a physical value. The multiplier is applied to the respective input value.

100 means a multiplier factor of 1 (measured value not changed).

Data type	Value	Information	Resolution
UINT	1 to 65535	For 0.01 to 655.35	0.01

Max. differential frequency (df_{max})

Name:
ConfigOutput11

A switch-on command on DO4 is only output if this configured differential frequency is not exceeded. This value specifies the upper frequency (positive value corresponds to positive slip → generator frequency is greater than the busbar frequency when synchronizing).

Data type	Value	Information	Resolution
UINT	2 to 49	For 0.02 to 0.49 Hz	0.01 Hz

Min. differential frequency (df_{min})

Name:
ConfigOutput12

A switch-on command on DO4 is only output if this configured differential frequency is not exceeded in the negative direction. This value specifies the lower frequency (negative value corresponds to negative slip → generator frequency is less than the busbar frequency when synchronizing).

Data type	Value	Information	Resolution
INT	-49 to 0	For -0.49 to 0 Hz	0.01 Hz

Max. differential voltage (dU_{max})

Name:
ConfigOutput13

A switch-on command on DO4 is only output if this configured differential voltage percentage based on the synchronization mains' nominal voltage is not exceeded.

Data type	Value	Information	Resolution
UINT	1 to 300	For 0.1 to 30% of U_{NomSyn}	0.1%

Max. permitted differential angle (ϕ_{Max})

Name:
ConfigOutput14

A switch-on command on DO4 is only output if the configured differential angle between the two synchronization mains is not exceeded.

Data type	Value	Information	Resolution
UINT	1 to 600	For 0.1 to 60°	0.1°

Phase rotation of sync mains 1 (dα)

Name:
ConfigOutput15

This parameter is used for correcting any phase shifting from upstream transformer vector groups before reaching the mains being synchronized.

This parameter specifies how many degrees the synchronization mains lags behind the mains being synchronized.

Data type	Value	Information	Resolution
UINT	0 to 3600	For 0 to 360°	0.1°

Nominal voltage range of synchronization mains

Name:
ConfigOutput22 (mains 1)
ConfigOutput23 (mains 2)

Can be toggled between 100 and 400 V.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Voltage	0	100 V
		1	400 V
1 - 7	Reserved	-	

Pulse duration of the turn-on delay

Name:
ConfigOutput47

The duration of the switch-on pulse can be adjusted for the following switching units. The time set here is valid for the switch-on pulse for DO4.

Data type	Value	Information	Resolution
UINT	40 to 500	For 0.04 to 0.5 s	0.001 s

Switching response time of the power switch

Name:
ConfigOutput48

The actuation time of the generator power switch corresponds to the lead time of the switch-on command. The switch-on command is executed before the point of synchronization according to the amount of time defined here.

Data type	Value	Information	Resolution
UINT	40 to 300	For 0.04 to 0.3 s	0.001 s

Synchronization configuration

Name:
ConfigOutput56

Parameter for configuring which mains or voltages should be synchronized with each other.

This configuration makes it possible to synchronize the AC mains on terminal X4 either with terminal X3, X5 or X6. In each case, synchronization mains 1 (X4) is the network to which synchronization takes place.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Synchronization	00	X4 - X6: Synchronization mains 1 - Synchronization mains 2
		01	X4 - X5: Synchronization mains 1 - Busbar
		10	X4 - X3: Synchronization mains 1 - Generator
		11	Reserved
2 - 15	Reserved	-	

Dead bus voltage

Name:
ConfigOutput58

Configurable threshold for dead bus synchronization based on the nominal voltage of the busbar.

Data type	Value	Information	Resolution
UINT	0 to 1000	For 0 to 100% of U_{NomBus}	0.1%

4.26.3.17.4.5 Maximum value buffer and power meter

Pulse value of energy meter output

Name:
ConfigOutput46

Output DO2 outputs pulses that occur at a frequency proportional to the measured energy. The frequency of the pulses can be specified. The length of the pulse is 400 ms. The frequency at which the pulses occur should be set so that the duration between two pulses does not exceed 400 ms at the highest possible power. The pulse output's internal meter starts at 0 kWh after a restart. This register has no effect on the "ConfigOutput54" and "ConfigOutput55" registers.

Data type	Value	Information	Resolution
UINT	0 to 65535	For 0 to 65535 kWh/pulse	1 kWh/pulse

Maximum value buffer and meter buffer

These registers are used for nonvolatile storage of the maximum value and meter level values. After restarting, the stored maximum values and meter states are loaded back into their registers and the module's internal work meter is reset. It is possible to reset or write to the stored maximum values and meter states using an acyclic register.

The maximum values are recorded by the effective measured values before reaching the configurable filter. The maximum values can be read or written to as acyclic registers.

Maximum phase current

Name:
Reading: ConfigOutput49 (generator I1)
Reading: ConfigOutput50 (generator I2)
Reading: ConfigOutput51 (generator I3)
Reset: ConfigOutput60 (generator I1)
Reset: ConfigOutput61 (generator I2)
Reset: ConfigOutput62 (generator I3)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Maximum total active power

Name:
Reading: ConfigOutput52
Reset: ConfigOutput63

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 kW

Maximum neutral conductor current

Name:
Reading: ConfigOutput53
Reset: ConfigOutput64

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Active energy counter

Name:
Reading: ConfigOutput54
Writing: ConfigOutput66

Data type	Value	Information	Resolution
DINT	-2,147,483,648 to 2,147,483,647	-	100 kWh

Reactive energy counter

Name:
Reading: ConfigOutput55
Writing: ConfigOutput67

Data type	Value	Information	Resolution
DINT	-2,147,483,648 to 2,147,483,647	-	100 kvarh

4.26.3.17.5 Communication registers

4.26.3.17.5.1 General registers

Digital outputs

Name:
DigitalOutput
DigitalOutput05
DigitalOutput06

(data point applied as BOOL)

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput05	0	Reset output 5
		1	Set output 5
1	DigitalOutput06	0	Reset output 6
		1	Set output 6

Status of digital outputs

Name:
StatusDigitalOutput01 to StatusDigitalOutput06
StatusInput16 to StatusInput17

(data point applied as BOOL)

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusDigitalOutput01	0	Current state of output 1 = LOW
		1	Current state of output 1 = HIGH
1 - 7	Reserved	-	
8	StatusDigitalOutput02	0	Current state of output 2 = LOW
		1	Current state of output 2 = HIGH
...		...	
12	StatusDigitalOutput06	0	Current state of output 6 = LOW
		1	Current state of output 6 = HIGH
13	Reserved	-	
14	StatusInput17	0	Status DO OK
		1	Status DO overload
15	StatusInput16	0	Status 24 V output supply OK
		1	Status 24 V output supply undervoltage

Error registers

Name:
StatusInput18
StatusInput01 to StatusInput15

This register contains status inputs (type BOOL).

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusInput01	0	Overvoltage (one phase), OK
		1	Overvoltage (one phase), present
1	StatusInput02	0	Undervoltage (one phase), OK
		1	Undervoltage (one phase), present
2	StatusInput03	0	Over-frequency, OK
		1	Over-frequency, present
3	StatusInput04	0	Under-frequency, OK
		1	Under-frequency, present
4	StatusInput05	0	Voltage asymmetry, OK
		1	Voltage asymmetry, present
5	StatusInput06	0	Current asymmetry, OK
		1	Current asymmetry, present
6	StatusInput07	0	Maximum neutral conductor current, OK
		1	Maximum neutral conductor current exceeded
7	StatusInput08	0	Short circuit-current, OK
		1	Short circuit-current, present
8	StatusInput09	0	Rating-dependent overcurrent OK
		1	Rating-dependent overcurrent occurring
9	StatusInput10	0	Capacitive reactive power (exciter failure), OK
		1	Capacitive reactive power (exciter failure), present
10	StatusInput11	0	Ready, OK
		1	Not ready
11	StatusInput12	0	Generator mains phase 1 OK
		1	Failure of generator mains phase 1
12	StatusInput13	0	Busbar phase 1 OK
		1	Busbar phase 1 failure
13	StatusInput14	0	Phase 1 sync mains 1 OK
		1	Phase 1 sync mains 1 failure
15	StatusInput15	0	Phase 1 sync mains 2 OK
		1	Phase 1 sync mains 2 failure
15	Reserved	-	

StatusInput11

The error message "Not ready" is triggered if the X20 I/O supply drops below 18 VDC.

StatusInput

(StatusInput12 to StatusInput 14)

Phase failure is detected if phase 1 of the respective terminal fails.

If this error occurs, it will mean losses in measurement precision.

4.26.3.17.5.2 Generator mains measured values

Phase currents of the generator

Name:
AnalogInput01 (I1)
AnalogInput02 (I2)
AnalogInput03 (I3)

Phase currents of the generator

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Current average of generator I1, I2, I3

Name:
AnalogInput04

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Neutral conductor current of generator I_n

Name:
AnalogInput05

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 A

Dynamic current average of generator (I_{m_dyn})

Name:
AnalogInput06

Describes the change to the current average.

The dynamic average is the amount of change (I_{m_diff}) of the current average (sampling time: 10 ms).

This value decays in an e-function.

$I_{m\_diff} > I_{m\_dyn} \rightarrow I_{m\_dyn} = I_{m\_diff}$

$I_{m\_diff} \leq I_{m\_dyn} \rightarrow I_{m\_dyn} = I_{m\_dyn} * 0.98$

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	1 A

Line-to-line voltages of the generator

Name:
AnalogInput07 (UG12)
AnalogInput08 (UG23)
AnalogInput09 (UG31)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Phase voltages of the generator

Name:
AnalogInput10 (UG 1)
AnalogInput11 (UG 2)
AnalogInput12 (UG 3)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Generator power: Total active power P

Name:
AnalogInput19

Filtered generator power values:

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 kW

Generator power: Total reactive power Q

Name:
AnalogInput20

Filtered generator power values:

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 kvar

Generator power: Total apparent power S

Name:
AnalogInput21

Filtered generator power values:

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 kVA

Voltage average of the generator

Name:
AnalogInput22

Voltage average of the generator UG12, UG23, UG31 (U~3 average)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Power factor of generator/cos ϕ

Name:
AnalogInput23

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	0.001

Frequency of the generator mains

Name:
AnalogInput24

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	0.01 Hz

4.26.3.17.5.3 Busbar measured values

Line-to-line voltages of the busbar

Name:
AnalogInput13 (UB12)
AnalogInput14 (UB23)
AnalogInput15 (UB31)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Phase voltages of the busbar

Name:
AnalogInput16 (UB1)
AnalogInput17 (UB2)
AnalogInput18 (UB3)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

4.26.3.17.5.4 Synchronization mains measured values

Line-to-line voltages

Name:
AnalogInput25 (sync mains 1 US1)
AnalogInput26 (sync mains 2 US2)

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

Frequencies

Name:
AnalogInput27 (sync mains 1)
AnalogInput28 (sync mains 2)

Data type	Value	Information	Resolution
UINT	0 to 65,535	-	0.01 Hz

Differential angle between synchronization mains

Name:
AnalogInput29

Angular difference between the mains being synchronized

Specifies how many degrees the sync mains are ahead of the mains being synchronized.

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	0.1°

Differential voltage between synchronization mains

Name:
AnalogInput30

Voltage difference between the mains being synchronized

Data type	Value	Information	Resolution
INT	-32768 to 32767	-	1 V

4.26.3.17.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
≥ 250 µs

4.26.3.17.7 Minimum I/O update time

The minimum I/O update time for the analog inputs depends on the respective period duration of the measurement signal frequency.

Minimum I/O update time	
At 50 Hz	20 ms

4.26.4 X20CM4810

4.26.4.1 Order data

Model number	Short description	Figure
	Other functions	
X20CM4810	X20 analog input module for vibration measurement and analyse of condition monitoring exercises. 4 IEPE analog input 51,5625 kHz sampling frequency 24 bit converter resolution	
	Required accessories	
	Bus modules	
X20BM31	X20 bus module for double-width modules, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	
	Optional accessories	
	Cables	
0ACC0020.01-1	Cable for acceleration sensor, length 2 m, 2x 0.34 mm², M12 socket on sensor side, can be used in cable drag chains, UL listed	
0ACC0050.01-1	Cable for acceleration sensor, length 5 m, 2x 0.34 mm², M12 socket on sensor side, can be used in cable drag chains, UL listed	
0ACC0100.01-1	Cable for acceleration sensor, length 10 m, 2x 0.34 mm², M12 socket on sensor side, can be used in cable drag chains, UL listed	
0ACC0150.01-1	Cable for acceleration sensor, length 15 m 2x 0.34 mm², Female M12 connector on sensor side, cable, UL listed	
0ACC0200.01-1	Cable for acceleration sensor, length 20 m, 2x 0.34 mm², M12 socket on sensor side, can be used in cable drag chains, UL listed	
	Sensors	
0ACS100A.00-1	Acceleration sensor, nominal sensitivity 100 mV/g, top exit	
0ACS100A.90-1	Acceleration sensor, nominal sensitivity 100 mV/g, side exit	

Table 585: X20CM4810 - Order data

4.26.4.2 Technical data

Information:

The X20CM4810 module is only supported by Automation Studio 3.0.90.x and Automation Runtime versions >= J3.09, J4.01 and O4.02.

4.26.4.2.1 Technical data

Product ID	X20CM4810
Short description	
I/O module	X20 4-channel analog input module for vibration measurement and analysis of condition monitoring tasks
General information	
Isolation voltage between channel and bus	500 V_{eff}
Nominal voltage	24 VDC ±20%
B&R ID code	0xC8F9
Status indicators	Run, error, vibration inputs 1 to 4
Diagnostics	
Module run/error	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	2.5 W
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
GOST-R	Yes
Analog inputs	
Quantity	4
Input type	IEPE sensor: Acceleration
Digital converter resolution	24-bit

Table 586: X20CM4810 - Technical data

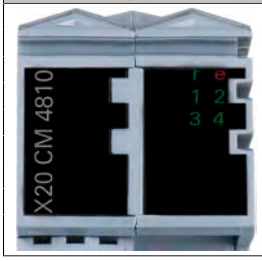
Product ID	X20CM4810
Open line detection	
Per channel	Yes
At minimum supply voltage [1]	17 V (or higher) for more than 1 ms
At nominal supply voltage [2]	21.3 V (or higher) for more than 1 ms
At maximum supply voltage [3]	25.5 V (or higher) for more than 1 ms
Permitted input signal	±10 VAC
Conversion procedure	Sigma Delta
Type	Vibration input
Sampling frequency	51.5625 kHz
Input high pass cutoff frequency	34 mHz
Input low pass cutoff frequency	19.75 kHz
Downsampling	200 Hz, 500 Hz, 1 kHz, 2 kHz, 5 kHz, 10 kHz (configurable)
Frequency resolution of the spectrums	0.0629 Hz, 0.1574 Hz, 0.3147 Hz, 0.6294 Hz, 1.5736 Hz, 3.1471 Hz
Sensor supply	IEPE, 5 mA constant current source (4.9 - 5.5 mA), can be switched off for each channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at altitudes above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 50°C
Vertical installation	-25 to 45°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM31 bus module separately
Spacing	25 $^{+0.2}$ mm

Table 586: X20CM4810 - Technical data

1) Input voltage: 19.2 V
2) Input voltage: 24 V
3) Input voltage: 28.8 V

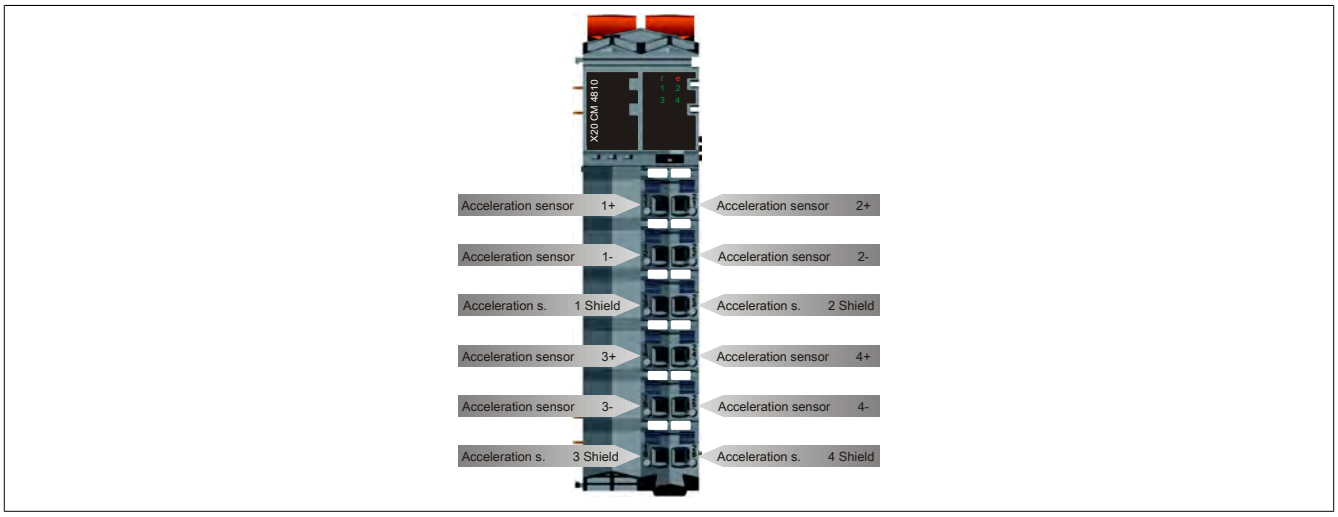
4.26.4.2.2 Status LEDs

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	Reset mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	Module supply not connected or everything OK
			On	Warning, error or reset status
	e + r	Red on and green single flash		Invalid firmware
	1 - 4	Green	On	Status of the respective acceleration sensor (no open circuit)

1) Depending on the configuration, a firmware update can take up to several minutes.

4.26.4.2.3 Pinout



4.26.4.2.4 Shielding

There are two ways to shield the cable for the acceleration sensors:

- Shielding possibilities on the terminal block. (Contact "Acceleration sensor 1 - 4 shield")
- X20 shielding on the bus module. (See the "Shielding" chapter in the X20 system user's manual)

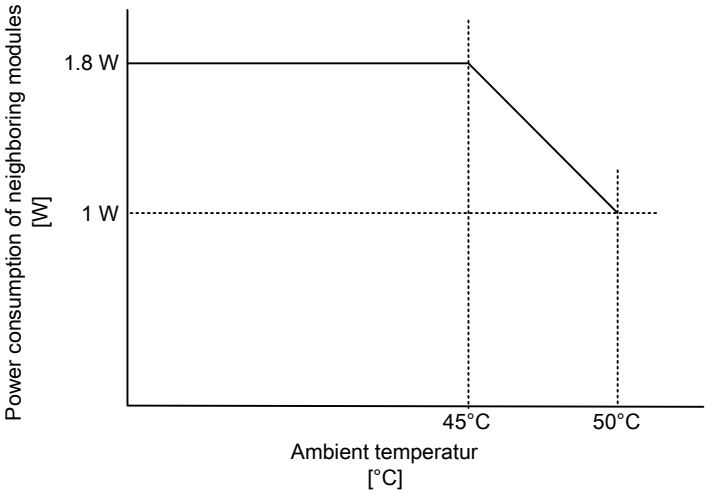
Shielding via the terminal block is perfectly sufficient for environments with no special EMC requirements.

However, if the X20CM4810 is used in an environment with special EMC requirements and high frequency disturbances, both options should be used together.

4.26.4.2.5 Derating

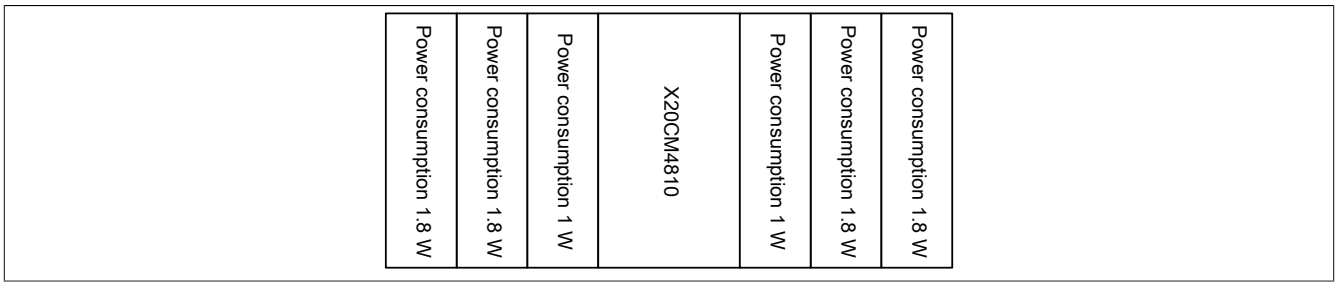
Horizontal installation

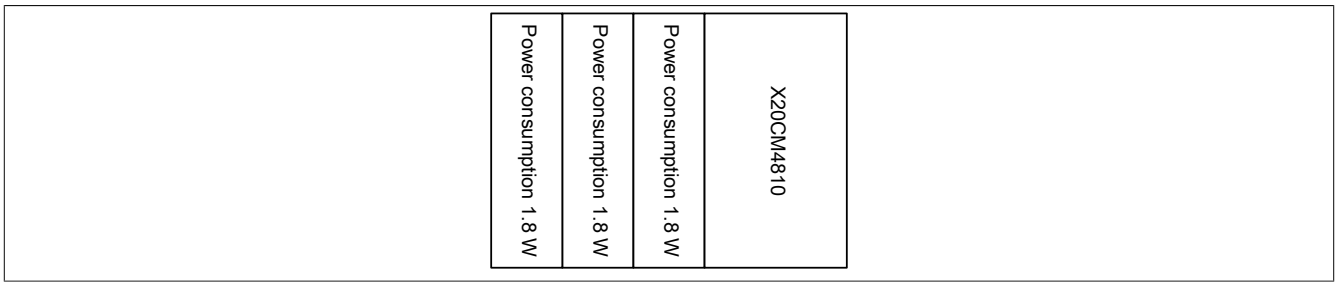
At ambient temperatures higher than 45°C, the X20CM4810 requires power derating:

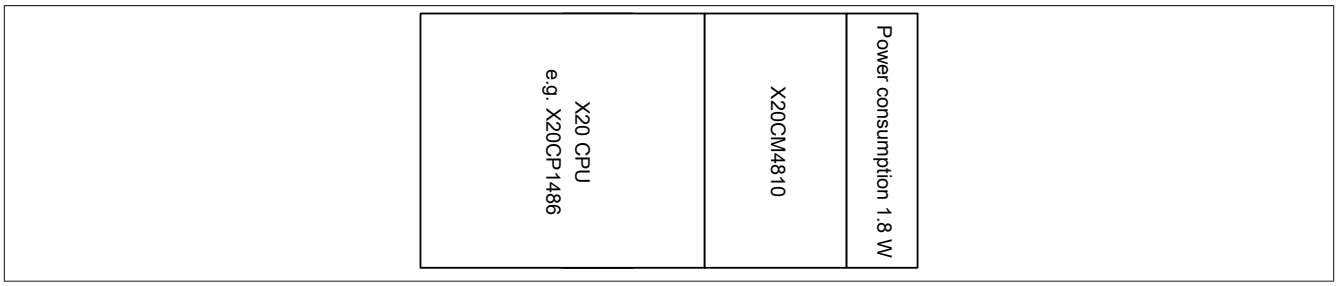


If the X20CM4810 is to be operated with ambient temperatures up to 50°C, then the neighboring modules must not consume more than 1 W.

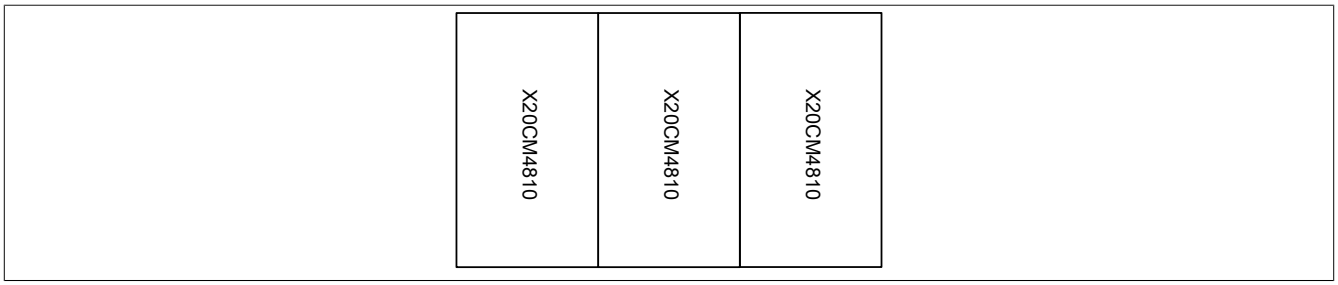
Example: ambient temperature up to 50°C



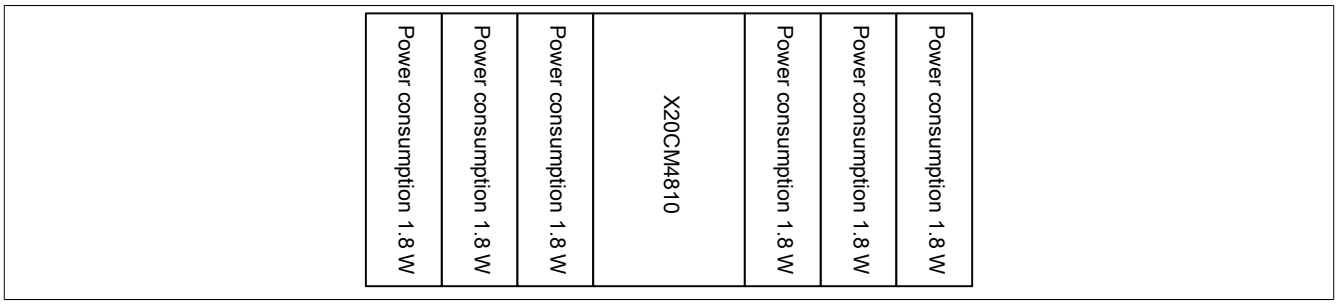




X20 double-width modules are an exception. It is also possible, for example, to place multiple X20CM4810 modules next to one another.

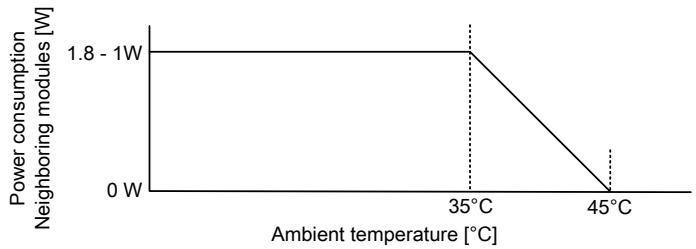


Example: ambient temperature up to 45°C



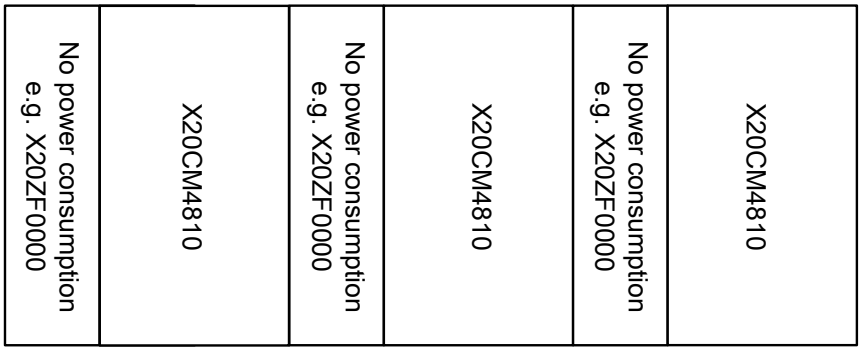
Vertical installation

At ambient temperatures higher than 35°C, the X20CM4810 requires power derating:

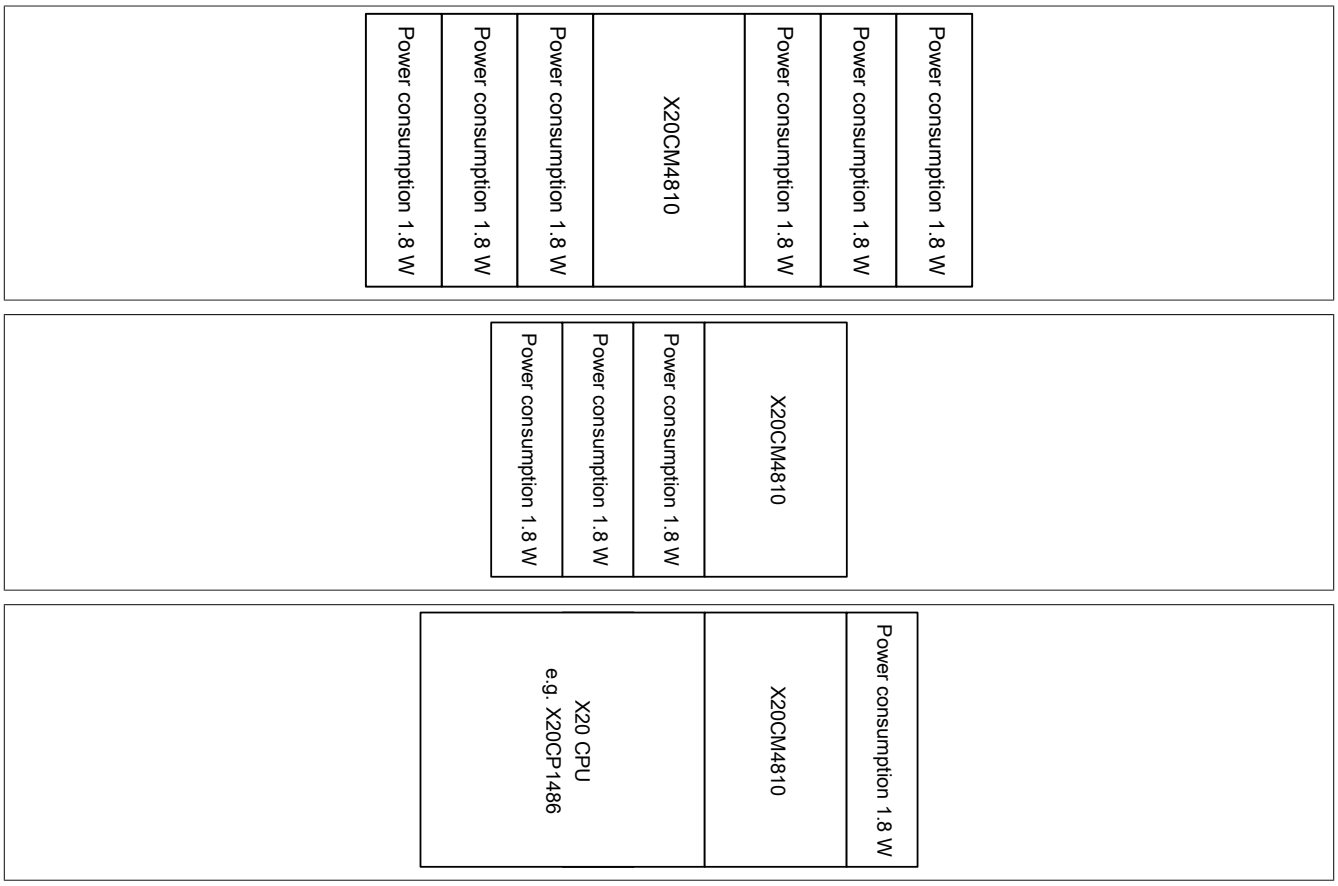


If the X20CM4810 is to be operated with ambient temperatures up to 45°C, then the neighboring modules must not consume power.

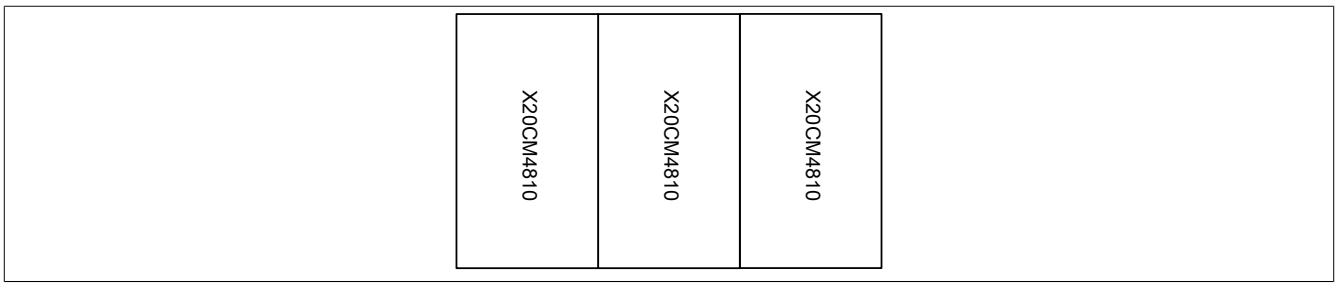
Example: ambient temperature up to 45°C



Example: ambient temperature up to 35°C



X20 double-width modules are an exception. For example, multiple neighboring X20CM4810 modules can be operated up to an ambient temperature of 30°C.



4.26.4.2.6 Gain curve

The following diagram shows a typical gain curve for the X20CM4810 module.

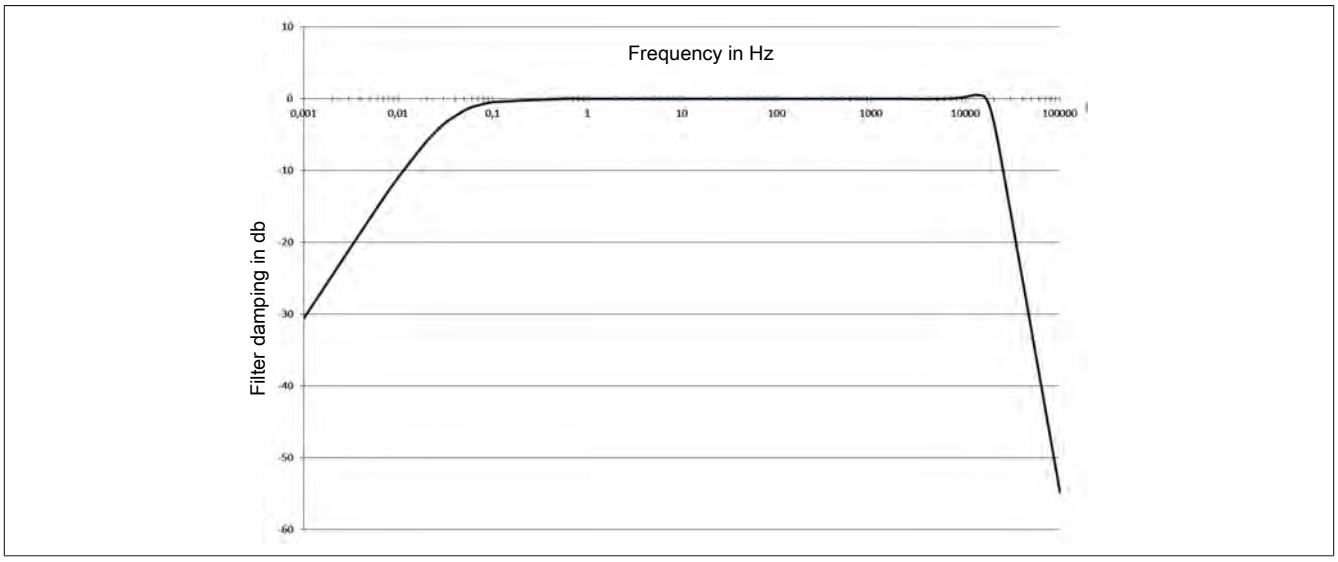


Figure 400: Typical gain curve

4.26.4.2.7 Signal generation

The following signals and characteristic values are calculated from the acceleration sensor's input signal:

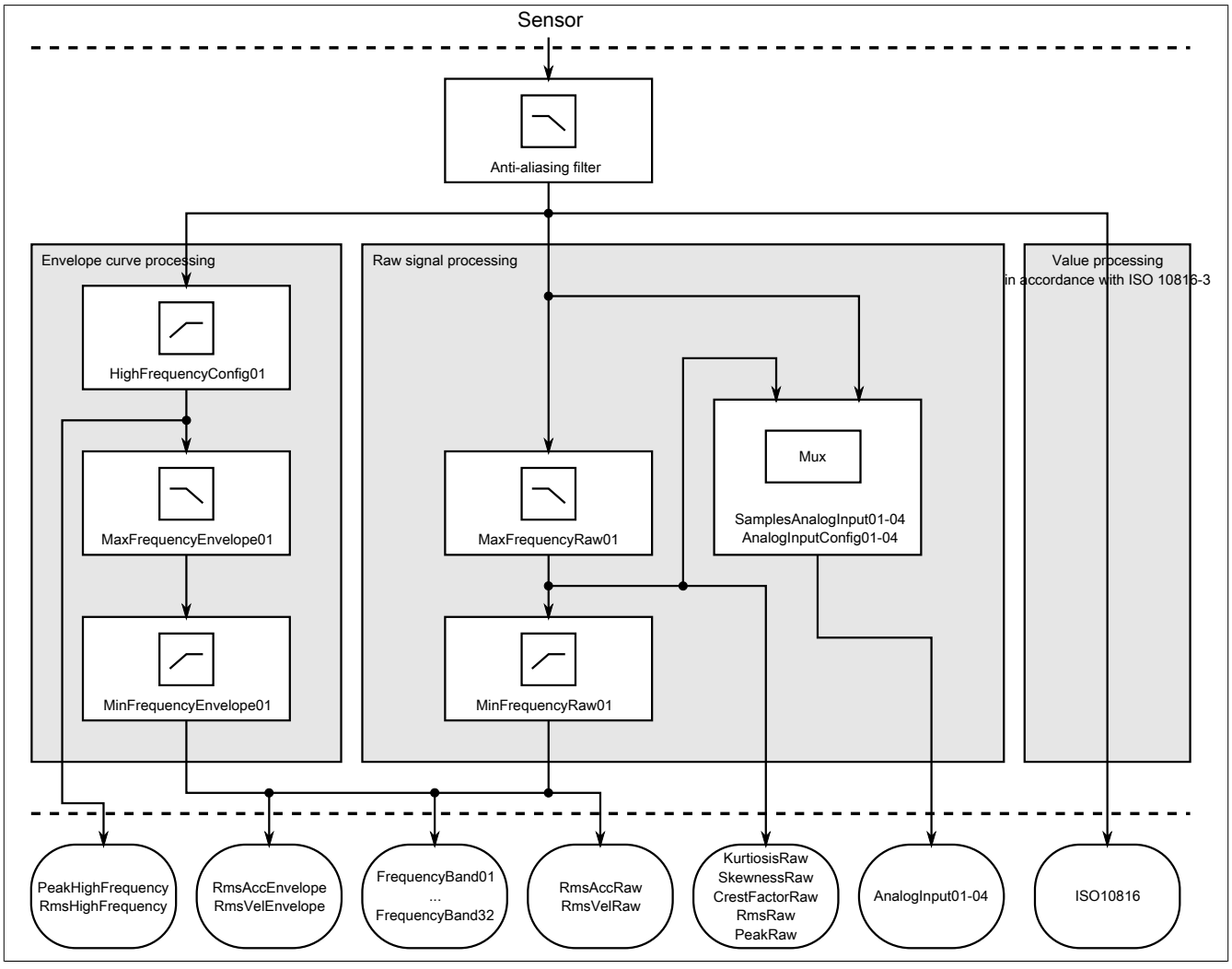


Figure 401: Signal generation in the module

4.26.4.2.8 Filter configuration

The X20CM4810 has a number of configurable filters.

There is an adjustable high-pass filter for the whole module that can be configured using "HighFrequencyConfig01". Possible settings are 500 Hz, 1 kHz and 2 kHz. This high-pass affects all high-frequency and envelope characteristic values of all module channels.

In addition, there are two adjustable low pass filters per channel.

- For the raw signal. This filter is configured using "MaxFrequencyRaw01". Possible settings are 200 Hz, 500 Hz, 1 kHz, 2 kHz, 5 kHz and 10 kHz.
- For the envelope signal. This filter is configured using "MaxFrequencyEnvelope01". Possible settings are 200 Hz, 500 Hz, 1 kHz and 2 kHz.

These low-pass filters affect all calculated characteristic values of the respective signal, i.e. the raw or envelope signal. They can be used to increase the frequency resolution of the FFT. When calculating characteristic values in AnalogInput, however, it is possible to select whether the characteristic values should be calculated directly from the input signal or from the low-pass filtered raw signal.

4.26.4.2.9 Frequency bands

It is possible to individually configure up to 32 frequency bands where the effective value (RMS) or the noise of a quadrant is calculated.

Configuration:

Parameter	Settings		
Enable	Off | RMS | Noise		
Channel	1 | 2 | 3 | 4		
Source	Raw acceleration signal | Raw velocity signal | Enveloped acceleration signal | Enveloped velocity signal		
Calculation of harmonics (RMS only)	Yes | No		
Rotation-dependent (RMS only)	On	Selects the data point for velocity ("ActSpeed01-04")	[1/100 Hz]
		Standardized damage frequency at 60 rpm	[1/100]
		± Width of the frequency band (tolerance band)	[1/100 Hz]
	Off	Lower frequency	[1/4 Hz]
		Upper frequency	[1/4 Hz]
Quadrant (noise only)	1 Quadrant | 2nd Quadrant | 3rd Quadrant | 4th Quadrant		

4.26.4.2.10 Characteristic values

The following condition parameters can be read from the X20CM4810 module for each channel:

Characteristic values	Description
"PeakHighFrequency"	Absolute maximum of the high-frequency portions of the input signal. The high-pass filter can be configured with the "HighFrequencyConfig01" register.
"CrestFactorHighFrequency"[1]	Ratio of the maximum amount to the RMS value ("Crest factor") of the high-frequency portions ("PeakHighFrequency" and "RmsHighFrequency") of the input signal
"Vdi3832KtHighFrequency"[1]	Ratio between the reference values and the currently measured values of the high-frequency portions of the input signal in accordance with the VDI 3832 guideline
"PeakRaw"	Peak value (absolute) of the input signal up to the maximum frequency ("MaxFrequencyRaw01") of the channel
"CrestFactorRaw"	Crest factor (peak-to-average power ratio) of the input signal up to the maximum frequency ("MaxFrequencyRaw01") of the channel
"SkewnessRaw"	Skewness (third statistical moment) of the input signal up to the maximum frequency ("MaxFrequencyRaw01")
"KurtosisRaw"	Peakedness, fourth statistical moment (kurtosis) of the input signal up to the maximum frequency ("MaxFrequencyRaw01") of the channel
"Vdi3832KtRaw"[1]	Ratio between the reference values and the currently measured values of the input signal in accordance with the VDI 3832 guideline
"RmsHighFrequency"	RMS value of the high-frequency portions of the input signal. The high-pass filter can be configured with the "HighFrequencyConfig01" register.
"RmsRaw"	RMS value of the input signal up to the maximum frequency ("MaxFrequencyRaw01") of the channel
"RmsAccRaw"	RMS value of the acceleration of the input signal from the configured minimum frequency ("MinFrequencyRaw01") up to the configured maximum frequency ("MaxFrequencyRaw01") of the channel
"RmsVelRaw"	RMS value of the speed of the input signal from the configured minimum frequency ("MinFrequencyRaw01") up to the configured maximum frequency ("MaxFrequencyRaw01") of the channel[2]
"ISO10816"	Effective value of the velocity in the frequency domain 10 Hz to 1 kHz in accordance with ISO 10816
"RmsAccEnvelope"	RMS value of the acceleration of the envelope from the configured minimum frequency ("MinFrequencyEnvelope01") up to the configured maximum frequency ("MaxFrequencyEnvelope01") of the channel
"RmsVelEnvelope"	RMS value of the speed of the envelope from the configured minimum frequency ("MinFrequencyEnvelope01") up to the configured maximum frequency ("MaxFrequencyEnvelope01") of the channel[2]

Table 587: Characteristic values

1) Only available in Function model 0 - Standard
2) Only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

4.26.4.2.11 Characteristic value format

Characteristic value	Format	Unit
"ActSpeed01-04"	REAL	Hz
"AnalogInput01-04"	REAL	mg or 1 when crest
"PeakHighFrequency01-04"	REAL	mg
"RmsHighFrequency01-04"	REAL	mg
CrestFactorHighFrequency01-04[1)]	REAL	1
Vdi3832KtHighFrequency01-04[1)]	REAL	1
"RmsAccEnvelope01-04"	REAL	mg
"RmsVelEnvelope01-04"	REAL	mm/s
"RmsAccRaw01-04"	REAL	mg
"RmsVelRaw01-04"	REAL	mm/s
"PeakRaw01-04"	REAL	mg
"RmsRaw01-04"	REAL	mg
"CrestFactorRaw01-04"	REAL	1
"SkewnessRaw01-04"	REAL	1
"KurtosisRaw01-04"	REAL	1
Vdi3832KtRaw01-04[1)]	REAL	1
"Iso10816_01-04"	REAL	mm/s
"FrequencyBand01-32"	REAL	mg or mm/s depending on the configuration

Table 588: Characteristic values after preparation by Automation Runtime in the standard function model

1) Additional characteristic value provided by Automation Runtime.

Characteristic value	Format	Resolution and unit	Value on overflow
"ActSpeed01-04"	UINT	0.01 Hz	
"AnalogInput01-04"	INT	AnalogInputScale/32768	32767 or -32768 (cap)
"PeakHighFrequency01-04"	24-bit unsigned	1/65536 g	16777215
"RmsHighFrequency01-04"	24-bit unsigned	1/65536 g	16777215
"RmsAccEnvelope01-04"	24-bit unsigned	0.001 g	16777215
"RmsVelEnvelope01-04"	24-bit unsigned	0.001 mm/s	16777215
"RmsAccRaw01-04"	24-bit unsigned	0.001 g	16777215
"RmsVelRaw01-04"	24-bit unsigned	0.001 mm/s	16777215
"PeakRaw01-04"	24-bit unsigned	1/65536 g	16777215
"RmsRaw01-04"	24-bit unsigned	1/65536 g	16777215
"CrestFactorRaw01-04"	24-bit unsigned	0.001	16777215
"SkewnessRaw01-04"	24-bit signed	0.001	8388607
"KurtosisRaw01-04"	24-bit signed	0.001	8388607
"Iso10816_01-04"	24-bit unsigned	0.001 mm/s	16777215
"FrequencyBand01-32" (configured as RMS)	24-bit unsigned	0.001 g or 0.001 mm/s depending on the configuration	16777215
"FrequencyBand01-32" (configured as noise)	24-bit unsigned	1/65536 g or 1/65536 mm/s depending on the configuration	16777215

Table 589: X20CM4810 characteristic values

4.26.4.3 General information about the module

4.26.4.3.1 X20CM4810 settling time

The input high-pass cut-off frequency of the AC voltage input (limit frequency of 34 MHz) means that a certain amount of settling time is required after changing the DC offset of the pending signal.

- Settling time of approximately 30 seconds at 100 mV/g sensor sensitivity and a 24 V supply voltage with an accuracy of 0.4 g
- Settling time of approximately 60 seconds at 100 mV/g sensor sensitivity and a 24 V supply voltage with an accuracy of 0.001 g
- The respective settling time must be allowed to pass in order to achieve accurate measurement results when an open line occurs. Because of this, all characteristic values and analog input values are set to 0 by the module during the first 30 seconds after a restart or wire breakage.

4.26.4.3.2 Sensor sensitivity

The X20CM4810 always assumes a 100 mV/g acceleration sensor on the input. When using Function model 0 - Standard, it is possible to configure a different sensor sensitivity directly in the function library.

If a different function model is used, for example an SGC controller or bus coupler, any conversion to a different sensitivity must be performed manually.

Example

Factor = 100 / (sensor sensitivity in mV/g)

All characteristic values and values must be multiplied by the calculated factor. This also applies to the analog characteristic values if the characteristic value calculation is enabled as well as for uploaded time signals and amplitude spectra. Exempt from this are all characteristic values without any units, such as "KurtosisRaw", "CrestFactorRaw" and "SkewnessRaw". See section 4.26.4.2.11 "Characteristic value format" on page 2602.

4.26.4.3.3 Information about FlatStream

When using FlatStream in Function model 0 - Standard and Function model 1 - Fast master, the following must be noted. The X20CM4810 changes the values in the FlatStream in every X2X Link cycle. To avoid missing anything in the task, it is important to select a task cycle that is either the same speed and synchronous to the module's bus or faster. This also applies to fieldbus connections between the CPU and bus coupler.

The maximum bus cycle time of 10 ms must not be exceeded since it is not possible to guarantee that the data calculated by the module every 300 ms will be fully transferred on the bus.

4.26.4.3.4 Information about using a SG4 CPU

The X20CM4810 calculates all characteristic values up to "Vdi3832KtRaw", "Vdi3832KtHighFrequency" and "CrestFactorHighFrequency" independently every 300 ms. Automation Runtime facilitates the handling of the module for the user (characteristic value upload), scales the characteristic values to the sensor resolution and also calculates the characteristic values specified above.

4.26.4.3.5 Calculating the velocity signal automatically

The X20CM4810 module can calculate the velocity signal from the signal provided by the acceleration sensor. This calculation is disabled by default since it can reduce the accuracy of the acceleration signal.

Reason

When converting from acceleration to velocity, low frequency portions become very large. As a result, the autogain is decreased by a few levels, which then further degrades accuracy.

If this calculation is not enabled, 0 is output for all characteristic values calculated on the velocity spectrum. The characteristic value "ISO10816" is not affected by this.

4.26.4.3.6 Information about AutogainDelay and overflow

The X20CM4810 automatically adjusts the measurement signal dynamically (autogain) to ensure that it is measured with the highest possible accuracy. This adjustment is made in multiple steps. Each step amplifies the input signal more than the last. If the signal was very small for a long time and a impact suddenly occurs, an overflow may occur with some calculated characteristic values. This is indicated by the overflow bit for the respective channel (Overflow01-04) being set and the affected module characteristic values being set to their maximum. See section 4.26.4.2.11 "Characteristic value format" on page 2602.

With Function model 0 - Standard, there are also the additional data points "OverflowCharacteristicValues01-04" and "OverflowFrequencyBands01". These are automatically generated by Automation Runtime and directly indicate the overflow status of the individual characteristic values and frequency bands.

If an overflow occurs or if an internal threshold is exceeded, the autogain for the next measurement is reduced by one level. If no overflow occurs for a certain number of measurements (adjustable by "AutogainDelay01"), or the signal stays below the internal threshold, the autogain is increased by one level again.

If overflows are occurring frequently, increasing AutogainDelay may help.

4.26.4.3.7 Important information when using a B&R Compact CPU or fieldbus CPU

Due to the size of the firmware for the X20CM4810 module, only CPUs with sufficient ROM (> 1MB) are supported. (X20CP0292 or X20XC0292)

4.26.4.3.8 Firmware update time

Updates to the firmware can take some time due to the size of the files.

The following firmware update times can be expected depending on the configured bus cycle time:

Bus cycle time	Update time
400 µs	Approx. 3 min
2 ms	Approx. 15 min

Table 590: Firmware update time

4.26.4.4 Condition monitoring / Oscillation analyses

4.26.4.4.1 General information

System availability is one of the most important criteria in machine operation. For this reason, increasing and ensuring this availability over the long term is a primary objective of the system operator.

Unplanned stoppages and the resulting loss of production can lead to substantial costs. The implementation of condition monitoring has proven to be a very good method for supporting anticipatory maintenance.

4.26.4.4.1.1 What is condition monitoring?

Condition monitoring involves recording the status of the machines at regular intervals by measuring important values in order to recognize impending problems in the system. The goal is to recognize imminent damage early enough so that a faulty machine part can be repaired or replaced before it leads to consequential damage or a partial or complete breakdown of the system.

The specific purpose of condition monitoring is to collect and process sensor data (e.g. oscillations, temperatures, lubricant conditions, pressures, flows) that can be used to assess the overall condition of the system.

Deviations from normal process or system conditions are caused by defects, which can occur for a variety of reasons. If corresponding countermeasures are not taken, this can quickly lead to a malfunction and breakdown of the system. Monitoring the sources of defects through the analysis of machine parameters can make it possible to recognize malfunctions as early as possible in order to take preventive action. Possible responses can include, for example, an error message or warning to the operator or an automated action for fault clearance and prevention of damage all the way up to automatic shutdown.

The integration and systematic implementation of condition monitoring provides many advantages:

- System components are only repaired or replaced when actually necessary. Potential defects are recognized early on in operation.
- Reliability can be significantly increased by integrating condition monitoring into the process.

Bathtub / Deterioration curve

The operating performance of every mechanical component changes over the course of operation, with each component becoming defective at some point. It is crucial to recognize such a change before the component can no longer fulfill its function. This behavior can be demonstrated using a "bathtub curve", which indicates the probable failure rate over time.

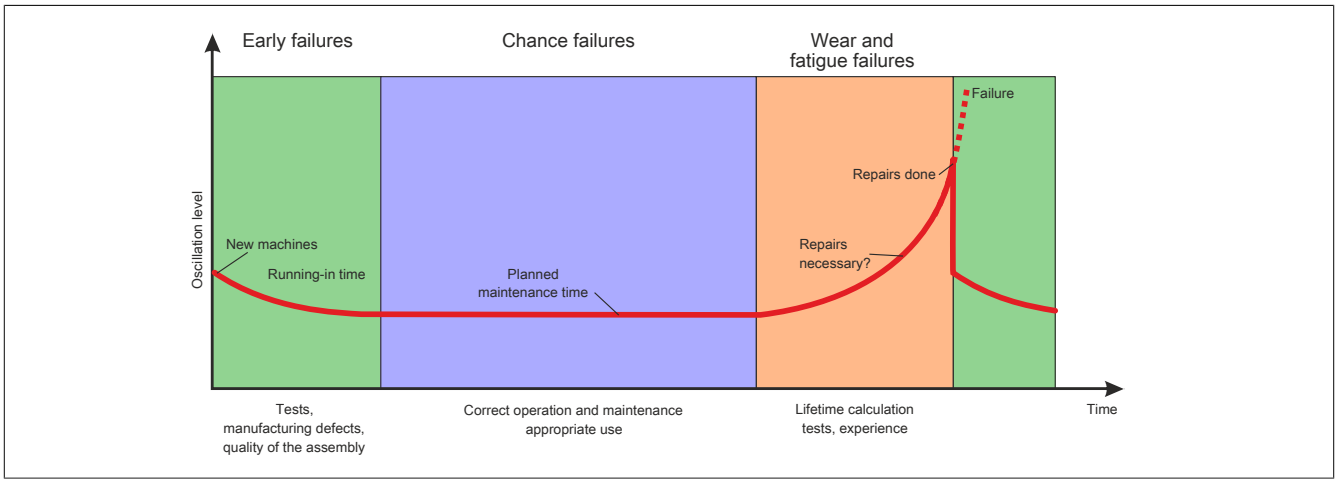


Figure 402: Bathtub curve illustrating the three typical phases

Each component is subject to the regularities of this curve, with a typical trend emerging as a result.

- **Area 1 (early failures)** is characterized by a decreasing failure rate. Early failures are caused almost exclusively by errors in assembly or construction. Nevertheless, particular care and quality during manufacturing and initial operation significantly reduces the failure rate at the beginning. This area also explains the increased failure performance after an intervention in a system that functions well.
- During continuous operation in **Area 2 (chance failures)**, the failure rate is almost consistent. These chance failures are fundamentally difficult to ascertain and, most importantly, not easily influenced. Operating and maintenance errors contribute towards an increase in the failure rate in this region.
- The failure rate increases dramatically in **Area 3 (wear and failure due to fatigue)**. Wear and fatigue failures are primarily characterized by damage that progresses slowly over time.

The trend provides valuable information about the failure probability of the parameters measured by condition monitoring. This usually behaves like the bathtub curve, i.e. an increase in the characteristic value signifies a change in the system. The characteristic values can be synchronized with the operating parameters through the integration of automation technology. Assessing curve performance and incorporating operating parameters makes it possible to identify the best time to perform service work depending on condition.

In addition, oscillations are often representative of the condition of a machine or component. They are a good indication of wear or damage. One example of this is roller bearings. Surface damage (pitting) leads to increased oscillations in the bearing housing, which can then be measured and analyzed. An increase in oscillations during operation indicates damage and/or increased wear. By constantly observing this condition, deviations from normal operation can be recognized immediately.

Damage development and the damage chain

Explaining damage development with a roller bearing example

The majority of bearing damage develops slowly and usually without being noticed. In many cases, it is only once the damage is more advanced that irregular running and unusual operating noises indicate bearing damage. This points to material fatigue, e.g. chipping or altered radial clearance through wear.
If the damage is so advanced that it can be detected without measuring equipment, spontaneous failures such as blockages and breakage of the bearing housing components often occur.

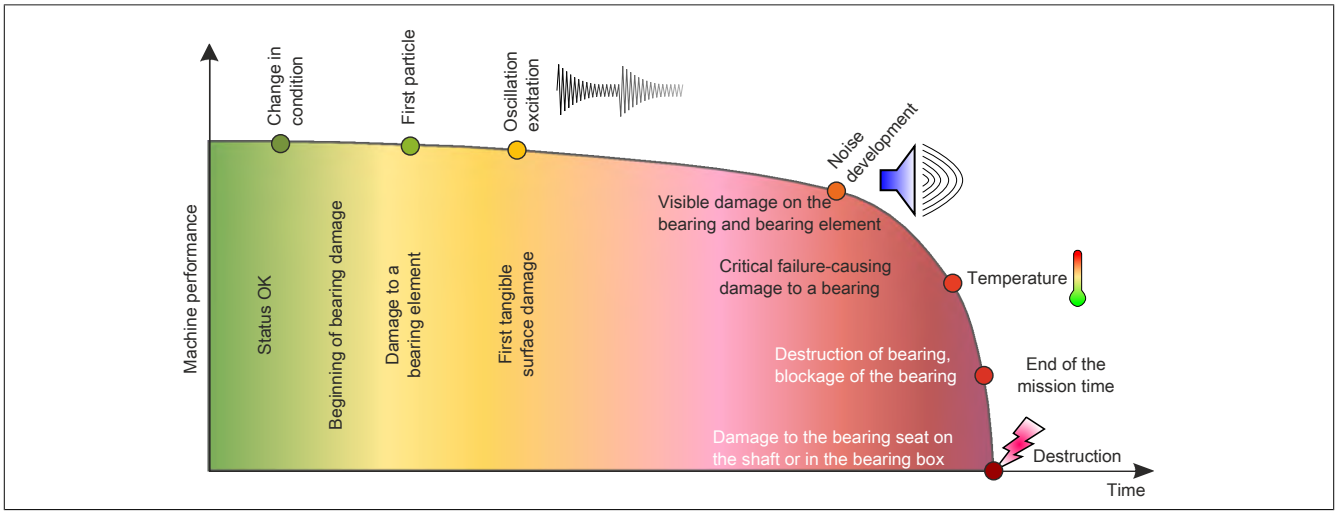


Figure 403: Illustration of the damage chain and the development of damage over time

The damage chain illustrated in the image above presents condition monitoring as an important tool in the condition-oriented operation and maintenance of a system.

It is possible to draw conclusions about the condition of the machine or its components from the parameters recorded by the sensors. Deterioration of the condition of components or system parts becomes apparent through the detection and observation of their condition, the consideration of the trend and, if necessary, through the detailed analysis of the measurement data obtained. Based on this, targeted measures can be put in place for maintenance.

Condition monitoring is a suitable option under the following conditions:

- Measurable parameters that correlate with a failure need to be identified and selected.
- The failure cannot be prevented by redesign or altered usage.

- Events lead to failures that occur randomly.
- Sufficient warning time must be given in advance before a function fails.

The consideration of the condition monitoring "tool" must not only be limited to the recognition of operating conditions, but should be integrated into the general asset management strategy as a component of this. In order to manage this, all types of condition monitoring and industrial diagnostics should be integrated into an overall strategy.

For a failure-oriented operational mode ("reactive maintenance"), components are only replaced if they can no longer fulfill their function. For a planned operational mode ("preventive maintenance"), components are replaced at a certain point in time – regardless of their current condition.

For state-oriented maintenance, the area where maintenance is planned can be significantly isolated while reducing the risk of failure at the same time.

	Advantages	Disadvantages
Reactive maintenance	- Utilization of the wear reserve - No costs during the period of use	- Unexpected failure - Consequential damage - High downtime costs - Low operational safety
Preventive maintenance	- Can be planned well	- No utilization of the wear reserve - Increased risk of failure after maintenance - Repair costs
State-oriented maintenance	- Early recognition of problems - Downtime can be planned - Utilization of the wear reserve - High operational safety - Avoidance of consequential damage	- Dealing with the issue - Investment costs

Table 591: Comparison of the advantages and disadvantages of standard maintenance strategies

4.26.4.4.1.2 Conventional condition monitoring

- There exists a lot of measurement and process data that is not currently used for condition monitoring (CM). Links and correlations with process parameters and further CM parameters can often be made possible only with considerable expenditure.
- CM systems are implemented as "isolated applications". In such cases condition monitoring is performed by standalone sensor and measurement systems with standalone hardware and software
- The range of different systems can lead to significant problems in the on-site operation of the system. Different software solutions make it more difficult since there is separate hardware and a separate user interface for each CM method and each CM tool.
- In many cases, necessary expert knowledge specific to a system is not available. The complexity of some configuration tools exceeds the user's existing expertise.

Using the X20CM4810 together with B&R standard modules has the following advantages:

- Easy exchange of process data and condition monitoring data
- Easy integration of parameters in the overall process
- Modular construction

4.26.4.4.1.3 Overview of condition monitoring methods

Method	Brief description of operation	Available signals / interfaces
Determination of the condition of coolants and lubricants Visual assessment, filtration, ferrography, magnet detection, spectroscopy, radioactive trace analysis	Quantitative examination of wear products (filtering, magnetic catches, ferrography, spectral oil analysis, particle counting) that are obtained from the lubricant oil or coolant fluid Regular taking of samples according to a defined time schedule or according to operating hours Quantitative comparison of the samples	Using suitable measurement systems, these condition monitoring methods can be processed in the B&R system using analog/digital inputs or bus coupler modules.
Thermal diagnostics Temperature sensors, thermometry, infrared measurement technology	Recording of temperatures through sensors with different physical modes of action Recording of temperature distribution through detection of infrared radiation	
Acoustic emission analysis Airborne sound measurement pulse analysis, pulse density fluctuation analysis, sound pressure measurement, acoustic emission location	Airborne sound measurement from infrasound to ultrasound using a microphone Multidimensional microphone structure for emission source location Recognition of microdamage (cracks) etc. through the measurement of acoustic emissions of transient waves with high frequencies	
Vibration measurement Structure-borne sound measurement, FFT analyses, order analyses, modal analyses	Vibroacoustic diagnostics Measurement of the structure-borne sound at bearing positions or structures with accelerometers, analysis and evaluation	
Electrical parameters, motor current analysis, insulation resistance measurement	Compilation of electro-technical parameters and analysis with regard to condition monitoring	These condition monitoring methods can be processed in the B&R system using analog/digital inputs, bus coupler modules or B&R drive systems (different functions from system to system).

4.26.4.4.2 Oscillation measurement technology

4.26.4.4.2.1 Sensor technology

Oscillation sensors convert the mechanical oscillations of the machines being measured into an electrical signal.

For the most part, structure-borne sound, i.e. the sound that spreads through a solid object, is measured. The three oscillation magnitudes correlate mathematically to the integration or differentiation of the basic variables. Oscillation velocity is calculated through integration from the oscillation acceleration; oscillation displacement is calculated through integration from the oscillation velocity.

The acceleration measured within the scope of the condition monitoring is typically measured with piezoelectric sensors. The oscillation sensors being used utilize the piezoelectric properties of quartz or certain ceramics. The actual measured value is a force that is proportional to the acceleration.

The piezoelectric effect involves a charge separation when a force acts on the piezoelectric material. This is in proportion to the force and is consequently proportional to the acceleration. Piezoelectric quartz or piezoelectric ceramic is used as the piezoelectric material. The output signal is an electrical charge that is specified in pC (picocoulombs). A charging amplifier is necessary in order to convert the charge into a voltage signal.

The **I**ntegrated **E**lectronics **P**iezo **E**lectric (IEPE) technology used in B&R sensors strengthens the signal directly in the sensor and emits it as a low-resistance voltage signal. The sensitivity is specified in mV/g where g represents the gravity of the earth.

$1g = 9.81\ m/s^2$

Information:

Piezoelectric sensors cannot measure static magnitudes.

Basic design

The piezoelectric crystal is jammed between the seismic mass and the foundation with what is known as a compression mode sensor. Through the acceleration that occurs, the force that is acting upon the crystal increases or decreases. The bigger the implemented seismic mass, the bigger the output signal.

Sensors of this type can be constructed with a very high rigidity and therefore have a correspondingly high resonant frequency.

Magnitudes of influence on the sensors

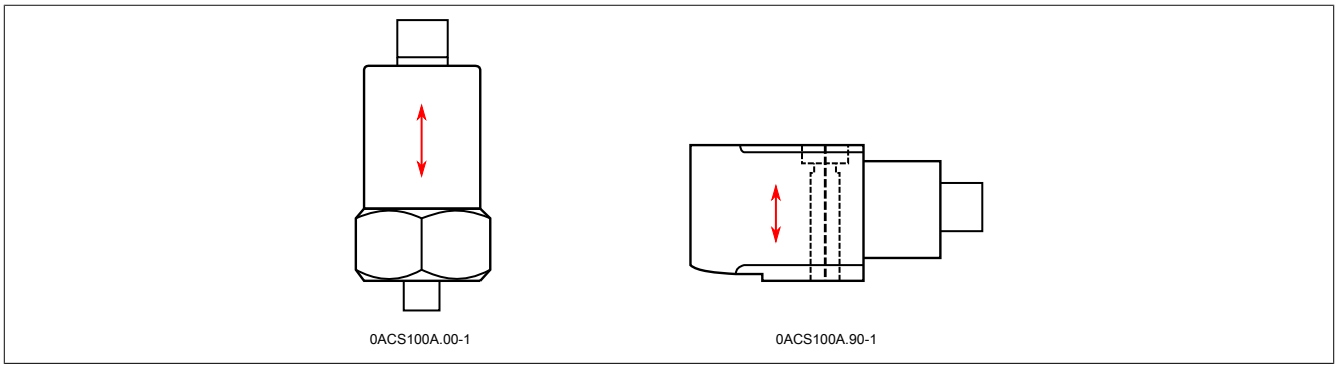
Mounting direction - Preferred direction

Oscillation sensors can be fitted at any location. The installation position usually results from the measuring task itself. Nevertheless, oscillation sensors have a preferred measurement direction that is usually indicated on the housing of the sensor.

Of course, oscillations in cross direction to the installation position also act upon the sensor. These can be compensated as much as possible through appropriate constructive measures and suitable selection of the piezoelectric crystal.

Installation position

The 0ACS100A.00-1 oscillation sensor from B&R is designed to measure the longitudinal axis; the 0ACS100A.90-1 sensor is designed to measure the lateral axis.



Cross-sensitivity

Oscillations in all directions act upon the sensor. The sensor should ideally transfer oscillations in its main direction, i.e. in the direction of the sensor. Oscillations that deviate from this main direction are still registered by the sensor, however, and transferred to the overall signal at different strengths depending on its type.

Cables

When transferring a signal over a connector, errors such as noise, ground loops and contortions may occur. This influence is particularly important in the transfer of charges since system noise is a function of the cable's capacity. When using IEPE technology, the sensor produces a high voltage signal with a low source impedance due to its internal electronics.
As a result, this technology is well suited for signal transmission over long lines.

The supply unit provides constant current to supply the IEPE electronics in the sensor. The maximum frequency that can be transferred via the test lead without considerable loss depends on the length of the cable, the cable capacity and the ratio between the output amplitude and the constant current.

Information:

Maximum cable length when using the 0ACCxxx0.01-1 cable from B&R: 20 m.

Temperature influence

All piezoelectric materials also have a distinct pyroelectric effect. This describes the change in the electric polarization of ferroelectric materials as a result of a change in temperature. This effect is undesirable since it often leads to charge separations in the oscillation measurement. These arise from the change in temperature and not through the mechanical vibrations occurring in the measured object.

This effect can be limited by the design, however. The interferences are grouped together in the interference transfer factor for temperature changes.

Temperature drift:

The values specified in the sensor's technical data have been determined as a step response to a change in temperature for the lower electrical limit frequency f_u = 1 Hz.

Changes in temperature, in particular, cause interference in the low frequency domain below f = 10 Hz since this is generally a low frequency event.

Interference

A backlash on the sensors occurs near electromechanical machines such as motors and generators due to electromagnetic alternating fields, the associated induction and magnetostriction. This backlash is very low, however, due to the screening concept used and the use of IEPE technology.

This effect is specified in the interference transfer factor. It is determined by a magnetic flow density of 0.01 T and a frequency of 50 Hz.

Information:

B&R sensors have an isolated base. When using sensors from other manufacturers, it is important to pay attention to isolation/screening in order to minimize interference. This allows interference frequencies with single and double mains frequency.

Linearity

The piezoelectric sensor is linear over long distances of the frequency response.

Frequency response

The frequency response of the sensor is determined by its mechanical construction. The seismic mass and the rigidity of the inner structure is crucial here, as is its construction.

The sensitivity is linear in other areas of the frequency response. The frequency response only increases significantly when near the resonant frequency. Since misinterpretations can occur in proximity to the resonant frequency, the resonant frequency must be correspondingly high.

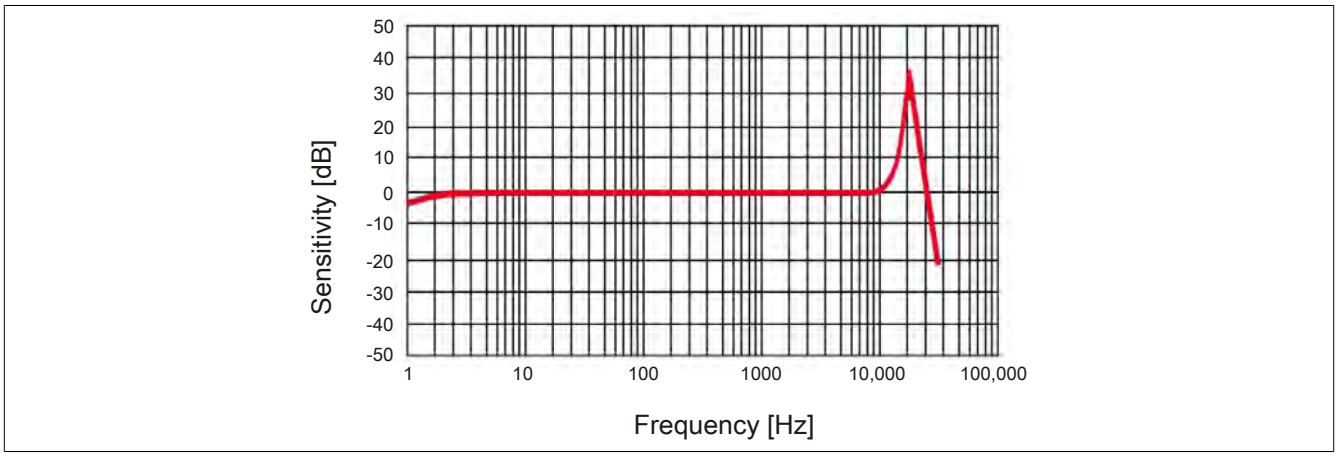


Figure 404: Frequency response of 0ACS100A.00-1 and 0ACS100A.90-1 sensors from B&R

Installing sensors

Sensors can be connected to object to be measured using various methods. How the sensors are installed on the measurement object is crucial for the quality of the overall measurement.
In order to transfer all frequency portions to be measured to the sensor accordingly, very good coupling of the sensor to the mechanical component is necessary.

Machine parts may be subject to temperature-related expansion and deformation, with the result that the sensor no longer has its whole measurement surface available. This affects the quality of the measurement.

Figure 405: Temperature deformation of a machine part (excessive deformation shown)

Information:

For optimal measurement, the base surface of the sensor must be flat and the sensor must be fully supported.

In order to increase the quality of the measurement accordingly, a fixed connection to the measurement object is necessary. Cover plates and plastic parts are therefore not suitable for the attaching sensors.

The following methods are available for installing sensors:

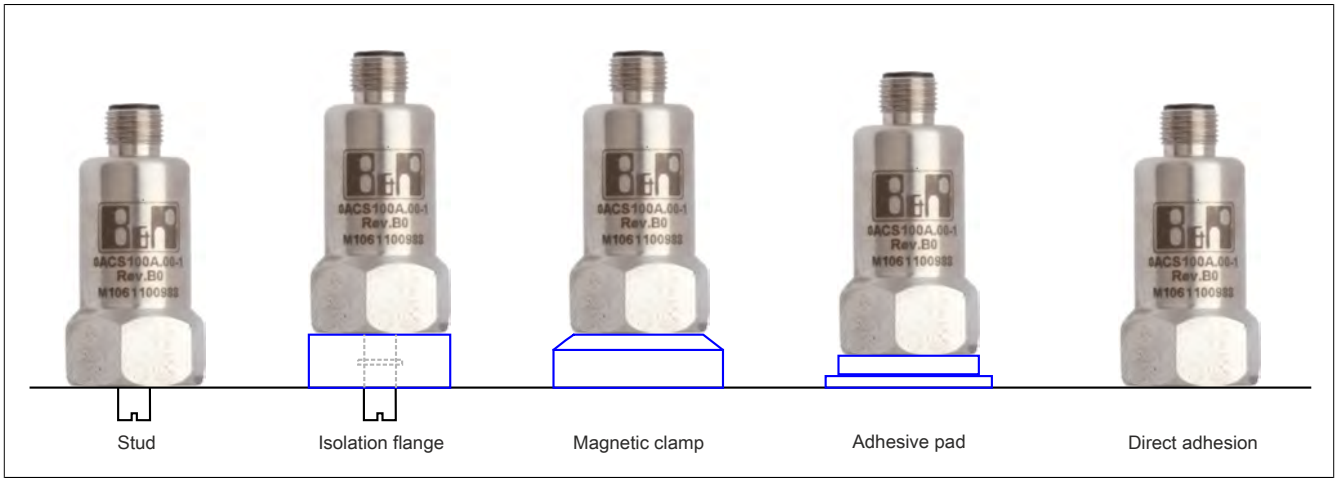


Figure 406: Overview of installation methods

Of all of the mounting methods, fastening by means of a screw is preferable due to the low attenuation between the sensor and the measurement surface.

Typical sensor installation is performed by screwing the sensor to the measurement object with what are called studs (supplied with the sensor). Studs are specially-made setscrews made from special materials that facilitate the optimal transfer of vibrations.

If the mounting location is well prepared and the sensor is screwed on correctly, frequencies of up to approximately 10 kHz can be transferred without significant loss.

Information:

To ensure measurements of sufficient quality, B&R recommends mounting the sensor with a screw.

Ground loops can occur at great distances. If necessary, isolated mounting must be performed using an isolated adhesive mounting plate.

The resonant frequency is reduced by additional elements such as an isolation flange, collar screw, magnetic clamp and probe tip positioned between the coupling surfaces. The coupling becomes softer using these elements. These differences can be clearly seen in the frequency response diagram
Different frequency responses of the relative voltage transfer factor are illustrated in the image below.

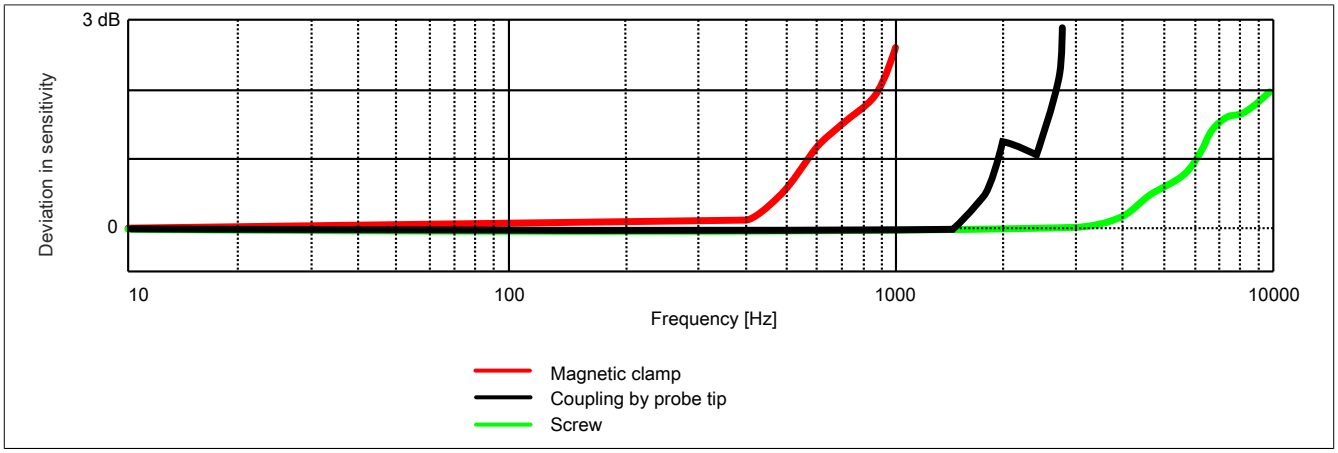


Figure 407: Attenuation of the different types of sensor mounting

The choice of mounting is influenced by the resonance frequency and temperature. The following table shows how strongly these influences impact on the different mounting methods.

	Resonant frequency	Temperature
Stud	●	●
Instant adhesive	●	●
Beeswax	◐	○
Double-sided adhesive tape	○	◐
Magnetic clamp	◐	●
Probe tip	○	○

Effects on the installation methods:

● High ◐ Medium ○ Low

Table 592: Overview of installation methods

Installation procedure

Depending on the conditions of the location, sensors can be screwed directly onto the surface of the object to be measured.

STEP 1: As smooth and flat a surface as possible is needed to mount the sensors. The size needed depends on the sensor and can be found in its data sheet.

For a vertical installation position: "Dimensions" on page 2732
For a horizontal installation position: "Dimensions" on page 2734

STEP 2: An M8 blind hole is needed to attach the B&R sensor.

STEP 3: To further improve the transfer performance, a thin layer of silicone grease can be applied between the object surface and the sensor mounting surface. The sensor should then be pressed on briefly so that any excess grease is pushed out. This is not an essential part of the application and is only useful when measuring particularly high frequencies.

STEP 4: The sensor should be tightened by approx. 8 Nm when using the M8x1 screw thread. If necessary, the sensor can be protected against loosening using an adhesive.

Sensor positioning

To ensure optimal detection and measurement of frequencies propagating from a point of damage, sensor positioning plays an important role. The ideal position for mounting a sensor on a structure is often difficult to reach and is not always necessary. Since sound waves propagate throughout the entire structure, the damage frequencies are measured with varying intensity or amplitude (green arrow). If a flexible connection is used, a valid measurement is no longer possible (red arrow).

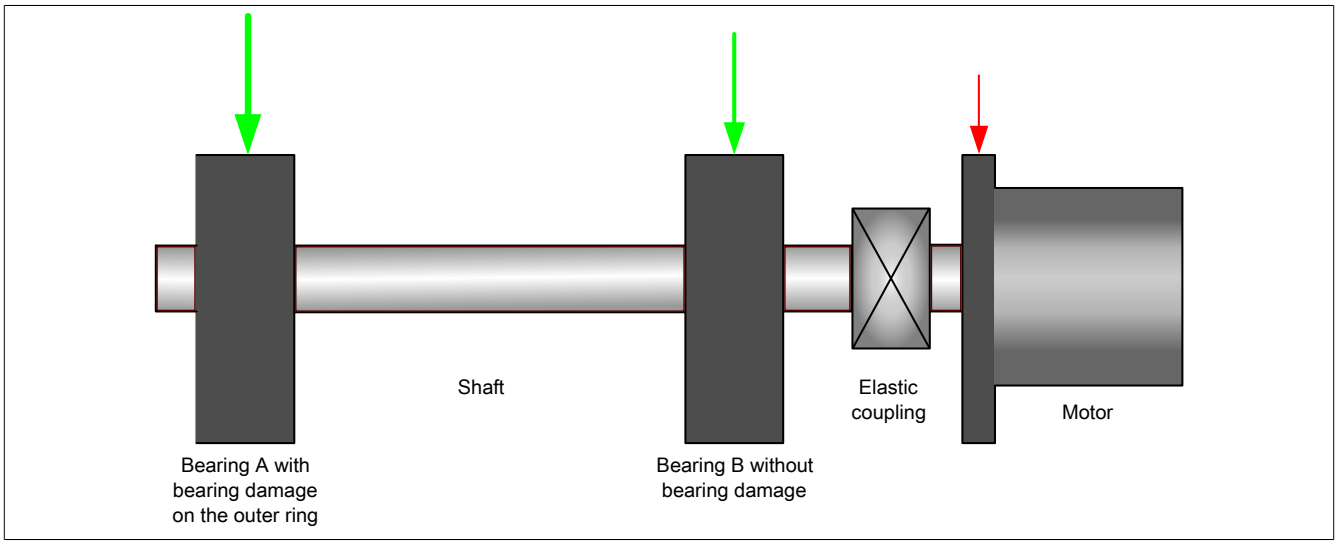


Figure 408: Suitable and unsuitable sensor attachments

4.26.4.4.2.2 Oscillations - Overview of measuring structure-borne sound

Oscillations

Mechanical oscillations

Oscillations are forms of movement that occur very frequently in nature. Harmonic oscillation is the third basic type of form of movement alongside uniform movement and uniform accelerating movement. An oscillation or vibration is a cyclical, i.e. repetitive simultaneous movement of a structure in its rest or equilibrium position.

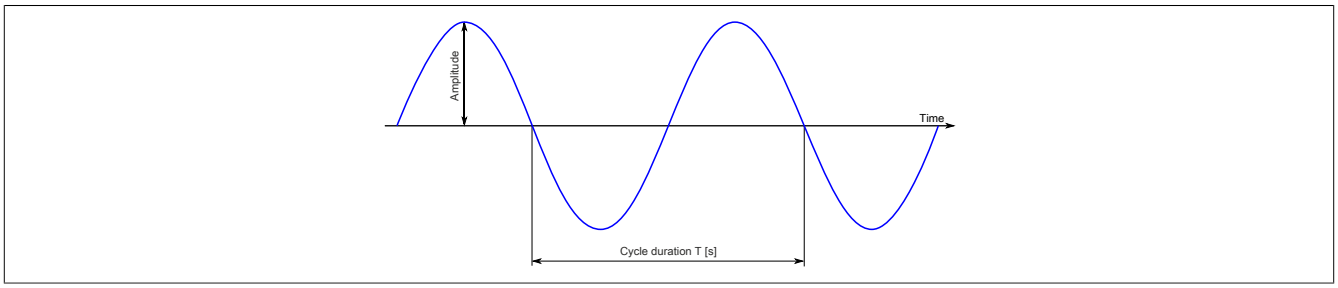


Figure 409: Illustration of a basic oscillation

If a fixed medium is stimulated by an impact, structure-borne sound spreads throughout it. This consists of additional frequencies which are determined by the shape of the structure and the material it is made from (e.g. gong or concrete block).

A portion of the structure-borne sound energy is converted into airborne sound through the surrounding atmosphere.

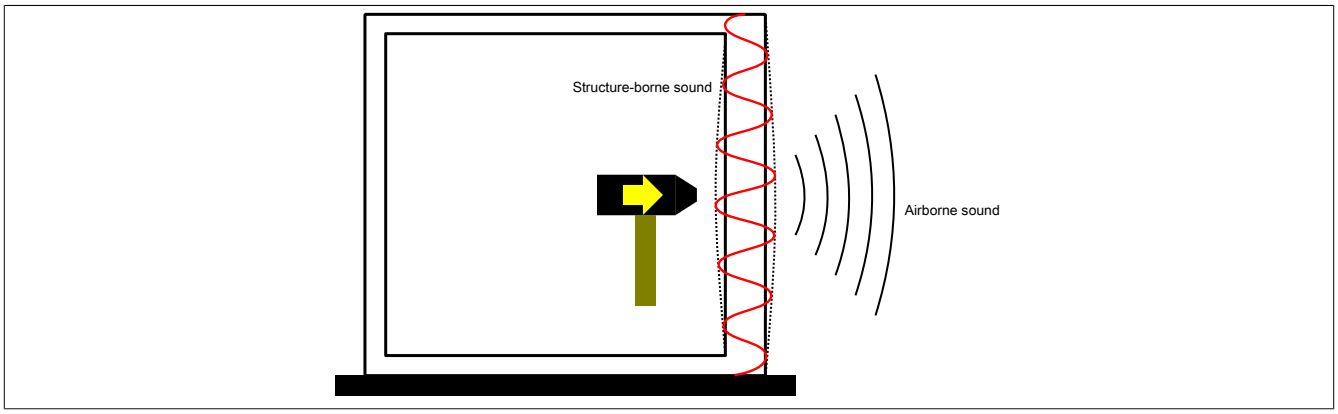


Figure 410: Propagation of structure-borne sound

Resonant frequency

Every machine has what are known as resonant frequencies. These must be observed during operation since with these frequencies the amplitude of the oscillation increases dramatically, putting strain on the mechanical components. If harmonic oscillations occur for a long time in proximity to the resonant frequency, this can lead to a so-called "resonance catastrophe", which causes the destruction of the affected part.

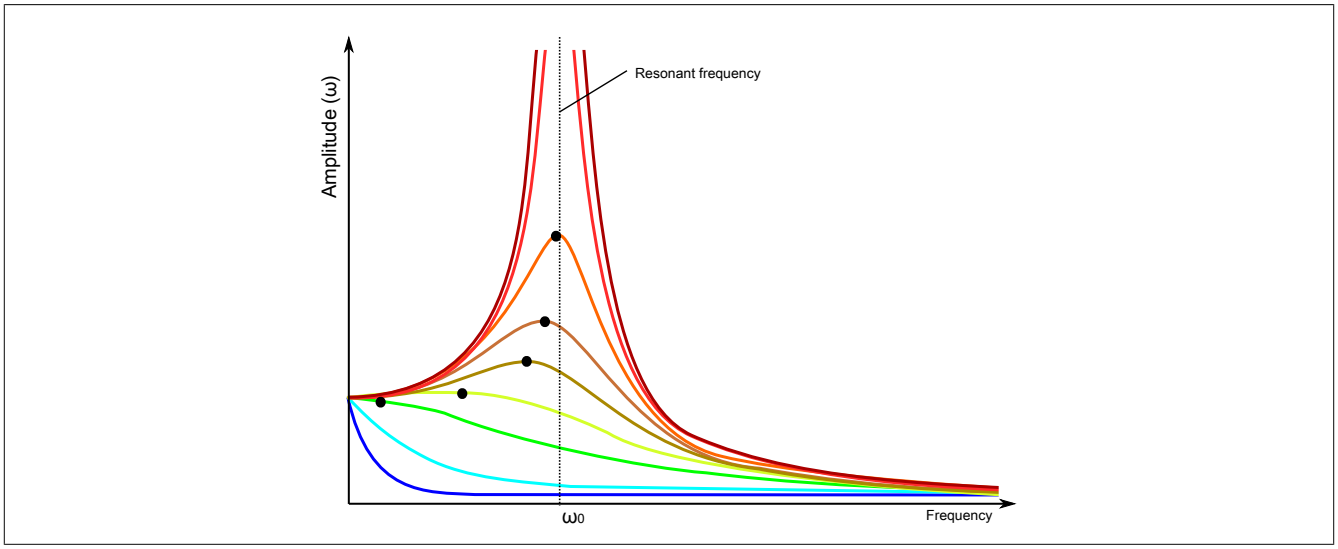


Figure 411: Increase of the amplitude in proximity to the resonant frequency

The measurement and subsequent analysis of the mechanical oscillations on stationary and rotating parts of machines, support structures and pipelines has become accepted as technically possible with practically applicable monitoring procedures.

Mechanical oscillations are a good parameter for detecting initial defects and damage and can be used for machine diagnostics.

The consequence of stress is always damage. If cyclical stress occur, it can be identified by its excitation frequency and intensity.

There are numerous overlapping causes for oscillations. The size (amplitude) of the oscillation depends on several factors such as attenuation through joints or grease, the rigidity of the component, the housing and foundations, and much more.

The absolute bearing oscillation is measured on the housing of the machine and involves the movements of the housing in relation to a fixed reference point in the room.

Causes of oscillations:

Imbalance

In accordance with DIN ISO 1925[1)], an imbalance is present in a rotating system if forces or oscillation movements are transferred to the bearing as a consequence of imbalanced centrifuges.

Imbalances on a rotating structure not only cause forces on the bearing and foundations, but also oscillations in the machine. These oscillations have a harmonic nature, with the excitation frequency corresponding to the rotary frequency of the unbalanced rotor.

Alignment errors

The main function of coupling is to connect two shafts in order to achieve a statically determinate overall system. In addition to transferring torque, couplings also offset misalignment (radial, axial, angular) to a certain extent. If the misalignment exceeds the ability of the coupling to compensate, however, additional stress such as increased bearing forces, shaft deformations and axial forces occur on the machine components involved.

Oscillations have a harmonic nature and are bound to the rotary frequency of the misaligned shafts and the multiples of this frequency. Misalignment can be measured using the rotary frequency of the misaligned part or its harmonic oscillations.

Shocks

Foreign objects as well as loose or colliding parts can cause shocks between rotating and stationary parts. These shocks repeat periodically once or several times each time the shaft revolves.

The frequency of these shock repetitions corresponds to the rotary frequency of the shaft or its harmonic frequency.

Roller bearing damage

Most bearing damage results from changes on the surface (pitting). By rolling over the damaged area on the inner ring, outer ring, cage or rolling element, pulse-shaped shocks occur that make the bearing structure and its components vibrate.

Each of these shocks appears in the oscillation signal through the typical course of a shock sequence. Characteristic values can be obtained from these measurements that give an indication of the condition of the bearing.

The excitation frequency on the inner ring, outer ring, cage and roller bearing damage is specified by the bearing manufacturer.

Magnetic induction

The rotating magnetic field causes counterforces in the stator of the machine. This electric magnetic stimulation often causes oscillations on the electric motors that are hard to detect.

Inverters also often lead to an inference of oscillations, the cause of which is of an electrical magnetic nature.

Effects

Machines and systems with moving parts cause mechanical oscillations. The effects on the immediate location and surrounding area include tremors and structure-borne sound, often creating a disturbing noise development.

Increased vibrations can lead to malfunctions in the machine, particularly in measurement and control devices. If this causes the measuring equipment to resonate as well, incorrect measurements will result and manufacturing quality will suffer.

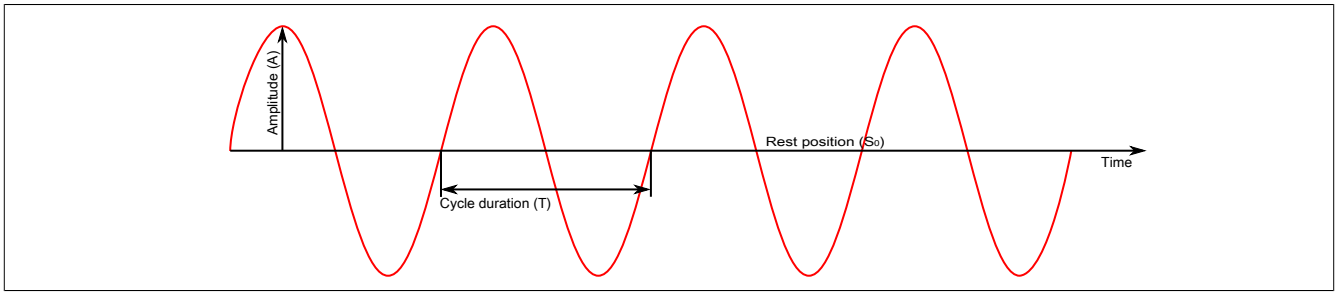
In addition, stress will develop on the components of the machine. Unwanted vibrations lead to increased wear with partly plastic distortion of components and increased crack formation all the way up to failure.

Noticeable oscillations are felt through the equilibrium organ and sense of touch. It can impair working performance and well-being, even leading to health damage.

[1)] DIN ISO 1925: Issue: 1996-11 Mechanical oscillations - Balancing technology - Terms (ISO 1925:1990 + AMD 1:1995)

Oscillation parameters

Parameter	Explanation	Symbol	Formula
Rest position	The structure's undisplaced position	s_0	
Amplitude	The greatest displacement from the rest position	A	
Period duration	Minimal time span for a complete oscillation after which a structure has reached its initial position and initial speed again	T	
Frequency	Number of oscillations per unit of time	f	f = 1 / T
Angular velocity	Change of angle in the radian measure over time	ω	ω = 2 * π * f



Large mechanical oscillations

An oscillation consists path (s), velocity (v) and acceleration (α) values.

These three values have a consistent relationship with one another and can be converted from one to the other using simple calculations.

The B&R sensors measure oscillation acceleration. The unit is m/s^2, although acceleration is often specified in the unit g ($1g = 9.81\ m/s^2$) for the earth's acceleration.

For some diagnostics, however, the oscillation velocity or displacement is more significant. The acceleration can then be passed converted to the oscillation velocity through integration. The path can be calculated from the acceleration by using integration twice.

Displacement

$$s = \hat{s} \cdot \sin(\omega t + \varphi)$$

Oscillation velocity

$$v = \frac{ds}{dt} = \hat{s} \cdot \omega \cdot \cos(\omega t + \varphi)$$

Oscillation acceleration

$$\alpha = \frac{d^2s}{dt^2} = \frac{dv}{dt} = -\hat{s} \cdot \omega^2 \cdot \sin(\omega t + \varphi)$$

Converting from one value to the other through Integration or differentiation

Table 593: Mathematical relationship

Information:

Displacement is not calculated by the X20CM4810.

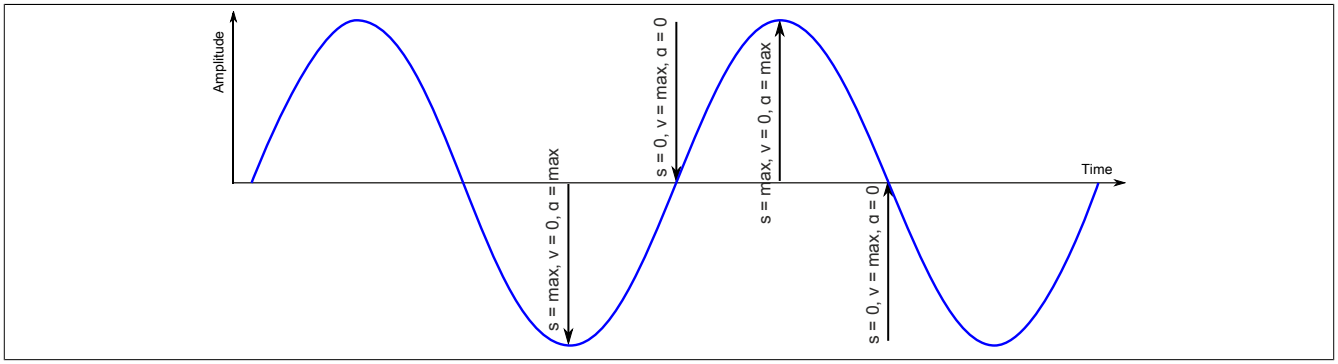


Figure 412: The s-v-a relationship

A harmonic oscillation can be clearly described by its amplitude, frequency and phase angle.

- The amplitude in the path, velocity or acceleration indicates the instantaneous value.
- The frequency describes how often an oscillation changes within one second. In oscillation diagnostics, this plays an important role since many frequencies can be assigned to one cause.
- The phase angle refers to the starting point of the oscillation. This is usually not that important since in most cases several oscillations are present.

Fast Fourier transforms (FFT)

Oscillation signals generally consist of a number of oscillations that occur simultaneously and overlap. Individual frequencies are not directly evident from a timing diagram.

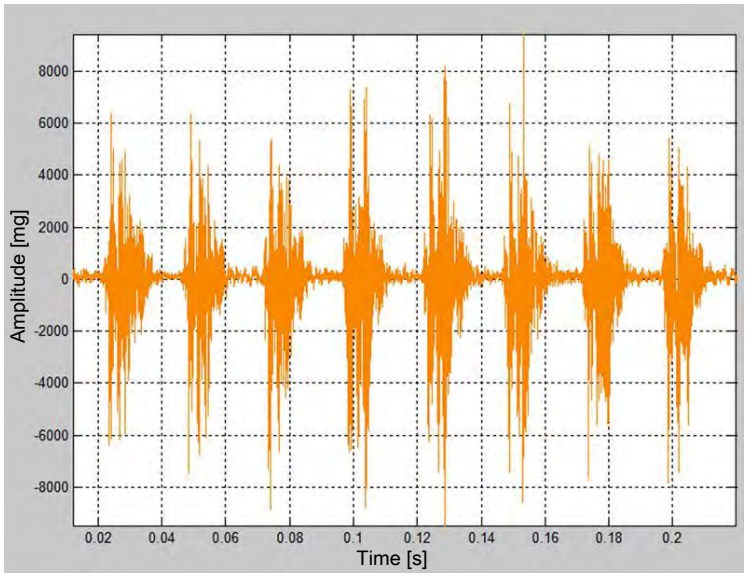


Figure 413: Timing diagram of an oscillation

Calculating a line spectrum is suitable for analyzing a mixture of oscillations of different frequencies where each participating oscillation and their frequencies and amplitudes are represented by a single line.

Within the scope of condition monitoring, spectra are a valuable aid in finding the cause of a failure. Many frequencies can be traced back to individual components so that damaged components can be identified.

Adding sinusoidal oscillations to generate a signal

The following figures show how a square wave signal is created by overlapping sinusoidal oscillations.

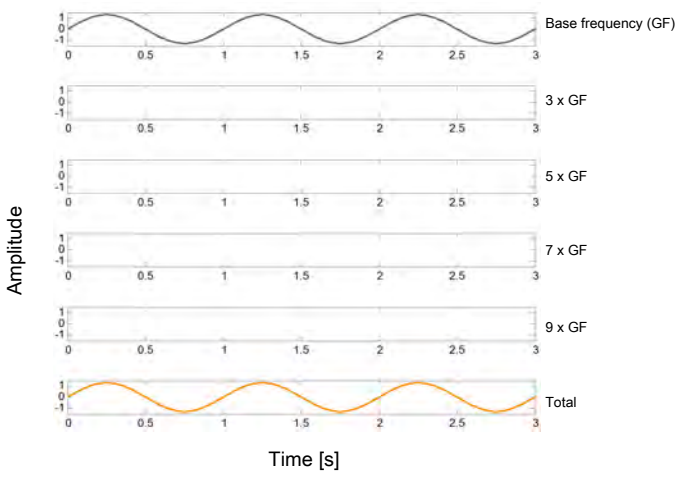


Figure 414: Pure sinusoidal oscillation

Sinusoidal oscillation with 1 hertz and an amplitude of 1.

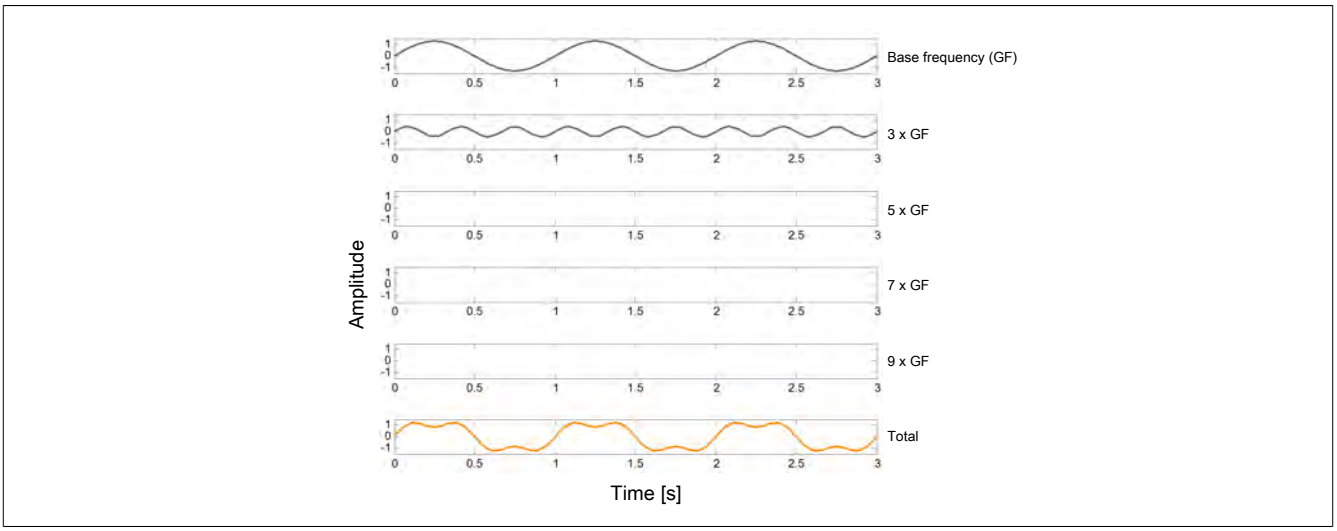


Figure 415: Sinusoidal oscillation with one harmonic

Sinusoidal oscillation with 1 hertz and an amplitude of 1 and sinusoidal oscillation with 3x the base frequency, i.e. 3 hertz and a lower amplitude.

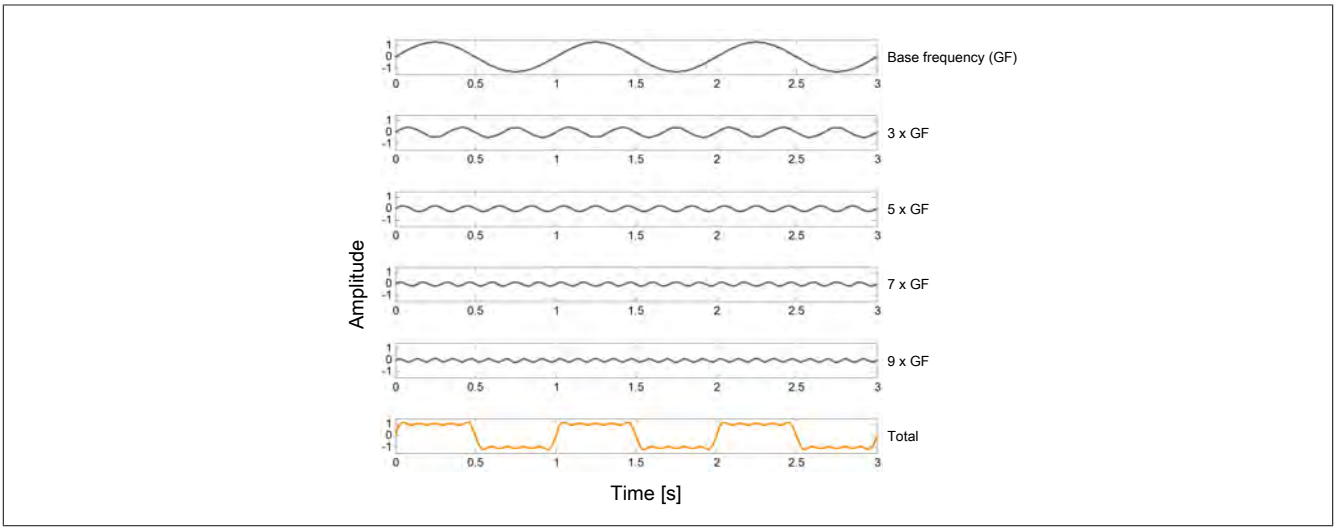


Figure 416: Sinusoidal oscillation with several harmonics

Sinusoidal oscillation with 1 hertz and an amplitude of 1 and sinusoidal oscillation with 3x the base frequency and a lower amplitude, and others with 5x 7x and 9x the base frequency.

General description

The Fourier transform is the basic principle of frequency analysis. Using mathematical approaches, this process brings the time signal waveform into the frequency representation (spectrum). Probably the most well-known concept in connection with signal processing and frequency analysis is the fast Fourier transform, or FFT.

The fast Fourier transform assumes that each harmonic oscillation can be broken down into any number of sinusoidal and cosinusoidal waves, the sum of which reproduces the original oscillation. Linked individual waves are "broken down" again accordingly.

If this procedure is then applied to a single sine signal with a constant frequency, a single line is shown in the frequency spectrum.

In order to be able to evaluate single partial oscillations into amplitude and frequency, the digitized time signal is converted into a frequency spectrum. In addition, a small extract is taken from the signal; this is known as the time window.

Using the FFT algorithm, the frequency spectrum is calculated from this so that each involved oscillation and its associated frequencies and amplitudes is shown as a single line in the line spectrum.

Information about using FFT

Window functions

Depending on the signal structure and boundary conditions, discontinuities may occur at the time window limits of the extract taken. These reflect partial oscillations that do not exist at all in reality.

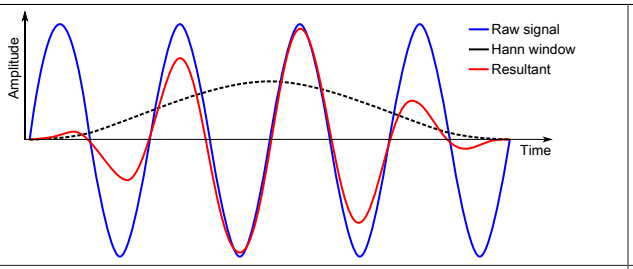
These discontinuities arise if the period of the sampling does not correspond to an integral multiple of the period of the time signal. This occurs with practically every real measured signal since this is composed of a number of signals with different period durations.

Window functions are used to suppress these discontinuities. This is done by multiplying the input signal with the window function and supplying the Fourier transform with the resulting signal.

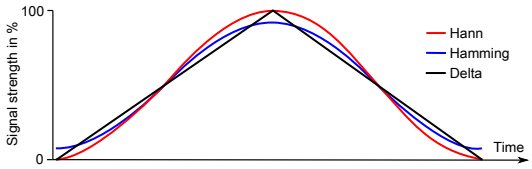
Common window functions are:

- Triangular window
- Hann window
- Hamming window

All of these functions share the fact that they approach zero at the edges, so the periodic continuation now no longer has any jump discontinuities.



Time signal with Hann window



Comparing window functions

Information:

Only the Hann window is used in the X20CM4810 module.

Sampling

Scanning or sampling refers to the recording of an analog value at certain intervals.

At the respective point in time, the precise voltage level of the signal is recorded and stored. The distance Δt (Delta t) between the recording points is called the sampling interval. If the inverse value is formed from the sampling rate, this results in the sampling frequency.

Sampling an analog signal once per second corresponds to a sampling rate of 1 Hz; sampling once per ms corresponds to a rate of 1 kHz.

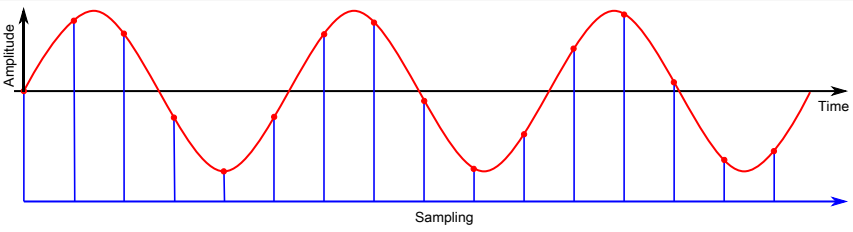


Figure 417: Sampling of a curve

If the sampling rate is many times higher than the theoretically required sampling frequency, it is called "oversampling". The reduction of the sampling rate to the required rate is called "downsampling".

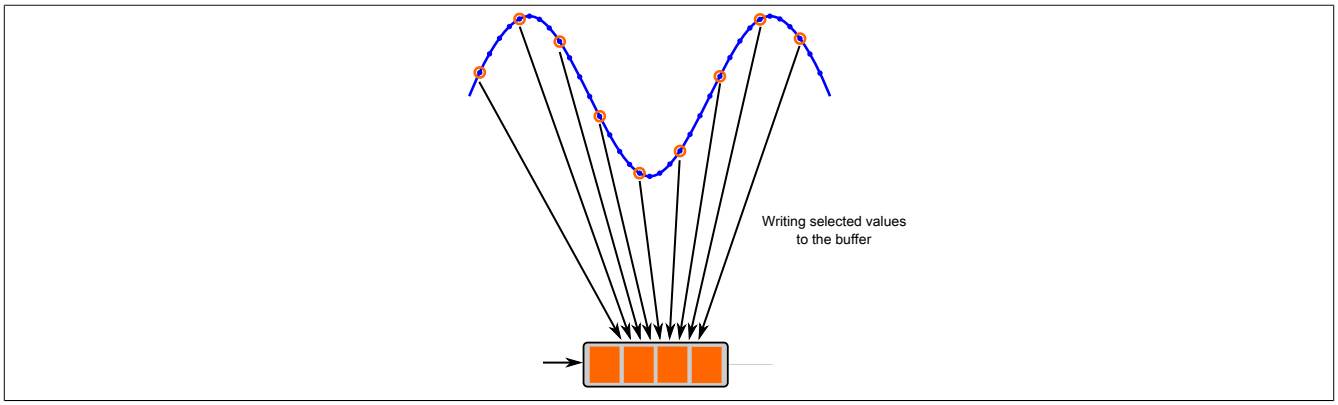
Using FFT for a signal with a multiple frequency of the sampling frequency results in only a single line on the spectrum.

Normally, however, frequency analysis is used on signals where the frequency is unknown. In other words, there is an arbitrary, periodic signal composed of various oscillations with different frequencies. As a result, no whole number frequencies of the oscillations being measured can be used as the sampling frequency. This causes additional lines to appear on the spectrum.

Depending on the resolution selected, the lines manifest themselves in different ways on the spectrum.

Buffer storage

The values that have been sampled are stored in the module's internal buffer. A copy of these values is transmitted every 300 ms.



The size of the buffer is constant and can store 8192 measurement values. This results in the ratio between the sampling frequency and the duration of measurement.

Duration of measurement = Buffer size / Sampling frequency

Since the values stored are dependent on the configured sampling frequency and not the hardware-based sampling frequency, not all values that are measured are stored. At a measurement duration of 318 ms, every second value is stored; at a duration of 15.9 ms, every hundredth value is stored.

These are indirectly adjustable using the registers "MaxFrequencyEnvelope01" and "MaxFrequencyRaw01"

Aliasing effect

The input signal is sampled at regular intervals. If the sampling rate used is too low, the input signal will be sampled incorrectly and a flawed image of the oscillation will occur. This undesirable phenomenon is called the aliasing effect.

To avoid such false results, the requirements of the theorem known as Nyquist's sampling theorem must be fulfilled in the sampling. This sampling theorem describes the necessary frequency ratio between the sampling and the signal and states that the sampling frequency must be more than double the maximum frequency of the measured signal.

Example of incorrect sampling

Sine wave with 4 kHz sampled at 6kHz. The red wave shows the sine wave measuring 2 kHz, which is a result of the sampling being too low.

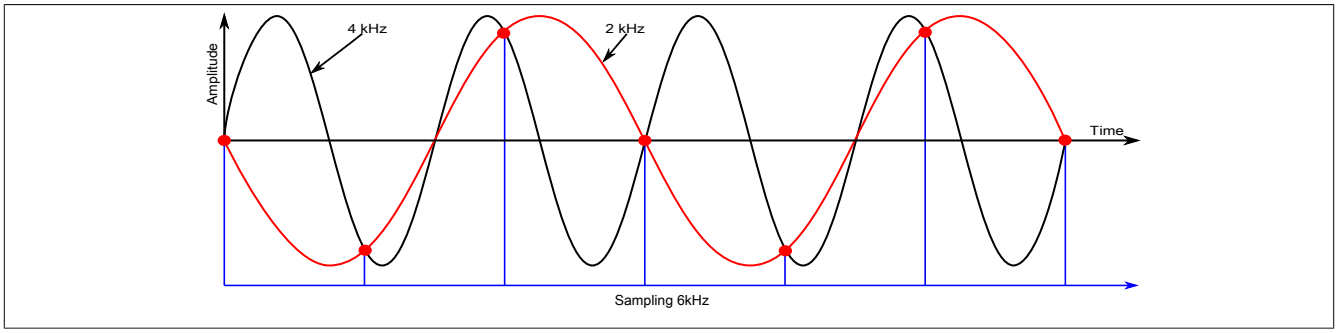


Figure 418: Incorrect sampling with 6 kHz and 4 kHz

Information:

The X20CM4810 module ensures that Nyquist's sampling theorem is always fulfilled.

In the X20CM4810 module, a sampling rate of 51.5625 is used to achieve a signal of 10 kHz.

Resolution

Resolution refers to the difference between two two adjacent measurement data points. This specifies the size of the distance between two lines along both the horizontal ("Time signal" or "Frequency spectrum") and vertical axis ("Quantization" of the amplitude).

An important factor affecting the quality of the resolution is the relationship between the number of measurement data points and the sampled frequency. The larger this ratio, the more accurately the measured signals correspond to the actual amplitude information. For example, 10,000 samplings of a 10 kHz signal yield a 10x more accurate amplitude characteristic than of a 100 kHz signal.

Information:

On the X20CM4810, a MaxFrequency of 200 Hz results in a distance of 0.0629 Hz between two lines.

Time signal

The resolution can be identified in the time signal from the distance between two adjacent measurement points.

Example

A "MaxFrequencyRaw" of 2 kHz is used in this example.

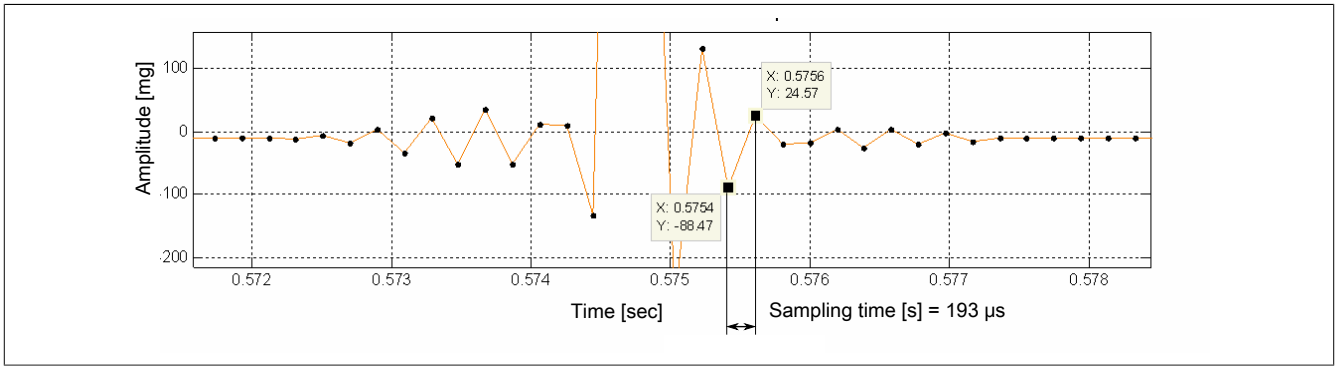


Figure 419: Time signal from a module with corresponding resolution

Frequency spectrum

The resolution in the frequency spectrum indicates the distance between the individual frequency lines (spectral lines) that can still be evaluated.

Example

Frequency spectrum at a MaxFrequency of 2 kHz.

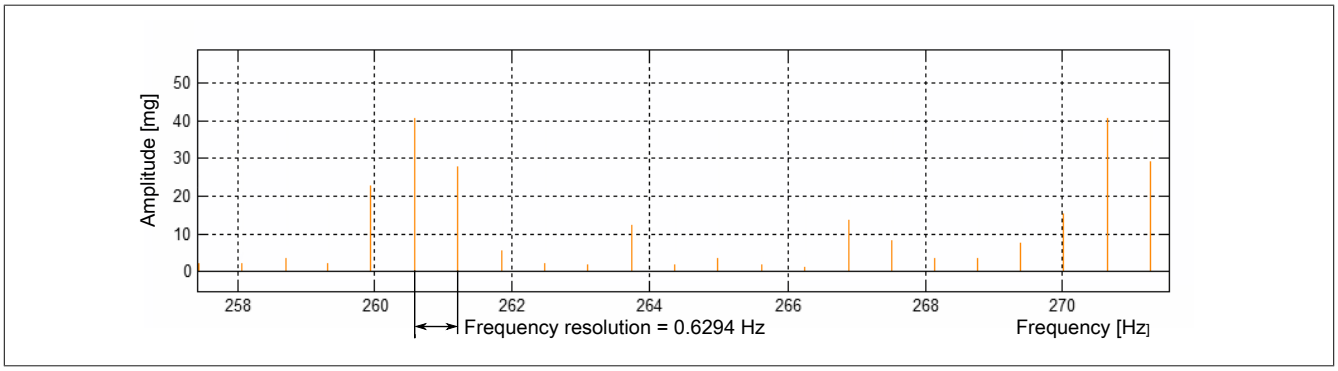


Figure 420: Frequency spectrum from the module

Quantization

To process the analog signal, an analog-to-digital converter (AD converter) is required. An AD converter can only measure voltage in stages, however. This is known as quantum voltage. The area to be measured is therefore quantized.

In an AD converter, the digital resolution depicts the number of levels there are in the quantization. This determines the accuracy and sensitivity with which a previously analog level value is depicted. The more available levels there are, the better the discrete signal received and the higher the sensitivity of the vibration measurement.

The resolution indicates how many varying digital values an analog signal can be converted into. The resolution is expressed in bits. "N-bit" means" 2^n", i.e. 2 to the power of n quantization levels are available.

8-bit resolution	256 level values
16-bit resolution	65,536 level values
24-bit resolution	16,777,216 level values

Example

At a sensor measurement range of ±50 g, the smallest distinguishable level is 5.96046E-06 (0.00000596046 g and 5.96 µg).

This resolution is much higher than the resolution of standard industrial sensors. This is in the range of 350 µg, representing a difference of a factor of 70.

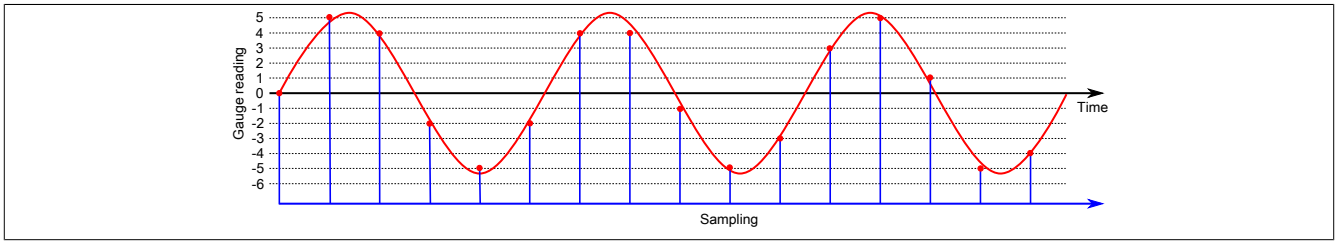


Figure 421: Quantization error at low resolution

Information:

The X20CM4810 module has 24-bit resolution.

Measurement time

The measurement time is dependent on the maximum frequency. See "MaxFrequencyEnvelope01" for the envelope characteristic values and "MaxFrequencyRaw01" for the raw values.

Maximum frequency	Sample frequency	Measurement time
10000 Hz	25781 Hz	0.3178 s
5000 Hz	12891 Hz	0.6355 s
2000 Hz	5156 Hz	1.5888 s
1000 Hz	2578 Hz	3.1775 s
500 Hz	1289 Hz	6.3550 s
200 Hz	516 Hz	15.8875 s

Table 594: Overview of possible measurement times.

Envelope

There are two main causes of oscillation.

1. Oscillations

Imbalance and problems with alignment lead to predominantly harmonic, sinusoidal oscillations.

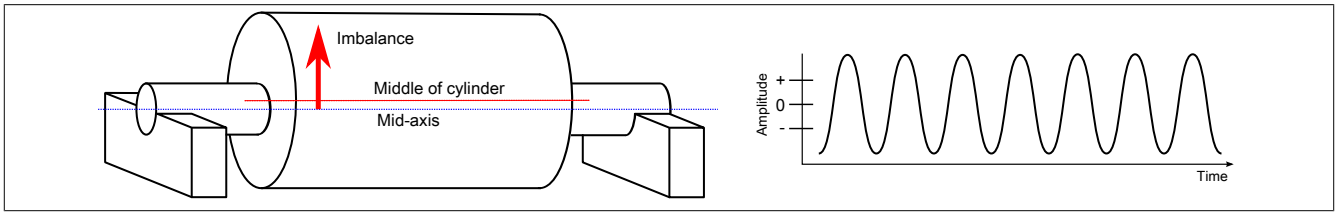


Figure 422: Imbalance - Harmonic oscillation

2 Impacts

Many types of machine damage can result in oscillations that cause the structure of the machine or adjacent machine parts to vibrate at their natural frequency. Impact-related causes of this are a result of corrosion, a rotor brushing up against the machine housing or roller bearing/gearing damage to the gears.

In the case of roller bearing damage, impact occurs when either the rolling elements roll over damage on the inner or outer track or when one of the rolling elements themselves is damaged.

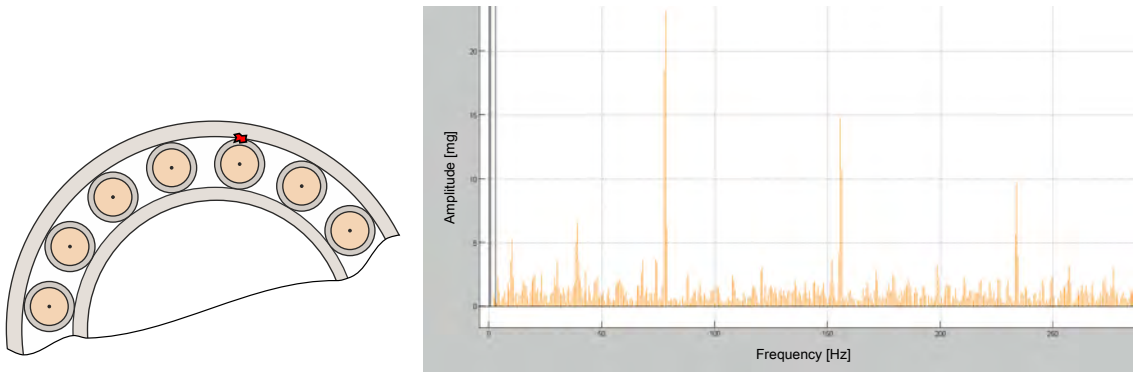


Figure 423: Bearing damage - FFT of envelope signal

This kind of impact can be compared to a clapper hitting a bell. If the bell is struck twice a second, it vibrates at its natural frequency and not 2 Hz. The natural frequency is determined by the constructive design and material properties. As with any sound boxes, mounting also factors into this.

If the damage is to the roller bearing track, every shock pulse will lead to a corresponding reaction in the vibrating system. It is only practical of course to measure the sum of all pulses, i.e. the total signal.

In the case of damage to roller bearings, the bearing rings are the first to start vibrating.

Oscillations are transmitted to the machine as waves and can be measured on the machine's surface. Naturally, it is a requirement that a path is available for the sound to be transmitted, i.e. no sound-absorbing limiting processes such as air, rubber etc. are present.

This signal can be measured on the surfaces of the machine by means of an acceleration sensor. The signal is made up of a variety of oscillations and impacts that overlap each other. When considering the time signal in this way, it is easy to see that allocating individual frequencies is impossible.

Using a Fast Fourier transform, this time signal can be converted to give the natural frequency of the system. These are in the high-frequency range. The rotor frequency and its harmonic frequency are clearly identifiable as the dominant frequency portion.

The rollover frequencies of the roller bearings are between 15 and 70 Hz at a speed of approximately 600 rpm, depending on the bearing.

In particular, shock pulses of a lower intensity, as they are when damage first begins, can barely be noticed or assessed. It is only when there is advanced damage to bearings that signal peaks can be clearly observed.

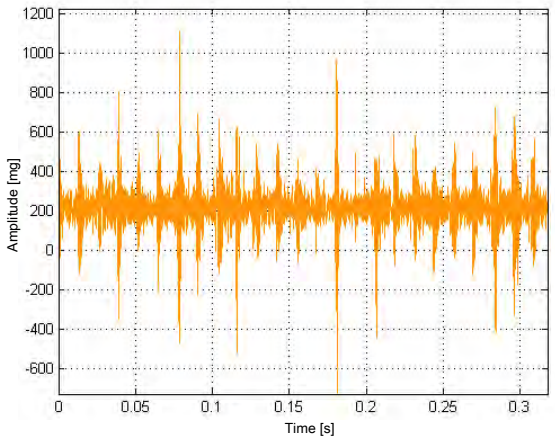


Figure 424: Advanced bearing damage at 600 rpm

To make the actual result, or shock sequence, clearly visible, it is obviously not enough to simply provide the amplitude spectrum. It is much more important that the process of convolution that took place when the signal occurred be appropriately reversed so as to separate the excitation function from the natural frequency. This is what envelope analysis provides.

An amplitude-modulated signal is made up of a high-frequency carrier signal in a low-frequency wanted signal. The amplitude of the carrier signal changes depending on the wanted signal. In the receiver, the wanted signal is extracted from the carrier signal by the formation of the envelope curve (demodulation).

In the case of machine resonances caused by periodic impacts, the machine resonances can be viewed as the carrier signal and the low-pass-filtered shock pulses can be viewed as the low-frequency modulation signal. Demodulation results in the shock pulses being extracted from the resonance frequencies.

Envelope analysis

Normally in an envelope analysis, the frequency spectrum of the envelope signal is evaluated. The frequency spectrum of the low-pass-filtered, aligned, amplitude-modulated sinusoidal oscillation is trivial since it relates to only one sinusoidal oscillation. Suppressing the steady component gives a frequency spectrum that exhibits only one increased amplitude at the frequency of the low-frequency sinusoidal oscillation.

The envelope signal of the periodically peaked excited machine resonance shows mostly increased amplitudes in the shock pulse repetition rate and its multiples.

The envelope analysis is therefore a method for differentiating between harmonic causes (imbalance, orientation) and impact-related causes (roller bearing damage, gearing damage, etc.).

Conversely, it must be stated that harmonic causes in an envelope spectrum cannot be determined accordingly.

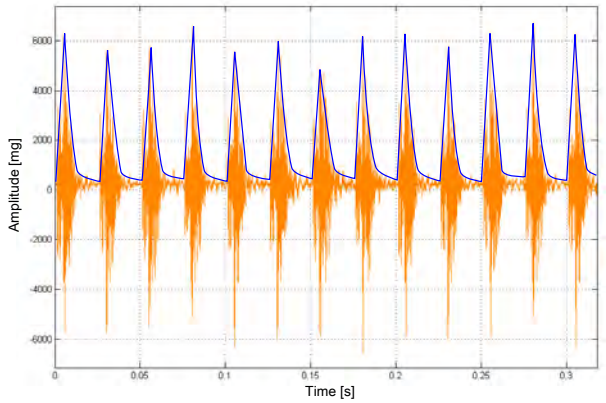


Figure 425: Time signal with envelope

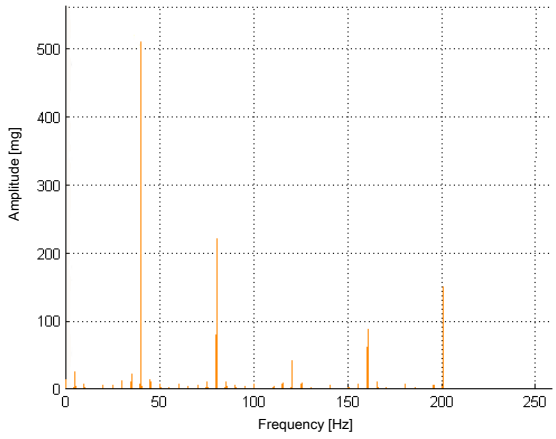


Figure 426: Resulting frequency spectrum

Displacement, velocity and acceleration

Sensors can record oscillation acceleration, oscillation velocity or oscillation displacement. Regardless of the physical size that the sensor records, the oscillation can be represented as acceleration, velocity or displacement since:

$$s = \int v dt = \iint a dt^2, \text{ or } \qquad a = \frac{dv}{dt} = \frac{d^2 s}{dt^2}$$

Where:

- s = Oscillation displacement
- v = Oscillation velocity
- a = Oscillation acceleration
- t = Time

Acceleration is proportional to the force. In contrast, the velocity is an indication of the energy.

The practical implication is that frequency has an influence when converting from one physical size to another. For a sinusoidal oscillation, the following applies:

$$s = \frac{a}{(2 \cdot \pi \cdot f)^2} \qquad v = \frac{a}{2 \cdot \pi \cdot f}$$

The frequency is in the denominator. As a result, high-frequency signal portions are underestimated when using oscillation velocity in comparison with oscillation acceleration. This effect is squared with the application of oscillation displacement.

Since oscillation velocity is calculated through integration from the oscillation acceleration and oscillation displacement is calculated through integration from the oscillation velocity, the mathematical relationship is easily identifiable.

4.26.4.4.2.3 Determining the limit - Alarm philosophy

A fundamental statement can be made by comparing the characteristic values with predefined limit values.

Characteristic values are calculated from the measured signals, which are representative of the status of the system at the given measurement point.

Norms can be used in part to determine alarm limits. In addition, limits can be set based on the machine's history and the experience of the operator.

Comparison with references and norms

For certain machines and systems, limits are fixed by norms. With the exception of ISO 10816, these give little information for assessing the actual status of the machine.

Manufacturer's limits

A few machine manufacturers give limits for permissible oscillations and other relevant factors for assessing the status of the machine.

These are based partly on calculations as well as the knowledge and experience of the manufacturers of these systems.

The limit values provided by the manufacturer should be used when making assessments.

Operator's limits - Experience-based values

Operators draw on their own experience when assessing the status of the machine. Long-term observation of the characteristic values and the machine's history can provide relevant values based on experience.

The limits ascertained from this can vary significantly from limits set by norms and those prescribed by the manufacturer of the machines.

This assessment is only possible when operators have considerable experience with oscillations in the machine and are in a position to differentiate between positive and negative characteristics.

Measuring the broadband values (see 4.26.4.4.3.1 "Characteristic values" on page 2629) is one well suited way to find limits. Some of the characteristics on which limits depend include:

- The location of the damage
- The location of the sensor
- The speed of the moving parts of the machine
- The load on the machine parts
- Etc.

Assessing the trend

In many cases, not enough is known about the actual behavior of a machine during operation, in particular when there is damage.

To make a reliable statement about its condition, the chronological sequence of the characteristic values (characteristic value trend) must also be used when making the assessment.

In the progression of the trend, the "Normal condition" is the starting point. The reference level (normal level) is the level of the characteristic value as set in the normal condition.

Changes in the trend are observed with the normal condition as the starting point. When there is damage, the relevant characteristic values in each case generally increase, although a decrease can also be an indication of a problem in the system.

In order to assess trends accurately, it is essential that the characteristic values of the oscillations are always recorded under the same operating conditions and always classified in the same way. In particular, the speed and load ratio, where applicable, have a strong effect on the characteristic values. Increases in trends under differing operating conditions cannot necessarily be a sign of a change in the actual condition. In many cases, trend observation can assist in monitoring the condition of the machine and bearings.

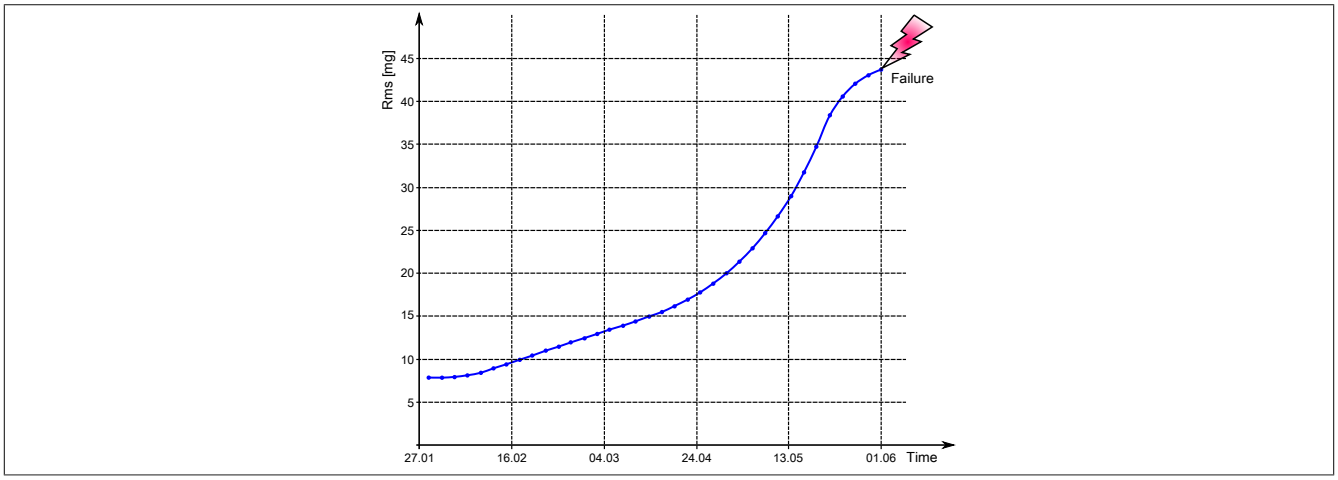


Figure 427: Typical trend progression

The first and second derivatives of the damage progression trend line can provide good information about how badly a component is damaged.

Example

This example will use the first and second derivative to determine the best time for repairs. The maximum service life will be taken into account when selecting a time to perform a replacement. The possibility of lowered production quality is not taken into consideration.

Various times for performing a replacement can be selected by referring to the trend progression.

- k1 = First increase. Very conservative, service life is wasted.
- k2 = Second increase. Good compromise between conservative and optimal.
- k3 = Drop in second derivative. Optimal utilization of service life.

Information:

This example of derivative usage should not be used in your own applications.

First derivative

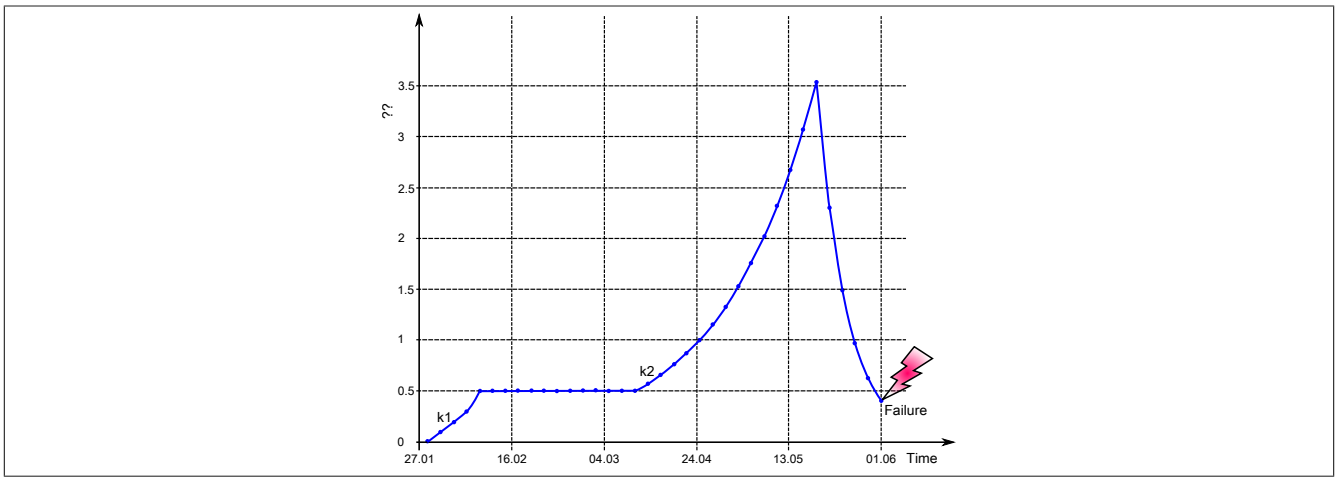


Figure 428: First derivative of the trend progression

Second derivative

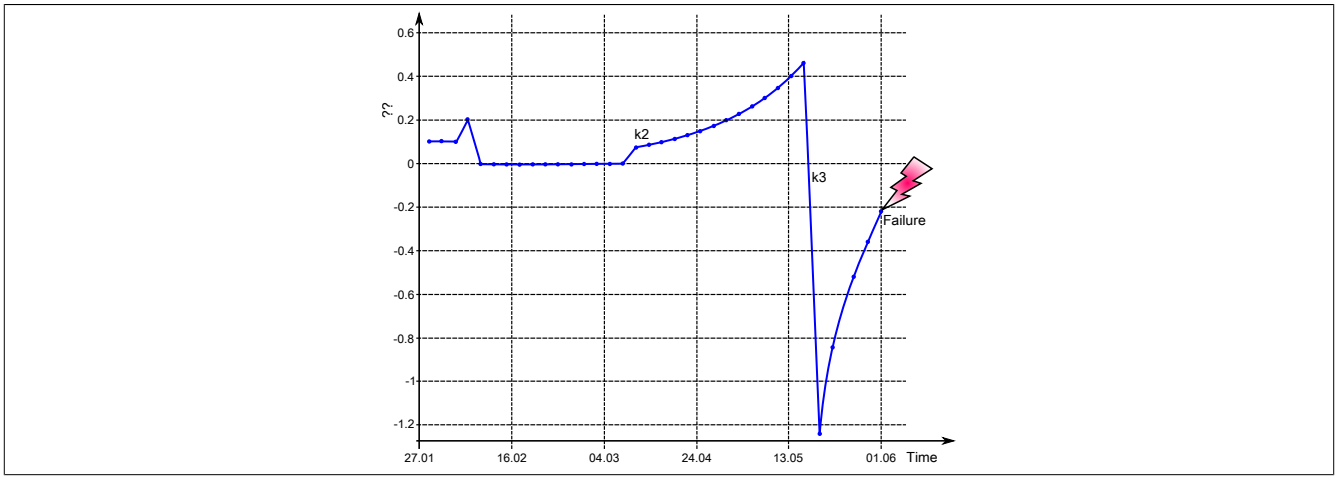


Figure 429: Second derivative of the trend progression

Dynamic speed change

With the FFT calculation in the X20CM4810 module, it is assumed that the lines do not shift during the calculation of a buffer. This is only the case when the system speed is constant.

In the case of dynamic speed, narrow-band frequencies cannot be used to monitor or analyze damaged frequencies since these do not give valid results. The following diagrams show the effect that such a change in speed during an FFT calculation can have.

Example

The speed of a wave changes from 100 Hz to 200 Hz.

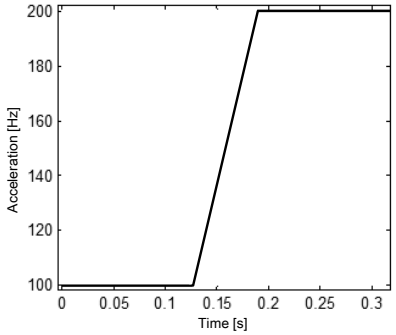


Figure 430: Speed profile

Changing the speed of a wave (within a buffer measuring length, damage is simulated with the speed frequency)

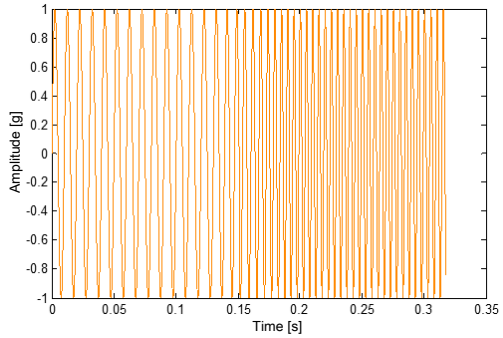


Figure 431: Time signal

Change in the time signal

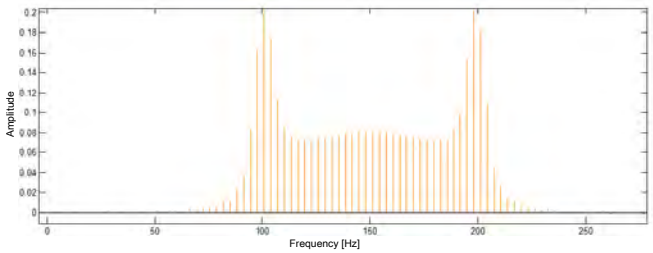


Figure 432: Result in the frequency spectrum

Resulting spectrum calculated from the time signal

Possible approaches to measuring in a dynamic system

- **Best solution:** Adopting separate measurements for trend analysis where the speed can be kept constant for the duration of measuring.
- If a measurement cannot be taken at constant speed, an assessment of the machine condition can be made using the characteristic values or a broadband frequency (in this example, this would be 80 to 220 Hz).

4.26.4.4.3 Practical applications of damage recognition

It is possible to gain good insight into the condition of a machine or system by measuring the parameters associated with errors. This parameter data is used by different algorithms in the module to even calculate the characteristic values. This method of forming characteristic values occurs continually and automatically. It requires little technical knowledge and is easy to use and implement. Damage and flawed conditions can therefore no longer be overlooked.

Selecting suitable characteristic values and assessing them over a longer time frame is the basis for effective and successful monitoring of a machine, a process known as "trending". It enables multiple aggregates to be monitored with a relatively low need for technical measuring and a low demand on staff.

When integrating condition monitoring into automation systems, simply setting basic limits as a warning is not enough. Instead, logical correlations with other parameters such as load or speed, or even the shape of the trend curve, are also required.

Characteristic values are thus gathered and compared with norms or values taken from available experience over a long period of time. This trend progression can be used to make a good assessment of the machine's condition. The trend development of this factor indicates whether the condition is worsening, i.e. if damage is beginning to occur.

Recording the measurement values in a diagram shows the status of the characteristic values at the default warning and alarm thresholds. If these thresholds are exceeded (and only then), oscillation diagnostics gives the cause of the error so that appropriate maintenance measures can be taken.

4.26.4.4.3.1 Characteristic values

The following matrix shows the relationship between potential failures and the suitability of the characteristic values provided in the module. The potential failures refer to the individual application possibilities.

This assessment is based on an estimation of typical applications.

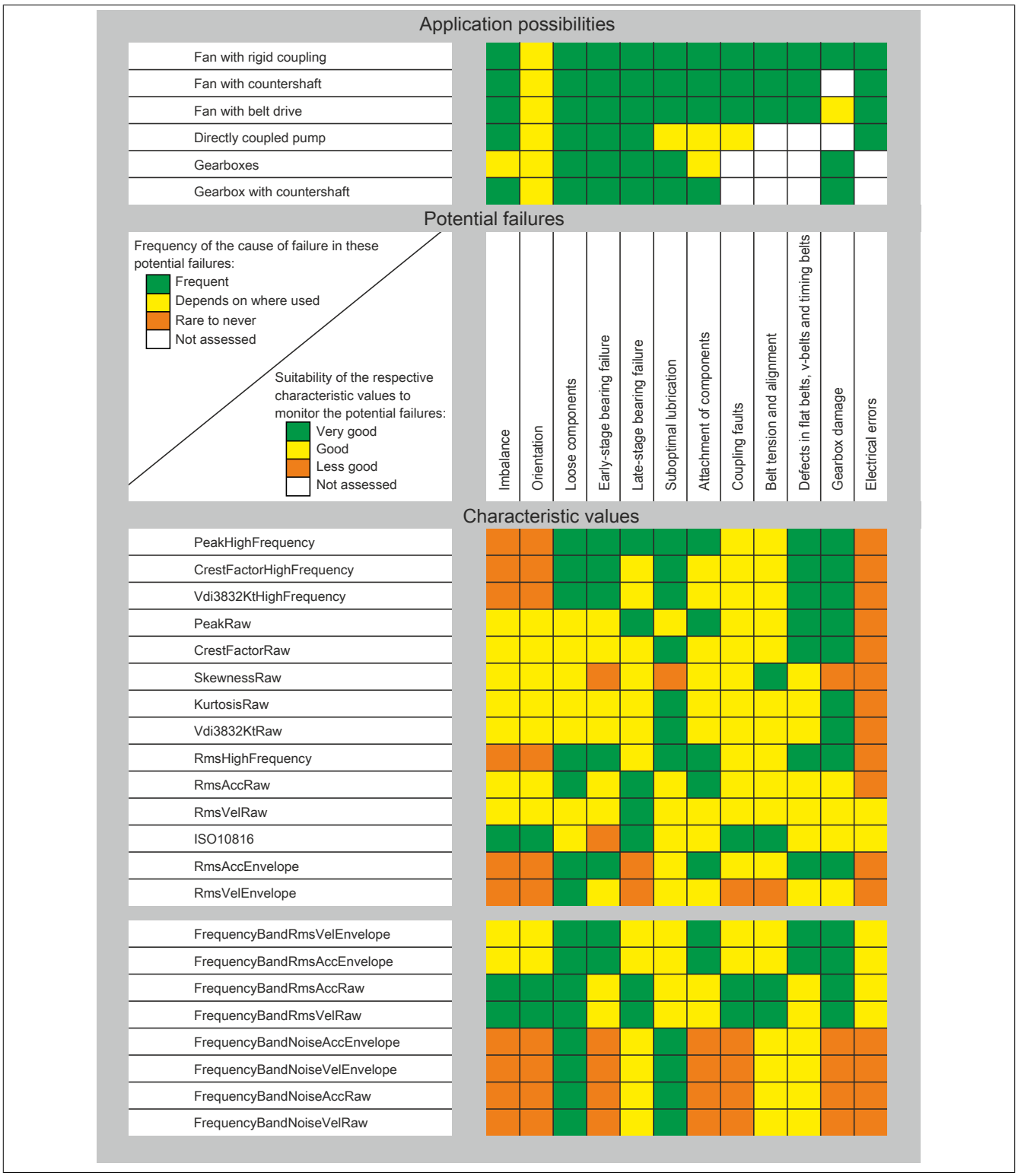


Figure 433: Relationship between potential failures, characteristic values and application possibilities

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Description of individual characteristic values

Sum of maximum value

The maximum value is often also referred to as the peak value.

The peak value of a mechanical oscillation signal indicate the maximum sum of individual impacts that come from the ambient noise. Different types of damage give rise to strong impacts, which show up in the peak value.

PeakHighFrequency

Maximum sum formed from the high-frequency portions of the input signal of the oscillation acceleration in the frequency range between "HighFrequencyConfig01" (500 Hz – 2 kHz) and 10 kHz.

Example: Loose components in the motors

PeakRaw

Maximum sum formed from the raw signal of the oscillation acceleration up until the configured maximum frequency ("MaxFrequencyRaw01") of the channel.

Example: Late-stage bearing damage

RMS value

The RMS value is also known as the quadratic mean, or the root-mean-square. Along with the amplitude, it also takes the energy content of the oscillation into consideration and is the mathematical background for many characteristic values of assessment.

If the RMS is calculated to be above the oscillation velocity, this can be referred to as oscillation speed. In the RMS value, everything contributing to the oscillation is added up. The high oscillation amplitudes of an imbalance are the same as the low oscillation level of bearing damage that is just beginning to occur.

If the RMS value is measured broadly, changes in individual elements contributing to the oscillation can be masked by the message. Early and reliable detection of damage, e.g. due to defects in roller bearings, is only conditionally possible.

ISO10816

The RMS value from the raw signal of the oscillation velocity in a frequency range from 10 Hz to 1 kHz according to ISO 10816.

This broad characteristic value is often used in the assessment of the machine condition since assessment limits are specified for this characteristic value in the standard. These depend on the type of machine and type of installation (rigid or non-rigid). The characteristic value limits for a pre-warning or a warning are given according to their defined classification.

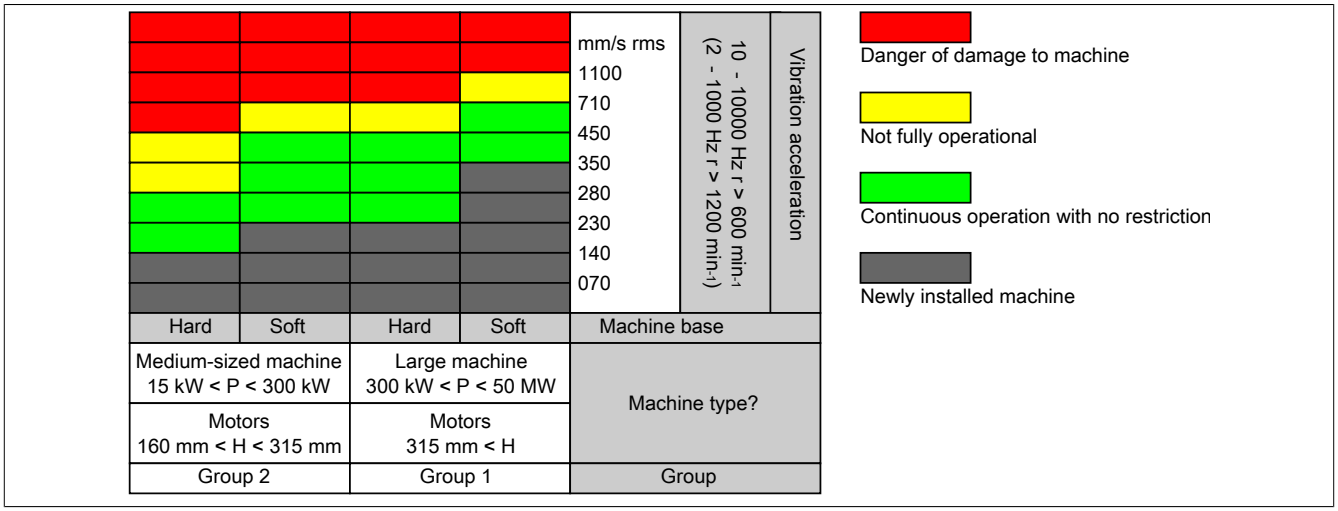


Figure 434: DIN assessment scheme

If the machine condition is in order, this characteristic value is low. If damage occurs, then this value increases severely. If the RMS is assessed in the range of the oscillation velocity, lower frequency portions such as drive speed (and associated imbalance and/or misalignment) that are emphasized more and reflected more heavily in the characteristic value.

Example: Wave imbalance

RmsAccEnvelope

The RMS value formed from the envelope signal of the oscillation acceleration from the configured minimum frequency ("MinFrequencyEnvelope01") to the maximum frequency ("MaxFrequencyEnvelope01") of the channel.

Example: Impact of components on fans

RmsAccRaw

The RMS value formed from the raw signal of the oscillation acceleration from the configured minimum frequency ("MinFrequencyRaw01") to the maximum frequency ("MaxFrequencyRaw01") of the respective channel.

Example: Loose components in pumps

RmsHighFrequency

The RMS value formed from the high-frequency portions of the input signal of the oscillation acceleration in the frequency range between "HighFrequencyConfig01" (500 Hz – 2 kHz) and 10 kHz.

Example: Early-stage bearing damage to electric motors

RmsRaw

The RMS formed from the raw signal of the oscillation acceleration up until the configured maximum frequency ("MaxFrequencyRaw01") of the respective channel.

Example: Loose components in pumps

RmsVelEnvelope

The RMS value formed from the envelope signal of the oscillation acceleration from the configured minimum frequency ("MinFrequencyEnvelope01") to the maximum frequency ("MaxFrequencyEnvelope01") of the channel.

This characteristic value is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

Example: Loose components in gears

RmsVelRaw

The RMS value formed from the raw signal of the oscillation velocity from the configured minimum frequency ("MinFrequencyRaw01") to the maximum frequency ("MaxFrequencyRaw01") of the respective channel.

This characteristic value is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

Example: Late stage bearing damage to fans

Crest factor

The crest factor is defined as a the quotient derived from the peak value and the RMS value. In a sinusoidal oscillation, this factor amounts to √2. This value is also known in electrical engineering as the crest factor.

In a bearing that is operating normally, the factor is also approximately the sum of √2 of the crest factor. If the condition of the bearing deteriorates, individual impacts affect the peak value and consequently raise the crest factor. If pronounced defects are then compounded by overall wear, the RMS value in increased further. In the worst case, the crest factor can remained unchanged or even sink again, even despite increasing damage.

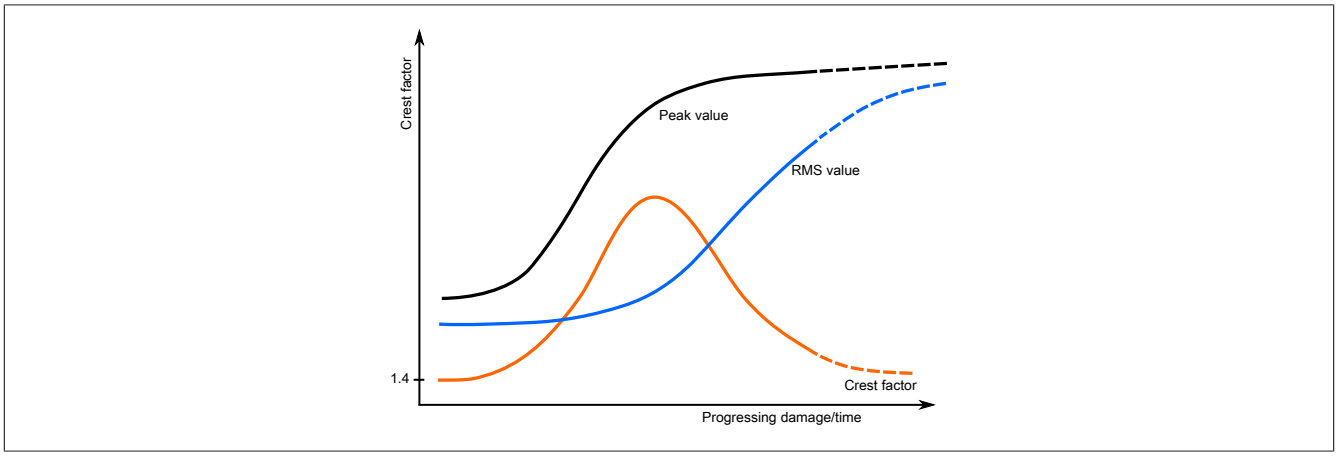


Figure 435: Relationship between the RMS value and peak value

Information:

When a recording of the crest factor is made, the peak and RMS values should also be recorded

CrestFactorHighFrequency

This crest factor is the ratio of the maximum amount to the RMS value formed from the high-frequency portions of the input signal ("PeakHighFrequency" and "RmsHighFrequency") of the oscillation acceleration in the frequency range between "HighFrequencyConfig01" (500 Hz – 2 kHz) and 10 kHz.

Example: Early stage bearing damage to pumps

CrestFactorRaw

This crest factor is the ratio of the maximum amount to the RMS value formed from the raw signal of the oscillation acceleration to the configured maximum frequency ("MaxFrequencyRaw01") of the respective channel.

Example: Notification of suboptimal lubrication of gears

K(t) value

The K(t) is described in the VDI 3832 guideline and is calculated from the RMS value and the peak value of a broadband time signal of the oscillation acceleration.

This ratio correlates to the reference values. The reference values should be measured by the operator shortly after the running-in time. These values can be classified as "System OK" and are therefore the initial values.

The K(t) value decreases with progressive wear. This allows it to be classified into three groups:

- Undamaged
- Early damage
- Pronounced damage

The advantage of the K(t) value is that does not change much, even when damage is severe.

$$K(t) = \frac{a_{RMS}(0) \cdot a_p(0)}{a_{RMS}(t): \; a_p(t):}$$

The following applies:

Formula symbols	Description	Characteristic value in the module
$a_{rms}(0)$	RMS value of the reference value	RmsHighFrequencyRef01-04 RmsRawRef
$a_p(0)$	Maximum value of the reference value	PeakHighFrequencyRef PeakRawRef
$a_{rms}(t)$	Current RMS value	RmsHighFrequency RmsRaw
$a_p(t)$	Current maximum value	PeakHighFrequency ReakRaw

Example

Possible progression of the (K/t) characteristic value

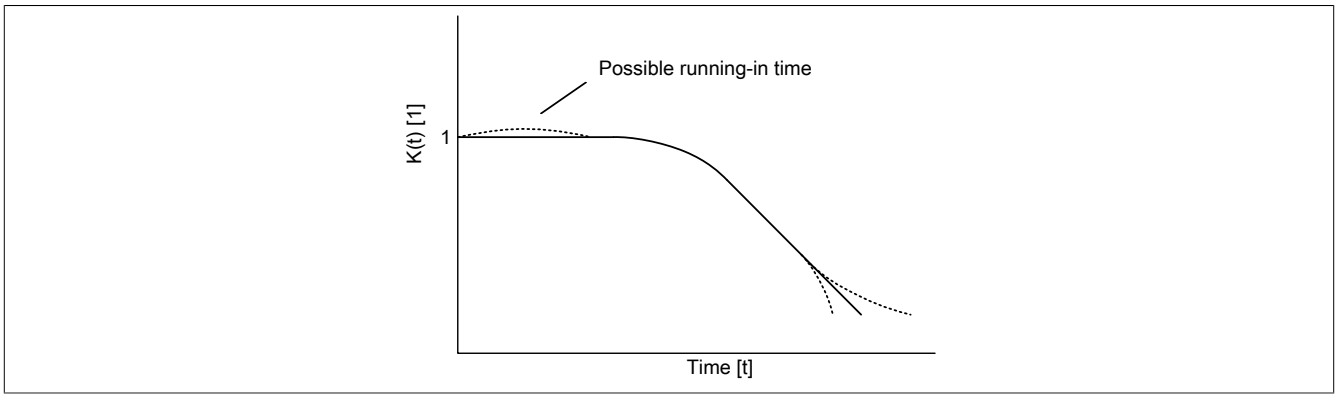


Figure 436: K(t) value progression

Vdi3832KtHighFrequency

K(t) value according to the VDI 3832 guideline formed from the high-frequency portions of the input signal ("PeakHighFrequency" and "RmsHighFrequency") of the oscillation acceleration in the frequency range between "HighFrequencyConfig01" (500 Hz – 2 kHz) and 10 kHz.

Example: Gear damage

Vdi3832KtRaw

K(t) value according to the VDI 3832 guideline formed from the raw signal of the oscillation acceleration up to the configured maximum frequency ("MaxFrequencyRaw01") of the respective channel.

Example: Suboptimal lubrication of electric motors

Kurtosis

Kurtosis is an effective characteristic value for assessing the number of peaks in a signal. Kurtosis (peakedness, fourth statistical moment) is defined as the ratio of two statistical characteristic values/processes.

Kurtosis is a type of weighted "Crest factor". The signal peaks are valued higher than the "signal noise" (also called the carpet value) due to the fourth power of the integral. Not only is the RMS value also used, but the entire signal progression as well. This increases the informational value of this characteristic value.

Information:

Kurtosis is standardized at zero in the X20CM4810 module.

A kurtosis factor of less than two is typical of a machine in good condition.

KurtosisRaw

The kurtosis factor formed from the raw signal of the oscillation acceleration up until the configured maximum frequency ("MaxFrequencyRaw01") of the respective channel.

Example: Suboptimal lubrication of fans

Skewness factor

The skewness factor (skewness, third statistical moment) specifies the degree of a signal's asymmetry in reference to its standard distribution. The lower the skewness, the more evenly distributed the signal. A signal with a high skewness factor has a much larger amplitude in the assessment range.

A symmetrically distributed signal has a skewness factor of 0. Depending on the direction of the slant, the skewness can be positive or negative. A considerable slant means approximately a skewness factor of ±1.

A large kurtosis factor combined with a large skewness factor indicates electrostatic discharge.

SkewnessRaw

Skewness factor formed from the raw signal of the oscillation acceleration up until the configured maximum frequency ("MaxFrequencyRaw01") of the channel.

Example: Determining the belt tension and belt alignment in flat belts and V-belts

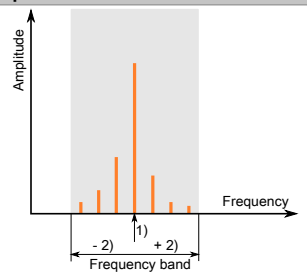
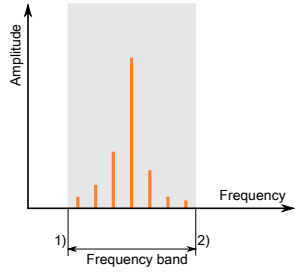
Description of frequency bands

For the early detection of damage and problems, it is often useful to monitor individual frequency bands. A selective RMS value can be used as the characteristic value for these frequency bands.

Possibilities:

- "Broadband RMS"
- "Speed-dependent RMS"
- "Noise"

Up to 32 different frequency bands can be defined. The center frequency and the frequency intervals are defined in terms of the upper and lower limits. It is important to note that the format varies slightly depending on the configuration (see section 4.26.4.2.11 "Characteristic value format" on page 2602).

Speed-dependent RMS	
	Frequency broadband is formed from the speed frequency ± the frequency interval. 1) Speed frequency: "FrequencyBandxxDmgFreq60Rpm" * "ActSpeed" 2) Frequency interval: "FrequencyBandxxTolerance"
Non speed-dependent RMS	
	Frequency bandwidth is formed of the lower and upper frequency band limits. 1) Lower frequency band limit: "FrequencyBandxxLowerFrequency" 2) Upper frequency band limit: "FrequencyBandxxUpperFrequency"

Restricting the frequency range allows certain errors to be identified easily.

One example of this is imbalance. This is clearly shown by an increase in the frequency line for speed. Forming a selective characteristic value for the speed frequency can thus improve classification.

Selective characteristic values can also be formed for RMS values formed from the envelope.

Damage to the outer ring is shown more clearly in the increase of the frequency known as the bearing damage frequency. Damage to the outer ring is shown in the increase of the component of the outer ring damage frequency.

This bearing damage frequency is generally available from the bearing manufacturer.

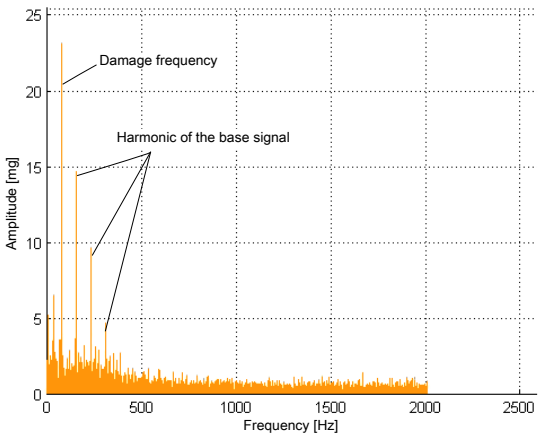


Figure 437: Selective characteristic value for outer ring damage

Bearing damage on the outer ring can be found early by the parameters of a characteristic value with a frequency range that encompasses the damage frequency.

If frequencies are entered that are outside the minimum and maximum signal frequency for the selected channel, then only the domains between the minimum and maximum frequency will be analyzed.

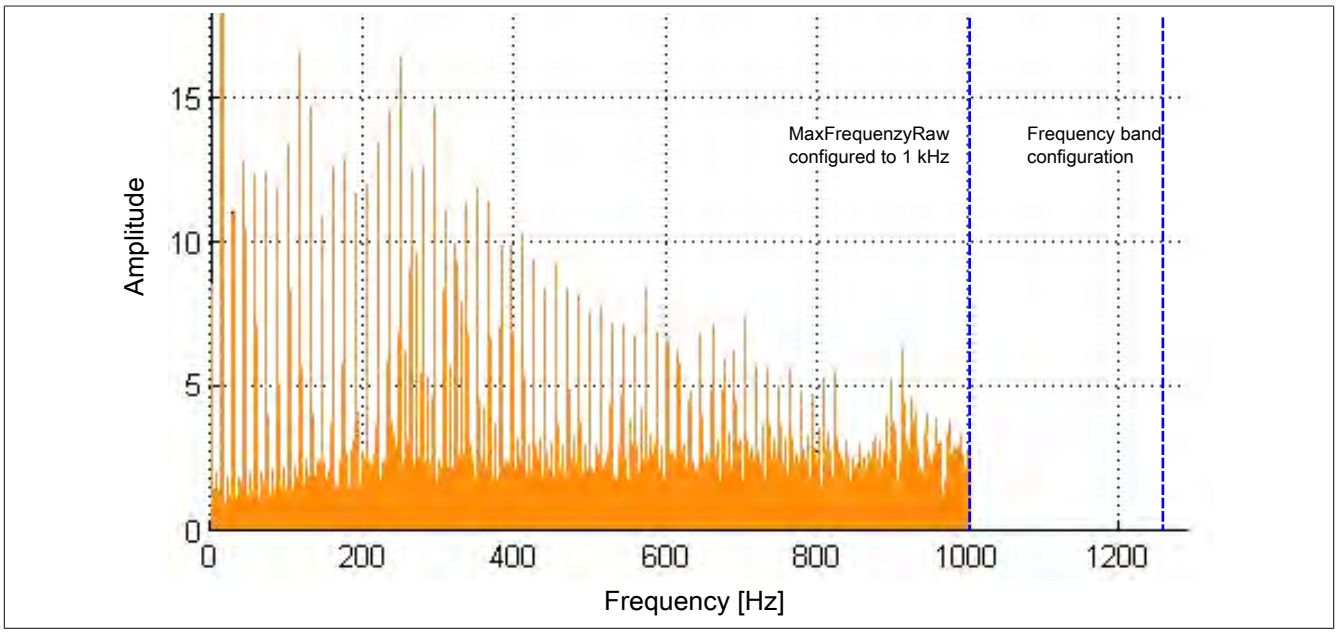


Figure 438: Restricting the frequency band evaluation

Two neighboring lines (samples) in the spectrum that are already outside the set window (one above and one below the window) will be partially included in the calculation depending on their distance from the window.

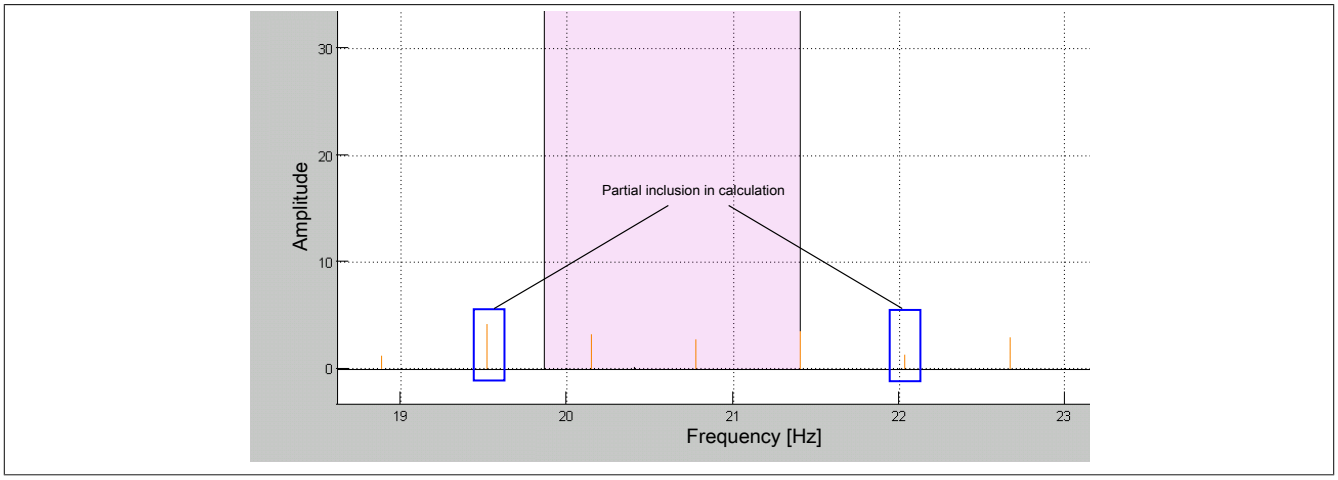


Figure 439: Partial inclusion of marginal lines in the calculation

Guidelines for configuring the frequency bands

- The total range of the frequency band is at least 2 * 0.005 * max. drive frequency [Hz].
- The upper and lower frequency limits must not be less than 0.005 * max. drive frequency [Hz] from the desired average frequency.
  Example
  At a maximum drive frequency of 50 Hz, a frequency band should be set at 10 Hz.
  10 Hz ± (0.005 * 50 Hz) = At least 9.75 Hz lower and 10.25 Hz upper frequency band limits
- Depending on the MaxFrequency selected, a least three lines should be configured within each frequency band.
- The first lines to the left and right of the configured frequency band are included proportionally based on their distance from the frequency band (see image above).

Broadband RMS

In this configuration, the RMS value of the configured signal and channel in the frequency band is calculated. The value is calculated from the minimum frequency ("FrequencyBandXXLowerFrequency") to the maximum frequency ("FrequencyBandXXUpperFrequency"). The minimum and maximum frequency can be entered here in increments of 0.25 Hz.

Any channel for any frequency band can be selected.

The following signals can be selected for each channel:

- Raw acceleration signal
- Raw velocity signal. Equal to 0 if the speed calculation is disabled.
- Enveloped acceleration signal
- Enveloped velocity signal. Equal to 0 if the speed calculation is disabled.

The harmonic frequencies (whole number multiples) of the window can also be included in the calculation. Here, the width of the window is simply retained and the mean frequency of the window is multiplied (by 1, 2, 3, etc.) until the maximum frequency of the configured signal and channel is reached.

Speed-dependent RMS

In this configuration, the RMS value is calculated in a movable window. There are 4 speed inputs for this ("ActSpeed01-04" in 0.01 Hz). One of the 4 speeds can be selected for each of the 32 frequency bands. In addition, the standardized damage frequency at 60 rpm ("FrequencyBandXXDmgFreq60rpm") and a tolerance ("FrequencyBandXXTolerance") must be configured. These can be configured separately for each frequency band.

The window in which the RMS is calculated is determined as follows:

Minimum frequency = (speed * standardized damage frequency at 60 rpm) – tolerance

Maximum frequency = (speed * standardized damage frequency at 60 rpm) + tolerance

The standardized damage frequency and tolerance can be entered here in increments of 0.01 Hz.

The following signals can be selected for each channel:

- Raw acceleration signal
- Raw velocity signal. Equal to 0 if the speed calculation is disabled.
- Enveloped acceleration signal
- Enveloped velocity signal. Equal to 0 if the speed calculation is disabled.

The harmonic frequencies (whole number multiples) of the window can also be included in the calculation. Here, the width of the window is simply retained and the mean frequency of the window is multiplied (by *1, *2, *3, etc.) until the maximum frequency of the set signal and channel is reached.

Useful information

If a fixed frequency band is needed in which the minimum frequency ("FrequencyBandXXLowerFrequency") and maximum frequency ("FrequencyBandXXUpperFrequency") must be set with a higher precision than 0.25 Hz, then a speed-dependent frequency band with a fixed speed can be used.

Noise

In this configuration, the noise from a quadrant of the respective signal on the selected channel that is within the frequency band is calculated.

To do this, the configured maximum frequency of the signal on the selected channel is divided by 4. This results in 4 quadrants. A configuration can then be used to select one of the 4 quadrants in which the noise should be determined.

The following signals can be selected for each channel:

- Raw acceleration signal
- Raw velocity signal. Equal to 0 if the speed calculation is disabled.
- Enveloped acceleration signal
- Enveloped velocity signal. Equal to 0 if the speed calculation is disabled.

This configuration allows slippage to be effectively measured, for example. The higher the friction, the more noise that is created.

Configuration options

Each of the 32 frequency bands can be configured to one of the following characteristic values.

FrequencyBandRmsVelEnvelope

The RMS value formed from the envelope signal of the oscillation acceleration in a freely selectable frequency range.

This frequency band is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

Example: Defects in toothed belts

FrequencyBandRmsAccEnvelope

The RMS value formed from the envelope signal of the oscillation acceleration in a freely selectable frequency range.

Example: Gear damage

FrequencyBandNoiseAccRaw

The noise value formed from the envelope signal of the oscillation acceleration in a freely selectable frequency range.

Example: Imbalance of toothed belts

FrequencyBandNoiseVelRaw

The noise value formed from the envelope signal of the oscillation acceleration in a freely selectable frequency range.

This frequency band is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

Example: Imbalance of toothed belts

FrequencyBandNoiseAccEnvelope

The noise value formed from the envelope signal of the oscillation acceleration in a freely selectable frequency range.

Example: Imbalance of toothed belts

FrequencyBandNoiseVelEnvelope

The noise value formed from the envelope signal of the oscillation acceleration in a freely selectable frequency range.

This frequency band is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

Example: Imbalance of toothed belts

FrequencyBandNoiseAccRaw

The noise value formed from the envelope signal of the oscillation acceleration in a freely selectable frequency range.

Example: Imbalance of toothed belts

FrequencyBandRmsVelRaw

The RMS value formed from the raw signal of the oscillation velocity in a freely selectable frequency range.

This frequency band is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

Example: Imbalance of toothed belts

4.26.4.4.3.2 Potential failures

The direct effect on the oscillation behavior is dependent on the type and extent of damage. For this reason, it must be assessed individually.

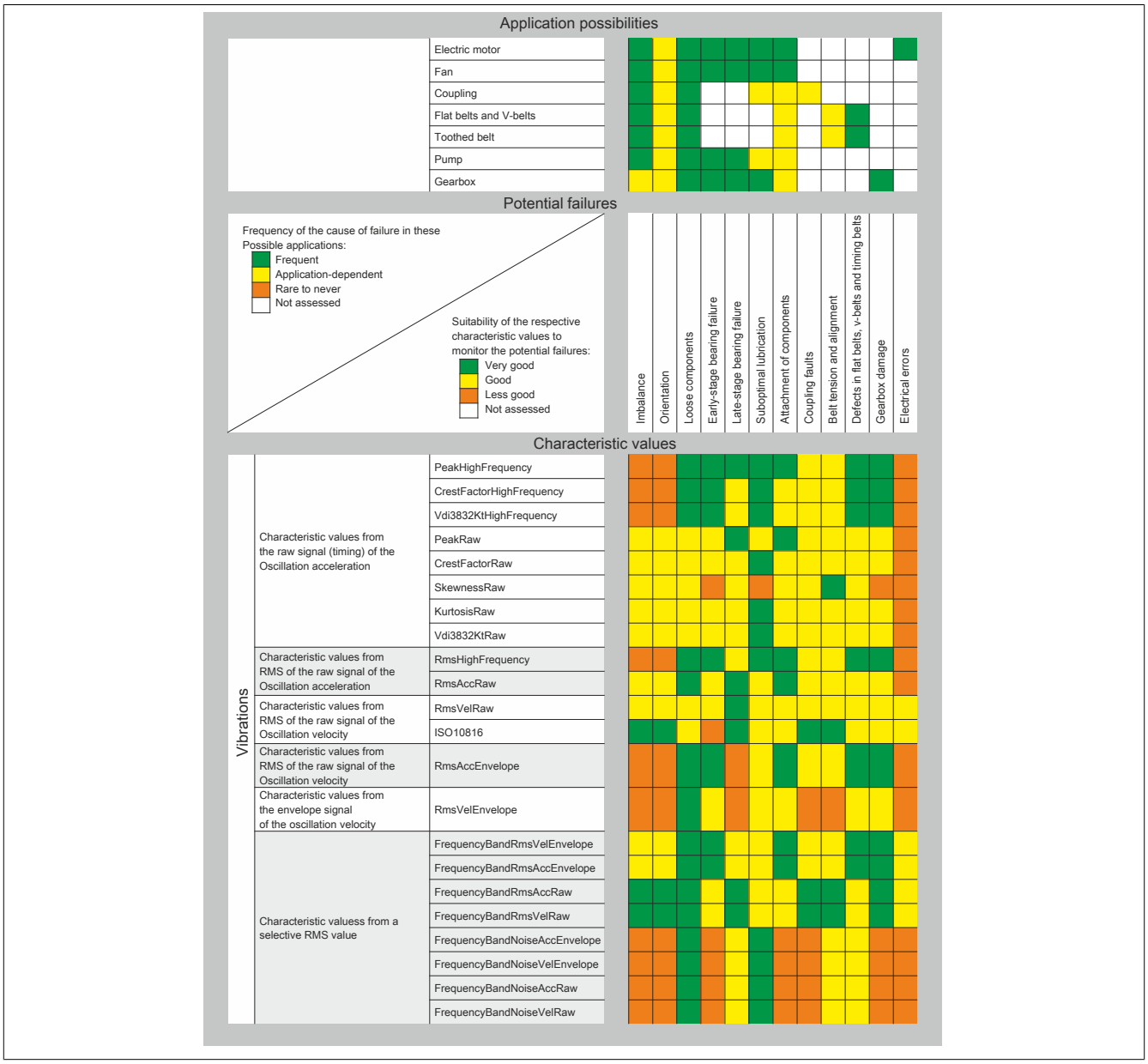


Figure 440: Overview of application possibilities, characteristic values and potential failures

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Imbalance

The term imbalance refers to rotating bodies with a mass that is not rotationally symmetrical. In other words, the center is not on the axis of rotation

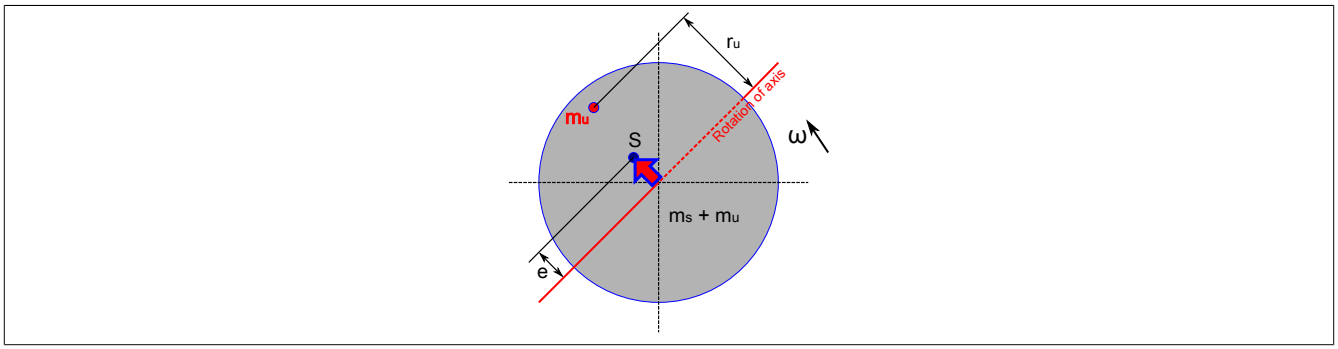


Figure 441: Representative sketch of an imbalance

Imbalance leads to vibrations and increased wear, particularly at high speeds, which is why counterweights are applied to compensate for this as counterbalance. In practice, it is never possible to fully compensate for this, meaning each rotating body always has residual imbalance.

The centrifugal force caused by imbalance is dependent on the square speed and thus has a more significant effect at higher speeds (higher speed frequency). On a spectrum, therefore, the frequency line denoting speed is significantly higher.

Failure mode	Frequency in the raw signal spectrum	Frequency in the envelope spectrum	Comment
Imbalance	1 x fn	-	Only severe imbalance causes peaks in the speed that show up in the envelope spectrum.

Table 595: Frequency of imbalance

fn ... Nominal speed

The X20CM4810 module can only measure the intensity of the imbalance, not its position on the wave. For this reason, it cannot be used for balancing.

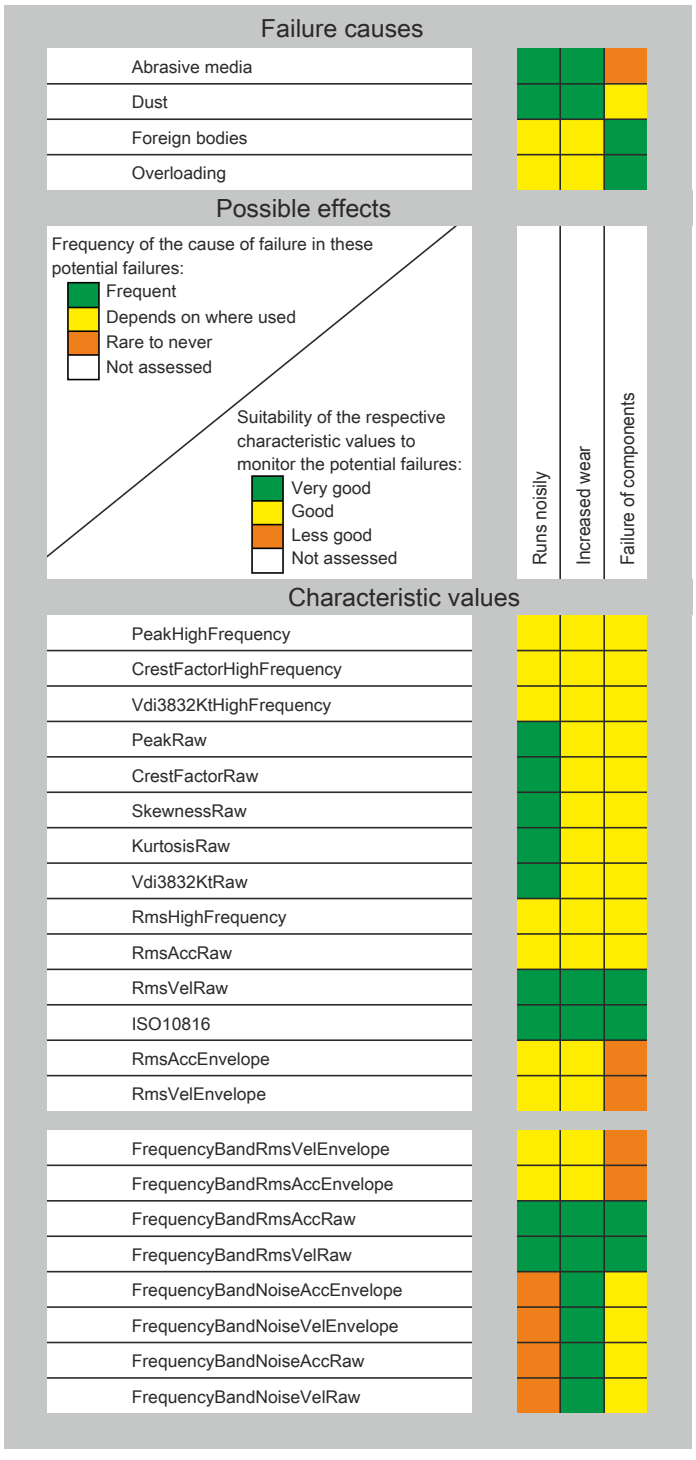


Figure 442: Failure causes and effects of imbalance

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Misalignment

During operation, a number of different factors can cause machine parts to fail to align or stop aligning with each other.

Shafts should rotate around a linear axis at the coupling positions, so that the restoring forces at the coupling position and the loading forces in the bearings are kept as low as possible. Misalignment causes increased vibrations and wear.

Misalignment usually consists of a parallel and an angular misalignment. In the event of a severe parallel misalignment, the frequency portions increase sharply at twice the speed.

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Misalignment in coupling	1 x fn, 2 x fn (sometimes 3 x fn, 4 x fn)	-	With a parallel misalignment, usually only "1 x fn" occurs.

Table 596: Frequency of misalignment

fn ... Nominal speed

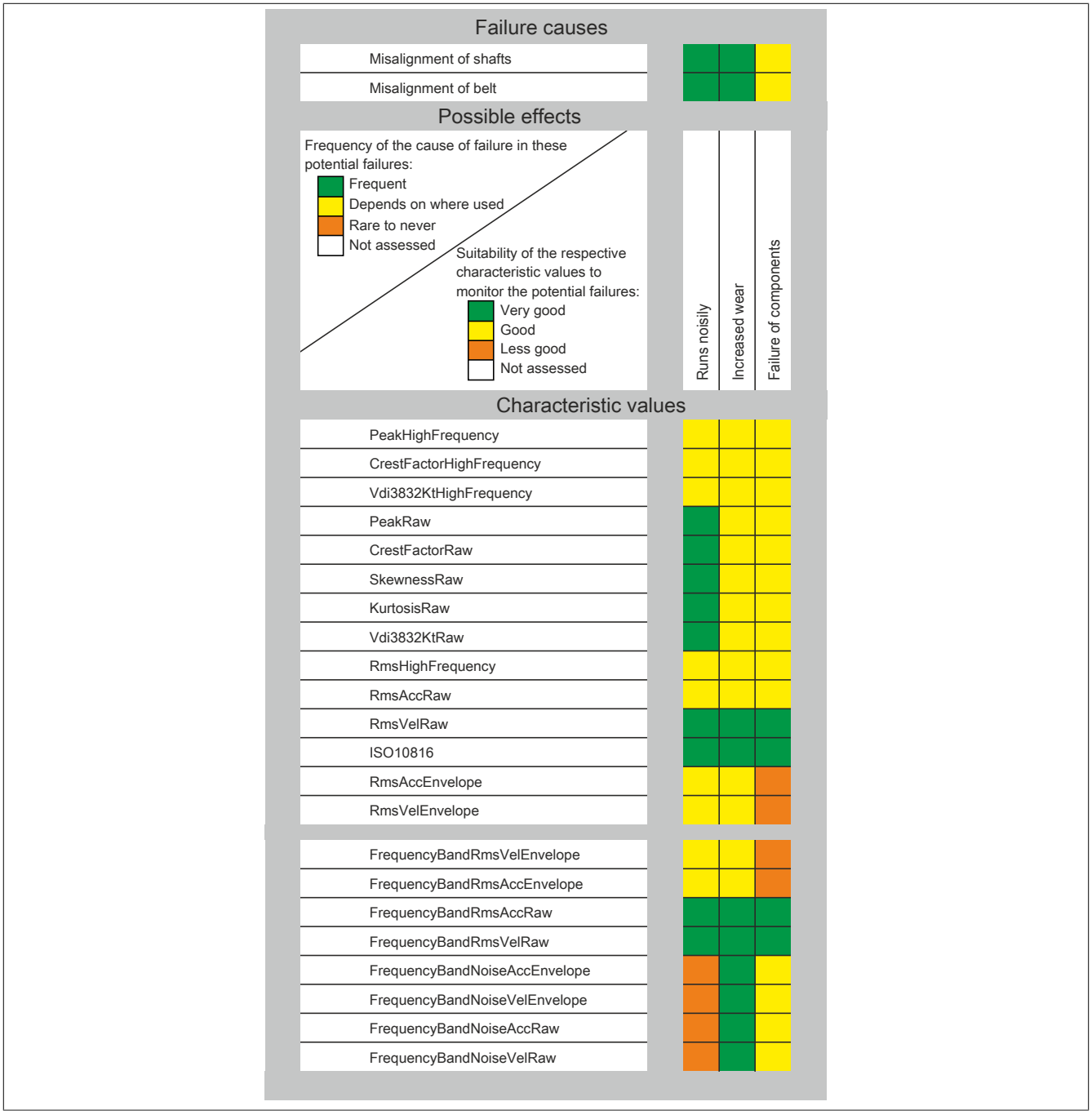


Figure 443: Failure causes and effects of an alignment failure

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Belt damage

Belts often cause various problems during operation. A belt can be damaged if the tension is too low or too high or if the belt is incorrectly aligned. If the damaged belt part rolls over the pulley, this causes impacts that can be measured.

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Defective belt	1 x fr, 2 x fr, 3 x fr ...	1 x fn1, 1 x fn2, 1 x fr	Belt frequencies usually occur in both spectra.

Table 597: Frequency of failure indicators on belt drives

fr ... Belt drive speed
fn1 ...
fn2 ...

Poorly aligned or incorrectly tensioned belts can also cause severe stress on the bearing points. The increased vibration also causes heavier wear on belts and pulleys.

The vibrations are clearly identifiable at the bearing points.

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Misalignment of belt	1 x fn, 2 x fn 1 x fr	1 x fn	If the belts strike against the pulley laterally, impacts can also occur with speed and belt frequency.

Table 598: Frequency of failure indicators on poorly aligned belt drives

fn ... Nominal speed
fr ... Belt drive speed

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Toothed belt damage	1 x frn	1 x frn, 1 x fzn	The tooth meshing frequencies in combination with the respective speed are clearly visible.

Table 599: Frequency of failure indicators on poorly aligned timing belts

frn ...
fzn ... Tooth meshing frequency

Flat belts and V-belts

With flat belts and V-belts, torque is transferred between the belt and the pulley through the contact surface. Belt drives are not particularly sensitive to alignment. If the deviation is too high, they can nevertheless cause oscillations to occur and, above all, increase the level of wear and energy consumption.

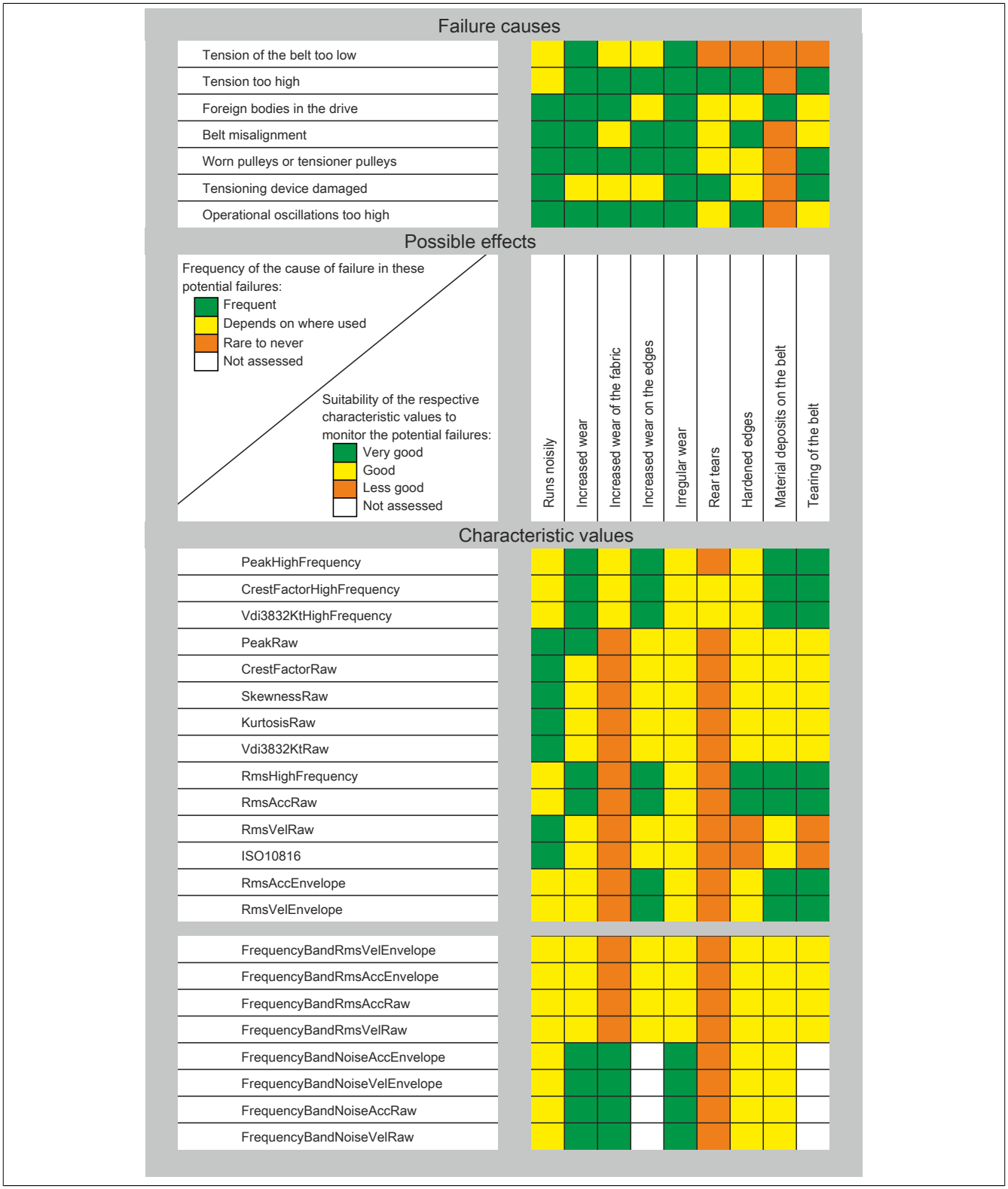


Figure 444: Failure causes and effects of belt damage in flat belts and V-belts

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Toothed belt

With toothed belts, torque is transferred via the meshing of the teeth. In addition to the already known failure causes, there are also the failures caused by the toothing.

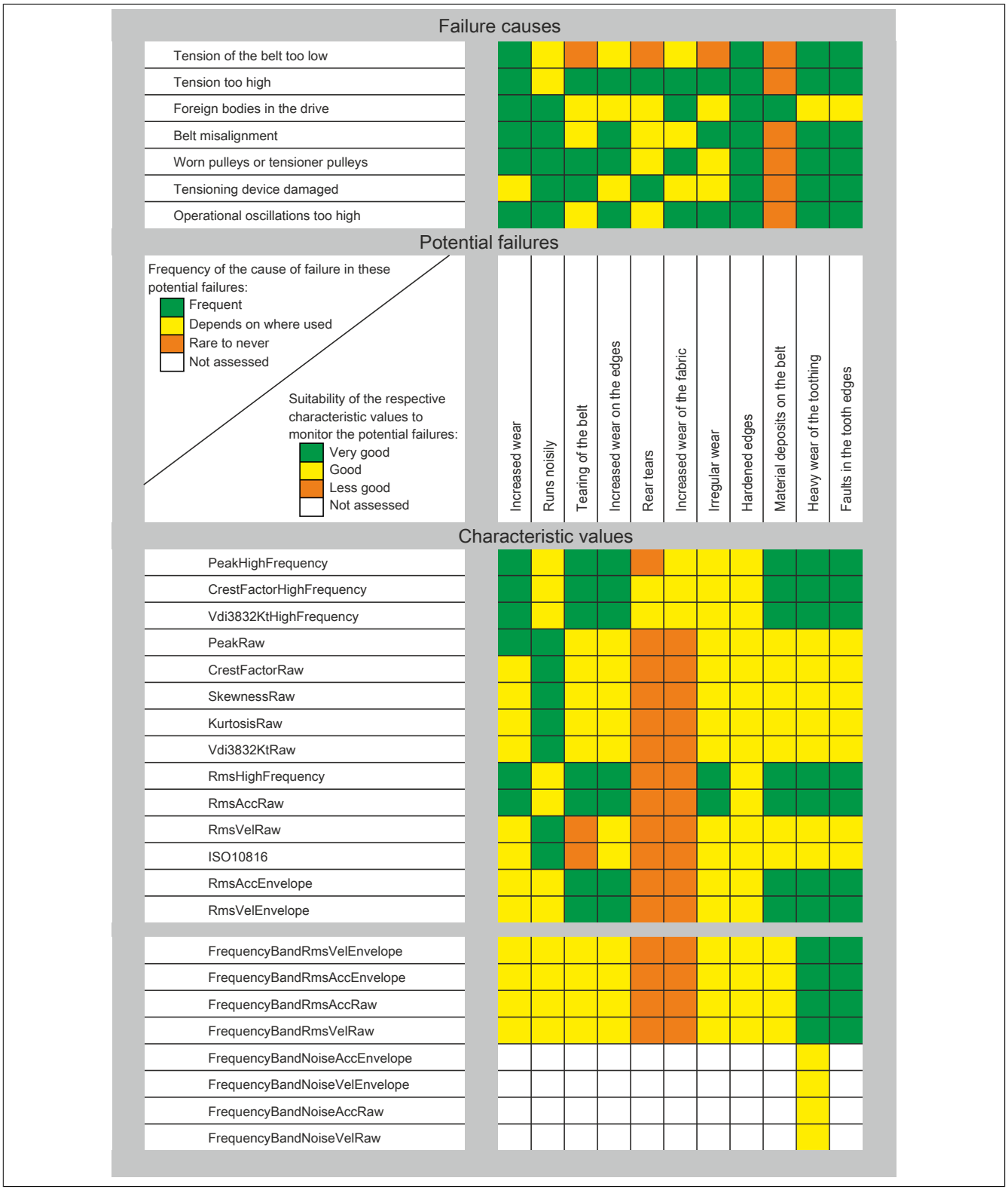


Figure 445: Frequency of failure indicators on toothed belts

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Loose parts, parts striking each other

If individual parts in the machine are loose, they can cause unwanted oscillations. When individual parts strike housings or attachment parts, these appear very similar. As a result, the two causes of damage cannot be analyzed separately.

In addition, components strike their counterparts on each revolution. This in turn causes the attachment parts to vibrate at their natural frequency. Envelope analysis can be used to separate the causes of impact.

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Loose parts, parts striking each other	(1 x fn)	1 x fn	There is usually one strike per revolution. If an envelope occurs for the load, a double frequency can be seen.

Table 600: Frequency of failure indicators for loose or impacting components

fn ... Nominal speed

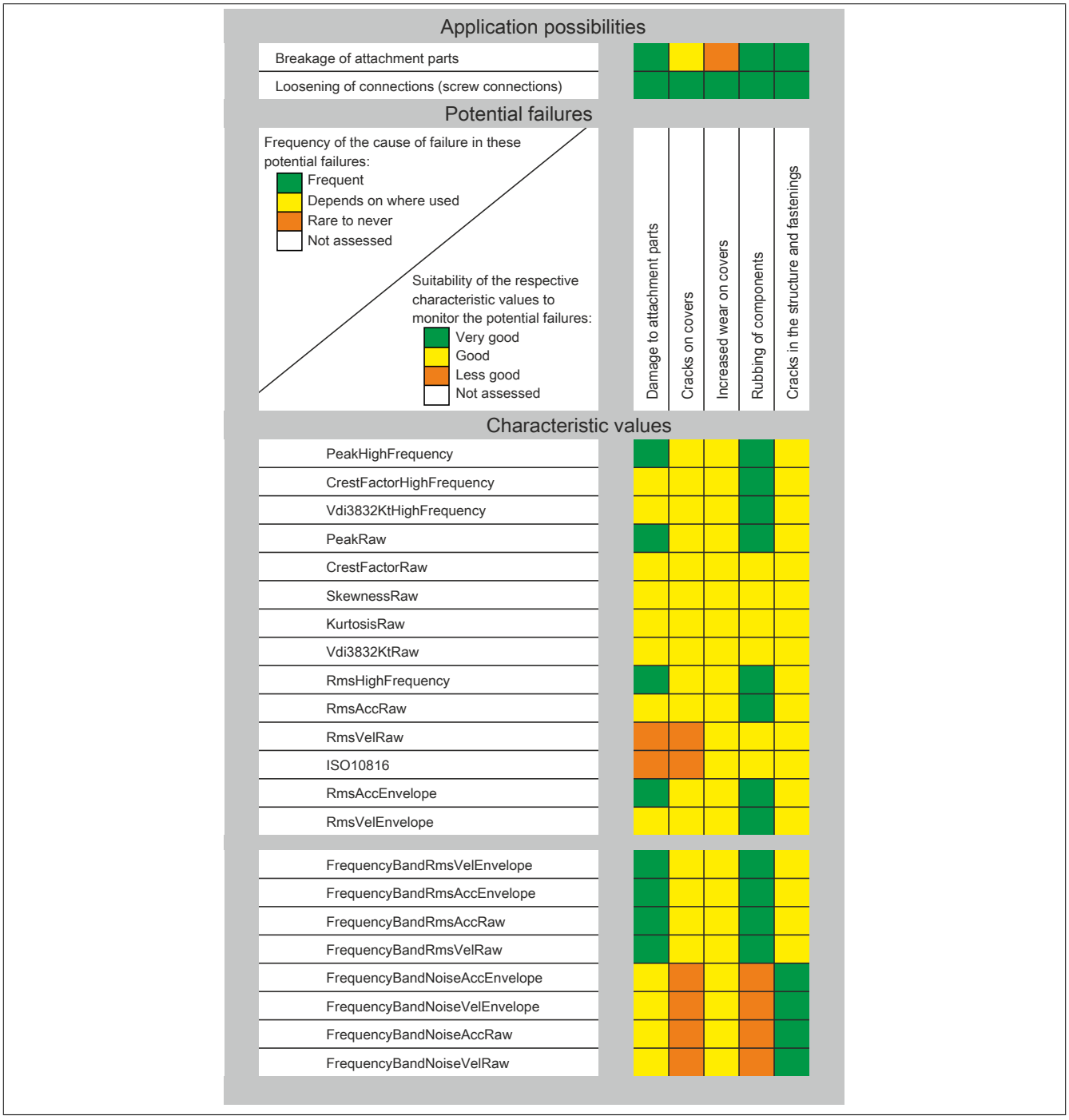


Figure 446: Failure causes and effects of belt damage

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Slide bearing damage

In a structure-borne sound measurement, the typical damage frequencies for a slide bearing do not manifest themselves until a very late stage. For this reason, this method is less suitable for early detection.

Roller bearing damage

Many types of bearing damage are caused by imprecisions in the bearing surface such as material damage or micro-cracks. These pits are rolled over by the roller elements and cause impacts on the roller bearing and its attachment parts.

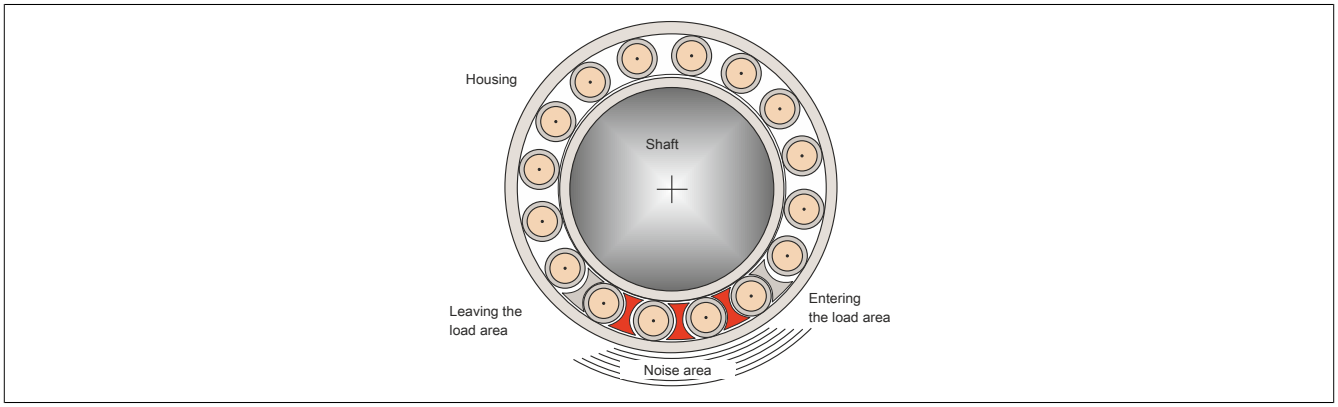


Figure 447: Roll-over processes in the bearing

The mechanism is very similar to the striking of a bell. The clapper strikes the body of the bell, and the bell starts vibrating at its natural frequency.

In the case of the bearing, each time the roller moves over the damaged area it is like the striking of the clapper, and the roller parts and attachment parts start to vibrate.

These very small oscillations can be measured as a modulation or superposition of the excitation frequency on the surface of the bearing.

Appropriate analysis methods such as formation of the envelope can separate the superposition to make the roll-over frequencies of the bearing clearly discernible.

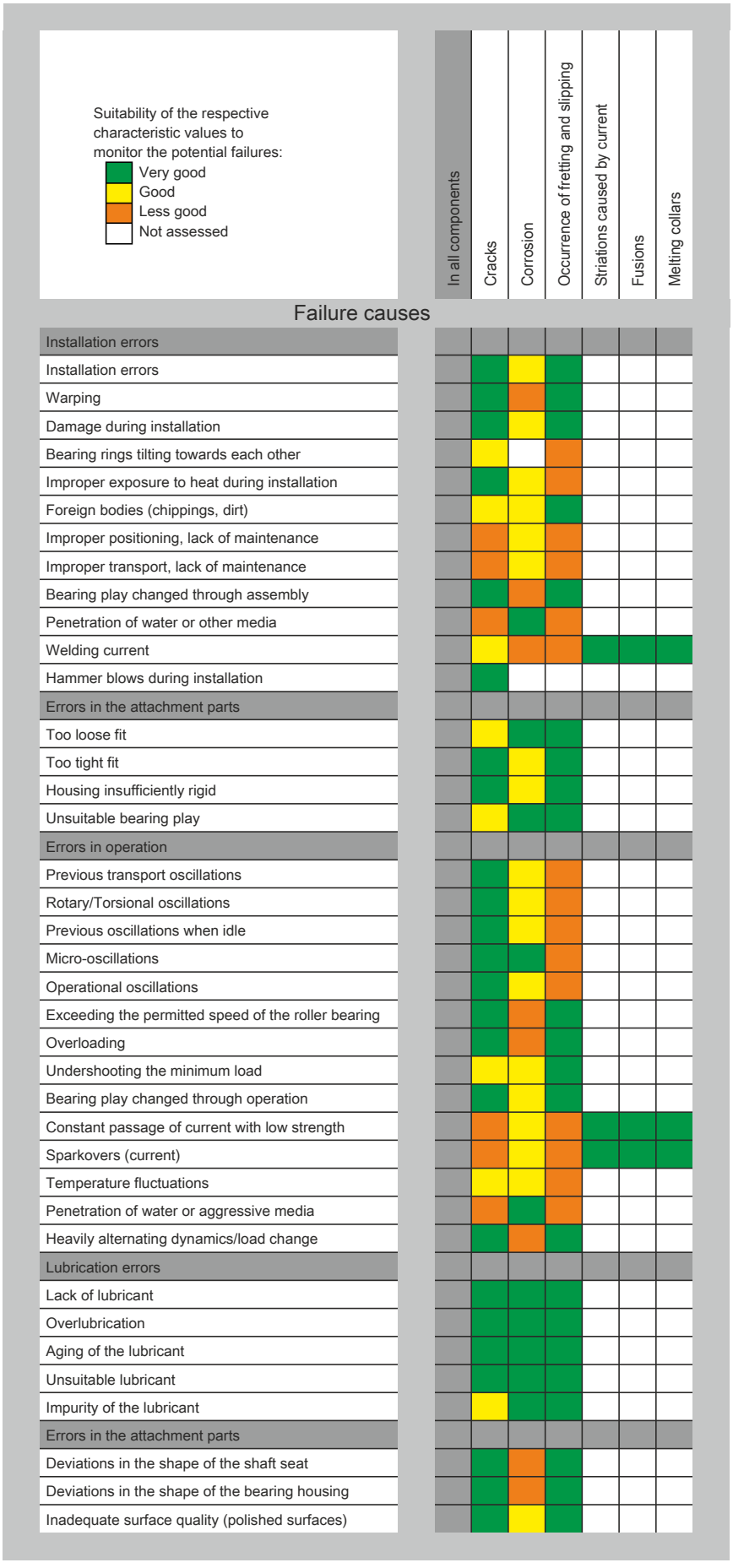


Figure 448: Frequency of failure indicators on roller bearings

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

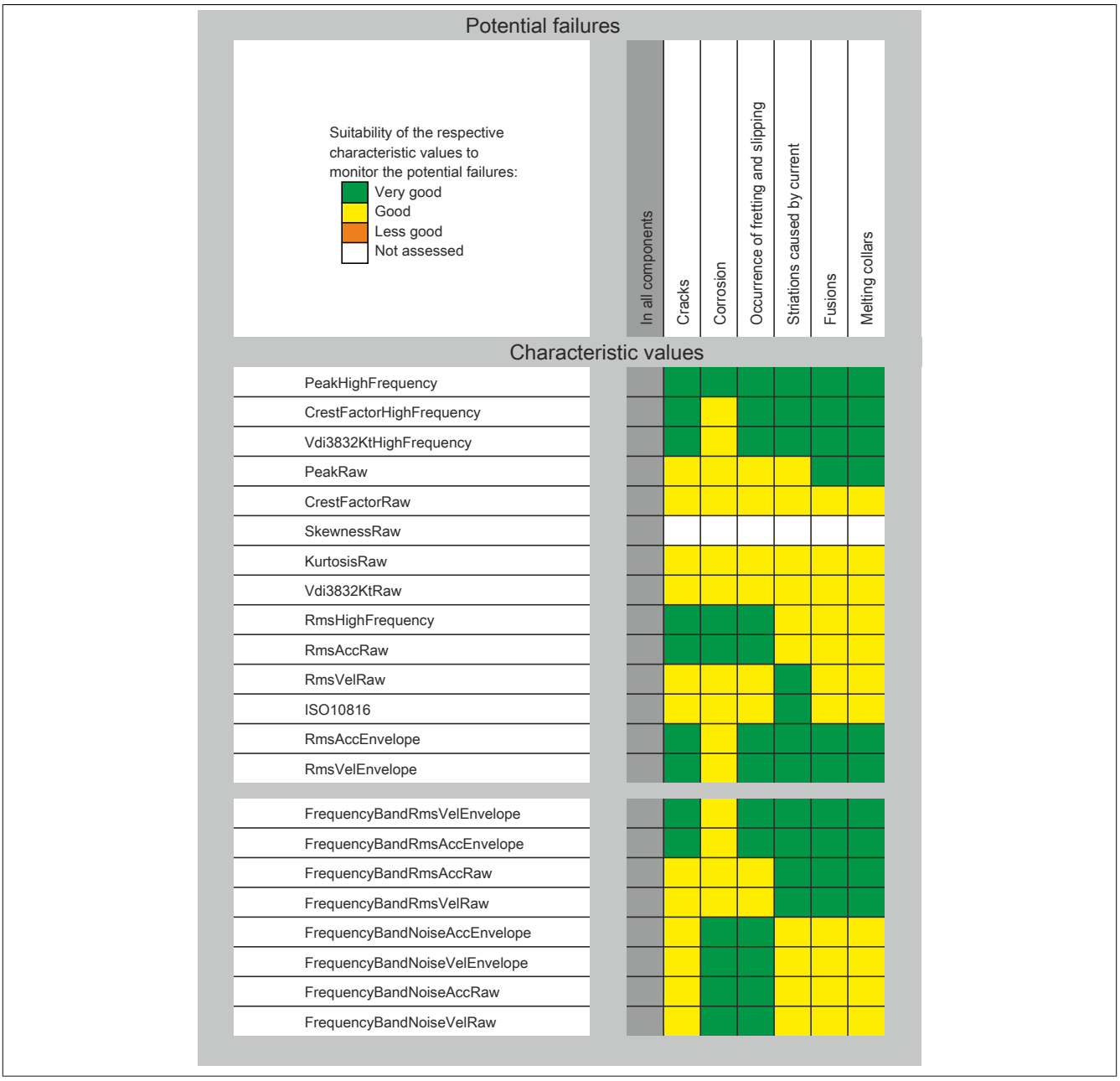


Figure 449: Frequency of failure indicators on roller bearings

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Typical outer and inner ring damage

Outer ring damage

In most cases the outer ring remains stationary while the inner ring turns. This gives a clearly defined fixed load zone. Most damage occurs in this load zone. If pitting or other surface damage forms, vibrations occur when the roller element moves over it that can be measured on the housing components.

Outer ring damage is manifested in the envelope spectrum as follows:

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Outer ring damage	(1 x fa)	1 x fa, 2 x fa, 3 x fa ...	With advanced damage, the outer ring frequencies can also be seen in the raw signal spectrum

Table 601: Frequency of outer ring damage

fa ... Frequency of the outer ring damage

Inner ring damage

Any inner ring damage that occurs travels with the rotating shaft. Due to the different rotary speeds of the revolving roller elements and the inner ring, pronounced modulations occur. As a result, inner ring damage frequencies are usually shown with sidebands in the spectrum.

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Inner ring damage	(1 x fi)	i x fi ± i x fn	Inner ring damage generally appears based on modulation with pronounced sidebands for the speed.

Table 602: Frequency of inner ring damage

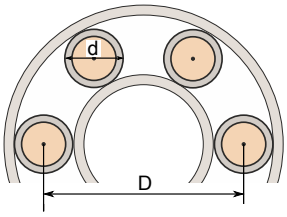
fi ... Frequency of the inner ring damage
fn ... Nominal speed

Calculating damage frequencies

Details of bearing damage frequencies are normally provided by the manufacturer and can be found in the data sheets for the bearings.

They can also be calculated easily using the following values:

N	Speed in rpm
n_b	Number of roller elements
d	Diameter of roller elements
β_c	Pressure angle
D	Roller ring diameter



Formula for calculating the inner ring damage frequency

$$fi = \frac{n_b \cdot N}{2 \cdot 60} \cdot \left[1 + \frac{d}{D} \cdot \cos \beta_c\right]$$

Figure 450: Calculation of the inner ring damage frequency

fi ... Inner ring damage frequency

Formula for calculating the outer ring damage frequency

$$fa = \frac{n_b \cdot N}{2 \cdot 60} \cdot \left[1 - \frac{d}{D} \cdot \cos \beta_c\right]$$

Figure 451: Calculation of the outer ring damage frequency

fa ... Outer ring damage frequency

Formula for calculating the roller element damage frequency

Damage impacting the individual pitch line:

$$few = \frac{1}{2} \cdot \frac{D \cdot N}{d \cdot 60} \cdot \left[1 - \left(\frac{d}{D} \cdot \cos \beta_c\right)^2\right]$$

Figure 452: Calculating the damage frequency on one roller element

few ... Damage frequency of the individual roller element

Damage impacting both pitch lines:

$$f_W = \frac{D \cdot N}{d \cdot 60} \cdot \left[1 - \left(\frac{d}{D} \cdot \cos \beta_c\right)^2\right]$$

Figure 453: Calculating the damage frequency on both roller elements

fw ... Damage frequency of both roller elements

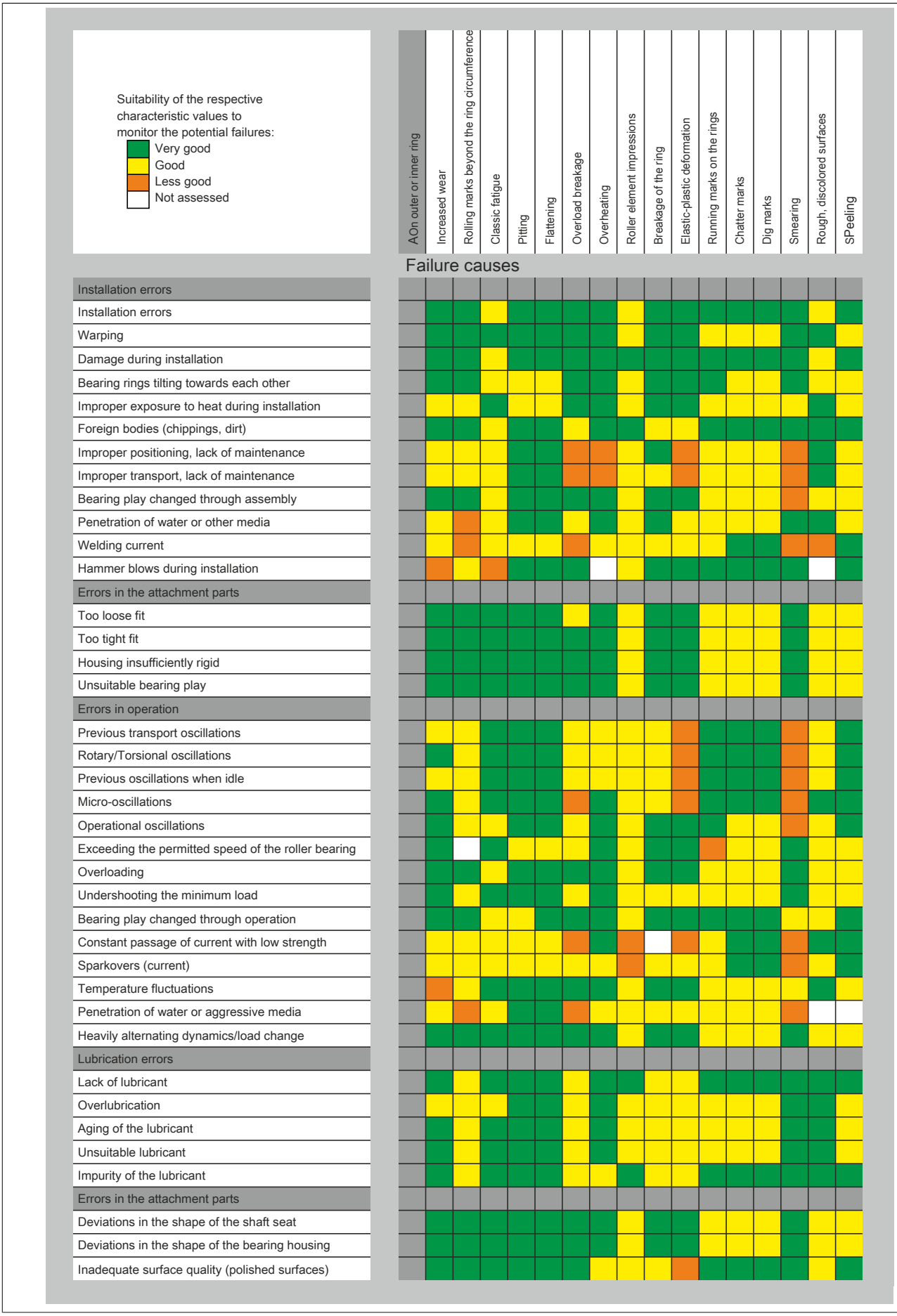


Figure 454: Frequency of failure indicators on roller bearings

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

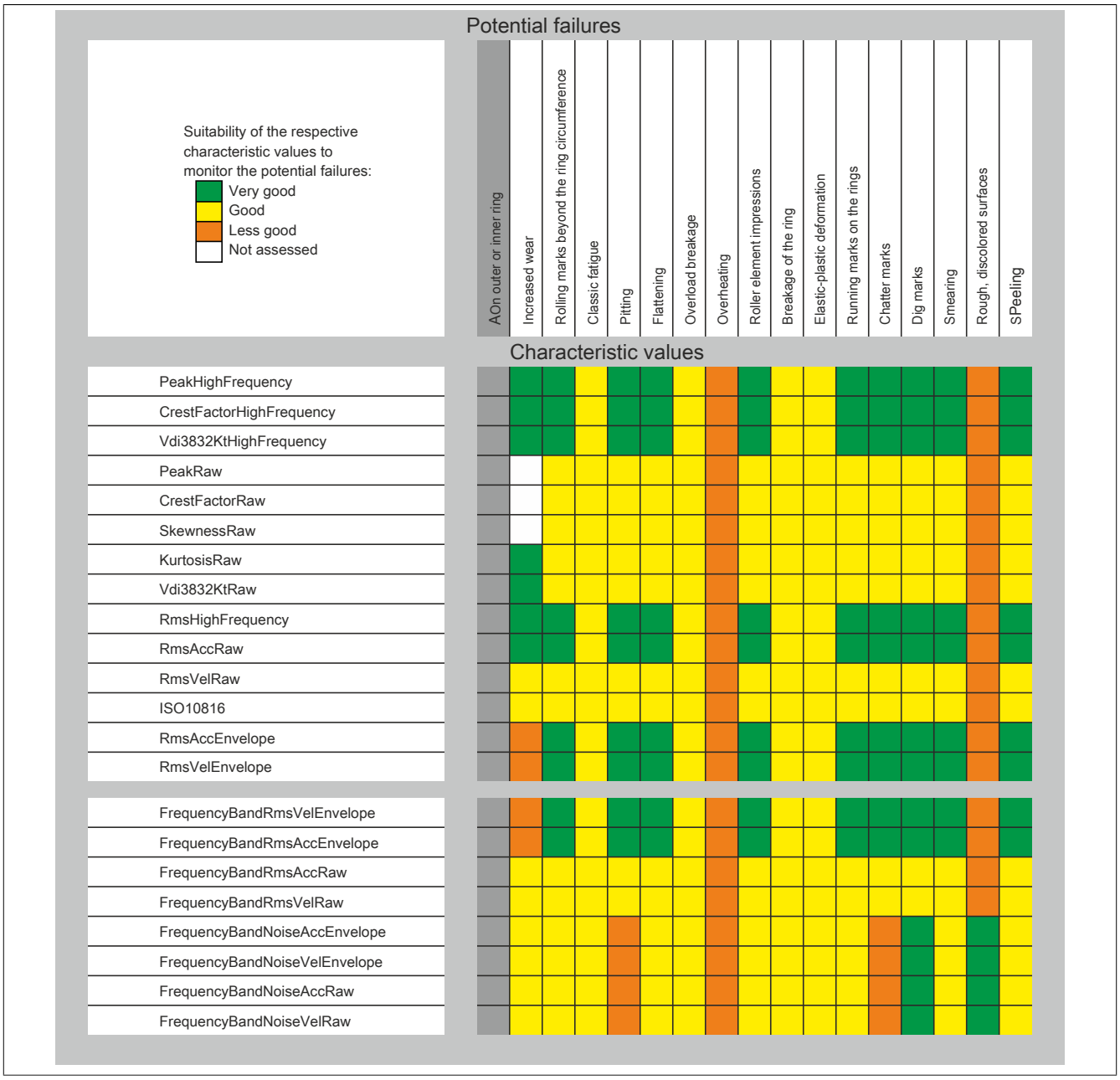


Figure 455: Frequency of failure indicators on roller bearings

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Typical cage and roller element damage

Cage damage

Cage frequencies often occur in electric motors, especially where bearings with increased bearing play are used. If this is not used, oscillation of the cage often occurs, which is evidenced by increased running noise.

Roller element damage

Roller element damage without outer or inner ring damage is extremely rare. The individual indicators are therefore listed for example purposes only.

If the roller element is damaged, an impact occurs either on the inner ring, outer ring, or both. Roller element damage can therefore be detected by the roll-over frequency or double the roll-over frequency. For this reason, the harmonic should be included in the characteristic value calculation where possible to detect roller element damage.

For the failure mode, see "Typical outer and inner ring damage" on page 2650

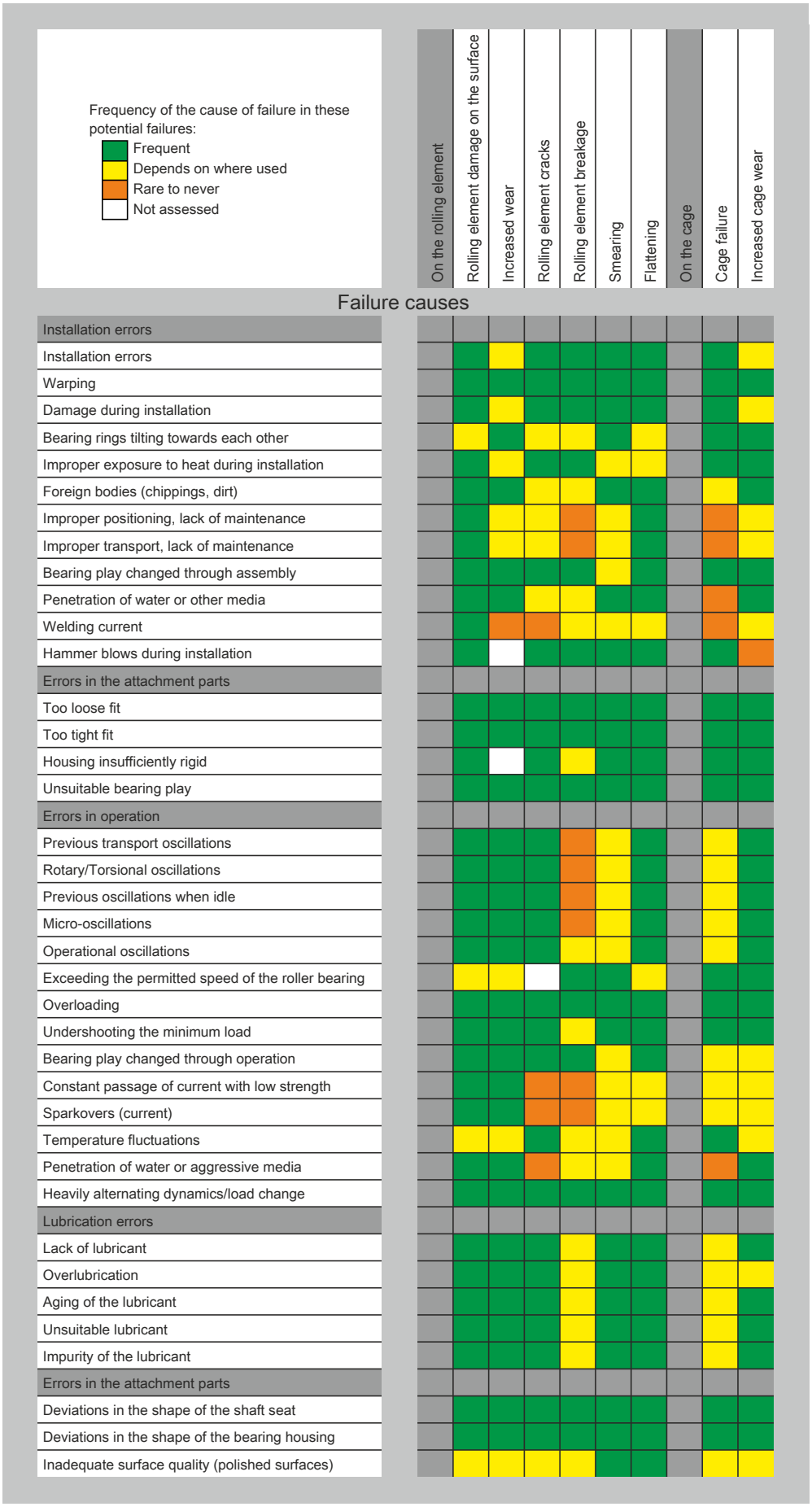


Figure 456: Frequency of failure indicators on roller bearings

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

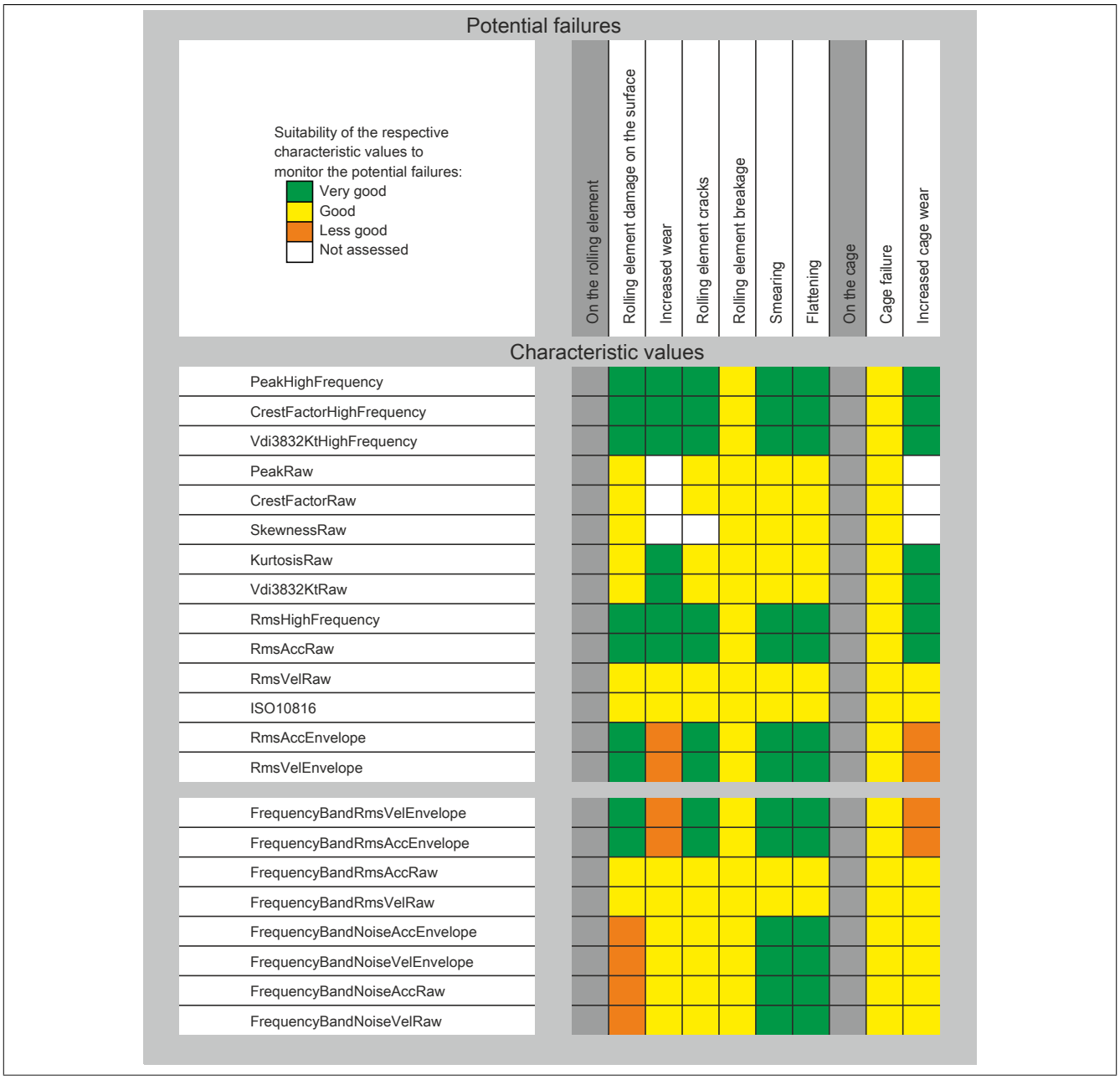


Figure 457: Frequency of failure indicators on roller bearings

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Gear damage

DIN 3979 provides a description of gear errors and defects. The most common errors in individual gearboxes are described below.

The complexity of the machine dynamics must be taken into consideration in individual applications.

Translation: The conversion of the speed ratio must always be considered in relation to the gear ratio. The frequencies on the gearwheels are always based on the speed of the respective axis.

Manufacturing defects

Oscillations due to manufacturing always occur in a gearbox. Typical manufacturing defects are pitch errors, profile deviations, concentricity and spacing errors.

Depending on the gearwheel pairing, these individual defects can intensify or become less intense depending on how the defects affect each other. The interplay of the individual defects is also responsible for the overall oscillation behavior.

Pitch error is a frequently occurring defect and is used as an example here. Depending on whether the pitch error is positive or negative, it is intensified or compensated by an existing load. The effects on the oscillation behavior depend very much on the rigidity of the gearwheel. If there is a pitch error, a shock occurs that can be measured effectively.

In addition to pitch errors, all form and dimensional gear errors lead to oscillations.

Outer ring damage is manifested in the envelope spectrum as follows:

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Meshing frequencies	1 x fz	1 x fz	Gear frequencies depend on the respective geometric ratios of the wheels but can be precisely calculated in any case.

Table 603: Frequency of a typical toothing error

fz ... Tooth meshing frequency

Defects caused by wear

If form and dimensional deviations occur during operation, observing the trend can lead to an appropriate level of confidence when performing diagnostics.

Failure mode	Frequency in raw signal spectrum	Frequency in envelope spectrum	Comment
Deterioration	1 x fz	1 x fz ± i x fn	Geometric errors increasingly appear additionally with sidebands for the tooth meshing frequency.

Table 604: Frequency of defects caused by wear

fz ... Tooth meshing frequency
fn ... Nominal speed

Wobbling

If the toothed belt axis and the rotation axis are not parallel, the phenomenon called wobbling occurs. This causes two flank errors per revolution. Depending on the position, there is one transmission on the inner edge and one on the outer edge of the toothed wheel.

The doubled speed frequency is clearly evident in the frequency spectrum.

Failure mode	Frequency in the raw signal spectrum	Frequency in the envelope spectrum	Comment
Wobbling	1 x fn, 2 x fn	1 x fz, 2 x fz	Wobbling movements manifest as doubled speed frequency and are usually accompanied by sidebands.

Table 605: Frequency of a typical toothing error

fn ... Nominal speed
fz ... Tooth meshing frequency

Cyclic running errors and axial distance errors

In DIN 3960, axial distance errors are defined as a deviation between the target/actual value.

An error in the distance between the axes causes a change in the contact of both toothed wheels. The so-called overlap ratio is negatively affected.

Even small pitch errors lead to a noise increase in the gearbox. Superposition with the previously mentioned errors often cause a frequency to form with various different frequency portions. Interpretation must be checked on a case-by-case basis

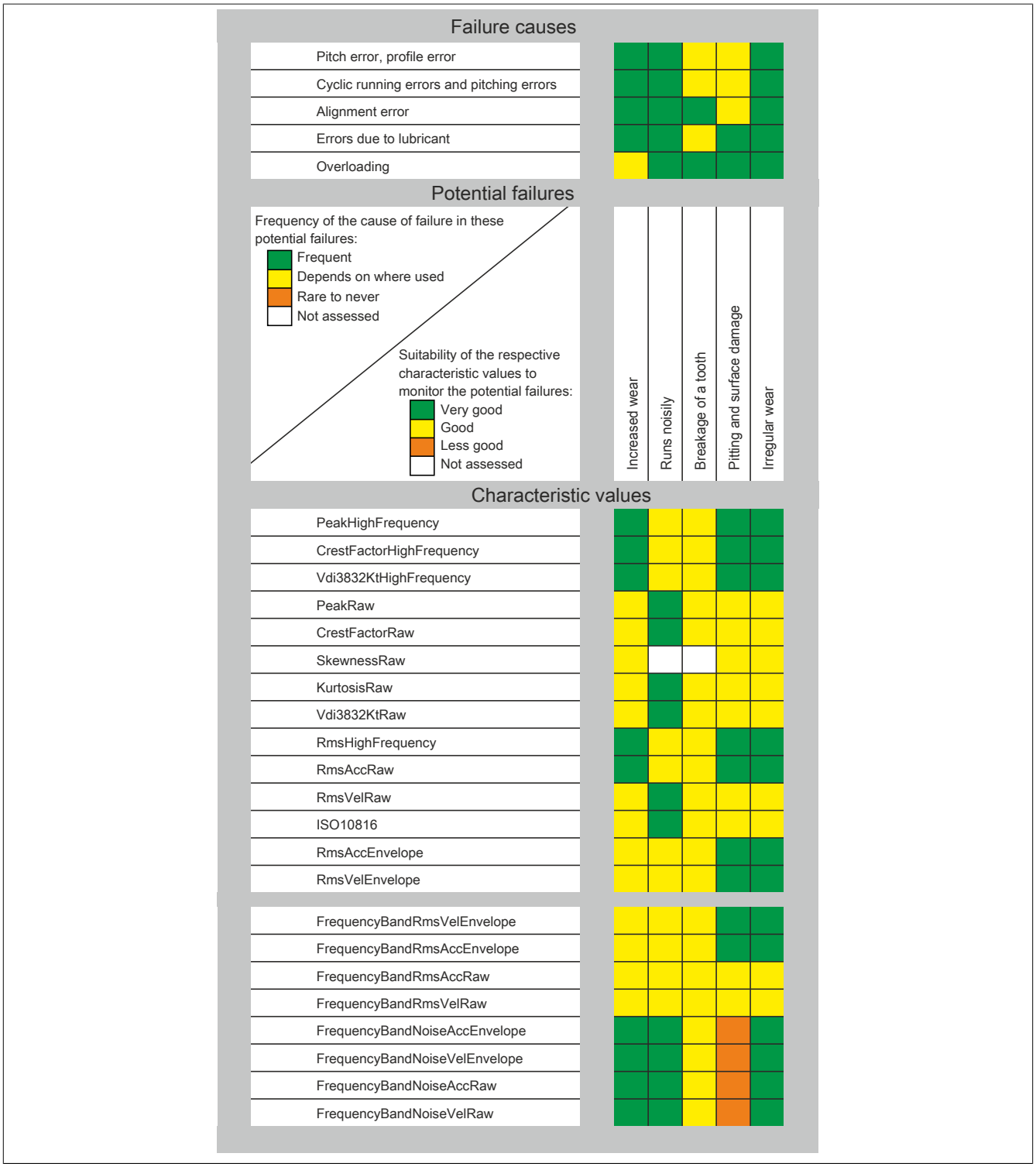


Figure 458: Frequency of failure indicators for gearbox damage

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Electrical errors

Occasionally, bridges in the rotor bars or short circuit rings occur. They occur as a result of overloading as well as aging and the ongoing oscillation load. This leads to a very uneven distribution of the induction current in the rotor.

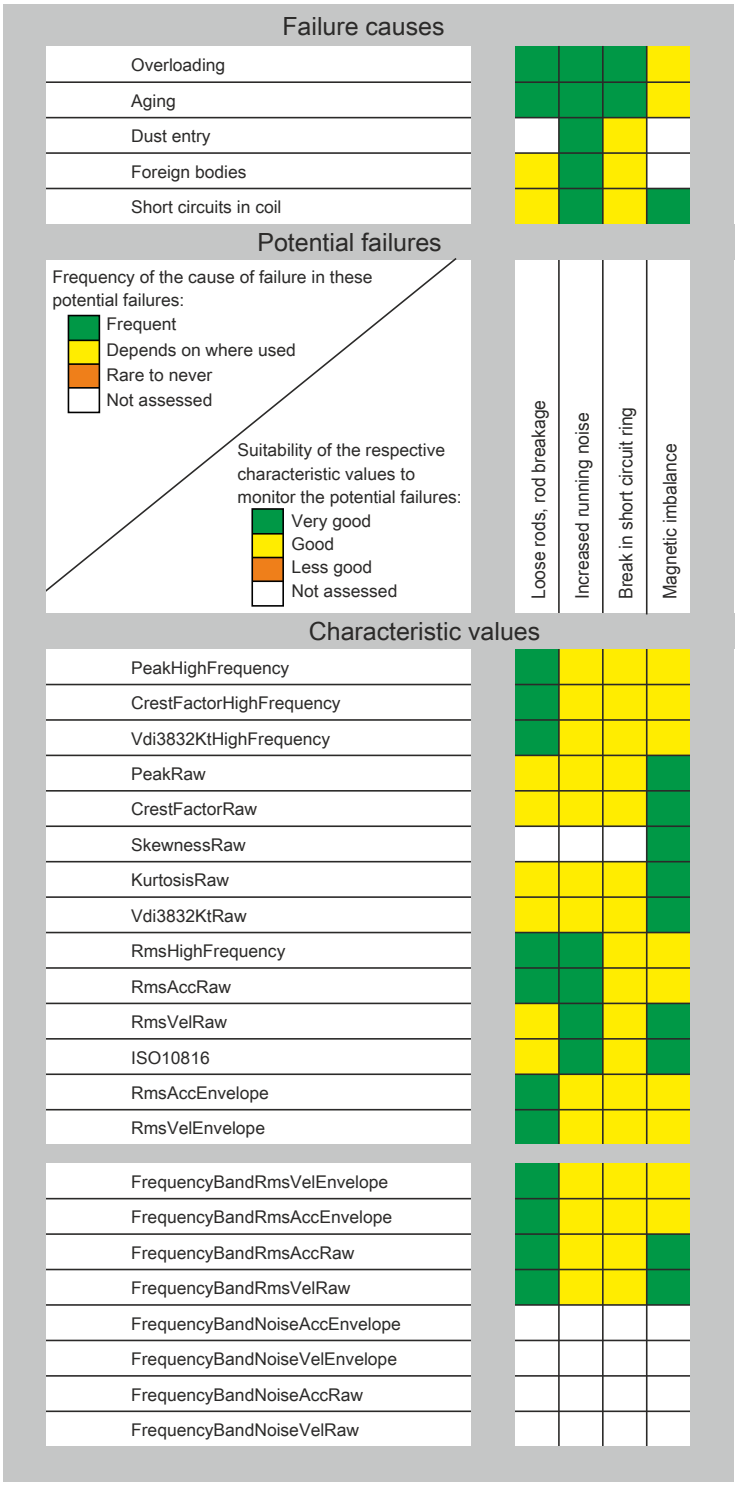


Figure 459: Electrical errors

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

4.26.4.4.3.3 Typical applications of damage recognition

The examples listed in the following are typical application cases and should provide assistance during integration. Detailed planning of usage must still be carried out for each individual case, however.

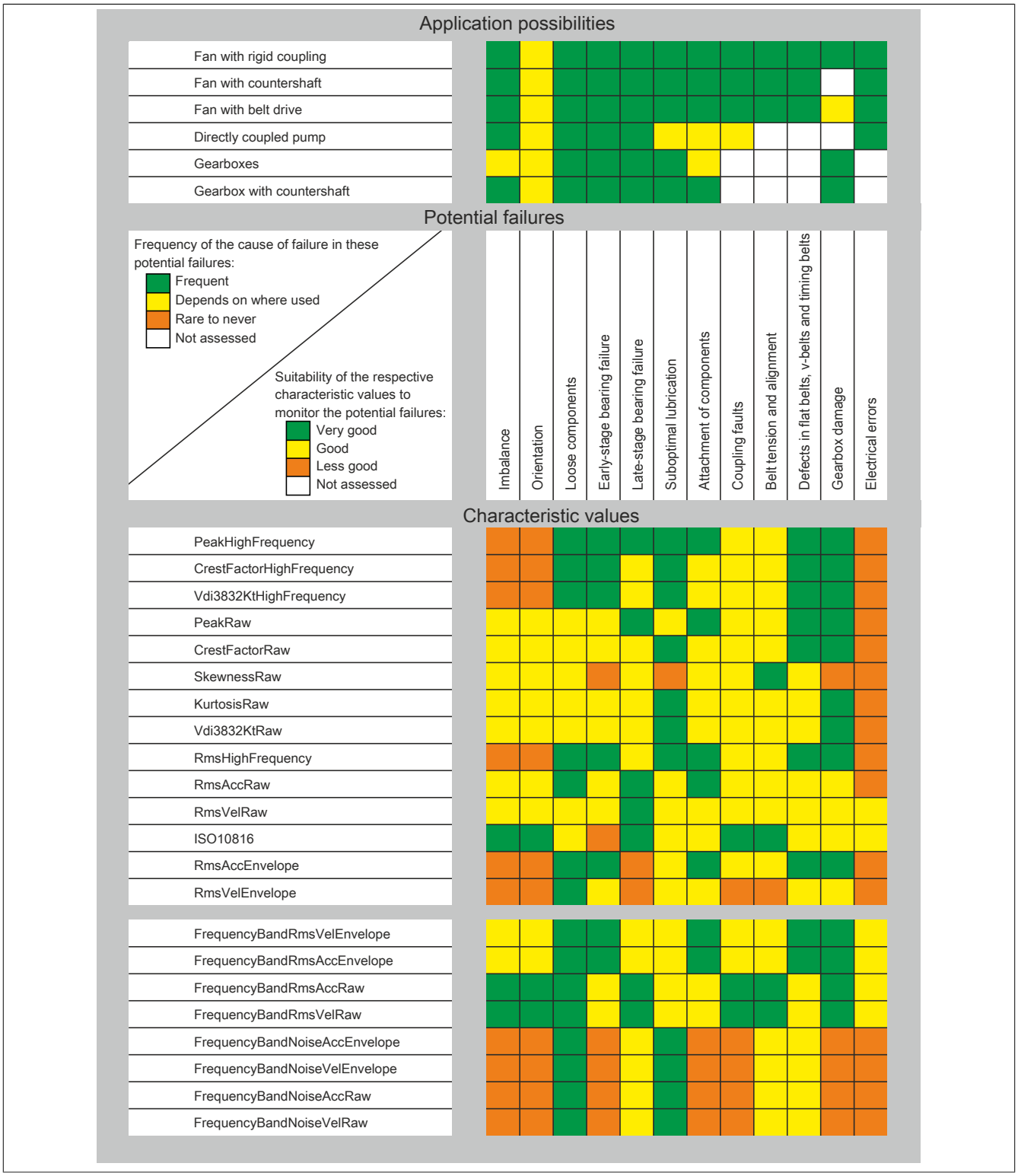


Figure 460: Typical applications of damage recognition

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Fan with rigid coupling

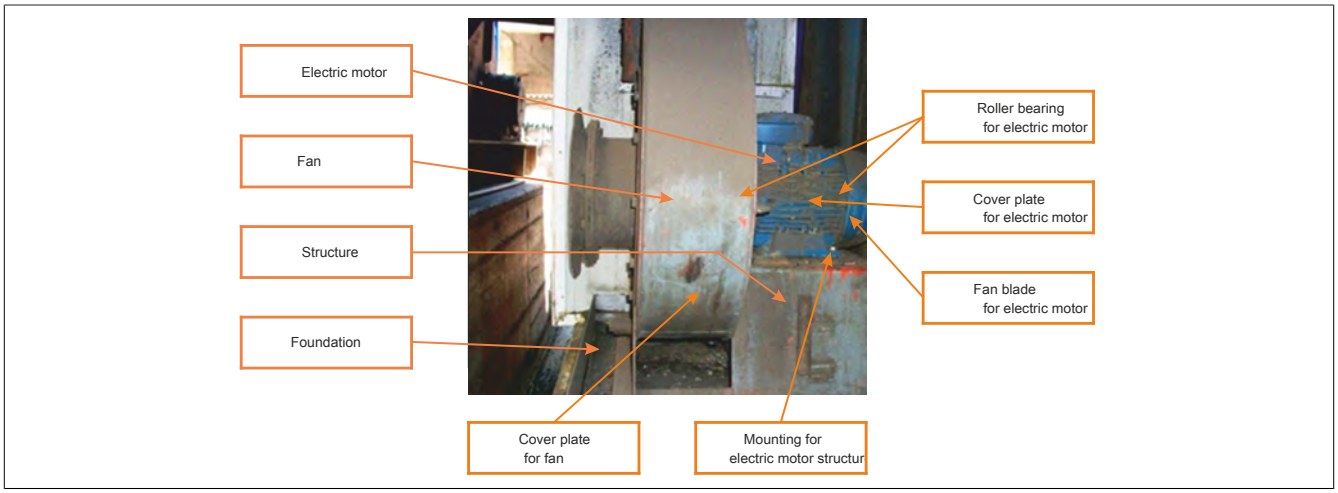


Figure 461: Drive unit with fan

Condition monitoring solution:

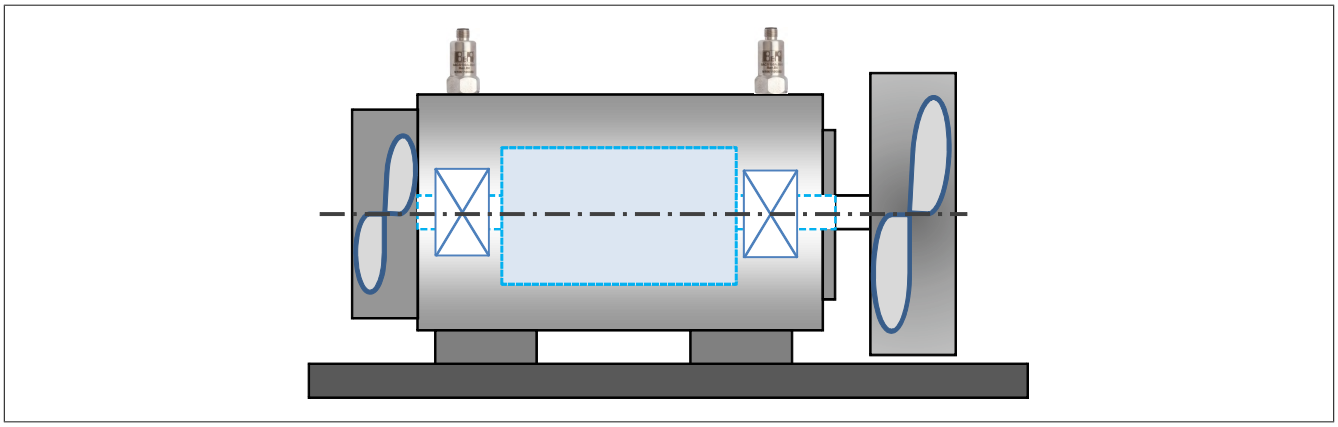


Figure 462: System diagram - Drive unit with fan

Sensor usage:

Number of sensors	Usually 2 sensors. One sensor is sufficient for smaller drive units.
Sensor installation	Preferably vertical. Horizontal installation is also possible, if necessary.

Frequent problems

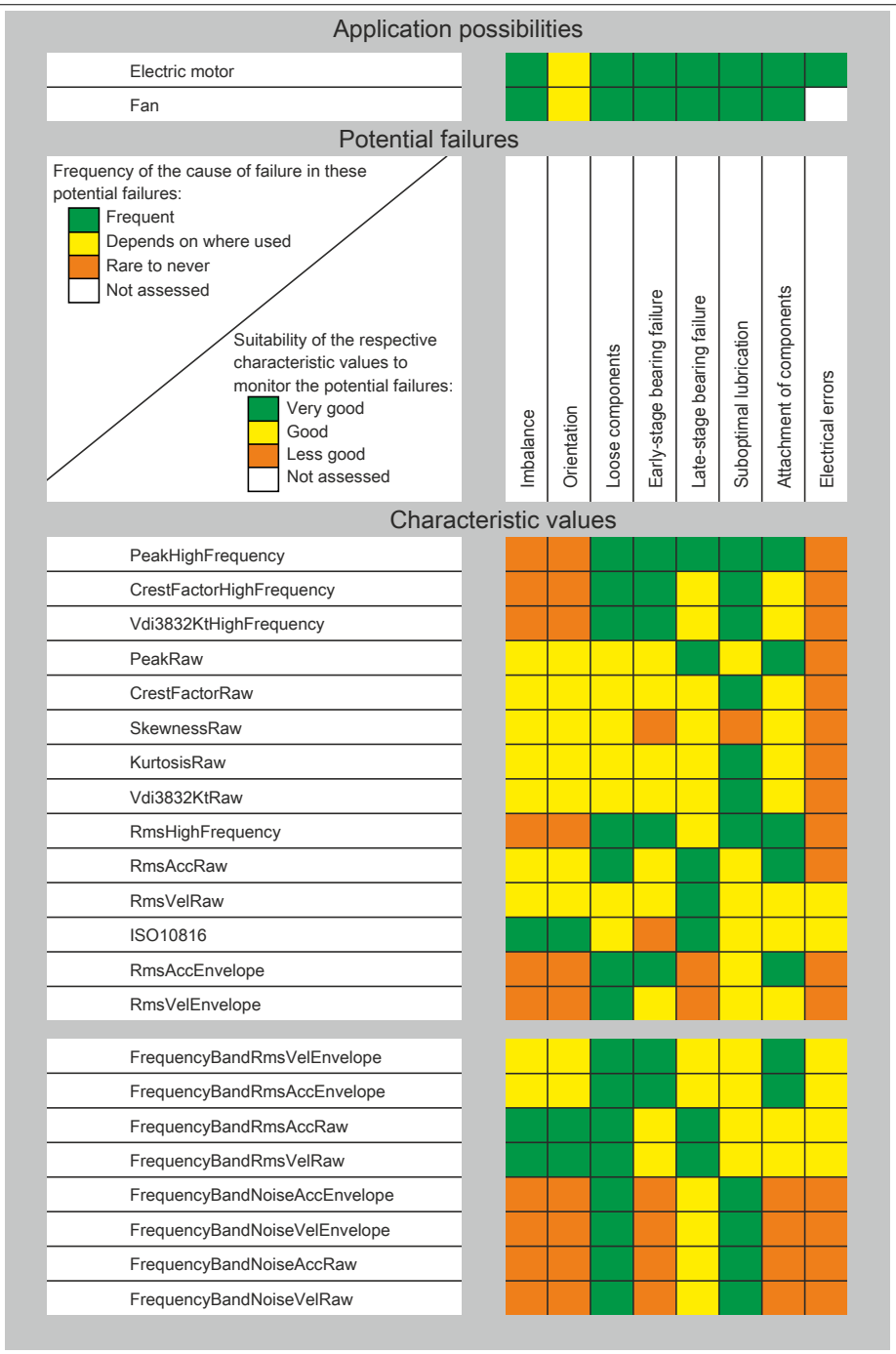


Figure 463: Fan with rigid coupling - Frequent problems

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Fan with countershaft

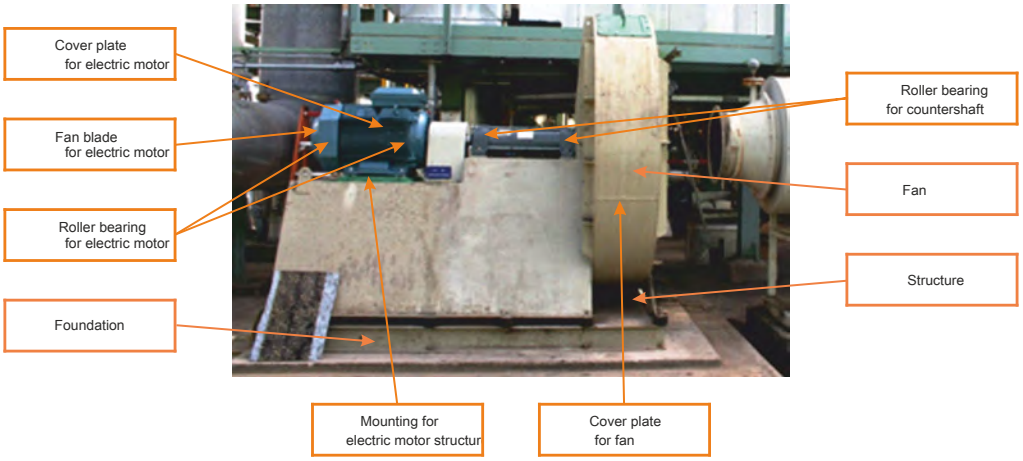


Figure 464: Drive unit with fan

Condition monitoring solution:

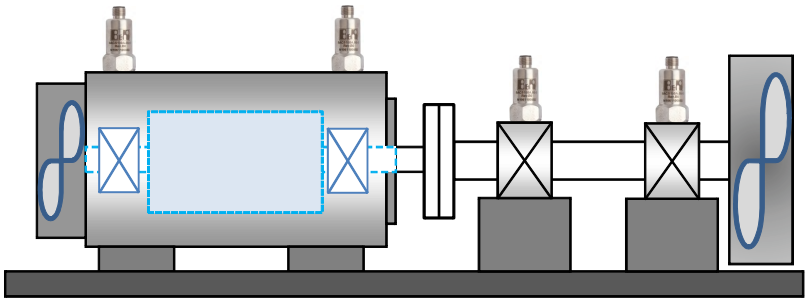


Figure 465: System diagram - Drive unit with countershaft and fan

Sensor usage:

Number of sensors	Usually 4 sensors. One sensor is sufficient for smaller drive units.
Sensor installation	Preferably vertical. Horizontal installation is also possible, if necessary.

Frequent problems

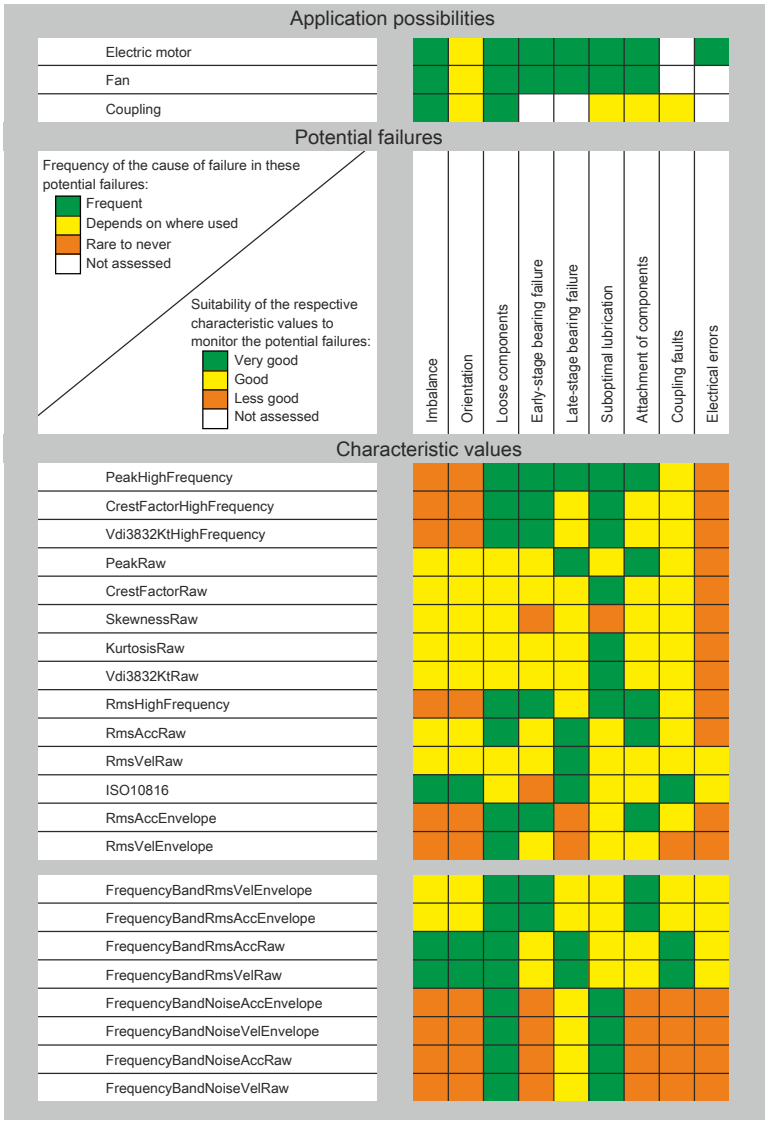


Figure 466: Fan with countershaft - Frequent problems

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Fan with belt drive

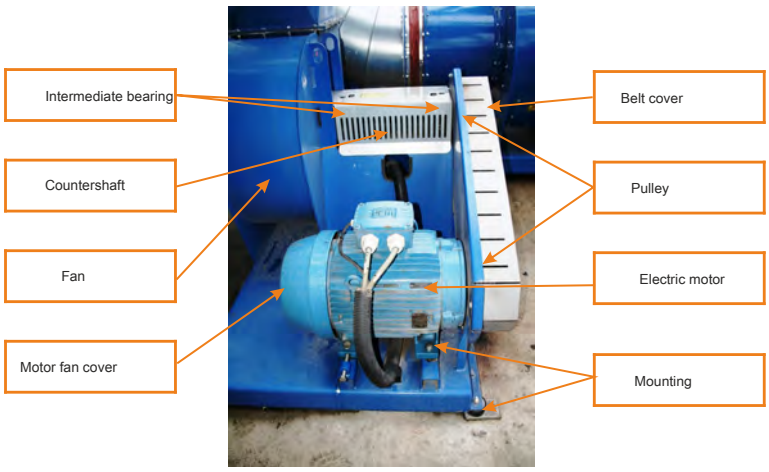


Figure 467: Structure of a fan with belt drive

Condition monitoring solutions:

Assembly A

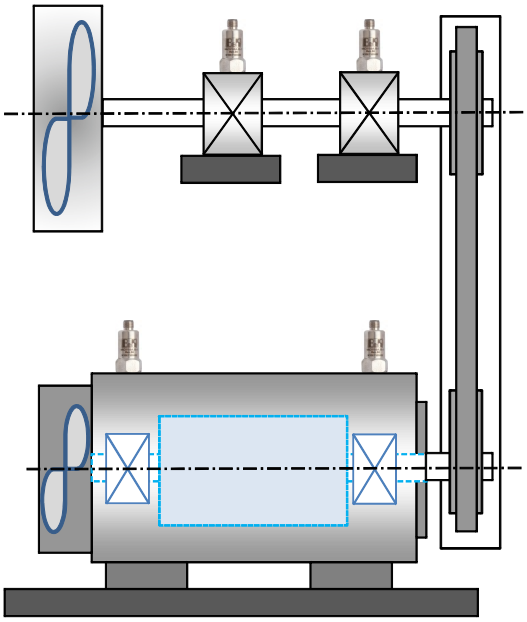


Figure 468: System diagram - Structure of a fan with belt drive

Assembly B

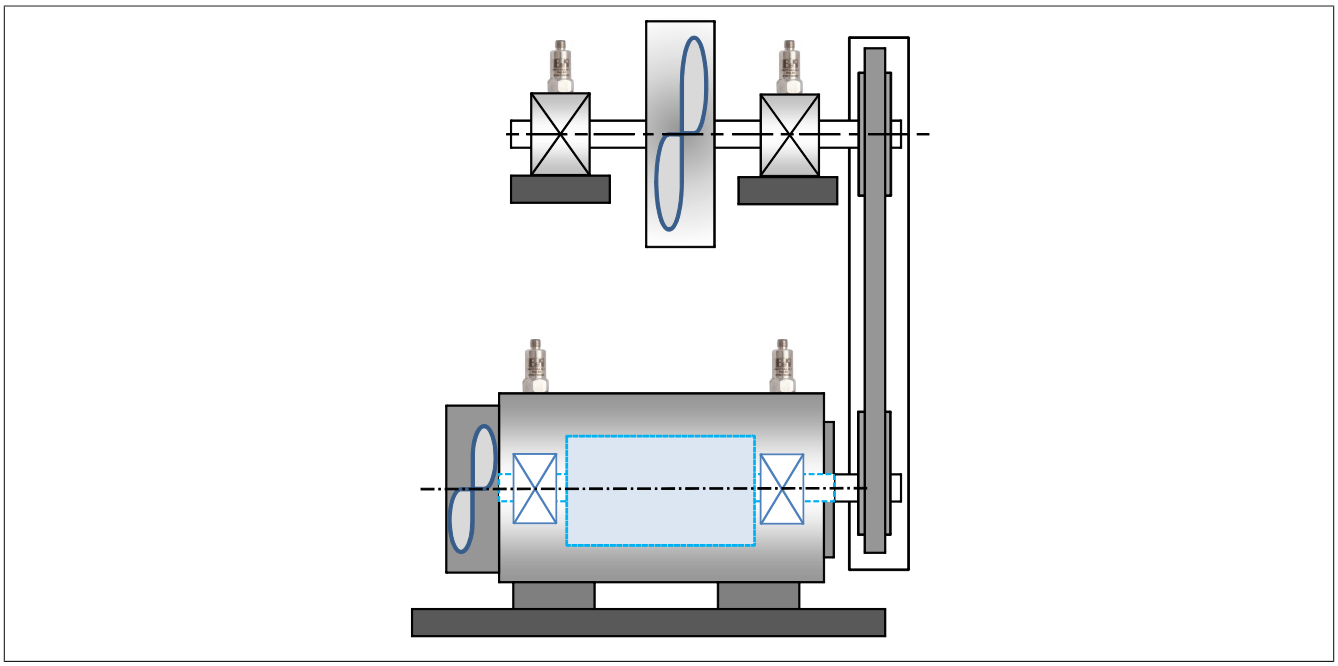


Figure 469: System diagram - Structure of a fan with belt drive - Alternative bearing

Sensor usage:

Number of sensors	Usually 4 sensors. One sensor is sufficient for smaller drive units.
Sensor installation	Preferably vertical. Horizontal installation is also possible, if necessary. Belt misalignment is particularly apparent in the axial direction.

Frequent problems

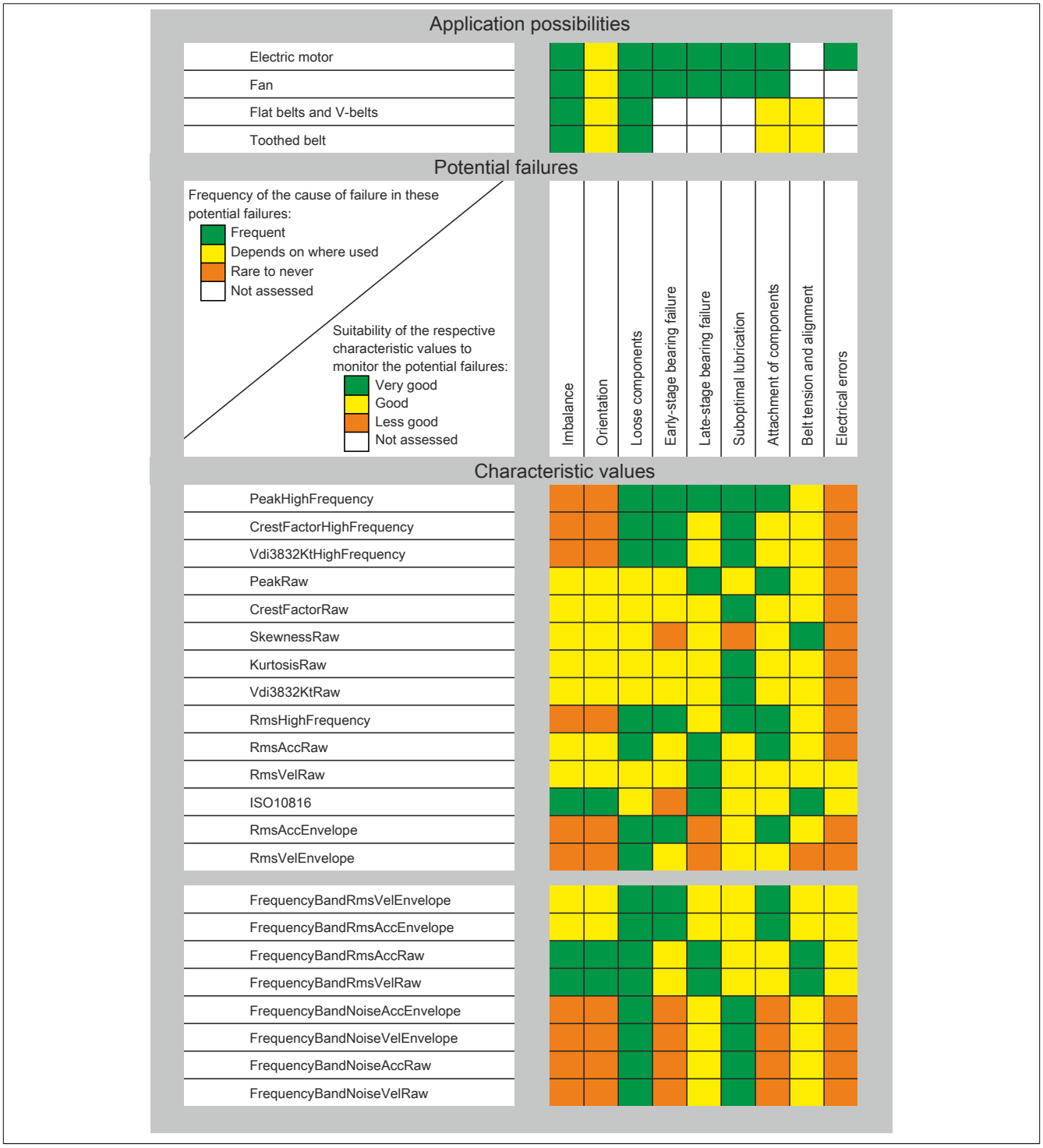


Figure 470: Fan with belt drive - Frequent problems

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Directly coupled pump

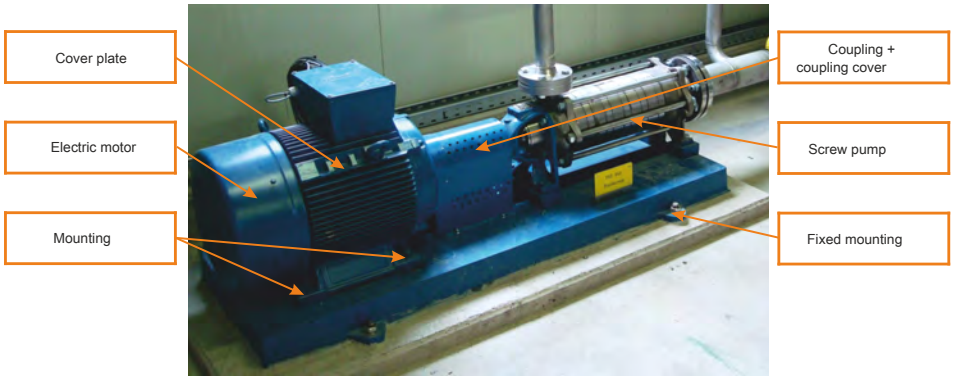


Figure 471: Structure of a pump drive

Condition monitoring solution:

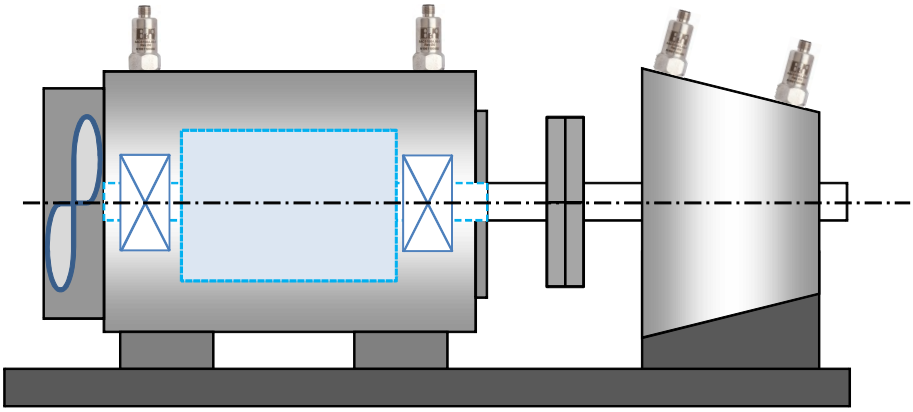


Figure 472: System diagram - Structure of a pump drive

Sensor usage:

Number of sensors	Usually 4 sensors. Two sensors are sufficient for smaller drive units.
Sensor installation	Preferably vertical. Horizontal installation is also possible, if necessary.

Frequent problems

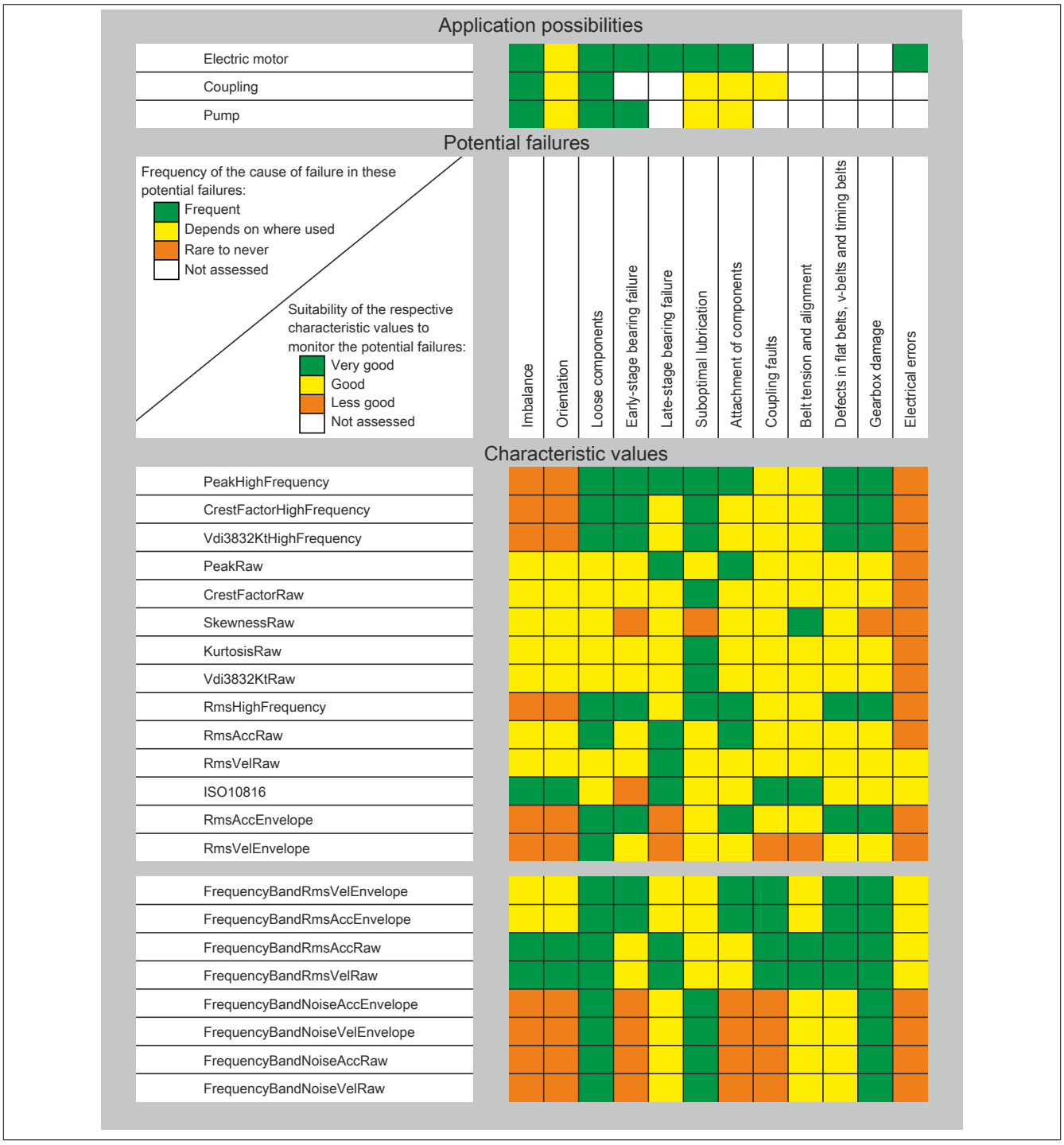


Figure 473: Directly coupled pump - Frequent problems

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Gearbox

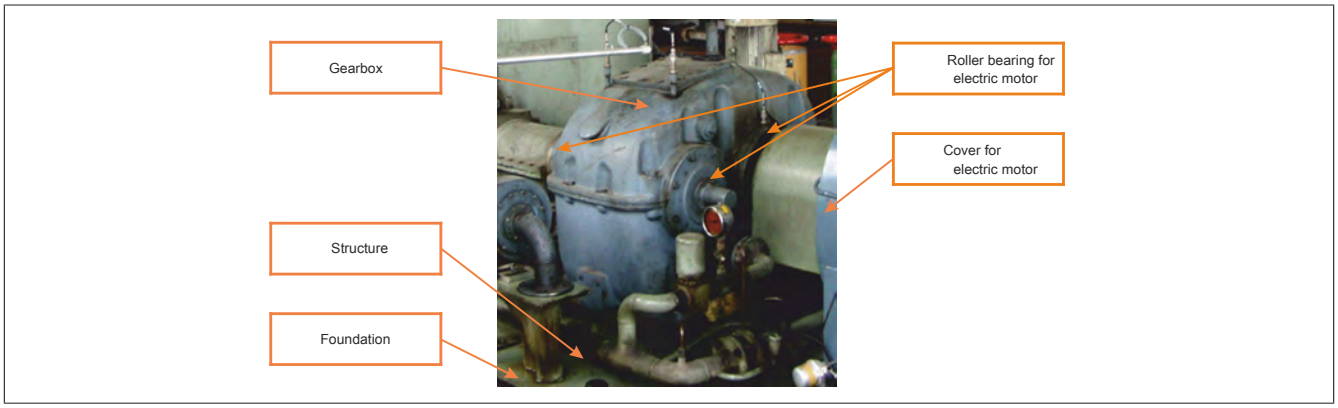


Figure 474: Structure of a gearbox

Condition monitoring solution:

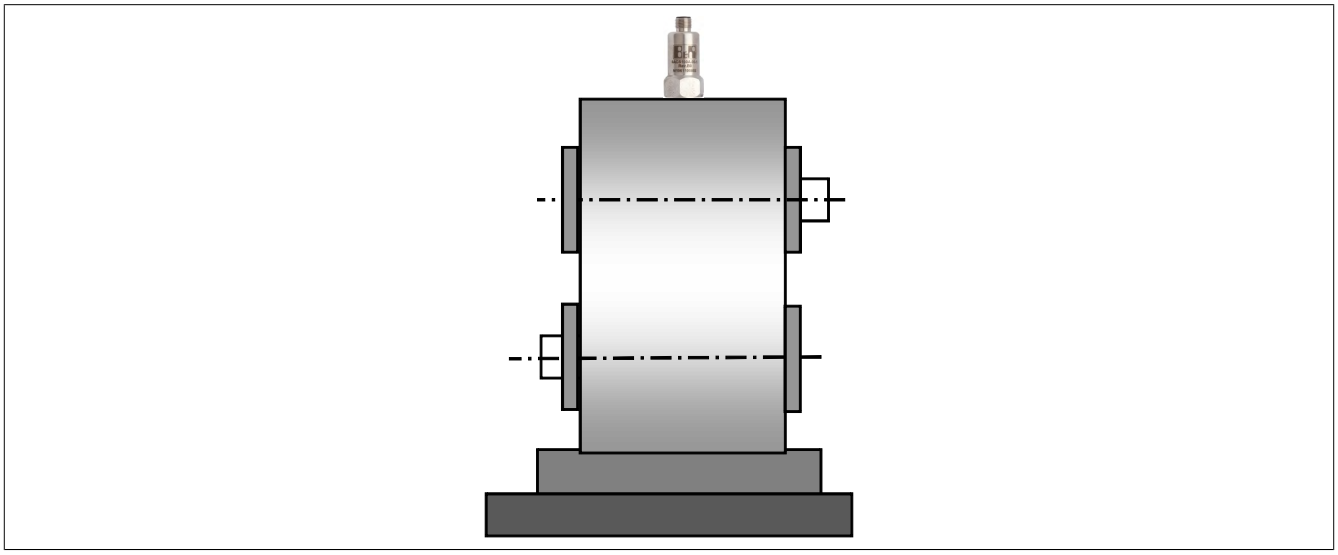


Figure 475: System diagram - Structure of a gearbox

Sensor usage:

Number of sensors	The number of sensors depends on the type and size of the gearbox.
Sensor installation	Preferably vertical. Horizontal installation is also possible, if necessary. The mounting direction depends greatly on the loading direction of the gearbox.

Frequent problems

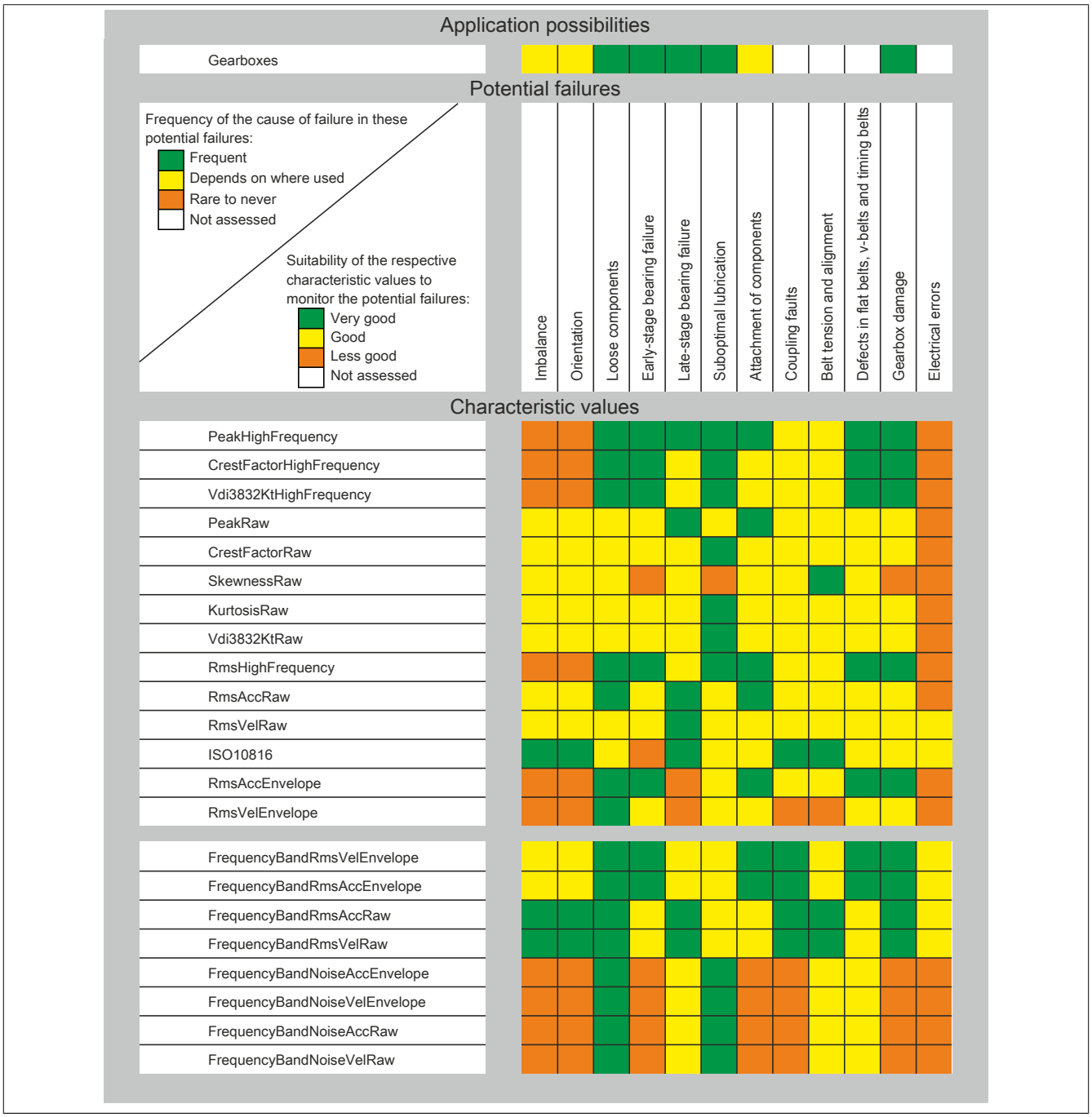


Figure 476: Gearbox - Frequent problems

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

Gearbox with countershaft

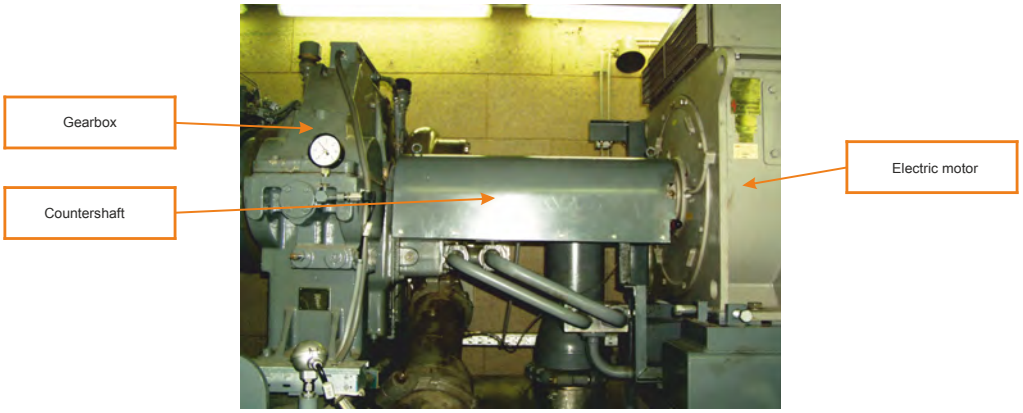


Figure 477: Structure of a gearbox with countershaft

Condition monitoring solution:

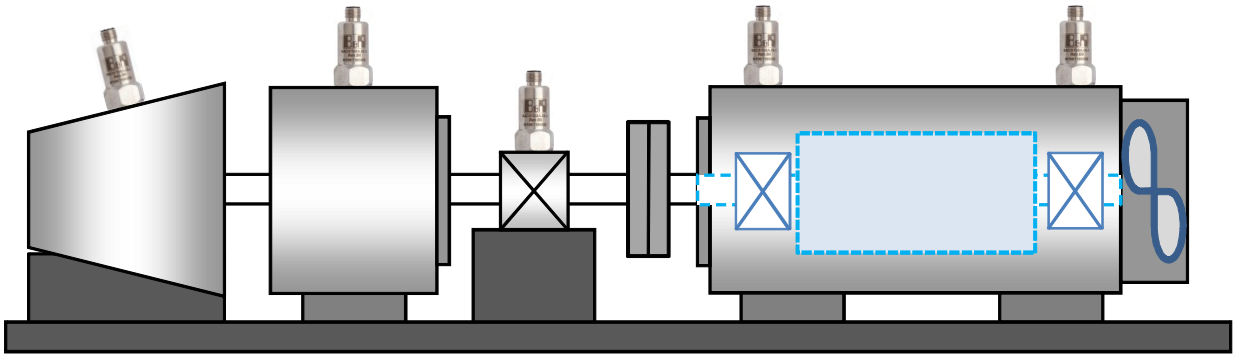


Figure 478: System diagram - Gearbox with countershaft

Sensor usage:

Number of sensors	Usually 5 sensors. Two sensors are sufficient for smaller and inflexibly coupled drive units.
Sensor installation	Preferably vertical. Horizontal installation is also possible, if necessary.

Frequent problems

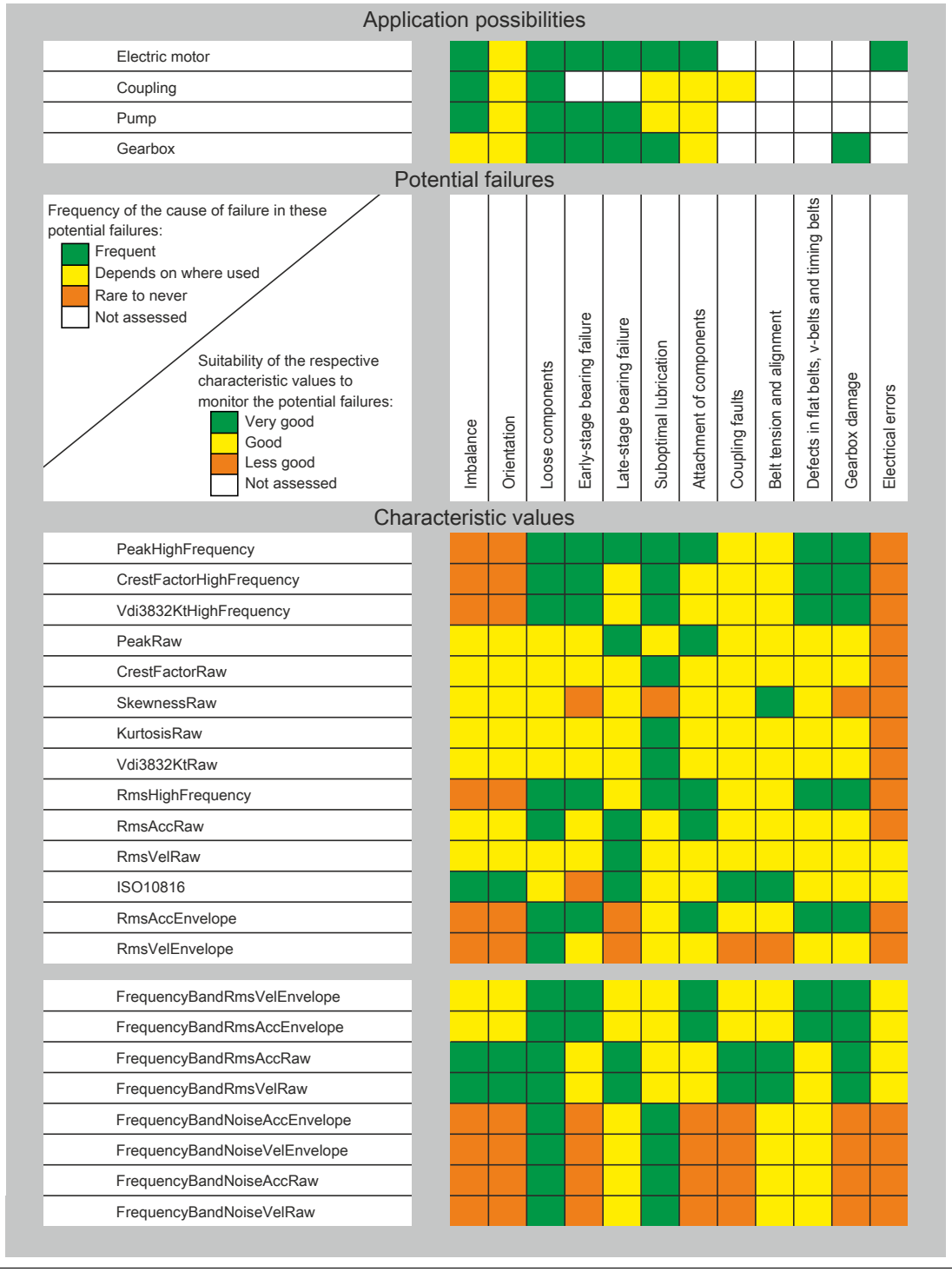


Figure 479: Gearbox with countershaft - Frequent problems

For the meaning of individual characteristic values, see "Characteristic values" and "Configuration options"

4.26.4.4.4 Further reading

Due to its extensive nature, the subject of oscillation analysis can only be outlined in this user's manual.

The following book is well suited to beginners and recommended for those wishing to research this subject in greater detail.

Zustandsüberwachung von Maschinen [Condition Monitoring of Machines]

Publisher:	Expert-Verlag GmbH
Author:	Dr. Josef Kolerus and Prof. Dr. Johann Wassermann
Edition:	5th, newly revised edition 2011
Language:	German
Pages:	408
ISBN-13:	978-3-8169-3080-8

4.26.4.5 Register description

4.26.4.5.1 Function models

A function model specifies the storage model used, i.e. which registers are available for the application. Only these registers are processed in the module during each cycle and transferred cyclically or acyclically via the bus.

The function model is used to determine the module's functionality. The following options are available:

- Standard (SG4)
- Fast master (SGC and bus coupler)
- Slow master (SGC and bus coupler)
- CANIOBusController (CANIO bus coupler)

4.26.4.5.2 Function model 0 - Standard

Automation Runtime support

This is the default function model for the X20CM4810. The calculated module characteristic values are streamed from the module via FlatStream every 300 ms and prepared for the user by Automation Runtime. If the streamed data is not collected by the next transfer, the measured characteristic values are lost. For this reason, the maximum cycle time must be observed for an error-free evaluation.

Analog inputs are provided as cyclic data points.

To help the user, all of the module's characteristic values – such as FlatStream handling for characteristic values, unit scaling and so on – are prepared in this function model using Automation Runtime and then made available to the user.

With this function model it is also possible to use an additional FlatStream to read data buffers (time signal and FFT spectrum) from the module.

The AsVib function library is available for this application.

In this function model, the X20CM4810 can only be configured using the I/O configuration. Registers may not be reconfigured asynchronously.

Features provided by Automation Runtime support:

- **"DataToggleBit01":** This bit changes its value whenever new characteristic values are loaded from the module.
- **"OverflowAnalogInput01-04":** Indicates whether a signal is pending on the input that is larger than the configured AnalogInputScale.
  Important! This is always based on a 100 mV/g sensor.
- **"OverflowCharacteristicValues01-04":** This register contains an overflow indicator bit for each characteristic value of the respective channel.
- **"OverflowFrequencyBands01"**: This register contains an overflow indicator bit for each frequency band.
- **"ActSpeed01-04"**: The module always expects a value in 0.01 Hz resolution on these data points. Automation Runtime support allows the the user to specify can state the current speed directly in Hz in the "standard" function model.
- **"SensitivitySensor01-04"**: The X20CM4810 module expects a 100 mV/g sensor on the input by default. When using other sensors, the sensor resolution can be specified in mV/g for each channel on these data points. All cyclical characteristic values are then automatically scaled to the correct sensor resolution by Automation Runtime. If this parameter is changed, then the next measurement indicated by "DataToggleBit01" is invalid.
- **"AnalogInput01-04":** The analog input is automatically scaled to the sensor resolution and with the defined AnalogInputScale. It is then made available to the user in mg. This scaling does not apply to the "Crest factor" since it is a non-dimensional value.
- **Characteristic values and frequency bands:** All characteristic values and frequency bands calculated by the X20CM4810 are flat and can be connected directly in the I/O mapping. They are already scaled to the correct sensor resolution and will be displayed in mg or mm/s or as non-dimensional values (kurtosis, crest factor, skewness and Vdi3832) depending on the characteristic value.
- **Additional characteristic values:** In addition to the characteristic values calculated by the module, the following characteristic values are also provided automatically via Automation Runtime:

- **Vdi3832KtRaw01-04:** Requires PeakRawRef and RmsRawRef as reference values and outputs the reference values used in the calculation to PeakRawRefCalculated and RmsRawRefCalulated.
- **CrestFactorHighFrequency01-04:** Ratio of the maximum amount to the RMS value ("Crest factor") of the high-frequency portions ("PeakHighFrequency" and "RmsHighFrequency") of the input signal.
- **Vdi3832KtHighFrequency01-04:** Requires PeakHighFrequencyRef and RmsHighFrequencyRef as reference values and outputs the reference values used in the calculated to PeakHighFrequencyRefCalculated and RmsHighFrequencyRefCalulated.

- **"DataConsistentWithLockedBuffers01"**: If the data buffers on the module are locked to prevent uploading, this bit is used to indicate the time at which all characteristic values and frequency bands are consistent with the locked buffers on the module.

4.26.4.5.2.1 Register of function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
General registers						
Index * 2 + 2	ActSpeed0N (Index N = 1 bis 4)	UINT			•	
1310	AutogainDelay01	UINT				•
526	AutogainDelay01Read	UINT		•		
0	Control01	UINT			•	
514	SensorConfig01	UINT				•
	SensorConfig01Read			•		
0	Status01	UINT	•			
Analog input functions						
Index * 2	AnalogInput0N (Index N = 1 bis 4)	INT	•			
1330	AnalogInputConfig01	UINT				•
570	AnalogInputConfig01Read	UINT		•		
2	AnalogInputControlByte01	UINT			•	
Index * 4 + 22	AnalogInputSamples0N (Index N = 1 bis 4)	UINT			•	
1298	AnalogInputScale01	UINT				•
546	AnalogInputScale01Read	UINT		•		
Index * 4 + 1310	SamplesAnalogInput0N (Index N = 1 bis 4)	UINT				•
Index * 4 + 526	SamplesAnalogInput0NRead (Index N = 1 bis 4)	UINT		•		
Features provided by Automation Runtime support						
	DataConsistentWithLockedBuffers01 bis 04	BOOL	•			
	DataToggleBit01	BOOL	•			
	OverflowAnalogInput01 bis 04	BOOL	•			
	OverflowCharacteristicValues01 bis 04	UINT	•			
	OverflowFrequencyBands01	UDINT	•			
	PeakHighFrequencyRef01 bis 04	REAL			•	
	PeakHighFrequencyRefCalculated01 bis 04	REAL	•			
	PeakRawRef01 bis 04	REAL			•	
	PeakRawRefCalculated01 bis 04	REAL	•			
	RmsHighFrequencyRef01 bis 04	REAL			•	
	RmsHighFrequencyRefCalculated01 bis 04	REAL	•			
	RmsRawRef01 bis 04	REAL			•	
	RmsRawRefCalculated01 bis 04	REAL	•			
	SensitivitySensor01 bis 04	REAL			•	
Characteristic values - minimum and maximum values						
2690	MinMaxCounter01	UINT		•		
Index * 8 + 3588	CrestRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2948	CrestRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3332	Iso10816Max0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2692	Iso10816Min0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3556	KurtosisRawMax0N (Index N = 1 bis 4)	DINT		•		
Index * 8 + 2916	KurtosisRawMin0N (Index N = 1 bis 4)	DINT		•		
Index * 8 + 3492	PeakHighFrequencyMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2852	PeakHighFrequencyMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3684	PeakRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3044	PeakRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3428	RmsAccEnvelopeMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2788	RmsAccEnvelopeMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3364	RmsAccRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2724	RmsAccRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3524	RmsHighFrequencyMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2884	RmsHighFrequencyMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3652	RmsRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3012	RmsRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3460	RmsVelEnvelopeMax0N (Index N = 1 bis 4)	UDINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Index * 8 + 2820	RmsVelEnvelopeMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3396	RmsVelRawMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2756	RmsVelRawMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3620	SkewnessRawMax0N (Index N = 1 bis 4)	DINT		●		
Index * 8 + 2980	SkewnessRawMin0N (Index N = 1 bis 4)	DINT		●		
Frequency configuration						
1302	HighFrequencyConfig01	UINT				●
550	HighFrequencyConfig01Read	UINT		●		
1306	MaxFrequencyEnvelope01	UINT				●
558	MaxFrequencyEnvelope01Read	UINT		●		
526	MaxFrequencyRaw01	UINT				●
554	MaxFrequencyRaw01Read	UINT		●		
522	MinFrequencyEnvelope01	UINT				●
566	MinFrequencyEnvelope01Read	UINT		●		
518	MinFrequencyRaw01	UINT				●
562	MinFrequencyRaw01Read	UINT		●		
Frequency bands						
Index * 8 + 3716	FrequencyBandMaxNN (Index NN = 01 bis 32)	UDINT		●		
Index * 8 + 3076	FrequencyBandMinNN (Index NN = 01 bis 32)	UDINT		●		
Index * 24 + 506	FrequencyBandNNConfig (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1194	FrequencyBandNNConfigRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 514	FrequencyBandNNDmgFreq60rpm (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1202	FrequencyBandNNDmgFreq60rpmRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 522	FrequencyBandNNLowerFrequency (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1210	FrequencyBandNNLowerFrequencyRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 518	FrequencyBandNNTolerance (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1206	FrequencyBandNNToleranceRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 526	FrequencyBand0NNUpperFrequency (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1214	FrequencyBandNNUpperFrequencyRead (Index NN = 01 bis 32)	UINT		●		
Flatstream						
2311	BufferForward01	USINT				●
2318	BufferForwardDelay01	UINT				●
2368	BufferInputSequence01	USINT	●			
2400	BufferOutputSequence01	USINT			●	
Index + 2368	BufferRxByte0N (Index N = 1 bis 5)	USINT	●			
Index + 2400	BufferTxByte0N (Index N = 1 bis 4)	USINT			●	
263	ParameterForward01	USINT				●

4.26.4.5.3 Function model 1 - Fast master

The characteristic values calculated by the module are streamed to the master every 300 ms via FlatStream. If the streamed data is not collected by the next transfer, the measured characteristic values are lost. For this reason, the maximum cycle time must be observed for an error-free evaluation.

With this function model, it is also possible to use an additional FlatStream to read data buffers (time signal and FFT spectrum) from the module.

Analog inputs are provided as cyclic data points. The AsVib library provides support for the user when using SGC CPUs.

This function model can only be used on **Ethernet-based masters**. However, it must be ensured that FlatStream handling is implemented on the master and that the module changes the data in the FlatStream in every X2X cycle.

4.26.4.5.3.1 Register of function model 1 - Fast master

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
General registers						
Index * 2 + 2	ActSpeed0N (Index N = 1 bis 4)	UINT			•	
1310	AutogainDelay01	UINT				•
526	AutogainDelay01Read	UINT		•		
0	Control01	UINT			•	
514	SensorConfig01	UINT				•
	SensorConfig01Read			•		
0	Status01	UINT	•			
Analog input functions						
Index * 2	AnalogInput0N (Index N = 1 bis 4)	INT	•			
1330	AnalogInputConfig01	UINT				•
570	AnalogInputConfig01Read	UINT		•		
2	AnalogInputControlByte01	UINT			•	
Index * 4 + 22	AnalogInputSamples0N (Index N = 1 bis 4)	UINT			•	
1298	AnalogInputScale01	UINT				•
546	AnalogInputScale01Read	UINT		•		
Index * 4 + 1310	SamplesAnalogInput0N (Index N = 1 bis 4)	UINT				•
Index * 4 + 526	SamplesAnalogInput0NRead (Index N = 1 bis 4)	UINT		•		
Characteristic values - minimum and maximum values						
2690	MinMaxCounter01	UINT		•		
Index * 8 + 3588	CrestRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2948	CrestRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3332	Iso10816Max0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2692	Iso10816Min0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3556	KurtosisRawMax0N (Index N = 1 bis 4)	DINT		•		
Index * 8 + 2916	KurtosisRawMin0N (Index N = 1 bis 4)	DINT		•		
Index * 8 + 3492	PeakHighFrequencyMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2852	PeakHighFrequencyMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3684	PeakRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3044	PeakRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3428	RmsAccEnvelopeMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2788	RmsAccEnvelopeMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3364	RmsAccRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2724	RmsAccRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3524	RmsHighFrequencyMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2884	RmsHighFrequencyMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3652	RmsRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3012	RmsRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3460	RmsVelEnvelopeMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2820	RmsVelEnvelopeMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3396	RmsVelRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2756	RmsVelRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3620	SkewnessRawMax0N (Index N = 1 bis 4)	DINT		•		
Index * 8 + 2980	SkewnessRawMin0N (Index N = 1 bis 4)	DINT		•		
Frequency configuration						
1302	HighFrequencyConfig01	UINT				•
550	HighFrequencyConfig01Read	UINT		•		
1306	MaxFrequencyEnvelope01	UINT				•
558	MaxFrequencyEnvelope01Read	UINT		•		
526	MaxFrequencyRaw01	UINT				•
554	MaxFrequencyRaw01Read	UINT		•		
522	MinFrequencyEnvelope01	UINT				•
566	MinFrequencyEnvelope01Read	UINT		•		
518	MinFrequencyRaw01	UINT				•
562	MinFrequencyRaw01Read	UINT		•		
Frequency bands						

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Index * 8 + 3716	FrequencyBandMaxNN (Index NN = 01 bis 32)	UDINT		●		
Index * 8 + 3076	FrequencyBandMinNN (Index NN = 01 bis 32)	UDINT		●		
Index * 24 + 506	FrequencyBandNNConfig (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1194	FrequencyBandNNConfigRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 514	FrequencyBandNNDmgFreq60rpm (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1202	FrequencyBandNNDmgFreq60rpmRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 522	FrequencyBandNNLowerFrequency (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1210	FrequencyBandNNLowerFrequencyRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 518	FrequencyBandNNTolerance (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1206	FrequencyBandNNToleranceRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 526	FrequencyBand0NNUpperFrequency (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1214	FrequencyBandNNUpperFrequencyRead (Index NN = 01 bis 32)	UINT		●		
Flatstream						
2311	BufferForward01	USINT				●
2318	BufferForwardDelay01	UINT				●
2368	BufferInputSequence01	USINT	●			
2400	BufferOutputSequence01	USINT			●	
Index + 2368	BufferRxByte0N (Index N = 1 bis 5)	USINT	●			
Index + 2400	BufferTxByte0N (Index N = 1 bis 4)	USINT			●	
263	ParameterForward01	USINT				●
270	ParameterForwardDelay01	INT				●
320	ParameterInputSequence01	USINT	●			
352	ParameterOutputSequence01	USINT			●	
Index + 320	ParameterRxByteN (Index N = 1 bis 13)	USINT	●			

4.26.4.5.4 Function model 2 - Slow master

This function model was developed specifically for operating the X20CM4810 with "slow masters" and for conserving resources on the PLC.

With this function model, it is not possible to upload data buffers from the module.

Analog inputs are provided as cyclic data points.

Characteristic values are calculated by the module every 300 ms and can only be read via acyclical access. In order to keep all characteristic values consistent with one another, they can be locked as they are read (RequestDataLock01). This function model does not allow for seamless measurements, however, although minimum and maximum functionality can be used for seamless recording. See 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705

This function model is recommended for all slow buses and masters. It is important to note that asynchronous register access must be implemented on the master if a B&R master is not being used.

4.26.4.5.4.1 Register of function model 2 - Slow master

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
General registers						
Index * 2 + 2	ActSpeed0N (Index N = 1 bis 4)	UINT			•	
1310	AutogainDelay01	UINT				•
526	AutogainDelay01Read	UINT		•		
0	Control01	UINT			•	
514	SensorConfig01	UINT				•
	SensorConfig01Read			•		
0	Status01	UINT	•			
Analog input functions						
Index * 2	AnalogInput0N (Index N = 1 bis 4)	INT	•			
1330	AnalogInputConfig01	UINT				•
570	AnalogInputConfig01Read	UINT		•		
2	AnalogInputControlByte01	UINT			•	
Index * 4 + 22	AnalogInputSamples0N (Index N = 1 bis 4)	UINT			•	
1298	AnalogInputScale01	UINT				•
546	AnalogInputScale01Read	UINT		•		
Index * 4 + 1310	SamplesAnalogInput0N (Index N = 1 bis 4)	UINT				•
Index * 4 + 526	SamplesAnalogInput0NRead (Index N = 1 bis 4)	UINT		•		
Characteristic values						
Index * 8 + 828	CrestFactorRaw0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 572	Iso10816_0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 796	KurtosisRaw0N (Index N = 1 bis 4)	DINT		•		
Index * 8 + 732	PeakHighFrequency0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 924	PeakRaw0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 668	RmsAccEnvelope0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 604	RmsAccRaw0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 764	RmsHighFrequency0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 982	RmsRaw0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 700	RmsVelEnvelope0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 636	RmsVelRaw0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 860	SkewnessRaw0N (Index N = 1 bis 4)	DINT		•		
Characteristic values - minimum and maximum values						
2690	MinMaxCounter01	UINT		•		
Index * 8 + 3588	CrestRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2948	CrestRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3332	Iso10816Max0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2692	Iso10816Min0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3556	KurtosisRawMax0N (Index N = 1 bis 4)	DINT		•		
Index * 8 + 2916	KurtosisRawMin0N (Index N = 1 bis 4)	DINT		•		
Index * 8 + 3492	PeakHighFrequencyMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2852	PeakHighFrequencyMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3684	PeakRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3044	PeakRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3428	RmsAccEnvelopeMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2788	RmsAccEnvelopeMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3364	RmsAccRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2724	RmsAccRawMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3524	RmsHighFrequencyMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 2884	RmsHighFrequencyMin0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3652	RmsRawMax0N (Index N = 1 bis 4)	UDINT		•		
Index * 8 + 3012	RmsRawMin0N (Index N = 1 bis 4)	UDINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Index * 8 + 3460	RmsVelEnvelopeMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2820	RmsVelEnvelopeMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3396	RmsVelRawMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2756	RmsVelRawMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3620	SkewnessRawMax0N (Index N = 1 bis 4)	DINT		●		
Index * 8 + 2980	SkewnessRawMin0N (Index N = 1 bis 4)	DINT		●		
Frequency configuration						
1302	HighFrequencyConfig01	UINT				●
550	HighFrequencyConfig01Read	UINT		●		
1306	MaxFrequencyEnvelope01	UINT				●
558	MaxFrequencyEnvelope01Read	UINT		●		
526	MaxFrequencyRaw01	UINT				●
554	MaxFrequencyRaw01Read	UINT		●		
522	MinFrequencyEnvelope01	UINT				●
566	MinFrequencyEnvelope01Read	UINT		●		
518	MinFrequencyRaw01	UINT				●
562	MinFrequencyRaw01Read	UINT		●		
Frequency bands						
Index * 8 + 3716	FrequencyBandMaxNN (Index NN = 01 bis 32)	UDINT		●		
Index * 8 + 3076	FrequencyBandMinNN (Index NN = 01 bis 32)	UDINT		●		
Index * 8 + 956	FrequencyBandNN (Index NN = 01 bis 32)	UDINT		●		
Index * 24 + 506	FrequencyBandNNConfig (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1194	FrequencyBandNNConfigRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 514	FrequencyBandNNDmgFreq60rpm (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1202	FrequencyBandNNDmgFreq60rpmRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 522	FrequencyBandNNLowerFrequency (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1210	FrequencyBandNNLowerFrequencyRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 518	FrequencyBandNNTolerance (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1206	FrequencyBandNNToleranceRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 526	FrequencyBand0NNUpperFrequency (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1214	FrequencyBandNNUpperFrequencyRead (Index NN = 01 bis 32)	UINT		●		

4.26.4.5.5 Function model 254 - Bus controller

This function model can only be used with a CANIO bus controller. It includes the same functionality as Function model 2 - Slow master.

Differences:

- The order of cyclical registers is different on the bus for reasons of consistency.
- Since the AnalogInputToggleBit01-04 data points cannot be consistently transferred to the "AnalogInput01-04" data points, they are not available in this function model. The user must watch for changes in the value of the data points "AnalogInput01-04" in order to determine whether a new value is available.

4.26.4.5.5.1 Register of function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
General registers							
Index * 2 + 2	Index * 4 + 2	ActSpeed0N (Index N = 1 bis 4)	UINT			●	
1310		AutogainDelay01	UINT				●
526		AutogainDelay01Read	UINT		●		
0	2	Control01	UINT			●	
514		SensorConfig01	UINT				●
		SensorConfig01Read			●		
0	2	Status01	UINT	●			
Analog input functions							
Index * 2	Index * 4 + 2	AnalogInput0N (Index N = 1 bis 4)	INT	●			
1330		AnalogInputConfig01	UINT				●
570		AnalogInputConfig01Read	UINT		●		
2	22	AnalogInputControlByte01	UINT			●	
1298		AnalogInputScale01	UINT				●
546		AnalogInputScale01Read	UINT		●		
Index * 4 + 1310		SamplesAnalogInput0N (Index N = 1 bis 4)	UINT				●
Index * 4 + 526		SamplesAnalogInput0NRead (Index N = 1 bis 4)	UINT		●		
Characteristic values							
Index * 8 + 828		CrestFactorRaw0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 572		Iso10816_0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 796		KurtosisRaw0N (Index N = 1 bis 4)	DINT		●		
Index * 8 + 732		PeakHighFrequency0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 924		PeakRaw0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 668		RmsAccEnvelope0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 604		RmsAccRaw0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 764		RmsHighFrequency0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 982		RmsRaw0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 700		RmsVelEnvelope0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 636		RmsVelRaw0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 860		SkewnessRaw0N (Index N = 1 bis 4)	DINT		●		
Characteristic values - minimum and maximum values							
2690		MinMaxCounter01	UINT		●		
Index * 8 + 3588		CrestRawMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2948		CrestRawMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3332		Iso10816Max0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2692		Iso10816Min0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3556		KurtosisRawMax0N (Index N = 1 bis 4)	DINT		●		
Index * 8 + 2916		KurtosisRawMin0N (Index N = 1 bis 4)	DINT		●		
Index * 8 + 3492		PeakHighFrequencyMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2852		PeakHighFrequencyMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3684		PeakRawMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3044		PeakRawMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3428		RmsAccEnvelopeMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2788		RmsAccEnvelopeMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3364		RmsAccRawMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2724		RmsAccRawMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3524		RmsHighFrequencyMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2884		RmsHighFrequencyMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3652		RmsRawMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3012		RmsRawMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3460		RmsVelEnvelopeMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2820		RmsVelEnvelopeMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3396		RmsVelRawMax0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 2756		RmsVelRawMin0N (Index N = 1 bis 4)	UDINT		●		
Index * 8 + 3620		SkewnessRawMax0N (Index N = 1 bis 4)	DINT		●		
Index * 8 + 2980		SkewnessRawMin0N (Index N = 1 bis 4)	DINT		●		
Frequency configuration							
1302		HighFrequencyConfig01	UINT				●

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
550		HighFrequencyConfig01Read	UINT		●		
1306		MaxFrequencyEnvelope01	UINT				●
558		MaxFrequencyEnvelope01Read	UINT		●		
526		MaxFrequencyRaw01	UINT				●
554		MaxFrequencyRaw01Read	UINT		●		
522		MinFrequencyEnvelope01	UINT				●
566		MinFrequencyEnvelope01Read	UINT		●		
518		MinFrequencyRaw01	UINT				●
562		MinFrequencyRaw01Read	UINT		●		
Frequency bands							
Index * 8 + 3716		FrequencyBandMaxNN (Index NN = 01 bis 32)	UDINT		●		
Index * 8 + 3076		FrequencyBandMinNN (Index NN = 01 bis 32)	UDINT		●		
Index * 8 + 956		FrequencyBandNN (Index NN = 01 bis 32)	UDINT		●		
Index * 24 + 506		FrequencyBandNNConfig (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1194		FrequencyBandNNConfigRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 514		FrequencyBandNNDmgFreq60rpm (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1202		FrequencyBandNNDmgFreq60rpmRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 522		FrequencyBandNNLowerFrequency (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1210		FrequencyBandNNLowerFrequencyRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 518		FrequencyBandNNTolerance (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1206		FrequencyBandNNToleranceRead (Index NN = 01 bis 32)	UINT		●		
Index * 24 + 526		FrequencyBand0NNUpperFrequency (Index NN = 01 bis 32)	UINT				●
Index * 24 + 1214		FrequencyBandNNUpperFrequencyRead (Index NN = 01 bis 32)	UINT		●		

1) The offset specifies the position of the register within the CAN object.

4.26.4.5.6 Module registers - General information

4.26.4.5.6.1 AnalogInput function

General information

Each of the four acceleration sensor inputs on the X20CM4810 can also be used directly as an analog input with various special functions ("AnalogInput01-04").

The resolution of the analog input can be set using the configuration ("AnalogInputScale01"). The lower the maximum value, the higher the resolution of the data point and vice versa. When the maximum value is exceeded, the data point is limited to the respective maximum (positive or negative).

A toggle bit (AnalogInputToggleBit01-04) signals when a new value has been transferred.

The following functions are available:

- Normal AnalogInput function
- Characteristic value calculation in continuous mode with enable (continuous mode)
- Characteristic value calculation in trigger mode (single shot)

AnalogInput

The last 8 measured values before the X2X cycle are always averaged and transferred on the bus. Here, the direct input signal (raw signal max. 10 kHz) with a sampling frequency of 25.781 kHz is always used and is not offset-adjusted.

Characteristic value calculation in AnalogInput

It is possible to display the following characteristic values directly in AnalogInput. In this case, it is necessary to check the configured scale.

- Average
- Peak value (absolute)
- RMS
- Crest factor

Two signals are available to calculate the configured characteristic values:

- Raw input signal filtered to 10 kHz with a sampling frequency of 25.781 kHz and without calculating the average (offset adjustment)
- Raw signal filtered to the maximum frequency with a sampling frequency that is dependent on the "MaxFrequencyRaw01" configuration and with an average calculation (offset adjustment) from the last 8192 samples.

Similarly, the registers ("SamplesAnalogInput") can be used to specify how many of the values (samples) are to be calculated for the relevant parameter. The time between 2 samples depends on the maximum frequency.

2 modes are available:

- Continuous mode with enable (continuous mode)
- Trigger mode (single shot)

Continuous mode with enable (continuous mode)

This mode offers the following advantages:

- When the parameters are configured correctly, nothing can be overlooked.
- Using "enable", measurement in the module can be started after an event or events can be hidden.
- The toggle bit toggles with every new value.

The following must be taken into consideration for the configuration:

- In order to guarantee seamless measurement, the sample time (number of samples * sample rate) must be longer than the X2X cycle (see section "SamplesAnalogInput" on page 2687).
- If a shorter sample time than the X2X Link cycle is configured, the last complete measurement is always transferred.

Information:

Values are lost here. The measured values cannot be transferred to the bus because multiple values are calculated in each X2X Link cycle.

Trigger mode (single shot)

This mode offers the following advantages:

- Only one measurement is taken at a time.
- The trigger is edge-sensitive, so it can be retriggered in each X2X Link cycle.
- The toggle bit toggles with every new value.

The following must be taken into consideration for the configuration:

- A new trigger will be ignored during an ongoing measurement. The runtime on the bus can cause retriggering before the toggle bit has changed.
- If a shorter sample time than the X2X Link cycle is configured, then the first complete measurement is always transferred.
- In trigger mode, values are lost because the measurement values are recorded asynchronously to the X2X Link and cannot be synchronized continually.
- The trigger results in temporary synchronization with X2X Link.

AnalogInput01-04

Depending on the configuration this data point contains:

- The actual input value of the associated input averaged over the last 8 samples
- Or the characteristic value to be calculated using the configured number of samples

The value in the data point is scaled according to the configuration "AnalogInputScale01".

If scaling the value takes it outside of the permitted value range for INT, then it will be limited to the minimum or maximum INT value. The overflow bit for the corresponding channel is not set in this case.

Information:

In Function model 0 - Standard, Automation Runtime automatically scales the analog input to mg or non-dimensional values (crest factor) while taking SensitivitySensor and AnalogInputScale into account. If the value of the analog input without sensor scaling exceeds the value range of the AnalogInputscale of 100 mV/g, then the corresponding AnalogInputOverflow bit is used.

AnalogInputConfig01

Register for configuring the characteristic value calculation in "AnalogInput01-04". This is only needed if "SamplesAnalogInput" of the respective channel is greater than 0.

Bit	Description
15	Signal source for characteristic value calculation AnalogInput04. For possible values, see signal source AnalogInput01.
14	Signal source for characteristic value calculation AnalogInput03. For possible values, see signal source AnalogInput01.
13	Signal source for characteristic value calculation AnalogInput02. For possible values, see signal source AnalogInput01.
12	Signal source for characteristic value calculation AnalogInput01 **Value** / **Description** 1 – Raw signal filtered to 10 kHz without calculating the average 0 – Raw signal filtered to the maximum frequency of the raw signal with calculation of the average value for the last 8192 samples
11	Trigger mode for AnalogInput04 (0 = Continuous with enable, 1 = Once with trigger)
10	Trigger mode for AnalogInput03 (0 = Continuous with enable, 1 = Once with trigger)
9	Trigger mode for AnalogInput02 (0 = Continuous with enable, 1 = Once with trigger)
8	Trigger mode for AnalogInput01 (0 = Continuous with enable, 1 = Once with trigger)
7-6	Value to be calculated in AnalogInput04. For possible values, see value to be calculated for AnalogInput01.
5-4	Value to be calculated in AnalogInput03. For possible values, see value to be calculated for AnalogInput01.
3-2	Value to be calculated in AnalogInput02. For possible values, see value to be calculated for AnalogInput01.
1-0	Value to be calculated in AnalogInput01 **Value** / **Description** 3 – Crest factor 2 – RMS value 1 – Peak value 0 – Average

Table 606: AnalogInputConfig01

AnalogInputConfig01Read

Register for reading the current AnalogInput01 configuration.

AnalogInputControlByte01

The control register for "AnalogInput01-04" is only functional if the respective "SamplesAnalogInput" configuration register is greater than 0.

The configuration in "AnalogInputConfig01" of each channel determines whether the respective bit is an enable or a trigger bit.

Bit	Description
15-4	Reserved = 0
3	AnalogInputControl04 for the parameter calculation by AnalogInput04
2	AnalogInputControl03 for the parameter calculation by AnalogInput03
1	AnalogInputControl02 for the parameter calculation by AnalogInput02
0	AnalogInputControl01 for the parameter calculation by AnalogInput01

Table 607: AnalogInputControlByte01

AnalogInputControl01-04 in continuous mode:

Bit to start the continuous characteristic value calculation of "AnalogInput01-04".

0 = Characteristic value calculation off

1 = Continuous calculation

If this bit = 1, then the characteristic value configured in "AnalogInputConfig01" for the respective channel is calculated continuously. The number of samples configured in "SamplesAnalogInput" is used. The calculated value is displayed in "AnalogInput01-04" with the scaling of the respective channel configured in "AnalogInputScale01". The value of AnalogInputToggleBit01-04 changes each time a new calculation takes place.

AnalogInputControl01-04 in single-shot mode:

Bit to start a new characteristic value calculation of "AnalogInput01-04". Every edge starts a new calculation provided the previous one is already completed.

If the value of this bit changes, then the characteristic value configured in "AnalogInputConfig01" for the respective channel is calculated. The number of samples configured in "SamplesAnalogInput" is used. The calculated value is displayed in "AnalogInput01-04" with the scaling of the respective channel configured in "AnalogInputScale01". The value of AnalogInputToggleBit01-04 changes each time a new calculation takes place.

AnalogInputSamples

Name:
AnalogInputSamples01 to AnalogInputSamples04

If Bit 15 of the corresponding SamplesAnalogInput register is 1, then this register is used cyclically to set the number of samples for parameter calculation.

Information:

If the register is changed during an active measurement, then the current measurement is discarded (AnalogInputToggleBit0X is not toggled). Keep an eye out for this, particularly with Enable in continuous mode.

Data type	Value
UINT	See bit structure.

Bit structure:

Data type	Value	Description
	> 8191	Invalid
	8191 to 1	Characteristic value calculation active for the respective channel in the corresponding analog input
	0	Invalid

The time between 2 samples depends on MaxFrequencyRaw:

Maximum frequency	Sample time (time between 2 samples)
10000 Hz	38.79 µs
5000 Hz	77.58 µs
2000 Hz	193.94 µs
1000 Hz	387.88 µs
500 Hz	775.76 µs
200 Hz	1939.39 µs

Table 608: Overview of the sample time at the maximum frequency of the raw signal

AnalogInputScale01

This register can be used to specify the scale of the four analog inputs ("AnalogInput01-04"). If the actual value is greater than the value configured in this register, the respective register for the analog input ("AnalogInput01-04") is limited to the positive maximum (32767).

For example, if ±128 is configured for AnalogInput04, then the 16 bits represent a value range of ±128 g or without units if the crest factor has been calculated.

Information:

The configured scaling value is always based on a 100 mV/g sensor. Any sensor that has a different sensor resolution must be reflected in the configuration.

Bit	Description
15-12	Scaling for AnalogInput04. For possible values, see AnalogInput01.
11-8	Scaling for AnalogInput03. For possible values, see AnalogInput01.
7-4	Scaling for AnalogInput02. For possible values, see AnalogInput01.
3-0	Scaling for AnalogInput01

Value	Description
15 - 9	Invalid
8	±128
7	±64
6	±32
5	±16
4	±8
3	±4
2	±2
1	±1
0	Invalid

Table 609: AnalogInputScale01

AnalogInputScale01Read

This register can be used to read the scale of the analog inputs ("AnalogInput01-04").

SamplesAnalogInput

Name:
SamplesAnalogInput01 to SamplesAnalogInput04

If the corresponding SamplesAnalogInput register is equal to 0, then the "AnalogInput01-04" data points will provide the current input value for the analog input.

If the SamplesAnalogInput register is greater than 0, the characteristic value configured in "AnalogInputConfig01" for the respective channel is calculated. For this, the number of samples configured in this register will be used and displayed in the corresponding AnalogInput with the configured scaling.

Data type	Value	Description
UINT	Bit 15	0 = The samples are set cyclically via the register AnalogInputSamples01 - 04
		1 = The samples are configured using the register AnalogInputSamples01 - 04
	> 8191	Invalid
	8191 to 1	Characteristic value calculation active for the respective channel in the corresponding analog input
	0	Characteristic value calculation not active for the respective channel in the corresponding analog input

Table 610: SamplesAnalogInput01-04

If Bit 15 of the SamplesAnalogInput is 1, then the parameter configured in "AnalogInputConfig01" is also calculated. However, the number of samples set cyclically in the AnalogInputSamples register will be used and displayed in the corresponding AnalogInput with the configured scaling.

The time between 2 samples depends on MaxFrequencyRaw:

Maximum frequency	Sample time (time between 2 samples)
10000 Hz	38.79 µs
5000 Hz	77.58 µs
2000 Hz	193.94 µs
1000 Hz	387.88 µs
500 Hz	775.76 µs
200 Hz	1939.39 µs

Table 611: Overview of the sample time at the maximum frequency of the raw signal

SamplesAnalogInputRead

Name:
SamplesAnalogInput01Read to SamplesAnalogInput04Read

Register for reading the current "SamplesAnalogInput" configuration.

Data type	Value
UINT	0 to 65535

4.26.4.5.6.2 Frequency bands

General information

The X20CM4810 has 32 frequency bands that can be configured as needed. It is important to note that the format varies depending on the configuration (see section 4.26.4.2.11 "Characteristic value format" on page 2602). The following functions are available:

- "Broadband RMS"
- "Speed-dependent RMS"
- "Noise"

If frequencies are entered that are outside the minimum and maximum signal frequency for the selected channel, then only the domains between the minimum and maximum frequency will be analyzed.

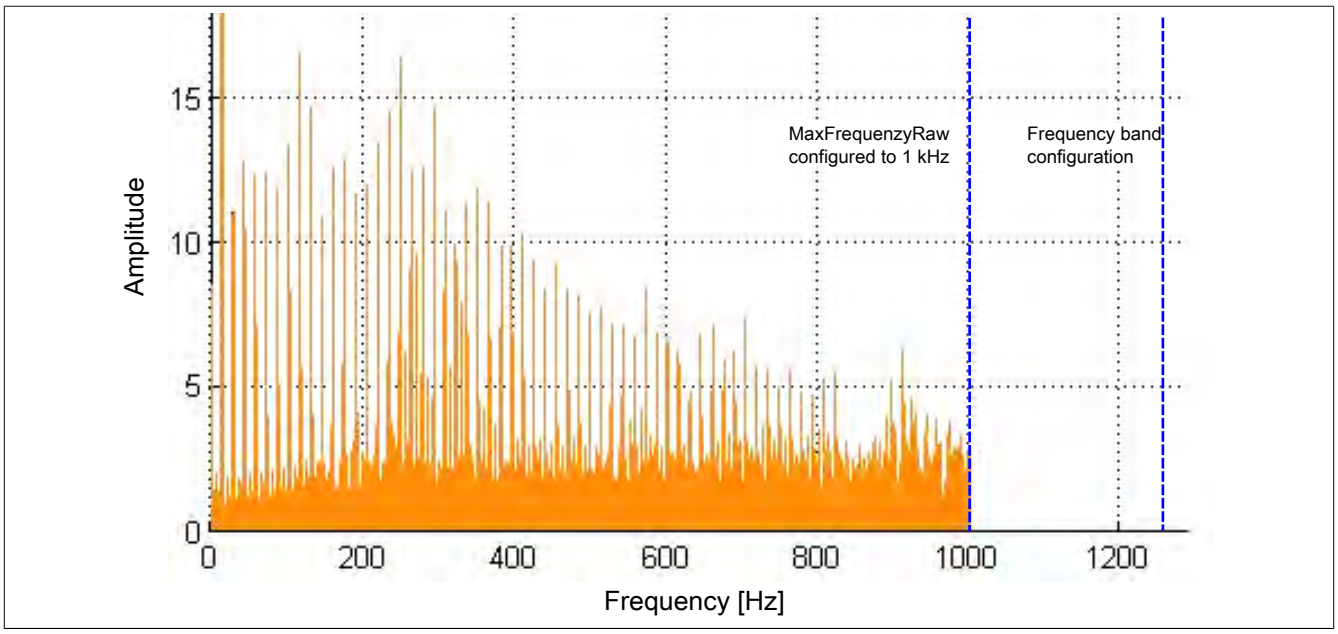


Figure 480: Restricting the frequency band evaluation

Two neighboring lines (samples) in the spectrum that are already outside the set window (one above and one below the window) will be partially included in the calculation depending on their distance from the window.

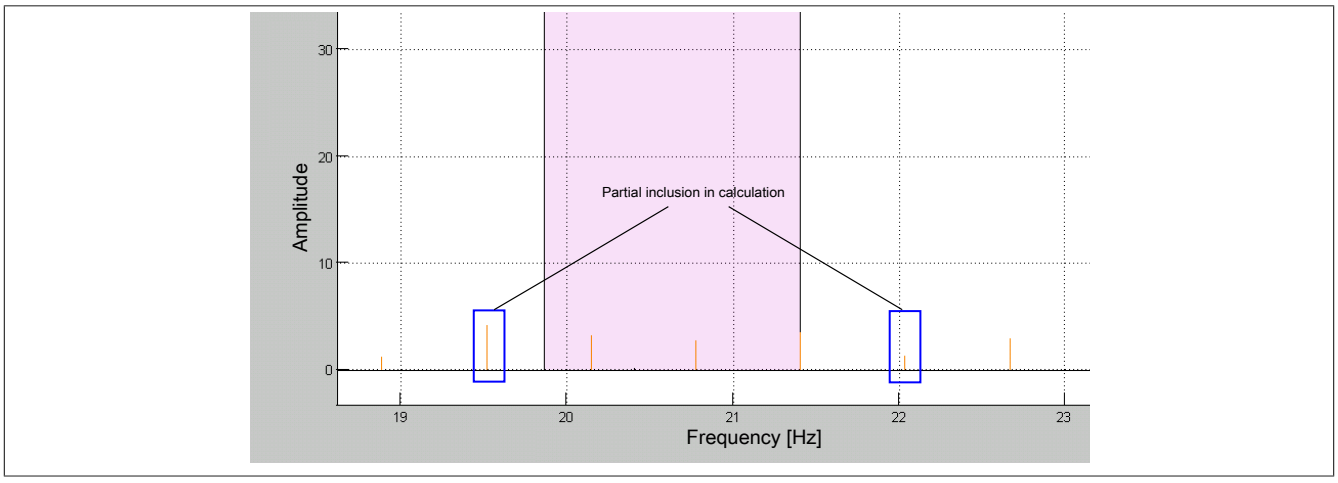


Figure 481: Partial inclusion of marginal lines in the calculation

Guidelines for configuring the frequency bands

- The total range of the frequency band is at least 2 * 0.005 * max. drive frequency [Hz].
- The upper and lower frequency limits must not be less than 0.005 * max. drive frequency [Hz] from the desired average frequency.
  Example
  At a maximum drive frequency of 50 Hz, a frequency band should be set at 10 Hz.
  10 Hz ± (0.005 * 50 Hz) = At least 9.75 Hz lower and 10.25 Hz upper frequency band limits
- Depending on the MaxFrequency selected, a least three lines should be configured within each frequency band.
- The first lines to the left and right of the configured frequency band are included proportionally based on their distance from the frequency band (see image above).

Broadband RMS

In this configuration, the RMS value of the configured signal and channel in the frequency band is calculated. The value is calculated from the minimum frequency ("FrequencyBandXXLowerFrequency") to the maximum frequency ("FrequencyBandXXUpperFrequency"). The minimum and maximum frequency can be entered here in increments of 0.25 Hz.

Any channel for any frequency band can be selected.

The following signals can be selected for each channel:

- Raw acceleration signal
- Raw velocity signal. Equal to 0 if the speed calculation is disabled.
- Enveloped acceleration signal
- Enveloped velocity signal. Equal to 0 if the speed calculation is disabled.

The harmonic frequencies (whole number multiples) of the window can also be included in the calculation. Here, the width of the window is simply retained and the mean frequency of the window is multiplied (by 1, 2, 3, etc.) until the maximum frequency of the configured signal and channel is reached.

Speed-dependent RMS

In this configuration, the RMS value is calculated in a movable window. There are 4 speed inputs for this ("ActSpeed01-04" in 0.01 Hz). One of the 4 speeds can be selected for each of the 32 frequency bands. In addition, the standardized damage frequency at 60 rpm ("FrequencyBandXXDmgFreq60rpm") and a tolerance ("FrequencyBandXXTolerance") must be configured. These can be configured separately for each frequency band.

The window in which the RMS is calculated is determined as follows:

Minimum frequency = (speed * standardized damage frequency at 60 rpm) – tolerance

Maximum frequency = (speed * standardized damage frequency at 60 rpm) + tolerance

The standardized damage frequency and tolerance can be entered here in increments of 0.01 Hz.

The following signals can be selected for each channel:

- Raw acceleration signal
- Raw velocity signal. Equal to 0 if the speed calculation is disabled.
- Enveloped acceleration signal
- Enveloped velocity signal. Equal to 0 if the speed calculation is disabled.

The harmonic frequencies (whole number multiples) of the window can also be included in the calculation. Here, the width of the window is simply retained and the mean frequency of the window is multiplied (by *1, *2, *3, etc.) until the maximum frequency of the set signal and channel is reached.

Useful information

If a fixed frequency band is needed in which the minimum frequency ("FrequencyBandXXLowerFrequency") and maximum frequency ("FrequencyBandXXUpperFrequency") must be set with a higher precision than 0.25 Hz, then a speed-dependent frequency band with a fixed speed can be used.

Noise

In this configuration, the noise from a quadrant of the respective signal on the selected channel that is within the frequency band is calculated.

To do this, the configured maximum frequency of the signal on the selected channel is divided by 4. This results in 4 quadrants. A configuration can then be used to select one of the 4 quadrants in which the noise should be determined.

The following signals can be selected for each channel:

- Raw acceleration signal
- Raw velocity signal. Equal to 0 if the speed calculation is disabled.
- Enveloped acceleration signal
- Enveloped velocity signal. Equal to 0 if the speed calculation is disabled.

This configuration allows slippage to be effectively measured, for example. The higher the friction, the more noise that is created.

ActSpeed01-04

Data point for the current speed to calculate FrequencyBands01-32 as long as they have been configured as being speed-dependent.

The current speed must be specified in 1/100 Hz. In Function model 0 - Standard, Automation Runtime handles this. The current speed is defined in hertz.

If the 4 different speed data points are not sufficient, e.g. for several different gear ratios, the speed ratio can also be included when calculating the standardized damage frequency for the frequency band ("FrequencyBand-DmgFreq60rpm").

FrequencyBandConfig

Name:
FrequencyBand01Config to FrequencyBand32Config

General configuration of individual frequency bands.

Each frequency band can be calculated on any channel with any of the four speed data points ("ActSpeed01-04").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description
15	Reserved = 0
14-13	Selects the quadrant to calculate the noise **Value** / **Description** 3 – 4 quadrant from 3/4 MaxFrequency to MaxFrequency of the respective signal (raw signal or envelope signal) on the channel 2 – 3 quadrant from 1/2 MaxFrequency to 3/4 MaxFrequency of the respective signal (raw signal or envelope signal) on the channel 1 – 2 quadrant from 1/4 MaxFrequency to 1/2 MaxFrequency of the respective signal (raw signal or envelope signal) on the channel 0 – 1 quadrant from MinFrequency to 1/4 MaxFrequency of the respective signal (raw signal or envelope signal) on the channel
12	Enables noise calculation instead of RMS (0 = Off, 1 = On) As soon as this is enabled, the speed-dependent and harmonic settings are ignored.
11-8	Selects which ActSpeed data point should be used for the calculation if the frequency band is speed-dependent **Value** / **Description** 15 - 4 – Invalid 3 – ActSpeed04 2 – ActSpeed03 1 – ActSpeed02 0 – ActSpeed01
7	Includes harmonic frequencies in the calculation (0 = Off, 1 = On) If enabled, all harmonic frequencies up to the maximum frequency are included in the calculation. **Information:** **The harmonic frequencies can also include frequency portions that are the result of damage at other positions. This can lead to a misinterpretation of the measurement.**
6	Speed-dependent (0 = Off, 1 = On) If enabled, the ActSpeed data point is used with the entered FrequencyBandDmgFreq60rpm and the configured FrequencyBandTolerance to calculate the frequency band. If disabled, then FrequencyBandLowerFrequency and FrequencyBandUpperFrequency are used to calculate the frequency band.
5-4	Selects the signal for calculating the frequency band **Value** / **Description** 3 – Enveloped acceleration signal 2 – Raw acceleration signal 1 – Enveloped velocity signal Only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output. 0 – Raw velocity signal Only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.
3-0	Selects which input channel should be used to calculate the frequency band **Value** / **Description** 15 - 4 – Invalid 3 – Channel 4 2 – Channel 3 1 – Channel 2 0 – Channel 1

Table 612: FrequencyBand01Config - FrequencyBand32Config

FrequencyBandConfigRead

Name:
FrequencyBand01ConfigRead to FrequencyBand32ConfigRead

Registers for reading the configuration of individual frequency bands.

Data type	Value
UINT	0 to 65535

FrequencyBandDmgFreq60rpm

Name:
FrequencyBand01DmgFreq60rpm to FrequencyBand32DmgFreq60rpm

Standardized damage frequency at 60 rpm if the frequency band is configured as speed-dependent.

This is multiplied with the configured velocity data point in the module to calculate the frequency band.

The standardized damage frequency must be specified in 1/100.

Data type	Value
UINT	1 bis 65,535

FrequencyBandDmgFreq60rpmRead

Name:
FrequencyBand01DmgFreq60rpmRead to FrequencyBand32DmgFreq60rpmRead

Register to read the standardized damage frequency at 60 rpm for the individual frequency bands.

The standardized damage frequency is specified in 1/100.

Data type	Value
UINT	1 bis 65,535

FrequencyBandTolerance

Name:
FrequencyBand01Tolerance to FrequencyBand32Tolerance

If the frequency band is configured as speed-dependent, then this data point can be used to specify the frequency band's width.

The FrequencyBandTolerance is subtracted once from the damage frequency calculated from the ActSpeed and FrequencyBandDmgFreq60rpm to get the frequency band's lower frequency and added once to get the higher frequency.

The tolerance must be specified in 1/100 Hz. Valid values are 1 to 65535.

Data type	Value
UINT	1 bis 65,535

FrequencyBandToleranceRead

Name:
FrequencyBand01ToleranceRead to FrequencyBand32ToleranceRead

Registers for reading the tolerance of individual frequency bands.

The tolerance is specified in 1/100 Hz.

Data type	Value
UINT	1 to 65,535

FrequencyBandLowerFrequency

Name:
FrequencyBand01LowerFrequency to FrequencyBand32LowerFrequency

Minimum frequency for calculating the frequency band if it is not speed-dependent.

The minimum frequency must be specified in 1/4 Hz.

Data type	Value
UINT	1 to 40,000

FrequencyBandLowerFrequencyRead

Name:
FrequencyBand01LowerFrequencyRead to FrequencyBand32LowerFrequencyRead

Registers for reading the minimum frequency of individual frequency bands.

The minimum frequency is specified in 1/4 Hz.

Data type	Value
UINT	1 to 40,000

FrequencyBandUpperFrequency

Name:
FrequencyBand01UpperFrequency to FrequencyBand32UpperFrequency

Maximum frequency for calculating the frequency band if it is not speed-dependent.

The maximum frequency must be specified in 1/4 Hz.

Data type	Value
UINT	1 to 40,000

FrequencyBandUpperFrequencyRead

Name:
FrequencyBand01UpperFrequencyRead to FrequencyBand32UpperFrequencyRead

Registers for reading the maximum frequency of individual frequency bands.

The maximum frequency is specified in 1/4 Hz.

Data type	Value
UINT	1 to 40,000

4.26.4.5.6.3 AutogainDelay01

This register can be used to configure the autogain delay for all four channels.

To ensure that even smaller signals can be calculated precisely, the autogain can be increased in steps. This happens if there has been no overflow in the number of measurement cycles configured in this register and all conditions for the next step were always met. If an overflow does occur, then autogain is reduced immediately by one step.

The unit for delaying autogain is specified in measurement cycles (300 ms). Only values from 1 - 200 are valid.

4.26.4.5.6.4 AutogainDelay01Read

Register for reading the current "AutogainDelay01" configuration.

4.26.4.5.6.5 Control01

General control register for the X20CM4810

Bit	Description
15-2	Reserved = 0
1	MinMaxUpdate01, asynchronous min. and max. values refreshed at each edge
0	RequestBufferLock01 or RequestDataLock01 (0 = Don't lock data, 1 = Lock data)

Table 613: Control01

RequestBufferLock01 or RequestDataLock01:

Function model 0 - Standard and Function model 1 - Fast master:
RequestBufferLock01 can be used to lock all buffers and parameters on the X20CM4810 module. When the bit is set to 1, all buffers (raw data and FFT) are locked starting at the beginning of the next measurement. Before a buffer can be uploaded, all data on the X20CM4810 must be locked.
The characteristic values associated with the locked buffers are transferred in the FlatStream characteristic values as soon as BufferLockValid01 = 1.

Information:

Since the measurement is universal, the parameters associated with the buffers are only transferred once.

Function model 2 - Slow master and Function model 254 - Bus controller:
RequestDataLock01 can be used to lock all parameters on the X20CM4810 module. When the bit is set to 1, then a consistent version of all measurement values is retained until the next measurement. Once all data on the module has been locked, all the calculated characteristic values can be read asynchronously from the module.
Data on the X20CM4810 is only locked once the BufferLockValid01 or DataLockValid01 bit has been set in the status register ("Status01").
Once the data has been uploaded, the RequestBufferLock01 or RequestDataLock01 bit can be reset to 0. Once BufferLockValid01 or DataLockValid01 in the status register ("Status01") has returned to 0, the data one the module is no longer locked.
The module doesn't permit another freeze until the channel's buffer has been filled with the maximum buffer length. The buffer length depends on "MaxFrequencyRaw01" and "MaxFrequencyEnvelope01".

MinMaxUpdate01

An edge on MinMaxUpdate01 updates all asynchronous minimum and maximum values. A new cycle then starts internally to generate the minimum and maximum values that are again copied to the acyclic registers on the next edge. Once an edge has been reached, the current minimum and maximum values can be read asynchronously in the next X2X cycle. The "MinMaxCounter01" register specifies how many measurement cycles were analyzed with minimum and maximum mapping. The minimum/maximum values themselves are only valid if the counter has a value other than 0.

4.26.4.5.6.6 DataConsistentWithLockedBuffers01

If the data buffers on the module are locked to prevent uploading, this bit is used to indicate the time at which all characteristic values and frequency bands are consistent with the locked buffers on the module.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.7 DataToggleBit01

This bit changes its value whenever new characteristic values are loaded from the module and updated (approximately every 300 ms).

It is only available in Function model 0 - Standard.

4.26.4.5.6.8 HighFrequencyConfig01

Register for defining the envelope signal high-pass and the high-frequency characteristic value ("PeakHighFrequency" and "RmsHighFrequency") for the entire module.

Bit	Description
15-4	Reserved = 0
3-0	High-pass configuration for the entire module **Value** / **Description** 15 - 3: Invalid 2: 500 Hz 1: 1000 Hz 0: 2000 Hz

Table 614: HighFrequencyConfig01

4.26.4.5.6.9 HighFrequencyConfig01Read

Register for reading the high-pass configuration for the envelope and high-frequency characteristic value ("PeakHighFrequency" and "RmsHighFrequency") of the module.

4.26.4.5.6.10 MaxFrequencyEnvelope01

This register defines the maximum channel frequency. Reducing the maximum frequency allows the frequency resolution in the spectrum to be increased.

Bit	Description
15-12	Maximum frequency for channel 4. For possible values, see channel 1.
11-8	Maximum frequency for channel 3. For possible values, see channel 1.
7-4	Maximum frequency for channel 2. For possible values, see channel 1.
3-0	Maximum frequency for channel 1 **Value** / **Description** 15 - 4: Invalid 3: 200 Hz 2: 500 Hz 1: 1000 Hz 0: 2000 Hz

Table 615: MaxFrequencyEnvelope01

Maximum frequency	Sample frequency	Duration of measurement	Frequency resolution in the frequency spectrum
2000 Hz	5156 Hz	1.5888 s	0.6294 Hz
1000 Hz	2578 Hz	3.1775 s	0.3147 Hz
500 Hz	1289 Hz	6.3550 s	0.1574 Hz
200 Hz	516 Hz	15.8875 s	0.0629 Hz

Table 616: Overview of the maximum frequency of the envelope signal

Important information for configuring the maximum frequency

- The frequency domain must be larger than the damage frequency. Otherwise, it must be kept as small as possible in order to obtain a good resolution.
- When using broad values (e.g. PeakRaw), only the largest peak value is returned during a measurement. Using a longer measurement time at a lower frequency can lead to the measured value being overlooked in some applications.
- The maximum frequency influences the size of the sample frequency and can be configured using the "Analog input" function.

4.26.4.5.6.11 MaxFrequencyEnvelope01Read

This register is used to read the configured maximum frequency for the individual channels' envelope signal.

4.26.4.5.6.12 MaxFrequencyRaw01

This register defines the maximum channel frequency. Reducing the maximum frequency allows the frequency resolution in the spectrum to be increased.

Bit	Description
15-12	Maximum frequency for channel 4. For possible values, see channel 1.
11-8	Maximum frequency for channel 3. For possible values, see channel 1.
7-4	Maximum frequency for channel 2. For possible values, see channel 1.
3-0	Maximum frequency for channel 1

Value	Description
15 - 6	Invalid
5	200 Hz
4	500 Hz
3	1000 Hz
2	2000 Hz
1	5000 Hz
0	10000 Hz

Table 617: MaxFrequencyRaw01

Maximum frequency	Sample frequency	Duration of measurement	Frequency resolution in the frequency spectrum
10000 Hz	25781 Hz	0.3178 s	3.1471 Hz
5000 Hz	12891 Hz	0.6355 s	1.5736 Hz
2000 Hz	5156 Hz	1.5888 s	0.6294 Hz
1000 Hz	2578 Hz	3.1775 s	0.3147 Hz
500 Hz	1289 Hz	6.3550 s	0.1574 Hz
200 Hz	516 Hz	15.8875 s	0.0629 Hz

Table 618: Overview of the maximum frequency of the raw signal

Important information for configuring the maximum frequency

- The frequency domain must be larger than the damage frequency. Otherwise, it must be kept as small as possible in order to obtain a good resolution.
- When using broad values (e.g. PeakRaw), only the largest peak value is returned during a measurement. Using a longer measurement time at a lower frequency can lead to the measured value being overlooked in some applications.
- The maximum frequency influences the size of the sample frequency and can be configured using the "Analog input" function.

4.26.4.5.6.13 MaxFrequencyRaw01Read

This register is used to read the configured maximum frequency for the raw signal of individual channels.

4.26.4.5.6.14 MinFrequencyEnvelope01

This register is used to configure the lowest frequency of the envelope signal still awaiting evaluation for the individual channels.

This configuration only needs to be set for channels whose EnableVelocityCalculation bit has been set (configured in the "SensorConfig01" register). Otherwise, the following minimum values based on the maximum frequency ("MaxFrequencyEnvelope") are used:

Maximum frequency	Frequency resolution in the frequency spectrum	Minimum frequency
2000 Hz	0.6294 Hz	1.888 Hz
1000 Hz	0.3147 Hz	0.944 Hz
500 Hz	0.1574 Hz	0.472 Hz
200 Hz	0.0629 Hz	0.188 Hz

Table 619: Minimum MinFrequencyEnvelope based on MaxFrequencyEnvelope

If the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) is set for the respective channel, then the following configuration applies:

Bit	Description
15-12	Minimum frequency for channel 4. For possible values, see channel 1.
11-8	Minimum frequency for channel 3. For possible values, see channel 1.
7-4	Minimum frequency for channel 2. For possible values, see channel 1.
3-0	Minimum frequency for channel 1 **Value** / **Description** 15 - 5: Invalid 4: 0.5 Hz 3: 1 Hz 2: 2 Hz 1: 5 Hz 0: 10 Hz

Table 620: MinFrequencyEnvelope01

Information:

If a channel's frequency is set lower than the minimum frequency, then the channel will be limited to this lower frequency.

4.26.4.5.6.15 MinFrequencyEnvelope01Read

This register is used to read the lowest frequency of the envelope signal still awaiting evaluation for the individual channels.

Bit	Description
15-12	Minimum frequency for channel 4. For possible values, see channel 1.
11-8	Minimum frequency for channel 3. For possible values, see channel 1.
7-4	Minimum frequency for channel 2. For possible values, see channel 1.
3-0	Minimum frequency for channel 1 **Value** / **Description** 15: Limited to minimum frequency 14 - 5: Invalid 4: 0.5 Hz 3: 1 Hz 2: 2 Hz 1: 5 Hz 0: 10 Hz

Table 621: MinFrequencyEnvelope01

4.26.4.5.6.16 MinFrequencyRaw01

This register is used to configure the lowest frequency of the raw signal still awaiting evaluation for the individual channels.

This configuration only needs to be set for channels whose EnableVelocityCalculation bit has been set (configured in the "SensorConfig01" register). Otherwise the following minimum values, based on the maximum frequency, ("MaxFrequencyRaw") are used:

Maximum frequency	Frequency resolution in the frequency spectrum	Minimum frequency
10000 Hz	3.1471 Hz	9.441 Hz
5000 Hz	1.5736 Hz	4.720 Hz
2000 Hz	0.6294 Hz	1.888 Hz
1000 Hz	0.3147 Hz	0.944 Hz
500 Hz	0.1574 Hz	0.472 Hz
200 Hz	0.0629 Hz	0.188 Hz

Table 622: Minimum MinFrequencyRaw based on MaxFrequencyRaw

If the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) is set for the respective channel, then the following configuration applies:

Bit	Description
15-12	Minimum frequency for Channel 4. For possible values, see channel 1.
11-8	Minimum frequency for Channel 3. For possible values, see channel 1.
7-4	Minimum frequency for Channel 2. For possible values, see channel 1.
3-0	Minimum frequency for channel 1 **Value** – **Description** 15 - 5 – Invalid 4 – 0.5 Hz 3 – 1 Hz 2 – 2 Hz 1 – 5 Hz 0 – 10 Hz

Table 623: MinFrequencyRaw01

Information:

If a channel's frequency is set lower than the minimum frequency, then the channel will be limited to this lower frequency.

4.26.4.5.6.17 MinFrequencyRaw01Read

This register is used to read the lowest frequency of the raw signal still awaiting evaluation for the individual channels.

Bit	Description
15-12	Minimum frequency for Channel 4. For possible values, see channel 1.
11-8	Minimum frequency for Channel 3. For possible values, see channel 1.
7-4	Minimum frequency for Channel 2. For possible values, see channel 1.
3-0	Minimum frequency for channel 1 **Value** – **Description** 15 – Limited to minimum frequency 14 - 5 – Invalid 4 – 0.5 Hz 3 – 1 Hz 2 – 2 Hz 1 – 5 Hz 0 – 10 Hz

Table 624: MinFrequencyRaw01Read

4.26.4.5.6.18 OverflowAnalogInput01-04

Indicates whether a signal is pending on the input that is greater than the configured "AnalogInputScale01".

Information:

This is always based on a 100 mV/g sensor.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.19 OverflowCharacteristicValues01-04

This register contains an overflow indicator bit for each characteristic value of the respective channel (1 = Overflow).

Bit	Description
15	Reserved (always 0)
14	RmsRaw overflow
13	Iso10816 overflow
12	Vdi3832KtRaw overflow
11	KurtosisRaw overflow
10	SkewnessRaw overflow
9	CrestFactorRaw overflow
8	PeakRaw overflow
7	RmsVelRaw overflow
6	RmsAccRaw overflow
5	RmsVelEnvelope overflow
4	RmsAccEnvelope overflow
3	Vdi3832KtHighFrequency overflow
2	CrestFactorHighFrequency overflow
1	RmsHighFrequency overflow
0	PeakHighFrequency overflow

Table 625: OverflowCharacteristicsValues01-04

This register is only available in Function model 0 - Standard.

4.26.4.5.6.20 OverflowFrequencyBands01

This register contains an overflow indicator bit for each frequency band (1 = overflow).

Bit	Description
31	FrequencyBand32 overflow
...	...
0	FrequencyBand01 overflow

Table 626: OverflowFrequencyBands01

This register is only available in Function model 0 - Standard.

4.26.4.5.6.21 PeakHighFrequencyRef01-04

Reference (correct state) of the high frequency signal's peak value for calculating the Vdi3832 K(t) of the high frequency signal.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.22 PeakHighFrequencyRefCalculated01-04

Reference (correct state) of the high frequency signal's peak value that was used to calculate the Vdi3832 K(t) of the peak value.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.23 PeakRawRef01-04

Reference (correct state) of the raw signal's peak value used to calculate the Vdi3832 K(t) of the raw signal.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.24 PeakRawRefCalculated01-04

Reference (correct state) of the raw signal's peak value that was used to calculate the Vdi3832 K(t) of the raw signal.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.25 RmsHighFrequencyRef01-04

Reference (correct state) of the high frequency signal's root mean square used to calculate the Vdi3832 K(t) of the high frequency signal.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.26 RmsHighFrequencyRefCalculated01-04

Reference (correct state) of the high frequency signal's root mean square that was used to calculating the Vdi3832 K(t) of the high frequency signal.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.27 RmsRawRef01-04

Reference (correct state) of the raw signal's root mean square for calculating the Vdi3832 K(t) of the raw signal.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.28 RmsRawRefCalculated01-04

Reference (correct state) of the raw signal's root mean square that was used to calculate the Vdi3832 K(t) of the raw signal.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.29 SensitivitySensor01-04

The X20CM4810 always calculates the characteristic values based on a 100 mV/g sensor on the input. Other sensors can be used by specifying the sensor resolution in mV/g for each channel on these data points. All cyclical characteristic values are then automatically scaled to the correct sensor resolution by Automation Runtime. If this parameter is changed, then the next measurement indicated by "DataToggleBit01" is invalid.

This register is only available in Function model 0 - Standard.

4.26.4.5.6.30 SensorConfig01

This register can be used to enable or disable the IEPE sensor supply for individual channels.

Bit	Description
15	1 = Function model 1 - Fast master 0 = Function model 2 - Slow master and Function model 254 - Bus controller
14	Buffer length (0 = 8192 bytes, 1 = 65535 bytes)
13-12	Reserved = 0
11	EnableVelocityCalculation for channel 4
10	EnableVelocityCalculation for channel 3
9	EnableVelocityCalculation for channel 2
8	EnableVelocityCalculation for channel 1
7-4	Reserved = 0
3	IEPE supply for channel 4 (0 = Off, 1 = On)
2	IEPE supply for channel 3 (0 = Off, 1 = On)
1	IEPE supply for channel 2 (0 = Off, 1 = On)
0	IEPE supply for channel 1 (0 = Off, 1 = On)

Table 627: SensorConfig01

EnableVelocityCalculation

This bit can be used to enable the calculation of all characteristic values calculated on the velocity spectrum (1 = Calculation enabled).
If this calculation is not enabled, 0 is output for all characteristic values calculated on the velocity spectrum.
To maximize the precision of the characteristic values based on the acceleration spectrum, it is recommended to only enable this bit if the velocity signals are absolutely required.

4.26.4.5.6.31 SensorConfig01Read

Register for reading the current "SensorConfig01" configuration.

4.26.4.5.6.32 Status01

General status register for the X20CM4810:

Bit	Description
15-13	Reserved
12	AnalogInputToggleBit04 toggles with each new calculation and each new input value from AnalogInput04.
11	AnalogInputToggleBit03 toggles with each new calculation and each new input value from AnalogInput03.
10	AnalogInputToggleBit02 toggles with each new calculation and each new input value from AnalogInput02.
9	AnalogInputToggleBit01 toggles with each new calculation and each new input value from AnalogInput01.
8	Overflow04 indicates an overflow of one or more characteristic values calculated on channel 4 (1 = Overflow).
7	Overflow03 indicates an overflow of one or more characteristic values calculated on channel 3 (1 = Overflow).
6	Overflow02 indicates an overflow of one or more characteristic values calculated on channel 2 (1 = Overflow).
5	Overflow01 indicates an overflow of one or more characteristic values calculated on channel 1 (1 = Overflow).
4	BufferLockValid01 and DataLockValid01 confirm RequestBufferLock01 and RequestDataLock01 (1 = Data locked, consistent and valid).
3	BrokenWire04 indicates an open line on channel 4 (1 = Open line).
2	BrokenWire03 indicates an open line on channel 3 (1 = Open line).
1	BrokenWire02 indicates an open line on channel 2 (1 = Open line).
0	BrokenWire01 indicates an open line on channel 1 (1 = Open line).

Table 628: Status01

4.26.4.5.7 Module registers - Characteristic values (acyclic)

The following applies to all characteristic value module registers:

- These registers are only available in Function model 2 - Slow master and Function model 254 - Bus controller.
- All calculated characteristic values can be locked using RequestDataLock01, which allows all registers to be read in a consistent manner.

4.26.4.5.7.1 CrestFactorRaw01-04

Asynchronous register for reading the characteristic value "CrestFactorRaw" of the respective channel.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

Format	Resolution and unit	Value on overflow
24-bit unsigned	0.001	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	1

4.26.4.5.7.2 FrequencyBand01-32

Asynchronous register to read the respective frequency band. See section 4.26.4.2.9 "Frequency bands" on page 2601.

If the frequency band parameter is set to a velocity signal, then this value is only calculated if the EnableVelocity-Calculation bit (configured in the "SensorConfig01" register) for the respective channel is set; otherwise, 0 is output.

Format	Resolution and unit	Value on overflow
24-bit unsigned	0.001 g or 0.001 mm/s depending on the configuration	16777215
24-bit unsigned	1/65536 g or 1/65536 mm/s depending on the configuration	16777215

Parameter after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mg or mm/s depending on the configuration

4.26.4.5.7.3 Iso10816_01-04

Asynchronous register for reading the characteristic value "ISO10816" of the respective channel.

Format	Resolution and unit	Value on overflow
24-bit unsigned	0.001 mm/s	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mm/s

4.26.4.5.7.4 KurtosisRaw01-04

Asynchronous register for reading the characteristic value "KurtosisRaw" of the respective channel.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

Format	Resolution and unit	Value on overflow
24-bit signed	0.001	8388607

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	1

4.26.4.5.7.5 PeakHighFrequency01-04

Asynchronous register for reading the characteristic value "PeakHighFrequency" of the respective channel.

Format	Resolution and unit	Value on overflow
24-bit unsigned	1/65536 g	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mg

4.26.4.5.7.6 PeakRaw01-04

Asynchronous register for reading the characteristic value "PeakRaw" of the respective channel.

Format	Resolution and unit	Value on overflow
24-bit unsigned	1/65536 g	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mg

4.26.4.5.7.7 RmsAccEnvelope01-04

Asynchronous register for reading the characteristic value "RmsAccEnvelope" of the respective channel.

Format	Resolution and unit	Value on overflow
24-bit unsigned	0.001 g	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mg

4.26.4.5.7.8 RmsAccRaw01-04

Asynchronous register for reading the characteristic value "RmsAccRaw" of the respective channel.

Format	Resolution and unit	Value on overflow
24-bit unsigned	0.001 g	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mg

4.26.4.5.7.9 RmsHighFrequency01-04

Asynchronous register for reading the characteristic value "RmsHighFrequency" of the respective channel.

Format	Resolution and unit	Value on overflow
24-bit unsigned	1/65536 g	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mg

4.26.4.5.7.10 RmsRaw01-04

Asynchronous register for reading the characteristic value "RmsRaw" of the respective channel.

Format	Resolution and unit	Value on overflow
24-bit unsigned	1/65536 g	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mg

4.26.4.5.7.11 RmsVelEnvelope01-04

Asynchronous register for reading the characteristic value "RmsVelEnvelope" of the respective channel.

This value is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

Format	Resolution and unit	Value on overflow
24-bit unsigned	0.001 mm/s	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mm/s

4.26.4.5.7.12 RmsVelRaw01-04

Asynchronous register for reading the characteristic value "RmsVelRaw" of the respective channel.

This value is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

Format	Resolution and unit	Value on overflow
24-bit unsigned	0.001 mm/s	16777215

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	mm/s

4.26.4.5.7.13 SkewnessRaw01-04

Asynchronous register for reading the characteristic value "SkewnessRaw" of the respective channel.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

Format	Resolution and unit	Value on overflow
24-bit signed	0.001	8388607

Characteristic value after preparation by Automation Runtime in Function model 0 - Standard

Format	Unit
REAL	1

4.26.4.5.8 Module registers - Minimum and maximum values

The characteristic values of the X20CM4810 are recalculated every 300 ms. To prevent values from being lost, it is necessary to collect this data quickly enough. If this is not possible, the characteristic values on the module can be locked using the RequestDataLock01 data point and then read asynchronously in Function model 2 - Slow master and Function model 254 - Bus controller. However, this method results in measurements being lost.

To prevent measurements from being lost, a special function has been implemented in the X20CM4810 that records the minimum and maximum values of all characteristic values calculated in the module. When an edge of the MinMaxUpdate01 data point occurs, a new measurement can be started whereby the minimum and maximum values are reinitialized. The current data is copied to the asynchronous register at the same time.

The number of collected measurements can then be read using the asynchronous data point "MinMaxCounter01". The respective values are read using the asynchronous minimum and maximum data points.

Example

For *Iso10816*, these are the *Iso10816Min01-04* and *Iso10816Max01-04 registers*.

Information:

- **If data is locked with RequestDataLock01, no further measurement values are collected. This only affects Function model 2 - Slow master and Function model 254 - Bus controller since the characteristic values are not locked in the standard function model.**
- **If a characteristic value overflow or open line occurs, no new values are collected.**
- **The minimum and maximum data points are each initialized using the maximum and minimum of the respective data type (see 4.26.4.2.11 "Characteristic value format" on page 2602). If there is no valid value on the characteristic value for the overall measurement, then the initial value is retained (e.g. on overflow, open line or locked data).**
- **If the data on the module is locked (DataLockValid01 = 1), then no new values are added when determining the minimum. The measurement cycles are still counted, however.**

Registers are only updated at an edge from "MinMaxUpdate01" and are only valid if "MinMaxCounter01" is not equal to 0. The asynchronous register "MinMaxCounter01" specifies the collected measurement cycles for the minimum and maximum.

4.26.4.5.8.1 CrestFactorRawMax01-04

Asynchronous maximum value of the "CrestFactorRaw" characteristic value of the respective channel in thousandths.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.2 CrestFactorRawMin01-04

Asynchronous minimum value of the "CrestFactorRaw" characteristic value of the respective channel in thousandths.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.3 FrequencyBandMax01-32

Asynchronous maximum value of the respective frequency band in thousandths of a mm/s or g depending on the configuration. See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 and 4.26.4.2.9 "Frequency bands" on page 2601 for additional information.

If the frequency band parameter is set to a velocity signal, then this value is only calculated if the EnableVelocity-Calculation bit (configured in the "SensorConfig01" register) for the respective channel is set; otherwise, 0 is output.

4.26.4.5.8.4 FrequencyBandMin01-32

Asynchronous minimum value of the respective frequency band in thousandths of a mm/s or g depending on the configuration. See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 and 4.26.4.2.9 "Frequency bands" on page 2601 for additional information.

If the frequency band parameter is set to a velocity signal, then this value is only calculated if the EnableVelocity-Calculation bit (configured in the "SensorConfig01" register) for the respective channel is set; otherwise, 0 is output.

4.26.4.5.8.5 Iso10816Max01-04

Asynchronous maximum value of the "ISO10816" characteristic value of the respective channel in thousandths of a mm/s. See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.6 Iso10816Min01-04

Asynchronous minimum value of the "ISO10816" characteristic value of the respective channel in thousandths of a mm/s. See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.7 KurtosisRawMax01-04

Asynchronous maximum value of the "KurtosisRaw" characteristic value of the respective channel in thousandths.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.8 KurtosisRawMin01-04

Asynchronous minimum value of the "KurtosisRaw" characteristic value of the respective channel in thousandths.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.9 MinMaxCounter01

This asynchronous register specifies how many measurements were collected the last time the minimum and maximum were determined. It is only updated when an edge occurs for MinMaxUpdate01. If the MinMaxUpdate01 bit is not toggled after 65535 measurements, then the counter is limited to 65535. Determination of the minimum and maximum continues, however. All asynchronous minimum and maximum values are only valid if "MinMax-Counter01" is not equal to 0.

4.26.4.5.8.10 PeakHighFrequencyMax01-04

Asynchronous maximum value of the "PeakHighFrequency" characteristic value of the respective channel in 1/65536 g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.11 PeakHighFrequencyMin01-04

Asynchronous minimum value of the "PeakHighFrequency" characteristic value of the respective channel in 1/65536 g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.12 PeakRawMax01-04

Asynchronous maximum value of the "PeakRaw" characteristic value of the respective channel in 1/65536 g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.13 PeakRawMin01-04

Asynchronous minimum value of the "PeakRaw" characteristic value of the respective channel in 1/65536 g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.14 RmsAccEnvelopeMax01-04

Asynchronous maximum value of the "RmsAccEnvelope" characteristic value of the respective channel in thousandths of a g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.15 RmsAccEnvelopeMin01-04

Asynchronous minimum value of the "RmsAccEnvelope" characteristic value of the respective channel in thousandths of a g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.16 RmsAccRawMax01-04

Asynchronous maximum value of the "RmsAccRaw" characteristic value of the respective channel in thousandths of a g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.17 RmsAccRawMin01-04

Asynchronous minimum value of the "RmsAccRaw" characteristic value of the respective channel in thousandths of a g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.18 RmsHighFrequencyMax01-04

Asynchronous maximum value of the "RmsHighFrequency" characteristic value of the respective channel in 1/65536 g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.19 RmsHighFrequencyMin01-04

Asynchronous minimum value of the "RmsHighFrequency" characteristic value of the respective channel in 1/65536 g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.20 RmsRawMax01-04

Asynchronous maximum value of the "RmsRaw" characteristic value of the respective channel in 1/65536 g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.21 RmsRawMin01-04

Asynchronous minimum value of the "RmsRaw" characteristic value of the respective channel in 1/65536 g. See also 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.22 RmsVelEnvelopeMax01-04

Asynchronous maximum value of the "RmsVelEnvelope" characteristic value of the respective channel in thousandths of a mm/s. See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

This value is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

4.26.4.5.8.23 RmsVelEnvelopeMin01-04

Asynchronous minimum value of the "RmsVelEnvelope" characteristic value of the respective channel in thousandths of a mm/s. See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

This value is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

4.26.4.5.8.24 RmsVelRawMin01-04

Asynchronous minimum value of the "RmsVelRaw" characteristic value of the respective channel in thousandths of a mm/s. See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

This value is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

4.26.4.5.8.25 RmsVelRawMax01-04

Asynchronous maximum value of the "RmsVelRaw" characteristic value of the respective channel in thousandths of a mm/s. See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

This value is only calculated if the EnableVelocityCalculation bit (configured in the "SensorConfig01" register) of the respective channel is set; otherwise, 0 is output.

4.26.4.5.8.26 SkewnessRawMax01-04

Asynchronous maximum value of the "SkewnessRaw" characteristic value of the respective channel in thousandths.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.8.27 SkewnessRawMin01-04

Asynchronous minimum value of the "SkewnessRaw" characteristic value of the respective channel in thousandths.

Since division by the RMS value takes place in the module ("RmsRaw"), there may be an overflow if the RMS value is very small. To prevent this, the module has an internal lower limit of 1 mg for the RMS value.

See also section 4.26.4.5.8 "Module registers - Minimum and maximum values" on page 2705 for additional information.

4.26.4.5.9 Maximum cycle time

The maximum cycle time defines how far the cycle time of the X2X Link can be increased without causing a communication error or impaired functionality.

Maximum cycle time	
Function model 0 - Standard	10 ms
Function model 1 - Fast master	10 ms
Function model 2 - Slow master	-
Function model 254 - Bus controller	-

Table 629: X20CM4810 - Maximum cycle time

4.26.4.5.10 Minimum cycle time

The minimum cycle time defines how far the cycle time of the X2X Link can be reduced without causing a communication error or impaired functionality. It is important to note that very fast cycles leave less idle time for monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Function model 0 - Standard	400 µs
Function model 1 - Fast master	400 µs
Function model 2 - Slow master	400 µs
Function model 254 - Bus controller	400 µs

Table 630: X20CM4810 - Minimum cycle time

4.26.4.6 FlatStream

4.26.4.6.1 FlatStream communication

4.26.4.6.1.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transfer adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

4.26.4.6.1.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.26.4.6.1.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

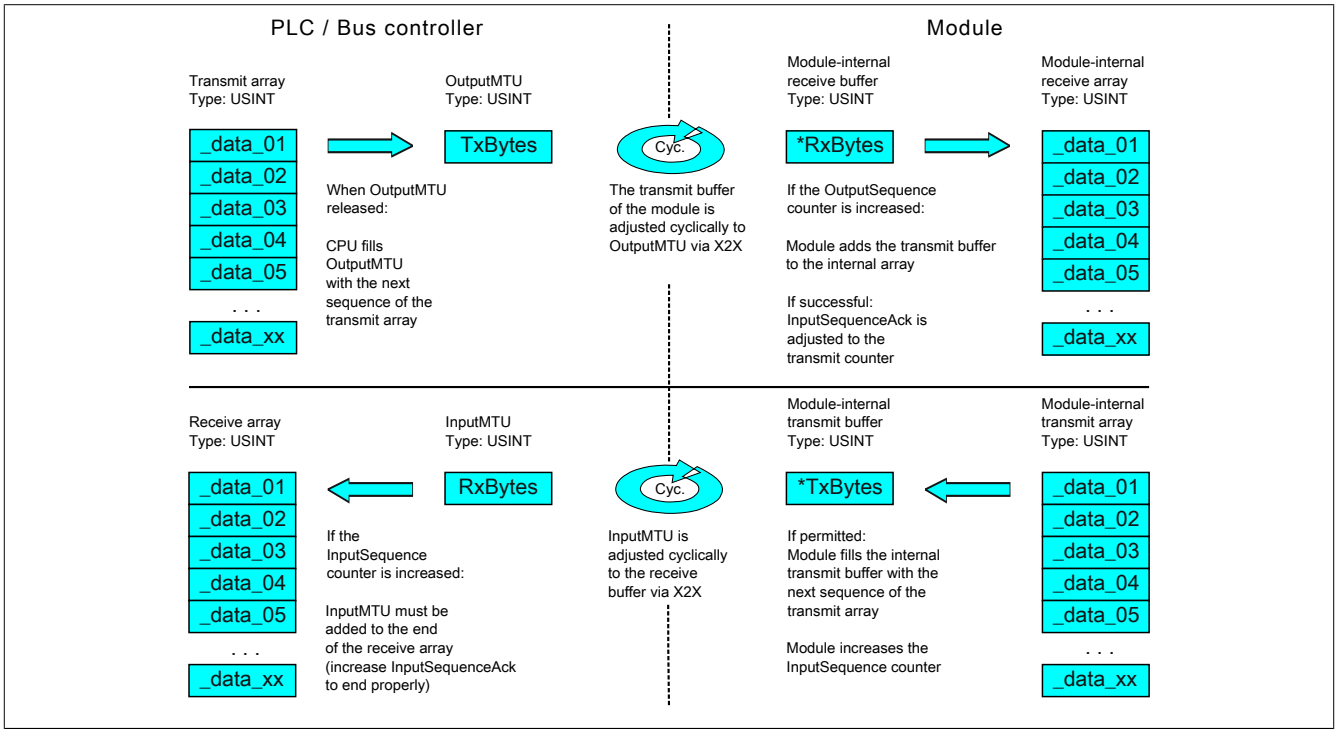


Figure 482: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.26.4.6.1.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

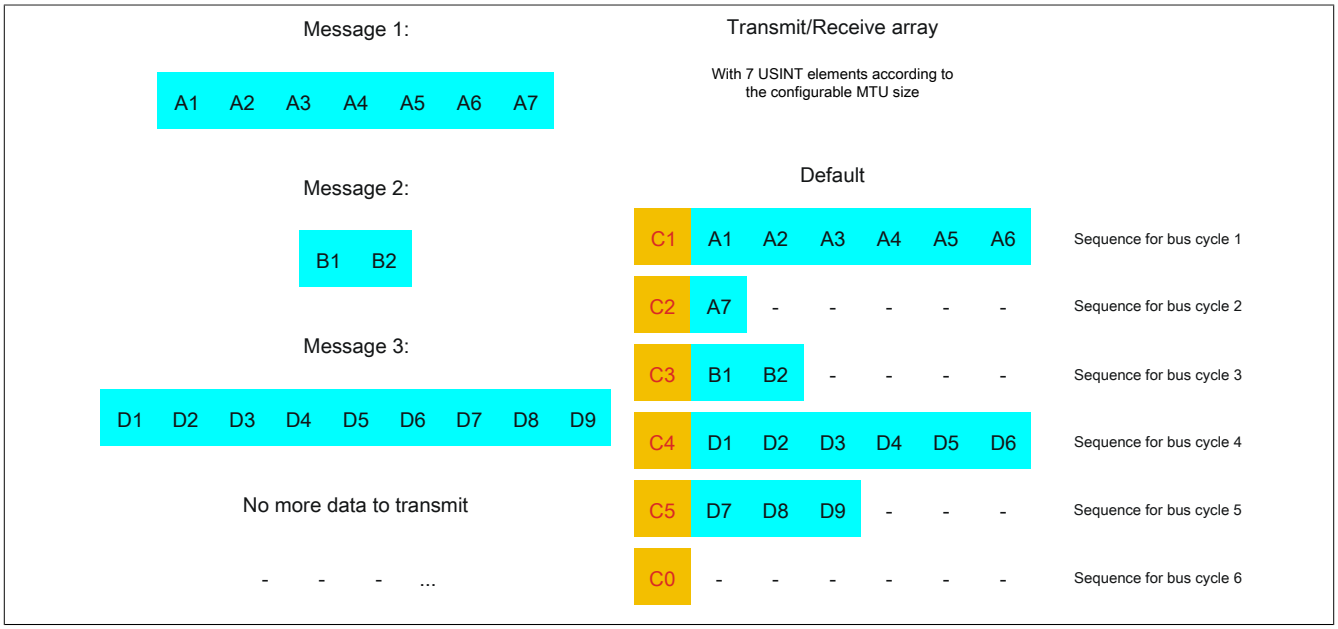


Figure 483: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			C1 (control byte 1)			C2 (control byte 2)		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 631: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			C4 (control byte 4)			C5 (control byte 5)		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 632: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

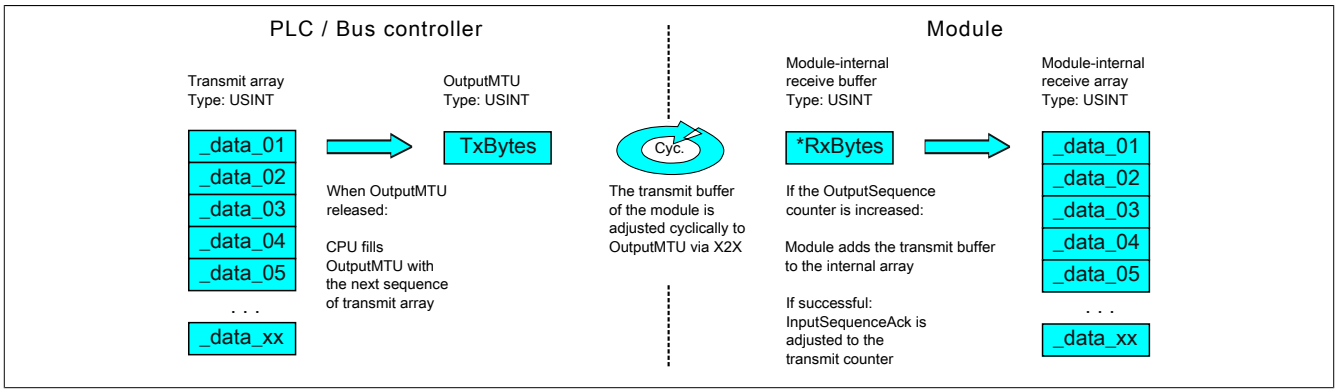


Figure 484: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

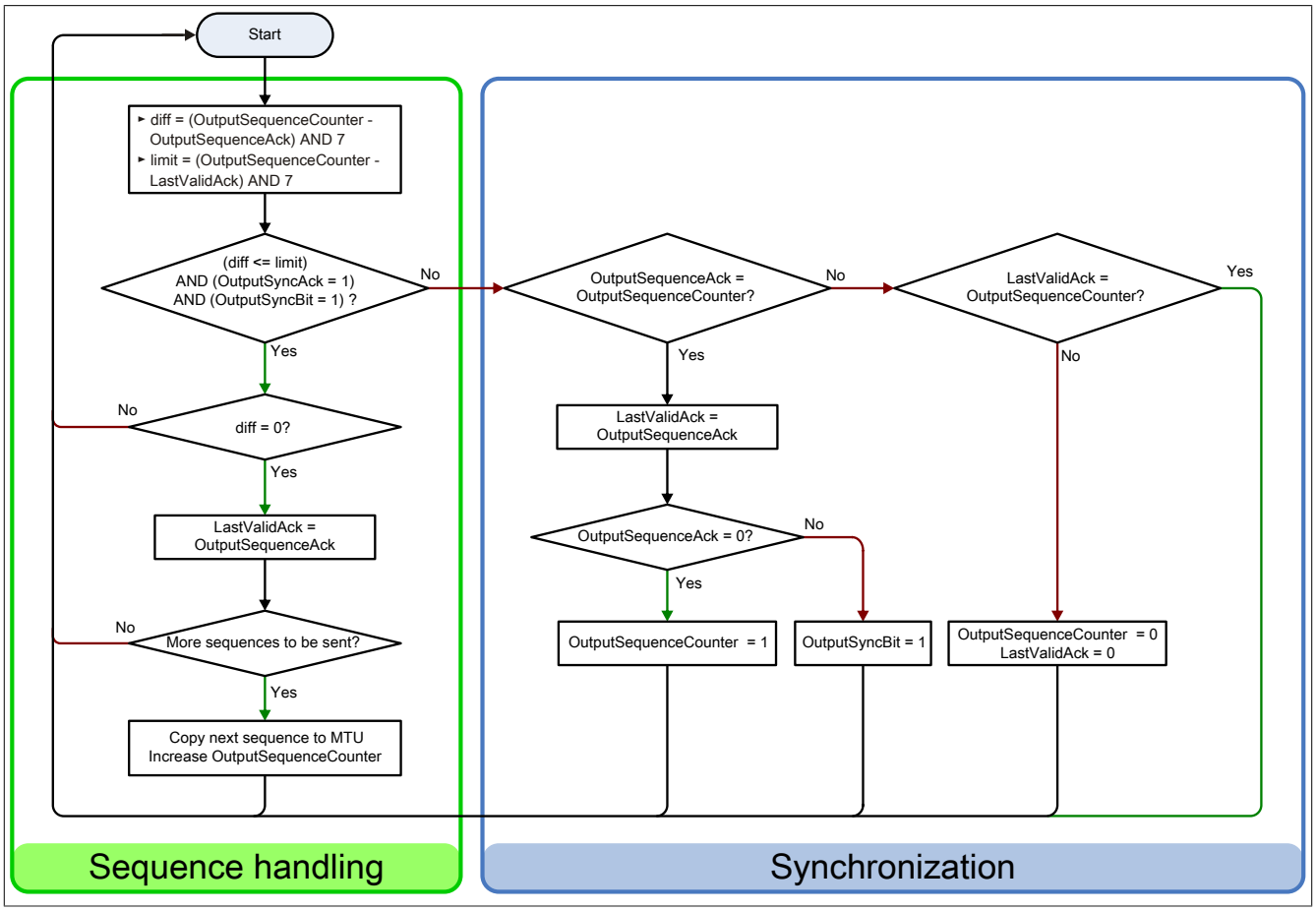


Figure 485: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

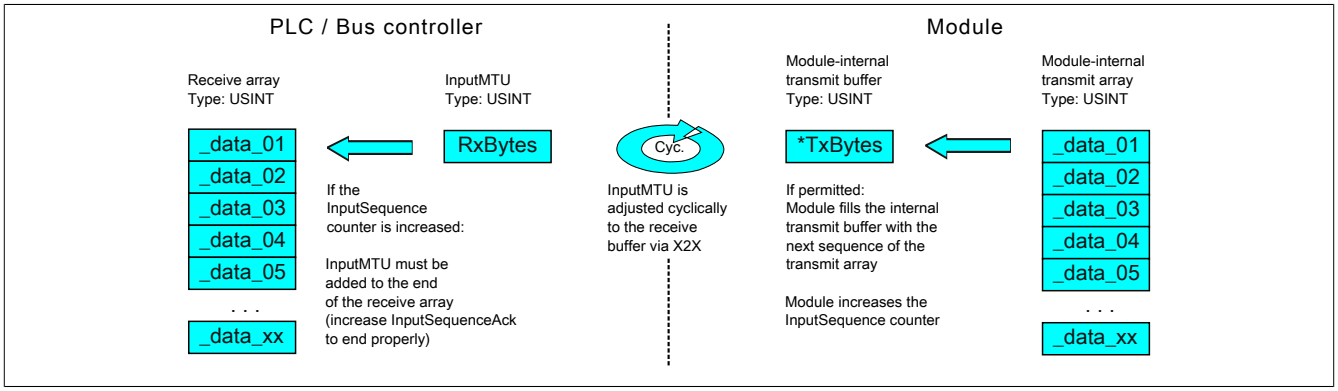


Figure 486: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

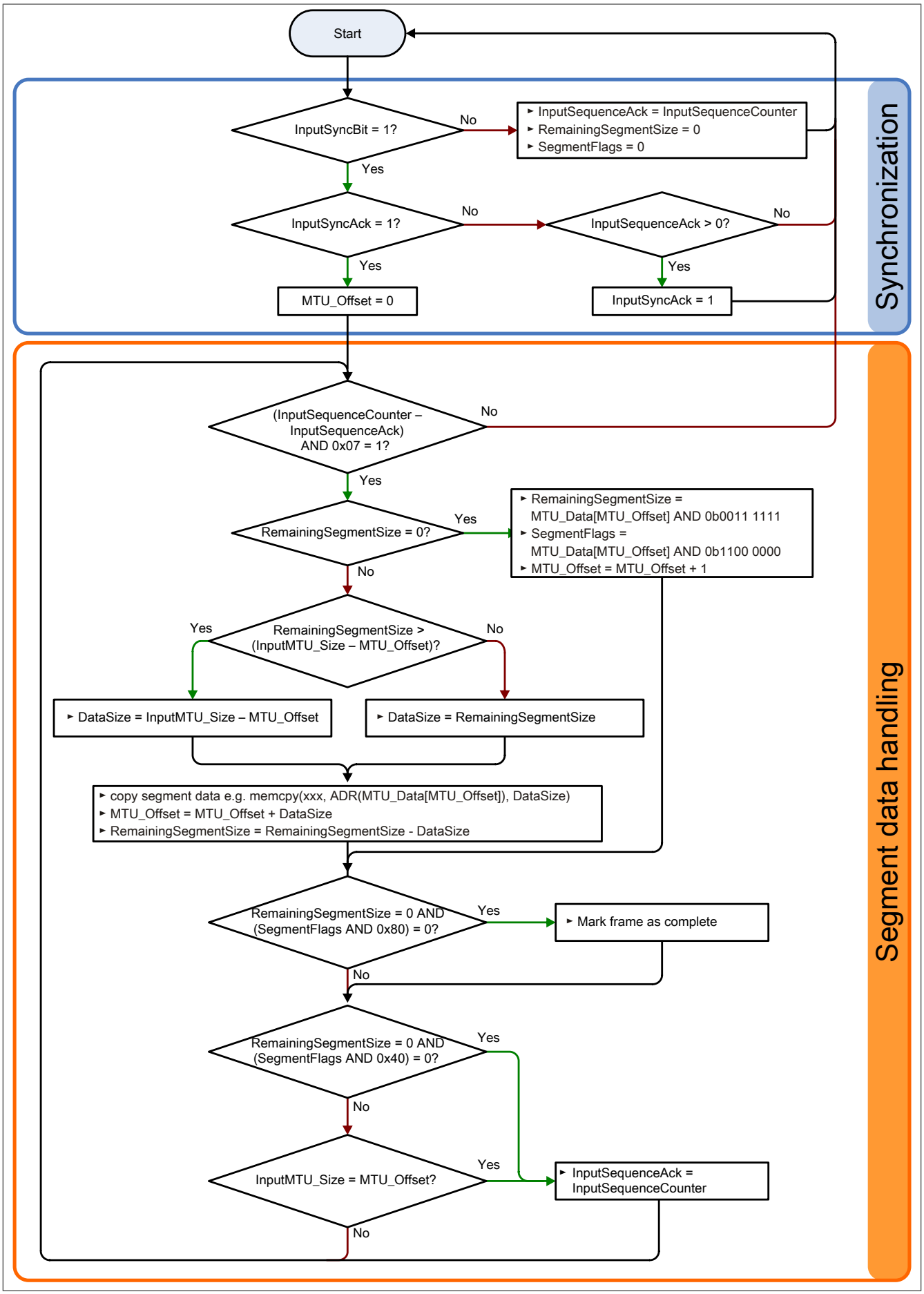


Figure 487: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode register

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name		Information
0	MultiSegmentMTU	0	Not permitted (default; can't be configured)
1	Large segments	0	Not permitted (default; can't be configured)
2-7	Reserved		

Default:
By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

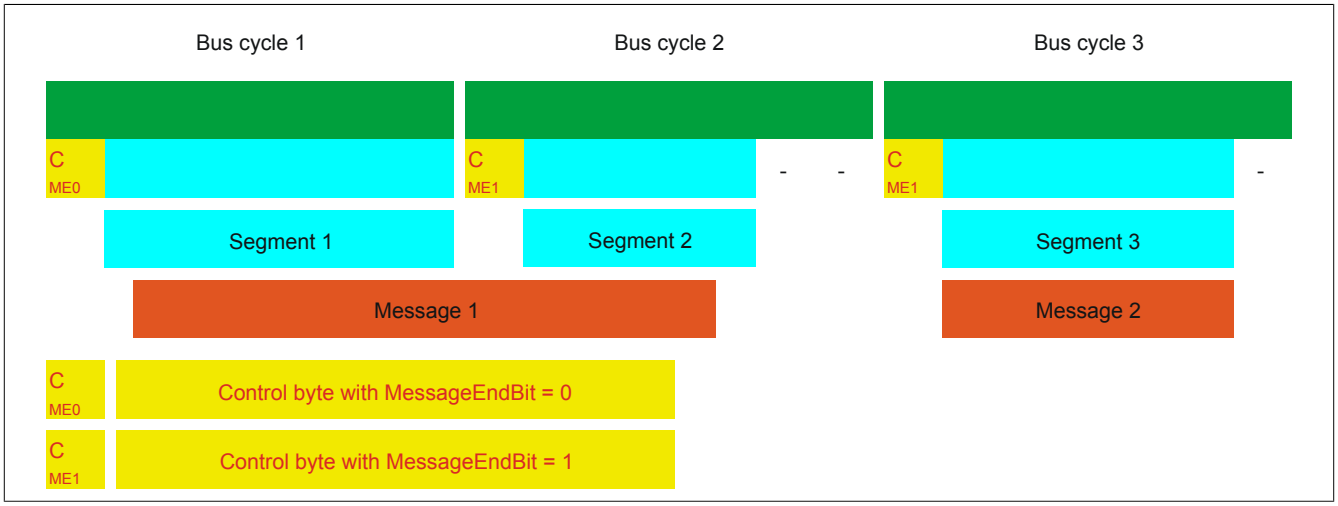


Figure 488: Message arrangement in the MTU (default)

4.26.4.6.1.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

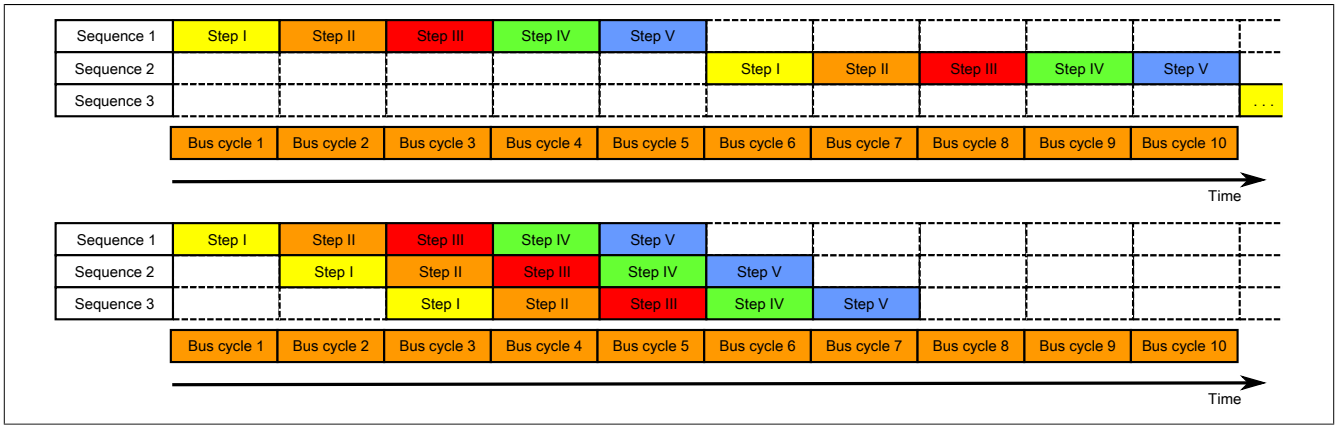


Figure 489: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration (defined by module)

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Forward:
With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	Default: 7

ForwardDelay:
The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Values [µs]
UINT	0...65535 Default: 0

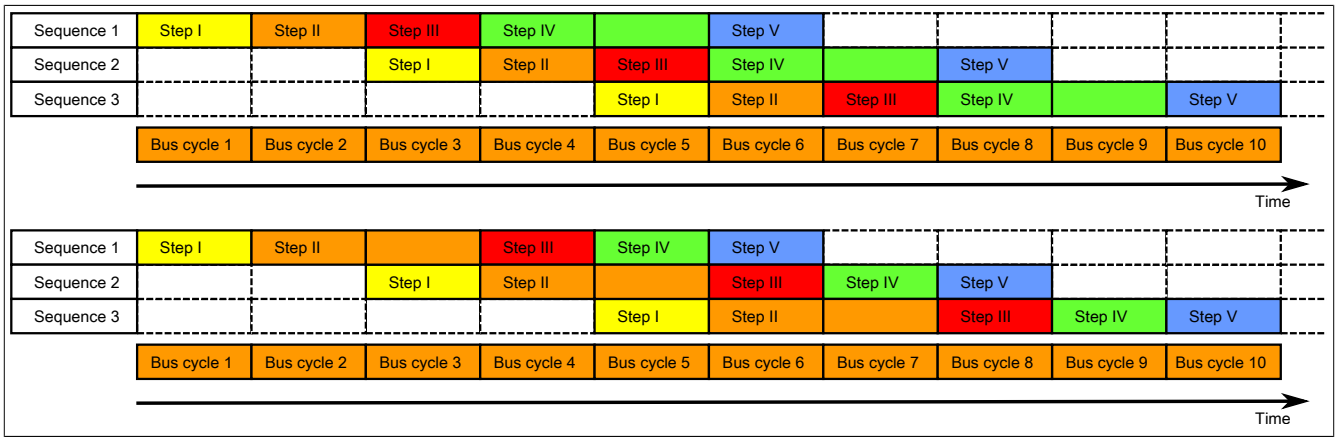


Figure 490: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting:

Cyclic status query: *- The Module monitors the OutputSequenceCounter.*
0. Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1. Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2. Transmitting: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module responds since OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array.* *- The module is acknowledged and the currently received value of the OutputSequenceCounter is transferred to OutputSequenceAck.* *- The module requests the status cyclically again.*
3. Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving:

0. Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck.* *- The module checks if InputMTU is enabled.* *→ Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array.*
Action: *- The module transmits the current part of the transmit array to the receive buffer.* *- The module increases the InputSequenceCounter.* *- The module waits for a new bus cycle.* *- The module repeats the action if the InputMTU is enabled.*
1 Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck.* *→ A sequence is only considered to have been transmitted successfully if it has been acknowledged via InputSequenceAck .*

Details/Background:

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > ## Information:
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

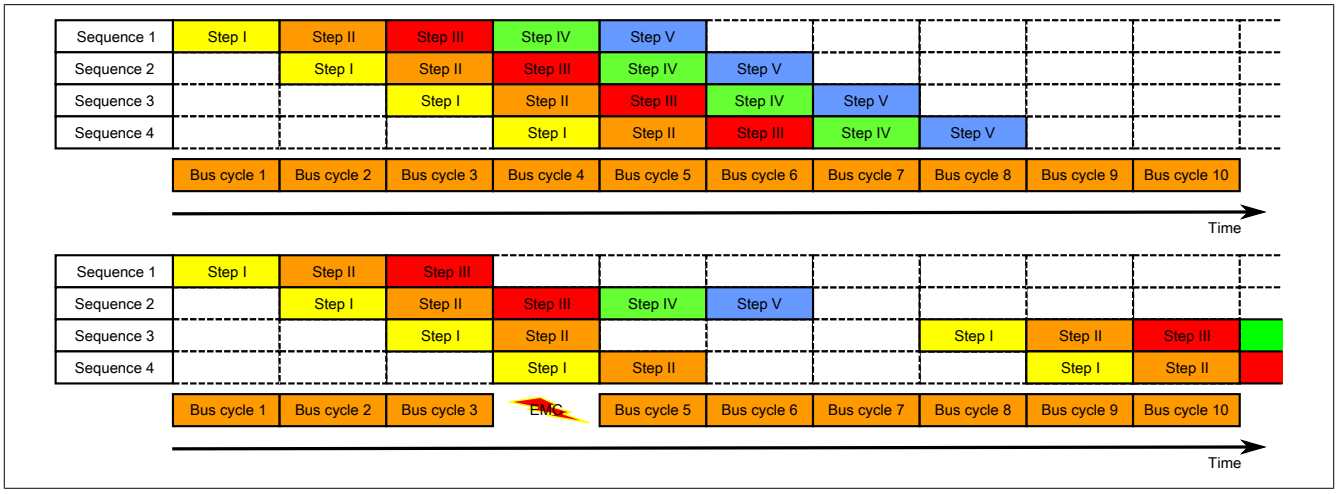


Figure 491: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

The Forward function on the X20CM4810

The ForwardDelay for BufferFlatstream can be asynchronously configured in Function model 0 - Standard and Function model 1 - Fast master in the I/O configuration of the X20CM4810 module (BufferForwardDelay01). When using the "Fast master" function model, the ForwardDelay can also be asynchronously configured for the ParameterFlatStream in the I/O configuration (ParamterForwardDelay01).

Forwarding for the parameter FlatStream and buffer FlatStream can be asynchronously adjusted (Forward01 and BufferForward01 parameters). However, it should only be adjusted after the ForwardDelay has been configured for the respective FlatStream.

When using a SG4 CPU, the ForwardDelay cannot be manually configured for the ParameterFlatStream. From version J3.09 and J4.01 of Automation Runtime, it is automatically configured and in earlier versions, it is ForwardDelay 0.

4.26.4.6.2 Transferring characteristic values via FlatStream

4.26.4.6.2.1 General information

For information about FlatStream functionality, see section 4.3.7.10.8 "FlatStream communication" on page 223.

Transferring characteristic values via FlatStream is only available on the module in Function model 0 - Standard and Function model 2 - Slow master.

Every 300 ms, the characteristic values calculated by the module are transferred automatically via the characteristic value FlatStream, but only if the previous transfer is already complete. For this reason a maximum X2X Link cycle time of 10 ms is recommended to prevent measurement data from being lost. It is also important to note that the module refreshes the data points of the characteristic value FlatStream every X2X Link cycle. Once the transmission is complete, the characteristic values from the stream need to be "reassembled" on the PLC.

Automation Runtime handles FlatStream communication when transferring characteristic values in the "Standard" function model. The user is automatically provided with all characteristic values, already properly scaled. Only the task cycle needs to be checked to make sure it is correct. As a result, the data points for the characteristic value FlatStream are not shown in the Function model 0 - Standard I/O mapping.

4.26.4.6.2.2 Registers for the characteristic value FlatStream

The following registers are needed to transfer characteristic values:

ParameterInputSequence01
ParameterRxByte01-13
ParameterOutputSequence01

This results in an InputMTU of 13 bytes and an OutputMTU of 0 bytes for the characteristic value FlatStream.

4.26.4.6.2.3 Structure of the characteristic value FlatStream

Each characteristic value transferred from the module via FlatStream has a length of 3 bytes with the high byte first. For the exact format, see section 4.26.4.2.11 "Characteristic value format" on page 2602. The stream has a total length of 240 bytes. First, all characteristic values from channel 1 are transferred, then those from channels 2, 3 and 4. The 32 frequency bands then follow next.

The RmsVelRaw and RmsVelEnvelope characteristic values and the frequency bands are only transferred if they are set to a velocity signal and the EnableVelocityCalculation bit for the respective channel is set. Otherwise, 0 is output. EnableVelocityCalculation is configured in the "SensorConfig01" register.

Byte offset in the stream				Characteristic value
Channel 1	Channel 2	Channel 3	Channel 4	
Channel parameters				
0	36	72	108	"RmsAccRaw"
3	39	75	111	"RmsVelRaw"
6	42	78	114	"RmsAccEnvelope"
9	45	81	117	RmsVelEnvelope
12	48	84	120	"PeakHighFrequency"
15	51	87	123	"RmsHighFrequency"
18	54	90	126	"ISO10816"
21	57	93	129	"CrestFactorRaw"
24	60	96	132	"KurtosisRaw"
27	63	99	135	"PeakRaw"
30	66	102	138	"SkewnessRaw"
33	69	105	141	"RmsRaw"
Frequency band 1 - 32				
144				FrequencyBand01
:				:
237				FrequencyBand32

4.26.4.6.3 Uploading buffers via FlatStream

4.26.4.6.3.1 General information

For information about FlatStream functionality, see section 4.3.7.10.8 "FlatStream communication" on page 223.

Uploading buffers via FlatStream is only available on the module in Function model 0 - Standard and Function model 1 - Fast master.

When requested (buffer FlatStream in Tx direction), the module's raw data buffers (raw signal and FFT) can be transferred via the buffer FlatStream (Rx direction). However, this is only possible if the buffers are first locked on the module with the settings RequestBufferLock01 = 1 and BufferLockValid01 = 1. It is important to note that the module refreshes the data points of the buffer FlatStream every X2X Link cycle. Once the transmission is complete, the buffer from the stream needs to be "reassembled" on the PLC.

4.26.4.6.3.2 Registers for the buffer FlatStream

The following registers are needed to upload buffers:

BufferInputSequence01
BufferRxByte01-05
BufferOutputSequence01
BufferTxByte01-04

This results in an InputMTU of 5 bytes and an OutputMTU of 4 bytes for the buffer FlatStream.

4.26.4.6.3.3 Buffer upload procedure

Before a buffer can be uploaded from the X20CM4810 module, it must first be locked on the module. This can be done by setting RequestBufferLock01 = 1. The upload can only begin once the buffers have been locked by setting BufferLockValid01 = 1. If an FFT buffer is being uploaded, it is important to check the asynchronous parameters CorrFFTRaw01-04 and CorrEnvelope01-04.

If a velocity buffer is being uploaded, it only contains values if the EnableVelocityCalculation bit is set for the respective channel; otherwise, 0 is output. The EnableVelocityCalculation bit can be configured in the "SensorConfig01" register.

A buffer first needs to be requested from the module via the buffer FlatStream (Tx direction). This means:

- BufferTxByte01: Value 0x83 (frame end and 3 byes are valid)
- BufferTxByte02: The request buffer from the module
- BufferTxByte03: High byte of the number of the values to be read (per 4-byte value)
- BufferTxByte04: Low byte of the number of the values to be read (per 4-byte value)

The sequence is subsequently increased by 1. Once the module has confirmed the sequence, it is important to set the number of valid bytes to 0 in BufferTxByte since the module would otherwise interpret this as a new request. The module can temporarily store up to 2 consecutive requests.

As soon as the module receives the request, it begins streaming the requested number of values from the specified buffer via the buffer FlatStream (Rx direction). Values are always transferred in 16.16 fixed data point format (1/65536) with the high byte first. A scaling factor is transferred first. All other values are then multiplied by this factor. With time signal buffers, the first value according to the scaling factor is always the oldest. With FFT buffers, the first value according to the scaling factor is always 0 Hz. FFT buffers are only valid from the configured MinFrequency to the configured MaxFrequency of the respective signal (raw or envelope) and the respective channel.

For the time and frequency intervals of individual values, see the "MinFrequencyRaw01" or "MinFrequencyEnvelope01" register.

RequestBufferLock01 must be set to 1 throughout the entire uploading process. Once the requested buffers have been uploaded from the module, the lock can be reset. In the module, the buffers are then once again filled with new values. After some time has passed, they can be locked and uploaded again (see register "Control01").

Buffer number (Dec)				Buffer	Max. values, 4 bytes each
Channel 1	Channel 2	Channel 3	Channel 4		
9	11	13	15	Raw signal (filtered to "MaxFrequencyRaw01")	8193[1)]
25	27	29	31	Envelope signal (filtered to "MinFrequencyEnvelope01")	8193
66	70	74	78	FFT amplitude spectrum raw velocity signal (filtered to "MaxFrequencyRaw01")	4097
67	71	75	79	FFT amplitude spectrum raw acceleration signal (filtered to "MaxFrequencyRaw01")	4097
82	86	90	94	FFT amplitude spectrum envelope velocity signal (filtered to "MinFrequencyEnvelope01")	4097
83	87	91	95	FFT amplitude spectrum envelope acceleration signal (filtered to "MinFrequencyEnvelope01")	4097

1) The first value in the buffer is the scaling factor.

In special applications it may be necessary to upload larger buffers.

In the SensorConfig01 register, a buffer length of 8192 or 65535 bytes can be configured using bit 14. This makes it possible to read the raw signal and acceleration signal (buffer number 9, 11, 13, 15, 25, 27, 29 and 31) using 65535 values, including the scaling factor, from the module. However, the FFT buffers also include 4097 values including a scaling factor and refer to the previous 8192 of the 65535 values of the raw or envelop signal.

After locking the buffer for the upload (RequestBufferLock01) until the next locking, it is necessary to wait until the longest buffer is filled again. If the buffer tries to lock again before this time elapses, it is prevented by the module until after the buffer is filled.

4.26.4.7 X20CM4810 on the fieldbus

4.26.4.7.1 Bus coupler with FieldbusDESIGNER support

Only Function model 1 - Fast master and Function model 2 - Slow master are available for this.

The X20CM4810 module is configured using FieldbusDESIGNER in Automation Studio. Implementation must be handled on the master.

4.26.4.7.2 Bus coupler without FieldbusDESIGNER support

Only Function model 2 - Slow master is available for this. Configuration and implementation must be handled on the master.

4.26.4.7.3 B&R SG4 CPU with an interface module

This combination offers the following advantages:

- Modular condition monitoring solution possible
- All characteristic values prepared by Automation Runtime (no extra work required for implementation)
- Communication with the master via the interface card

4.26.4.7.4 CANIO bus coupler

Only Function model 254 - Bus controller is available for this. Configuration and implementation must be handled on the master.

4.26.4.8 Accessories

4.26.4.8.1 Sensors

4.26.4.8.1.1 0ACS100A.00-1

Order data

Model number	Short description	Figure
	Sensors	
0ACS100A.00-1	Acceleration sensor, nominal sensitivity 100 mV/g, top exit	

Table 633: 0ACS100A.00-1 - Order data

Technical data

Product ID	0ACS100A.00-1
Sensor properties	
Natural resonance (mounted)	22 kHz (rated)
Sensitivity	100 mV/g ±10% nominal 80 Hz at 22°C
Frequency response	2 Hz to 10 kHz ±5% 0.8 Hz to 15 kHz ±3 dB
Isolation	Isolated base
Measurement range	±50 g
Cross-sensitivity	<5%
Electrical characteristics	
Electrical disturbances	Max. 0.1 mg
Broadband resolution	0.2 mg (200 µg) over 1 Hz to 15 kHz

Table 634: 0ACS100A.00-1 - Technical data

Product ID	0ACS100A.00-1
Spectral noise	10 Hz to 10 µg/Hz 100 Hz to 4 µg/Hz 1 kHz to 3 µg/Hz
Current range	0.5 mA to 8 mA
Bias voltage	10 to 12 VDC
Settling time	2 seconds
Output impedance	Max. 200 Ω
Housing isolation	>10^8 Ω at 500 V
Operating conditions	
EN 60529 protection	IP67
Environmental conditions	
Temperature Operation	 -55 to 140°C
Max. shock resistance	5000 g
Emitted interferences	EN61000-6-4:2001
Immunity to disturbances	EN61000-6-2:1999
Mechanical characteristics	
Housing Material	 Stainless steel
Weight	110 g
Measurement element	PZT piezoelectric crystal (lead zirconate titanate)
Measurement execution	compressed
Fastening torque	8 Nm
Connection plugs	M12, straight

Table 634: 0ACS100A.00-1 - Technical data

Dimensions

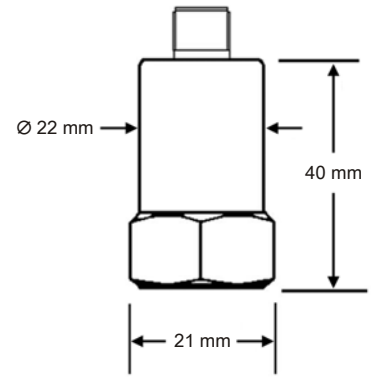


Figure 492: Dimensions - 0ACS100A.00-1

4.26.4.8.1.2 0ACS100A.90-1

Order data

Model number	Short description	Figure
	Sensors	
0ACS100A.90-1	Acceleration sensor, nominal sensitivity 100 mV/g, side exit	

Table 635: 0ACS100A.90-1 - Order data

Technical data

Product ID	0ACS100A.90-1
Sensor properties	
Natural resonance (mounted)	22 kHz (rated)
Sensitivity	100 mV/g ±10% nominal 80 Hz at 22°C
Frequency response	2 Hz to 10 kHz ±5% 0.8 Hz to 15 kHz ±3 dB
Isolation	Isolated base
Measurement range	±50 g
Cross-sensitivity	<5%
Electrical characteristics	
Electrical disturbances	Max. 0.1 mg
Broadband resolution	0.2 mg (200 µg) over 1 Hz to 15 kHz
Spectral noise	10 Hz to 10 µg/Hz 100 Hz to 4 µg/Hz 1 kHz to 3 µg/Hz
Current range	0.5 mA to 8 mA
Bias voltage	10 to 12 VDC
Settling time	2 seconds
Output impedance	Max. 200 Ω
Housing isolation	$>10^8$ Ω at 500 V
Operating conditions	
EN 60529 protection	IP67
Environmental conditions	
Temperature Operation	 -55 to 140°C
Max. shock resistance	5000 g
Emitted interferences	EN61000-6-4:2001
Immunity to disturbances	EN61000-6-2:1999
Mechanical characteristics	
Housing Material	 Stainless steel
Usable screws	M8 x 33 mm
Weight	170 g
Measurement element	PZT piezoelectric crystal (lead zirconate titanate)
Measurement execution	compressed
Fastening torque	8 Nm
Connection plugs	M12

Table 636: 0ACS100A.90-1 - Technical data

Dimensions

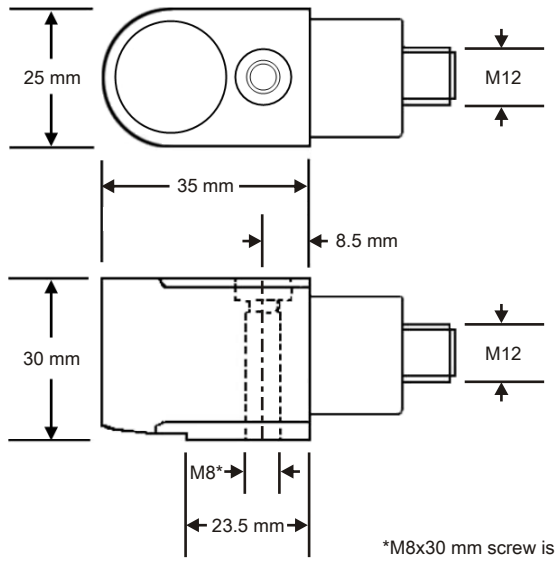
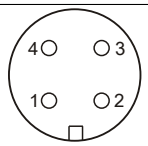


Figure 493: Dimensions - 0ACS100A.90-1

4.26.4.8.1.3 General Information

Pinout



Pin	Description
1	Not assigned
2	18 to 30 V (brown)
3	Not assigned
4	0 V (blue)

Table 637: 0ACS100A.x0-1 - Pinout

Frequency response

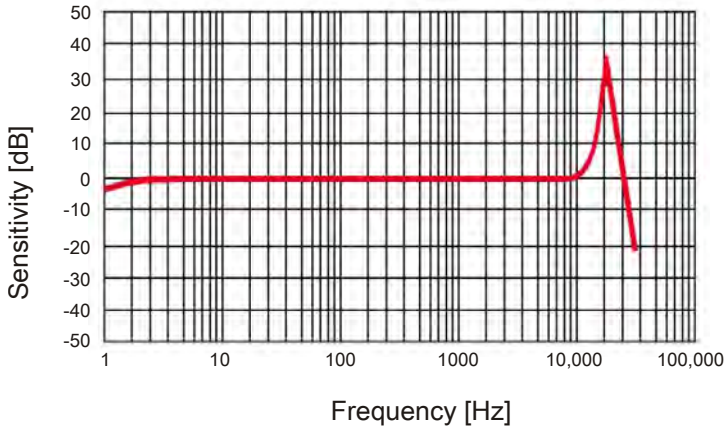


Figure 494: 0ACS100A.x0-1 - Frequency response

4.26.4.8.2 Sensor cables

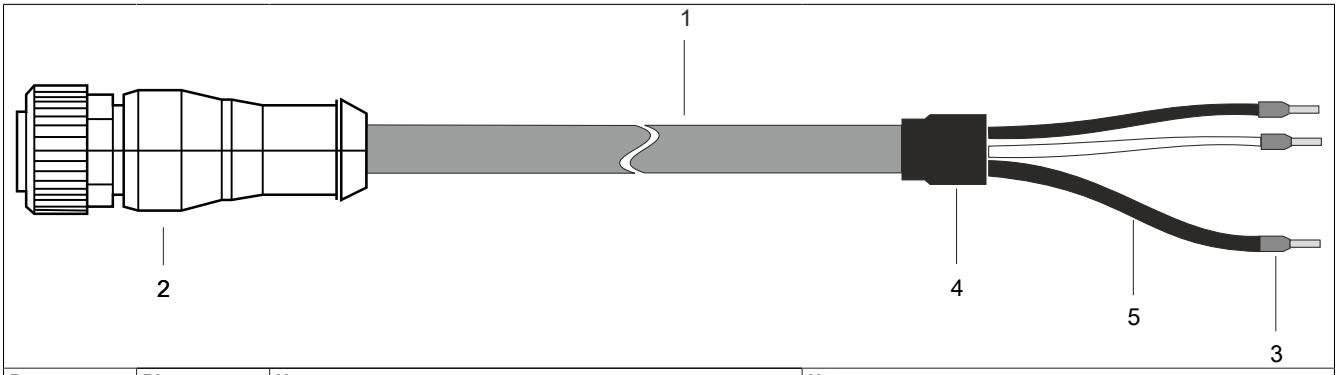
4.26.4.8.2.1 Order data

Model number	Length	Short description
0ACC0020.01-1	2 m	Cable for acceleration sensor, 2x 0.34 mm², 1x 0.25 mm², female M12 connector on sensor, 1x 25 mm² shield connection, can be used in cable drag chains, UL/CSA listed
0ACC0050.01-1	5 m	
0ACC0100.01-1	10 m	
0ACC0150.01-1	15 m	
0ACC0200.01-1	20 m	

4.26.4.8.2.2 Technical data

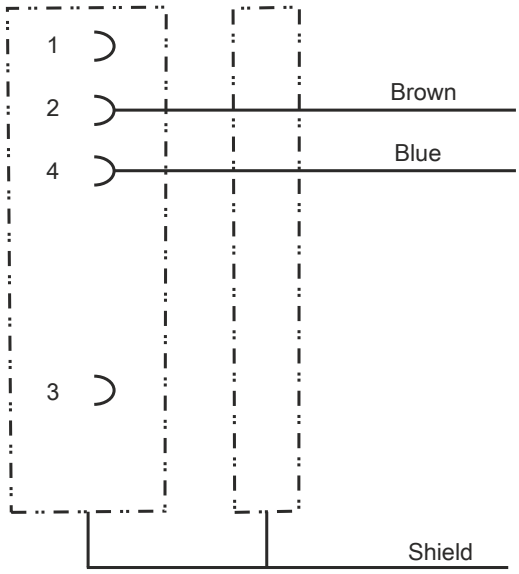
Name	0ACC0xx0.01-1
General information	
Number of poles	3
Cable length	x
Characteristic values of the wire	
Cable type	PUR halogen-free black shielded
AWG signal lead	22
Conductor design signal lead	42x 0.10 mm
Wire diameter incl. insulation	1.27 mm ±0.02 mm
Wall thickness insulation	≥0.21 mm (wire insulation) Approx. 1.1 mm (outer sheath)
Cable external diameter	5.9 mm ±0.15 mm
Insulation resistance	≥100 GΩ*km (at 20°C)
Conductor resistance	Max. 58 Ω/km (at 20°C)
Shielding	Braided copper wires
Cable weight	44 kg/km
Smallest flex radius, fixed	29.5 mm
Smallest flex radius, movable	59 mm
Number of flex cycles	4,000,000
Flex radius	59 mm
Movement range	10 m
Movement speed	3 m/s
Acceleration	10 m/s²
Ambient temperature (during operation)	-40°C ... 80°C (cable, inflexible installation) -25°C ... 80°C (cable, flexible installation)
EN 60529 protection	IP67

4.26.4.8.2.3 Sensor cables with M12 connector



Pos.	Pieces	Name	Note
1	1	Sensor cable	2x 0.34 mm² (1501702 3x 0.34)
2	1	M12 socket (axial)	M12 socket (M12x1 A coded)
3	2	Wire end ferrules (2x sensor cables)	3203066 AI 0.34-8 TQ
4	1	Heat shrink tubing	
5	1	Shield connection	1x 0.25 mm² black
6	1	Wire end ferrules (1x shield connection)	3200632 AI 0.25-12 BU

4.26.4.8.2.4 Cable diagram



4.26.5 X20CM6209

4.26.5.1 General information

This module is a diode array module with six diodes. It is usually used to capture the status of a key. The diodes can also be used as freewheeling diodes or decoupling diodes.

The diode array module has no connection to X2X Link. It behaves like a dummy module.

- 6 potential-free diodes
- 24 VDC
- 1 A current load for each diode

4.26.5.2 Order data

Model number	Short description	Figure
	Other functions	
X20CM6209	X20 diode array module, 1 A, 40 V reverse voltage, no module status data	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

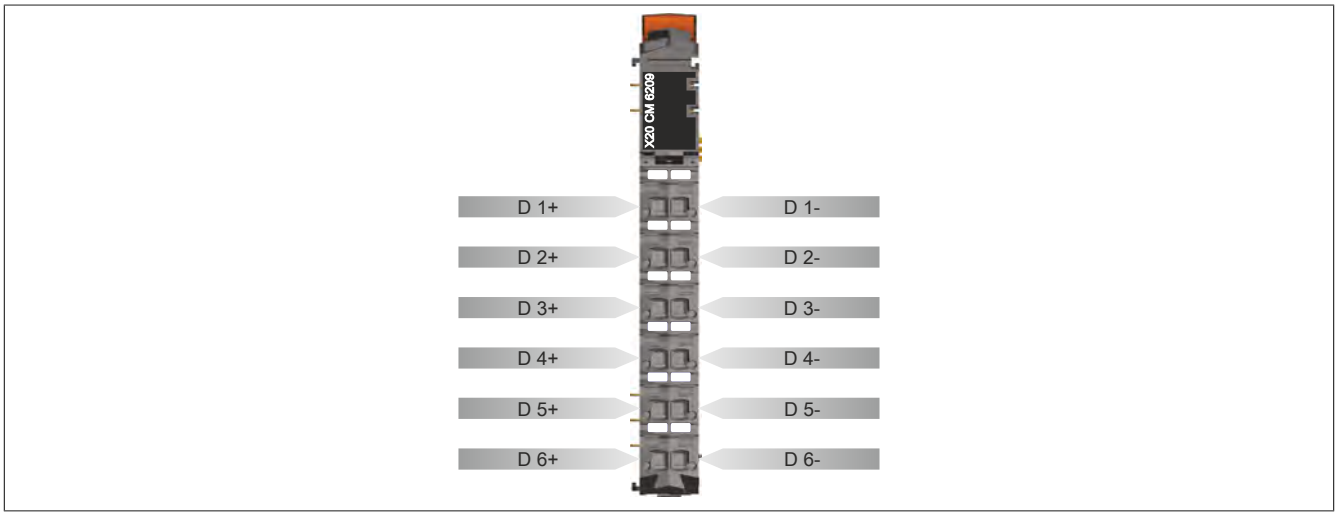
Table 638: X20CM6209 - Order data

4.26.5.3 Technical data

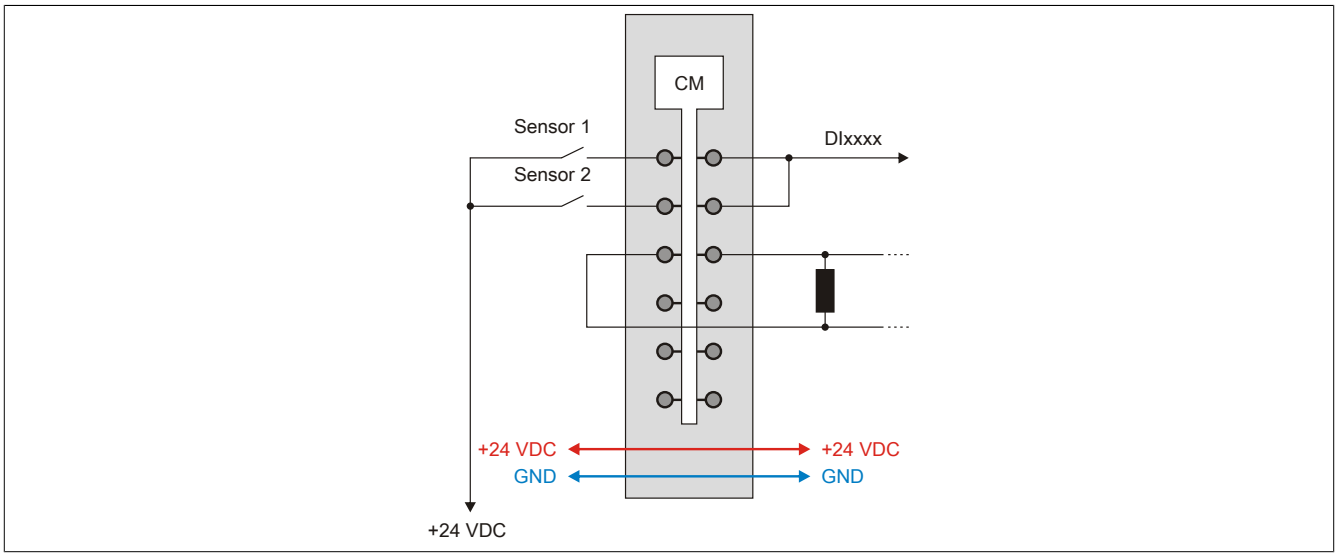
Product ID	X20CM6209
Short description	
I/O module	6 diodes, 24 VDC
General information	
B&R ID code	0xA7A1
Power consumption	
Bus	-
Internal I/O	-
External I/O	2.5 W
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2	Yes
KC	Yes
GOST-R	Yes
Diode array	
Nominal voltage	24 VDC
Nominal input current	1.0 A
Input voltage	24 VDC -15% / +20%
Summation current	6 A, see section "Derating"
Short circuit protection	No
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	See section "Derating"
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module or 1x X20BM01 supply bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 639: X20CM6209 - Technical data

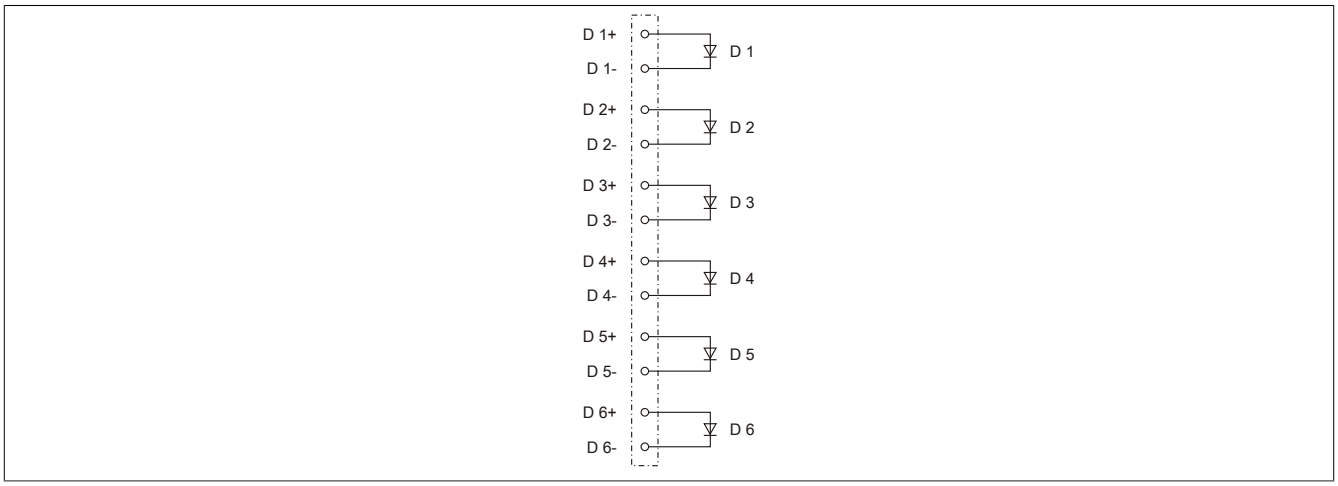
4.26.5.4 Pinout



4.26.5.5 Connection example

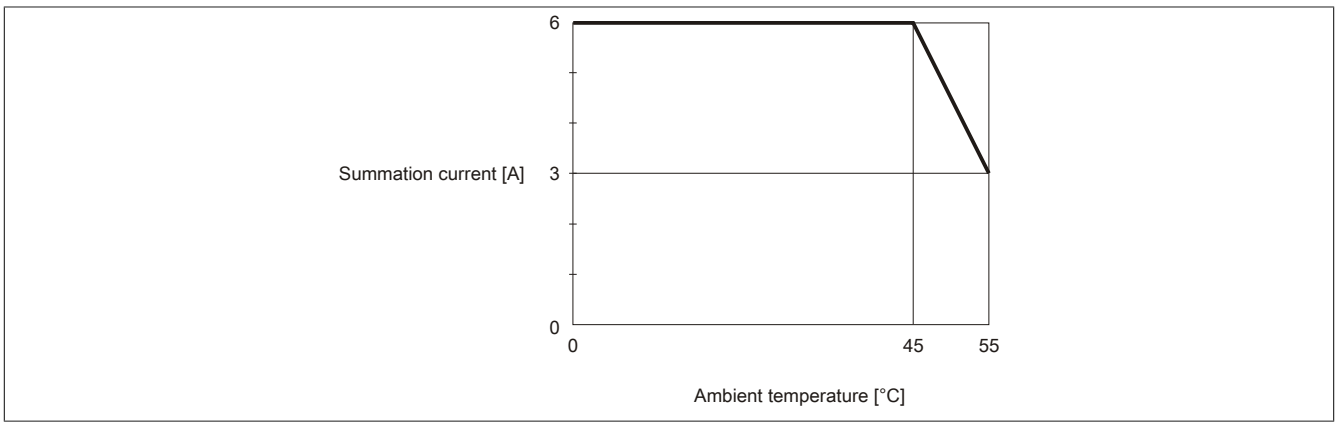


4.26.5.6 Input circuit diagram



4.26.5.7 Derating

The following diagram illustrates the permitted summation current depending on the ambient temperature.



4.26.6 X20CM8281

4.26.6.1 General information

The module is a universal mixed module. On this module, digital I/O and analog I/O are combined. A current or voltage signal can be used for the analog I/O as desired. Counter functions on two of the digital inputs expand the range of use.

- Digital and analog channels
- Selectable current and voltage for AI and AO
- Counter functions

4.26.6.2 Order data

Model number	Short description	Figure
	Other functions	
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 640: X20CM8281 - Order data

4.26.6.3 Technical data

Product ID	X20CM8281
Short description	
I/O module	4 digital inputs, 2 digital outputs, 1 analog input, 1 analog output, special functions
General information	
B&R ID code	0x24C3
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Analog inputs	Yes, using status LED and software
Digital outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.01 W
Internal I/O	1.75 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Digital inputs	
Quantity	4
Nominal voltage	24 VDC
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 3.3 mA
Input filter	
Hardware	≤2 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	1-wire connections

Table 641: X20CM8281 - Technical data

Product ID	X20CM8281
Input circuit	Sink
Additional functions	20 kHz event counting, gate measurement
Input resistance	Typ. 7.18 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Event counter	
Quantity	2
Signal form	Square wave pulse
Evaluation	Each falling edge, cyclic counter
Input frequency	Max. 20 kHz
Counter 1	Input 1
Counter 2	Input 3
Counter frequency	Max. 20 kHz
Counter size	16-bit
Gate measurement	
Quantity	1
Signal form	Square wave pulse
Evaluation	Rising edge - falling edge
Counter frequency	
Internal	48 MHz, 24 MHz, 12 MHz, 6 MHz, 3 MHz, 1.5 MHz, 750 kHz, 375 kHz, 187.5 kHz
Counter size	16-bit
Length of pause between pulses	≥100 µs
Pulse length	≥20 µs
Supported inputs	Input 4
Analog inputs	
Quantity	1
Input	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections
Input type	Single ended
Digital converter resolution	
Voltage	±12-bit
Current	12-bit
Conversion time	400 µs, conversion runs asynchronously to the X2X Link cycle
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Input impedance in signal range	
Voltage	>1 MΩ
Current	-
Load	
Voltage	-
Current	<300 Ω
Input protection	Protection against wiring with supply voltage
Permitted input signal	
Voltage	Max. ±15 V
Current	Max. ±50 mA
Output of the digital value during overload	
Below lower limit	
Voltage	0x8001
Current	0x0000
Above upper limit	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	Successive approximation
Input filter	2nd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Voltage	
Gain	0.08% [2]
Offset	0.02% [3]
Current	
Gain	0 to 20 mA = 0.08 % / 4 to 20 mA = 0.1 % [2]
Offset	0 to 20 mA = 0.03 % / 4 to 20 mA = 0.16 % [4]
Max. gain drift	
Voltage	0.01 %/°C [2]
Current	0 to 20 mA = 0.009 %/°C 4 to 20 mA = 0.0113 %/°C [2]
Max. offset drift	
Voltage	0.002 %/°C [3]
Current	0 to 20 mA = 0.004 %/°C 4 to 20 mA = 0.005 %/°C [4]

Table 641: X20CM8281 - Technical data

Product ID	X20CM8281
Nonlinearity	
Voltage	<0.02% [3]
Current	<0.02% [4]
Isolation voltage between channel and bus	500 V_{eff}
Digital outputs	
Design	FET positive switching
Quantity	2
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	1 A
Connection type	1-wire connections
Output circuit	Source
Output protection	Thermal cutoff for overcurrent and short circuit, integrated protection for switching inductances, reverse polarity protection
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
$R_{DS(on)}$	105 mΩ
Peak short circuit current	<14 A
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 -> 1	<250 µs
1 -> 0	<270 µs
Switching frequency	
Resistive load	Max. 100 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 50 VDC
Isolation voltage between channel and bus	500 V_{eff}
Analog outputs	
Quantity	1
Output	±10 V or 0 to 20 mA, via different terminal connections
Digital converter resolution	12-bit
Conversion time	300 µs, conversion runs asynchronously to the X2X Link cycle
Settling time for output changes over entire range	1 ms
Power on/off behavior	Internal enable relay for booting and errors
Max. error at 25°C	
Voltage	
Gain	0.04% [5]
Offset	0.0225% [6]
Current	
Gain	0.05% [5]
Offset	0.125% [6]
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0010 = 4.882 mV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0010 = 9.766 µA
Load per channel	
Voltage	Max. ±10 mA, load ≥ 1 kΩ
Current	Max. load is 400 Ω
Max. gain drift	
Voltage	0.012 %/°C [5]
Current	0.014 %/°C [5]
Max. offset drift	
Voltage	0.0075 %/°C [6]
Current	0.03 %/°C [6]
Error caused by load change	
Voltage	Max. 0.02%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 400 Ω, resistive
Nonlinearity	<0.1% [7]
Isolation voltage between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20

Table 641: X20CM8281 - Technical data

Product ID	X20CM8281
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 641: X20CM8281 - Technical data

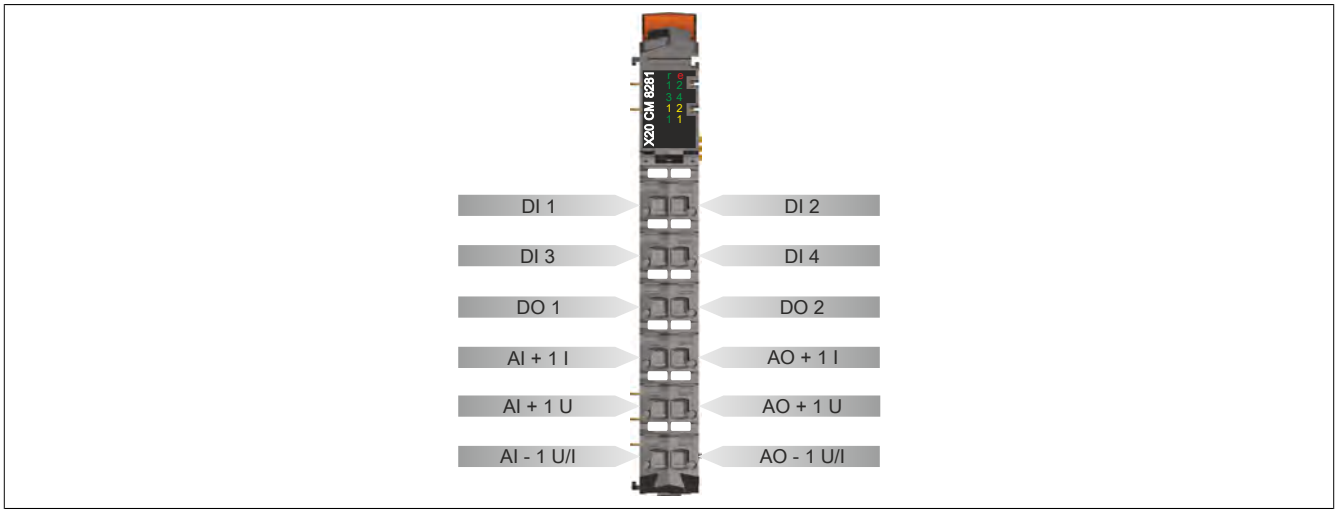
1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.
5) Based on the current output value.
6) Based on the entire output range.
7) Based on the output range.

4.26.6.4 LED status indicators

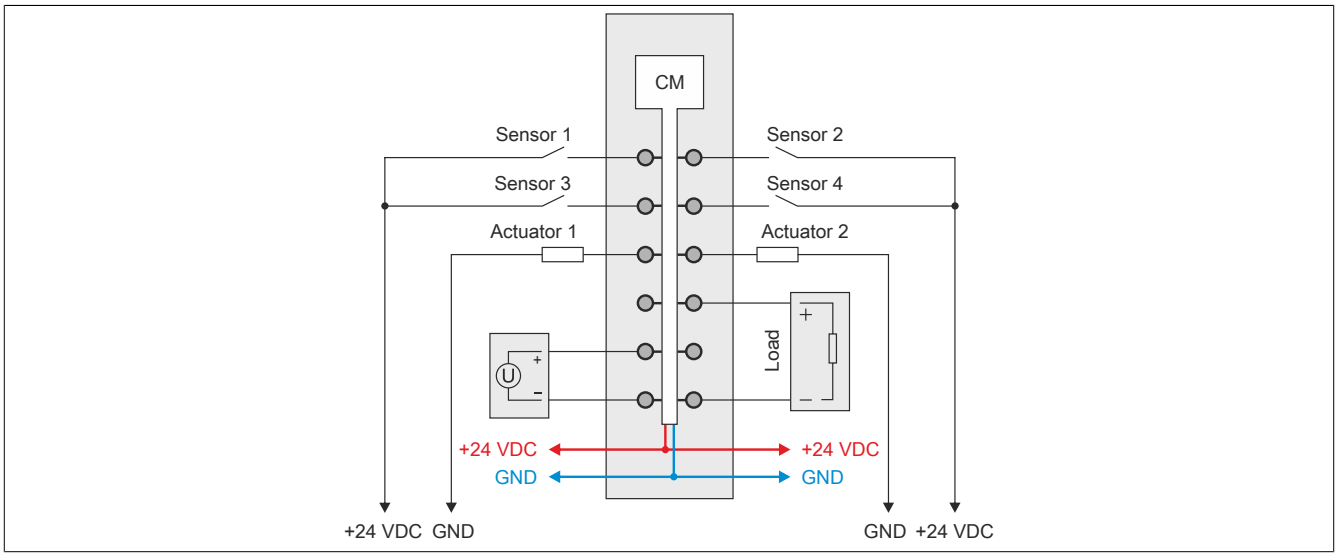
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green		Input state of the corresponding digital input
	1 - 2	Orange		Output status of the corresponding digital output
	1	Green	Off	Open line or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK
	1	Orange	Off	Value = 0
			On	Value ≠ 0

4.26.6.5 Pinout

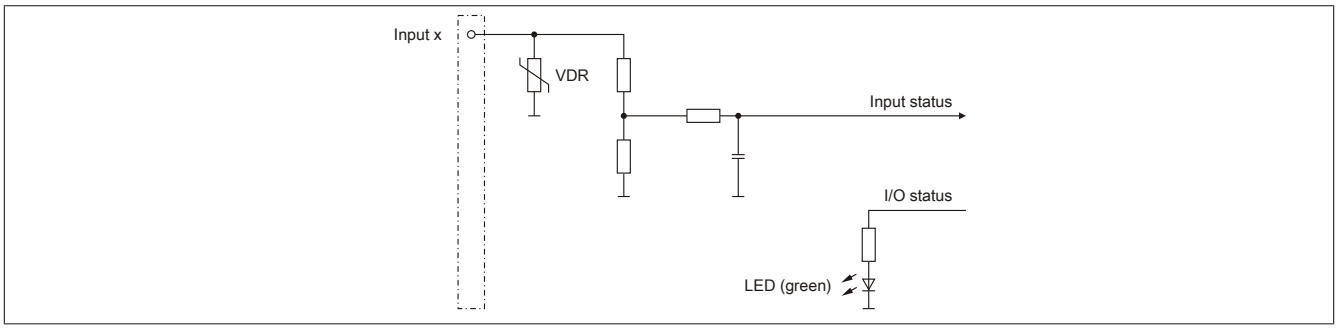


4.26.6.6 Connection example

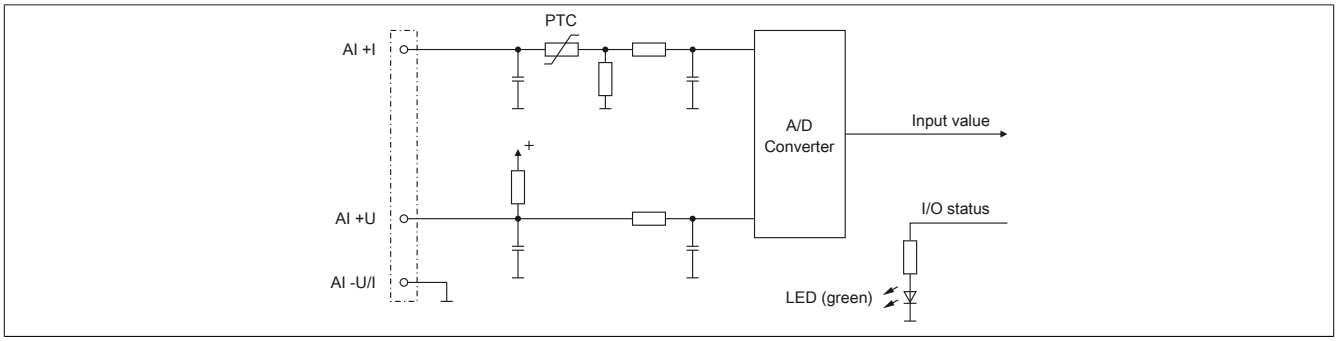


4.26.6.7 Input circuit diagram

Digital inputs

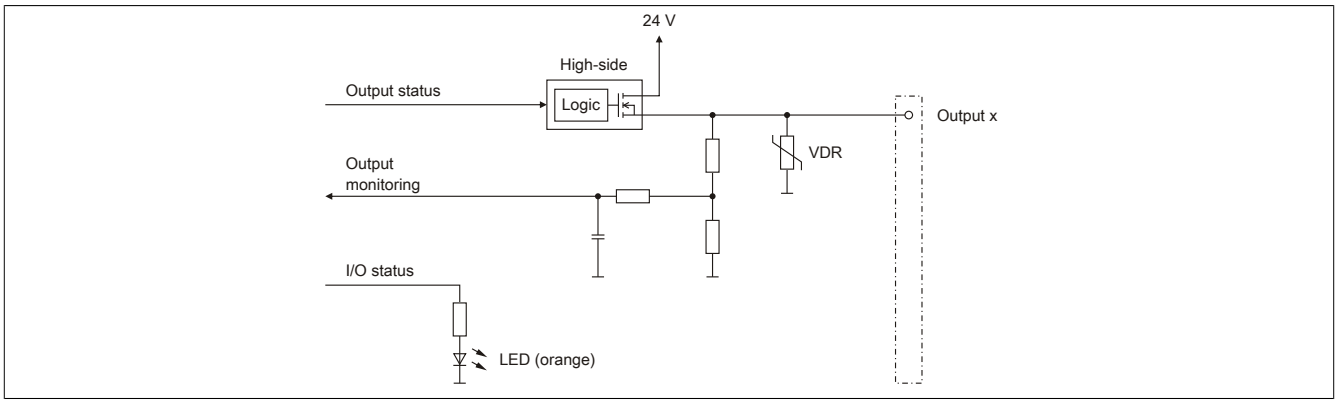


Analog inputs

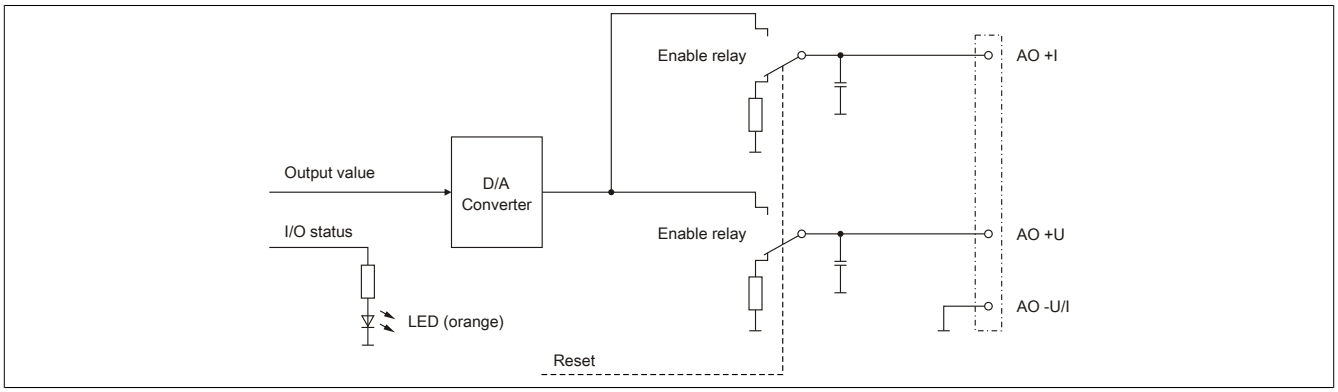


4.26.6.8 Output circuit diagram

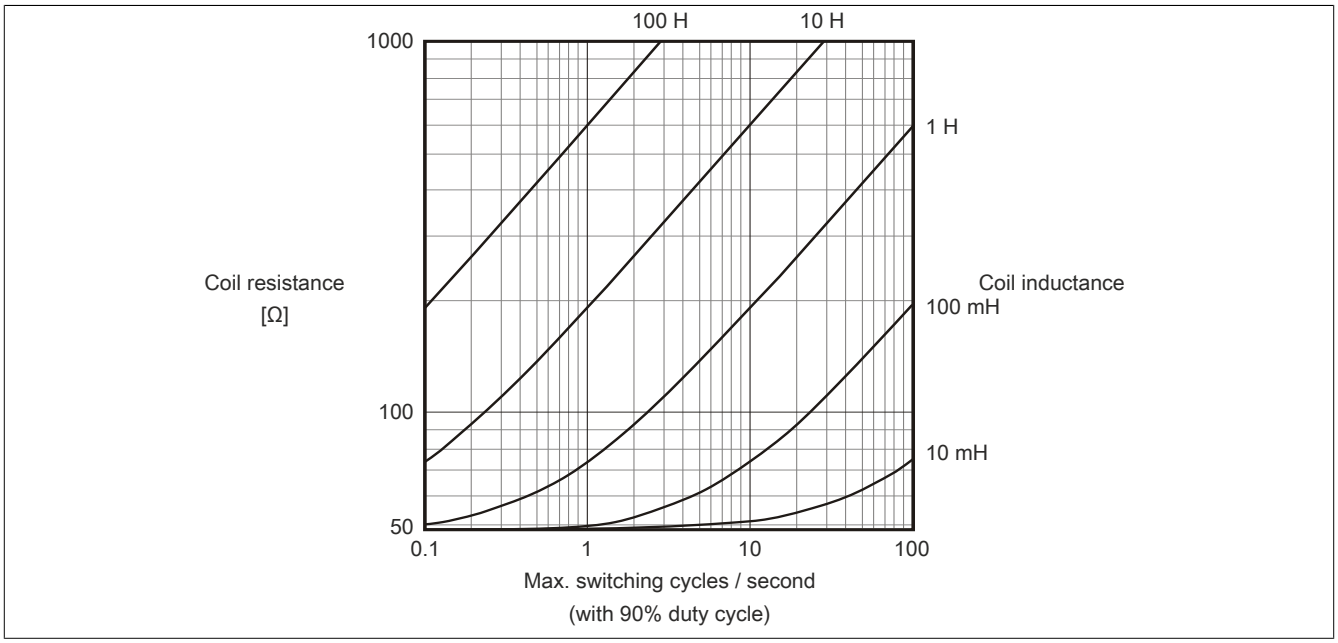
Digital outputs



Analog outputs



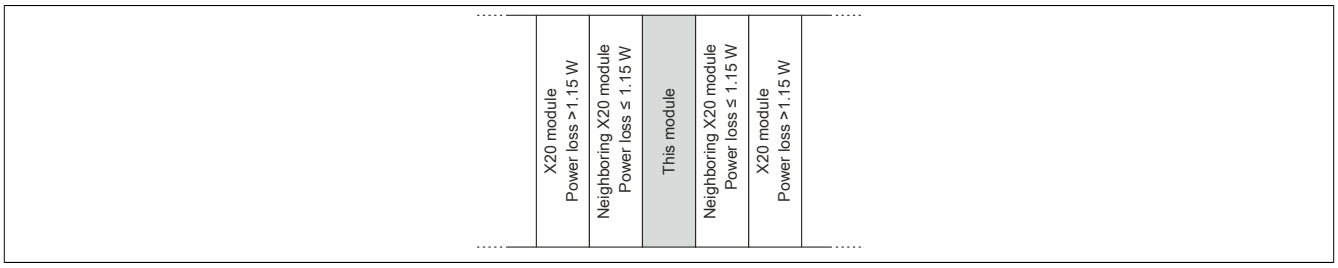
4.26.6.9 Switching inductive loads



4.26.6.10 Derating

There is no derating when operated below 55°C.

When operated at temperatures above 55°C, the power consumption of the modules to the left and right of this module must not exceed 1.15 W



4.26.6.11 Register description

4.26.6.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.6.11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Digital inputs						
0	Digital inputs	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput04	Bit 3				
4	Counter01	UINT	•			
6	Counter02	UINT	•			
12	ConfigOutput01	USINT				•
14	ConfigOutput02	USINT			•	
	ResetCounter01	Bit 4				
	ResetCounter02	Bit 5				
16	Input state of digital latch inputs 1 - 4	DINT	•			
	DigitalInput01Latch	Bit 0				
	...	...				
	DigitalInput04Latch	Bit 3				
18	Acknowledge digital inputs	USINT			•	
	DigitalInput01LatchQuit	Bit 0				
	...	...				
	DigitalInput04LatchQuit	Bit 3				
Digital outputs						
0	Status of the digital outputs	USINT	•			
	StatusDigitalOutput01	Bit 4				
	StatusDigitalOutput02	Bit 5				
2	Switching state of digital outputs 1 to 2	USINT			•	
	DigitalOutput01	USINT				
	DigitalOutput02	UINT				
Analog input						
8	AnalogInput01	INT	•			
22	ConfigOutput03	USINT				•
26	ConfigOutput05	INT				•
28	ConfigOutput06	INT				•
31	StatusInput01	USINT	•			
Analog output						
10	AnalogOutput01	INT			•	
Configuration of the analog inputs and outputs						
24	ConfigOutput04	USINT				•

4.26.6.11.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Digital inputs							
0	0	Digital inputs	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
4	2	Counter01	UINT	•			
6	4	Counter02	UINT	•			
12	-	ConfigOutput01	USINT		•		
14	-	ConfigOutput02	USINT				•
		ResetCounter01	Bit 4				
		ResetCounter02	Bit 5				
16	-	Input state of digital latch inputs 1 - 4	DINT		•		
		DigitalInput01Latch	Bit 0				
		...	...				
		DigitalInput04Latch	Bit 3				
18	-	Acknowledge digital inputs	USINT				•
		DigitalInput01LatchQuit	Bit 0				
		...	...				
		DigitalInput04LatchQuit	Bit 3				
Digital outputs							
0	0	Status of the digital outputs	USINT	•			
		StatusDigitalOutput01	Bit 4				
		StatusDigitalOutput02	Bit 5				
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	USINT				
		DigitalOutput02	UINT				
Analog input							
8	6	AnalogInput01	INT	•			
22	-	ConfigOutput03	USINT				•
26	-	ConfigOutput05	INT				•
28	-	ConfigOutput06	INT				•
31	-	StatusInput01	USINT		•		
Analog output							
10	2	AnalogOutput01	INT			•	
Configuration of the analog inputs and outputs							
24	-	ConfigOutput04	USINT				•

1) The offset specifies the position of the register within the CAN object.

4.26.6.11.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.26.6.11.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

4.26.6.11.4.1 Digital inputs and status of the digital outputs

Name:
DigitalInput01 to DigitalInput04
StatusDigitalOutput01 to StatusDigitalOutput02

This register is used to indicate the input state of the digital inputs and the status of the digital outputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input state - Digital input 1
4	StatusDigitalOutput01	0	Digital output channel 1: No error
		1	Digital output channel 1: Short circuit or overload
5	StatusDigitalOutput02	0	Digital output channel 2: No error
		1	Digital output channel 2: Short circuit or overload
6 - 7	Reserved	-	

4.26.6.11.4.2 Digital input filter

Register name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.26.6.11.4.3 Event or gate counter

Event counter operation

The rising (positive) edges are registered on the counter input.

The counter status is collected with a fixed offset to the network cycle and transferred in the same cycle.

Gate measurement

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF) and corrected with the adjustable prescaler.

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

Event or gate counter

Name:
Counter01 to Counter02

Counter01 is intended for event counter operation.

Event counter operation or gate measurement can be selected for Counter02:

Data type	Value
USINT	Counter value

Counter configuration

Name:
ConfigOutput02

This register can be used to configure and reset the individual counters.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Counter02 (counter frequency, only with gate measurement)	0	48 MHz
		1	3 MHz
		2	187.5 kHz
		3	24 MHz
		4	12 MHz
		5	6 MHz
		6	1.5 MHz
		7	750 kHz
		8	375 kHz
4	ResetCounter01	0	No influence on the counter
		1	Clear counter (at positive edge)
5	ResetCounter02	0	No influence on the counter
		1	Clear counter (at positive edge)
6 - 7	Counter02 (operating mode)	0	Event counter measurement
		1	Gate measurement

This register also includes configuration data in addition to the cyclic data. If the register is used cyclically and in the init script, then the preset configuration only remains available when operated directly on the CPU. On the bus controller, the configuration is always overwritten with 0.

However, starting with upgrade version 1.0.2.1, the cyclic bit can be hidden in order to prevent the configuration from being overwritten.

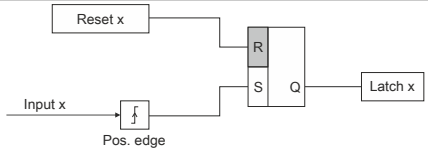
Information:

If the counter should be cleared, this must be done using a non-cyclic write command. When doing so, the configuration bit must be transferred together with the reset counter bit!

4.26.6.11.4.4 Rising edge input latch

Using this function, the rising edges of the input signal can be latched with a resolution of 200 µs. With the "Acknowledge - input latch" function, the input latch is either reset or prevented from latching.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	Status
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

Input state of digital latch inputs 1 - 4

Name:
DigitalInputLatch01 to DigitalInputLatch04

This register is used to indicate input state of digital inputs 1 to 4 after expiration of the input filter time.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInputLatch01	0 or 1	Input state of digital input 1 after expiration of the delay time
...		...	
3	DigitalInputLatch04	0 or 1	Input state of digital input 4 after expiration of the delay time
4 - 7	Reserved	-	

Acknowledge digital inputs

Name:
DigitalInput01LatchQuitt to DigitalInput04LatchQuitt

This register is used to reset the input latches channel by channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01LatchQuitt	0	No influence on the latch status
		1	Resets the latch status
...		...	
3	DigitalInput04LatchQuitt	0	No influence on the latch status
		1	Resets the latch status
4 - 7	Reserved	-	

4.26.6.11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

4.26.6.11.5.1 Switching state of digital outputs 1 to 2

Name:
DigitalOutput01 to DigitalOutput02

This register is used to store the switching state of digital outputs 1 to 2.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
1	DigitalOutput02	0	Digital output 02 reset
		1	Digital output 02 set

4.26.6.11.5.2 Digital inputs and status of the digital outputs

Name:
DigitalInput01 to DigitalInput04
StatusDigitalOutput01 to StatusDigitalOutput02

This register is used to indicate the input state of the digital inputs and the status of the digital outputs.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input state - Digital input 1
4	StatusDigitalOutput01	0	Digital output channel 1: No error
		1	Digital output channel 1: Short circuit or overload
5	StatusDigitalOutput02	0	Digital output channel 2: No error
		1	Digital output channel 2: Short circuit or overload
6 - 7	Reserved	-	

4.26.6.11.6 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

4.26.6.11.6.1 Analog input register

Name:
AnalogInput01

This register is used to indicate the analog input value depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA
	0 to 32767	Current signal 4 mA to 20 mA

4.26.6.11.6.2 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >400 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the channels are scanned in 1 ms cycles. Conversion is performed acyclically to the X2X cycle.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

Input ramp limitation

Input ramp limitation can only take place when a filter is used; the input ramp is limited before filtering takes place.

The amount the input value changes is checked to make sure that specified limits are not exceeded. If the values are exceeded, the adjusted input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limitation is well suited for suppressing disturbances (spikes). The following examples show the function of the input ramp limitation based on an input jump and a disturbance.

Example 1

The input value jumps from 8,000 to 17,000. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

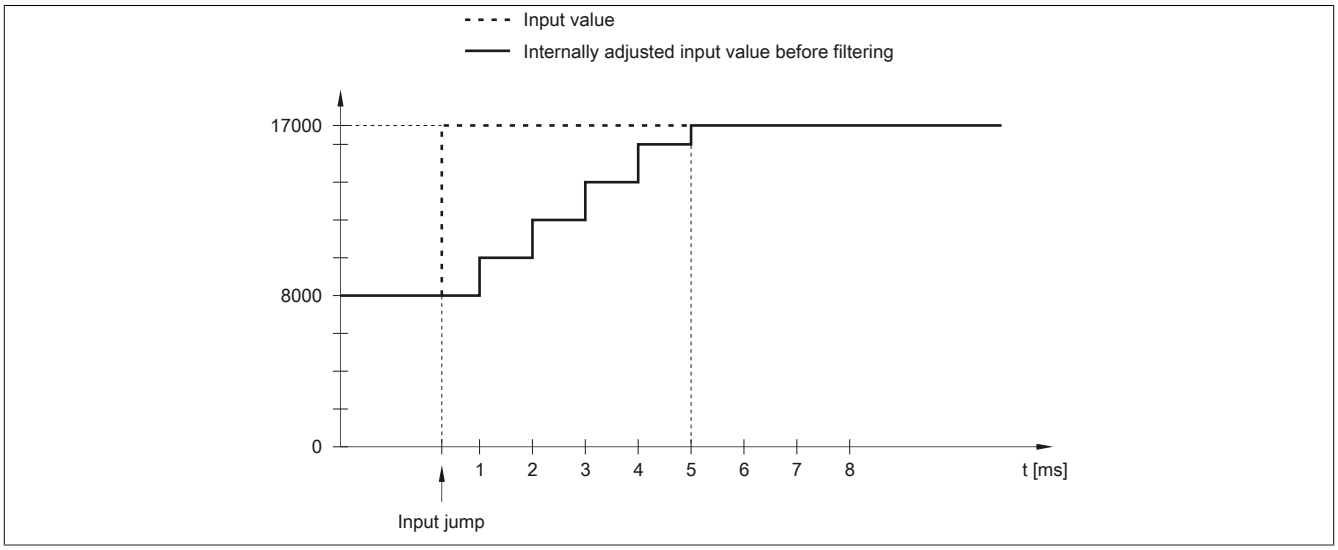


Figure 495: Adjusted input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the adjusted input value with the following settings:

Input ramp limitation = 4 = 0x07FF = 2047

Filter level = 2

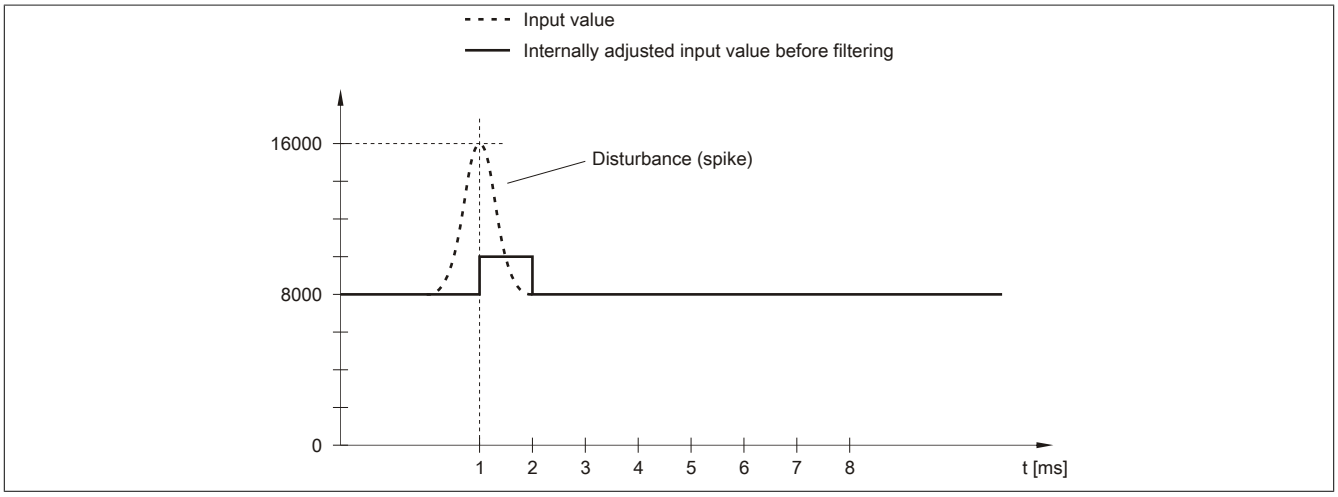


Figure 496: Adjusted input value for disturbance

Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$Value_{new} = Value_{old} - \frac{Value_{old}}{Filter\ level} + \frac{Input\ value}{Filter\ level}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8,000 to 16,000. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

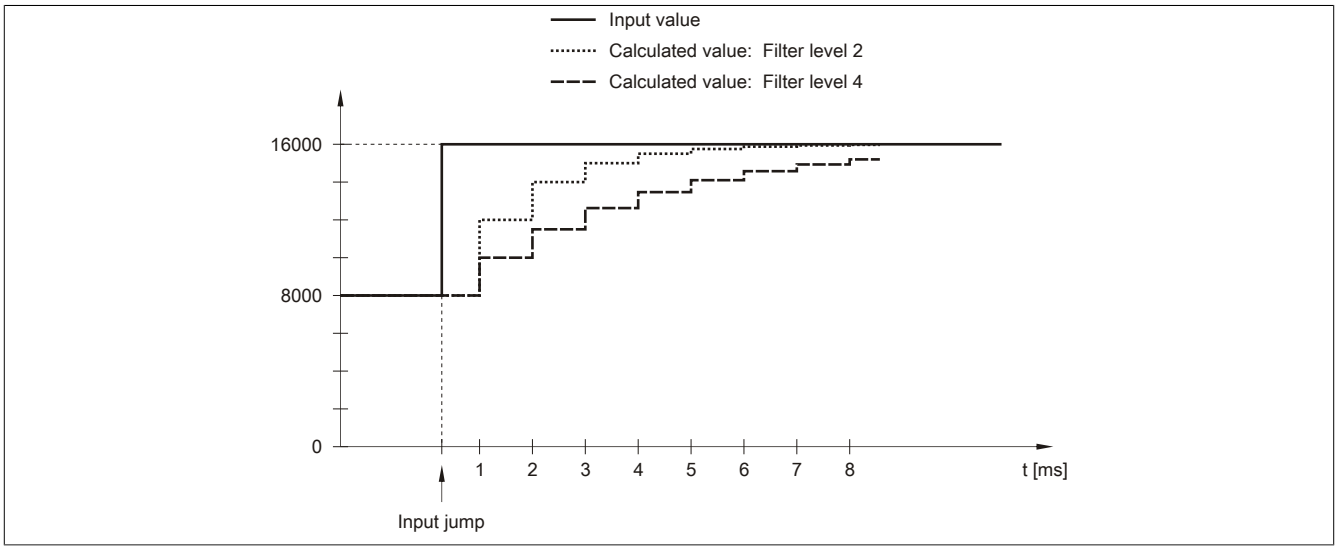


Figure 497: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limitation = 0

Filter level = 2 or 4

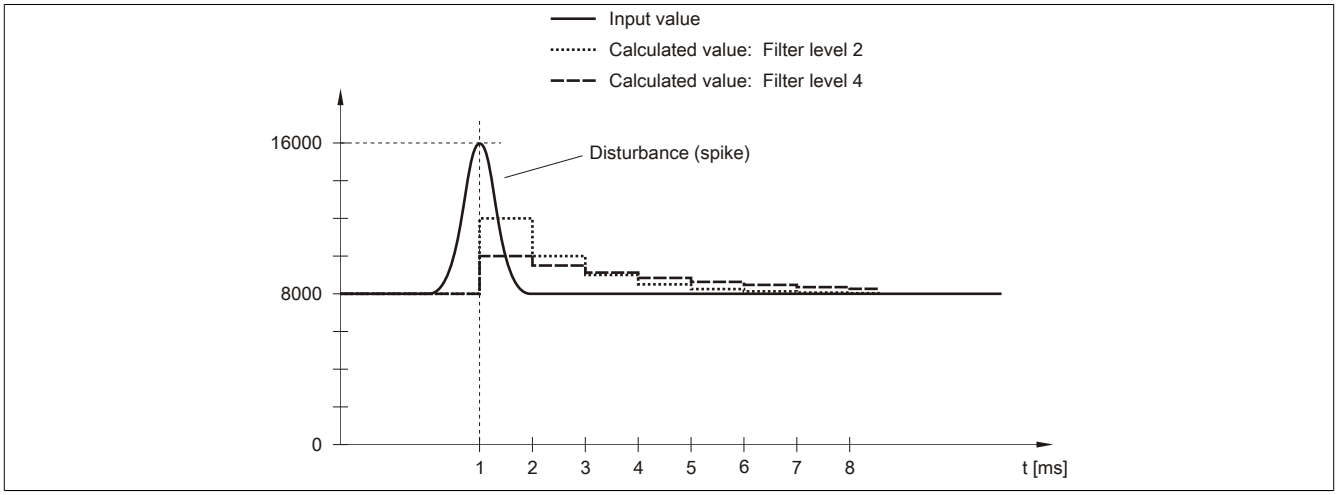


Figure 498: Calculated value during disturbance

4.26.6.11.6.3 Configuring the input filter

Name:
ConfigOutput03

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter switched off
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is used without limitation
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

4.26.6.11.6.4 Lower limit for the analog value

Name:
ConfigOutput05

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Information:

- **The default value of -32768 corresponds to the minimum default value of -10 VDC.**
- **For current measurements, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Data type	Value
INT	-32768 to 32767

4.26.6.11.6.5 Upper limit for the analog value

Name:
ConfigOutput06

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Information:

- **The default value of 32767 corresponds to the maximum default value of 20 mA or +10 VDC.**

Data type	Value
INT	-32768 to 32767

4.26.6.11.6.6 Status of the analog input

Name:
StatusInput01

This register is used to monitor the analog input on the module. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line[1)]
2 - 7	Reserved	0	

1) Open-circuit detection does not occur during current signal measurement.

4.26.6.11.7 Analog output

The channel can be configured for either current or voltage signals. The type of signal is also determined by the connection terminals used.

4.26.6.11.7.1 Analog output register

Name:
AnalogOutput01

This register is used to output the analog output value appears depending on the operating mode that is set.

Data type	Value	Information
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA

4.26.6.11.8 Configuration of the analog inputs and outputs

Name:
ConfigOutput04

This register can be used to define the type and range of signal measurement.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the connection terminals used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal.

Input signal:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Output signal:

- ±10 V voltage signal
- 0 to 20 mA current signal

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Analog input	00	Voltage signal -10 VDC to +10 VDC
		01	Current signal 0 mA to 20 mA
		11	Current signal 4 mA to 20 mA
2 - 3	Reserved	0	
4	Analog output	0	Voltage signal -10 VDC to +10 VDC
		1	Current signal 0 mA to 20 mA
5 - 7	Reserved	0	

4.26.6.11.9 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

4.26.6.11.10 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Digital without filtering	150 µs
Digital with filtering	200 µs
Analog without filtering	400 µs
Analog with filtering	1000 µs

4.26.7 X20CM8323

4.26.7.1 General information

The module has digital outputs for switching electromechanical loads (e.g. valves, relays) and additional functions.

- 8 digital outputs
- Current trace
- Switching time detection
- Pulse width modulation

4.26.7.2 Order data

Model number	Short description	Figure
	Other functions	
X20CM8323	X20 PWM module, 8 digital outputs for switching electromechanical loads, 0.6 A continuous current, 2 A peak current, current monitoring, switching time detection	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 642: X20CM8323 - Order data

4.26.7.3 Technical data

Product ID	X20CM8323
Short description	
I/O module	8 digital outputs for switching electromechanical loads, current monitoring, switching time detection, pulse width modulation
General information	
B&R ID code	0x1D43
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.01 W
Internal I/O	1 W (Rev. ≥ G0), 1.5 W (Rev. < G0)
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Channel - I/O supply	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Digital outputs	
Nominal voltage	24 VDC
Nominal output current	0.6 A
Total nominal current	4.8 A
Connection type	1-wire connections
Output circuit	Sink
Output protection	Thermal cutoff if overcurrent or short circuit occurs, integrated protection for switching inductances
Pulse width modulation	
Period duration	1 ms (1 kHz) or 20 µs (50 kHz)
Pulse duration	0 to 100 %
Resolution for pulse duration	1%
Starting current	Max. 2 A for max. 25.5 ms

Table 643: X20CM8323 - Technical data

Product ID	X20CM8323
Braking voltage when switching off inductive loads	39 VDC
Reverse polarity protection	No (must be protected externally)
Output voltage	
Minimum	18 VDC
Nominal	24 VDC
Maximum	42 VDC
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 60°C (Rev. ≥ G0); 0 to 55°C (Rev. < G0) [2]
Vertical installation	0 to 50°C [3]
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 643: X20CM8323 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Rev. G0 and higher: Up to a maximum of 6 channels only are permitted to be switched on simultaneously over 55°C.
3) Rev. G0 and higher: Up to a maximum of 6 channels only are permitted to be switched on simultaneously over 45°C.

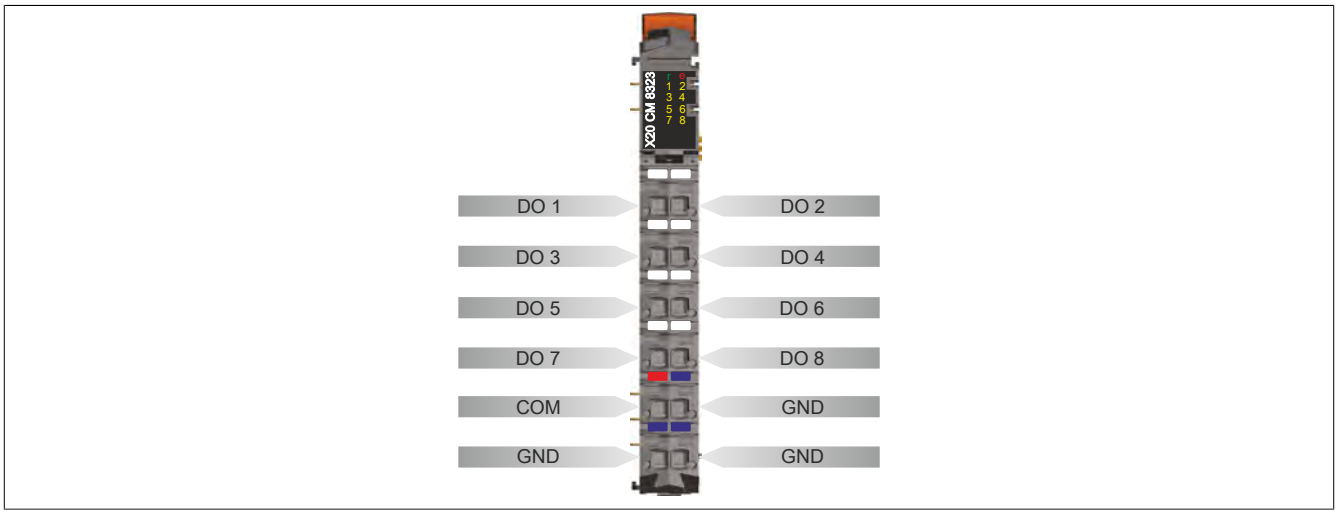
4.26.7.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

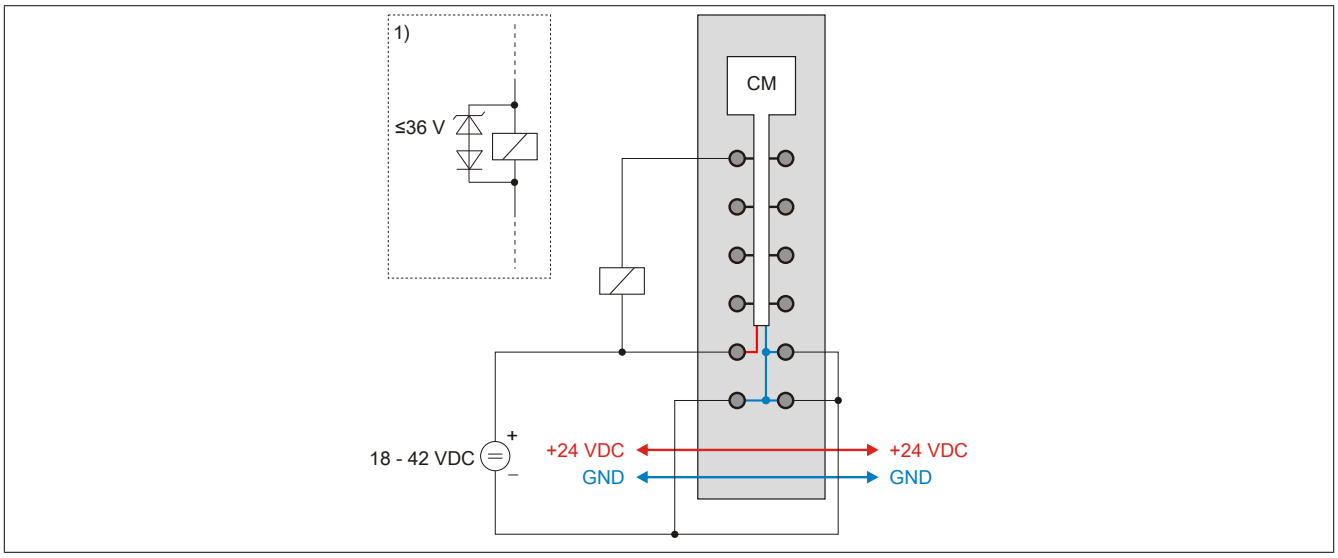
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 8	Orange	On/Off	Status of the digital outputs
			Blinking	Short-circuit / overcurrent cutoff **Information:** **The output is not automatically activated after an overcurrent cutoff. It must be switched on again.**

1) Depending on the configuration, a firmware update can take up to several minutes.

4.26.7.5 Pinout

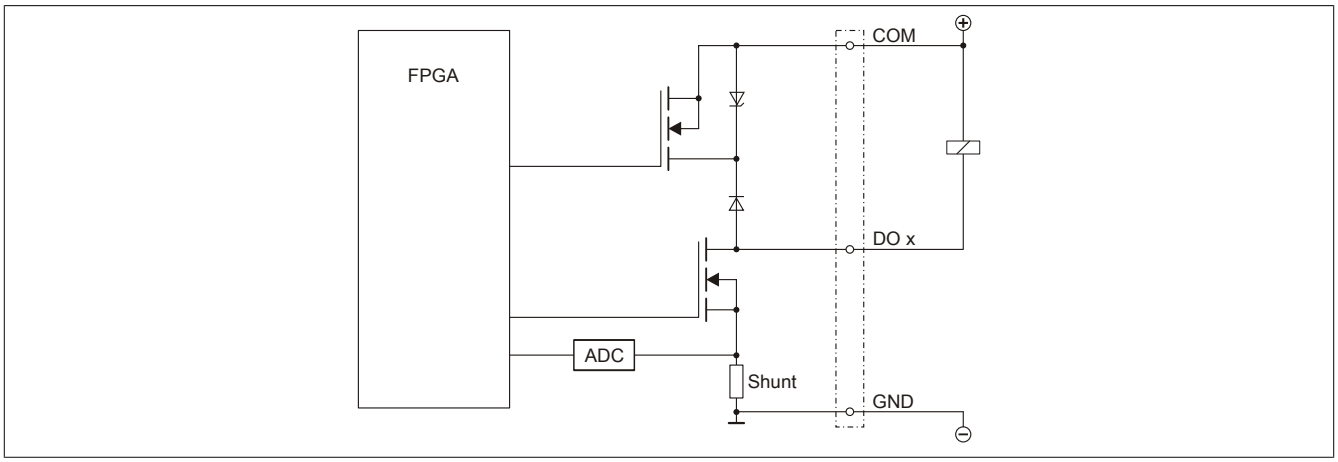


4.26.7.6 Connection example



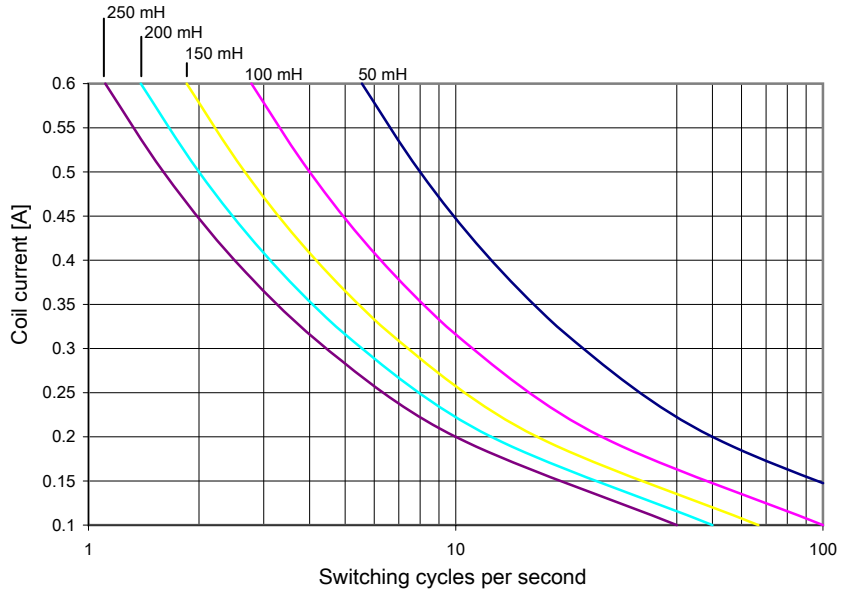
1) If larger inductances or more current are used; the "transil-diode combination" must be placed externally on the relay/valve.

4.26.7.7 Output circuit diagram

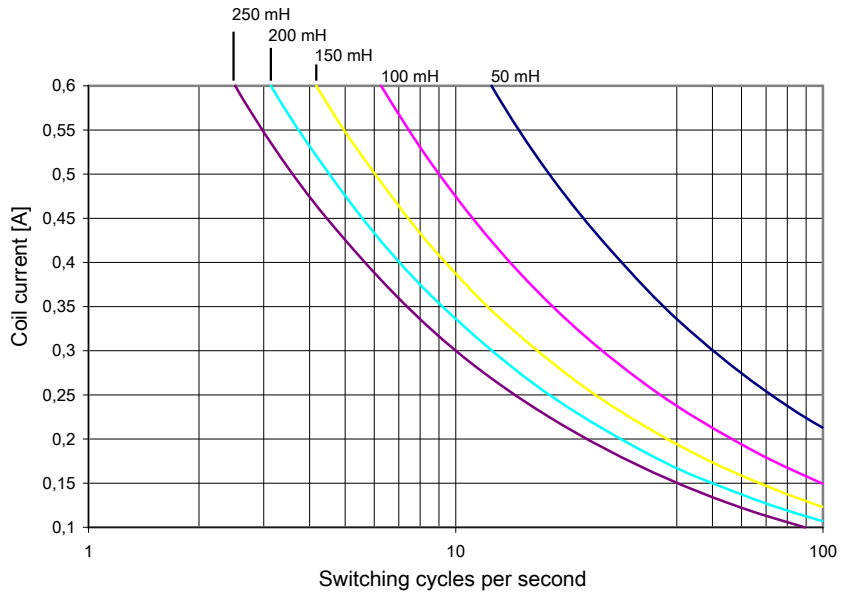


4.26.7.8 Switching inductive loads

Before revision G0



From revision G0



In principle, the inductance that is connected is limited by the maximum power dissipation of the module.

If larger inductances or more current are used, the the "transil-diode combination" must be placed externally on the relay/valve (see 4.26.7.6 "Connection example").

Information:

The inductance of a relay/valve depends greatly on the core material being used. Therefore, an inductance must be used that corresponds to the diagram at 1Hz. This information can be found in the data sheet of the connected inductance (relay/valve).

4.26.7.9 Register description

4.26.7.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.7.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
12	ConfigOutput02	USINT				•
13	ConfigOutput03	USINT				•
14	ConfigOutput04	USINT				•
Index + 10	ConfigOutputN (Index N = 05 to 20)	USINT				•
38	ConfigOutput21	USINT				•
Communication						
9	Digital outputs	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput08	Bit 7				
9	StatusInput01	USINT	•			
10	StatusInput02	USINT		•		
0	AnalogInput01	USINT	•			
Index - 1	AnalogInput0N (Index N = 2 to 9)	USINT	•			
10	StatusOutput01	UINT			•	
Index + 47	Current0N (Index N = 1 to 8)	USINT	•			
56	StatusCurrent	USINT	•			
	StatusCurrent01	Bit 0				
	...	...				
	StatusCurrent08	Bit 7				

4.26.7.9.3 Function model 1

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
12	ConfigOutput02	USINT				•
13	ConfigOutput03	USINT				•
14	ConfigOutput04	USINT				•
Index + 10	ConfigOutputN (Index N = 05 to 20)	USINT				•
38	ConfigOutput21	USINT				•
Communication						
9	DigitalOutput	USINT			•	
9	StatusInput01	USINT	•			
10	StatusInput02	USINT		•		
0	AnalogInput01	USINT	•			
Index - 1	AnalogInput0N (Index N = 2 to 9)	USINT	•			
10	StatusOutput01	UINT			•	
Index + 47	Current0N (Index N = 1 to 8)	USINT	•			

4.26.7.9.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration							
12	-	ConfigOutput02	USINT				●
13	-	ConfigOutput03	USINT				●
14	-	ConfigOutput04	USINT				●
Index + 10	-	ConfigOutputN (Index N = 05 to 20)	USINT				●
38	-	ConfigOutput21	USINT				●
48	-	TimeBase	UINT				●
Communication							
9	0	Digital outputs	USINT			●	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
9	6	StatusInput01	USINT	●			
10	-	StatusInput02	USINT		●		
Index + 1	Index + 1	AnalogInput0N (Index N = 1 to 4)	USINT	●			
10	2	StatusOutput01	UINT			●	
0	4	AddressSet	UINT			●	
	4	LineID_Set	USINT				
	5	BlockID_Set	USINT				
0	0	IndexAct	UINT	●			
	0	LineID_Act	USINT				
	1	BlockID_Act	USINT				

1) The offset specifies the position of the register within the CAN object.

4.26.7.9.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.26.7.9.5 Configuration registers

4.26.7.9.5.1 Excitation time

Name:
ConfigOutput02

The excitation time is configured in this register.
The output is switched fully on for the time set in this register after the module is switched on. After the excitation time expires, the module goes into PWM mode.

Data type	Value	Information
USINT	0 to 255	In steps of 100 µs or 1000 µs

4.26.7.9.5.2 PWM ratio

Name:
ConfigOutput03

The PWM ratio between switch-off time and period duration is set in this register (in percent).

Data type	Value	Information
USINT	0	Permanently switched off
	1 to 99	Ratio = switch-off time / period duration (1 to 99%)
	100	Permanently switched off

4.26.7.9.5.3 Module configuration

Name:
ConfigOutput04

This register is used to configure the module's general parameters.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	PWM frequency	0	1 kHz
		1	50 kHz
1	Reserved		
2	Excitation time base	0	100 µs
		1	1000 µs
3	Reserved		
4	Switching point search	0	Low-point method
		1	Curvature method
5 - 7	Reserved		

4.26.7.9.5.4 Current and time differential

Name:
ConfigOutput05 to ConfigOutput20

The switching point search is configured with the parameters dI and dt in these non-cyclic registers.

- dI - Current differential in LSB
- dt - Time differential in 100 µs steps

For a sample configuration, see 4.26.7.9.7 "Configuring dI and dt"

Data type	Value
USINT	0 to 255

Registers	Description	
ConfigOutput05	**dI**	Channel 1
ConfigOutput06	d**t**	
...		...
ConfigOutput19	**dI**	Channel 8
ConfigOutput20	d**t**	

4.26.7.9.5.5 Disables the high-speed cutoff

Name:
ConfigOutput21

This register can be used to enable or disable the high-speed cutoff for individual channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	High-speed cutoff	0	Enabled for Channel 1
		1	Disabled for Channel 1
...		...	
7	High-speed cutoff	0	Enabled for Channel 8
		1	Disabled for Channel 8

4.26.7.9.5.6 Configuration of the time base

Name:
TimeBase

This register can be used to configure the interval between current measurement points.
The interval between measurement points is normally one quarter of the defined X2X Link cycle. When using a CAN controller this value is not available. The time base for the 1/4 measurement cycle must therefore be set separately in Function model 254 - Bus controller.

Data type	Value	Information
UINT	400 to 10000	Measurement point interval in µs for 1/4 measurement cycle

4.26.7.9.6 Communication registers

4.26.7.9.6.1 Uploading the current curves (function models 0 and 1)

A current curve with 200 values is recorded for each channel. The interval between measurement points is equal to a quarter of the defined X2X Link cycle.

The following registers are used to read the current curve recorded by the module:

- AnalogInput01
- AnalogInput02 to Analog09

Set the channel number and line index

Name:
AnalogInput01

If this register contains a valid value (i.e. index is in the valid range) then registers AnalogInput02 to AnalogInput09 provide a block of 8 current values for Channel X.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Channel number	0	Channel 1
		...	
		7	Channel 8
3 - 7	Index	0 to 24	Line index

The index specifies which part of the current curve is represented by the block of 8 values:

Value X of the current curve	Index	Register
1	0	AnalogInput02
2		AnalogInput03
...		...
8		AnalogInput09
9	1	AnalogInput02
...	:	...
193	24	AnalogInput02
...		...
200		AnalogInput09

Table 644: Relationship between index, channel and AnalogInput02 - AnalogInput09

Examples

The 200th value of the curve contains the switching point of the connected valve/relay found by the module.

- Value 200 = 78: The 78th measurement point corresponds to the switching point of the valve/relay.
- Value 200 = 255: No switching point was found.

Analog input values

Name:
AnalogInput02 to AnalogInput09

A current curve with 200 values is recorded for each channel. These registers provide a block of 8 current values from Channel X.
The following register is required for configuration:

- The AnalogInput01 register defines the channel used and the block index.
- The interval between measurement points is equal to a quarter of the defined X2X Link cycle.

Data type	Value
USINT	0 to 255

Programming example in ANSI C for uploading the curves:

```
#include <bur/plctypes.h>
#define ILEN 200

typedef struct {
      USINT                         data[ILEN];
}     curve_typ;
typedef struct {
      BOOL                          ok;
      UDINT                         serial;
      UINT                          id, hw, fwver;
      BOOL                          out[8];
      UINT                          delay;
      USINT                         i_addr;
      USINT                         i_ch1_in, i_ch2_in, i_ch3_in, i_ch4_in;
      USINT                         i_ch5_in, i_ch6_in, i_ch7_in, i_ch8_in;
      curve_typ                     curves[8];
      USINT                         switched;
}     cm8323_typ;
_LOCAL cm8323_typ                   cm;
_LOCAL USINT                        ventilNummer, adrPtr;

void _INIT up() {}

void _CYCLIC cycle() {
      ventilNummer = cm.i_addr & 0x07;
      adrPtr = cm.i_addr >> 3;

      if(cm.i_addr != 200 && ventilNummer <= 7) {
            cm.curves[ventilNummer].data[adrPtr * 8 + 0] = cm.i_ch1_in;
            cm.curves[ventilNummer].data[adrPtr * 8 + 1] = cm.i_ch2_in;
            cm.curves[ventilNummer].data[adrPtr * 8 + 2] = cm.i_ch3_in;
            cm.curves[ventilNummer].data[adrPtr * 8 + 3] = cm.i_ch4_in;
            cm.curves[ventilNummer].data[adrPtr * 8 + 4] = cm.i_ch5_in;
            cm.curves[ventilNummer].data[adrPtr * 8 + 5] = cm.i_ch6_in;
            cm.curves[ventilNummer].data[adrPtr * 8 + 6] = cm.i_ch7_in;
            cm.curves[ventilNummer].data[adrPtr * 8 + 7] = cm.i_ch8_in;
      }
}
```

I/O mapping of following data points for curve evaluation:

Data point	Variable
AnalogInput01	cm.i_addr
AnalogInput02	cm.i_ch1_in
AnalogInput03	cm.i_ch2_in
AnalogInput04	cm.i_ch3_in
AnalogInput05	cm.i_ch4_in
AnalogInput06	cm.i_ch5_in
AnalogInput07	cm.i_ch6_in
AnalogInput08	cm.i_ch7_in
AnalogInput09	cm.i_ch8_in

4.26.7.9.6.2 Uploading the current curves with CAN I/O

A current curve with 200 values is recorded for each channel. The interval between measurement points is equal to the value set in the 4.26.7.9.5.6 "TimeBase" register.

The following registers are needed in order to read the current curve recorded by the module in the Function model 254 - Bus controller:

- BlockID_Set
- BlockID_Act
- LineID_Set
- LineID_Act
- AnalogInput01 to AnalogInput04

Summary of set registers

Name:
AddressSet

This register is a summary of the LineID_Set and BlockID_Set registers.

Data type	Bit	Information
UINT	0 - 7	LineID_Set
	8 - 15	BlockID_Set

Summary of read registers

Name:
IndexAct

This register is a summary of the LineID_Act and BlockID_Act.

Data type	Bit	Information
UINT	0 - 7	LineID_Act
	8 - 15	BlockID_Act

Sets the channel number

Name:
BlockID_Set

The channel for the data stream can be selected in this register. The value of this register can be read using BlockID_Act.

Data type	Value	Information
USINT	0	Channel 1
	...	...
	7	Channel 8

Reads the channel number

Name:
BlockID_Act

Reads the BlockID_Set register. This register allows you to determine which channel is providing the current values in registers AnalogInput01 to AnalogInput04. If the selected channel or line does not exist, then this register returns the value 255.

Data type	Value	Information
USINT	0 to 7	Channel or line currently being used
	255	Invalid selection

Setting the line index

Name:
LineID_Set

The line index for the data stream can be selected in this register. The value of this register can be read using LineID_Act.

Data type	Value	Information
USINT	0 to 49	Line index currently used

Reading the line index

Name:
LineID_Act

Reads the LineID_Set register. This register allows you to determine which line is providing the current values in registers AnalogInput01 to AnalogInput04. If the selected channel or line does not exist, then this register returns the value 255.

If the channel number and index are in the valid range, then registers AnalogInput01 to AnalogInput04 provide a block of 4 current values for Channel X.
The index specifies which part of the current curve is represented by the block of 4 values:

Data type	Value	Information	
USINT	**Value X of the current curve**	**Index**	**Register**
	1	0	AnalogInput01
	...		...
	4		AnalogInput04
	5	1	AnalogInput01
	...		...
	197	49	AnalogInput01
	...		...
	200		AnalogInput04
	255	Invalid selection	

Analog input values - CAN I/O

Name:
AnalogInput01 to AnalogInput04

A current curve with 200 values is recorded for each channel. These registers provide a block of 4 current values from Channel X.
The following registers are required for configuration:

- The BlockID_Set register defines the channel used.
- The LineID_Set register defines the block index within the channel.
- The interval between measurement points is equal to the value set in the TimeBase register.

Data type	Value
USINT	0 to 255

4.26.7.9.6.3 Digital outputs

Name:
DigitalOutput
DigitalOutput01 to DigitalOutput08

Registers "DigitalOutput01" to "DigitalOutput08" set the output value of Channels 1 to 8.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput01	0 or 1	Output value of digital output 01
...		...	
7	DigitalOutput08	0 or 1	Output value of digital output 08

4.26.7.9.6.4 Status of the outputs

Name:
StatusInput01

This register indicates whether a switching point has been found for a channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Switching point	0	Channel 1 was not switched or no switching point was found
		1	Switching point found for Channel 1
...		...	
7	Switching point	0	Channel 8 was not switched or no switching point was found
		1	Switching point found for Channel 8

4.26.7.9.6.5 Module status

Name:
StatusInput02

The current module status is indicated in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Reserved	0	
3	Overload cutoff	0	No overcurrent
		1	Overcurrent cutoff activated
4 - 7	Reserved	0	

4.26.7.9.6.6 Switching delay of channels

Name:
StatusOutput01

2 bits of this register are used to set the switching delay for each channel. Values of the switching delay are specified in quarter-steps of the X2X Link cycle.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Switching delay of channel 1	00	No delay
		01	1/4 of the X2X Link cycle
		10	2/4 of the X2X Link cycle
		11	3/4 of the X2X Link cycle
2 - 3	Switching delay of channel 2	x	For possible values, see channel 1.
...		...	
14 - 15	Switching delay of channel 8	x	For possible values, see channel 1.

4.26.7.9.6.7 Reads actual values of the current

Name:
Current01 to Current08

These registers are used to read the actual value of the current from channels 1 to 8. These values have no units and are used only as characteristic values. A more precise, compensated current measurement is not possible using this module.

Relationship between register name and channel number:

Register name	Channel number
Current01	Actual value of the current of Channel 1
...	...
Current08	Actual value of the current of Channel 8

If an output is switched off, the corresponding register returns the value 0. After the output is switched on, valid current measurements are not available on the module until after two X2X Link cycles. The measurements in the registers are delayed by two cycles to account for this.

When the output is switched on, the corresponding bit in the StatusCurrent register can be used to check whether the register contains valid measurements. The first measured value is provided with the rising edge of this bit.

Data type	Value	Information
USINT	0	Output is switched off
	1 to 255	Current value

4.26.7.9.6.8 Checking for measured values

Name:
StatusCurrent
StatusCurrent01 to StatusCurrent08

These registers can be used to check whether registers Current01 bis Current08 contain valid measured values.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusCurrent01	0	Output switched off
		1	Current value of Channel 01 is valid
...		...	
7	StatusCurrent08	0	Output switched off
		1	Current value of Channel 08 is valid

4.26.7.9.7 Configuring dI and dt

4.26.7.9.7.1 Procedure - Searching for switching points

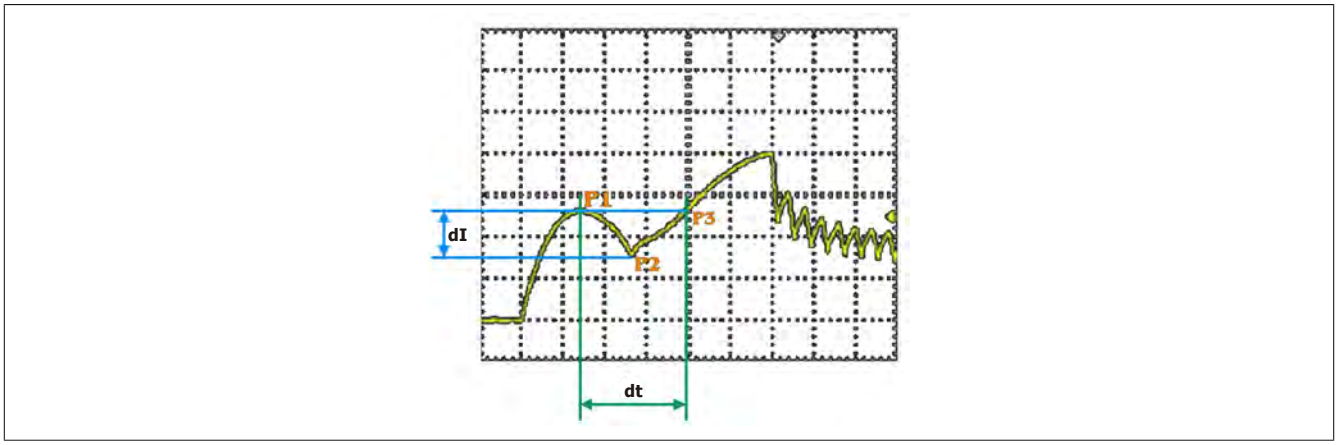


Figure 499: Searching for switching points

The current in the inductance gradually rises when the valve is switched on. The valve starts to move mechanically at a certain point. This process becomes noticeable due to a current dip that occurs as a result of the braking voltage (anti-EMF) (point P1).

When this mechanical process is complete, the current returns to its original curve and continues to rise (point P2).

Point P3 and point P1 have the same current value, but different times.

A valid low-point, which simultaneously corresponds to the switching point, must meet the following criteria:

- Point 2 must be lower than P1 by dI
- The time between P1 and P3 must be longer than dt

4.26.7.9.7.2 Configuration example for dI and dt with trace data from Automation Studio

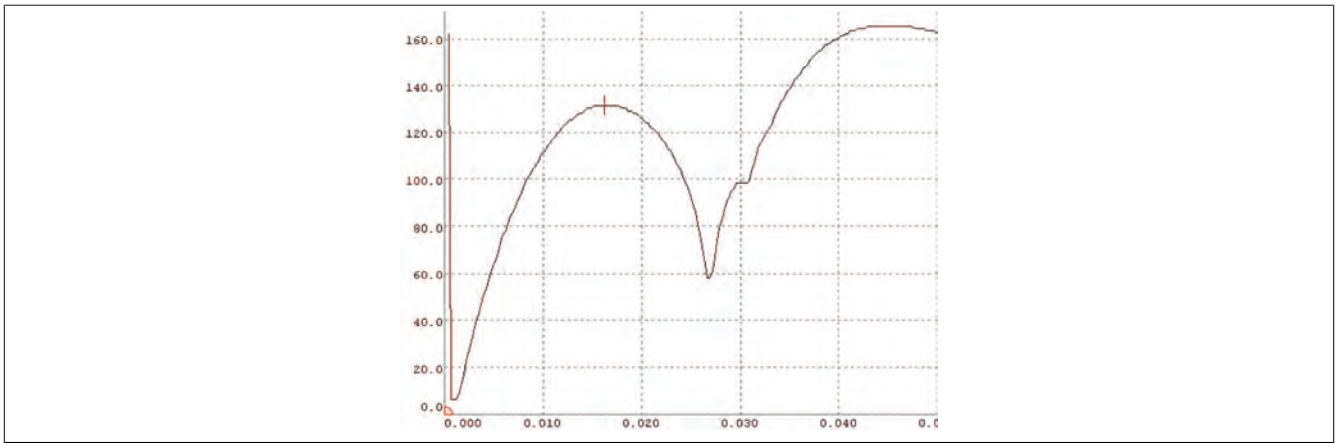


Figure 500: Search for the switching point with trace data from Automation Studio

The difference between the "current high-point" (P1 = 131) and the subsequent low-point (P2 = 58) is calculated (P1 - P2 = 73). The module compares this difference to the configured parameter dI.

If the difference measured by the module is larger than the configured dI value, then the first condition for a switching point search is met:

- In the module, the parameter dI should therefore be set to at least 72.

The next criteria is the time between P1 and P3. This must be larger than the value set for the parameter dt.

According to the trace data, this is 4.43 ms:

- In the module, the parameter dt should therefore be set to 43 (4430 µs / 100 µs).

With that, the second condition is met and a valid switching point can be detected.

It is recommended to avoid setting values all the way to the limits, since valves and relays change mechanically over time, which can lead to faulty readings (unless you wish to detect every minor deviation from the reference curve).

4.26.7.9.7.3 Modified switching point search (curvature method)

The method described (searching for and detecting switching points by locating low-points in the current trace) may not provide the desired level of reliability for certain types of valves and under certain conditions (e.g. pneumatic pressure).

For this reason, an alternative method of switchover detection is provided. This method is based on an evaluation of the curvature of the current curve. In the module configuration, the user can select which method to use for switchover detection (see 4.26.7.9.5.3 "Module configuration").

The modified switching point search calculates the first derivative (slope) and then the second derivative (curvature) for every point in the current curve. At the switching point this second derivative has a local maximum, which is found by the module. More specifically, in order to improve the signal/noise ratio, a summation window is moved over the second derivative and the maximum of this summation is searched for.

This is not only valid when the current trace itself has a more or less low minimum in the switching point, but also in cases where the current increase only levels-out in the area of the switching point, but never becomes negative. Therefore, it can be said that the curvature method should generally be more sensitive.

Like the switching point search with the low-point method, valid switching points are configured using the parameters dI and dt. The meaning of these parameters is different here, however.

- dI - minimum curvature sum
- dt - width of the summation window in 1/4 X2X Link cycles

Meaningful values for this parameter can no longer be obtained simply by reading / measuring the current trace. That is why the module provides, in addition to the switching point (200th value of the current curve), also the following measurement and calculation values that can be used for the configuration:

Value X of the current curve	Description
1	1. Value of the current curve
:	:
197	Peak position of the first valid or highest invalid curvature peak
198	Height of the peak sum of the first valid or highest invalid peak
199	Width of the first valid or highest invalid peak (**Important:** not standardized to 100 µs)
200	255 at invalid peak, otherwise peak position in the current trace

When a valid maximum curvature has been found (Value 198 ≥ dI) then Values 197 to 199 represent the position (= Value 200), height and width of the first maximum that meets the criteria. Any higher and/or wider maximum that occurs later will not be found!

If no maximum curvature reaches the necessary height, then Values 197 through 200 represent the highest invalid maximum.

Determining the parameters dI and dt

dI << Value 198	Set dI much lower than 198
dt ≈ Value 199	dt should be set approximately the same as Value 199 **Note**: Maximum value for dt = 16

A certain amount of jitter in Value 198 must be assumed due to the high sensitivity of the modified switching point search. It is therefore recommended to monitor Value 198 over several switching cycles before setting dI with a safety clearance from the lowest monitored value.

As you can see in the examples below, the switching point peak is a number of times higher than any other peak in the summation curves.

The switching point peak is also still the first peak that occurs in the positive range. Therefore, it should not be a problem to set dI far enough from the minimum of the Value198 and far above the highest peak that arises from the noise (or valve chatter).

Example 1:

Configuration example of the modified switching point detection for a valve with a distinctive switching point.

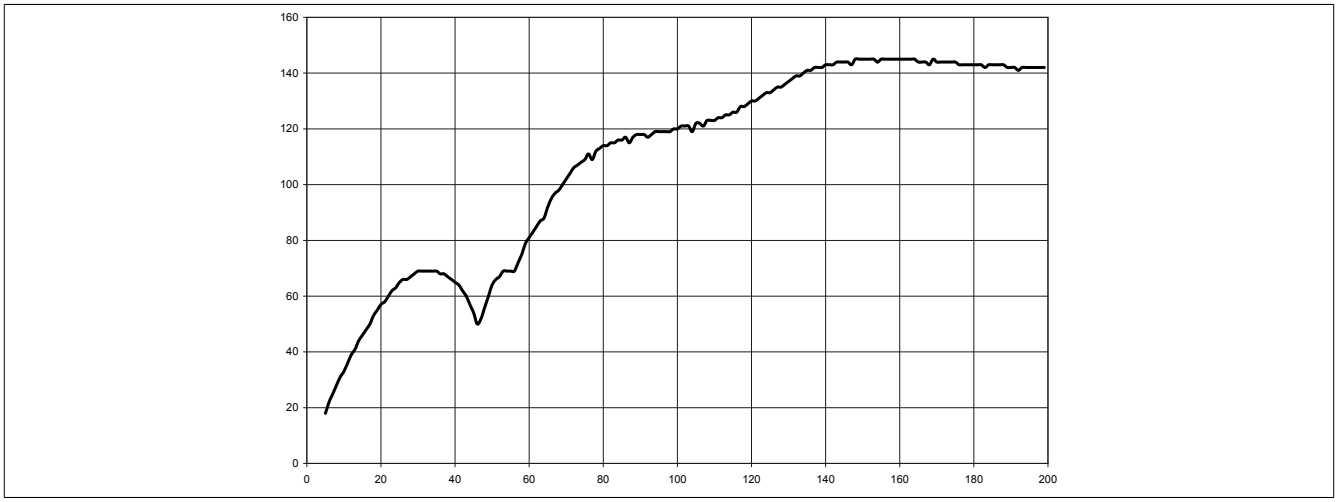


Figure 501: Example 1 - Valve current

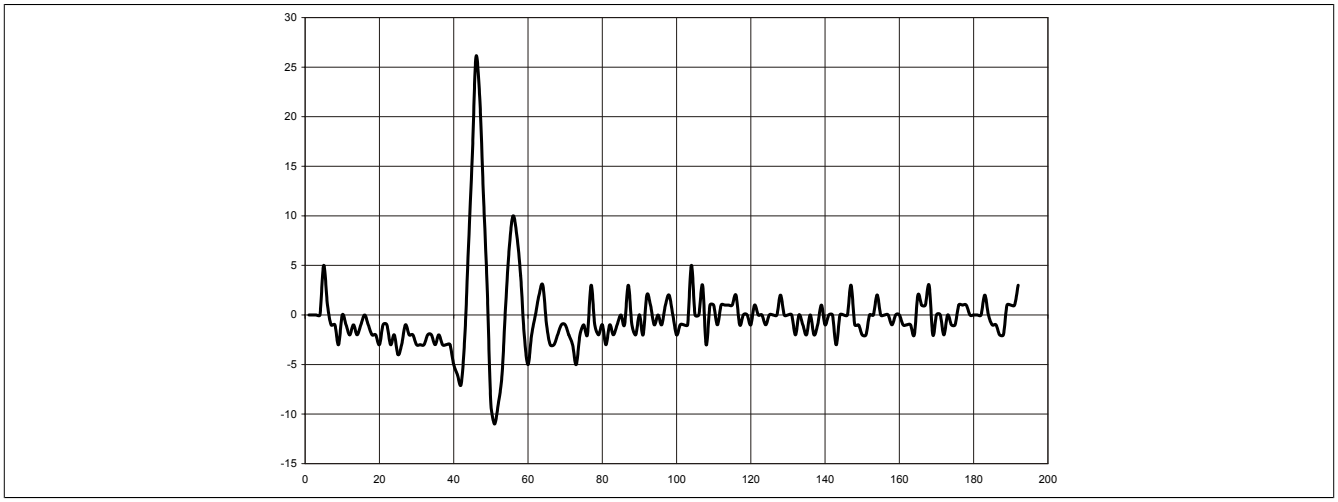


Figure 502: Example 1 - Calculated curvature (2nd derivative) of the current curve

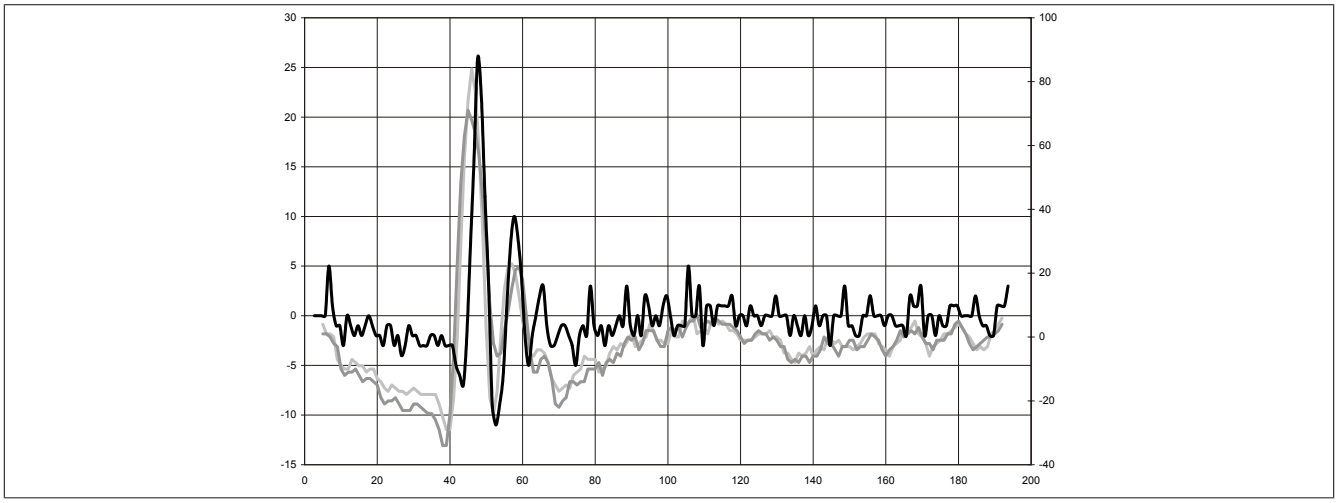


Figure 503: Example 1 - Calculated curvature (2nd derivative) of the current curve including overlapping sum with 3 different window widths

Example 2:

Configuration example of the modified switching point detection for a valve with a faintly distinctive switching point.

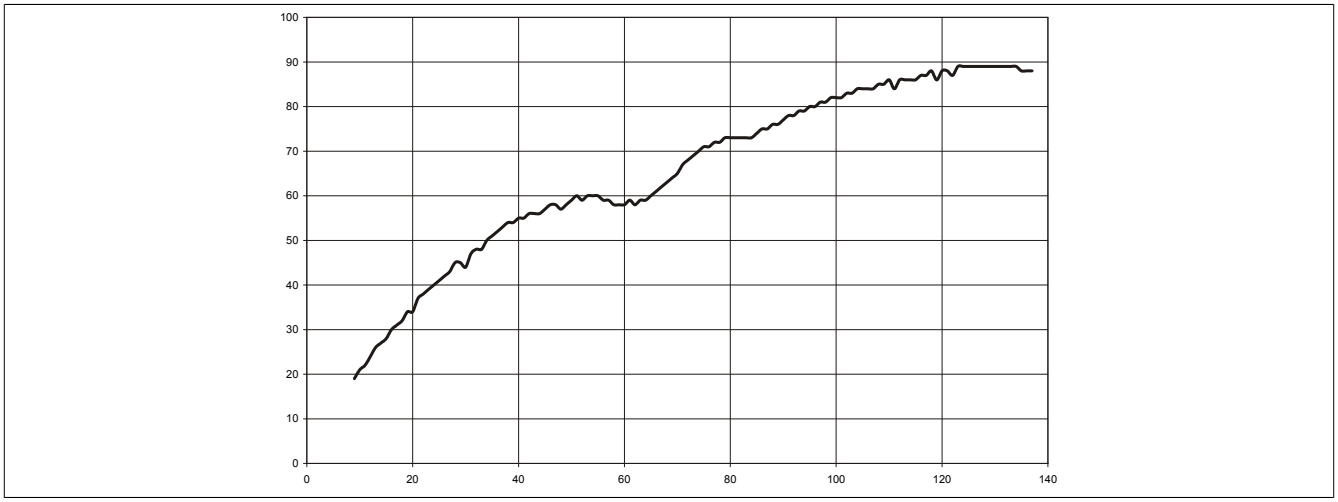


Figure 504: Example 2 - Valve current

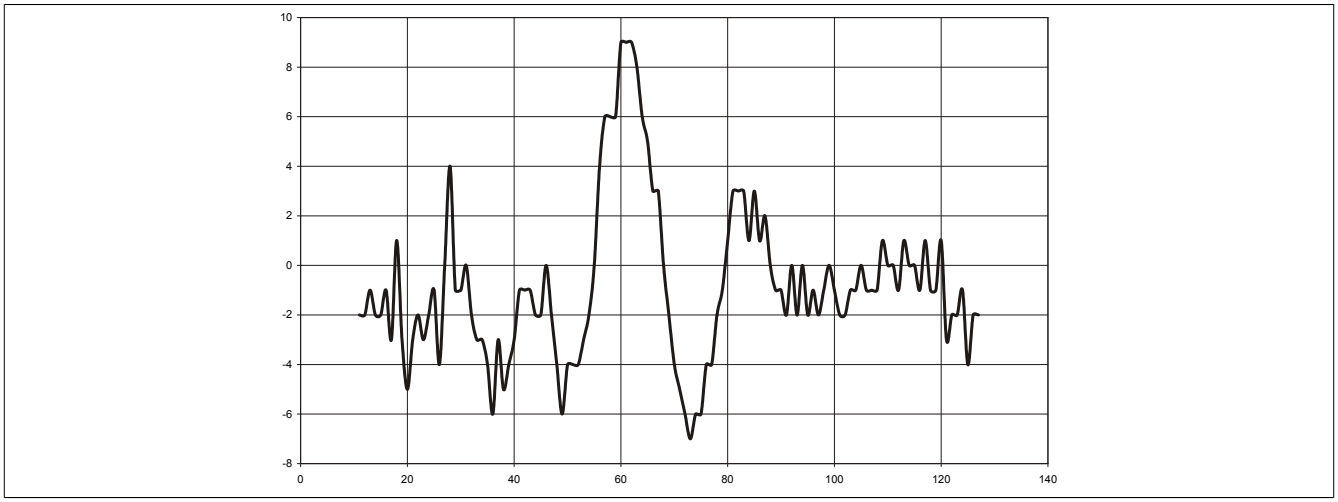


Figure 505: Example 2 - Calculated curvature (2nd derivative) of the current curve

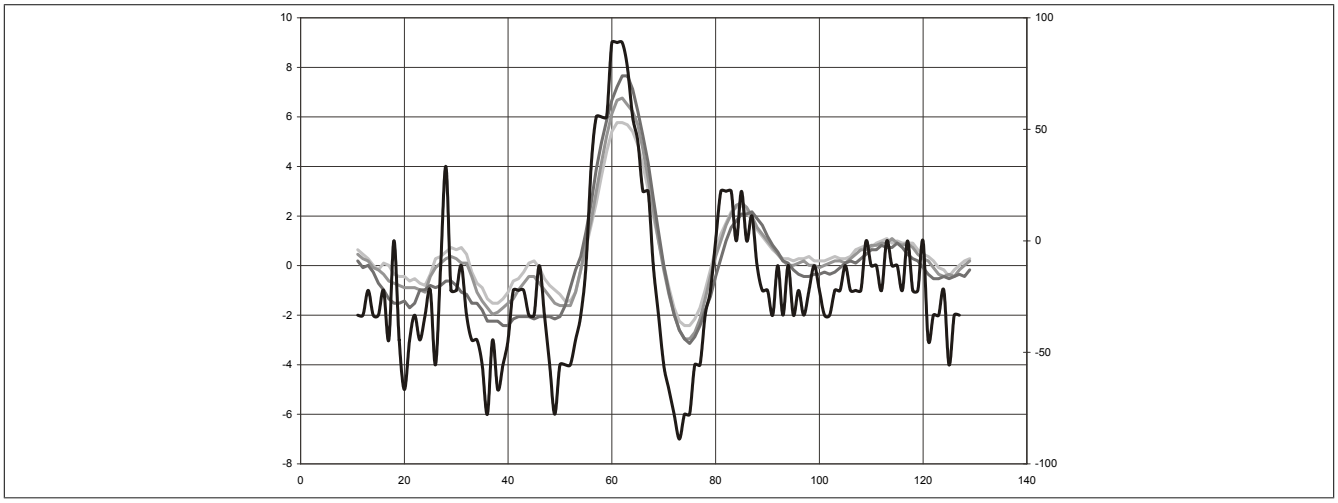


Figure 506: Example 2 - Calculated curvature (2nd derivative) of the current curve including overlapping sum with 3 different window widths

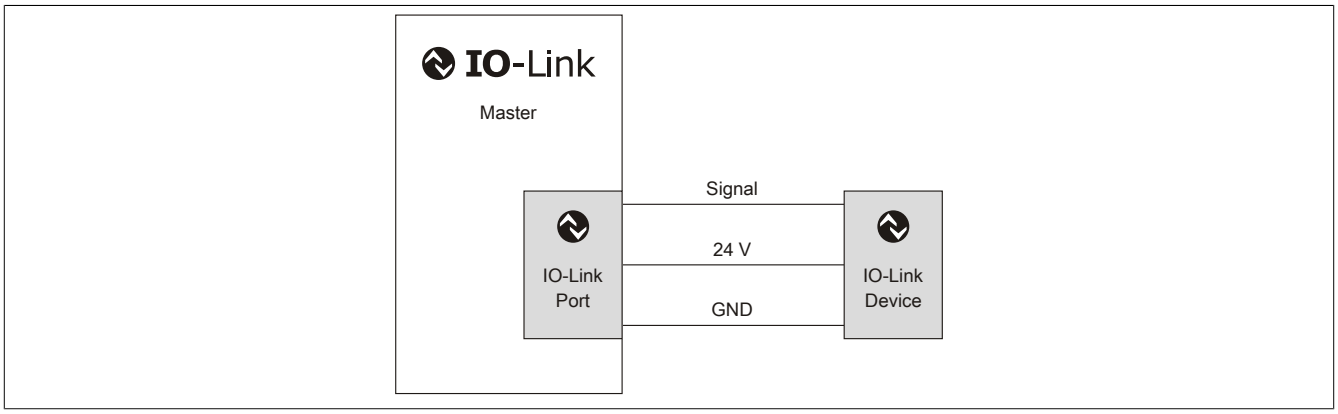
4.26.8 X20DS4387

4.26.8.1 General information

IO-Link is a standardized communication system for connecting intelligent sensors and actuators in an automation system. The standardization includes electrical connection data as well as a digital communication protocol, which is used by the sensors and actuators in the automation system for data exchange.

An IO-Link system consists of an IO-Link master and one or more IO-Link devices, i.e. sensors and actuators. The IO-Link master makes the interface available for higher level control and controls communication with the connected IO-Link devices.

An IO-Link device is an intelligent sensor or actuator. With regard to IO-Link, "intelligent" means that a device possesses a series number or parameter data (sensitivity, switching delays or characteristic curves), which can be written to or read via the IO-Link protocol.



Process optimization

The use of intelligent sensors and actuators contributes to process optimization. Process optimization means that downtimes should be kept as short as possible. These consist mainly of standstills due to errors and setup times.

Integrated communication down to the IO-Link devices offers many advantages in error diagnostics. Errors are detected much faster than before. If a sensor or actuator must be replaced, lengthy configuration work is no longer necessary after the change thanks to a potentiometer, or a configuration tool and laptop. After changing the sensor/actuator, the parameters are automatically transferred to the sensor.

This parameter download is not only beneficial when errors occur. It can also be used for changing parameters when a load change is performed. This shortens setup times, making product changes and small batches more economical.

Integration of IO-Link in X20 System

IO-Link is integrated in the X20 system using this digital module. All 4 channels are IO-Link interfaces, but can also be used as standard inputs or outputs. The specified 3-wire connections can be ideally implemented thanks to the X20 connector system with 12 terminal points per module. All specified transfer rates are also supported.

POWERLINK integration

IO-Link doesn't stop at the I/O module. It must be integrated in the higher-level bus system to fully utilize the benefits. When using POWERLINK, access is made possible via device description files in XML format.

- 4 IO-Link interfaces per module
- Each interface can be configured as a standard input or output
- Seamless integration in POWERLINK
- Supports all transfer rates

4.26.8.2 Order data

Model number	Short description	Figure
	Other functions	
X20DS4387	X20 digital signal module, 4x IO-Link master, 4 digital channels configurable as inputs or outputs, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 645: X20DS4387 - Order data

4.26.8.3 Technical data

Product ID	X20DS4387
Short description	
I/O module	IO-Link master with 4 IO-Link interfaces
General information	
B&R ID code	0xA38E
Status indicators	IO-Link, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
IO-Link operating state	Yes, using status LED and software
C/Q status	Yes, using status LED and software
Cable specification	
Cable type	3-pin standard sensor cable
Cable length	Max. 20 m
Line capacitance	Max. 3 nF
Loop resistance	Max. 6 Ω
Power consumption	
Bus	0.01 W
Internal I/O	1.6 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - IO-Link	Yes
IO-Link - IO-Link	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Sensor/Actuator supply	
Voltage	I/O supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 0.3 A	Max. 1 VDC
Power consumption	Max. 9 W per interface
Short circuit protection	Yes
IO-Link in master mode	
Transfer rates	
COM1	4.8 kbaud
COM2	38.4 kbaud
COM3	230.4 kbaud
Limits for COM3	
Max. connection capacity	47 nF (cable + device)
Max. load	100 Ω / 0.3 A
Data format	1 start bit, 8 data bits, 1 parity bit (even), 1 stop bit
Bus level	24 VDC (active), 0 VDC (resting voltage)
IO-Link device supply	24 VDC / max. 0.3 A per interface (protected)
IO-Link in master mode or in SIO mode "digital output"	
Design	Bipolar, positive and negative switching
Diagnostics	Output monitoring with 100 ns delay and internal semiconductor protection with 100 µs delay

Table 646: X20DS4387 - Technical data

Product ID	X20DS4387
Peak short circuit current	<1.5 A
Residual voltage	<1.5 VDC at nominal current 0.2 A
Switching voltage	I/O supply minus voltage drop for short circuit protection and semiconductor switch
Voltage drop on semiconductor switch	Max. 1.5 VDC at 0.2 A
Switching frequency	Typ. 25 kHz 300 kHz in IO-Link master mode
Switching delay	
0 -> 1	<10 µs
1 -> 0	<10 µs
Switching on after overload or short circuit cutoff	Approx. 10 ms (depends on the module temperature)
Braking voltage when switching off inductive loads	Typ. 52 VDC
Isolation voltage between IO-Link and bus	500 V_{eff}
IO-Link in SIO mode "digital output"	
Nominal voltage	24 VDC
Nominal output current	0.2 A
Total nominal current	0.4 A
Output circuit	Sink or source
Output protection	Thermal cutoff if overcurrent or short circuit occurs, integrated protection for switching inductances
Actuator supply	24 VDC / max. 0.3 A per interface (protected)
IO-Link in SIO mode "digital input"	
Nominal voltage	24 VDC
Input filter	
Hardware	100 ns
Software	-
Input circuit	Sink
Sensor supply	24 VDC / max. 0.3 A per interface (protected)
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 5 mA
Input resistance	Typ. 4.8 kΩ
Switching threshold	
Low	<8 VDC
High	>13 VDC
Isolation voltage between IO-Link and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 45°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately, Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 646: X20DS4387 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

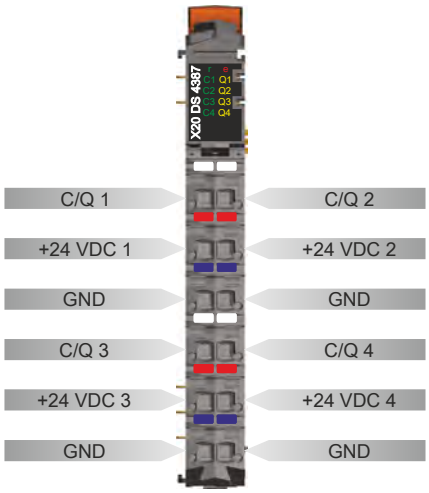
4.26.8.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

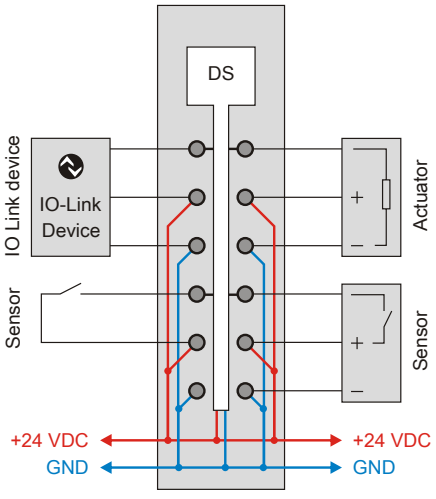
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Warning / error for an IO-Link interface
	1 - 4	Green/Red	Off	Interface in SIO mode
			Green	Interface in IO-Link mode
			Red	Output overloaded (short circuit, temperature)
	1 - 4	Orange		Input/output status of the corresponding IO-Link interface

1) Depending on the configuration, a firmware update can take up to several minutes.

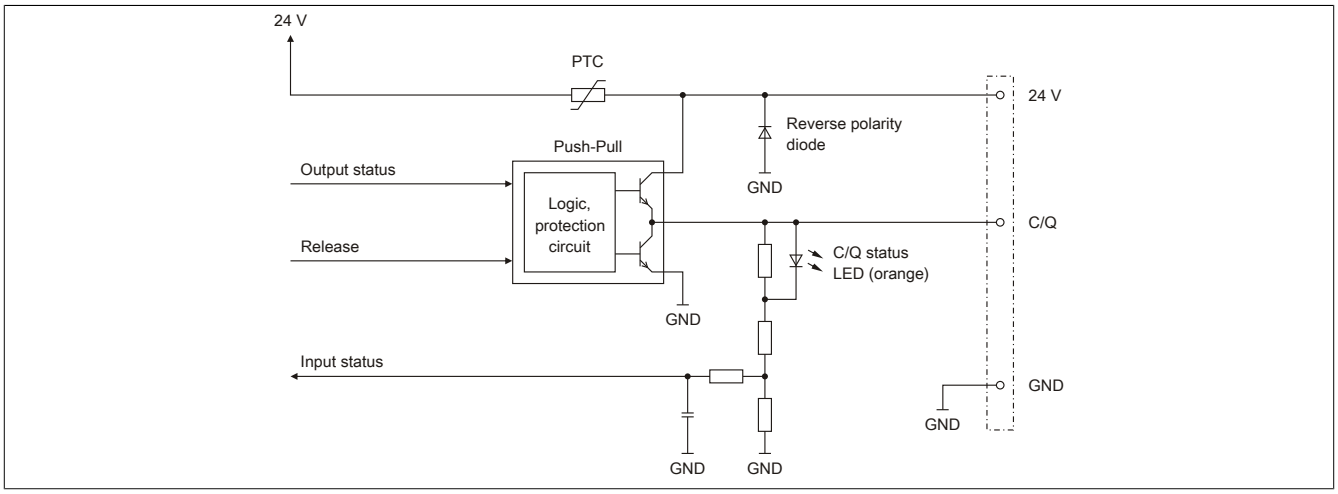
4.26.8.5 Pinout



4.26.8.6 Connection example



4.26.8.7 Output circuit diagram



4.26.8.8 Register description

4.26.8.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.8.8.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Interface operation						
321 + (N-1) * 256	Control0N (index N = 1 to 4)	USINT				●
328 + (N-1) * 256	StatusEvents0N (index N = 1 to 4)	U(S)INT	●			
328 + (N-1) * 256	CycleLength0N (index N = 1 to 4)	UINT	●			
342 + (N-1) * 256	DeviceId0N (index N = 1 to 4)	UDINT	●			
336 + (N-1) * 256	FunctionId0N (index N = 1 to 4)	UINT	●			
332 + (N-1) * 256	VendorId0N (index N = 1 to 4)	UINT	●			
255 + N	DataIn01_N (index N = 01 to 27)	USINT	●			
511 + N	DataIn02_N (index N = 01 to 27)	USINT	●			
767 + N	DataIn03_N (index N = 01 to 27)	USINT	●			
1023 + N	DataIn04_N (index N = 01 to 27)	USINT	●			
255 + N	DataOut01_N (index N = 01 to 30)	USINT			●	
511 + N	DataOut02_N (index N = 01 to 30)	USINT			●	
767 + N	DataOut03_N (index N = 01 to 30)	USINT			●	
1023 + N	DataOut04_N (index N = 01 to 30)	USINT			●	
SIO mode						
356 + (N-1) * 256	ChInputFilter0N (index N = 1 to 4)	USINT				●
256 + (N-1) * 256	Digital inputs	USINT	●			
	DigitalInput0N (index N = 1 to 4)	Bit 0				
256 + (N-1) * 256	Digital outputs	USINT			●	
	DigitalOutput0N (index N = 1 to 4)	Bit 0				
Boot configuration						
14852 + N*8	ODW_Data_N (index N = 0 to 127)	UDINT				●
14848 + N*8	ODW_Target_N (index N = 0 to 127)	UDINT				●
Runtime configuration						
7680	ParameterCtrlIn	UINT	●			
7680	ParameterCtrlOut	UINT			●	
7684	ParameterCmdIn	UDINT		●		
7684	ParameterCmdOut	UDINT			●	
7688 + N*4	ParameterDataIn_N (index N = 0 to 57)	UDINT	●[1)]	●		
7688 + N*4	ParameterDataOut_N (index N = 0 to 57)	UDINT			●[1)]	●
Errors and warnings						
325 + (N-1) * 256	ErrorsWarnings0N (index N = 1 to 4)	USINT	●			
IO-Link events						
7937	EventPortSeq	USINT	●			
7939	EventQualifier	USINT	●			
7942	EventCode	UINT	●			
7952	EventQuit	USINT			●	

1) Only parameters with index = 0

4.26.8.8.3 Function model 256 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Interface operation							
321 + (N-1) * 256	-	Control0N (index N = 1 to 4)	USINT				●
328 + (N-1) * 256	4 + (N-1) * 8	StatusEvents0N (index N = 1 to 4)	USINT	●			
328 + (N-1) * 256	-	CycleLength0N (index N = 1 to 4)	UINT		●		
342 + (N-1) * 256	-	DeviceId0N (index N = 1 to 4)	UDINT		●		
336 + (N-1) * 256	-	FunctionId0N (index N = 1 to 4)	UINT		●		
332 + (N-1) * 256	-	VendorId0N (index N = 1 to 4)	UINT		●		
255 + N	N - 1	DataIn01_N (Index 0N = 1 to 4)	USINT	●			
511 + N	7 + N	DataIn02_N (Index 0N = 1 to 4)	USINT	●			
767 + N	15 + N	DataIn03_N (Index 0N = 1 to 4)	USINT	●			
1023 + N	23 + N	DataIn04_N (Index 0N = 1 to 4)	USINT	●			
255 + N	N - 1	DataOut01_0N (index N = 1 to 4)	USINT			●	
511 + N	3 + N	DataOut02_0N (index N = 1 to 4)	USINT			●	
767 + N	7 + N	DataOut03_0N (index N = 1 to 4)	USINT			●	
1023 + N	11 + N	DataOut04_0N (index N = 1 to 4)	USINT			●	
SIO mode							
356 + (N-1) * 256	-	ChInputFilter0N (index N = 1 to 4)	USINT				●
256 + (N-1) * 256	(N-1) * 8	Digital inputs	USINT	●			
		DigitalInput0N (index N = 1 to 4)	Bit 0				
256 + (N-1) * 256	(N-1) * 4	Digital outputs	USINT			●	
		DigitalOutput0N (index N = 1 to 4)	Bit 0				
Boot configuration							
14852 + N*8	-	ODW_Data_N (index N = 0 to 127)	UDINT				●
14848 + N*8	-	ODW_Target_N (index N = 0 to 127)	UDINT				●
Runtime configuration							
7680	-	ParameterCtrlIn	UINT		●		
7680	-	ParameterCtrlOut	UINT				●
7684	-	ParameterCmdIn	UDINT		●		
7684	-	ParameterCmdOut	UDINT				●
7688 + N*4	-	ParameterDataIn_N (index N = 0 to 57)	UDINT		●		
7688 + N*4	-	ParameterDataOut_N (index N = 0 to 57)	UDINT				●
Errors and warnings							
325 + (N-1) * 256	5 + (N-1) * 8	ErrorsWarnings0N (index N = 1 to 4)	USINT	●			
IO-Link events							
7937	-	EventPortSeq	USINT		●		
7939	-	EventQualifier	USINT		●		
7942	-	EventCode	UINT		●		
7952	-	EventQuit	USINT				●

1) The offset specifies the position of the register within the CAN object.

4.26.8.8.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.26.8.8.4 Limitations

The I/O module offers extensive function and configuration options. Many of these options require cycle data. The amount of cycle data required depends on the following parameters:

- Number of interfaces in use
- Use of events
- Runtime configuration in the cycle data

Take note that the amount of cycle data available for each I/O module used in the system is limited:

Sum of the input data:	29 bytes
Sum of the output data:	30 bytes

Runtime configuration and events

Each I/O module requires the following amounts of cycle data for runtime configuration and events, if enabled:

Activated function	Input	Output
Runtime configuration in the cycle data	6	10
Events	4	1

Interface data

The following amounts of cyclic data are required for each interface being used:

Functionality	Operating state							
	OPERATE		DIGINPUT		DIGOUTPUT		INACTIVE	
	Input	Output	Input	Output	Input	Output	Input	Output
Payload	0 to 27[1)]	0 to 30[1)]	1	-	-	1	-	-
Status information	2	-	2	-	2	-	-	-

1) User configurable

4.26.8.8.5 Interface operation

4.26.8.8.5.1 Communication mode

Name:
Control01 to Control04

Writing to this register defines the desired state of the IO-Link device. This register can be used to define if the IO-Link device should be operated in "normal" communication mode (OPERATE), as a digital input (DIGINPUT) or as a digital output (DIGOUTPUT).

Switching to SIO mode can make sense for IO-Link devices that only transfer digital information anyway (e.g. light curtains) but after the basic configuration should be faster than is possible in "normal" communication mode. A parameter configuration for the object directory can also be made in SIO mode.

To deactivate an interface, INACTIV should be used.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Communication mode	0	INACTIV
		1	DIGINPUT
		2	DIGOUTPUT
		10	OPERATE
4 - 7	Reserved	-	

4.26.8.8.5.2 Operating state

Name:
StatusEvents01 to StatusEvents04

The actual status of communication between the module and the IO-Link device is indicated in this register. Additionally, the number of events read by the IO-Link device are also counted in this register.

Data type	Value
USINT[1)]	See bit structure.
UINT	

1) In the bus controller or standard function model, of communication mode = INACTIV

Bit structure:

Bit	Description	Value	Information
0 - 3	Status of the IO-Link device	x	See table below
4 - 7 or 15	Event counter from the respective IO-Link device	x	

Status of the IO-Link device

Value	ID	Description
0	INACTIVE	Interface is active: No communication and signal output or input. This state is not changed automatically.
1	DIGINPUT	SIO input mode: The interface acts like a digital input
2	DIGOUTPUT	SIO output mode: The interface acts like a digital output
4	ESTABLISHCOMM	Establishing connection to IO-Link device. This state remains as long as a device is not found.
5	INITMASTER	Consecutive states experienced during booting and configuration of an IO-Link device.
6	INITDEVICE	
7	INITOPERATE	
8	PREOPERATE	
9	READYTOOPERATE	Waiting for valid data from the IO-Link device. This state can follow the OPERATE state if the device reports during operation that it cannot send any more valid data.
10	OPERATE	Communication with the IO-Link device via serial protocol. Valid data is exchanged.
11	COMSTOP	The IO-Link interface is reinitialized. The ESTABLISHCOMM state follows this state.
12	FALLBACK	For switching to SIO mode
13	STARTUP	IO-Link device restart
14	SIO	Switching to SIO mode

States with a gray background are applied continuously, all others are intermediate states. An exception is the state ESTABLISHCOMM (4): This state is applied continuously if there is no device connected.

Dynamic values from the IO-Link device make up the input data for an IO-Link interface if one of the states DIGINPUT, DIGOUTPUT or OPERATE has been reached. These states can also be exited when errors occur. The device is restarted if a fatal error occurs, which means the state reverts back to ESTABLISHCOMM. Another possibility is that there is no new data being read from the device in the OPERATE state. In this case, the state changes to READYTOOPERATE and waits for new data.

During the first boot procedure, the module sends the value 0 for the inputs of an IO-Link interface. If the states DIGINPUT, DIGOUTPUT or OPERATE are exited, then the inputs are frozen at the most recently read value until valid data is able to be read from the device again.

4.26.8.8.5.3 Length of the I/O cycle

Name:
CycleLength01 to CycleLength04

The value in this register specifies how many X2X cycles are required on the respective interface for a the IO-Link process data to be completely updated.

The module automatically selects the best possible IO-Link cycle time per interface for the connected IO-Link device. This is always a multiple of the X2X cycle time. The cycle times of the 4 IO-Link interfaces are independent of one another.

Data type	Value
UINT	0 to 65535

4.26.8.8.5.4 Reading

Name:
DeviceID01 to DeviceID04

This register contains the IO-Link device ID assigned by the manufacturer. The device ID can be read for every IO-Link interface.

Data type	Value
UDINT	0 to 4,294,967,295

4.26.8.8.5.5 Function ID

Name:
FunctionID01 to FunctionID04

This register contains the IO-Link function ID assigned by the manufacturer. The function ID can be read for every IO-Link interface.

Data type	Value
UINT	0 to 65535

4.26.8.8.5.6 IO-Link vendor ID

Name:
VendorID01 to VendorID04

This register contains the IO-Link vendor ID. The ID can be read for every IO-Link interface.

Data type	Value
UINT	0 to 65535

4.26.8.8.5.7 Cyclic input data

Name:
DataIn01_01 to DataIn01_27 (bus controller function model: up to xx01_04)
...
DataIn04_01 to DataIn04_27 (bus controller function model: up to xx04_04)

This register contains the cyclic input data for the respective interface.

Data type	Value
USINT	0 to 255

4.26.8.8.5.8 Cyclic output data

Name:
DataOut01_01 to DataOut01_30 (bus controller function model: up to xx01_04)
...
DataOut04_01 to DataOut04_30 (bus controller function model: up to xx04_04)

This register contains the cyclic output data for the respective interface.

Data type	Value
USINT	0 to 255

4.26.8.8.6 SIO mode

The IO-Link interface can be used like a digital input or output in SIO mode. To activate the SIO mode, the operating state must be set in the 4.26.8.8.5.1 "Control0x" register to DIGINPUT or DIGOUTPUT. Runtime configuration is not possible during operation in SIO mode, however the boot configuration can be used.

4.26.8.8.6.1 Digital input filter

Name:
ChInputFilter01 to ChInputFilter04

When used as a digital input, a filter time can be configured in this register. Valid values for the filter time are 0 and 2 to 250. A value of 0 will deactivate the filter. Other values specify the filter time as a multiple of 0.1 ms. The default value is 10 (= 1 ms).

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

4.26.8.8.6.2 Digital inputs

Name:
DigitalInput01 to DigitalInput04

These registers display the input states of the digital inputs individually for each channel.

Data type	Value
USINT	See bit structure.

Bit	Name	Value	Information
0	DigitalInput0x	0 or 1	Input state - Digital input x
1 - 7	Reserved	-	

4.26.8.8.6.3 Digital outputs

Name:
DigitalOutput01 to DigitalOutput04

These registers display the output states of the digital outputs individually for each channel.

Data type	Value
USINT	See bit structure.

Bit	Name	Value	Information
0	DigitalOutput0x	0	Digital output x reset
		1	Digital output x set
1 - 7	Reserved	-	

4.26.8.8.7 Parameter

IO-Link devices can provide user parameters. There are two ways to access these parameters:

- Boot configuration
- Runtime configuration

4.26.8.8.7.1 Boot configuration

The values specified by the user are transferred during the boot procedure (or when the IO-Link device is connected).

Up to 32 parameter values can be specified for each IO-Link interface. 1, 2, and 4 byte parameters are supported.

The boot configuration can be used in the operating states OPERATE, DIGINPUT and DIGOUTPUT.

The following specifications are necessary for parameters that should be set during the boot procedure:

Name	Range of values	Description
Index	0 to 65535	Parameter index according to device manufacturer's specifications
Subindex	0 to 255	Parameter sub index according to device manufacturer's specifications
Length	1, 2, 4	Length of data in bytes
Data	0 to 4,294,967,295	Data to be written. Only low-order bytes are used for 1 or 2 byte parameters.

4.26.8.8.7.2 Runtime configuration

The runtime configuration can also be made after the IO-Link device has booted up. Parameters can be read or written.

The runtime configuration can take place in the cyclic data or through acyclic communication (function blocks AsIOAccRd and AsIOAccWr).

Runtime configuration is available for interfaces in the OPERATE state.

The following specifications are necessary for accessing parameters:

Name	Range of values	Description
Interface	0, 1, 2, 3	Addressed interface of the module
Sequence number	0 to 15	A change to this value indicates a new task. The sequence number is set identically to the value of the request in the response message.
Index	0 to 65535	Parameter index according to device manufacturer's specifications.
Subindex	0 to 255	Parameter sub index according to device manufacturer's specifications.
Length	0 to 228 (229)	Length of data in bytes. Up to 228 bytes are supported for write access and 229 bytes for read access. The length does not have to be specified when requesting a read access (the device reports the length of the read data).
Data		IO-Link supports up to 228 (229) bytes of data each time a parameter is accessed. The length is limited to 1, 2 or 4 bytes in the cyclic data with boot configuration and runtime configuration. The full data range can be used with acyclic runtime configuration (AsIOAcc Library).
Read/write	0, 1	For the request to the IO-Link device. 0 → read 1 → write
Errors	0, 1	Defined in the response from the IO-Link device. 0 → No error occurred 1 → Error When an error occurs, the first two bytes of data are contained in the error code (the reported length is 2).
Sequence number	0 to 15	

Access to an IO-Link device's parameters occurs via a request and subsequent response from the device.

A new request is detected due to a changed sequence number. Therefore, the sequence number must be the last data item that is written.

The response contains the sequence number of the request.

The length is not relevant for a read request. It is automatically determined by the IO-Link device and reported in the response message.

If an error occurs (e.g. due to accessing an index or sub index that does not exist), this is signaled by a set error bit in the response. The error response always has a length of 2. These 2 bytes contain the manufacturer-specific error code.

4.26.8.8.8 Object directory access

Writing to the corresponding registers 4.26.8.8.8.4 "ParameterCmdOut" and 4.26.8.8.8.2 "ParameterCtrlOut" defines and sends an order for reading or writing an IO-Link object.

Procedure for sending an order

- Define register 4.26.8.8.8.4 "ParameterCmdOut" by entering the length, index and subindex
- During write access, write the required parameter data that is to be stored in the object directory to registers 4.26.8.8.8.6 "ParameterDataOut_0" to ParameterDataOut_57.
- Define register 4.26.8.8.8.2 "ParameterCtrlOut" by entering the interface number, read/write ID and the incremental sequence number. Additionally, an error bit can be configured during read access.

The module detects when the sequence number changes and accepts the order. Communication with the IO-Link device takes place.

When evaluating read/write access, the following is available from the register 4.26.8.8.8.1 "ParameterCtrlIn":

- Access sequence number
- Access interface number
- Type of access
- Payload length for read access to values smaller than 15 bytes
- Read access error bit

When evaluating read/write access, the following is available from the register 4.26.8.8.8.3 "ParameterCmdIn":

- Payload length for read access
- Access index and subindex

When evaluating read access, the following is available from the register 4.26.8.8.8.5 "ParameterDataIn_0" to ParameterDataIn_57:

- Values read/written

During write access, the sequence number in register 4.26.8.8.8.1 "ParameterCtrlIn" is only set to the written value when processing the order has been completed and the parameter data has been read from the object directory for the IO-Link device and entered in the registers 4.26.8.8.8.5 "ParameterDataIn_0" to ParameterDataIn_57.

A response provided by increasing the sequence number must be guaranteed (a timeout may be necessary for this purpose). That means, if the written sequence number from register 4.26.8.8.8.2 "ParameterCtrlOut" is accepted by register 4.26.8.8.8.1 "ParameterCtrlIn", then the application can safely assume that access has taken place.

Limit values for write/read access

- Index: 0 to 65535
- Subindex: 0 to 255
- Data length: 1 to 228 bytes for write access
- Data length: 1 to 229 bytes for read access

The resulting changes are written once to the IO-Link device without being temporarily saved on the module. That means, after disconnecting the IO-Link device, the values from the ODW registers are written back to the IO-Link device (see register 4.26.8.8.8.7 "ODW_Data_0" to ODW_Data_127).

4.26.8.8.8.1 Response to read/write access

Name:
ParameterCtrlIn

This register contains the response for dynamic read/write access of the object directory.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Sequence number	x	
4 - 7	Interface number	00	Interface 1
		01	Interface 2
		10	Interface 3
		11	Interface 4
8 - 11	Nutzdatenlänge	0000 to 1111	Number of bytes
12 - 13	Reserved	-	
14	Read / write	0	Read access
		1	Write access
15	Errors	0	No error
		1	Errors

Payload data length

The payload data length of the parameter access is copied by the module from the register 4.26.8.8.8.3 "ParameterCmdIn" (bit 24 to 27). Because this is a 4-bit value, the specification of the payload length is possible for a value with a maximum of 15 bytes. In the event that parameter sets larger than 15 bytes are accessed, the information about the number of bytes read during the parameter access must be taken from "ParameterCmdIn".

4.26.8.8.8.2 Configuration of dynamic read/write access

Name:
ParameterCtrlOut

This register is used to configure dynamic read/write access of the object directory.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Sequence number	x	
4 - 7	Interface number	00	Interface 1
		01	Interface 2
		10	Interface 3
		11	Interface 4
8 - 13	Reserved	-	
14	Read / write	0	Read access
		1	Write access
15	Error response (only defined for read access, this bit should be set to "0" for write access)	0	Inactive
		1	Active

4.26.8.8.8.3 Feedback from I/O object information

Name:
ParameterCmdIn

This register returns the number of bytes read during a read access.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 15	Object index being used	x	
16 - 23	Object subindex being used	x	
24 - 31	Number of bytes read	x	

4.26.8.8.8.4 Configuration of the I/O object information

Name:
ParameterCmdOut

This register is used to configure dynamic read/write access of the object directory.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 15	Object index	0 to 65535	
16 - 23	Object subindex	0 to 255	
24 - 31	Payload length in bytes	0 to 255	

4.26.8.8.8.5 Runtime parameter data read

Name:
ParameterDataIn_0 to ParameterDataIn_57

The corresponding parameter data is written to this register during read access of the object directory for the IO-Link device.

The length specified in register "ParameterCmdOut" determines how many 4-byte registers are read from the object directory for the IO-Link device and how many in the last byte are still valid.

Data type	Value
UDINT	0 to 4,294,967,295

4.26.8.8.8.6 Runtime parameter data written

Name:
ParameterDataOut_0 to ParameterDataOut_57

The parameter data from this register is written during write access of the object directory for the IO-Link device.

The length specified in register 4.26.8.8.8.4 "ParameterCmdOut" determines how many 4-byte registers are written to the object directory for the IO-Link device and how many in the last byte are still valid.

Data type	Value
UDINT	0 to 4,294,967,295

4.26.8.8.8.7 Boot parameter data

Name:
ODW_Data_0 to ODW_Data_127

This register contains parameter data for configuration of the IO-Link device.

Data type	Value
UDINT	0 to 4,294,967,295

4.26.8.8.8 Boot I/O object information

Name:
ODW_Target_0 to ODW_Target_127

A write procedure on this register will transfer the parameter information from the corresponding ODW_Data register to the IO-Link device.

Example:

If the ODW_Target_0 register is written to, the parameter data from ODW_Data_0 is applied by the module and transferred to the object dictionary of the IO-Link device.

Unlike short-term access, the values are also stored in RAM on the module in order to be able to reload these parameters in the object directory for the IO-Link device when restarting the IO-Link device.

Information:

"ODW_Data" must be defined before "ODW_Target".

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 15	Object index	x	
16 - 23	Subindex	x	
24 - 27	Interface number	00	Interface 1
		01	Interface 2
		10	Interface 3
		11	Interface 4
28 - 30	Length in bytes	x	

4.26.8.8.9 Errors and warnings

Name:
ErrorsWarnings01 to ErrorsWarnings04

The counter is increased by one if the IO-Link device reports an error or warning.

An error is a fatal event if it causes an IO-Link device to lose its intended functionality. An error causes the IO-Link device to leave the OPERATE state (see section 4.26.8.8.5.2 "Operating state" on page 2784) and re-initialize.

The cause of a warning could be one-time communication disturbances. Warnings are events that deviate from normal operating behavior but do not necessarily result in loss of functionality. Several consecutively occurring warnings can result in an error.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Warning counter	x	Counts the errors that do not immediately lead to ending the communication with the IO-Link device
4-7	Error counter	x	Counts the errors that causes the IO-Link device to change from status "10 = cyclic data exchange" and be reinitialized

4.26.8.8.10 Event handling

If an event occurs on an IO-Link device, then the device retrieves it and stores the data in the following registers:

Register	Description
4.26.8.8.10.3 "EventPortSeq"	IO-Link device interface that triggered the event.
	Sequence number, incremented with each event
4.26.8.8.10.2 "Event description"	Event description: Instance, type and mode
4.26.8.8.10.1 "Event code"	Event code

The sequence number for the event counter is incremented by 1 with each event in order to notify the application. After the application has read the event data, the module has to use the 4.26.8.8.10.4 "EventQuit" register to signal that the values were retrieved from registers "EventQualifier" and "EventCode" and then the module can read the next event from IO-Link device. The value in register "EventPortSeq" is considered a correct acknowledgment value.

Events are available for interfaces in the OPERATE state. An event inhibit can also be set in Automation Studio. This is specified as a number of X2X Link cycles for an event before it can be overwritten by the next event. Events that occur during the inhibit time are cached on the module.

4.26.8.8.10.1 Event code

Name:
EventCode

This register is used to indicate the manufacturer-specific code for the IO-Link device.
In addition to manufacturer-specific codes, there are also the event codes specified for IO-Link in case the IO-Link device does not provide an EventCode.

Data type	Value	Information
UINT	0 to 65535	Event code
	0x34 / 0xFFF0	Invalid event from the IO-Link device
	0x54 / 0xFF80	IO-Link device message
	0x74 / 0xFF80	IO-Link device error
	0x74 / 0x6320	Parameter error
	0x70 / 0xFF10	Communication error

4.26.8.8.10.2 Event description

Name:
EventQualifier

IO-Link devices can generate events (including manufacturer-specific events). Information about the instance, type and mode of the event can be read from this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Instance layer generated by the event	000	Unknown
		001	Hardware
		010	Data exchange layer for the IO-Link device
		011	Application layer for the IO-Link device
		100	Application
		101 to 111	Reserved
3	Reserved	-	
4 - 5	Type of event	00	Reserved
		01	Information
		10	Warning
		11	Errors
6 - 7	Mode of the event	00	Reserved
		01	One-time event
		10	Pending event is gone
		11	Pending event

4.26.8.8.10.3 Event interface

Name:
EventPortSeq

IO-Link devices can generate events (including manufacturer-specific events). Information about the interface that caused the event can be read from this register. By reading the sequence number, the application can determine if a new event has occurred. For this topic, see also 4.26.8.8.10 "Event handling".

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Interface	0	Interface 1
		1	Interface 2
		2	Interface 3
		3	Interface 4
		4 - 7	Reserved
4 - 7	Event counter	0 to 15	Sequence number is incremented with each new event that occurs

4.26.8.8.10.4 Acknowledge events

Name:
EventQuit

Register for acknowledging events so that the module can retrieve the next event. The event that has been read must be acknowledged with the value from register 4.26.8.8.10.3 "EventPortSeq".

Data type	Value
USINT	0 to 255

4.26.8.8.11 IO-Link cycle time

The I/O module automatically selects the best possible IO-Link cycle time per interface for the connected IO-Link device. This is always a multiple of the X2X cycle time. The cycle times of the 4 IO-Link interfaces are independent of one another. The module can read back which cycle time was selected for an IO-Link interface.

The minimum cycle time is 2.3 ms.

4.26.9 X20DS438A

4.26.9.1 General information

The module is an IO-Link master that can be used to connect intelligent sensors and actuators to the X20 system in accordance with the IO-Link standard. The module can operate up to 4 IO-Link devices. All IO-Link channels can be used as standard digital inputs or outputs.

- 4 IO-Link devices
- 4 digital channels, can be configured as input or output
- 24 VDC and GND for sensor/actuator supply

4.26.9.2 Order data

Model number	Short description	Figure
	Other functions	
X20DS438A	X20 digital signal module, 4x I/O-Link master V1.1, can also be configured as 4x digital input or output channels, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 647: X20DS438A - Order data

4.26.9.3 Technical data

Product ID	X20DS438A
Short description	
I/O module	IO-Link master with 4 IO-Link interfaces
General information	
B&R ID code	0xCAC0
Status indicators	IO-Link, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
IO-Link operating state	Yes, using status LED and software
C/Q status	Yes, using status LED and software
Cable specification	
Cable type	3-pin standard sensor cable, unshielded
Cable length	Max. 20 m
Line capacitance	Max. 3 nF
Loop resistance	Max. 6 Ω
Power consumption	
Bus	0.01 W
Internal I/O	0.71 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Bus - IO-Link	Yes
IO-Link - IO-Link	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
GOST-R	Yes
Sensor/Actuator supply	
Voltage	I/O supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 0.5 A	Max. 0.3 V
Power consumption	Max. 12 W per IO-Link interface
Short circuit protection	Yes
Overload protection	
Turn-off delay	Configurable using software
Turn-off duration	Configurable using software
IO-Link in master mode	
Transfer rates	
COM1	4.8 kbaud
COM2	38.4 kbaud
COM3	230.4 kbaud
Limits for COM3	
Max. connection capacity	22 nF (cable + IO-Link device)
Max. load	96 Ω / 250 mA
Data format	1 start bit, 8 data bits, 1 parity bit (even), 1 stop bit
Bus level	24 VDC (active), 0 VDC (resting voltage)
IO-Link in master mode or in SIO mode "digital output"	
Design	Bipolar, positive and negative switching
Peak short circuit current	<1.3 A
Residual voltage	<0.7 VDC at nominal current 0.25 A
Switching voltage	I/O supply minus voltage drop for short circuit protection and semiconductor switch
Voltage drop on semiconductor switch	Max. 0.5 VDC at 0.25 A
Switching frequency	Typ. 25 kHz 300 kHz in IO-Link master mode
Switching delay	
0 -> 1	<10 µs
1 -> 0	<10 µs
Switching on after overload or short circuit cutoff	Configurable with software
Isolation voltage between IO-Link and bus	500 V_{eff}
IO-Link in SIO mode "digital output"	
Nominal voltage	24 VDC
Nominal output current	0.25 A
Total nominal current	Max. 1 A
Output circuit	Sink or source
Switching frequency (resistive load)	Max. 500 Hz
Output protection [2)]	Thermal cutoff if overcurrent or short circuit occurs, integrated protection for switching inductances
IO-Link in SIO mode "digital input"	
Nominal voltage	24 VDC
Input filter	
Hardware	300 ns
Software	-
Input circuit	Sink

Table 648: X20DS438A - Technical data

Product ID	X20DS438A
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 4 mA
Input resistance	Typ. 6 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between IO-Link and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately, Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 648: X20DS438A - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Interrupting current during overload: Between 0.3 A and 0.8 A.

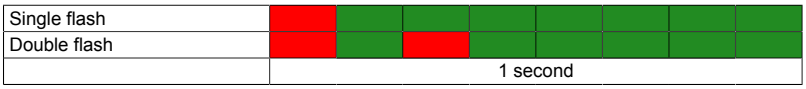
4.26.9.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

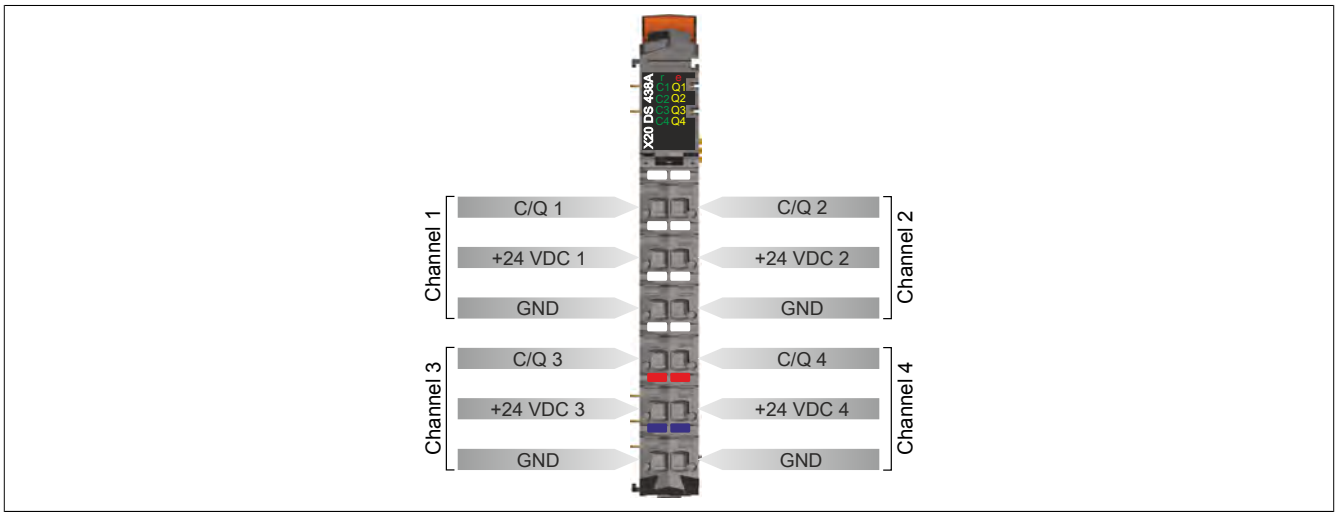
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			Double flash	BOOT mode (during firmware update)[1]
			On	OPERATE mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	One of the following errors has curred:
	C1 - C4	Red	On	Overload on the supply or on the channel's C/Q line
		Green/Red	Off	Interface in SIO mode
			Single flash	Channel in OPERATE mode, no IO-Link communication
			Double flash	Channel in OPERATE mode, error on inspection level
		Green	On	Channel in OPERATE mode, IO-Link communication active
	Q1 - Q4	Orange		Input/output state of corresponding IO-Link interface

1) Depending on the configuration, a firmware update can take up to several minutes.

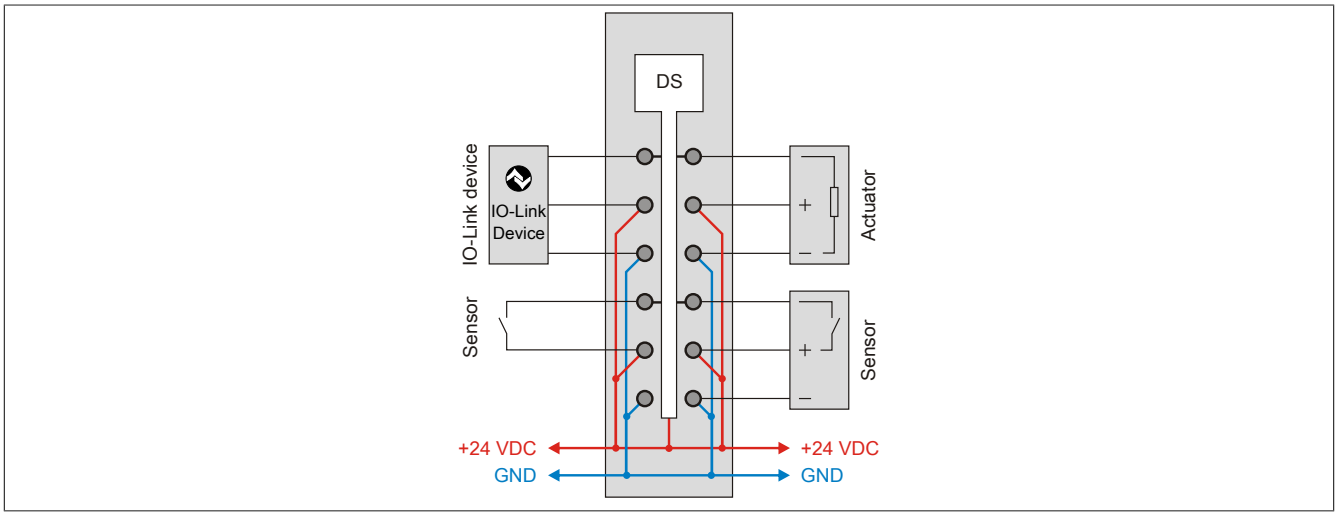
Blink times of LEDs C1 through C4 for single and double flash.



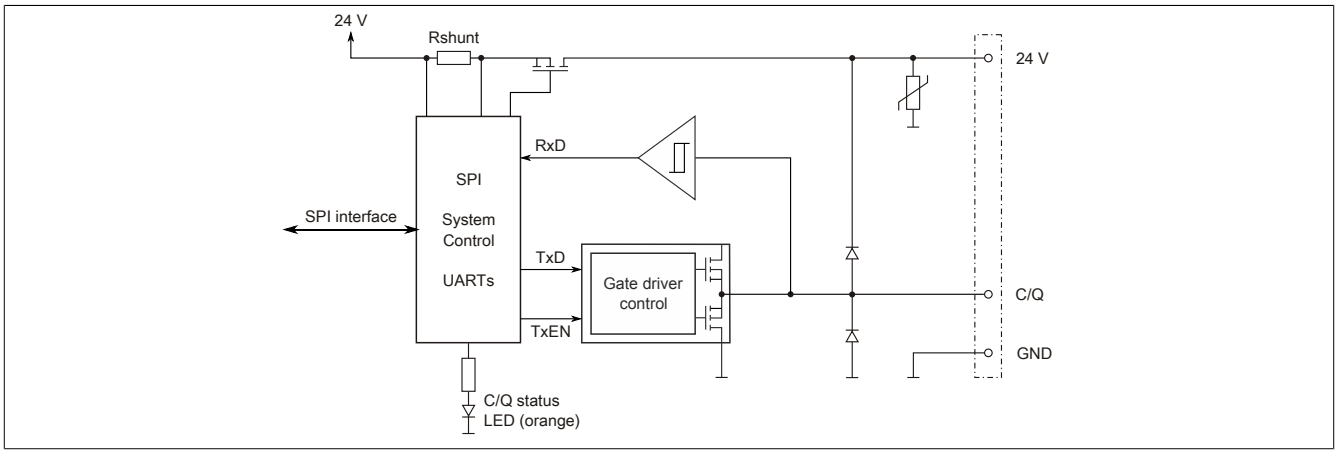
4.26.9.5 Pinout



4.26.9.6 Connection example



4.26.9.7 Input/output circuit diagram



4.26.9.8 SG3 support

This module does not support SG3 target systems.

4.26.9.9 Register description

4.26.9.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.9.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
General module properties						
513	CfO_SupplyConfig	USINT				•
Index*1024 + 3073	CfO_OperatingMode0N (Index N = 1 to 4)	USINT				•
IO-Link - configuration						
Index*1024 + 3076	CfO_ChannelMode0N (Index N = 1 to 4)	UDINT				•
Index*1024 + 3102	CfO_IdentificationVendorId0N (Index N = 1 to 4)	UINT				•
Index*1024 + 3108	CfO_IdentificationDeviceId0N (Index N = 1 to 4)	UDINT				•
Index*1024 + 3116	CfO_PDI_TypeInfo0N (Index N = 1 to 4)	UDINT				•
Index*1024 + 3124	CfO_PDO_TypeInfo0N (Index N = 1 to 4)	UDINT				•
15372	CfO_TimerCycle	UDINT				•
15366	CfO_TimerOffset	INT				•
Index*1024 + 3086	CfO_ReqCycleMultiple0N (Index N = 1 to 4)	UINT				•
Index*1024 + 3090	CfO_ReqCycleDivisor0N (Index N = 1 to 4)	UINT				•
Index*1024 + 3094	CfO_ReqCycleOffset0N (Index N = 1 to 4)	UINT				•
Index*1024 + 3082	CfO_ReqCycleTime0N (Index N = 1 to 4)	UINT				•
IO-Link - general						
7	SIO or digital outputs	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput04	Bit 3				
	DisablePowerSupply01	Bit 4				
	...	...				
	DisablePowerSupply04	Bit 7				
1	SIO or digital inputs	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput04	Bit 3				
3	Sync (status byte)	USINT	•			
	Synchronized01	Bit 0				
	...	...				
	Synchronized04	Bit 3				
	CycleEnd01	Bit 4				
	...	...				
	CycleEnd04	Bit 7				
5	Overload (status byte)	USINT	•			
	Overload01	Bit 0				
	...	...				
	Overload04	Bit 3				
Index*16 + 17	ChannelStatus0N (Index N = 1 to 4)	USINT	•			
Index*16 + 22	FrameCount0N (Index N = 1 to 4)	SINT	•			
Index*1024 + 3586	CycleStartNettime0N (Index N = 1 to 4)	INT	•			
Index*1024 + 3588	CycleStartNettime0N (Index N = 1 to 4)	DINT				
Index*1024 + 3594	CycleEndNettime0N (Index N = 1 to 4)	INT	•			
Index*1024 + 3596	CycleEndNettime0N (Index N = 1 to 4)	DINT				
IO-Link - parameter server for IO-Link device						
Index*16 + 19	DsControl0N (Index N = 1 to 4)	USINT			•	•
Index*1024 + 3140	Cfo_DS_Config0N (Index N = 1 to 4)	UDINT				•
Index*1024 + 3241	DsProgress0N (Index N = 1 to 4)	USINT		•		
Index*1024 + 3148	CfO_DS_SaveCtrl0N (Index N = 1 to 4)	UDINT				•
Index*1024 + 3156	CfO_DS_SaveData0N (Index N = 1 to 4)	UDINT				•
IO-Link - timestamp						
Index*1024 + 3610	IoLinkTimestampIn0N (Index N = 1 to 4)	INT	•			
Index*1024 + 3612	IoLinkTimestampIn0N (Index N = 1 to 4)	DINT				
Index*1024 + 3617	IoLinkTimestampInStatusSeq0N (Index N = 1 to 4)	USINT	•			
Index*1024 + 3614	IoLinkTimestampOut0N (Index N = 1 to 4)	INT			•	
Index*1024 + 3616	IoLinkTimestampOut0N (Index N = 1 to 4)	DINT				
Index*1024 + 3621	IoLinkTimestampOutCtrlSeq0N (Index N = 1 to 4)	USINT			•	
Index*1024 + 3619	IoLinkTimestampOutStatus0N (Index N = 1 to 4)	USINT	•			
Index*8 + 4473	OutputData01_N (Index N = 1 to 8)	(U)SINT			•	
Index*8 + 4474	OutputData01_N (Index N = 1 to 8)	(U)INT				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Index*8 + 4476	OutputData01_N (Index N = 1 to 8)	(U)DINT REAL				
Index*8 + 5497	OutputData02_N (Index N = 1 to 8)	(U)SINT			●	
Index*8 + 5498	OutputData02_N (Index N = 1 to 8)	(U)INT				
Index*8 + 5500	OutputData02_N (Index N = 1 to 8)	(U)DINT REAL				
Index*8 + 6521	OutputData03_N (Index N = 1 to 8)	(U)SINT			●	
Index*8 + 6522	OutputData03_N (Index N = 1 to 8)	(U)INT				
Index*8 + 6524	OutputData03_N (Index N = 1 to 8)	(U)DINT REAL				
Index*8 + 7545	OutputData04_N (Index N = 1 to 8)	(U)SINT			●	
Index*8 + 7546	OutputData04_N (Index N = 1 to 8)	(U)INT				
Index*8 + 7548	OutputData04_N (Index N = 1 to 8)	(U)DINT REAL				
Index*8 + 4345	InputData01_N (Index N = 1 to 8)	(U)SINT	●			
Index*8 + 4346	InputData01_N (Index N = 1 to 8)	(U)INT				
Index*8 + 4348	InputData01_N (Index N = 1 to 8)	(U)DINT REAL				
Index*8 + 5369	InputData01_N (Index N = 1 to 8)	(U)SINT	●			
Index*8 + 5370	InputData01_N (Index N = 1 to 8)	(U)INT				
Index*8 + 5372	InputData01_N (Index N = 1 to 8)	(U)DINT REAL				
Index*8 + 6393	InputData01_N (Index N = 1 to 8)	(U)SINT	●			
Index*8 + 6394	InputData01_N (Index N = 1 to 8)	(U)INT				
Index*8 + 6396	InputData01_N (Index N = 1 to 8)	(U)DINT REAL				
Index*8 + 7417	InputData01_N (Index N = 1 to 8)	(U)SINT	●			
Index*8 + 7418	InputData01_N (Index N = 1 to 8)	(U)INT				
Index*8 + 7420	InputData01_N (Index N = 1 to 8)	(U)DINT REAL				
IO-Link - information						
Index*1024 + 3206	VendorId0N (Index N = 1 to 4)	UINT	●	●		
Index*1024 + 3212	DeviceId0N (Index N = 1 to 4)	UDINT	●	●		
Index*1024 + 3206	FunctionId0N (Index N = 1 to 4)	UINT	●	●		
Index*1024 + 3218	CycleTime0N (Index N = 1 to 4)	UINT	●	●		
Index*1024 + 3222	CycleMultible0N (Index N = 1 to 4)	UINT		●		
Index*1024 + 3226	CycleDivisor0N (Index N = 1 to 4)	UINT		●		
Index*1024 + 3230	MinCycleTime0N (Index N = 1 to 4)	UINT		●		
Index*1024 + 3233	PDI_Size0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3235	PDO_Size0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3237	Baudrate0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3239	IoLinkVersionID0N (Index N = 1 to 4)	USINT		●		
Event interface						
113	EventPortSeq	USINT	●	●		
115	EventQualifier	USINT	●	●		
118	EventCode	UINT	●	●		
121	EventsLeft	USINT		●		
123	EventQuit	USINT			●	●
123	EventQuitReadBack	USINT		●		
Command interface						
98	ParameterIndexOut	UINT			●	●
101	ParameterSubIndexOut	USINT			●	●
103	ParameterCtrlOut	USINT			●	●
108	ParameterDataOut_0	UDINT			●	●
103	ParameterCtrlIn	USINT	●	●		
108	ParameterDataIn_0	UDINT	●	●		
FlatStream						
193	CfO_OutputMTU	USINT				●
195	CfO_InputMTU	USINT				●
197	CfO_FlatStreamMode	USINT				●
199	CfO_Forward	USINT				●
204	CfO_ForwardDelay	UDINT				●
129	InputSequence	USINT	●			
Index*2 + 129	RxByteN (Index N = 1 to 27)	USINT	●			
129	OutputSequence	USINT			●	
Index*2 + 129	TxByteN (Index N = 1 to 27)	USINT			●	

4.26.9.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
General module properties							
513	-	CfO_SupplyConfig	USINT				●
Index*1024 + 3073	-	CfO_OperatingMode0N (Index N = 1 to 4)	USINT				●
IO-Link - configuration							
Index*1024 + 3076	-	CfO_ChannelMode0N (Index N = 1 to 4)	UDINT				●
Index*1024 + 3102	-	CfO_IdentificationVendorId0N (Index N = 1 to 4)	UINT				●
Index*1024 + 3108	-	CfO_IdentificationDeviceId0N (Index N = 1 to 4)	UDINT				●
Index*1024 + 3116	-	CfO_PDI_TypeInfo0N (Index N = 1 to 4)	UDINT				●
Index*1024 + 3124	-	CfO_PDO_TypeInfo0N (Index N = 1 to 4)	UDINT				●
15372	-	CfO_TimerCycle	UDINT				●
15366	-	CfO_TimerOffset	INT				●
Index*1024 + 3086	-	CfO_ReqCycleMultiple0N (Index N = 1 to 4)	UINT				●
Index*1024 + 3090	-	CfO_ReqCycleDivisor0N (Index N = 1 to 4)	UINT				●
Index*1024 + 3094	-	CfO_ReqCycleOffset0N (Index N = 1 to 4)	UINT				●
Index*1024 + 3082	-	CfO_ReqCycleTime0N (Index N = 1 to 4)	UINT				●
IO-Link - general							
7	-	SIO or digital outputs	USINT				●
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput04	Bit 3				
		DisablePowerSupply01	Bit 4				
		...	...				
		DisablePowerSupply04	Bit 7				
1	20	SIO or digital inputs	USINT	●			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
3	21	Sync (status byte)	USINT	●			
		Synchronized01	Bit 0				
		...	...				
		Synchronized04	Bit 3				
		CycleEnd01	Bit 4				
		...	...				
		CycleEnd04	Bit 7				
5	22	Overload (status byte)	USINT	●			
		Overload01	Bit 0				
		...	...				
		Overload04	Bit 3				
Index*16 + 17	Index+15	ChannelStatus0N (Index N = 1 to 4)	USINT	●			
Index*16 + 22	-	FrameCount0N (Index N = 1 to 4)	SINT		●		
Index*1024 + 3586	-	CycleStartNettime0N (Index N = 1 to 4)	INT		●		
Index*1024 + 3588	-	CycleStartNettime0N (Index N = 1 to 4)	DINT				
Index*1024 + 3594	-	CycleEndNettime0N (Index N = 1 to 4)	INT		●		
Index*1024 + 3596	-	CycleEndNettime0N (Index N = 1 to 4)	DINT				
IO-Link - parameter server for IO-Link device							
Index*16 + 19	-	DsContol0N (Index N = 1 to 4)	USINT				●
Index*1024 + 3140	-	CfO_DS_Config0N (Index N = 1 to 4)	UDINT				●
Index*1024 + 3241	-	DsProgress0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3148	-	CfO_DS_SaveCtrl0N (Index N = 1 to 4)	UDINT				●
Index*1024 + 3156	-	CfO_DS_SaveData0N (Index N = 1 to 4)	UDINT				●
IO-Link - timestamp							
Index*1024 + 3610	-	IoLinkTimestampIn0N (Index N = 1 to 4)	INT		●		
Index*1024 + 3612	-	IoLinkTimestampIn0N (Index N = 1 to 4)	DINT				
Index*1024 + 3617	-	IoLinkTimestampInStatusSeq0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3614	-	IoLinkTimestampOut0N (Index N = 1 to 4)	INT				●
Index*1024 + 3616	-	IoLinkTimestampOut0N (Index N = 1 to 4)	DINT				
Index*1024 + 3621	-	IoLinkTimestampOutCtrlSeq0N (Index N = 1 to 4)	USINT				●
Index*1024 + 3619	-	IoLinkTimestampOutStatus0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3353	-	InputData0N_4 (Index N = 1 to 8)	USINT	●			
IO-Link - information							
Index*1024 + 3202	-	VendorId0N (Index N = 1 to 4)	UINT		●		
Index*1024 + 3212	-	DeviceId0N (Index N = 1 to 4)	UDINT		●		
Index*1024 + 3206	-	FunctionId0N (Index N = 1 to 4)	UINT		●		
Index*1024 + 3218	-	CycleTime0N (Index N = 1 to 4)	UINT		●		
Index*1024 + 3222	-	CycleMultible0N (Index N = 1 to 4)	UINT		●		
Index*1024 + 3226	-	CycleDivisor0N (Index N = 1 to 4)	UINT		●		
Index*1024 + 3230	-	MinCycleTime0N (Index N = 1 to 4)	UINT		●		

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Index*1024 + 3233	-	PDI_Size0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3235	-	PDO_Size0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3237	-	Baudrate0N (Index N = 1 to 4)	USINT		●		
Index*1024 + 3239	-	IoLinkVersionID0N (Index N = 1 to 4)	USINT		●		
Event interface							
113	-	EventPortSeq	USINT		●		
115	-	EventQualifier	USINT		●		
118	-	EventCode	UINT		●		
121	-	EventsLeft	USINT		●		
123	-	EventQuit	USINT				●
123	-	EventQuitReadBack	USINT		●		
Command interface							
98	-	ParameterIndexOut	UINT				●
101	-	ParameterSubIndexOut	USINT				●
103	-	ParameterCtrlOut	USINT				●
108	-	ParameterDataOut_0	UDINT				●
103	-	ParameterCtrlIn	USINT		●		
108	-	ParameterDataIn_0	UDINT		●		
FlatStream							
193	-	CfO_OutputMTU	USINT				●
195	-	CfO_InputMTU	USINT				●
197	-	CfO_FlatStreamMode	USINT				●
199	-	CfO_Forward	USINT				●
204	-	CfO_ForwardDelay	UDINT				●
129	-	InputSequence	USINT		●		
Index*2 + 129	-	RxByteN (Index N = 1 to 27)	USINT		●		
129	-	OutputSequence	USINT			●	
Index*2 + 129	-	TxByteN (Index N = 1 to 27)	USINT			●	

1) The offset specifies the position of the register within the CAN object.

4.26.9.9.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.26.9.9.4 General module properties

The module has the option of supplying power to IO-Link devices.
To prevent damage to hardware, each channel is monitored individually and equipped with its own overload protection. In this way, an overload in the power supply on one channel does not affect the other channels.

4.26.9.9.4.1 Configuring overload protection for the IO-Link supply

Name:
CfO_SupplyConfig

This register can be used to define how the module supply behaves for all channels when an overload occurs. The following rules apply:

- The overload duration (bits 6-7) corresponds to the time that the supply remains switched on after an overload is detected. The supply is only cut off if the overcurrent occurs for the entire time configured.
- The switch-off duration (bits 4-5) corresponds to the time that the supply remains switched off after a overload-related cutoff until it is switched back on.
  For this reason, an overload that occurs over a longer period can cause the module supply to cyclically switch on/off.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4 - 5	Switch-off duration after overload	00	5 ms
		01	20 ms
		10	50 ms
		11	Forbidden
6 - 7	Overload duration until error detection	00	1 ms
		01	4 ms
		10	10 ms
		11	Forbidden

4.26.9.9.4.2 OperatingMode

Name:
CfO_OperatingMode01 to CfO_OperatingMode04

This register is the same as the first bytes of the ChannelMode register in the IO-Link configuration.
It can be used to switch a channel's mode at runtime. The rest of the settings for the ChannelMode register are unchanged and continue to be used in the selected mode.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel mode	00	Mode: Inactive
		01	Mode: SIO output The channel's C/Q connector is configured as a digital output.
		10	Mode: SIO input The channel's C/Q connector is configured as a digital input.
		11	Mode: Operate The channel's C/Q connector is configured for IO-Link data transfer.
2 - 7	Reserved	-	

4.26.9.9.5 IO-Link - configuration

In order to establish communication between the module and IO-Link device, the ChannelMode register must be configured at least. Additional registers allow the data stream to be adjusted and the connected devices to be checked. This way, the IO-Link communication can be better adjusted to the user's requirements.

4.26.9.9.5.1 ChannelMode

Name:
CfO_ChannelMode01 to CfO_ChannelMode04

The user has the option of setting all channel-specific settings via this register.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel mode	00	Mode: Inactive
		01	Mode: SIO output The channel's C/Q connector is configured as a digital output.
		10	Mode: SIO input The channel's C/Q connector is configured as a digital input.
		11	Mode: Operate The channel's C/Q connector is configured for IO-Link data transfer.
2 - 7	Reserved	-	
8 - 9	Threshold value for overcurrent on the channel[1)] (OverCurrentThreshold in Automation Studio configuration)	00	250 mA
		01	125 mA
		10	75 mA
		11	50 mA
10 - 11	Reserved	-	
12 - 13	Switch-off duration after overload[1)] (OverloadOffTime in Automation Studio configuration)	00	20 ms
		01	12 ms
		10	6.4 ms
		11	32 ms
14 - 15	Reserved	-	
16 - 17	Synchronization mode	00	Free-wheeling (asynchronous)
		01	Synchronous (manual)
		10	Synchronous (automatic)
		11	Forbidden
18 - 19	Reserved	-	
20 - 23	Inspection level	0	Tests disabled
		1	Testing VendorID and DeviceID
24 - 25	IO-Link timestamp	00	No timestamp
		01	Input timestamp
		10	Output timestamp
		11	Input and output timestamps
26	Format of the IO-Link output timestamp[2)]	0	32-bit (DINT)
		1	16-bit (INT)
27 - 32	Reserved	-	

1) This is overload protection for the C/Q connector of the IO-Link channel (IO-Link data line or SIO output) as opposed to overload protection of the IO-Link supply.
2) This bit informs the module of the format used for the IoLinkTimestampOut output timestamp. In Automation Studio, this setting is made implicitly in the I/O configuration together with the selection of the data type for the IO-Link timestamp.

4.26.9.9.5.2 IdentificationVendorID

Name:
CfO_IdentificationVendorId01 to CfO_IdentificationVendorId04

If the Vendor ID is to be verified during startup, then the expected value must be specified in this register. The verification can be enabled by setting the inspection level in the ChannelMode register.

Information:

If the expected ID does not match the actual ID of the connected IO-Link device, communication will not be started for this channel.

Data type	Value
UINT	0 to 65535

4.26.9.9.5.3 IdentificationDeviceID

Name:
CfO_IdentificationDeviceId01 to CfO_IdentificationDeviceId04

If the device ID should be verified during startup, then the expected ID of the IO-Link device must be specified in this register. The verification can be enabled by setting the inspection level in the ChannelMode register.

Information:

If the expected ID does not match the actual ID of the connected IO-Link device, communication will not be started for this channel.

Data type	Value
UDINT	0 to 4,294,967,295

4.26.9.9.5.4 PDI_TypeInfo

Name: CfO_PDI_TypeInfo01 to CfO_PDI_TypeInfo04

To transfer process data from the IO-Link device to the CPU (application), the information is first read from the module and saved temporarily. Typically, four bytes are reserved for each piece for registered information (see 4.26.9.9.9 "IO-Link process data").

This register can be used to configure how the incoming IO-Link process data stream (IO-Link frame) is divided up. According to this configuration, the IO-Link process data is made available to the application via the corresponding InputData registers. The input data registers are assigned to individual data points with the corresponding data type in the I/O mapping.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 to 3	IO-Link information 1	0000	Array[4] of Bytes
		0001	USINT
		0010	SINT
		0011	UINT
		0100	INT
		0101	UDINT
		0110	DINT
		0111	REAL
		1000 - 1111	Reserved
4 - 7	IO-Link information 2		Possible values are identical with IO-Link information 1
8 - 11	IO-Link information 3		
12 - 15	IO-Link information 4		
16 - 19	IO-Link information 5		
20 - 23	IO-Link information 6		
24 - 27	IO-Link information 7		
28 - 31	IO-Link information 8		

Information:

With setting 0 (Array[4] of Bytes), the bytes are copied from the IO-Link data stream unchanged. In all other modes, the byte order is changed (from big endian to little endian).

4.26.9.9.5.5 PDO_TypeInfo

Name: CfO_PDO_TypeInfo01 to CfO_PDO_TypeInfo04

To transfer process data to an IO-Link device, this register can be used to configure which data types of the individual OutputData registers are used to put together the outgoing IO-Link process data stream (IO-Link frame, see 4.26.9.9.9 "IO-Link process data"). According to this configuration, OutputData registers are assigned to data points with the corresponding data types in Automation Studio (I/O mapping).

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 to 3	IO-Link information 1	0000	Array[4] of Bytes
		0001	USINT
		0010	SINT
		0011	UINT
		0100	INT
		0101	UDINT
		0110	DINT
		0111	REAL
		1000 - 1111	Reserved
4 - 7	IO-Link information 2		Possible values are identical with IO-Link information 1
8 - 11	IO-Link information 3		
12 - 15	IO-Link information 4		
16 - 19	IO-Link information 5		
20 - 23	IO-Link information 6		
24 - 27	IO-Link information 7		
28 - 31	IO-Link information 8		

Information:

With setting 0 (Array[4] of Bytes), the bytes are copied from the IO-Link data stream unchanged. In all other modes, the byte order is changed (from big endian to little endian).

4.26.9.9.5.6 Timing of IO-Link communication

At runtime, the module needs to manage data sets from 2 different communication standards. For efficient X2X Link communication, it is important to make sure that the cycle time of all X2X modules is the same as the bus cycle time.

Cycle times specified in IO-Link

The IO-Link specification defines the timing cycle for polling an IO-Link device. This cycle is called the IO-Link cycle. Valid IO-Link cycle times range from 0.4 ms to 132.8 ms. There are three ranges:

Area	Increment	Calculation	Valid cycle times
0.4 to 6.3 ms	0.1 ms	Cycle time = 0.1 ms * n + 0.4 ms	0.4, 0.5, 0.6 to 6.2, 6.3 ms
6.4 to 32.6 ms	0.4 ms	Cycle time = 0.4 ms * n + 6.4 ms	6.4, 6.8, 7.2 to 32.2, 32.6 ms
32.0 to 132.8 ms	1.6 ms	Cycle time = 1.6 ms * n + 32.0 ms	32.0, 33.6, 35.2 to 131.2, 132.8 ms

Module timer

An internal module timer that applies globally to all channels serves as the bases for synchronizing the individual channels. Using this defined time basis, X2X and IO-Link communication can be synchronized with each other. The period duration for the module timer can be defined in µs. To make communication as efficient and deterministic as possible, the module timer is configured in automatic mode to match the X2X Link cycle time by default. If necessary, the start of the module timer can be offset using the TimerOffset.

The module timer's cycle is synchronized automatically with the X2X cycle. Depending of the ratio between the X2X and module timer cycle time, there may be different ratios between the cycles.

Examples

1 to 1	(X2X cycle 1000, cycle timer 1000)	→ Always exactly one timer cycle per X2X cycle
2 to 1	(X2X cycle 2000, cycle timer 1000)	→ Always exactly two timer cycles per X2X cycle
1 to 2	(X2X cycle 1000, cycle timer 2000)	→ Always exactly one timer cycle per 2 X2X cycles
3 to 5	(X2X cycle 1500, cycle timer 2500)	→ Always exactly 3 timer cycles per 5 X2X cycles

Synchronous operation

Unlike to free-running operation, synchronous mode and the synchronization cycle time in this operating mode can be configured individually for each channel.

The SYNCHRONIZED operating mode optimizes the interaction between X2X and IO-Link communication. The module's resources were designed for this mode, so this configuration should be used for the module's channels.

- In the mode SYNCHRONIZED (automatic), the module calculates the necessary timing parameters itself. An IO-Link cycle is set that complies with the IO-Link specification. The selected IO-Link cycle time corresponds to the lowest possible multiple of the module timer cycle time that meets the following conditions:
  - Valid IO-Link cycle time
  - Greater than or equal to the minimum cycle time on the device
- In the mode SYNCHRONIZED (manual), the user can configure the module's timing manually. Both the synchronization cycle time and the IO-Link cycle can be defined manually by setting a factor.

Synchronization cycle time

Synchronization cycle time = Timer cycle time * CfO_ReqCycleMultiple0x

The synchronization ensures that synchronization cycles run parallel with the same synchronization cycle time and are not offset by timer cycles.

IO-Link cycle time

IO-Link cycle time = Synchronization cycle time / CfO_ReqCycleDivisor0x

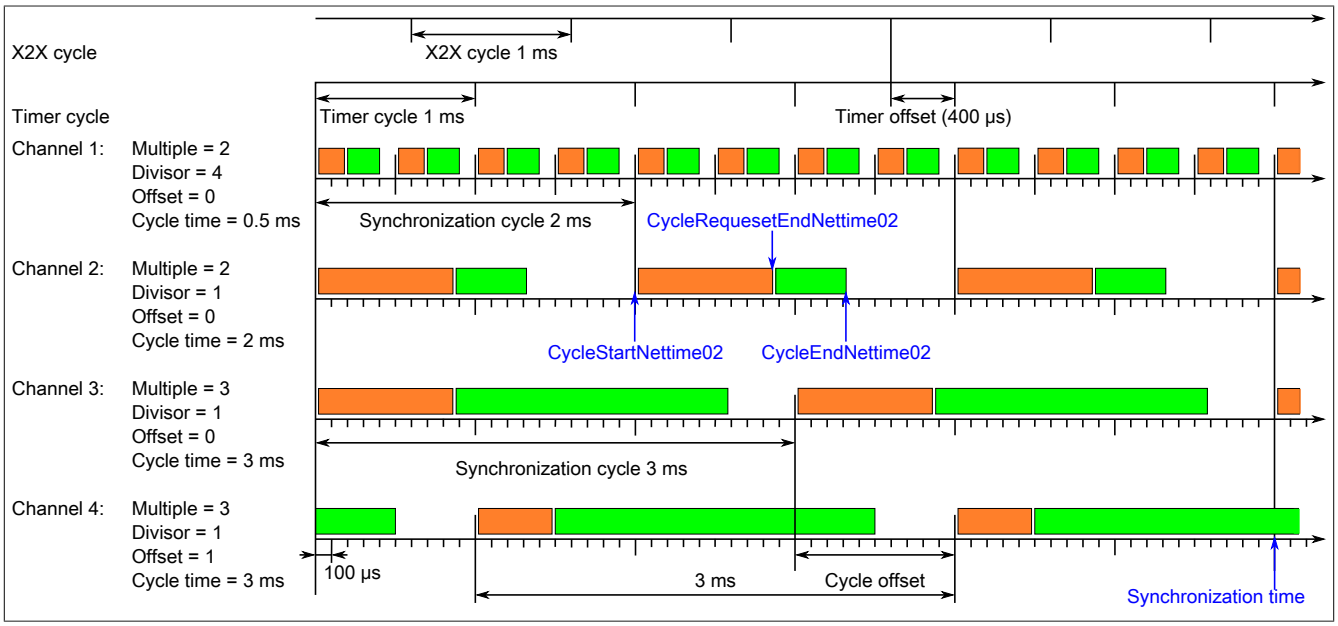
The IO-Link cycle is set individually for each channel. If necessary, the IO-Link cycle of a channel can be offset using a channel-specific offset. This allows channels to be adjusted so that their queries end at the same time, for example.
With very short cycle times (<1 ms) it is possible that the data cannot be processed fast enough. When this happens, the subsequent cycles are delayed, which is indicated by the status bit for synchronization being reset.

Information:

If the IO-Link cycle is configured to be less than the device's minimum cycle time, then a cycle that meets the following conditions is selected automatically:

- **Multiple of the module timer cycle**
- **Valid IO-Link cycle time**
- **Greater than or equal to the minimum cycle time on the device**

Example of a configuration



The module timer in this example

- The duration of the module timer period was not defined explicitly. In this case, it corresponds to the X2X Link cycle time.
- An offset of 400 µs was applied to the module timer; i.e. the module timer cycle begins 400 µs after the X2X Link cycle.

IO-Link communication in this example

- The parameters Multiple and Divisor produce a channel-specific cycle time for IO-Link communication.
- Channels 1 and 2 have a shared synchronization cycle of 2 ms.
  Channels 3 and 4 have a shared synchronization cycle of 3 ms, which is shifted due to the offset.
- Channels start their query together at the beginning of a shared synchronization cycle.
- The IO-Link cycle of the fourth channel was delayed with an offset of 1 ms.
- All channels have a shared synchronization cycle of 6 ms.

Free-running (asynchronous) mode

If the IO-Link and X2X cycle times cannot be synchronized, then the IO-Link cycle time can be defined explicitly. IO-Link communication then runs independently of the module timer and X2X cycle. Except for CycleEndNettime, no other net time data points can be used. The cycle times of free-running IO-Link channels are defined directly via the corresponding registers. However, deviations may occur if the module's resources are exhausted.

TimerCycle

Name:
CfO_TimerCycle

This register can be used to configure synchronous IO-Link communication. If the module timer is not meant to be operated with the same cycle, then it is possible to define the period length of the module timer in µs using this register. This allows channels to be synchronized with one another even if using a very unusual X2X cycle time.

Data type	Value
UDINT	0 to 4,294,967,295

TimerOffset

Name:
CfO_TimerOffset

This register can be used to configure synchronous IO-Link communication. If the module timer should run with a timing offset to X2X Link, this register can be used to define how many microseconds in front of or behind the module timer should be shifted.

Data type	Value
INT	-32768 to 32767

ReqCycleMultiple

Name:
CfO_ReqCycleMultiple01 to CfO_ReqCycleMultiple04

This register can be used to manually configure the synchronization cycle time. This cycle time can be used together with the ReqCycleDivisor register to define the IO-Link cycle time. See Synchronous operation for an example.

Information:

If this register is not defined for an IO-Link channel or predefined with zero, the values of the CycleMultiple and CycleDivisor registers are calculated automatically when the module is started.

Data type	Value
UINT	0 to 65535

ReqCycleDivisor

Name:
CfO_ReqCycleDivisor01 to CfO_ReqCycleDivisor04

This register can be used together with ReqCycleMultiple to define the IO-Link cycle time. See Synchronous operation for an example.

Information:

If this register is not defined for an IO-Link channel or predefined with zero, the values of the CycleMultiple and CycleDivisor registers are calculated automatically when the module is started.

Data type	Value
UINT	0 to 65535

ReqCycleOffset

Name:
CfO_ReqCycleOffset01 to CfO_ReqCycleOffset04

This register can be used to offset the IO-Link cycle of a channel with the synchronization cycle.
This offset may be sensible if all channels are running with the same cycle time. In this case, all channels are finished at the same time, which could result in the module not being able to process all data in time. Offsets can be used to prevent these sorts of bottlenecks so that data traffic can be divided up more evenly.

Data type	Value	Information
UINT	0 to 65535	Configured in timer cycles

ReqCycleTime

Name:
CfO_ReqCycleTime01 to CfO_ReqCycleTime04

This register is used with free-running (asynchronous) IO-Link communication. It contains the explicitly defined cycle time for the IO-Link query in µs.

Information:

- **In free-running mode, no net time data points are permitted to be used except for CycleEnd-Nettime.**
- **If the cycle time predefined for IO-Link communication falls below the device's minimum cycle time, the IO-Link data is queried using the device's minimum cycle time.**
- **For efficient IO-Link communication, the configured query time should correspond to the specified IO-Link cycle times. If a value is unsuitable, the next suitable cycle time is used automatically.**

Data type	Value	Information
UINT	0 to 65535	In 100 µs steps

4.26.9.9.6 IO-Link - General

The following registers are used for general communication. They are mainly used for repair status and runtime control.

4.26.9.9.6.1 Digital SIO outputs

Name:
DigitalOutput01 to DigitalOutput04
DisablePowerSupply01 to DisablePowerSupply04

If a channel is being operated in SIO mode (SIO output), this register can be used to control the SIO output of the IO-Link channel. It is also possible switch on/off the supply for each IO-Link channel individually.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput01	0	Reset digital SIO output 01
		1	Set digital SIO output 01
...		...	
3	DigitalOutput04	0	Reset digital SIO output 04
		1	Set digital SIO output 04
4	DisablePowerSupply01	0	Switch on supply for IO-Link channel 01
		1	Switch off supply for IO-Link channel 01
...		...	
7	DisablePowerSupply04	0	Switch on supply for IO-Link channel 04
		1	Switch off supply for IO-Link channel 04

4.26.9.9.6.2 Digital SIO inputs

Name:
DigitalInput01 to DigitalInput04

If a channel is being operated in SIO mode (SOI input), this register can be used to read the input status of the channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	DigitalInput01	0	Reset digital SIO input 01
		1	Set digital SIO input 01
...		...	
3	DigitalInput04	0	Reset digital SIO input 04
		1	Set digital SIO input 04
4 - 7	Reserved	-	

4.26.9.9.6.3 Sync (status byte)

Name:
Synchronized01 to Synchronized04
CycleEnd01 to CycleEnd04

The module uses this status register to report whether error-free communication with the device was possible during the last module cycle.

- The CycleEnd bits indicate whether the last data transmitted to the IO-Link device has been processed. The CycleEnd bits are reset after each X2X cycle.
- The synchronized bits indicate that the channel is synchronized without errors.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Synchronized01	0	Synchronization for channel 1 not OK
		1	Synchronization for channel 1 OK
...		...	
3	Synchronized04	0	Synchronization for channel 4 not OK
		1	Synchronization for channel 1 OK
4	CycleEnd01	0	I/O cycle end: No new IO-Link data
		1	I/O cycle end: New data transmitted and received
...		...	
7	CycleEnd04	0	I/O cycle end: No new IO-Link data
		1	I/O cycle end: New data transmitted and received

4.26.9.9.6.4 Overload (status byte)

Name:
Overload01 to Overload04

This status register is used by the module to report whether an overload in the form of overcurrent or overtemperature occurred in the channel supply.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Overload01	0	Channel 1: No overload
		1	Channel 1: Overload
...		...	
3	Overload04	0	Channel 4: No overload
		1	Channel 4: Overload
4 - 7	Reserved	-	

4.26.9.9.6.5 ChannelStatus

Name:
ChannelStatus01 to ChannelStatus04

This register is used to show the current status of the IO-Link channel.

Data type	Value	Information	Status
USINT	0	Channel inactive	Disabled
	1	Use as digital SIO output	SIO mode
	2	Use as digital SIO input	
	3	Startup of IO-Link device, PREOPERATIONAL mode	Communication is running but no process data is exchanged. However, acyclic access is also possible.
	4	Operation, OPERATE mode	Communication is running
	5	Operation, parameter server data OK	
	6	Parameter server: Upload active	Communication is running and process data is being returned.
	7	Parameter server: Download active	
	8	Parameter server: Deleting active	
	9	IODD parameters are written	
	10 to 19	Reserved	
	21	General error in the parameter server. For example: • Parameter server not supported • Error accessing an object that is managed by the parameter server • Internal error	Communication is running. However, an error has occurred on the parameter server. Parameter server errors can be acknowledged via the DsControl register.
	22	Parameter server locked by IO-Link device	
	23	Parameter server empty: Tried to load data to the IO-Link device even though no data is saved in EEPROM	
	24	New serial number recognized: The user must decide via the DsControl register what has to be done (Upload – Download – Restore default values)	
	25	Parameter server not compatible (new DeviceID or new VendorID recognized): The data in EEPROM is not suitable for the connected IO-Link device. The user must decide via the DsControl register whether an upload should be carried out.	
	26	Upload request received. The user must decide via the DsControl register what must be done (Upload – Download – Restore default values).	
	27	The parameter checksum of the IO-Link device has changed: The user must decide via the DsControl register what must be done (Upload – Download – Restore default values).	
	28	Error when sending the SAVE command	
	29	Reserved	
	30	Process data invalid	Communication is running. However, process data was marked as invalid by the device.
	31 - 39	Reserved	
	40	No connection	No communication
	41	Reserved	
	42	The DeviceID and VendorID of the connected IO-Link device do not match the predefined IDs.	Communication is running but no process data is exchanged. However, acyclic access is also possible.
	43	Reserved	
	44	Timestamp error The IO-Link device does not support IO-Link timestamps.	
	45	Error starting up the device	No communication
	46 to 255	Reserved	

4.26.9.9.6.6 FrameCount

Name:
FrameCount01 to FrameCount04

Received IO-Link frames are counted in this register. Unlike the sync bits, the FrameCount register ensures that all frames are actually recognized. This is the case even if X2X cycles are lost or if the IO-Link cycle is faster than the X2X cycle.

Data type	Value
SINT	-128 to 127

4.26.9.9.6.7 CycleStartNettime

Name:
CycleStartNettime01 to CycleStartNettime04

This register can be used to read out the value of the net time at the start of the last IO-Link cycle.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.26.9.9.6.8 CycleEndNettime

Name:
CycleEndNettime01 to CycleEndNettime04

This register can be used to read out the value of the net time at the end of the last IO-Link cycle.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.26.9.9.7 IO-Link data storage

The parameter server

If supported by the IO-Link device, the IO-Link parameter server can be used to read the application-specific device configuration from the IO-Link master, for example. The parameter server of the module is generally activated and can be used with the help of a controller register.

Which data storage parameters are transferred depends on the connected IO-Link device. The read information is stored in EEPROM on the DS module and can be fed back automatically after replacing the device, for example.

The module is capable of processing the data storage upload request (event code 0xFF91) of the IO-Link specification. The request is usually triggered if parameters on the device are changed. In this case, depending on the configuration, an upload of data storage data can be started (standard).

Automatic management of data storage parameters

Automatic management has been designed according to IO-Link specification. Since the IO-Link standard exhibits a degree of tolerance here, it is possible that some IO-Link devices may have to be handled differently. This can be configured using the 4.26.9.9.7.3 "CfO_DS_Config" register.

An upload/download is performed under the following conditions:

- DsControl0x = 1
- When the device is being started up or if a data storage upload requirement has been received.

Offline configuration

With offline configuration, the configuration data set up for the device in Automation Studio is stored in the project. This data is then used to configure the CPU automatically when the project is downloaded or data is generated for the memory card. In contrast to the parameter server, where values are read from an existing device, the values in this case are defined explicitly in the application. The values are automatically configured only one time after the download. This procedure only occurs again if a new parameter file is received from Automation Studio, the device is replaced or if the download is started manually by the library.

This function works independently of the parameter server. If the parameter server is still enabled, however, it can be started as needed after the offline configuration to store the corresponding data. In the event of a replaced device, the data can be loaded to the device from the parameter server.

4.26.9.9.7.1 DsControl

Name:
DsControl01 to DsControl04

This register can be used to control the parameter server manually. Each action is carried out exactly once when the corresponding value is set. If the same action should be executed multiple times, then this register must be set to the value 0 beforehand.

Data type	Value	Information
USINT	0	No action
	1	Operating mode of the parameter server: Automatic upload and download
	2	Upload if data storage parameters are available on the device
	3	Download if data storage parameters are available in the CPU's memory and the device can process them
	4	Acknowledge error status from parameter server (see 4.26.9.9.6.5 "ChannelStatus": error messages 21 to 28)
	5	Delete data storage parameters on the CPU's memory
	6	Start dummy upload. Starts an upload without saving the data. This can be used to acknowledge an upload request.
	7 to 255	Reserved

4.26.9.9.7.2 DsProgress

Name:
DsProgress01 to DsProgress04

The module uses this register to report the progress of the upload or download from the parameter server. The values from 0 to 100 can be used for implementing a progress display.

Data type	Value
USINT	0 to 100

4.26.9.9.7.3 CfO_DS_Config

Name:
CfO_DS_Config01 to CfO_DS_Config04

This register can be used to set the behavior of the parameter server module (when operating the parameter server manually). By doing this, a corresponding reaction is assigned to every trigger event.

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Event	Value	Reaction
0 - 3	The device ID of the connected device no longer matches the device ID saved together with the parameters.	000	No response
		001	Cancel
		010	User-defined reaction. See 4.26.9.9.6.5 "ChannelStatus": Status message 25
		011	Upload (default value)
4 - 7	The device transmitted an upload request.	000	No response
		001	Cancel
		010	User-defined reaction. See 4.26.9.9.6.5 "ChannelStatus": Status message 26
		011	Upload (default value)
8 - 11	A new parameter checksum was detected when starting the device.	000	No response
		001	Cancel
		010	User-defined reaction. See ChannelStatus: Status message 27
		011	Upload
		100	Download (default value)
12 - 15	The serial number of the connected device no longer matches the serial number saved together with the parameters.	000	No response
		001	Cancel
		010	User-defined reaction. See ChannelStatus: Status message 24
		011	Upload
		100	Download (default value)
16 - 23	Reserved	-	
24 - 26	Specifies the order that individual events are checked	000	DeviceID, serial number, upload request, parameter checksum (default value)
		001	DeviceID, serial number, parameter checksum, upload request
		010	DeviceID, upload request, parameter checksum, serial number
		011	DeviceID, upload request, serial number, parameter checksum
		100	DeviceID, parameter checksum, upload request, serial number
		101	DeviceID, parameter checksum, serial number, upload request
27 - 31	Reserved	-	

4.26.9.9.7.4 CfO_DS_SaveCtrl

Name:
CfO_DS_SaveCtrl01 to CfO_DS_SaveCtrl04

This register is used together with 4.26.9.9.7.5 "CfO_DS_SaveData".

Some IO-Link devices must be instructed to save transferred data storage parameters in remanent memory after a download. In order for these parameters to be applied to remanent memory on these devices, the recorded index and subindex in these registers must be sent together with the save command (e.g. value 163 on index 2, subindex 0).

Data type	Value
UDINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 15	Index	0 to 255	Device-specific index for save command
16 - 24	Subindex	0 to 255	Device-specific subindex for save command
24 - 26	Data length	0	Save command disabled
		1 to 4	The data length of the save command estimated by the device in bytes
27 - 31	Reserved		

4.26.9.9.7.5 CfO_DS_SaveData

Name:
CfO_DS_SaveData01 to CfO_DS_SaveData04

This register is used together with 4.26.9.9.7.4 "CfO_DS_SaveCtrl" and contains the value written to the index configured in the CfO_DS_SaveCtrl register.

Data type	Value
UDINT	0 to 4,294,967,295

4.26.9.9.8 IO-Link timestamp

The IO-Link timestamp register allows the relation of IO-Link timestamps to the net time of a controller, and vice versa.

This makes it possible to relate the times of value changes of the IO-Link device exactly to the net time of the controller, and vice versa. Events can be captured or triggered with a higher timing resolution than would be possible with the IO-Link cycle. This allows a highly precise timed response from the controller to signals from the sensor, and vice versa. The resolution depends on the devices being used.

Examples

- For an input device, the timestamp is saved directly by the device when a certain event occurs (e.g. photo-electric sensor triggered) and then transferred via IO-Link. The IO-Link master converts this IO-Link-specific timestamp to a net time timestamp that can be used across the system.
- In the output direction, a converted timestamp is transferred to the device via IO-Link. The output device responds at the corresponding instant and executes the intended event (e.g. closes a switch).

Information:

- **The timestamp function is device-specific and not supported by every IO-Link device.**
- **This function cannot be used if the channel is being operated in free-running mode (asynchronous).**

4.26.9.9.8.1 IoLinkTimestampIn

Name:
IoLinkTimestampIn01 to IoLinkTimestampIn04

This register indicates the net time instant at which the application event occurred.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.26.9.9.8.2 IoLinkTimestampInStatusSeq

Name:
IoLinkTimestampInStatusSeq01 to IoLinkTimestampInStatusSeq04

This register indicates information about the timestamp input.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Sequence number	0 to 15	The sequence number is increased by 1 each time a valid timestamp is received. If the sequence number is increased by more than 1, it means that the event was lost.
4	Event 1 triggered by application	x	Signal state when timestamp occurs
5	Event 2 triggered by application	x	Signal state when timestamp occurs **Example:** Signal state when timestamp occurs – Photoelectric sensor triggered → This bit = 0 – Photoelectric sensor not triggered → This bit = 1
6	Reserved	-	
7	Timestamp error	0	No error
		1	An error occurred on the IO-Link device. Possible causes: • More timestamps were generated than could be transferred. • The value of the IO-Link timestamp exceeded the permitted range of values. In both cases, it may help to reduce the IO-Link cycle time.

4.26.9.9.8.3 IoLinkTimestampOut

Name:
IoLinkTimestampOut01 to IoLinkTimestampOut04

The user can write the net time for the output timestamp to this register.
The net time is automatically converted to an IO-Link timestamp. The event is triggered at the defined net time. The IoLinkTimestampOutStatus register is used for acknowledgment.

Information:

The net time must be at least three IO-Link cycles in the future; otherwise, a warning is set in IoLinkTimestampOutStatus.

This register's data type must match the format configured in register 4.26.9.9.5.1 "ChannelMode", bit 26.

Data type	Value
INT	-32,768 to 32,767
DINT	-2,147,483,648 to 2,147,483,647

4.26.9.9.8.4 IoLinkTimestampOutCtrlSeq

Name:
IoLinkTimestampOutCtrlSeq01 to IoLinkTimestampOutCtrlSeq04

This register is used to control how the timestamp is applied.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Sequence number	0 to 15	Output timestamp and application event bits applied when the sequence number is increased by 1
4	Application event 1	x	Output state at the timestamp
5	Application event 2	x	Output state at the timestamp
6	Acknowledge warning	0	Do not acknowledge
		1	Acknowledge warning
7	Acknowledging errors	0	Do not acknowledge
		1	Acknowledging errors

4.26.9.9.8.5 IoLinkTimestampOutStatus

Name:
IoLinkTimestampOutStatus01 to IoLinkTimestampOutStatus04

This register is used to show the status of the timestamp output.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Acknowledgment of sequence number	0 to 15	When an output timestamp has been successfully applied, then the sequence number from IoLinkTimestampOutCtrlSeq is acknowledged here.
4 - 5	Reserved	-	
6	Warning	0	No warning
		1	A timestamp was not at least 3 cycles in the future, so output may be delayed.
7	Errors	0	No error
		1	More timestamps were transferred to the module than could be output.

4.26.9.9.9 IO-Link process data

The input or output data stream of IO-Link process data can be broken down into any structure. The structure is configured as follows:

- The firmware provides 8 32-bit registers for each channel to allow the mapping of maximum 32 bytes of IO-Link process data.
- The I/O configuration sets the type with which the register should be registered. So that the length is correct, the PDI_TypeInfo register (for input data) or PDO_TypeInfo register (for output data) is used to configure how many bytes of the IO-Link data stream should be copied to the register, or vice versa.

Limitations:

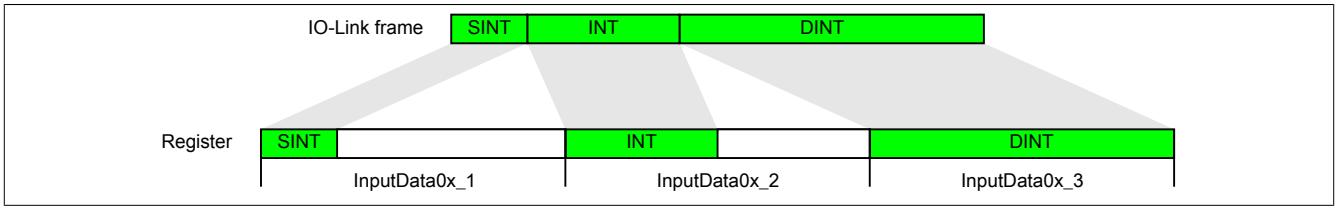
8 registers with 32 bits are available per channel. This makes it possible to register any 8 data points in this way. If this is not sufficient, it is also possible to use a byte array. The user then has to make sure that the bytes are divided up into the necessary data types.

Information:

With a bit array, it is important that the byte arrangement is correct within the register. The module DOES NOT make any necessary conversions from big-endian to little-endian or reverse.

Example

Dividing up elements from an IO-Link data stream into multiple 32-bit registers:



4.26.9.9.9.1 OutputData

Name:
OutputData01_1 to OutputData04_8

Output data from the IO-Link device in IO-Link communication mode. A byte array is also a possible alternative. The user then has to make sure that the bytes are divided up into the necessary data types.
The PDO_TypeInfo register can be used to configure how many bytes should be applied to the IO-Link frame from the output registers.

Data type	Value
USINT	0 to 255
SINT	-128 to 127
UINT	0 to 65535
INT	-32,768 to 32,767
UDINT	0 to 4,294,967,295
DINT	-2,147,483,648 to 2,147,483,647
REAL	-3.4E38 – 3.4E38

4.26.9.9.9.2 InputData

Name:
InputData01_1 to InputData04_8

Input data from the IO-Link device in IO-Link communication mode. A byte array is also a possible alternative. The user then has to make sure that the bytes are divided up into the necessary data types.

Data type	Value
USINT	0 to 255
SINT	-128 to 127
UINT	0 to 65535
INT	-32,768 to 32,767
UDINT	0 to 4,294,967,295
DINT	-2,147,483,648 to 2,147,483,647
REAL	-3.4E38 – 3.4E38

4.26.9.9.10 IO-Link information data

The IO-Link information data is used to read device-specific values as well as to check the IO-Link configuration. It is only possible to read the following registers.

4.26.9.9.10.1 VendorId

Name:
VendorId01 to VendorId04

This register contains the unique vendor ID of the IO-Link device.

Data type	Value
UINT	0 to 65535

4.26.9.9.10.2 DeviceId

Name:
DeviceId01 to DeviceId04

This register contains the unique ID of the IO-Link device.

Data type	Value
UDINT	0 to 4,294,967,295

4.26.9.9.10.3 FunctionId

Name:
FunctionId01 to FunctionId04

This register contains the device's function class provided by the vendor.

Data type	Value
UINT	0 to 65535

4.26.9.9.10.4 CycleTime

Name:
CycleTime01 to CycleTime04

Some IO-Link devices cannot handle high-speed cycles and require a higher cycle time. This register can be used to read back the channel's IO-Link cycle time currently being used. The time used for communication is always a multiple of 100 µs, e.g. 50 for 5 ms cycle time.

Data type	Value	Information
UINT	0 to 65535	Specified in 100 µs steps

4.26.9.9.10.5 CycleMultible

Name: CycleMultible01 to CycleMultible04

This register can be used to read back the multiplicator currently being used for the channel's IO-Link cycles.

Data type	Value
UINT	0 to 65535

4.26.9.9.10.6 CycleDivisor

Name:
CycleDivisor01 to CycleDivisor04

This register can be used to read back the divisor currently being used for the channel's IO-Link cycles.

Data type	Value
UINT	0 to 65535

4.26.9.9.10.7 MinCycleTime

Name:
MinCycleTime01 to MinCycleTime04

This register can be used to read back the minimum IO-Link cycle time. The minimum IO-Link cycle time depends on the IO-Link device and is read from the module after establishing communication with the IO-Link device.

Data type	Value
UINT	0 to 65535

4.26.9.9.10.8 PDI_Size

Name:
PDI_Size01 to PDI_Size04

This register can be used to read back the size of the input process data defined by the device. This value is read when starting up the IO-Link device.

Data type	Value
USINT	0 to 255

4.26.9.9.10.9 PDO_Size

Name:
PDO_Size01 to PDO_Size04

This register can be used to read back the size of the output process data defined by the device. This value is read when starting up the IO-Link device.

Data type	Value
USINT	0 to 255

4.26.9.9.10.10 Baud rate

Name:
Baudrate01 to Baudrate04

This register can be used to read back the baud rate defined by the IO-Link device. This value is read when starting up the IO-Link device.

Data type	Value	Information
USINT	1	COM1 = 4.8 kbit/s
	2	COM2 = 38.4 kbit/s
	3	COM3 = 230.4 kbit/s

4.26.9.9.10.11 IoLinkVersionID

Name:
IoLinkVersionID01 to IoLinkVersionID04

This register can be used to read back the IO-Link version.

Data type	Value	Information
USINT	16 (= 0x10)	V1.0
	17 (= 0x11)	V1.1

4.26.9.9.11 Event interface

IO-Link devices are able to send events that can be retrieved using cyclic data points. The events are written to a FIFO buffer that has space for up to 16 elements. If events are not retrieved or more than 16 events take place, then the oldest event is automatically discarded.

Sequence for reading an event

- A new event was triggered by the device. This is indicated by an increase in EventPortSeq.
- Event data can be read using the EventQualifier and EventCode registers.
- The event must be acknowledged. To do so, the sequence number from EventPortSeq must be copied to the sequence number from EventQuit.
- The next event is specified only after the event is acknowledged.

4.26.9.9.11.1 EventPortSeq

Name:
EventPortSeq

As soon as a new event is generated by an IO-Link device, the sequence number is increased in this register. The affected channel number is also displayed.

Data type	Value
USINT	0 to 255

Bit structure:

Bit	Description	Value	Information
0 - 3	Sequence number	0 to 15	
4 - 5	IO-Link channel number	00	IF1 (channel 1)
		01	IF2 (channel 2)
		10	IF3 (channel 3)
		11	IF4 (channel 4)
6 - 7	Reserved	0	

4.26.9.9.11.2 EventQualifier

Name:
EventQualifier

This register contains additional information about the event.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Instance layer generated by the event	000	Unknown
		001	Hardware
		010	Data exchange layer of the IO-Link device
		011	Application layer of the IO-Link device
		100	Application
3	Cause of the event	0	Device
		1	Master
4 - 5	Type of event	00	Reserved
		01	Information
		10	Warning
		11	Errors
6 - 7	Mode of the event	00	Reserved
		01	One-time event
		10	Event no longer reported (e.g. voltage OK again)
		11	Event reported (e.g. voltage too low)

4.26.9.9.11.3 EventCode

Name:
EventCode

The event code of the event being transferred is indicated in this register. The event codes may be vendor-specific event codes or event codes defined in the IO-Link specification.

Data type	Value
UINT	0 to 65535

4.26.9.9.11.4 EventsLeft

Name:
EventsLeft

This register indicates the number of as yet unprocessed events in the FIFO buffer.

Data type	Value
USINT	0 to 16

4.26.9.9.11.5 EventQuit

Name:
EventQuit

This register can be used to acknowledge errors. This is done by copying the sequence number of the event to be acknowledged to this register.

Data type	Value
USINT	0 to 15

4.26.9.9.11.6 EventQuitReadBack

Name:
EventQuitReadBack

This register contains the sequence number of the most recently acknowledged event.

Data type	Value
USINT	0 to 15

4.26.9.9.12 Command interface

The command interface offers the option of accessing the object dictionary of the IO-Link device using the index and subindex. Access is also possible using the AsIOLink library or FlatStream.

Information:

With this interface, up to the first 4 bytes of an object can be read or written.

Procedure for write operation:

- Set the object to be written using ParameterIndexOut and ParameterSubIndexOut.
- Write the data to be written to ParameterDataOut.
- Set read/write, IF and the sequence number increased by 1 in the ParameterCtrlOut register.
- Wait until the sequence acknowledgment in ParameterCtrlIn is the same as the sequence number.

Procedure for read operation:

- Set the object to be read using ParameterIndexOut and ParameterSubIndexOut.
- Delete bit 7 in the ParameterCtrlOut parameter, set the channel number and increase the sequence number.
- Wait until the sequence acknowledgment in ParameterCtrlIn is the same as the sequence number.
- Read the error status from ParameterCtrlIn. An error is indicated by a set error bit.
- Read the data from ParameterCtrlIn.

For error-related behavior, see 4.26.9.9.15 "Error codes".

4.26.9.9.12.1 ParameterIndexOut

Name:
ParameterIndexOut

This register defines the index of the object in the object dictionary that should be accessed.

Data type	Value
UINT	0 to 65535

4.26.9.9.12.2 ParameterSubIndexOut

Name:
ParameterSubIndexOut

This register defines the subindex of the object in the object dictionary that should be accessed.

Data type	Value
USINT	0 to 255

4.26.9.9.12.3 ParameterCtrlOut

Name:
ParameterCtrlOut

This register defines the type of access to be used.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Sequence number	0 to 3	
2 - 3	IO-Link channel number	0	IF1 (channel 1)
		1	IF2 (channel 2)
		2	IF3 (channel 3)
		3	IF4 (channel 4)
4 - 6	Data length	0 to 4	
7	Read or write	0	Read
		1	Write

4.26.9.9.12.4 ParameterDataOut

Name:
ParameterDataOut_0

This register contains the data that should be written.

Data type	Value
UDINT	0 to 4,294,967,295

4.26.9.9.12.5 ParameterCtrlIn

Name:
ParameterCtrlIn

This register monitors the status of the access.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Sequence confirmation	0 to 3	
2 - 3	IO-Link channel number	0	IF1 (channel 1)
		1	IF2 (channel 2)
		2	IF3 (channel 3)
		3	IF4 (channel 4)
4 - 6	Data length	0 to 4	
7	Error bit	0	No error
		1	Error, the error code is indicated in ParameterDataIn.

4.26.9.9.12.6 ParameterDataIn

Name:
ParameterDataIn_0

After a successful read operation, this register contains the input data. In the event of an error, it contains the error codes.

Data type	Value
UDINT	0 to 4,294,967,295

Error display

- If the error code does not equal 8 (e.g. error reported by device), then the LSB receives the error code.
- If an error is reported by the device, then the error specified by the IO-Link device is also indicated.

UDINT			
MSB			**LSB**
Reserved	IO-Link error code	Additional IO-Link error code	8

4.26.9.9.13 FlatStream communication

4.26.9.9.13.1 Introduction

B&R offers an additional communication method for some modules. "FlatStream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transmission to be handled more efficiently than with standard cyclic polling.

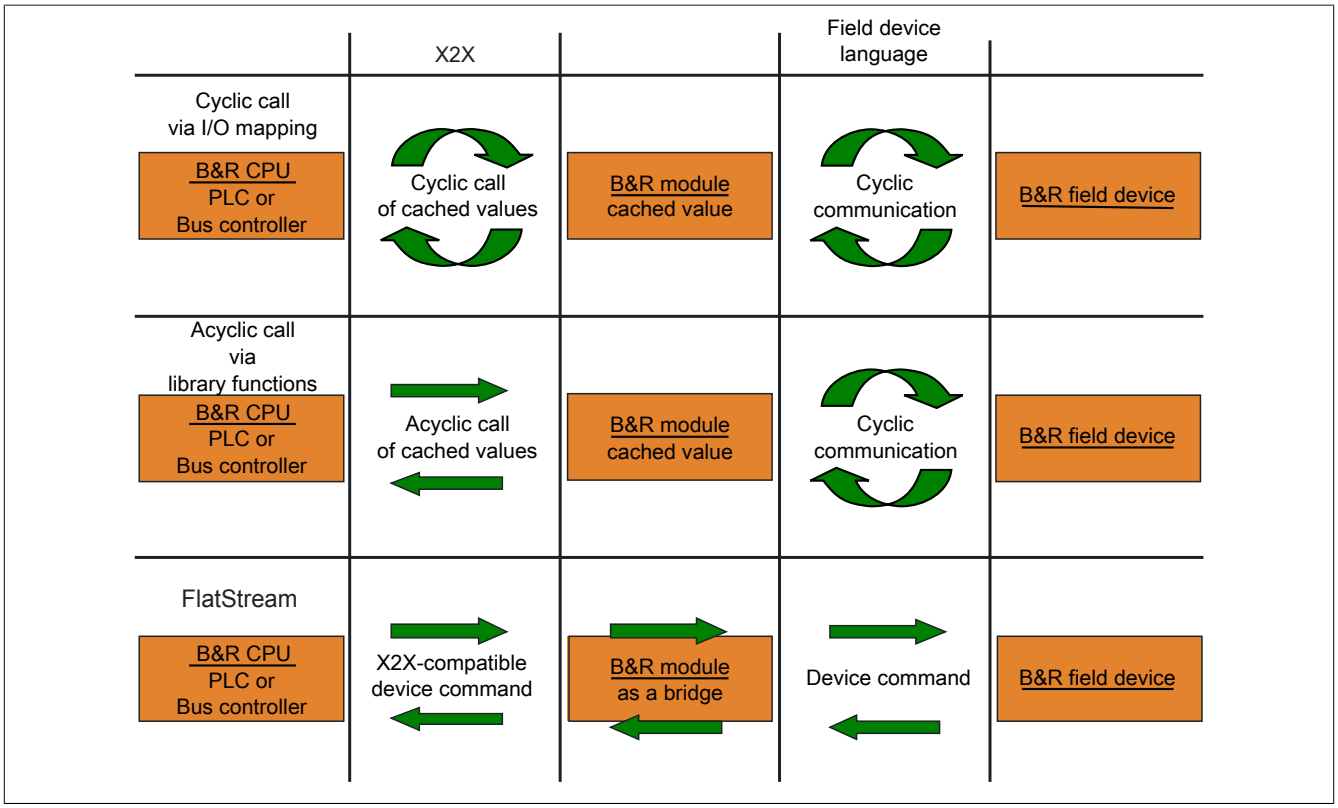


Figure 507: Three types of communication

FlatStream extends cyclic and acyclic data queries. With FlatStream communication, the module acts as a bridge. It is used to pass CPU queries directly on to the field device.

4.26.9.9.13.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With FlatStream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between two partner stations. The length of a message is not restricted by the FlatStream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transmitted segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment needs to be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transmitted to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With FlatStream communication, the number of sequences sent are counted. Successfully transmitted sequences must be acknowledged by the receiving station to ensure the integrity of the transmission.

MTU (Maximum Transmission Unit) – Physical transport:

MTU refers to the enabled USINT registers used with FlatStream. These registers can accept at least one sequence and pass it on to the receiving station. A separate MTU is defined for each direction of communication. The OutputMTU defines the number of FlatStream Tx bytes, and the InputMTU specifies the number of FlatStream Rx bytes. The MTUs are transported cyclically via the X2X Link, increasing the load with each additional enabled USINT register.

Features

FlatStream messages are not transmitted cyclically or in 100% real time. Many bus cycles may be needed to transmit a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by the "InputSequence" or "OutputSequence" register.

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using FlatStream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses the SequenceAck to determine that the transmission was faulty and that all affected sequences will have to be repeated.

4.26.9.9.13.3 The FlatStream principle

Prerequisites and requirements

Before FlatStream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to FlatStream conventions. This allows the FlatStream data to be organized very efficiently without having to block other important resources.

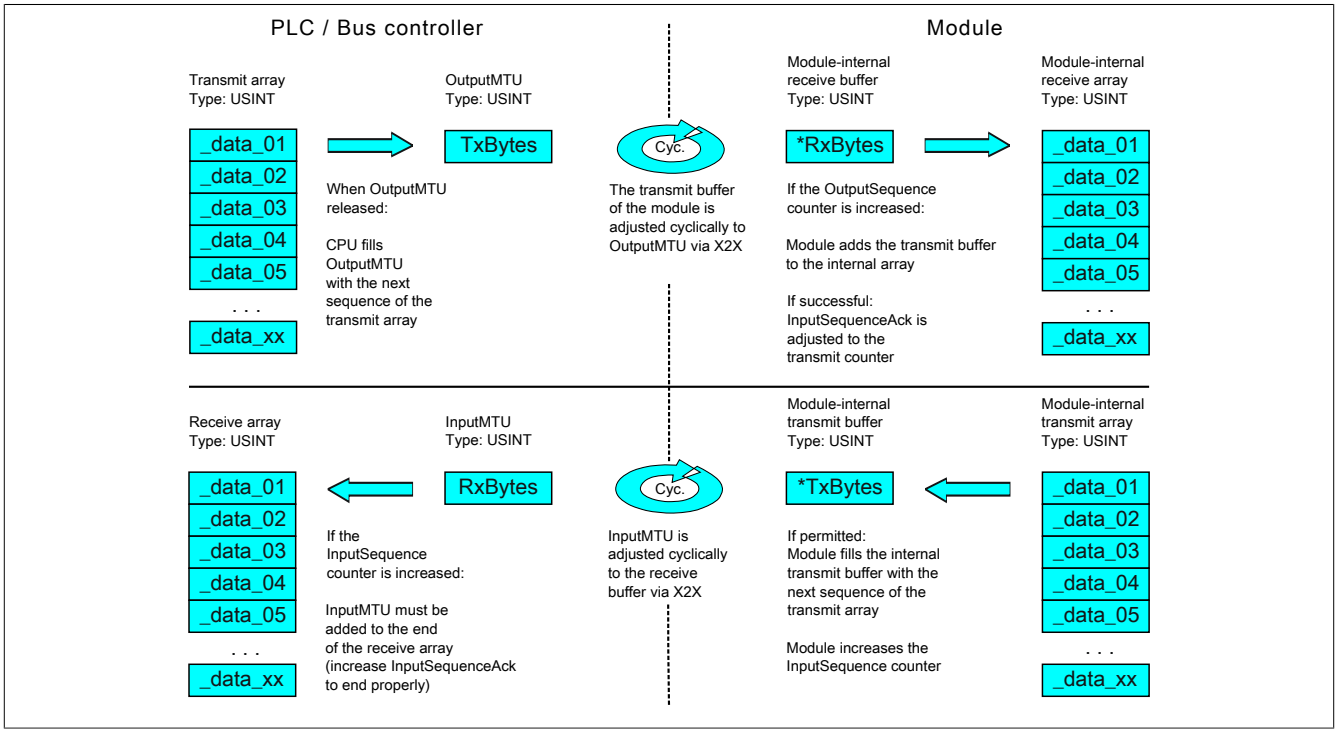


Figure 508: FlatStream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
When the array has been completely created, the transmitter checks whether the MTU is allowed to be refilled. Then it copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transmission is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transmission, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages once they have been completely transmitted.

4.26.9.9.13.4 Registers for FlatStream mode

Five registers are available for configuring FlatStream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via the "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

FlatStream configuration

To use FlatStream, the program sequence must first be expanded. The cycle time of the FlatStream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, the "InputMTU" and "OutputMTU" registers need to be configured. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transmit data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the FlatStream protocol. This functionality is useful for substantially increasing the FlatStream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes, i.e. the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this documentation, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Value
USINT	See the module-specific register overview (theoretically: 3 to 27)

FlatStream operation

When using FlatStream, the communication direction is enormously important. For sending data to a module ("output" direction), the Tx bytes are used. For receiving data from a module ("input" direction), the Rx bytes are used. The "OutputSequence" and "InputSequence" registers are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transmitted successfully.

Transporting the payload data and the control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of the "OutputMTU" and "InputMTU" registers, respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, names were chosen from the CPU point of view.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Value
USINT	0 to 65,535

Control bytes

In addition to the payload data, the Tx and Rx bytes also transmit the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transmitted segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the configured segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 of the control byte.

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is to be expected. This information is especially important when using the "MultiSegmentMTU" option.
When using FlatStream communication with multi-segment MTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but directly after the current segment.

MessageEndBit

The "MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transmitted and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transmitted can be calculated by adding all of the message's segment lengths together.

FlatStream formula for calculating message length:

Message [bytes] = SegmentLengths (all CBs without ME) + SegmentLength (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

The "OutputSequence" register contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors the InputSequenceCounter value
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses the OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses the OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of the InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

The "InputSequence" register contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors the OutputSequenceCounter value
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses the InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses the InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of the OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

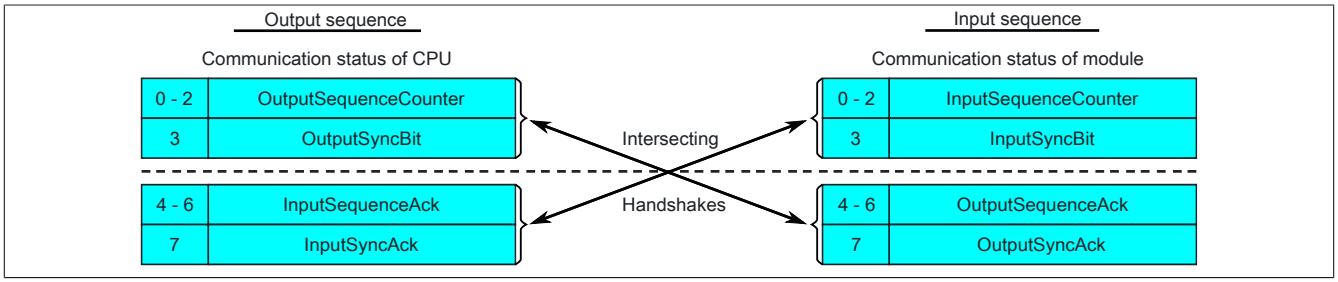


Figure 509: Relationship between OutputSequence and InputSequence

The "OutputSequence" and "InputSequence" registers are logically composed of two half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then the SyncBit must be adjusted on that station. Before new data can be transmitted, the channel needs to be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transmitted completely are processed.

Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of the SequenceCounter is stored on the station receiving the message.
FlatStream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They have to be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to the OutputSequenceCounter and reset the OutputSyncBit. The CPU must cyclically query the high nibble of the "InputSequence" register (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module doesn't accept the current contents of the InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) When the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is allowed to increment the OutputSequenceCounter. The CPU continues cyclically querying the high nibble of the "OutputSequence" register (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transmitted from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transmitting data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, FlatStream cannot be used at this point in time to send messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments the InputSequenceCounter. *The module monitors the high nibble of the "OutputSequence" registers and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not allowed to accept the current contents of the InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets the InputSyncBit. *The module monitors the high nibble of the "OutputSequence" register and expects 1 in InputSyncAck.*
3) The CPU is allowed to set InputSyncAck. **Note:** Theoretically, data can already be transmitted in this cycle. If the InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes have to be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

Transmitting and receiving

If a channel is synchronized, then the opposite station is ready to receive messages from the transmitter. Before the transmitter can send data, it needs to first create a transmit array in order to meet FlatStream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transmitted should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

FlatStream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

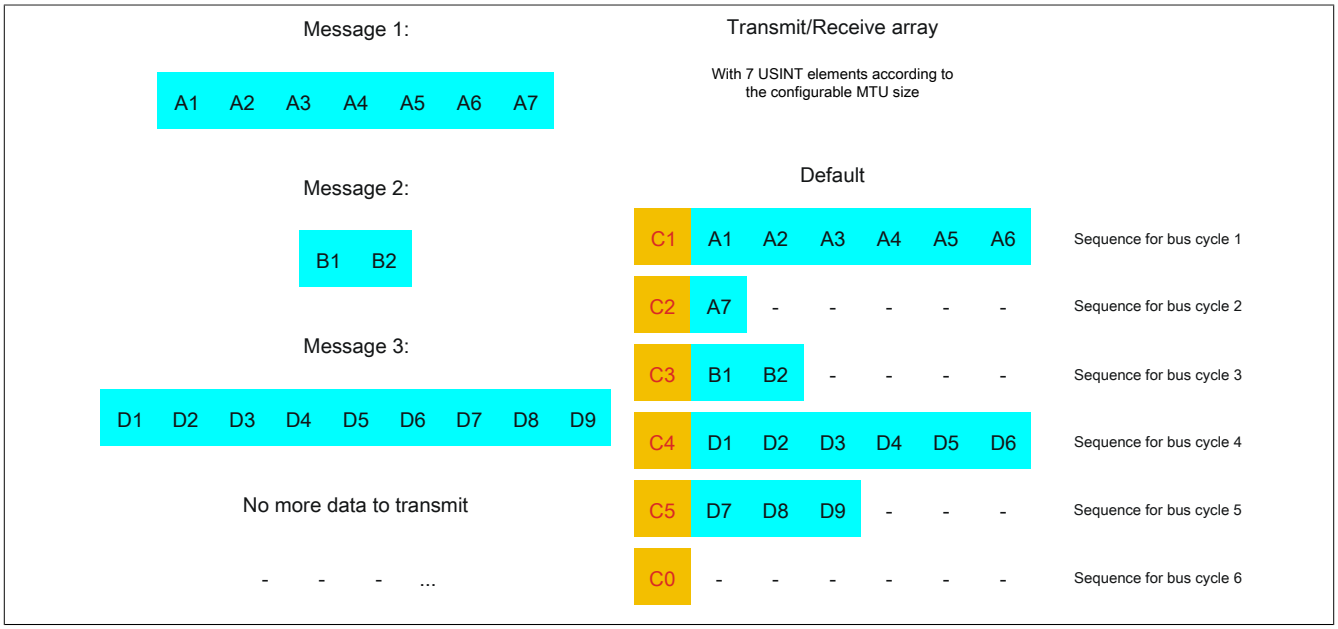


Figure 510: Transmit/Receive array (default)

First, the messages must be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 649: FlatStream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 650: FlatStream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transmitted one by one using FlatStream and received by the module.

Information:

Although all B&R modules with FlatStream communication always support the most compact transmissions in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

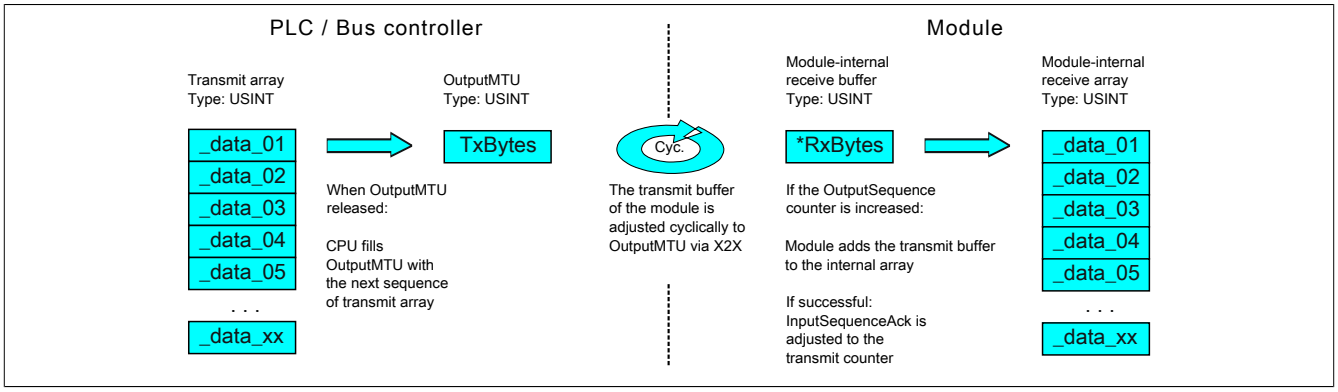


Figure 511: FlatStream communication (output)

The length of the message is initially smaller than the OutputMTU. In this case, one sequence would be sufficient to transmit the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to the OutputMTU. → The OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase the OutputSequenceCounter.
Response: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array* *- The module sends acknowledgment, writes the value of OutputSequenceCounter to OutputSequenceAck*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually.) - Subsequent sequences can only be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than the OutputMTU

The transmit array, which needs to be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flow chart

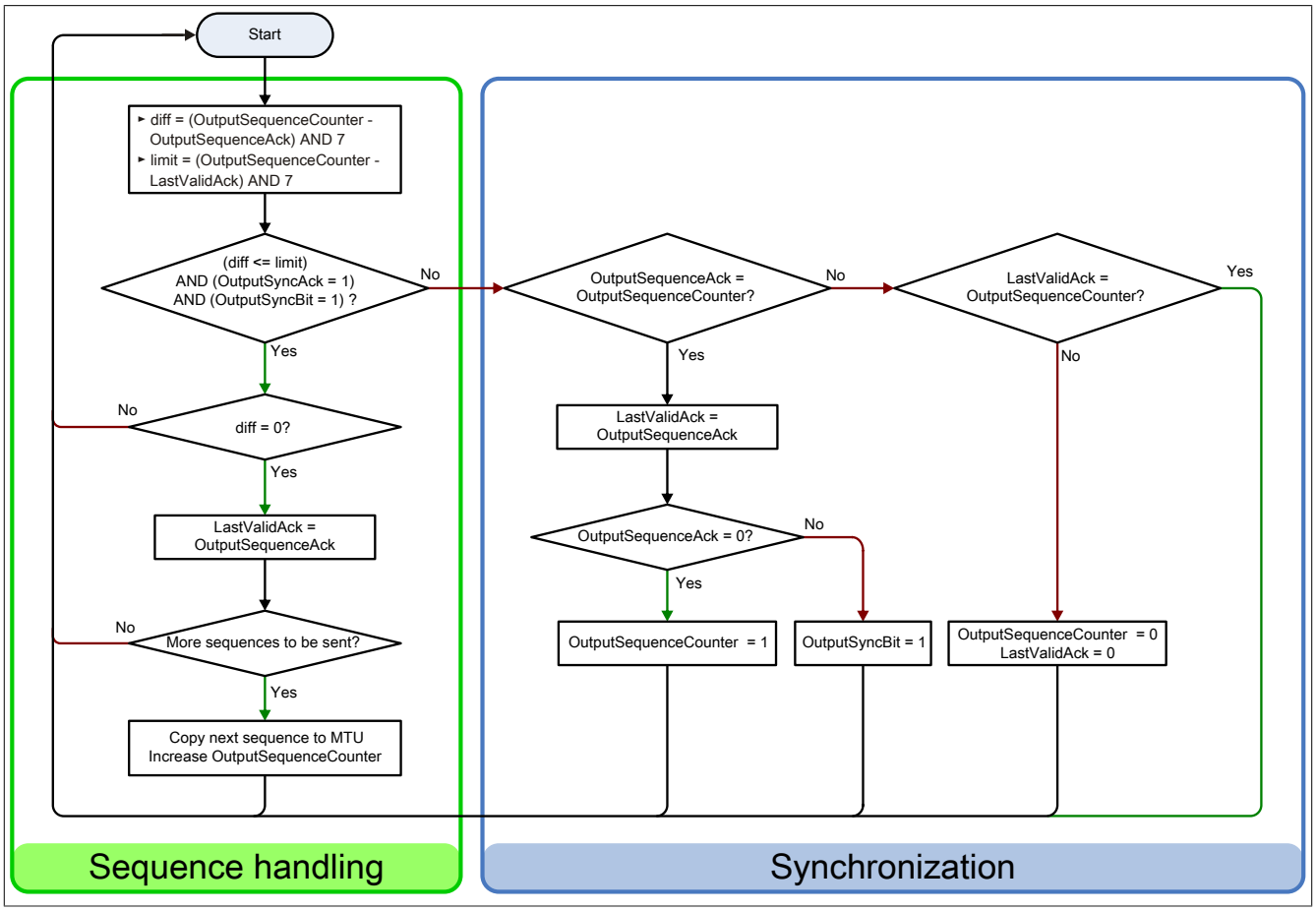


Figure 512: Flow chart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via FlatStream and must then be reproduced in the receive array. The structure of the incoming data stream can be configured with the mode register. The algorithm for receiving the data does not change in this regard.

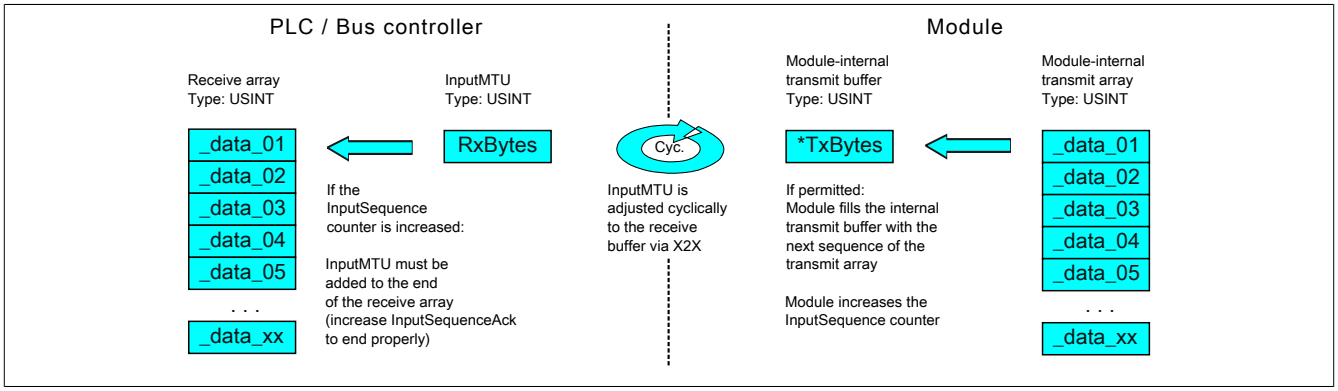


Figure 513: FlatStream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputSequenceAck*
Preparation: *- The module forms the segments, creates the control bytes and transmit array*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer* *- The module increases InputSequenceCounter*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences may only be sent in the next bus cycle after the completion check has been carried out successfully.*

General flow chart

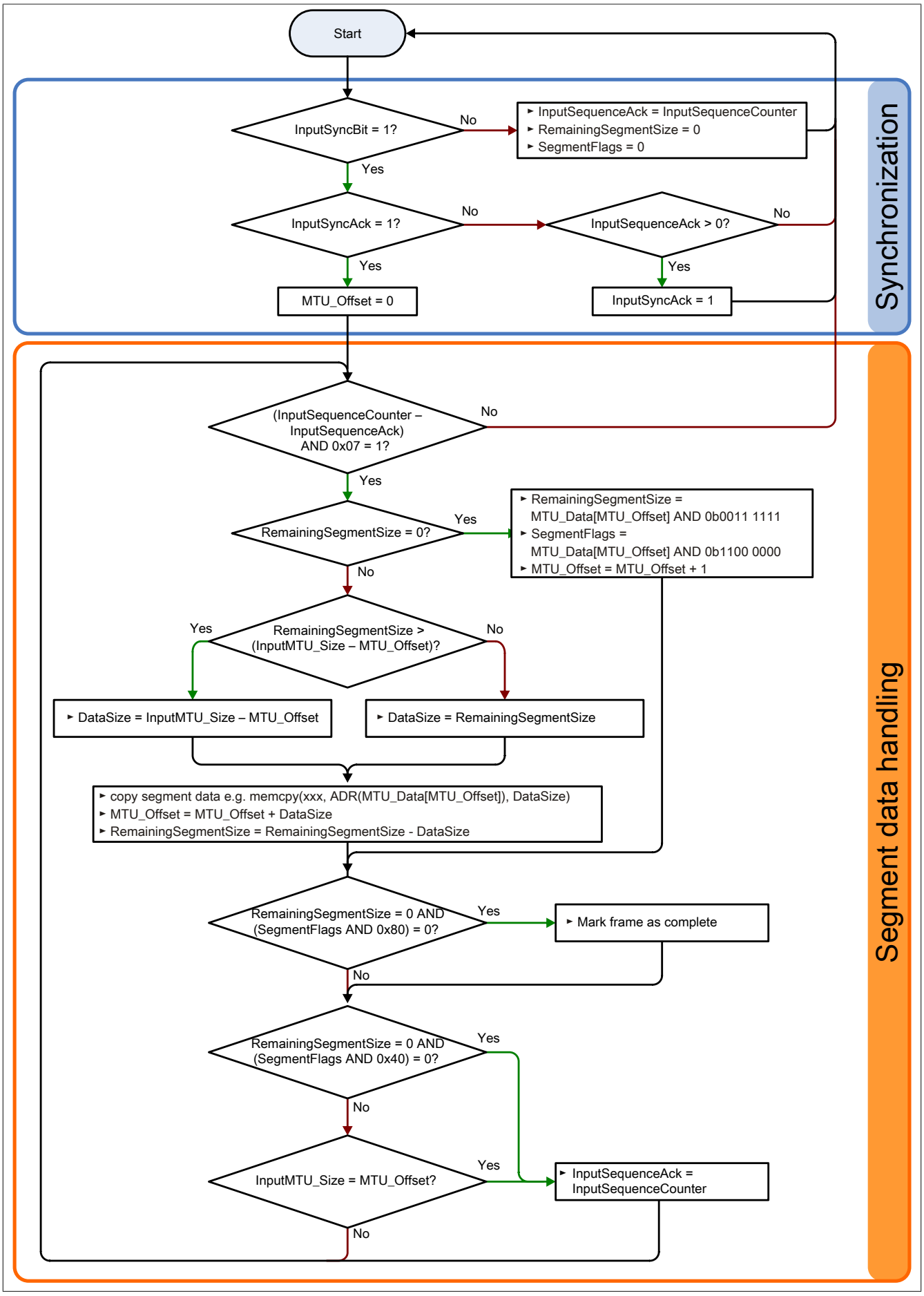


Figure 514: Flow chart for the input direction

Details

It is recommended to store transmitted messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transmitting with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it's important to make sure that a sufficient number of receive arrays can be managed. The entire sequence must be accepted before it is possible to change the Acknowledge register.

If a SequenceCounter is incremented by more than one value, then an error has occurred.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transmitted sequence from the opposite station's SequenceAck and continue the transmission from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the SequenceCounter value sent along with the transmission and matches the SequenceAck to it. The transmitter reads the SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transmission needs to be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It needs to be sent again once the channel has been resynchronized.

FlatStream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers two options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer FlatStream mode support the options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transmission only needs to be explicitly allowed in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Allowed
1	Large segments	0	Not allowed (default)
		1	Allowed
2 - 7	Reserved		

Standard

By default, both options relating to compact transmission in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a FlatStream message can be of any length, the last segment of the message frequently doesn't fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

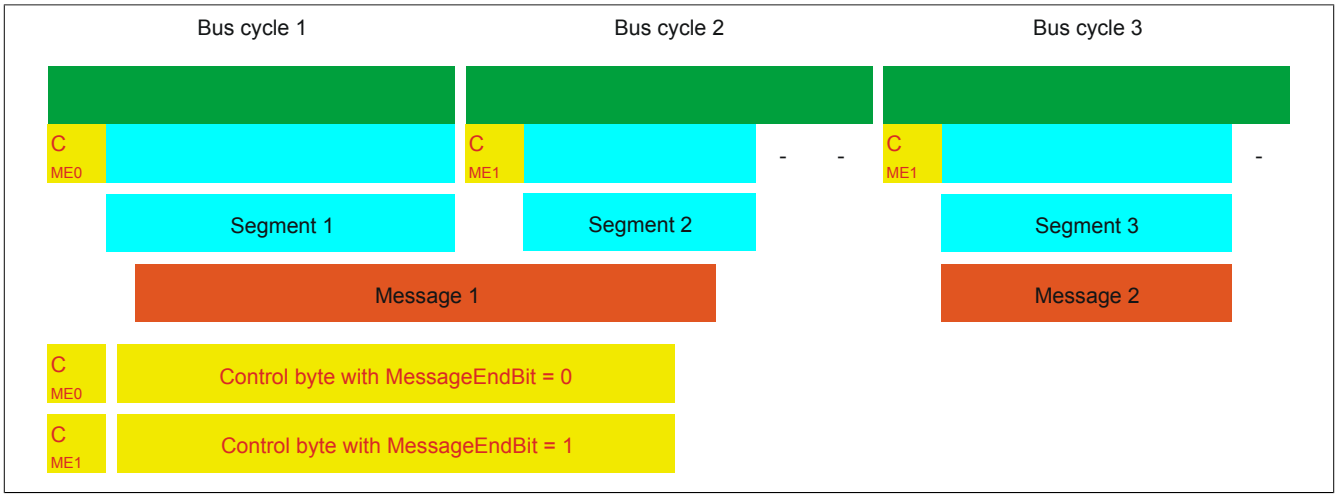


Figure 515: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, the InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transmit the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

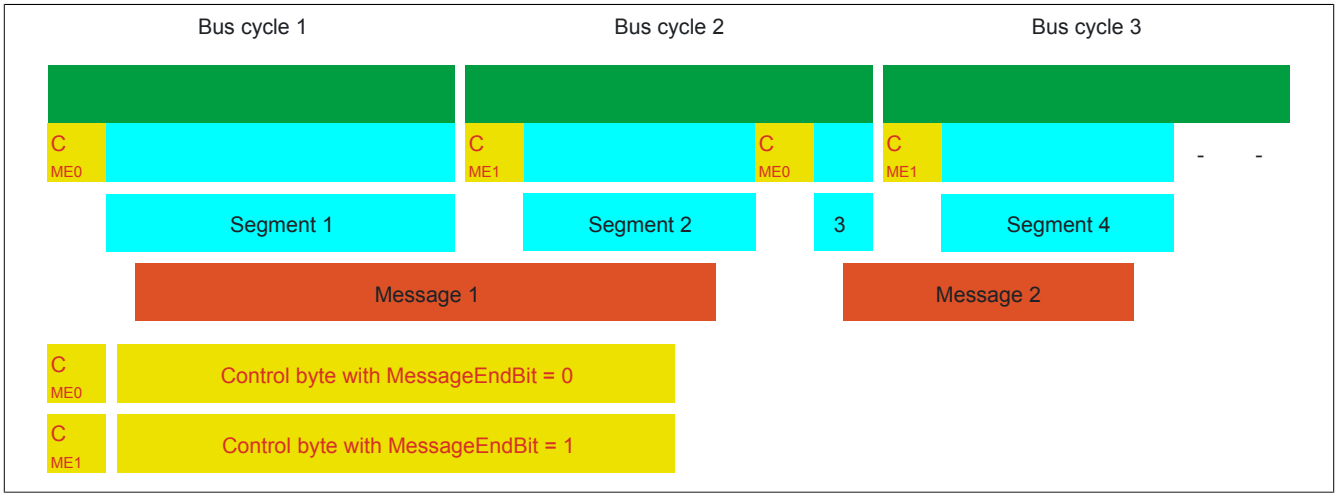


Figure 516: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transmitting very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte needs to be created and transmitted for each segment. With the "Large segments" option, the segment length is limited to 63 bytes independently of the InputMTU. One segment can stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

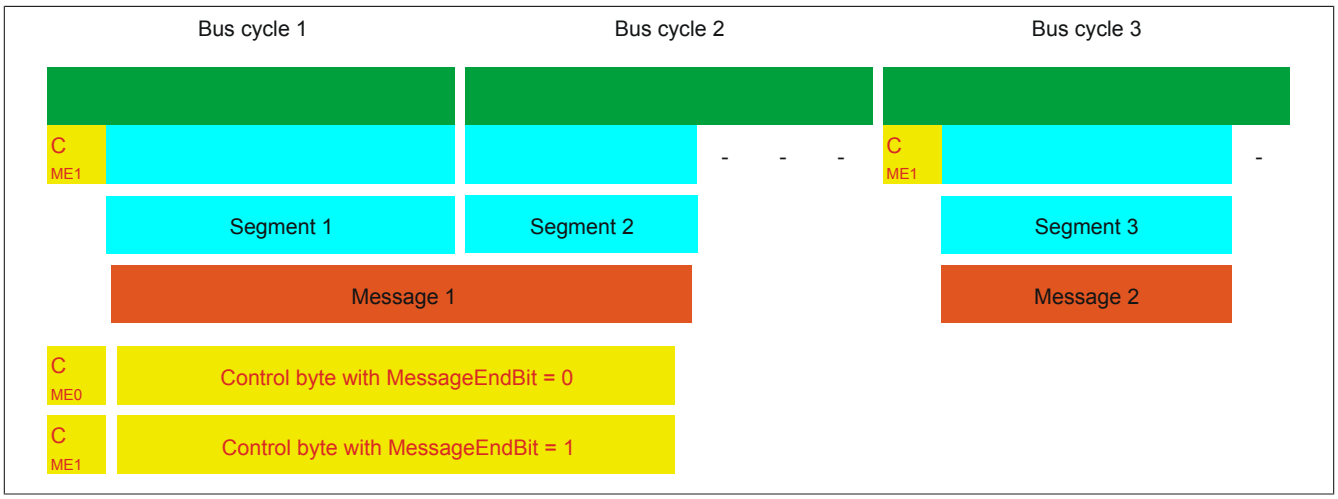


Figure 517: Arrangement of messages in the MTU (large segments)

Using both options

It is also possible to use both options at the same time.

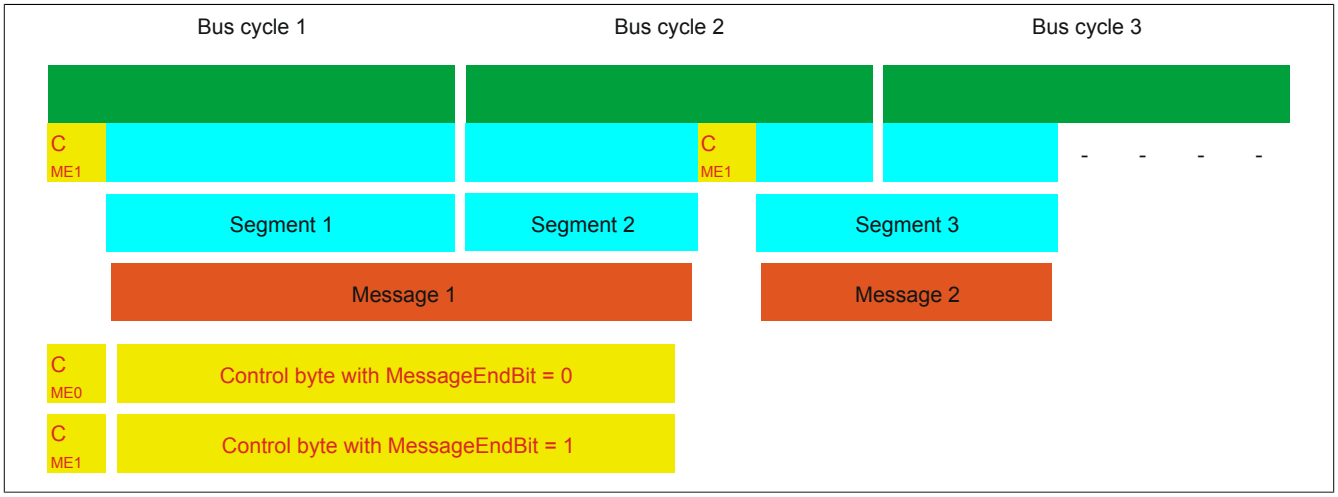


Figure 518: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

Adjusting the FlatStream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transmit the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of MultiSegmentMTUs.

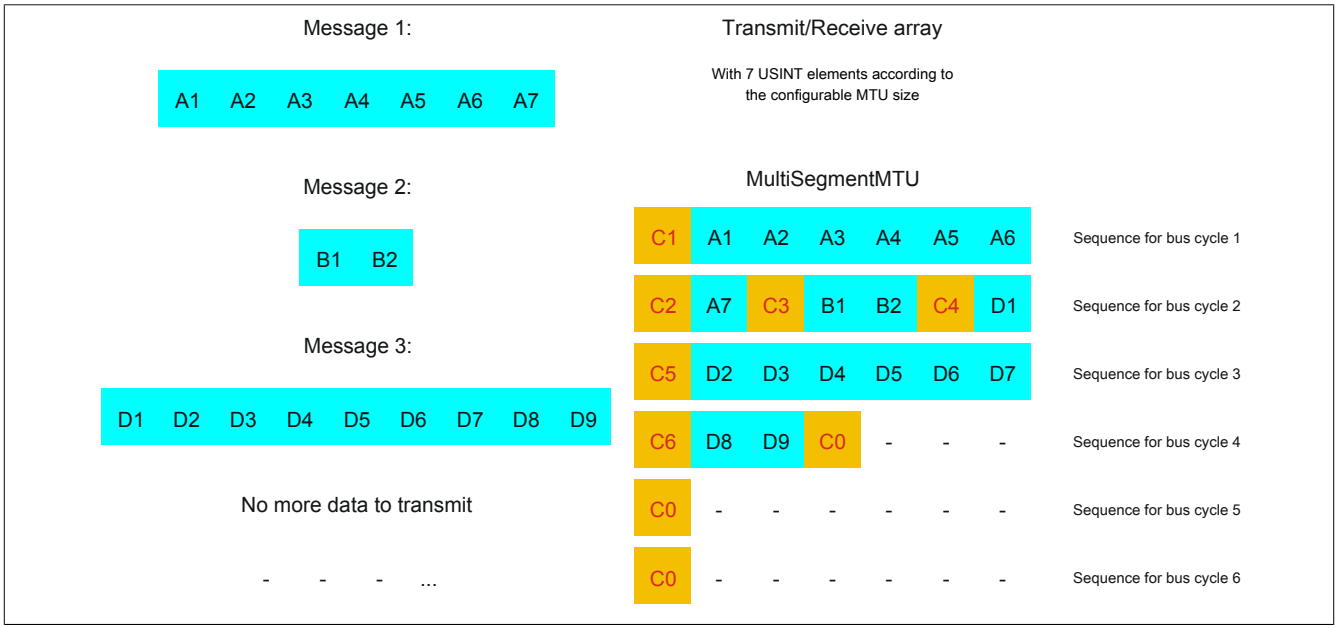


Figure 519: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is sent after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 651: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence must have been completely processed before it can be acknowledged with SequenceAck. In this example, there are three different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 652: FlatStream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transmitted. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transmission of large segments.

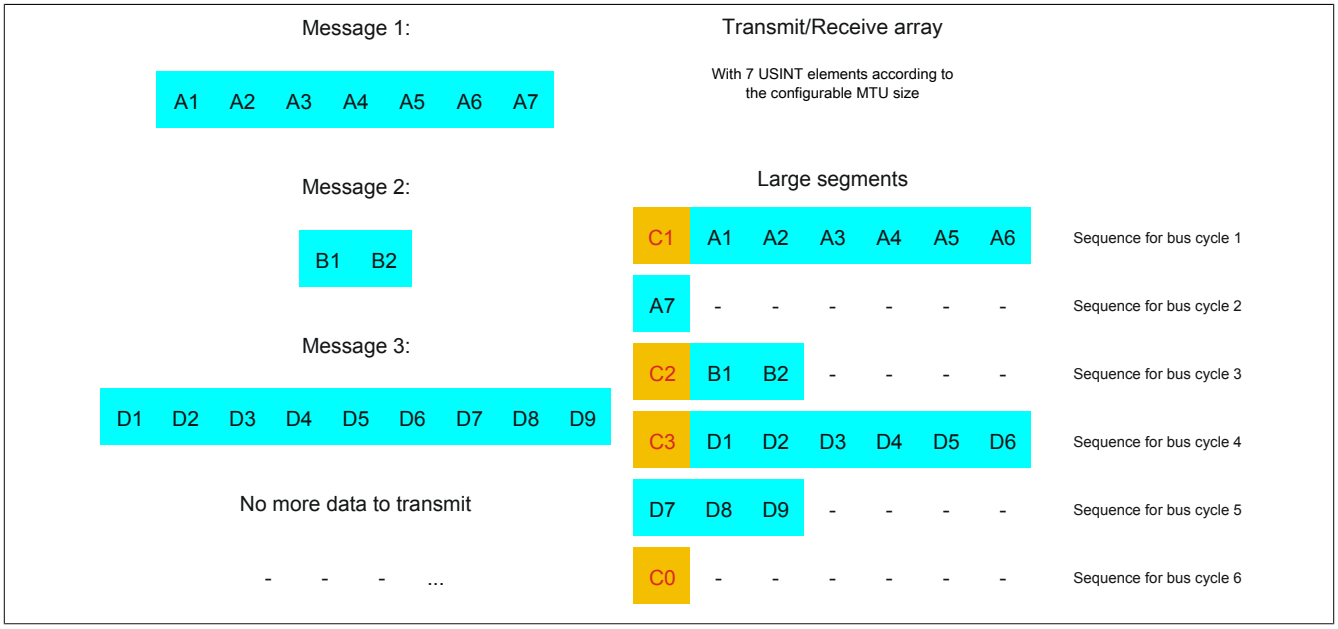


Figure 520: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 653: FlatStream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

Three autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transmission of large segments as well as MultiSegmentMTUs.

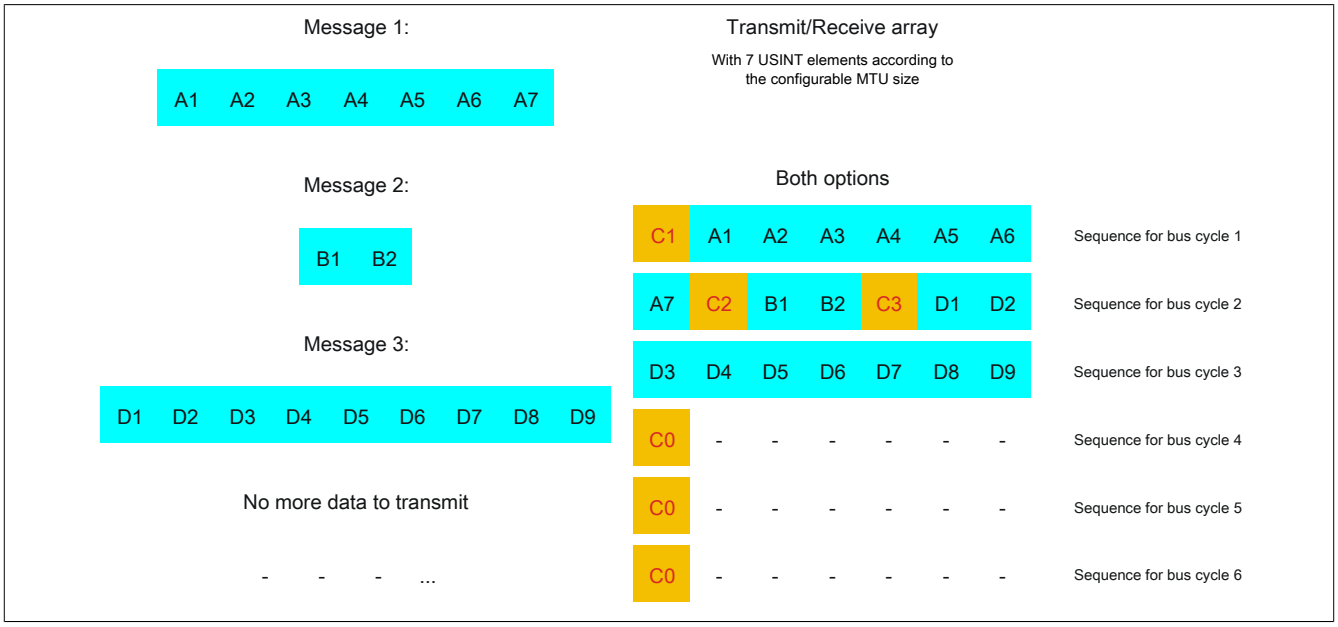


Figure 521: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it can be used for other data in the data stream. The "nextCBPos" bit must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with the "Large segments" option.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)

  ⇨ First segment = Control byte + 7 bytes of data

- Message 2 (2 bytes)

  ⇨ First segment = Control byte + 2 bytes of data

- Message 3 (9 bytes)

  ⇨ First segment = Control byte + 9 bytes of data

- No more messages

  ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 654: FlatStream determination of the control bytes for the large segment and MultiSegmentMTU example

4.26.9.9.13.5 Example of Forward functionality on X2X Link

Forward functionality is a method that can be used to substantially increase the FlatStream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

Operating principle

X2X Link communication cycles through five different steps to transmit a FlatStream sequence. At least five bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase Sequence-Counter	Cyclic matching of MTU and module buffer	Append sequence to receive array Adjust SequenceAck	Cyclic matching of MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipient (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

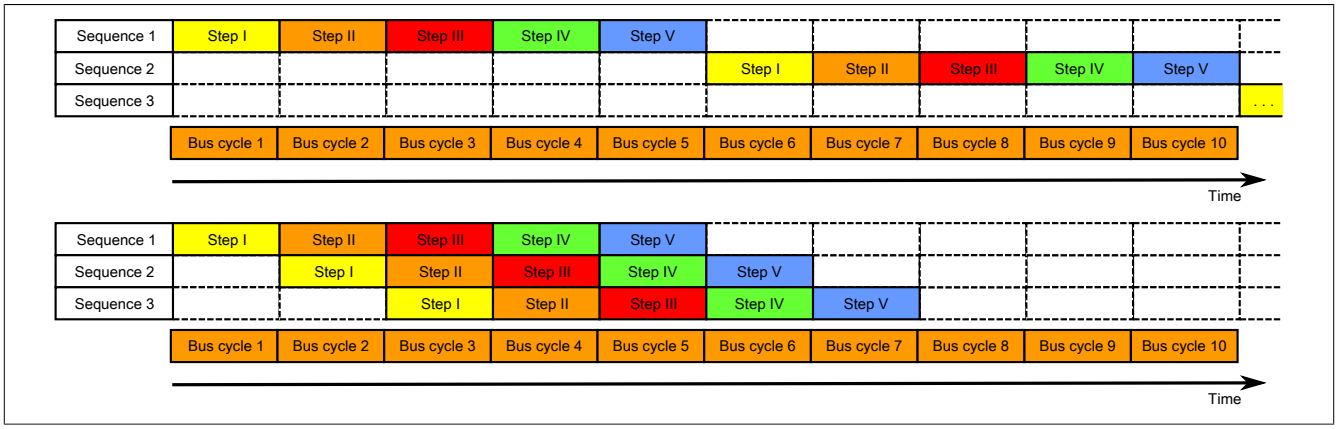


Figure 522: Comparison of transmission without/with Forward

Each of the five steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver still has to acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transmitted successfully.

Configuration

The Forward function only has to be enabled for the input direction. Two additional configuration registers are available for doing so. FlatStream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of the OutputMTU is specified.

Number of unconfirmed sequences

Name:
Forward

With the "Forward" register, the user specifies how many unacknowledged sequences the module is allowed to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Value
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

The "ForwardDelay" register is used to specify the delay time in µs. This is the amount of time the module has to wait after sending a sequence until it is allowed to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Value
UINT	0 to 65,535 [µs] Default: 0

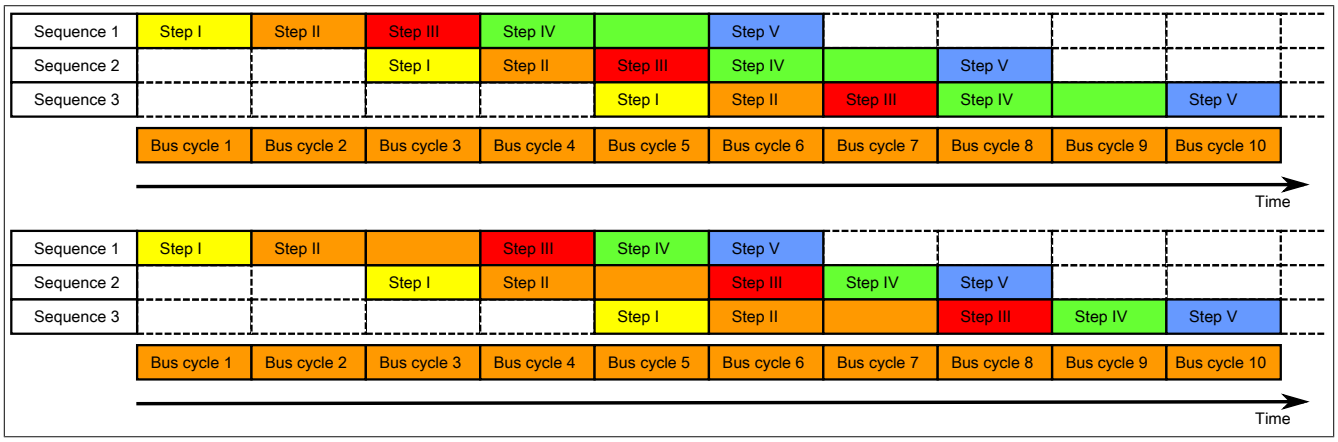


Figure 523: Effect of ForwardDelay when using FlatStream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to seven unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- Module monitors OutputSequenceCounter*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset the OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to the OutputMTU. - The CPU must increase the OutputSequenceCounter for the sequence to be accepted by the module. - The CPU can then *transmit* in the next bus cycle if the MTU has been enabled.
The module respondssince OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array* *- Module acknowledged; current received value of OutputSequenceCounter transferred to OutputSequenceAck* *- The module polls the status once more*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transmitted successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transmission errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of the OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transmission can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value needs to be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor the InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck* *- The module checks InputMTU for enabling* *→Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array*
Action: *- The module transfers the current part of the transmit array to the receive buffer* *- The module increases the InputSequenceCounter* *- The module waits on a new bus cycle after the ForwardDelay time has passed* *- The module repeats the action if InputMTU is enabled*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must accept data from the InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to the InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck is larger than allowed during transmission, then a transmission error has occurred. In this case, all unacknowledged sequences must be repeated with the old SequenceCounter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence has been acknowledged more than once, then a fatal error has occurred. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **This is not an error. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transmitted successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for X2X Link transmissions if this type of interference occurs. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transmitted.

Using Forward functionality with FlatStream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transmitted properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transmitted successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and the SequenceCounter value and/or filled MTU are lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only allowed to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

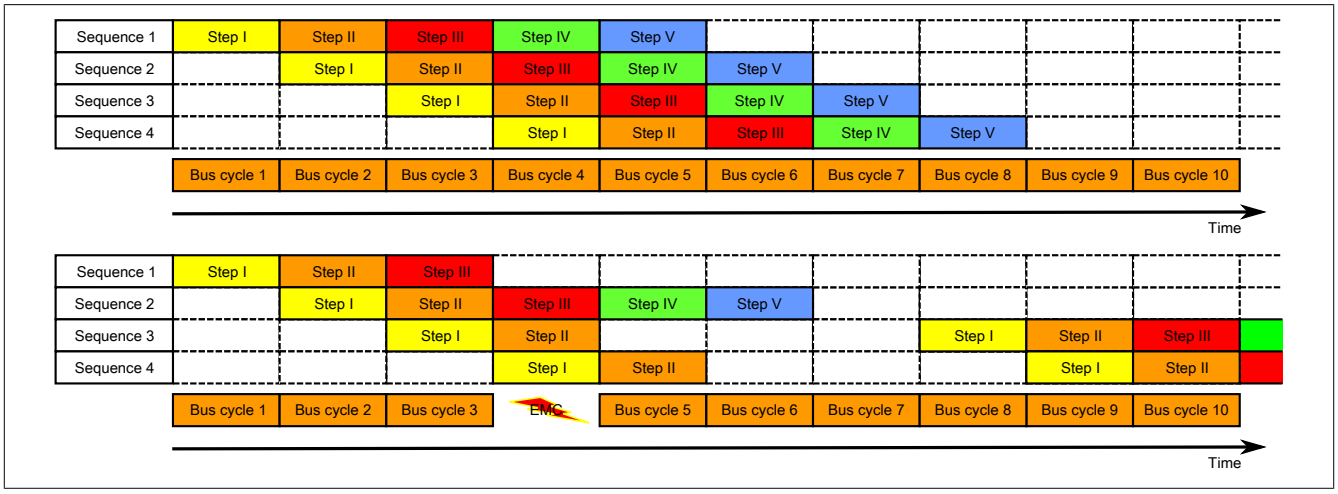


Figure 524: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permitted number of unacknowledged transmissions.
Five bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

4.26.9.9.14 Using IO-Link with FlatStream

With this module, the user has the option of communicating with the connected IO-Link device via FlatStream.

Communication takes place separately with respect to timing, i.e. output data is transferred completely from the CPU to the module and checked. Only then does the module initiate the actual communication with the IO-Link device.

The module acts the same way in the input direction. Messages from the IO-Link device must have been received completely by the X2X module before the FlatStream message is generated and transmitted to the CPU.

4.26.9.9.14.1 General handling of FlatStream

Input/Output sequence	Rx/Tx bytes	
(unchanged)	Control byte (unchanged)	Payload data for FlatStream (IO-Link information)

The user has a choice when using FlatStream.

- Using FlatStream as described in the "FlatStream communication" section
- Using the "AsFltGen" library to manage input/output sequence and FlatStream control bytes automatically

In both cases, a module-specific array with FlatStream payload data must be created in the application.

4.26.9.9.14.2 IO-Link information for the FlatStream

To be able to use IO-Link communication via FlatStream, you must define an individual array in the application.

The following must be defined for the query in the direction CPU → Module → IO-Link device:

- Module's channel number
- Frame number for the query
- Type of query
- The corresponding IO-Link data must then be attached depending on the query.

The response consists of the following parts:

- The frame number, access type and type of query are repeated.
- The module generates the error bit and manages the confirmation bit.
- The successfully received IO-Link information or corresponding error code is then appended.

Module-specific FlatStream array for IO-Link communication

Bytes	Name	Value	Description
1	Channel number	1 to 4	
2	Frame number	0 to 255	This number is repeated in the module's response. This allows the later response from the module to be distinctly attributed to the request.
3	See Byte 3	x	
...	IO-Link data or error code		Depends on byte 3

Byte 3

Bit	Description	Value	Information
0 - 2	Type of query	0	Access to object dictionary
		1	Access to inputs' process data
		2	Access to outputs' process data
		3	Read individual event
		4	Read multiple events
		5	Enable event forwarding
		6	Disable event forwarding
		7	Announcement of automatically forwarded event
3 - 4	Reserved	-	
5	Confirm	0	Message without query
		1	Response to query[1)]
6	Status bit (for response frame)	0	No error
		1	Error
7	Access types	0	Read
		1	Write

1) This confirmation bit is additionally set with the response to a query. The response for confirming a query frequently contains additional data that must be processed.

4.26.9.9.14.3 IO-Link data

Depending on the type of query, different IO-Link data results that must be appended to the FlatStream array.

Access to object dictionary

Request

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4	High index number	0 to 255	Index of the desired IO-Link parameter
5	Low index number	0 to 255	
6	Subindex number	0 to 255	Subindex of the IO-Link parameter
7 to ...	Data	0 to 255	Optional, for write operation

Response

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4 to ...	Data / Error code	0 to 255	Omitted if data has been written successfully

Accessing process data

Request

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4	Data	0 to 255	Optional, for write operation

Response

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4	Data / Error code	0 to 255	Omitted if data has been written successfully

Accessing event data

Request

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		

Response

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4	Event counter - Current	Bit 0 to 3	Number of attached events
	Event counter - Pending	Bit 4 to 7	Number of pending events
5	Event 0 – Event qualifier	0 to 255	See EventQualifier.
6	Event 0 – High event data	0 to 255	
7	Event 0 – Low event data	0 to 255	
8 - 10	Event 1		
x to (x + 2)	Event n[1)]		

1) Applies only if multiple events were queried with byte 3 (bits 0 to 2 = 4). Only 1 event comes with byte 3 (bits 0 to 2 = 3).

or

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4	Error code	0 to 255	

Enable/Disable event forwarding

Request

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		

Response

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		

or

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4	Error code	0 to 255	

Announcement of forwarded event

After enabling event forwarding, events no longer have to be queried cyclically. The module generates the event as soon as the corresponding event occurs.

Message

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4	Event counter - Current	Bit 0 to 3	Number of attached events
	Event counter - Pending	Bit 4 to 7	Number of pending events
5	Event 0 – Event qualifier	0 to 255	See EventQualifier.
6	Event 0 – High event data	0 to 255	
7	Event 0 – Low event data	0 to 255	
8 - 10	Event 1		
x to (x + 2)	Event n[1)]		

1) Applies only if multiple events were queried with byte 3 (bits 0 to 2 = 4). Only 1 event comes with byte 3 (bits 0 to 2 = 3).

or

Bytes	Name	Value	Description
1 to 3	Module-specific FlatStream array for IO-Link communication		
4	Error code	0 to 255	

4.26.9.9.15 Error codes

Queries can be made via registers or FlatStream. If a query fails, the error bit is set and an error code generated. In addition to general error codes, vendor-specific error codes can also occur. Information about these can be found in the operating instructions for the corresponding IO-Link device.

Error indicators in the registers

- The error bit is set in ParameterCtrIn, whereas the length of the error code is indicated in the data length parameter.
- ParameterDataIn contains the error code.

Error indicators in FlatStream

If the error bit is set, the FlatStream bytes are put together as follows:

- Bytes 1 to 3: Module-specific FlatStream array
- Byte 4: Error code; if 8 (error reported by device), bytes 5 and 6 will include additional information.
- Bytes 5 and 6: Error code from IO-Link device
- ...

Error codes

Code	Function
1	No device on this channel
2	IO-Link disabled
3	Communication error with device
4	Query buffer full
5	Event queue empty
6	Query not supported
7	Object access failed
8	Object access, error reported by device
9	Incorrect channel number
10	Write operation not possible
11	No input data available
12	Frame too short
13	One or more events discarded
14	Device has no input data
15	Device has no output data

4.26.9.9.16 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without IO-Link (all channels in SIO-Modus)	≥200 µs
With IO-Link	≥400 µs

4.26.9.9.17 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without IO-Link (all channels in SIO-Modus)	≥200 µs
With IO-Link	≥400 µs (depends on the minimum IO-Link cycle time of the IO-Link device)

4.26.10 X20PD0011

4.26.10.1 General information

The potential distributor module provides 12x ground (from the internal I/O supply) on the terminal connections and opens up additional wiring possibilities for actuators and sensors. The module is equipped with a replaceable microfuse between the GND potential on the terminal block and the X20 system I/O supply. The function of the fuse is monitored.

- Integrated exchangeable microfuse
- Monitoring of the fuse
- Potential for routing as needed

Information:

The wired load must be supplied with 24 VDC!

4.26.10.2 Order data

Model number	Short description	Figure
	Other functions	
X20PD0011	X20 potential distributor module, 12x GND, integrated microfuse	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 655: X20PD0011 - Order data

4.26.10.3 Technical data

Product ID	X20PD0011
Short description	
Potential distributor module	12x ground on the terminal connections
General information	
B&R ID code	0x267D
Status indicators	Operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Fuse monitoring	Yes, using status LED and software
Power consumption [1]	
Bus	0.12 W
Internal I/O	-
External I/O	1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Output I/O supply	
Rated output voltage	Ground from the internal I/O supply
Fuse	Integrated 6.3 A, slow-blow, can be replaced
Behavior if a short circuit occurs	Integrated fuse
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 656: X20PD0011 - Technical data

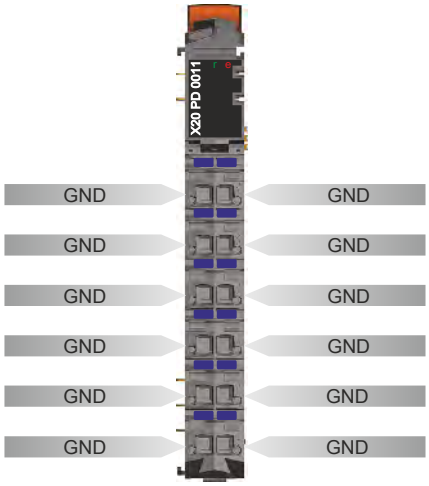
1) The specified values are maximum values. The exact calculation is available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.26.10.4 LED status indicators

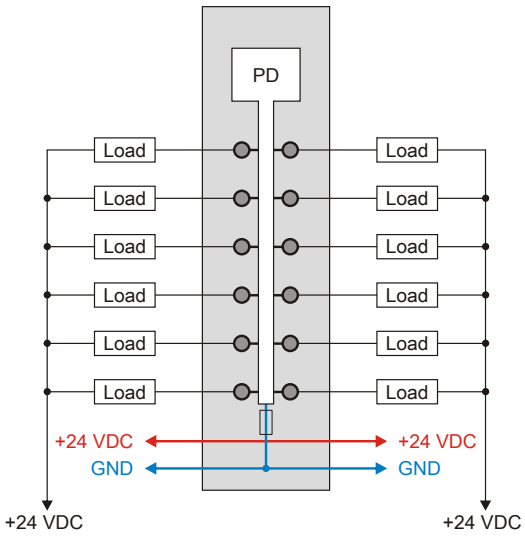
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Fuse defective or missing
	e + r	Red on / Green single flash		Invalid firmware

4.26.10.5 Pinout



4.26.10.6 Connection example



4.26.10.7 Register description

4.26.10.7.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.10.7.2 Function model 1 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	1	Module status	USINT	•			
		StatusFuse	Bit 0				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Non-cyclic access continues to be based on the register numbers.

4.26.10.7.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	USINT	•			
		StatusFuse	Bit 0				

1) The offset specifies the position of the register within the CAN object.

4.26.10.7.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.26.10.7.4 Module status

Name:
Module status
StatusFuse

This register can be used to read the status of the installed fuse.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusFuse	0	Fuse OK
		1	Fuse not OK
1 - 7	Reserved	-	

4.26.10.7.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.26.10.7.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
100 µs

4.26.11 X20PD0012

4.26.11.1 General information

The potential distributor module provides 12x 24 VDC (from the internal I/O supply) on the terminal connections and opens up additional wiring possibilities for actuators and sensors. The module is equipped with a replaceable microfuse between the 24 VDC potential on the terminal block and the X20 system I/O supply. The function of the fuse is monitored.

- Integrated exchangeable microfuse
- Monitoring of the fuse
- Potential for routing as needed

4.26.11.2 Order data

Model number	Short description	Figure
	Other functions	
X20PD0012	X20 potential distributor module, 12x 24 VDC, integrated micro-fuse	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 657: X20PD0012 - Order data

4.26.11.3 Technical data

Product ID	X20PD0012
Short description	
Potential distributor module	12x 24 VDC on the terminal connections
General information	
B&R ID code	0x267E
Status indicators	Operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Fuse monitoring	Yes, using status LED and software
Power consumption [1]	
Bus	0.12 W
Internal I/O	1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Output I/O supply	
Rated output voltage	24 VDC from the internal I/O supply
Fuse	Integrated 6.3 A, slow-blow, can be replaced
Behavior if a short circuit occurs	Integrated fuse
Permitted contact load	10 A
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 658: X20PD0012 - Technical data

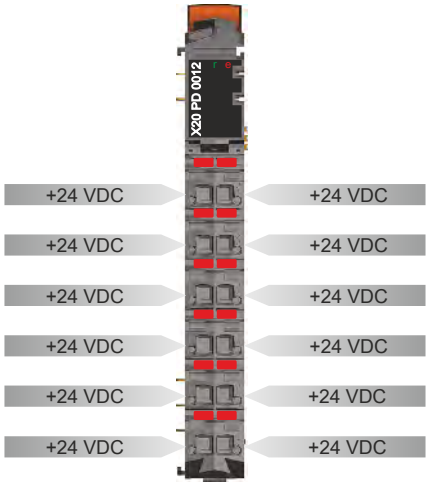
1) The specified values are maximum values. The exact calculation is available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.26.11.4 LED status indicators

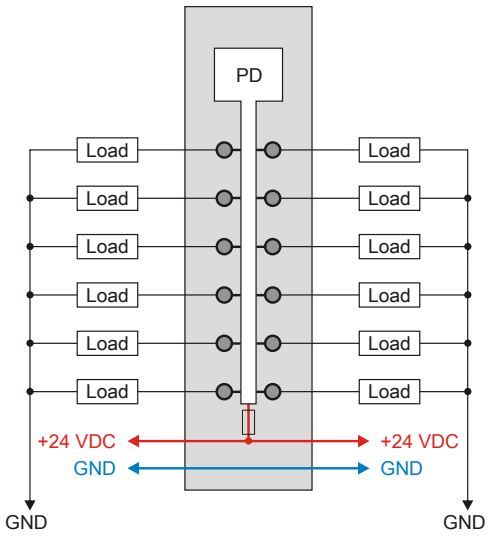
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Fuse defective or missing
	e + r	Red on / Green single flash		Invalid firmware

4.26.11.5 Pinout



4.26.11.6 Connection example



4.26.11.7 Register description

4.26.11.7.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.11.7.2 Function model 1 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	1	Module status	USINT	•			
		StatusFuse	Bit 0				

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Non-cyclic access continues to be based on the register numbers.

4.26.11.7.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	USINT	•			
		StatusFuse	Bit 0				

1) The offset specifies the position of the register within the CAN object.

4.26.11.7.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.26.11.7.4 Module status

Name:
Module status
StatusFuse

This register can be used to read the status of the installed fuse.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusFuse	0	Fuse OK
		1	Fuse not OK
1 - 7	Reserved	-	

4.26.11.7.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.26.11.7.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
100 µs

4.26.12 X20PD0016

4.26.12.1 General information

The potential distributor module provides 5x 24 VDC and 5x ground connections (from an external supply) at the terminals. There is no connection to the internal I/O supply, so this module only serves to distribute an external supply for the load and electronics supply. The externally fed 24 VDC supply is provided on the terminal connections through a replaceable microfuse. The 24 VDC feed and the functionality of the fuse are monitored.

- Integrated exchangeable microfuse
- Monitoring of the fuse
- Potential for routing as needed
- Distribution of the load and electronics supply
- Isolation from the internal I/O supply

4.26.12.2 Order data

Model number	Short description	Figure
	Other functions	
X20PD0016	X20 potential distributor module, 5x GND, 5x 24 VDC, each with 1x floating feed, integrated microfuse	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 659: X20PD0016 - Order data

4.26.12.3 Technical data

Product ID	X20PD0016
Short description	
Potential distributor module	5x 24 VDC on the terminal connections, 5x ground on the terminal connections
General information	
B&R ID code	0x2680
Status indicators	Operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Fuse monitoring	Yes, using status LED and software
Power consumption [1]	
Bus	0.12 W
Internal I/O	-
External I/O	1.15 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [2]	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Input supply	
Nominal input voltage	24 VDC -15% / +20% external, external ground
Fuse	Integrated 6.3 A, slow-blow, can be replaced
Reverse polarity protection	No
Output supply	
Rated output voltage	24 VDC, ground
Permitted contact load	10 A
Behavior if a short circuit occurs	
On the 24 VDC supply	Integrated fuse
On the GND connection	No protection available
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 660: X20PD0016 - Technical data

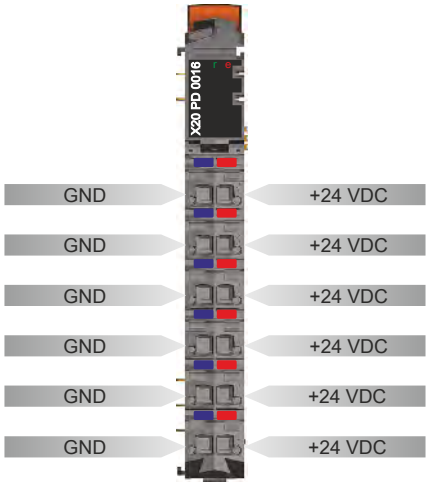
1) The specified values are maximum values. The exact calculation is available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.26.12.4 LED status indicators

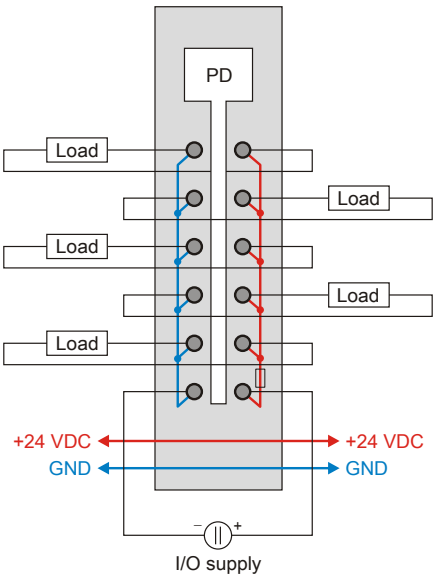
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Fuse defective or missing
			Double flash	Supply voltage too low
	e + r	Red on / Green single flash		Invalid firmware

4.26.12.5 Pinout



4.26.12.6 Connection example



4.26.12.7 Register description

4.26.12.7.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.12.7.2 Function model 1 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	1	Module status	USINT	•			
		StatusFuse	Bit 0				
		StatusPowerSupply	Bit 1				
2	2	Counter01	USINT	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Non-cyclic access continues to be based on the register numbers.

4.26.12.7.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	USINT	•			
		StatusFuse	Bit 0				
		StatusPowerSupply	Bit 1				
2	2	Counter01	USINT	•			

1) The offset specifies the position of the register within the CAN object.

4.26.12.7.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.26.12.7.4 Module status

Name:
Module status
StatusFuse
StatusPowerSupply

This register can be used to read the status of the power supply.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusFuse	0	Fuse OK
		1	Fuse not OK
	StatusPowerSupply	0	Level of fed voltage OK
		1	Level of fed voltage not OK
2 - 7	Reserved	-	

4.26.12.7.5 Counter for the voltage dips

Name:
Counter01

This register is used to count how often the voltage dips on the PD module.

Data type	Value
USINT	0 to 255

4.26.12.7.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.26.12.7.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
100 µs

4.26.13 X20(c)PD2113

4.26.13.1 General information

The potential distributor module with feed can provide 6x 24 VDC and 6x ground connections from the internal I/O supply on the terminals. This module can also be used instead of a special feed module for the internal I/O supply. The internal 24 VDC supply is connected to the terminal connections through a replaceable microfuse for protection. The 24 VDC feed and the functionality of the fuse are monitored.

Information:

Since the 6x 24 VDC terminals are interconnected and the fuse is located between the terminals and the internal I/O supply, the terminal potentials are not protected against short circuits from an external feed. If using an external feed, the respective 24 VDC terminals must be protected with an external fuse. In this case a X20BM01 bus module should be used.

- Integrated exchangeable microfuse
- Monitoring of the fuse
- Potential for routing as needed
- Can be used as feed module for the I/O supply

4.26.13.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.26.13.3 Order data

Model number	Short description	Figure
	Other functions	
X20PD2113	X20 potential distributor module, 6x GND, 6x 24 VDC, with feed option, integrated microfuse	
X20cPD2113	X20 potential distributor, coated, 6x GND, 6x 24 VDC, with supply option, integrated microfuse	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 661: X20PD2113, X20cPD2113 - Order data

4.26.13.4 Technical data

Product ID	X20PD2113	X20cPD2113
Short description		
Potential distributor module with feed	6x 24 VDC on the terminal connections, 6x ground on the terminal connections	
General information		
B&R ID code	0x267F	0xE23B
Status indicators	Operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Fuse monitoring	Yes, using status LED and software	
Power consumption [1]		
Bus	0.12 W	
Internal I/O	-	
External I/O	1.15 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GL	Yes	
GOST-R	Yes	
Input supply with feed		
Nominal input voltage	24 VDC -15% / +20% external, external ground	
Input current	Max. 6 A	
Fuse	Integrated 6.3 A, slow-blow, can be replaced	
Behavior if a short circuit occurs	No protection available Use external fuse	
Reverse polarity protection	No	
Output I/O supply		
Rated output voltage	24 VDC, ground	
Permitted contact load	6 A	
Behavior if a short circuit occurs		
On the 24 VDC supply	Integrated fuse	
On the GND connection	No protection available	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM01 or X20B-M11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM01 or X20cB-M11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 662: X20PD2113, X20cPD2113 - Technical data

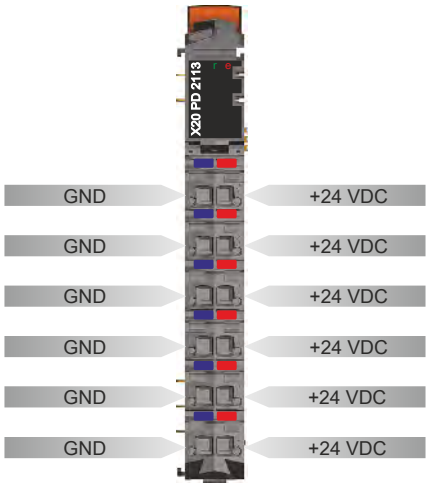
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.26.13.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

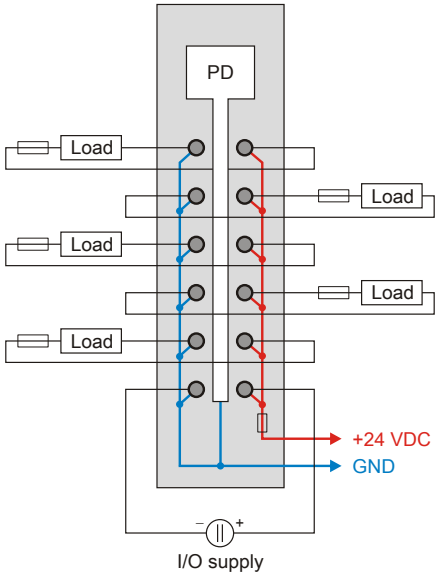
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Fuse defective or missing
			Double flash	Supply voltage too low
			Triple flash	Internal I/O supply OK but fuse defective and supply voltage too low
	e + r	Red on / Green single flash		Invalid firmware

4.26.13.6 Pinout

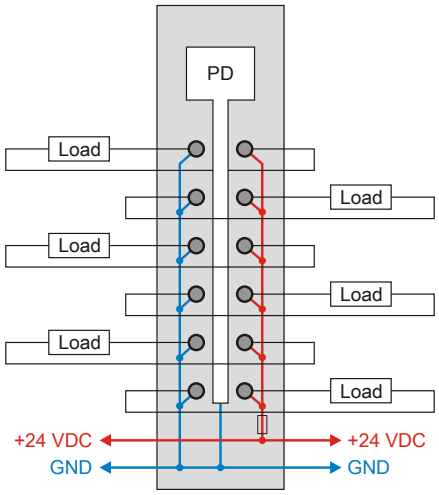


4.26.13.7 Connection examples

Connection example with external supply



Connection example with internal supply



4.26.13.8 Register description

4.26.13.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.13.8.2 Function model 1 - Standard

Register	Fixed offset	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	1	Module status	USINT	•			
		StatusFuse	Bit 0				
		StatusPowerSupply	Bit 1				
2	2	Counter01	USINT	•			

Fixed modules require their data points to be in a specific order in the X2X frame. Cyclic access occurs according to a predefined offset, not based on the register address.

Non-cyclic access continues to be based on the register numbers.

4.26.13.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	USINT	•			
		StatusFuse	Bit 0				
		StatusPowerSupply	Bit 1				
2	2	Counter01	USINT	•			

1) The offset specifies the position of the register within the CAN object.

4.26.13.8.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.26.13.8.4 Module status

Name:
Module status
StatusFuse
StatusPowerSupply

This register can be used to read the status of the power supply.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	StatusFuse	0	Fuse OK
		1	Fuse not OK
	StatusPowerSupply	0	Level of fed voltage OK
		1	Level of fed voltage not OK
2 - 7	Reserved	-	

4.26.13.8.5 Counter for the voltage dips

Name:
Counter01

This register is used to count how often the voltage dips on the PD module.

Data type	Value
USINT	0 to 255

4.26.13.8.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.26.13.8.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
100 µs

4.26.14 X20PS4951

4.26.14.1 General information

In order to connect potentiometers, modules must first be supplied with the appropriate voltage. The potentiometer supply module can be used to supply four potentiometers with ±10 V. The data is evaluated using standard analog input modules.

- Open circuit and short circuit detection
- Simple implementation of potentiometer inputs
- 4x supply

4.26.14.2 Order data

Model number	Short description	Figure
	Other functions	
X20PS4951	X20 power supply module, for potentiometers, 4x ±10 V for potentiometer supply	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 663: X20PS4951 - Order data

4.26.14.3 Technical data

Product ID	X20PS4951
Short description	
System module	Supplies 4 potentiometers with ±10 V
General information	
B&R ID code	0x1F43
Status indicators	Potentiometer supply monitoring by channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Open line	Yes, using status LED and software
Overload	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.8 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 1)	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Potentiometer supply	
Number of supplies	4
Voltage	±10 V
Potentiometer resistance	1 kΩ to 10 kΩ
Load	Max. 20 mA per supply channel
Short circuit protection	Yes
Basic accuracy	
+10 V	±0.12% at 25°C
-10 V	±0.21% at 25°C
20 V	±0.165% at 25°C
Isolation voltage between channel and bus	500 V_{eff}
Max. drift	
+10 V	±0.00012%/°C
-10 V	±0.00032%/°C
20 V	±0.00022%/°C
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	Values derated when mounted vertically
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 664: X20PS4951 - Technical data

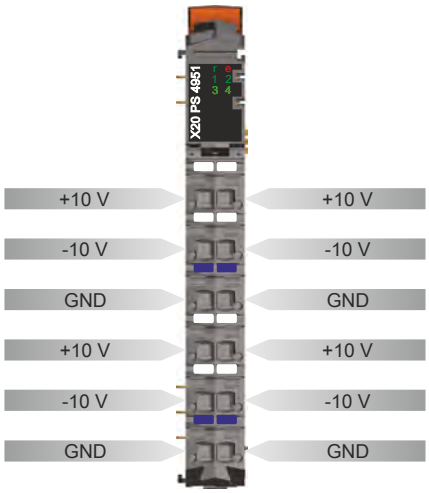
1) Ta min.: 0°C
Ta max.: See environmental conditions

4.26.14.4 LED status indicators

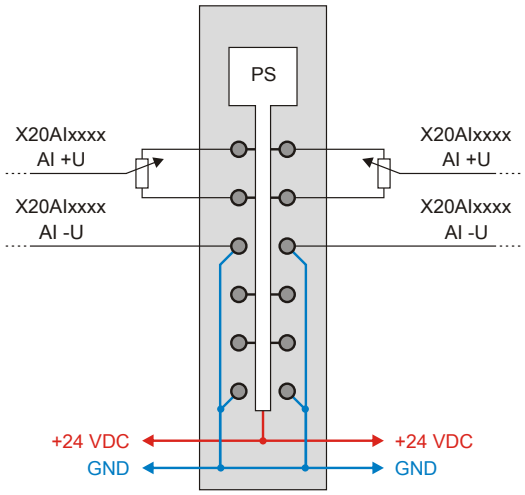
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	At least one supply channel overloaded
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Off	No power to module or open line
			Blinking	Overload: Output is off
			On	There is a load on the output, normal operation

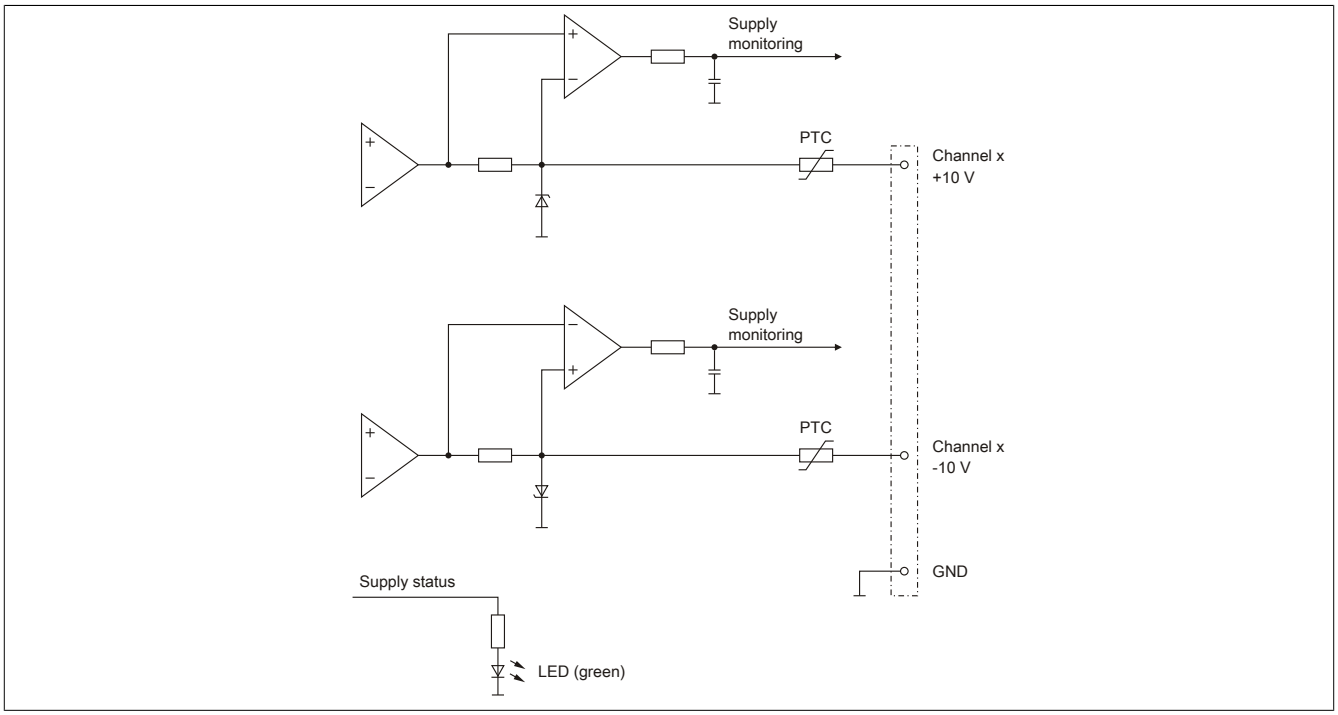
4.26.14.5 Pinout



4.26.14.6 Connection example



4.26.14.7 Output circuit diagram



4.26.14.8 Register description

4.26.14.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.26.14.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Supply status	USINT	•			
	ShortCircuit01	Bit 0				
	...	...				
	ShortCircuit01	Bit 3				
	OpenLine01	Bit 4				
	...	...				
	OpenLine04	Bit 7				

4.26.14.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Supply status	USINT	•			
		ShortCircuit01	Bit 0				
		...	...				
		ShortCircuit01	Bit 3				
		OpenLine01	Bit 4				
		...	...				
		OpenLine04	Bit 7				

1) The offset specifies the position of the register within the CAN object.

4.26.14.8.3.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O.

4.26.14.8.4 Supply status

Name:
OpenLine01 to OpenLine04
ShortCircuit01 to ShortCircuit04

This register can be used to display the status of the respective channels.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	ShortCircuit01	0	No short circuit
		1	Short circuit on channel 1
...		...	
3	ShortCircuit04	0	No short circuit
		1	Short circuit on channel 4
4	OpenLine01	0	No open line
		1	Open line on channel 1
...		...	
7	OpenLine04	0	No open line
		1	Open line on channel 4

4.26.14.8.5 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.26.14.8.6 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 ms

4.27 Power supply modules

The internal I/Os and the X2X Link are fed by the supply modules.

4.27.1 Brief information

Product ID	Short description	on page
X20PS2100	X20 power supply module, for internal I/O supply	2884
X20PS2110	X20 supply module, for internal I/O supply, integrated microfuse	2889
X20PS3300	X20 power supply module, for X2X Link and internal I/O supply	2900
X20cPS2100	X20 power supply module, coated, for internal I/O supply	2884
X20cPS2110	X20 power supply module, coated, for internal I/O supply, integrated microfuse	2889
X20cPS3300	X20 power supply module, coated, for X2X Link and internal I/O supply	2900

4.27.2 X20(c)PS2100

4.27.2.1 General information

The supply module is used for the internal I/O supply.

- 24 VDC supply module for internal I/O supply

4.27.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.27.2.3 Order data

Model number	Short description	Figure
	Power supplies	
X20PS2100	X20 power supply module, for internal I/O supply	
X20cPS2100	X20 power supply module, coated, for internal I/O supply	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20BM05	X20 power supply bus module, with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 665: X20PS2100, X20cPS2100 - Order data

4.27.2.4 Technical data

Product ID	X20PS2100	X20cPS2100
Short description		
Power supply module	24 VDC supply module for internal I/O supply	
General information		
B&R ID code	0x1BBF	0xE23C
Status indicators	Operating state, module status	
Diagnostics Module run/error	 Yes, using status LED and software	
Power consumption [1] Bus Internal I/O	 0.2 W 0.6 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation I/O feed - I/O supply	 No	
Certification CE cULus cCSAus HazLoc Class 1 Division 2 ATEX Zone 2 [2] KC GL LR GOST-R	 Yes Yes Yes Yes Yes Yes Yes Yes	 - - - - - - -
Input I/O supply		
Input voltage	24 VDC -15 % / +20 %	
Fuse	Required line fuse: Max. 10 A, slow-blow	
Reverse polarity protection	No	
Output I/O supply		
Rated output voltage	24 VDC	
Behavior if a short circuit occurs	Required line fuse	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation Horizontal Vertical	 Yes Yes	
Installation at elevations above sea level 0 to 2000 m >2000 m	 No limitations Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature Operation Horizontal installation Vertical installation Derating Storage Transport	 -25 to 60°C -25 to 50°C - -40 to 85°C -40 to 85°C	
Relative humidity Operation Storage Transport	 5 to 95%, non-condensing 5 to 95%, non-condensing 5 to 95%, non-condensing	 Up to 100%, condensing
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM01 supply bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM01 supply bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 666: X20PS2100, X20cPS2100 - Technical data

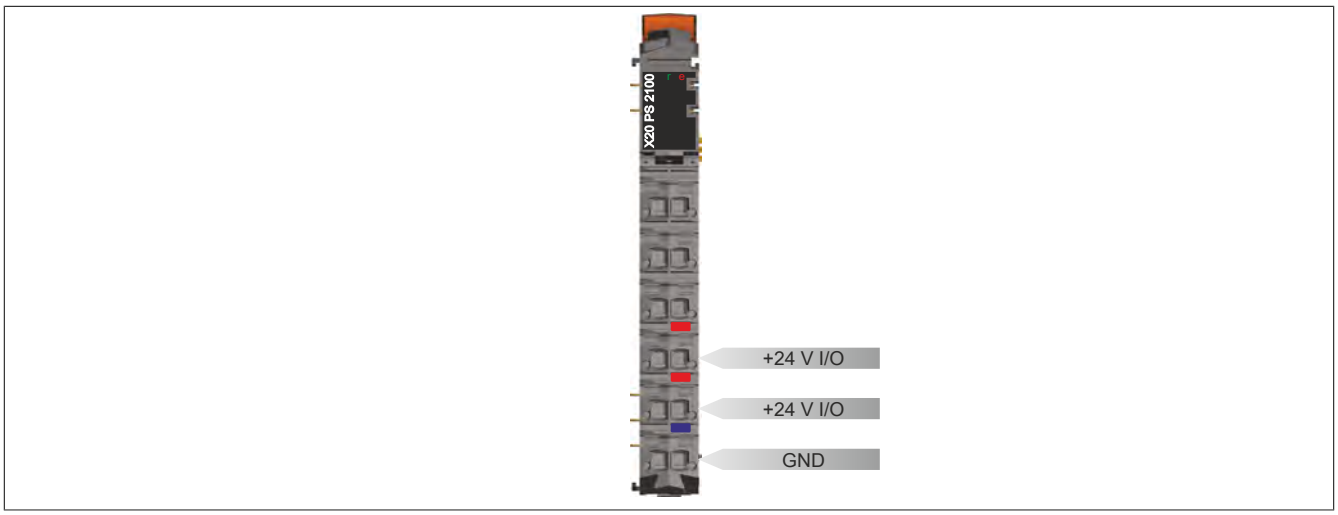
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.27.2.5 LED status indicators

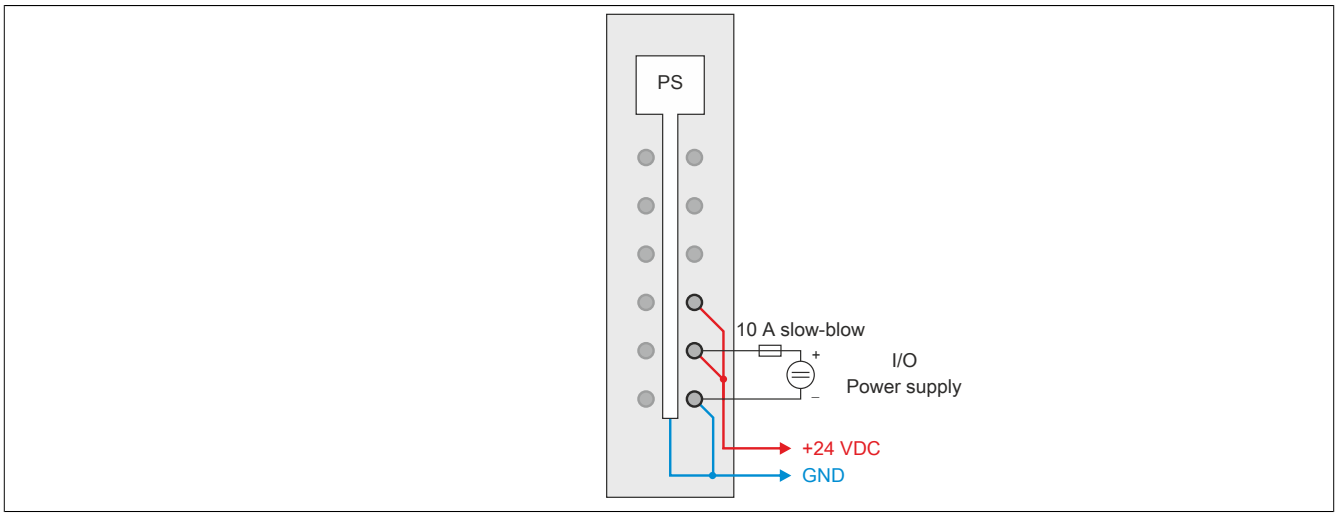
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • I/O supply too low • X2X link voltage too low
	e + r	Red on / Green single flash		Invalid firmware

4.27.2.6 Pinout



4.27.2.7 Connection example



4.27.2.8 Shutting the potential group down safely

In safety-related applications, it must be guaranteed that the potential group is safely shutdown in order to achieve category 4 shutdown in accordance with ISO 13849. An X20PS2100 (rev.F0 or higher) or X20PS2110 (rev.C0 or higher) supply module must be used to do this.

Important notes on "Safe shutdown" are listed in the X20 system user's manual, section"Mechanical and electrical configuration", section "Safe shutdown". The user's manual is available in the Downloads section of the B&R website (www.br-automation.com).

4.27.2.9 Register description

4.27.2.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.27.2.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
4	SupplyVoltage	USINT	•			

4.27.2.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 2				
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.27.2.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.27.2.9.4 Module status

Name:
Module status

The following module supply voltages are monitored in this register:

Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Bus supply warning - Undervoltage (<4.7V)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.27.2.9.5 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.27.2.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.27.2.9.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.27.3 X20(c)PS2110

4.27.3.1 General information

The supply module is used for the internal I/O supply. The module has an integrated replaceable fuse for the I/O supply.

- 24 VDC supply module for internal I/O supply
- Fuse for I/O supply integrated in module

4.27.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.27.3.3 Order data

Model number	Short description	Figure
	Power supplies	
X20PS2110	X20 supply module, for internal I/O supply, integrated microfuse	
X20cPS2110	X20 power supply module, coated, for internal I/O supply, integrated microfuse	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20BM05	X20 power supply bus module, with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 667: X20PS2110, X20cPS2110 - Order data

4.27.3.4 Technical data

Product ID	X20PS2110	X20cPS2110
Short description		
Power supply module	24 VDC supply module for internal I/O supply	
General information		
B&R ID code	0x2016	0xE23D
Status indicators	Operating state, module status	
Diagnostics Module run/error	 Yes, using status LED and software	
Power consumption [1] Bus Internal I/O	 0.2 W 0.82 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation I/O feed - I/O supply	 No	
Certification CE cULus cCSAus HazLoc Class 1 Division 2 ATEX Zone 2 [2] KC GOST-R	 Yes Yes Yes Yes Yes Yes	 - -
Input I/O supply		
Input voltage	24 VDC -15 % / +20 %	
Input current	Max. 6 A	
Fuse	Integrated 6.3 A, slow-blow, can be replaced	
Reverse polarity protection	No	
Output I/O supply		
Rated output voltage	24 VDC	
Behavior if a short circuit occurs	Integrated fuse	
Permitted contact load	6 A	
Operating conditions		
Mounting orientation Horizontal Vertical	 Yes Yes	
Installation at elevations above sea level 0 to 2000 m >2000 m	 No limitations Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature Operation Horizontal installation Vertical installation Derating Storage Transport	 -25 to 60°C -25 to 50°C - -40 to 85°C -40 to 85°C	
Relative humidity Operation Storage Transport	 5 to 95%, non-condensing 5 to 95%, non-condensing 5 to 95%, non-condensing	 Up to 100%, condensing
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM01 supply bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM01 supply bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 668: X20PS2110, X20cPS2110 - Technical data

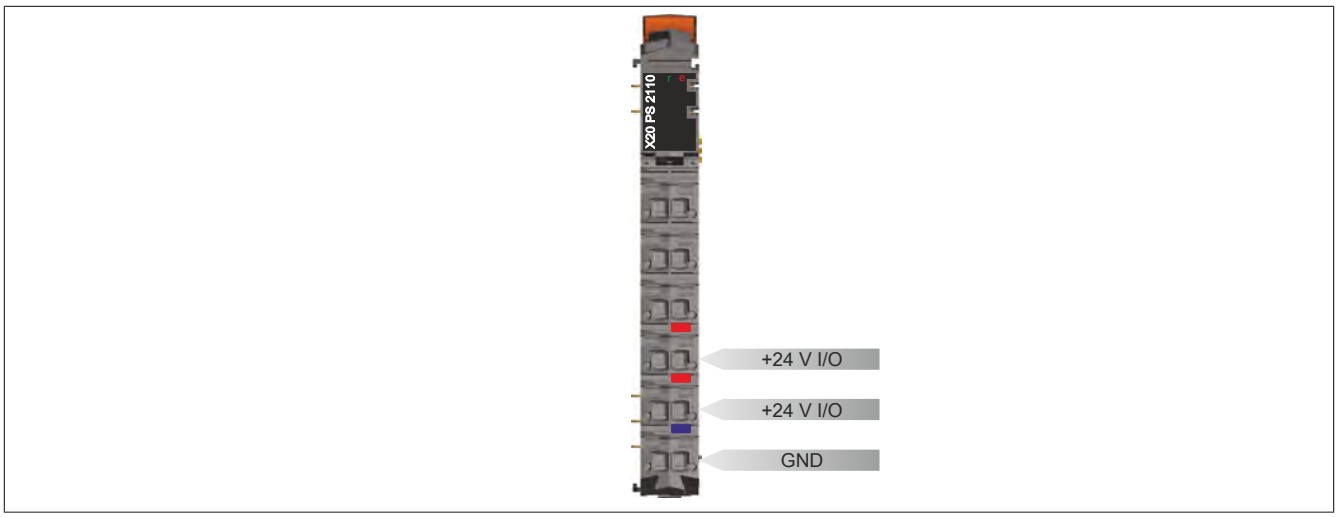
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

4.27.3.5 LED status indicators

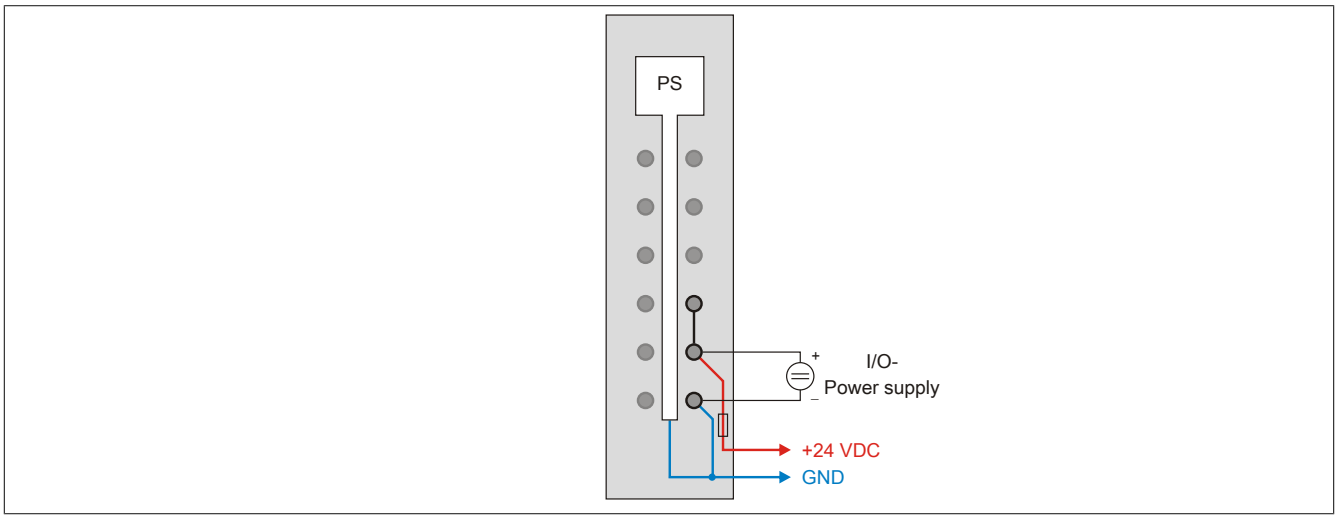
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • I/O supply too low • X2X Link voltage too low
	e + r	Red on / Green single flash		Invalid firmware

4.27.3.6 Pinout



4.27.3.7 Connection example



4.27.3.8 Shutting the potential group down safely

In safety-related applications, it must be guaranteed that the potential group is safely shutdown in order to achieve category 4 shutdown in accordance with ISO 13849. An X20PS2100 (rev.F0 or higher) or X20PS2110 (rev.C0 or higher) supply module must be used to do this.

Important notes on "Safe shutdown" are listed in the X20 system user's manual, section"Mechanical and electrical configuration", section "Safe shutdown". The user's manual is available in the Downloads section of the B&R website (www.br-automation.com).

4.27.3.9 Register description

4.27.3.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.27.3.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 1				
	StatusInput03	Bit 2				
4	SupplyVoltage	USINT	•			

4.27.3.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 1				
		StatusInput03	Bit 2				
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.27.3.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.27.3.9.4 Module status

Name:
Module status

The following module supply voltages are monitored in this register:

Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.
Fuse status:	Applies for hardware revision C0 and later. When using modules C0, a defective fuse is not detected.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Bus supply warning - Undervoltage (<4.7V)
1	StatusInput02	0	Fuse OK or hardware revision <C0
		1	Fuse defective
2	StatusInput03	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.27.3.9.5 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.27.3.9.6 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.27.3.9.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.27.4 X20(c)PS3300

4.27.4.1 General information

The supply module is equipped with a feed for the X2X Link as well as the internal I/O supply.

- Feed for X2X Link and internal I/O supply
- Electrical isolation of feed and X2X Link supply
- Redundancy of X2X Link supply possible by operating multiple supply modules simultaneously

4.27.4.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.27.4.3 Order data

Model number	Short description	Figure
	Power supplies	
X20PS3300	X20 power supply module, for X2X Link and internal I/O supply	
X20cPS3300	X20 power supply module, coated, for X2X Link and internal I/O supply	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20BM05	X20 power supply bus module, with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 669: X20PS3300, X20cPS3300 - Order data

4.27.4.4 Technical data

Product ID	X20PS3300	X20cPS3300
Short description		
Power supply module	24 VDC supply module for I/O and bus	
General information		
B&R ID code	0x1BC0	0xDF13
Status indicators	Overload, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Overload	Yes, using status LED and software	
Power consumption [1]		
Bus	1.31 W	
Internal I/O	0.6 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
I/O feed - I/O supply	No	
X2X Link feed - X2X Link supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
X2X Link input supply		
Input voltage	24 VDC -15 % / +20 %	
Input current	Max. 0.7 A	
Fuse	Integrated, cannot be replaced	
Reverse polarity protection	Yes	
X2X Link supply output		
Nominal output power	7 W	
Parallel operation	Yes [3]	
Redundant operation	Yes	
Overload behavior	Short circuit / temporary overload protection	
Input I/O supply		
Input voltage	24 VDC -15 % / +20 %	
Fuse	Required line fuse: Max. 10 A, slow-blow	
Reverse polarity protection	No	
Output I/O supply		
Rated output voltage	24 VDC	
Behavior if a short circuit occurs	Required line fuse	
Permitted contact load	10 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	

Table 670: X20PS3300, X20cPS3300 - Technical data

Product ID	X20PS3300	X20cPS3300
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM01 supply bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM01 supply bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 670: X20PS3300, X20cPS3300 - Technical data

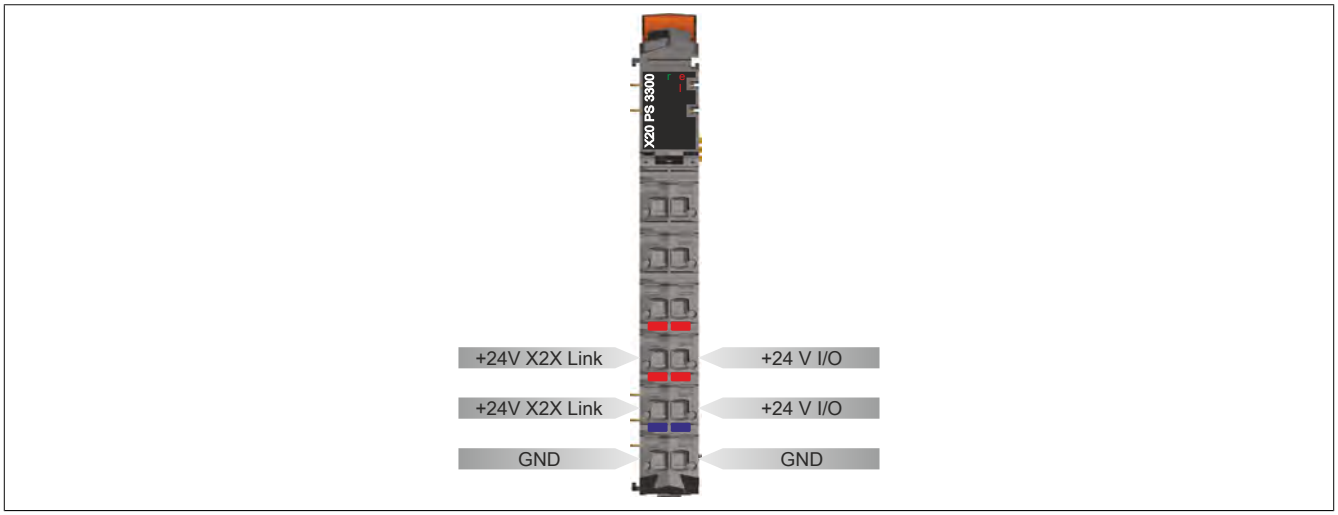
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
   Ta max.: See environmental conditions
3) In parallel operation, only 75% of the rated power can be assumed. It is important to make sure that all power supplies operated in parallel are switched on and off at the same time.

4.27.4.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

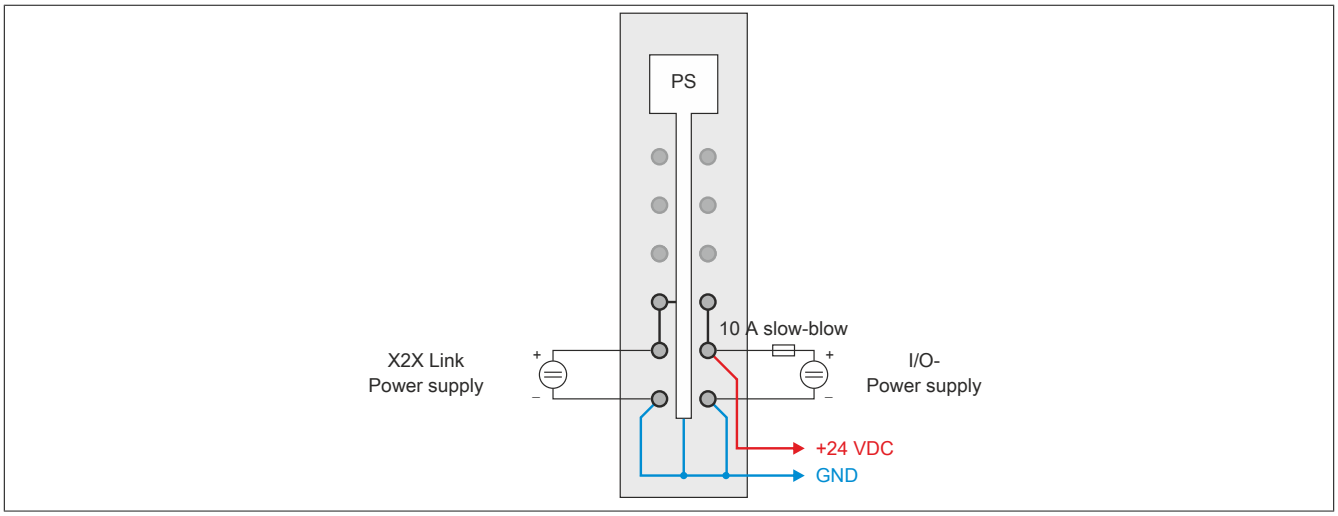
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • The X2X Link supply for the power supply is overloaded • I/O supply too low • Input voltage for X2X Link supply too low
	e + r	Red on / Green single flash		Invalid firmware
	l	Red	Off	The X2X Link supply is within the valid limits
			On	The X2X Link supply for the power supply is overloaded

4.27.4.6 Pinout

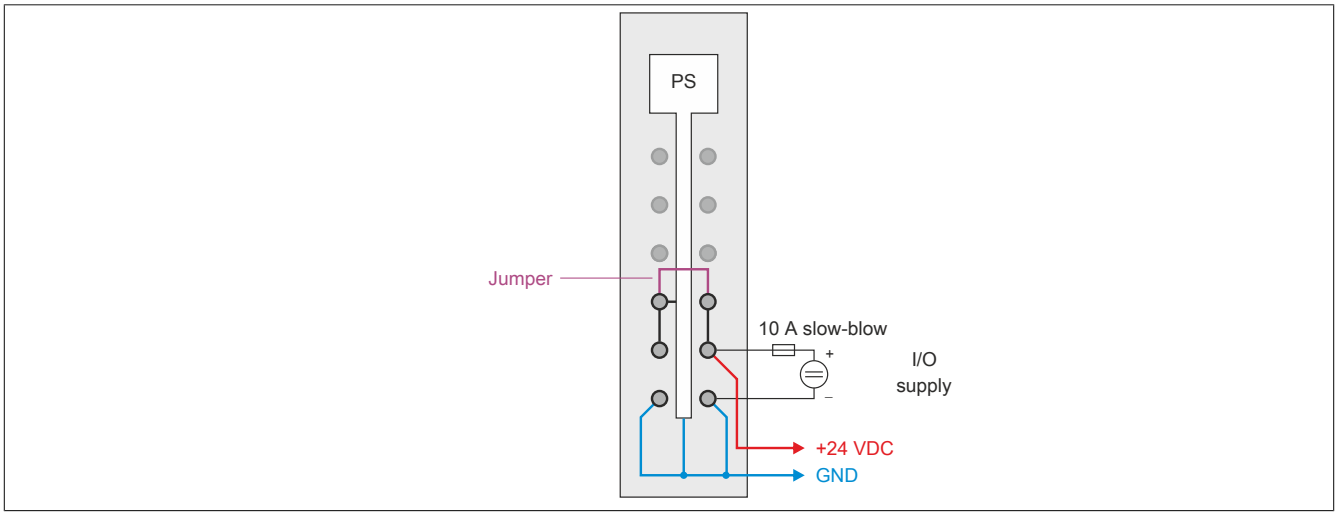


4.27.4.7 Connection examples

With 2 separate supplies

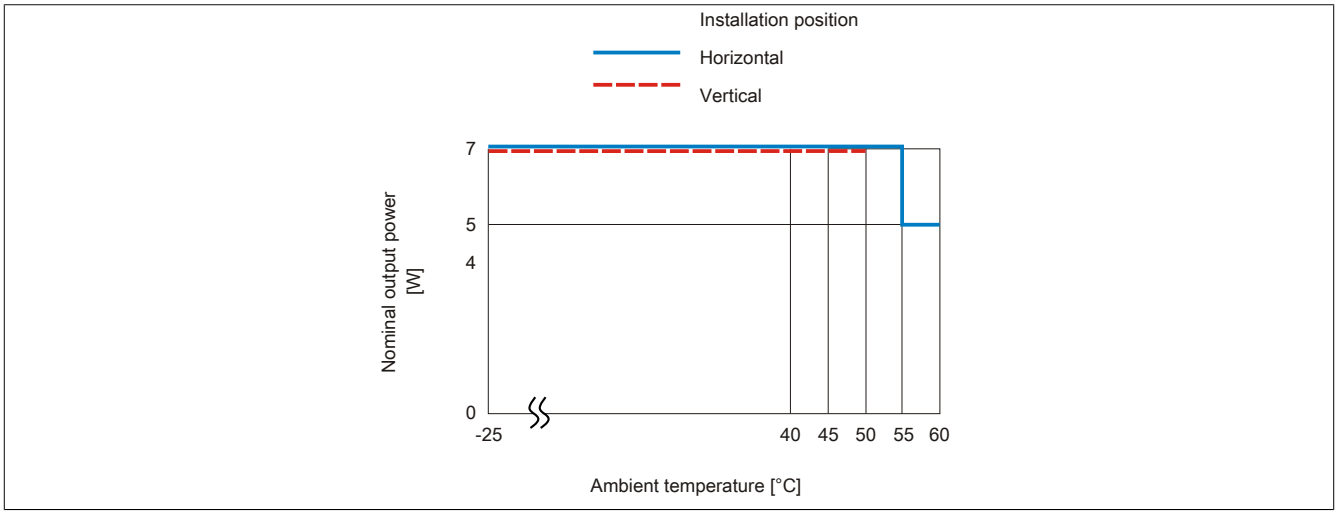


With a supply and jumper



4.27.4.8 Derating

The rated output current for the supply is 7 W. Derating must be taken into consideration based on mounting orientation.



4.27.4.9 Register description

4.27.4.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.27.4.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
2	SupplyCurrent	USINT	•			
4	SupplyVoltage	USINT	•			

4.27.4.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 2				
2	2	SupplyCurrent	UINT	•			
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.27.4.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.27.4.9.4 Module status

Name:
Module status

The following voltage and current states of the module are monitored in this register:

Bus supply current:	A bus supply current of >2.3A is displayed as a warning.
Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Warning - overcurrent (>2.3 A) or undervoltage (<4.7 V)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.27.4.9.5 Bus supply current

Name:
SupplyCurrent

This register displays the bus supply current measured at a resolution of 0.1 A.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.27.4.9.6 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.27.4.9.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.27.4.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.27.5 X20(c)PS3310

4.27.5.1 General information

The supply module is equipped with a feed for the X2X Link as well as the internal I/O supply. The module has an integrated replaceable fuse for the I/O supply.

- Feed for X2X Link and internal I/O supply
- Electrical isolation of feed and X2X Link supply
- Redundancy of X2X Link supply possible by operating multiple supply modules simultaneously
- Fuse for I/O supply integrated in module

4.27.5.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.27.5.3 Order data

Model number	Short description	Figure
	Power supplies	
X20PS3300	X20 power supply module, for X2X Link and internal I/O supply	
X20cPS3300	X20 power supply module, coated, for X2X Link and internal I/O supply	
	Required accessories	
	Bus modules	
X20BM01	X20 power supply bus module, 24 VDC keyed, internal I/O supply interrupted to the left	
X20BM05	X20 power supply bus module, with node number switch, 24 VDC keyed, internal I/O supply interrupted to the left	
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 671: X20PS3300, X20cPS3300 - Order data

4.27.5.4 Technical data

Product ID	X20PS3310	X20cPS3310
Short description		
Power supply module	24 VDC supply module for I/O and bus	
General information		
B&R ID code	0x2017	0xDD46
Status indicators	Overload, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Overload	Yes, using status LED and software	
Power consumption [1]		
Bus	1.31 W	
Internal I/O	0.82 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
I/O feed - I/O supply	No	
X2X Link feed - X2X Link supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
X2X Link input supply		
Input voltage	24 VDC -15 % / +20 %	
Input current	Max. 0.7 A	
Fuse	Integrated, cannot be replaced	
Reverse polarity protection	Yes	
X2X Link supply output		
Nominal output power	7 W	
Parallel operation	Yes [3]	
Redundant operation	Yes	
Overload behavior	Short circuit / temporary overload protection	
Input I/O supply		
Input voltage	24 VDC -15 % / +20 %	
Input current	Max. 6 A	
Fuse	Integrated 6.3 A, slow-blow, can be replaced	
Reverse polarity protection	No	
Output I/O supply		
Rated output voltage	24 VDC	
Behavior if a short circuit occurs	Integrated fuse	
Permitted contact load	6 A	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section "Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM01 supply bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM01 supply bus module separately
Spacing	12.5$^{+0.2}$ mm	

Table 672: X20PS3310, X20cPS3310 - Technical data

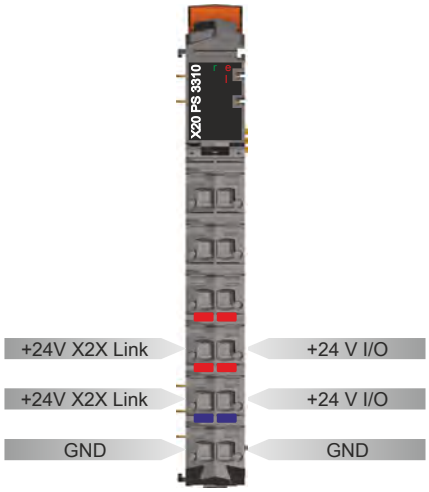
1) The specified values are maximum values. The exact calculation is also available for download as a data sheet with the other module documentation on the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions
3) In parallel operation, only 75% of the rated power can be assumed. It is important to make sure that all power supplies operated in parallel are switched on and off at the same time.

4.27.5.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

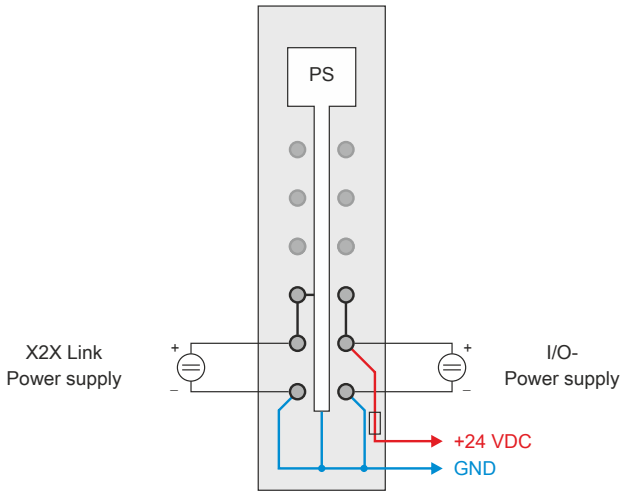
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Double flash	LED indicates one of the following states: • The X2X Link supply for the power supply is overloaded • I/O supply too low • Input voltage for X2X Link supply too low
	e + r	Red on / Green single flash		Invalid firmware
	l	Red	Off	The X2X Link supply is within the valid limits
			On	The X2X Link supply for the power supply is overloaded

4.27.5.6 Pinout

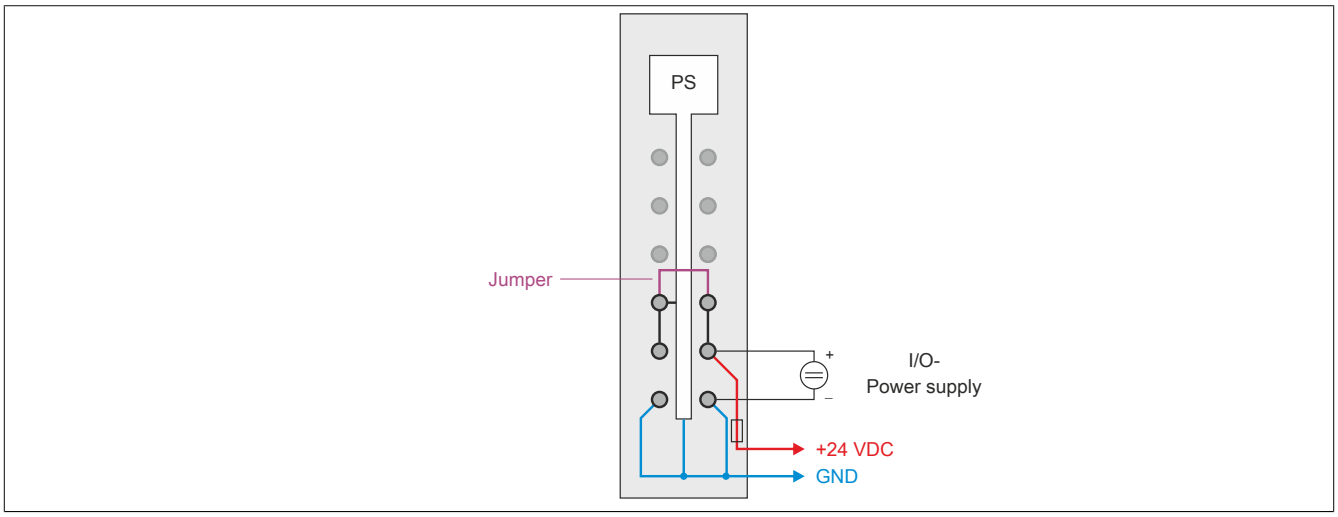


4.27.5.7 Connection examples

With 2 separate supplies

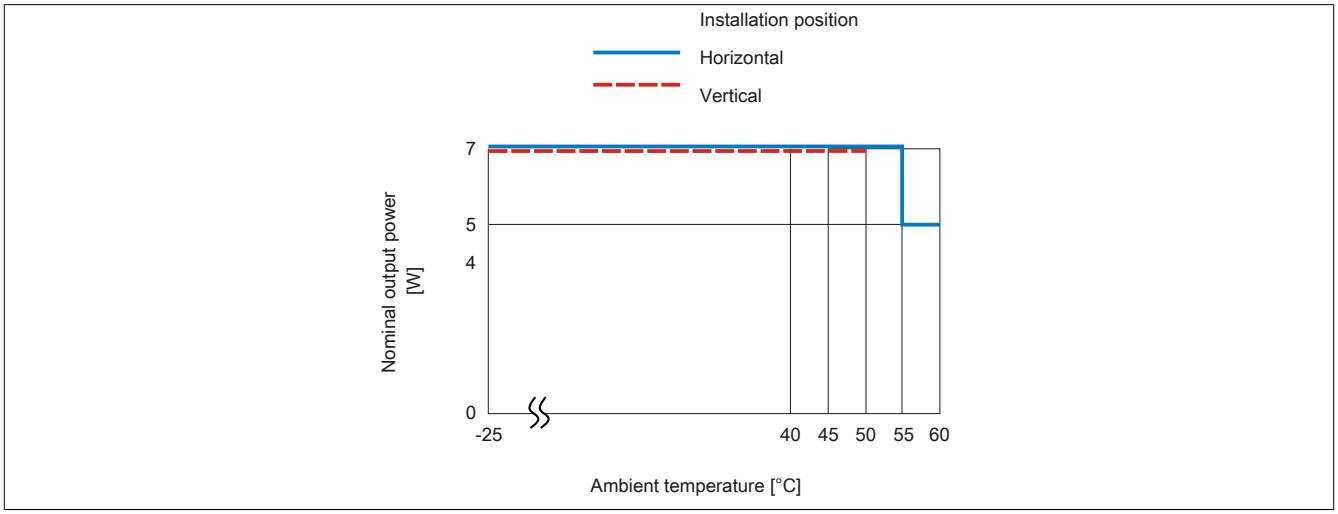


With a supply and jumper



4.27.5.8 Derating

The rated output current for the supply is 7 W. Derating must be taken into consideration based on mounting orientation.



4.27.5.9 Register description

4.27.5.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.27.5.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	Module status	USINT	•			
	StatusInput01	Bit 0				
	StatusInput02	Bit 2				
2	SupplyCurrent	USINT	•			
4	SupplyVoltage	USINT	•			

4.27.5.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
0	0	Module status	UINT	•			
		StatusInput01	Bit 0				
		StatusInput02	Bit 2				
2	2	SupplyCurrent	UINT	•			
4	4	SupplyVoltage	UINT	•			

1) The offset specifies the position of the register within the CAN object.

4.27.5.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.27.5.9.4 Module status

Name:
Module status

The following voltage and current states of the module are monitored in this register:

Bus supply current:	A bus supply current of >2.3A is displayed as a warning.
Bus supply voltage:	A bus supply voltage of <4.7V is displayed as a warning.
24 VDC I/O supply voltage:	An I/O supply voltage of <20.4 V is displayed as a warning.

Function model	Data type	Value
0 - Standard	USINT	See bit structure.
254 - Bus controller	UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusInput01	0	No error
		1	Warning - overcurrent (>2.3 A) or undervoltage (<4.7 V)
1	Reserved	0	
2	StatusInput02	0	I/O supply above the warning level of 20.4 V
		1	I/O supply below the warning level of 20.4 V
3 - x	Reserved	0	

4.27.5.9.5 Bus supply current

Name:
SupplyCurrent

This register displays the bus supply current measured at a resolution of 0.1 A.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.27.5.9.6 Bus supply voltage

Name:
SupplyVoltage

This register displays the bus supply voltage measured at a resolution of 0.1 V.

Function model	Data type
0 - Standard	USINT
254 - Bus controller	UINT

4.27.5.9.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.27.5.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
2 ms

4.28 Redundancy system

Redundant network cabling is often essential to safe operation, especially in processing plants. The potential for danger, especially to the lines that run through the plant, can be disproportionately high in relation to the need to keep communication active in all operating situations. Redundant cabling and separate cable routing are effective ways to help reduce this risk.

POWERLINK cable redundancy is based on the principle of doubling the communication lines as well as providing continuous and simultaneous monitoring. A mechanism feeds data simultaneously into two cable lines. The same mechanisms are used to receive this data from the redundant network.

The following modules can be used to set up a POWERLINK network with cable redundancy:

- X20IF2181-2 interface module
- X20HB8884 compact link selector
- X20BC8084 bus controller

4.28.1 Brief information

Product ID	Short description	on page
X20HB8884	X20 compact link selector, 2x RJ45, order bus base, power supply module and terminal block separately.	2908
X20cHB8884	X20 compact link selector, coated, 2x RJ45, order bus base, power supply module and terminal block separately.	2908

4.28.2 X20(c)HB8884

4.28.2.1 General information

POWERLINK is a standard protocol for Fast Ethernet with hard real-time properties. The Ethernet POWERLINK Standardization Group (EPSG) ensures that the standard remains open and is continually developed. www.ethernet-powerlink.org

Systems with redundant cabling can be implemented easily using POWERLINK. Unlike ring redundancy, cable redundancy does not require cable looping, which can sometimes be problematic. This allows the creation of all types of tree structures. When using a device with the link selector function, data is always transferred via the highest quality network lines. The link selector function is integrated in the module compact link selector. This makes it easy to connect any POWERLINK device to a redundant POWERLINK network.

- Connecting POWERLINK devices to the POWERLINK cable redundancy system
- Integrated compact link selector function

4.28.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.28.2.3 Order data

Model number	Short description	Figure
	X20 redundancy systems	
X20HB8884	X20 compact link selector, 2x RJ45, order bus base, power supply module and terminal block separately.	
X20cHB8884	X20 compact link selector, coated, 2x RJ45, order bus base, power supply module and terminal block separately.	
	Required accessories	
	System modules for X20 redundancy systems	
X20HB2885	X20 hub expansion module, integrated active 2-port hub, 2x RJ45	
	System modules for expandable bus controllers	
X20BB81	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	System modules for the X20 hub system	
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45	
X20PS8002	X20 power supply module for standalone hub and compact link selector	
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45	
X20cPS8002	X20 power supply module, coated, for standalone hub and compact link selector	
	System modules for the X20 redundancy system	
X20cHB2885	X20 hub expansion module, coated, integrated active 2-port hub, 2x RJ45	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 673: X20HB8884, X20cHB8884 - Order data

4.28.2.4 Technical data

Product ID	X20HB8884	X20cHB8884
Short description		
POWERLINK compact link selector	Connects POWERLINK devices to a redundant POWERLINK network	
General information		
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED	
Bus function	Yes, using status LED	
Power consumption	2 W	
Electrical isolation		
Fieldbus - Supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Type	POWERLINK compact link selector	
Design	2x shielded RJ45	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100 BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20PS8002 power supply module separately Order 1x X20HB2880 or 2x X20HB2885 hub expansion module separately Order 1x X20BB81 or X20BB82 bus base separately	Order 1x X20TB12 terminal block separately Order 1x X20cPS8002 supply module separately Order 1x X20cHB2880 or 2x X20cHB2885 hub expansion module separately Order 1x X20cBB81 or X20cBB82 bus base separately
Spacing [2]		
X20BB81	62.5 $^{+.02}$ mm	
X20BB82	87.5 $^{+0.2}$ mm	

Table 674: X20HB8884, X20cHB8884 - Technical data

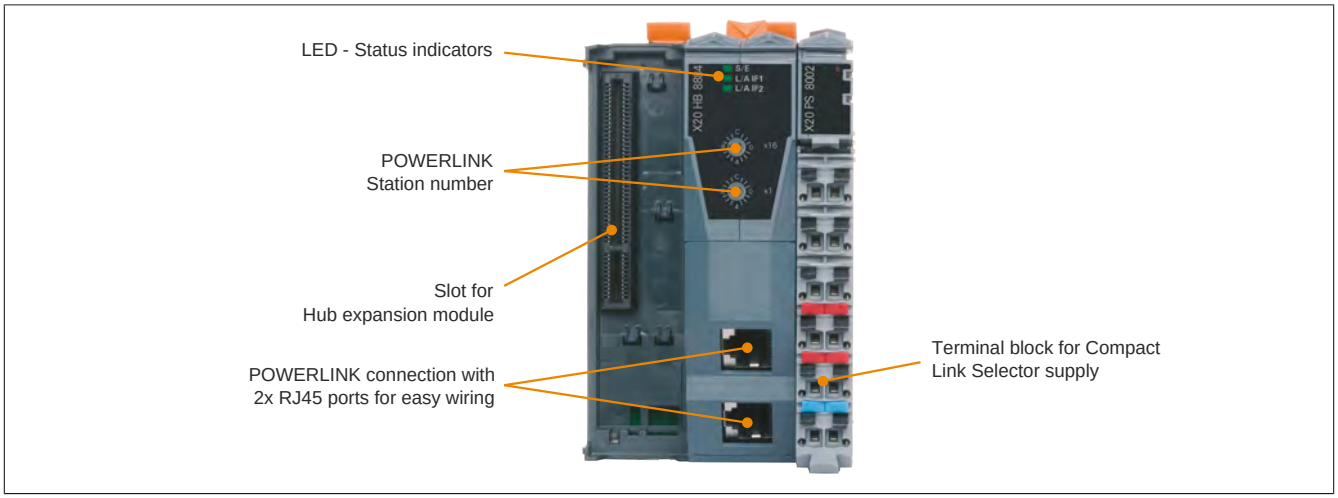
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) Spacing is based on the width of the X20BB81 or X20BB82 bus base. One X20HB2880 hub expansion module or two X20HB2885 hub expansion modules and an X20PS8002 supply module are also always required for the compact link selector.

4.28.2.5 LED status indicators

Figure	LED	Color	Status	Description
	S/E[1]	Green	On	An active POWERLINK network was detected on both networks.
		Red	Single flash	Network 2 is active. Disturbances detected on network 1 or there is no POWERLINK network active. **The LED blinks red several times immediately after startup. This is not an error.**
			Double flash	Network 1 is active. Disturbances detected on network 2 or there is no POWERLINK network active. Note: The LED blinks red several times immediately after startup. This is not an error.
			On	Failure of both networks.
	L/A IFx	Green	Blinking	A link to the peer station has been established. The LED blinks when Ethernet activity is taking place on the bus.
			On	A link to the remote station has been established.

1) The Status/Error LED is a green/red dual LED.

4.28.2.6 Operating and connection elements

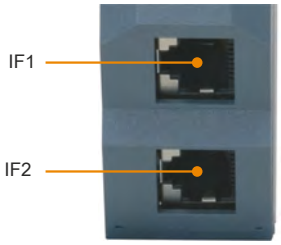


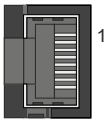
4.28.2.7 POWERLINK node numbers

The number switches have no function during operation. They are only used for product testing.

4.28.2.8 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 1 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.28.2.9 POWERLINK cable redundancy system

It is often indispensable to have redundant network cabling, especially in systems that handle technical processes. The potential for danger, especially to the lines that run through the system, is disproportionately high in relation to the need to keep communication active in all operating situations. This risk is effectively reduced with double cabling that is routed separately.

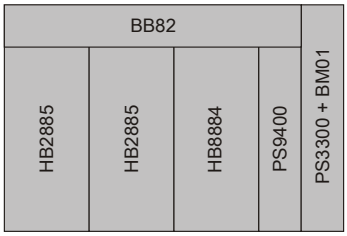
The POWERLINK cable redundancy system is based on the principle of doubling the transfer routing as well as providing continual and simultaneous monitoring. That means data is simultaneously fed into two cable lines using a corresponding mechanism. The same mechanisms are used to receive these telegrams from the redundant network.

Details about the structure of a redundancy system can be found in the "Redundancy for control systems" user's manual. The user's manual is available in the Downloads section of the B&R website www.br-automation.com.

4.28.2.10 Redundant supply voltage

When operating the X20HB8884 with two X20HB2885 hub modules, a redundant supply voltage for the system can be easily implemented using two X20 supply modules.

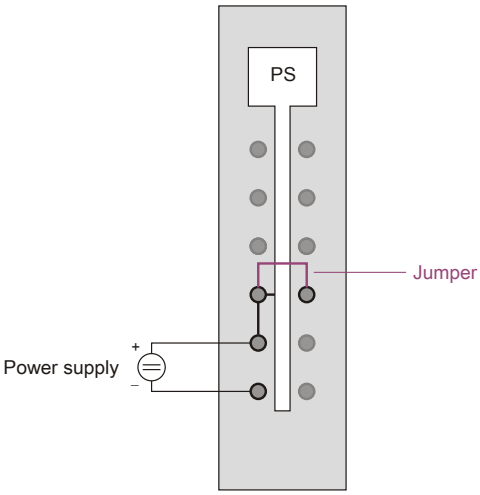
Hardware configuration



Connection example for supply modules

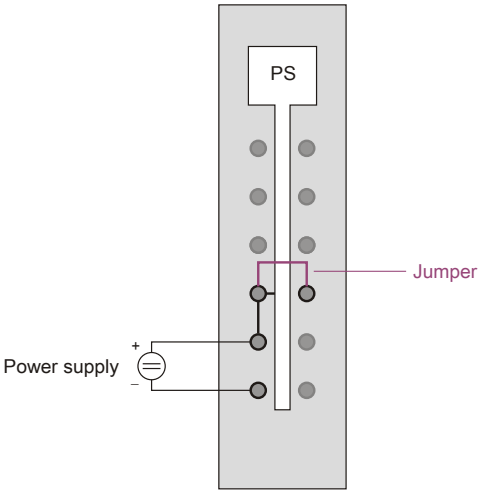
X20PS9400

On the X20PS9400, only the supply for the X20HB8884 is connected. For correct operation of the Error LED, a jumper is required.



X20PS3300

The supply module X20PS3300 is operated with a X20BM01 bus module. Only the supply for the X20HB8884 is connected. For correct operation of the Error LED, a jumper is required.



4.29 System modules for the X20 hub system

The X20 hub system has a modular structure. In addition to the basis modules, the following system modules are also required,

- Bus base
- Hub expansion module(s)
- Power supply module for standalone hub

4.29.1 Brief information

Product ID	Short description	on page
X20HB1881	X20 hub expansion module, integrated 1-port hub, for fiber optic cable	2914
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45	2917
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable	2920
X20HB28G0	X20 EtherCAT junction module, integrated 2-port EtherCAT junction, 2x RJ45	2923
X20PS8002	X20 power supply module for standalone hub and compact link selector	2926
X20cHB1881	X20 hub expansion module, coated, integrated 1-port hub, for fiber optic cable	2914
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45	2917
X20cHB2881	X20 hub expansion module, coated, integrated 2-port hub, for fiber optic cable	2920
X20cPS8002	X20 power supply module, coated, for standalone hub and compact link selector	2926

4.29.2 X20(c)HB1881

4.29.2.1 General information

The POWERLINK bus controllers X20BC8083, X20BC8084 (revision D0 or higher) and the stand-alone hub X20HB8880 are equipped with a modular hub expansion. An additional 1 or 2 slots are available, depending on the bus base used. The X20HB1881 hub expansion module can be operated in these slots. Note that the hardware revision of the X20BC8083 and the X20HB8880 must be ≥F0.

The hub expansion module is a 1x hub. The Ethernet connection is made using 62.5/125 µm or 50/125 µm fiber optic multimode cable with a duplex LC connection. The module and network status is indicated using LEDs.

- Hub expansion module
- 1x hub 100 BASE-FX
- Hot-swap-capable

4.29.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.29.2.3 Order data

Model number	Short description	Figure
	System modules for the X20 hub system	
X20HB1881	X20 hub expansion module, integrated 1-port hub, for fiber optic cable	
X20cHB1881	X20 hub expansion module, coated, integrated 1-port hub, for fiber optic cable	

Table 675: X20HB1881, X20cHB1881 - Order data

4.29.2.4 Technical data

Product ID	X20HB1881	X20cHB1881
Short description		
Hub	1 Fast Ethernet interface for fiber optic cable for hub expansion	
General information		
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED	
Bus function	Yes, using status LED	
Power consumption	1.45 W (Rev. <D0: 1.65 W)	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - Supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 1)	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Type	Hub expansion module	
Design	1x duplex LC female	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100 BASE-FX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	No	
Auto-MDI / MDIX	No	
Hub runtime	0.96 to 1 µs	
Cable fiber type	Multimode fiber with 62.5/125 µm or 50/125 µm core diameter On both sides: Duplex LC male connector	
Optical power budget		
Optical fiber 62.5/125 µm, NA = 0.275	11 dB	
Optical fiber 50/125 µm, NA = 0.200	7.5 dB	
Cable length		
Half-duplex	Max. 400 m between 2 stations (segment length)	
POWERLINK	Max. 2 km between 2 stations (segment length)	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	Hub expansion for X20BC8083, X20BC8084 and X20HB8880 2)	Hub expansion for X20cBC8084 and X20cHB8880 3)

Table 676: X20HB1881, X20cHB1881 - Technical data

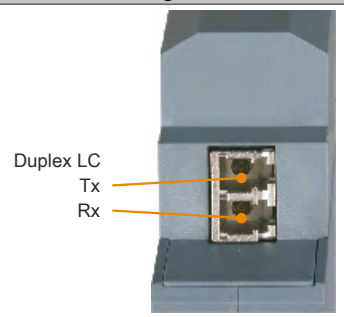
1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The hardware revision of X20BC8083 and X20HB8880 must be ≥F0 and the hardware revision of X20BC8084 must be ≥D0.
3) The hardware revision of X20cHB8880 must be ≥F0 and the hardware revision of X20cBC8084 must be ≥D0.

4.29.2.5 LED status indicators

Figure	LED	Color	Status	Description
	ERR	Red	On	Slot not detected
	RDY	Orange	On	Slow detected, module is active
	L/A	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus.

4.29.2.6 Operating and connection elements

4.29.2.7 Ethernet interface

Figure	Description
	100 BASE-FX, Duplex LC female

4.29.2.8 Wiring guidelines for X20 modules with fiber optic cable

The following wiring guidelines must be observed:

- Cable fiber type: Multimode fiber with 62.5/125 µm or 50/125 µm core diameter
- On both sides: Duplex LC male connector
- Observe minimum cable flex radius (see data sheet for the cable)

4.29.3 X20(c)HB2880

4.29.3.1 General information

The POWERLINK bus controller X20BC8083 and the stand-alone hubs X20HB8880 and X20HB8815 are equipped with a modular hub expansion. An additional 1 or 2 slots are available, depending on the bus base used. The X20HB2880 hub expansion module can be operated in these slots.

The status of the module and network are indicated by LEDs.

- Hub expansion module
- 2x hub 100 BASE-TX

4.29.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.29.3.3 Order data

Model number	Short description	Figure
	System modules for the X20 hub system	
X20HB2880	X20 hub expansion module, integrated 2-port hub, 2x RJ45	
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45	

Table 677: X20HB2880, X20cHB2880 - Order data

4.29.3.4 Technical data

Product ID	X20HB2880	X20cHB2880
Short description		
Hub	2 Fast Ethernet hubs for hub expansion	
General information		
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED	
Bus function	Yes, using status LED	
Power consumption	1.17 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - Supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Interfaces		
Type	Hub expansion module	
Design	2x shielded RJ45	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	Hub expansion for X20BC8083 and X20HB8880	Hub expansion for X20cBC8083 and X20cHB8880

Table 678: X20HB2880, X20cHB2880 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

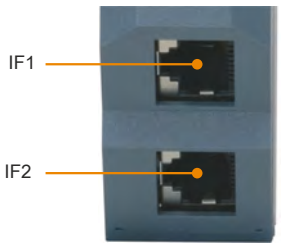
4.29.3.5 LED status indicators

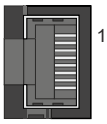
Figure	LED	Color	Status	Description
	ERR	Red	On	Slot not detected
	RDY	Orange	On	Slow detected, module is active
	L/A IFx	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus.

4.29.3.6 Operating and connection elements

4.29.3.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.29.4 X20(c)HB2881

4.29.4.1 General information

The POWERLINK bus controller X20BC8083 and the stand-alone hubs X20HB8880 and X20HB8815 are equipped with a modular hub expansion. An additional 1 or 2 slots are available, depending on the bus base used. The X20HB2881 hub expansion module can be operated in these slots. Note that the hardware revision of the X20BC8083 and the X20HB8880 must be ≥F0.

The hub expansion module is a 2x hub. The Ethernet connection is made using 62.5/125 µm or 50/125 µm fiber optic multimode cable with a duplex LC connection. The status of the module and network are indicated by LEDs.

- Hub expansion module
- 2x Hub 100 BASE-FX

4.29.4.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.29.4.3 Order data

Model number	Short description	Figure
	System modules for the X20 hub system	
X20HB2881	X20 hub expansion module, integrated 2-port hub, for fiber optic cable	
X20cHB2881	X20 hub expansion module, coated, integrated 2-port hub, for fiber optic cable	

Table 679: X20HB2881, X20cHB2881 - Order data

4.29.4.4 Technical data

Product ID	X20HB2881	X20cHB2881
Short description		
Hub	2 Fast Ethernet interfaces for fiber optic cable for hub expansion	
General information		
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED	
Bus function	Yes, using status LED	
Power consumption	2.3 W (Rev. <E0: 2.8 W)	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - Supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Type	Hub expansion module	
Design	2x duplex LC female	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100 BASE-FX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	No	
Auto-MDI / MDIX	No	
Hub runtime	0.96 to 1 µs	
Cable fiber type	Multimode fiber with 62.5/125 µm or 50/125 µm core diameter On both sides: Duplex LC male connector	
Optical power budget		
Optical fiber 62.5/125 µm, NA = 0.275	11 dB	
Optical fiber 50/125 µm, NA = 0.200	7.5 dB	
Cable length		
Half-duplex	Max. 400 m between 2 stations (segment length)	
POWERLINK	Max. 2 km between 2 stations (segment length)	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation (with 1 hub)	-25 to 55°C (Rev. <E0: 0 to 45°C)	
Horizontal installation (with ≥2 hubs)	-25 to 50°C (Rev. <E0: 0 to 40°C)	
Vertical installation (with 1 hub)	-25 to 40°C (Rev. <E0: 0 to 40°C)	
Vertical installation (with ≥2 hubs)	-25 to 35°C (Rev. <E0: 0 to 35°C)	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	Hub expansion for X20BC8083 and X20HB8880 [2]	Hub expansion for X20cBC8083 and X20cHB8880 [3]

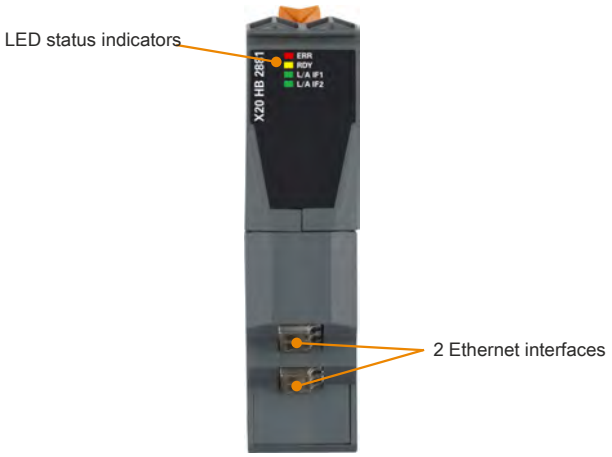
Table 680: X20HB2881, X20cHB2881 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The hardware revision of X20BC8083 and X20HB8880 must be ≥F0.
3) The hardware revision of X20cBC8083 and X20cHB8880 must be ≥F0.

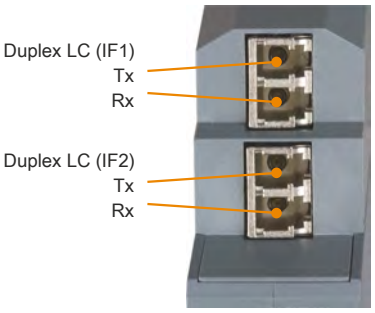
4.29.4.5 LED status indicators

Figure	LED	Color	Status	Description
	ERR	Red	On	Slot not detected
	RDY	Orange	On	Slow detected, module is active
	L/A IFx	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus.

4.29.4.6 Operating and connection elements



4.29.4.7 Ethernet interfaces

Figure	Description
	100 BASE-FX, Duplex LC female

4.29.4.8 Wiring guidelines for X20 modules with fiber optic cable

The following wiring guidelines must be observed:

- Cable fiber type: Multimode fiber with 62.5/125 µm or 50/125 µm core diameter
- On both sides: Duplex LC male connector
- Observe minimum cable flex radius (see data sheet for the cable)

4.29.5 X20HB28G0

4.29.5.1 General information

The X20BC80G3 expandable EtherCAT bus controller and the X20HB88G0 stand-alone EtherCAT junction base module are equipped with an additional slot. The X20HB28G0 EtherCAT junction module is operated in this slot.

The X20HB28G0 module is equipped with a 2x EtherCAT junction. The status of the module and network are indicated by LEDs.

- EtherCAT junction module
- 2x EtherCAT junction

4.29.5.2 Order data

Model number	Short description	Figure
	System modules for the X20 hub system	
X20HB28G0	X20 EtherCAT junction module, integrated 2-port EtherCAT junction, 2x RJ45	

Table 681: X20HB28G0 - Order data

4.29.5.3 Technical data

Product ID	X20HB28G0
Short description	
Junction module	2x EtherCAT junction for expansion
General information	
Status indicators	Module status, bus function
Diagnostics	
Module status	Yes, using status LED
Bus function	Yes, using status LED
Power consumption	1.01 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Fieldbus - Supply	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Interfaces	
Type	EtherCAT junction expansion module
Design	2x RJ45, shielded
Cable length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transmission	
Physical layer	100 BASE-TX
Half-duplex	Yes
Full-duplex	Yes
Autonegotiation	Yes
Auto-MDI / MDIX	Yes
Hub runtime	See data sheet for X20BC80G3 and X20HB88G0
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-25 to 70°C
Transport	-25 to 70°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Slot	Hub expansion for X20BC80G3 and X20HB88G0

Table 682: X20HB28G0 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

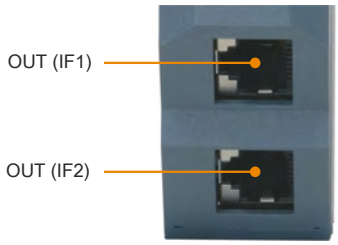
4.29.5.4 LED status indicators

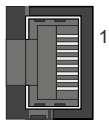
Figure	LED	Color	Status	Description
	RUN	Green	On	Module is active
	L/A OUT	Green	Blinking	The respective LED blinks when Ethernet activity is present (PORT OPEN) on the corresponding interface.
			On	Connection (link) established, however no communication (PORT OPEN).
			Off	No physical Ethernet connection exists (PORT CLOSED).

4.29.5.5 Operating and connection elements

4.29.5.6 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	TXD	Transmit data
	2	TXD\	Transmit data\
	3	RXD	Receive data
	4	Termination	
	5	Termination	
	6	RXD\	Receive data\
	7	Termination	
	8	Termination	

4.29.6 X20(c)PS8002

4.29.6.1 General information

The supply module is used to supply X20 stand-alone devices. These include e.g. the X20HB8884 POWERLINK compact link selector and the X20HB8880 stand alone hub.

- Supply for X20 stand-alone devices
- No electrical isolation between the I/O supply and the device power supply

4.29.6.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.29.6.3 Order data

Model number	Short description	Figure
	System modules for the X20 hub system	
X20PS8002	X20 power supply module for standalone hub and compact link selector	
X20cPS8002	X20 power supply module, coated, for standalone hub and compact link selector	
	Required accessories	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 683: X20PS8002, X20cPS8002 - Order data

4.29.6.4 Technical data

Product ID	X20PS8002	X20cPS8002
Short description		
Power supply module	24 VDC power supply module for X20 standalone devices	
General information		
Status indicators	Operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED	
Overload	Yes, using status LED	
Power consumption [1]	1.34 W	
Electrical isolation		
I/O supply - Device supply	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [2]	Yes	
KC	Yes	-
GOST-R	Yes	
Input supply		
Input voltage	24 VDC -15 % / +20 %	
Input current	Max. 0.7 A	
Fuse	Integrated, cannot be replaced	
Reverse polarity protection	Yes	
Output supply		
Overload behavior	Short circuit / temporary overload protection	
Nominal output power		
Horizontal installation	7 W at 45°C and 5 W at 55°C	
Vertical installation	7 W at 40°C and 5 W at 50°C	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	See section"Derating"	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately	
Spacing	$12.5^{+0.2}$ mm	

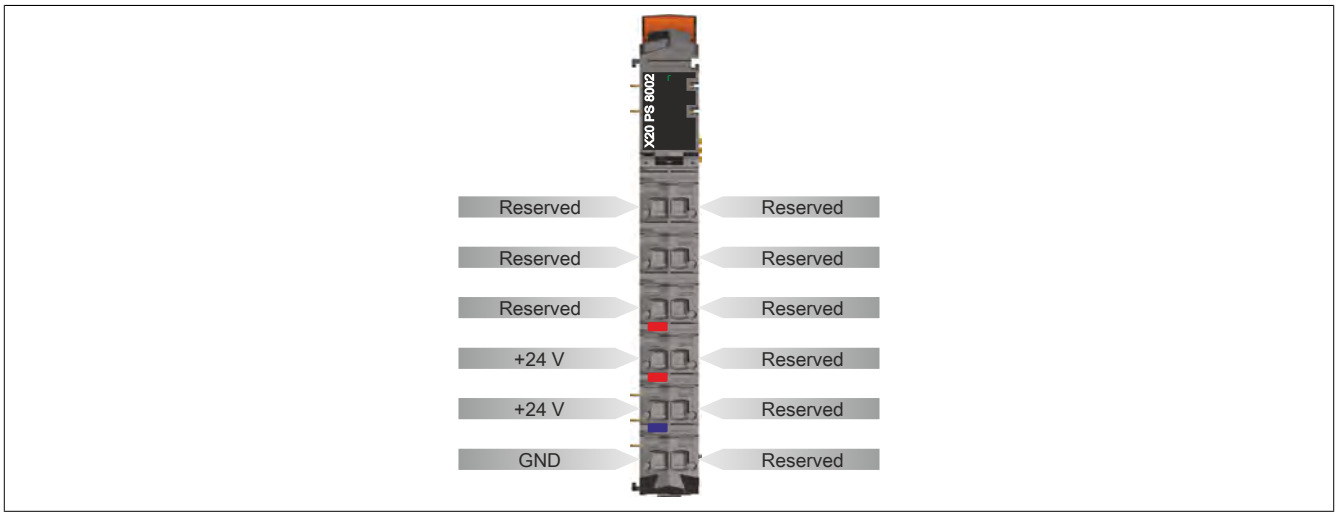
Table 684: X20PS8002, X20cPS8002 - Technical data

1) The specified values are maximum values. The exact calculation is included as a data sheet in the module documentation and can be downloaded from the B&R website.
2) Ta min.: 0°C
Ta max.: See environmental conditions

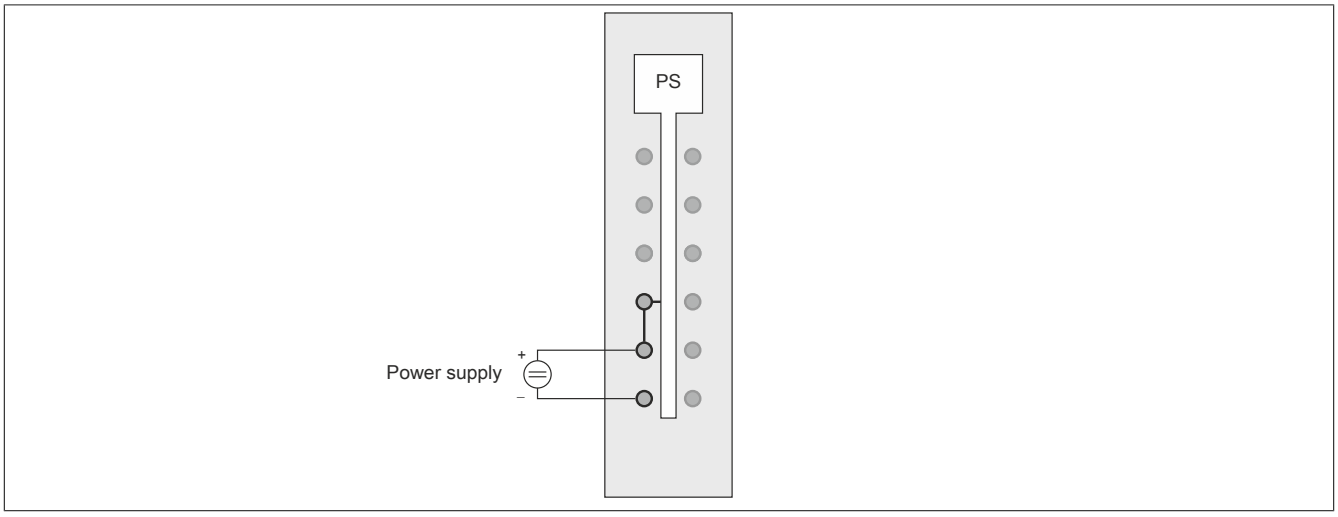
4.29.6.5 LED status indicators

Figure	LED	Color	Status	Description
	r	Green	On	Input voltage > 19.2 V

4.29.6.6 Pinout

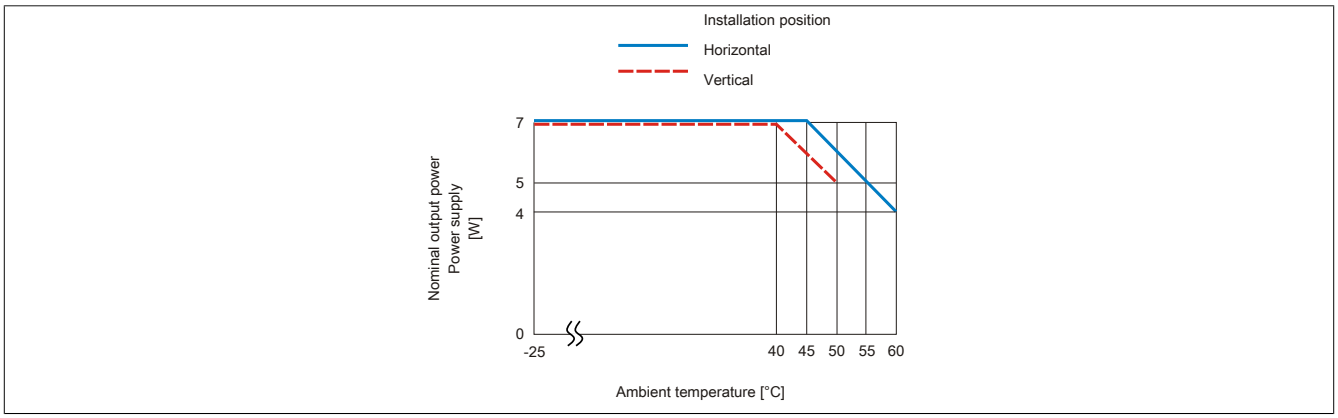


4.29.6.7 Connection example



4.29.6.8 Derating

The rated output current for the supply is 7 W. Derating must be taken into consideration based on mounting orientation.



4.30 System modules for the X20 redundancy system

The X20 redundancy system has a modular structure. In addition to the basis modules, the following system modules are also required,

- Bus base
- Hub expansion module(s)
- Power supply module for standalone hub

4.30.1 Brief information

Product ID	Short description	on page
X20HB2885	X20 hub expansion module, integrated active 2-port hub, 2x RJ45	2930
X20HB2886	X20 hub expansion module, integrated active 2-port hub, 2 fiber optic interfaces	2934
X20cHB2885	X20 hub expansion module, coated, integrated active 2-port hub, 2x RJ45	2930
X20cHB2886	X20 hub expansion module, coated, integrated active 2-port hub, 2 fiber optic interfaces	2934

4.30.2 X20(c)HB2885

4.30.2.1 General information

The X20BC8084 POWERLINK bus controller and the X20HB8884 module are equipped with an integrated link selector function. An additional 1 or 2 slots are available, depending on the bus base used. The active X20HB2885 hub expansion module can be operated in these slots.

The active hub expansion module is equipped with one integrated 2x hub and allows redundant wiring. This means that the connection between the two ports remains intact if there is a failure in the bus controller or Compact Link Selector. The status of the module and network are indicated by LEDs.

- Active hub expansion module
- 2x Fast Ethernet hub for redundant wiring
- Hot-swap-capable

4.30.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.30.2.3 Order data

Model number	Short description	Figure
	System modules for X20 redundancy systems	
X20HB2885	X20 hub expansion module, integrated active 2-port hub, 2x RJ45	
	System modules for the X20 redundancy system	
X20cHB2885	X20 hub expansion module, coated, integrated active 2-port hub, 2x RJ45	
	Required accessories	
	Expandable bus controllers	
X20BC8084	X20 bus controller, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
X20BC9984	X20 bus controller POWERLINK, redundancy, ALSTOM	
X20cBC8084	X20 bus controller, coated, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
	System modules for expandable bus controllers	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	X20 redundancy systems	
X20HB8884	X20 compact link selector, 2x RJ45, order bus base, power supply module and terminal block separately	
X20cHB8884	X20 compact link selector, coated, 2x RJ45, order bus base, power supply module and terminal block separately	

Table 685: X20HB2885, X20cHB2885 - Order data

4.30.2.4 Technical data

Product ID	X20HB2885	X20cHB2885
Short description		
Hub	2 Fast Ethernet hubs for redundant wiring	
General information		
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED	
Bus function	Yes, using status LED	
Power consumption	1.17 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - Supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Type	Active hub expansion module	
Design	2x shielded RJ45	
Cable length	Max. 100 m between 2 stations (segment length)	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100BASE-TX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	Yes	
Auto-MDI / MDIX	Yes	
Hub runtime	0.96 to 1 µs	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	Hub expansion for X20BC8084 and X20HB8884	Hub expansion for X20cBC8084 and X20cHB8884

Table 686: X20HB2885, X20cHB2885 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions

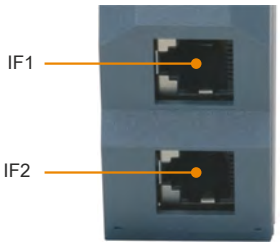
4.30.2.5 LED status indicators

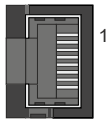
Figure	LED	Color	Status	Description
	RUN	Red	On	Module inactive. Module is in the reset state.
		Green	On	Module active
	STAT	Orange	Off	Normal operation
			Blinking	No X20BC8084 or X20HB8884 found.
			On	Normal operation. However, the X20BC8084 or X20HB8884 was inserted after the system had booted.
	L/A IFx	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus.

4.30.2.6 Operating and connection elements

4.30.2.7 Ethernet interface

Information about cabling X20 modules with an Ethernet interface can be found in the module's download section on the B&R website (www.br-automation.com).



Interface	Pinout		
	Pin	Ethernet	
 Shielded RJ45	1	RXD	Receive data
	2	RXD\	Receive data\
	3	TXD	Transmit data
	4	Termination	
	5	Termination	
	6	TXD\	Transmit data\
	7	Termination	
	8	Termination	

4.30.3 X20(c)HB2886

4.30.3.1 General information

The X20BC8084 POWERLINK bus controller and the X20HB8884 module are equipped with an integrated link selector function. An additional 1 or 2 slots are available, depending on the bus base used. The active X20HB2886 hub expansion module can be operated in these slots. Note that the hardware revision of the X20BC8084 and the X20HB8884 must be ≥E0.

The active hub expansion module is equipped with one integrated 2x hub and allows redundant wiring. This means that the connection between the two 100 Base-FX interfaces remains intact if there is a failure in the bus controller or Compact Link Selector. The Ethernet connection is made using 62.5/125 µm or 50/125 µm fiber optic multimode cable with a duplex LC connection. The status of the module and network are indicated by LEDs.

- Active hub expansion module
- 2x 100 BASE-FX hub for redundant wiring
- Hot-swap-capable

4.30.3.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.30.3.3 Order data

Model number	Short description	Figure
	System modules for X20 redundancy systems	
X20HB2886	X20 hub expansion module, integrated active 2-port hub, 2 fiber optic interfaces	
	System modules for the X20 redundancy system	
X20cHB2886	X20 hub expansion module, coated, integrated active 2-port hub, 2 fiber optic interfaces	
	Required accessories	
	Expandable bus controllers	
X20BC8084	X20 bus controller, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
X20cBC8084	X20 bus controller, coated, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately	
	System modules for expandable bus controllers	
X20BB82	X20 bus base, for X20 base module (BC, HB, etc.) and X20 power supply module, with 2 expansion slots for 2 X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included	
	X20 redundancy systems	
X20HB8884	X20 compact link selector, 2x RJ45, order bus base, power supply module and terminal block separately	
X20cHB8884	X20 compact link selector, coated, 2x RJ45, order bus base, power supply module and terminal block separately	

Table 687: X20HB2886, X20cHB2886 - Order data

4.30.3.4 Technical data

Product ID	X20HB2886	X20cHB2886
Short description		
Hub	2 Fast Ethernet interfaces for fiber optic cable for redundant wiring	
General information		
Status indicators	Module status, bus function	
Diagnostics		
Module status	Yes, using status LED	
Bus function	Yes, using status LED	
Power consumption	2.3 W (Rev. <D0: 2.8 W)	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Fieldbus - Supply	Yes	
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GOST-R	Yes	
Interfaces		
Type	Active hub expansion module	
Design	2x duplex LC female	
Transfer rate	100 Mbit/s	
Transmission		
Physical layer	100 BASE-FX	
Half-duplex	Yes	
Full-duplex	No	
Autonegotiation	No	
Auto-MDI / MDIX	No	
Hub runtime	0.96 to 1 µs	
Cable fiber type	Multimode fiber with 62.5/125 µm or 50/125 µm core diameter On both sides: Duplex LC male connector	
Optical power budget		
Optical fiber 62.5/125 µm, NA = 0.275	11 dB	
Optical fiber 50/125 µm, NA = 0.200	7.7 dB	
Cable length		
Half-duplex	Max. 400 m between 2 stations (segment length)	
POWERLINK	Max. 2 km between 2 stations (segment length)	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation (with ≥2 hubs)	-25 to 50°C (Rev. <D0: 0 to 40°C)	
Vertical installation (with ≥2 hubs)	-25 to 35°C (Rev. <D0: 0 to 35°C)	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Slot	Hub expansion for X20BC8084 and X20HB8884 [2]	Hub expansion for X20cBC8084 and X20cHB8884 [3]

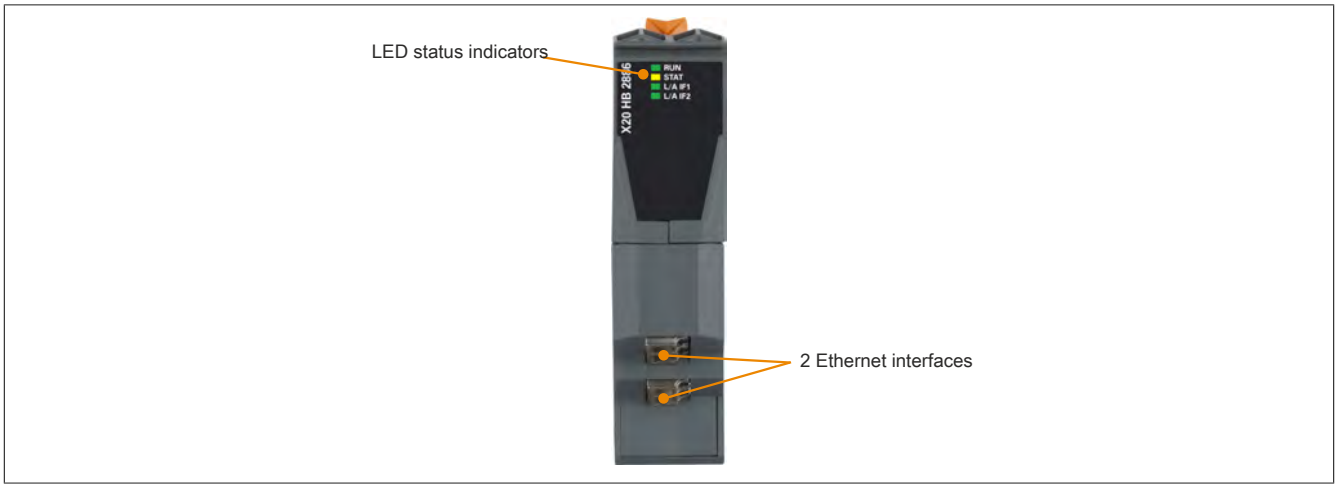
Table 688: X20HB2886, X20cHB2886 - Technical data

1) Ta min.: 0°C
Ta max.: See environmental conditions
2) The hardware revision of X20BC8084 and X20HB8884 must be ≥E0.
3) The hardware revision of X20cBC8084 and X20cHB8884 must be ≥E0.

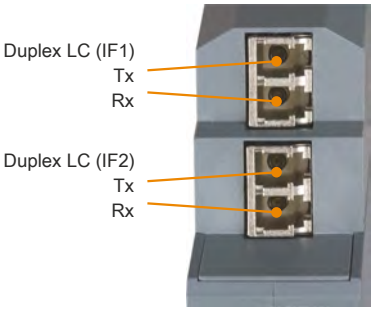
4.30.3.5 LED status indicators

Figure	LED	Color	Status	Description
	RUN	Red	On	Module inactive. Module is in the reset state.
		Green	On	Module active
	STAT	Orange	Off	Normal operation
			Blinking	No X20BC8084 or X20HB8884 found.
			On	Normal operation. However, the X20BC8084 or X20HB8884 was inserted after the system had booted.
	L/A IFx	Green	On	A link to the remote station has been established.
			Blinking	A link to the remote station has been established. Indicates Ethernet activity is taking place on the bus.

4.30.3.6 Operating and connection elements



4.30.3.7 Ethernet interfaces

Figure	Description
	100 BASE-FX, Duplex LC female

4.30.3.8 Wiring guidelines for X20 modules with fiber optic cable

The following wiring guidelines must be observed:

- Cable fiber type: Multimode fiber with 62.5/125 µm or 50/125 µm core diameter
- On both sides: Duplex LC male connector
- Observe minimum cable flex radius (see data sheet for the cable)

4.31 Temperature modules

Temperature measurement values are converted into number values which can be processed by the PLC using temperature modules.

In the PLC, the number values are always in 16-bit 2s complement, regardless of the resolution. In this way, the resolution (number of steps) of the temperature module does not have to be considered when creating the application program.

For temperature measurements, the temperature module returns the measured value in 0.1°C steps. That means, a result of 750 corresponds to 75.0°C. The data format 0.1°C is supported as standard by all temperature modules.

Every channel on temperature module has a status LED.

4.31.1 Brief information

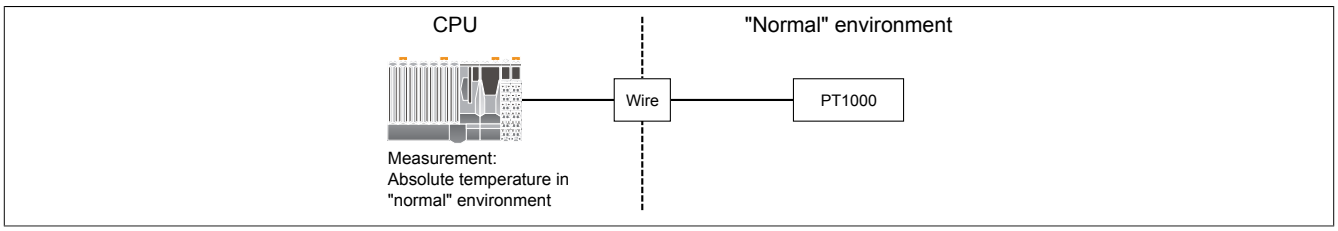
Product ID	Short description	on page
X20AT2222	X20 temperature input module, 2 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections	2939
X20AT2311	X20 temperature input module, 2 inputs for resistance measurement, PT100, resolution 0.001°C, 4-wire connections	2949
X20AT2402	X20 temperature input module, 2 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C	2957
X20AT4222	X20 temperature input module, 4 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections	2969
X20AT6402	X20 temperature input module, 6 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C	2979
X20ATA312	X20 temperature input module, 2 inputs for resistance measurement, PT100, resolution 0.01°C, 4-wire connections	2991
X20ATA492	X20 temperature input module, 2 thermocouple inputs, type J, K, N, S, B, R, E, C, T, single channel electrically isolated, 2x PT1000 integrated for terminal temperature compensation, with 1x X20TB1E terminal block, order terminal block separately	3002
X20ATB312	X20 temperature input module, 4 inputs for resistance measurement, PT100, resolution 0.01 °C, 4-wire connections	3025
X20ATC402	X20 temperature input module, 6 thermocouple inputs, type J, K, N, S, B, R, E, C, T, 2x PT1000 integrated for terminal temperature compensation, with 1x X20TB1E terminal block, order terminal block separately	3036
X20cAT4222	X20 temperature input module, coated, 4 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections	2969
X20cAT6402	X20 temperature input module, coated, 6 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C	2979

4.31.2 Measurement methods

Depending on the area to be measured, there are two different methods for determining the temperature.

Method 1: Direct measurement using measurement resistor

The temperature module measures an electrical value that makes it possible to directly infer the current absolute temperature.

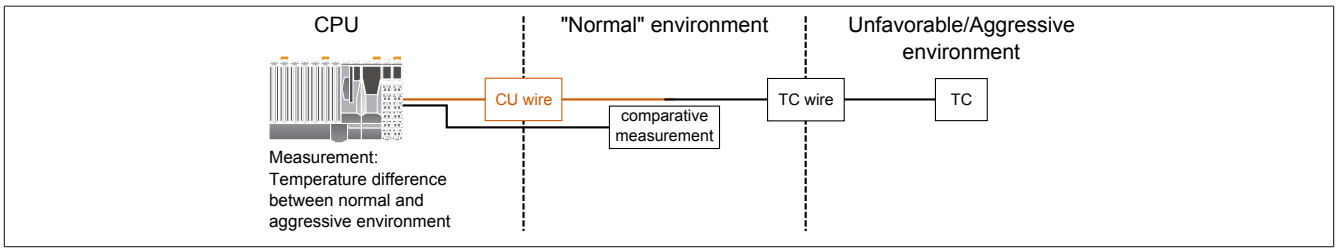


A measurement resistor often used in this method is the PT1000. Measuring the electrical resistance can be used to determine the absolute temperature at the measurement point for a temperature range of approximately -200°C to 850°C.

Method 2: Indirect measurement using thermocouples

Thermocouples are primarily used whenever it is not possible to use measurement resistors, for example because the environment directly around the measurement point contains aggressive gases.

This method of measuring bears on the basics of the thermoelectric effect. The module measures an electrical voltage, which can then be used to derive the difference in temperature.



Thermocouple modules from B&R prepare the temperature value at the measurement point as an absolute value. The measured temperature difference is referenced against another temperature that is usually measured directly at another location (see method 1).

Information:

In the best case, the temperature at the location where the thermocouple crosses an inexpensive copper cable is used as the reference or compensation value.

4.31.3 X20AT2222

4.31.3.1 General information

The module is equipped with 2 inputs for PT100/PT1000 resistance temperature measurement.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 inputs for resistance temperature measurement
- For PT100 and PT1000
- Configurable sensor type per channel
- Direct resistance measurement
- Configurable 2- or 3- wire connections per module
- Configurable filter time

4.31.3.2 Order data

Model number	Short description	Figure
	Temperature measurement	
X20AT2222	X20 temperature input module, 2 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 689: X20AT2222 - Order data

4.31.3.3 Technical data

Product ID	X20AT2222
Short description	
I/O module	2 inputs for PT100 or PT1000 resistance temperature measurement
General information	
B&R ID code	0x1BA6
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1]	Yes
KC	Yes
GL	Yes
GOST-R	Yes
Temperature inputs resistance measurement	
Input	Resistance measurement with constant current supply for 2- or 3-wire connections
Digital converter resolution	16-bit
Filter time	Configurable between 1 ms and 66.7 ms
Conversion time	
1 channel	20 ms with 50 Hz filter
2 channels	80 ms with 50 Hz filter
Conversion procedure	Sigma Delta
Output format	INT or UINT for resistance measurement
Sensor	
Sensor type	Configurable per channel
PT100	-200 to 850°C
PT1000	-200 to 850°C
Resistance measurement range	0.1 to 4500 Ω / 0.05 to 2250 Ω
Input filter	1st-order low pass / cutoff frequency 500 Hz
Sensor standard	IEC/EN 60751
Common-mode range	>0.7 V
Isolation voltage between channel and bus	500 V_{eff}
Linearization method	Internal
Measuring current	250 µA ±1.25%
Reference	4530 Ω ±0.1%
Permitted input signal	Short-term max. ±30 V
Max. error at 25°C	
Gain	0.037% [2]
Offset	0.0015% [3]
Max. gain drift	0.004% per °C [2]
Max. offset drift	0.00015% per °C [3]
Nonlinearity	<0.0010% [3]
Crosstalk between channels	<-93 dB
Temperature sensor resolution	
PT100	1 LSB = 0.1°C
PT1000	1 LSB = 0.1°C
Resistance measurement resolution	
G = 1	0.1 Ω
G = 2	0.05 Ω
Common-mode rejection	
50 Hz	>80 dB
DC	>95 dB
Standardized value range for resistance measurement	
G = 1	0.1 to 4500.0 Ω
G = 2	0.05 to 2250.0 Ω
Temperature sensor standardization	
PT100	-200.0 to 850.0°C
PT1000	-200.0 to 850.0°C

Table 690: X20AT2222 - Technical data

Product ID	X20AT2222
Temperature measurement monitoring	
Range exceeded (neg.)	0x8001
Above upper range limit	0x7FFF
Open line	0x7FFF
General error	0x8000
Open inputs	0x7FFF
Resistance measurement monitoring	
Above upper range limit	0xFFFF
Open line	0xFFFF
General error	0xFFFF
Open inputs	0xFFFF
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 690: X20AT2222 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current resistance value.
3) Based on the entire resistance measurement range.

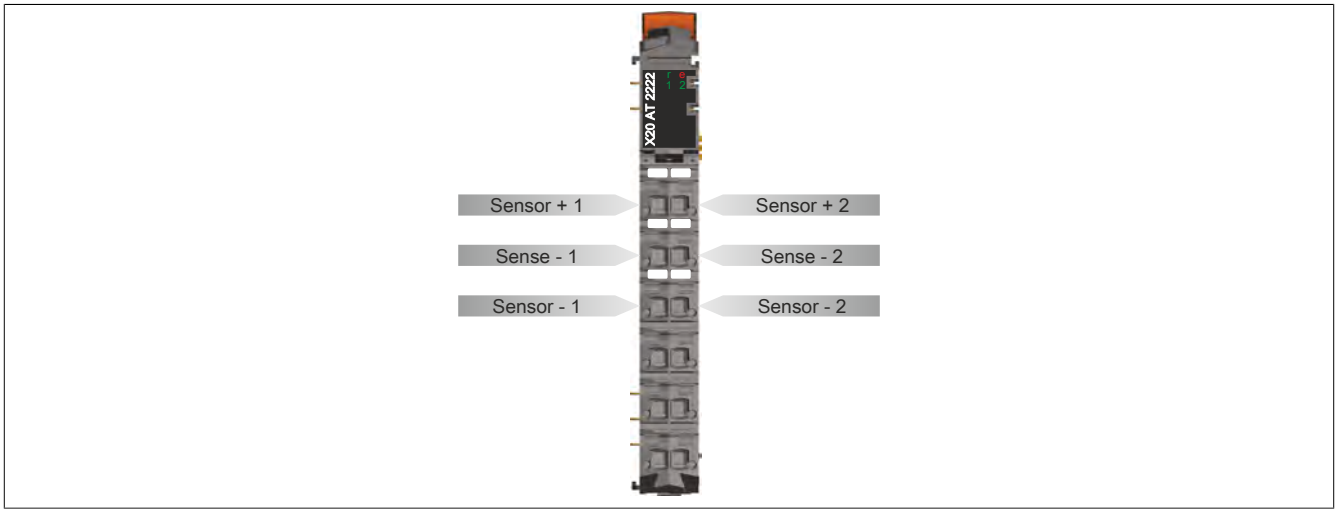
4.31.3.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

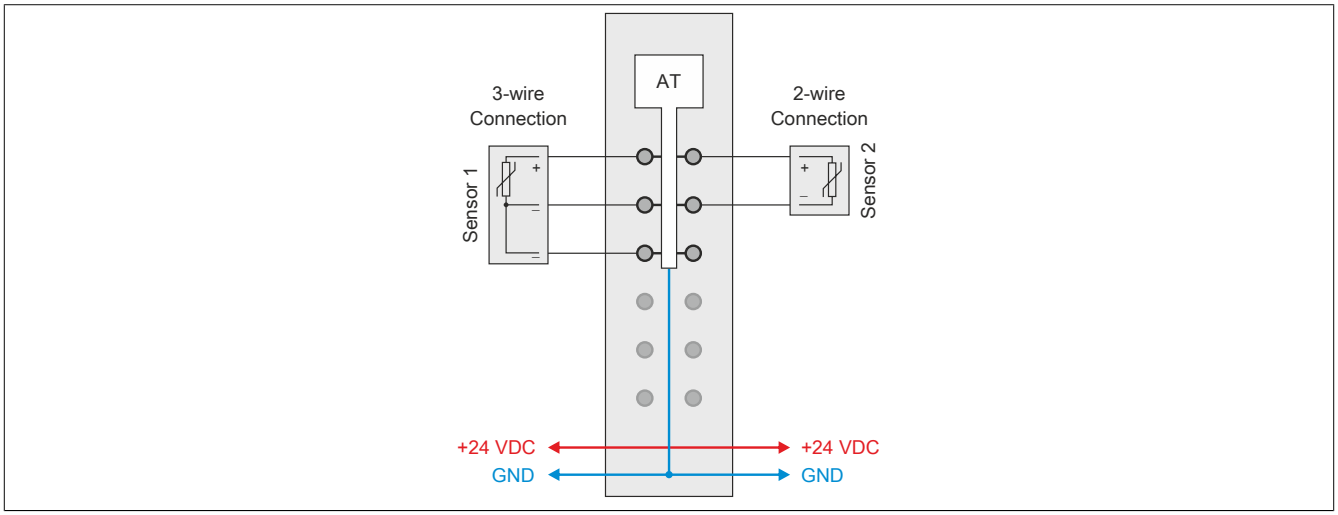
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel. Overflow or underflow of the analog inputs.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	The input is switched off
			Blinking	Overflow, underflow or open line
			On	Analog/digital converter running, value OK

4.31.3.5 Pinout

Channels that are not being used should be disabled.

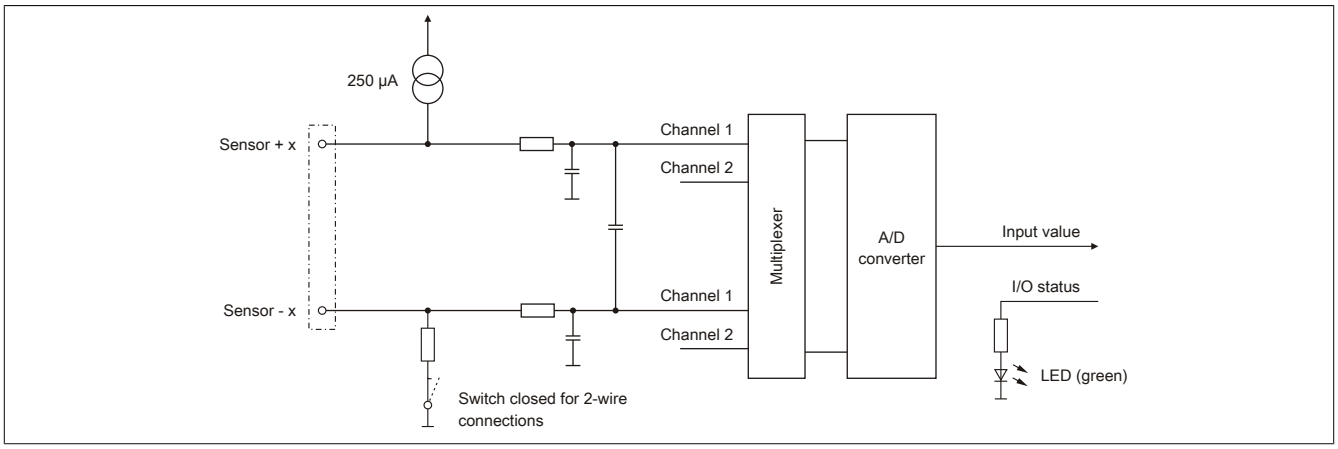


4.31.3.6 Connection example

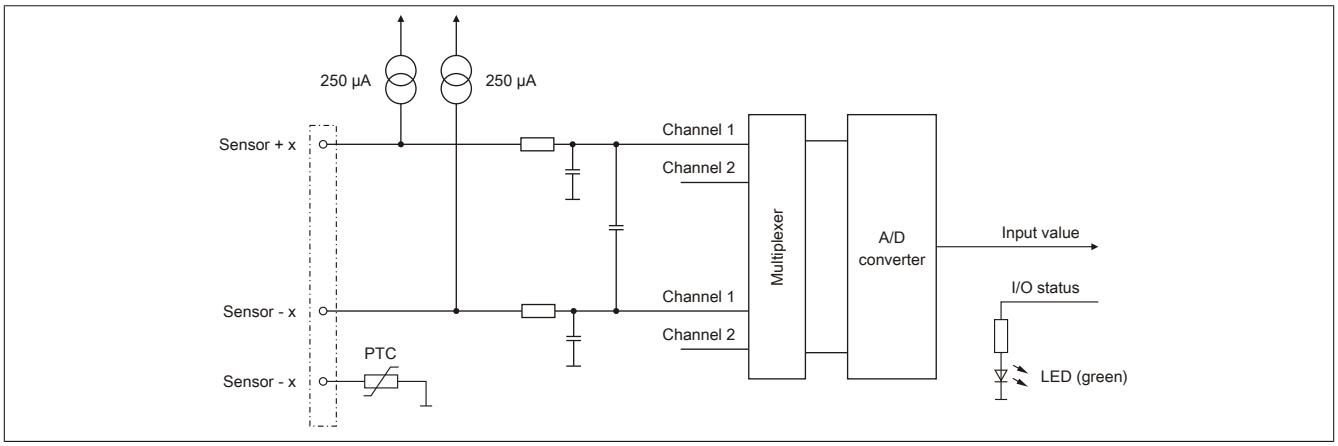


4.31.3.7 Input circuit diagram

2-wire connections



3-wire connections



4.31.3.8 Register description

4.31.3.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.3.8.2 Function model 0 - "3-wire connections" and function model 1 - "2-wire connections"

For this module, the connection type is selected using function models 0 and 1.

Function model	Connection type
0	3-wire connections (standard)
1	2-wire connections

The registers used are identical for both function models:

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigOutput01	USINT				●
18	ConfigOutput02	USINT				●
Communication						
0	Temperature01	INT	●			
	Resistor01	UINT				
2	Temperature02	INT	●			
	Resistor02	UINT				
28	IOCycleCounter	USINT	●			
30	StatusInput01	USINT	●			

4.31.3.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigOutput01	USINT				●
18	-	ConfigOutput02	USINT				●
Communication							
0	0	Temperature01	INT	●			
	0	Resistor01	UINT				
2	2	Temperature02	INT	●			
	2	Resistor02	UINT				
28	-	IOCycleCounter	USINT		●		
30	-	StatusInput01	USINT		●		

1) The offset specifies the position of the register within the CAN object.

4.31.3.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.31.3.8.4 General information

4.31.3.8.4.1 Analog inputs

This module stores converted analog values in the registers. Different resistance or temperature measurements will result in different value ranges and data types.

Information:

Operating channels outside the specification can have an effect on neighboring channels.

4.31.3.8.4.2 Timing

The timing for acquiring measurement values is determined by the converter hardware. All switched-on inputs are converted during each conversion cycle and transferred halfway through the X2X Link cycle.

4.31.3.8.4.3 Conversion time

The conversion time for the channels depends on their use. For the formulas listed in the table, "n" corresponds to the number of channels that are switched on.

Channel uses	Conversion time
1 channel	1 · Filter time
n channels with the same sensor type	n · (20 ms + Filter time)
n channels with different sensor types	n · (20 ms + 2 · Filter time)

4.31.3.8.4.4 Reduced update time

Any inputs that are not needed can be switched off, which reduces the I/O update time. Inputs can also be only switched off temporarily.

The time saved is equal to:

$$\text{Time saved} = 2 \cdot 20\ \text{ms} + \text{Filter time}$$

The filter time is the conversion time for the remaining channels.

Examples

Inputs are filtered using a 60 Hz filter.

	Example 1	Example 2
Switched on inputs	1	1 to 2
Conversion time	16.7 ms	734 ms

4.31.3.8.5 Configuration

4.31.3.8.5.1 Input filter

Name:
ConfigOutput01

This register can be used to configure the filter time for all analog inputs.

Data type	Value	Filter	Filter time
USINT	0	15 Hz	66.7 ms
	1	25 Hz	40 ms
	2	30 Hz	33.3 ms
	3	50 Hz	20 ms
	4	60 Hz	16.7 ms
	5	100 Hz	10 ms
	6	500 Hz	2 ms
	7	1000 Hz	1 ms

4.31.3.8.5.2 Sensor configuration

Name:
ConfigOutput02

This register can be used to configure the sensor type for individual channels.

This module is designed for temperature and resistance measurement. The sensor type must be specified because of the different calibration values for temperature and resistance.

The default setting for all channels is ON. To save time, individual channels can be switched off (see "Reduced update time").

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Channel 1	0000 - 0001	Reserved
		0010	PT100 sensor type
		0011	PT1000 sensor type
		0100	Reserved
		0101	Resistance measurement 0.1 to 4500 Ω
		0110	Resistance measurement 0.05 to 2250 Ω
		1111	Channel disabled
4 - 7	Channel 2	0000 - 0001	Reserved
		0010	PT100 sensor type
		0011	PT1000 sensor type
		0100	Reserved
		0101	Resistance measurement 0.1 to 4500 Ω
		0110	Resistance measurement 0.05 to 2250 Ω
		1111	Channel disabled

4.31.3.8.6 Communication

4.31.3.8.6.1 Analog input values

Name:
Temperature01 to Temperature02
Resistor01 to Resistor02

This register is used to indicate the analog input values depending on the configured operating mode.

Data type	Digital value	Input signal
INT	-2000 to 8500 (for -200.0 to 850.0°C)	PT100 sensor type
	-2000 to 8500 (for -200.0 to 850.0°C)	PT1000 sensor type
UINT	1 to 45000 (resolution 0.1 Ω)	Resistance measurement 0.1 to 4500 Ω
	1 to 45000 (resolution 0.05 Ω)	Resistance measurement 0.05 to 2250 Ω

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is not switched on, 0x8000 is output.

4.31.3.8.6.2 I/O cycle counter

Name:
IOCycleCounter

The cyclic counter increases after all input data has been updated.

Data type	Value	Information
USINT	0 to 255	Repeating counter

4.31.3.8.6.3 Input status

Name:
StatusInput01

The module's inputs are monitored. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7		0	

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs.

Error status	Temperature measurement Digital value for error	Resistance measurement Digital value for error
Open line	32767 (0x7FFF)	65535 (0xFFFF)
Upper limit value exceeded	32767 (0x7FFF)	65535 (0xFFFF)
Lower limit value exceeded	-32767 (0x8001)	0 (0x0000)
Invalid value	-32768 (0x8000)[1)] 32767 (0x7FFF)[2)] 65535 (0xFFFF)[3)]	65535 (0xFFFF)

1) Default value or channel was disabled in the I/O configuration.
2) After switching off the channel during operation.
3) Value in function model 254 - Bus controller.

4.31.3.8.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.31.3.8.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
1 input	Equal to the filter time
2 inputs	2 · 20 ms + filter time

4.31.4 X20AT2311

4.31.4.1 General information

The module is equipped with 2 inputs for PT100 4-line resistance temperature measurement.

- 2 inputs for resistance temperature measurement
- PT100 sensor
- Direct resistance measurement
- 4-wire measurement
- Configurable filter time

4.31.4.2 Order data

Model number	Short description	Figure
	Temperature measurement	
X20AT2311	X20 temperature input module, 2 inputs for resistance measurement, PT100, resolution 0.001°C, 4-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 691: X20AT2311 - Order data

4.31.4.3 Technical data

Product ID	X20AT2311
Short description	
I/O module	2 inputs for PT100 resistance temperature measurement
General information	
B&R ID code	0xA4AA
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.35 W
Internal I/O	0.85 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2	Yes
KC	Yes
GOST-R	Yes
Temperature inputs resistance measurement	
Input	Resistance measurement with constant current supply for 4-wire connections
Digital converter resolution	24-bit
Filter time	Configurable between 1 ms and 400 ms
Conversion time	
1000 Hz filter	1 ms for all inputs
50 Hz filter	20 ms for all inputs
Conversion procedure	Sigma-delta
Output format	DINT or UDINT for resistance measurement
Resistance measurement range	0.5 to 390 Ω
Temperature sensor resolution	1 LSB = 0.001°C

Table 692: X20AT2311 - Technical data

Product ID	X20AT2311
Resistance measurement resolution	0.001 Ω
Input filter	1st-order low pass / cutoff frequency 1050 Hz
Sensor standard	IEC/EN 60751
Isolation voltage between channel and bus	500 V_{eff}
Isolation voltage between channel and channel	500 V_{eff}
Linearization method	Internal
Measuring current	1 mA
Temperature sensor standardization	-200 to 850°C
Reference	1568 Ω ±0.1%
Temperature measurement range	-200 to 850°C
Permitted input signal	Short-term max. 28.8 V
Max. error at 25°C [1]	
Gain	0.0059% [2]
Offset	0.0015% [3]
Max. gain drift	<0.00065% per °C [2]
Max. offset drift	<0.000025% per °C [3]
Non-linearity	<0.001% [3]
Standardized value range for resistance measurement	0.5 Ω to 390.0 Ω
Temperature measurement monitoring	
Range exceeded (neg.)	0x80000001
Above upper range limit	0x7FFFFFFF
Open line	0x7FFFFFFF
General error	0x80000000
Open inputs	0x7FFFFFFF
Resistance measurement monitoring	
Range exceeded (neg.)	0x80000001
Above upper range limit	0xFFFFFFFF
Open line	0xFFFFFFFF
General error	0x80000000
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 692: X20AT2311 - Technical data

1) To ensure accuracy, a ZF0000 dummy module must be inserted on the left and right of the AT2311 module.
2) Based on the current resistance value.
3) Based on the entire resistance measurement range.

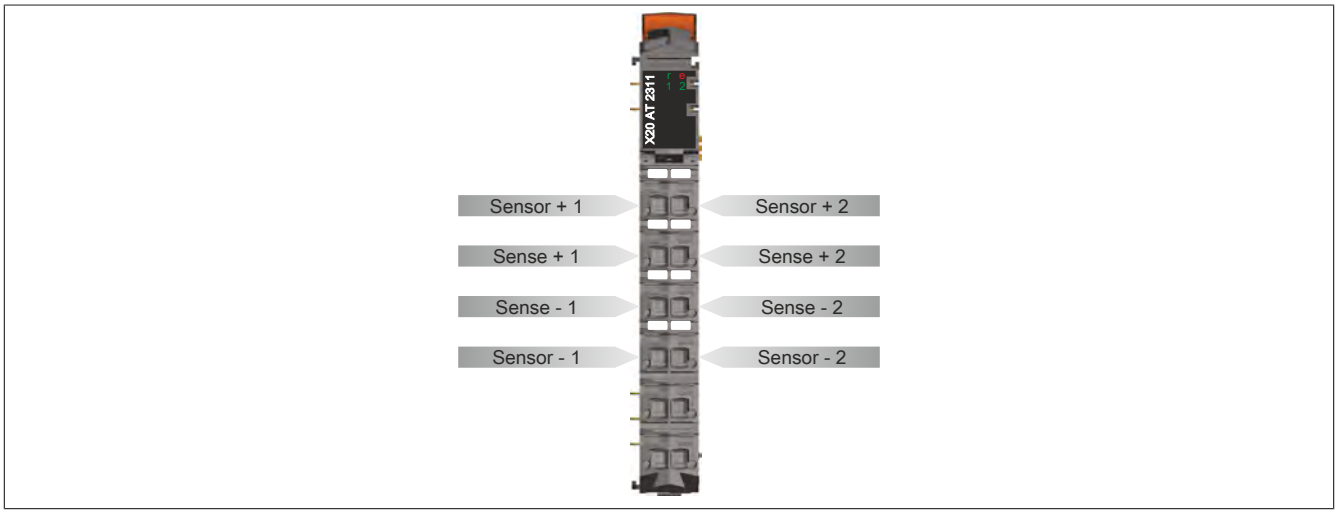
4.31.4.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel. Overflow or underflow of the analog inputs.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	The input is switched off
			Blinking	Overflow, underflow or open line
			On	Analog/digital converter running, value OK

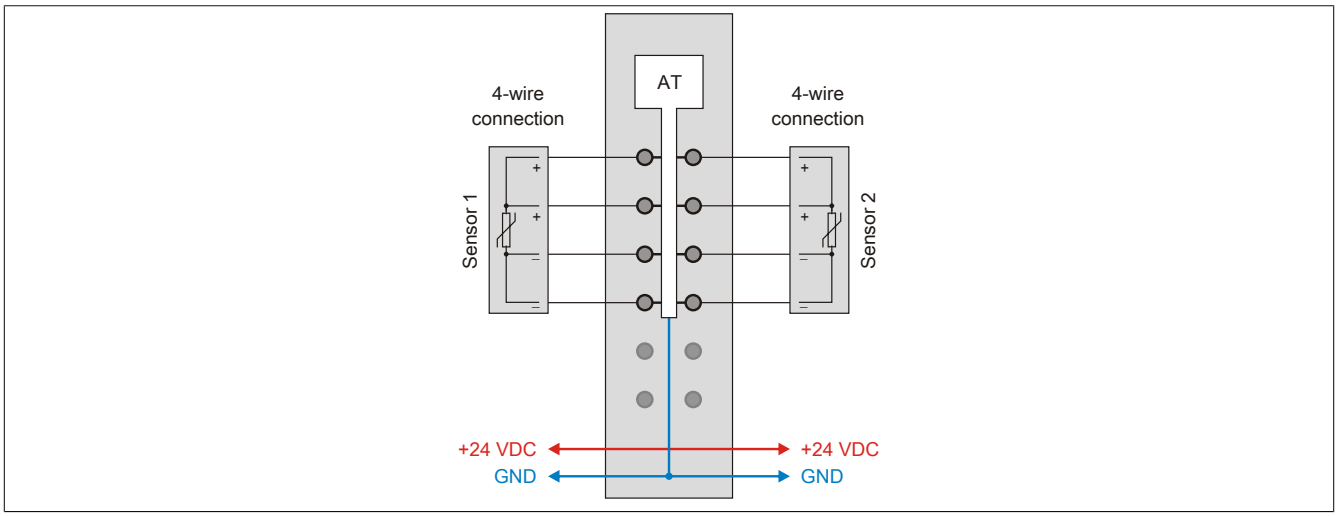
1) Depending on the configuration, a firmware update can take up to several minutes.

4.31.4.5 Pinout

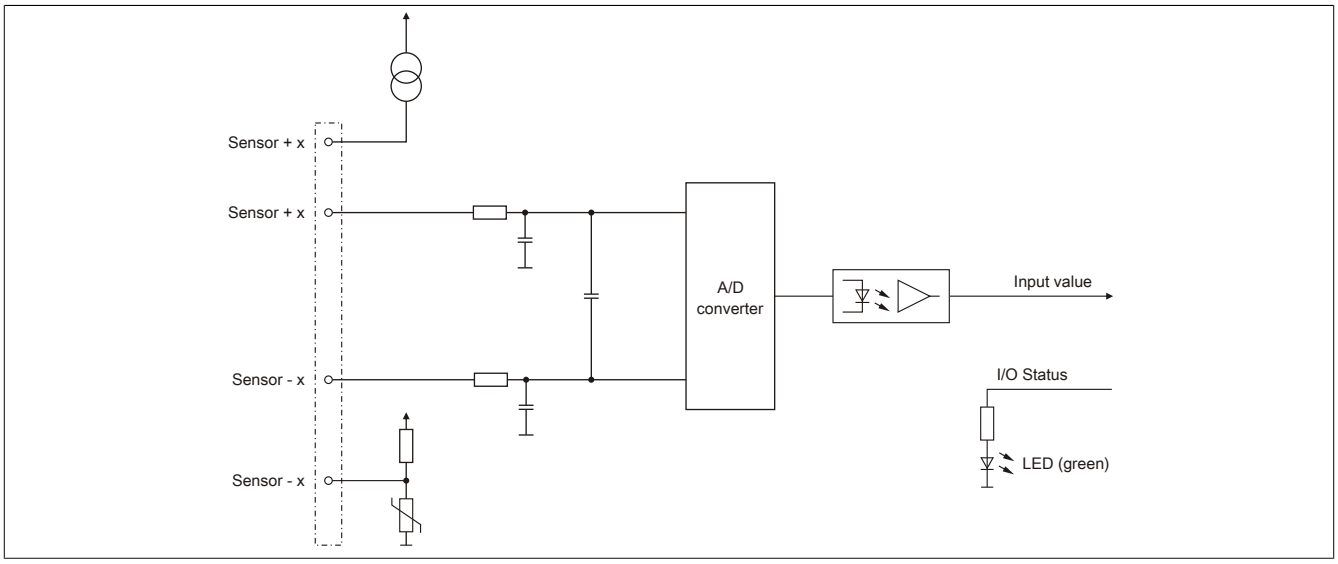


4.31.4.6 Connection example

To ensure accuracy, a ZF dummy module must be inserted on the left and right of the module.



4.31.4.7 Input circuit diagram



4.31.4.8 Register description

4.31.4.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.4.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2308	Temperature01	DINT	•			
	Resistor01	UDINT				
2316	Temperature02	DINT	•			
	Resistor02	UDINT				
2049	ConfigOutput01	USINT				•
2051	ConfigOutput02	USINT				•
2337	IOCycleCounter	USINT	•			
2345	StatusInput01	USINT	•			

4.31.4.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
0	0	Temperature01	DINT	•			
		Resistor01	UDINT				
4	4	Temperature02	DINT	•			
		Resistor02	UDINT				
2049	-	ConfigOutput01	USINT				•
2051	-	ConfigOutput02	USINT				•
2337	-	IOCycleCounter	USINT		•		
2345	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

4.31.4.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.31.4.8.4 General information

4.31.4.8.4.1 Timing

The timing for acquiring measurement values is determined by the converter hardware. All switched-on inputs are converted during each conversion cycle and transferred halfway through the X2X Link cycle.

4.31.4.8.4.2 Conversion time

The conversion time for the channels depends on the filter time configured in the 4.31.4.8.5.1 "ConfigOutput1" register.

Channel uses	Conversion time
All channels independent of the configuration	1x filter time

4.31.4.8.4.3 Ratio of filter time to resolution

The following table shows the maximum frequency with which the specified resolution can be achieved.

Filter / Filter time	Resolution
5 Hz / 200 ms	0001°C
50 Hz / 20 ms	001°C
1000 Hz / 1 ms	01°C

4.31.4.8.5 Configuration

4.31.4.8.5.1 Input filter

Name:
ConfigOutput01

This register can be used to configure the filter time for all analog inputs.

Data type	Value	Filter	Filter time
USINT	0	15 Hz	66.7 ms
	1	25 Hz	40 ms
	2	30 Hz	33.3 ms
	3	50 Hz	20 ms
	4	60 Hz	16.7 ms
	5	100 Hz	10 ms
	6	500 Hz	2 ms
	7	1000 Hz	1 ms
	8	10 Hz	100 ms
	9	5 Hz	200 ms
	19	25 Hz	400 ms

4.31.4.8.5.2 Sensor type and channel disabling

Name:
ConfigOutput02

This register can be used to configure the sensor type for individual channels.

This module is designed for temperature and resistance measurement. The sensor type must be specified because of the different calibration values for temperature and resistance.

The default setting for all channels is ON.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Channel 1	0000	Reserved
		0001	Sensor type PT100, resolution 1 mK
		0010	Resistance measurement 0.5 Ω to 390 Ω, resolution 1 mΩ
		0011 to 0110	Reserved
		0111	Channel disabled
		1xxx	Reserved
4 - 7	Channel 2	0000	Reserved
		0001	Sensor type PT100, resolution 1 mK
		0010	Resistance measurement 0.5 Ω to 390 Ω, resolution 1 mΩ
		0011 to 0110	Reserved
		0111	Channel disabled
		1xxx	Reserved

4.31.4.8.6 Communication

4.31.4.8.6.1 Analog measurement inputs

Name:
Temperatur01 to Temperatur02
Resistor01 to Resistor02

These registers are used to indicate the analog input values depending on the configured operating mode. Different resistance or temperature measurements will result in different value ranges and data types.

Name	Data type	Input signal	Digital value
Temperatur01 to Temperatur02	DINT	PT100 sensor type	-200000 to +850000 (for -200 to +850°C)
Resistor01 to Resistor02	UDINT	Resistance measurement 0.5 to 390 Ω	500 to 390000 (resolution 0.001 Ω)

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x80000000 is output.
- After switching the sensor type, 0x80000000 is output until the first conversion.
- If the input is not switched on, 0x80000000 is output.

4.31.4.8.6.2 I/O cycle counter

Name:
IOCycleCounter

The cyclic counter increases after all input data has been updated.

Data type	Value	Information
USINT	0 to 255	Repeating counter

4.31.4.8.6.3 Input status

Name:
StatusInput01

The module's inputs are monitored. A change in the monitoring status generates an error message.

After an error, it takes about 15 filter times until a valid value is available again.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

Analog value in the event of error

In addition to the status info, the error type also sets the analog value as follows:

Error status	Temperature measurement - Digital value for error	Resistance measurement - Digital value for error
Open line	+2147483647 (0x7FFFFFFF)	+4294967295 (0xFFFFFFFF)
Upper limit value exceeded	+2147483647 (0x7FFFFFFF)	+4294967295 (0xFFFFFFFF)
Lower limit value exceeded	-2147483647 (0x80000001)	-2147483647 (0x80000001)
Invalid value	-2147483648 (0x80000000)	-2147483648 (0x80000000)

4.31.4.8.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.31.4.8.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1x filter time

4.31.5 X20AT2402

4.31.5.1 General information

The module is equipped with 2 inputs for J, K, N, S, B and R thermocouple sensors. The module has an integrated terminal temperature compensation.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 inputs for thermocouples
- For sensor types J, K, N, S, B, R
- Additional direct raw value measurement
- Integrated terminal temperature compensation
- Configurable filter time

4.31.5.2 Order data

Model number	Short description	Figure
	Temperature measurement	
X20AT2402	X20 temperature input module, 2 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 693: X20AT2402 - Order data

4.31.5.3 Technical data

Product ID	X20AT2402
Short description	
I/O module	2 inputs for thermocouples
General information	
B&R ID code	0x1BA8
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.72 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
cCSAus HazLoc Class 1 Division 2	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Thermocouple temperature inputs	
Input	Thermocouple
Digital converter resolution	16-bit
Filter time	Configurable between 1 ms and 66.7 ms
Conversion time	
1 channel	80.4 ms with 50 Hz filter
2 channels	120.6 ms with 50 Hz filter
Output format	INT
Measurement range	
Sensor temperature	
Type J: Fe-CuNi	-210 to 1200°C
Type K: NiCr-Ni	-270 to 1372°C
Type N: NiCrSi-NiSi	-270 to 1300°C (Rev. ≥D0)
Type S: PtRh10-Pt	-50 to 1768°C
Type B: PtRh30-PtRh6	0 to 1820°C
Type R: PtRh13-Pt	-50 to 1664°C
Terminal temperature	-25 to 85°C
Raw value	±65.534 mV
Terminal temperature compensation	Internal
Sensor standard	EN 60584
Resolution	
Sensor temperature	1 LSB = 0.1°C
Terminal temperature	1 LSB = 0.1°C
Raw value output with respect to gain	1 LSB = 1 µV or 2 µV
Normalization	
Type J	-210 to 1200.0°C
Type K	-270 to 1372°C
Type N (Rev. ≥ D0)	-270 to 1300°C
Type S	-50 to 1768°C
Type B	0 to 1820°C
Type R	-50 to 1664°C
Terminal temperature	-25 to 85°C
Monitoring	
Range exceeded (neg.)	0x8001
Above upper range limit	0x7FFF
Open line	0x7FFF
Open inputs	0x7FFF
General error	0x8000
Conversion procedure	Sigma-delta
Linearization method	Internal
Permitted input signal	Max. ±5 V
Input filter	1st-order low pass / cutoff frequency 500 Hz

Table 694: X20AT2402 - Technical data

Product ID	X20AT2402
Max. error at 25°C	
Gain	0.06% 2)
Offset	
Type J	0.04% 3)
Type K	0.05% 3)
Type N (Rev. ≥ D0)	0.05% 3)
Type S	0.11% 3)
Type B	0.13% 3)
Type R	0.09% 3)
Max. gain drift	0.01 %/°C 2)
Max. offset drift	
Type J	0.0019 %/°C 3)
Type K	0.0024 %/°C 3)
Type N (Rev. ≥ D0)	0.0029 %/°C 3)
Type S	0.0079 %/°C 3)
Type B	0.0114 %/°C 3)
Type R	0.0074 %/°C 3)
Nonlinearity	±0.001% 3)
Common-mode rejection	
DC	>70 dB
50 Hz	>70 dB
Common-mode range	±15 V
Crosstalk between channels	<-70 dB
Isolation voltage	
Between channel and bus	500 V_{eff}
Terminal temperature compensation precision	
With artificial convection	±4°C after 10 min
With natural convection	±2°C after 10 min
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	0 to 55°C
Vertical installation	0 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 694: X20AT2402 - Technical data

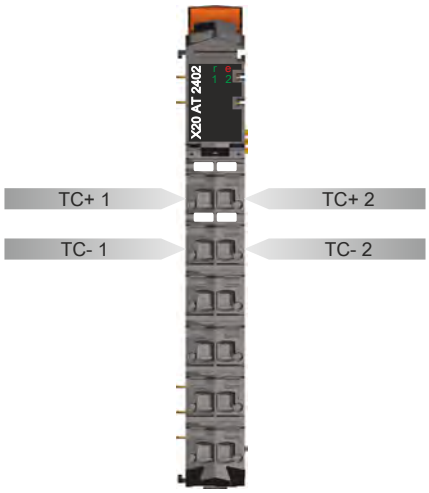
1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current measured value.
3) Based on the entire measurement range.

4.31.5.4 LED status indicators

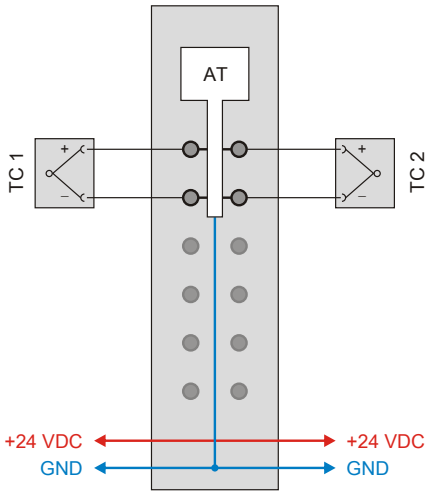
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel. Overflow or underflow of the analog inputs.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	The input is switched off
			Blinking	Overflow, underflow or open line
			On	Analog/digital converter running, value OK

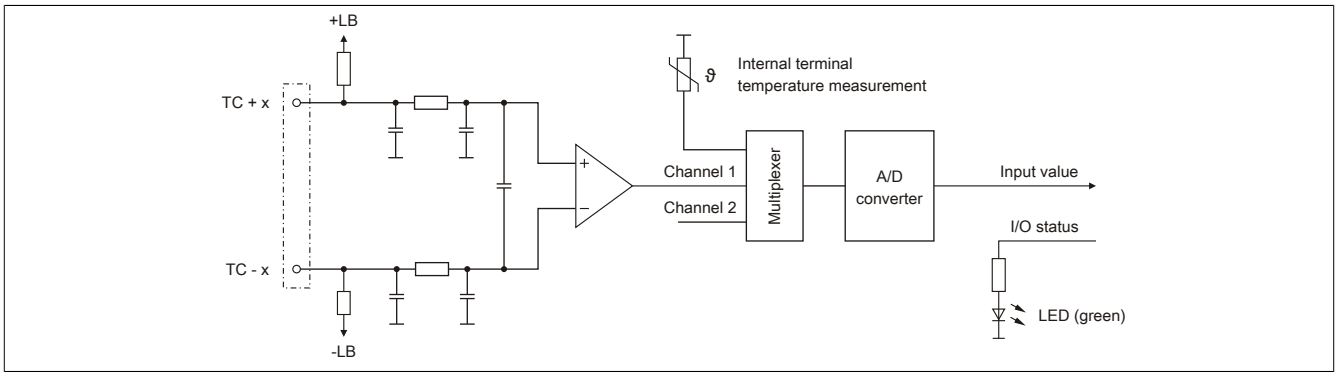
4.31.5.5 Pinout



4.31.5.6 Connection example

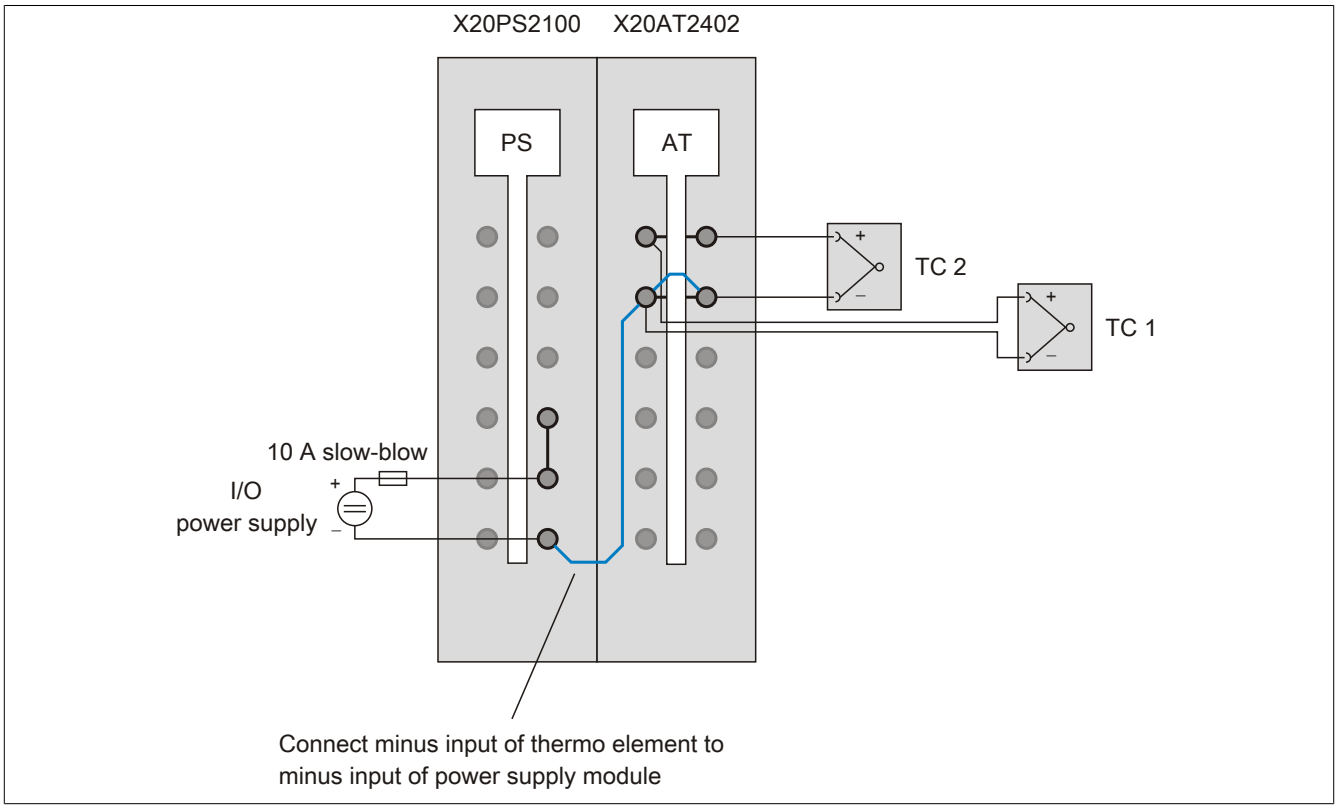


4.31.5.7 Input circuit diagram



4.31.5.8 Ceramic heating element with integrated thermo elements

We recommend connecting the minus input of the thermo element to the minus input of the supply feed module. This prevents potential measurement errors caused by ripple voltage effects in the measurement signal.



4.31.5.9 External cold junction

General information

An external cold junction temperature value can be predefined for the module for measurement value correction. This makes it possible to set up an external cold junction. The same external cold junction temperature is used for measurement value correction on all channels.

An external cold junction makes sense in the following applications and situations:

- Large distances between the controller and measurement point
- To increase precision

To bridge large distances

Setting up an external cold junction is recommended when there are large distances between the controller and the measurement point. The thermocouple voltage is routed from the external cold junction to the terminal on the X20AT2402 via copper wires. The temperature measured at the external cold junction (e.g. with PT100 - X20AT2222) is stored in the I/O area of the X20AT2402 module. The X20AT2402 uses the measured voltage and the cold junction temperature to internally calculate the needed thermocouple temperature.

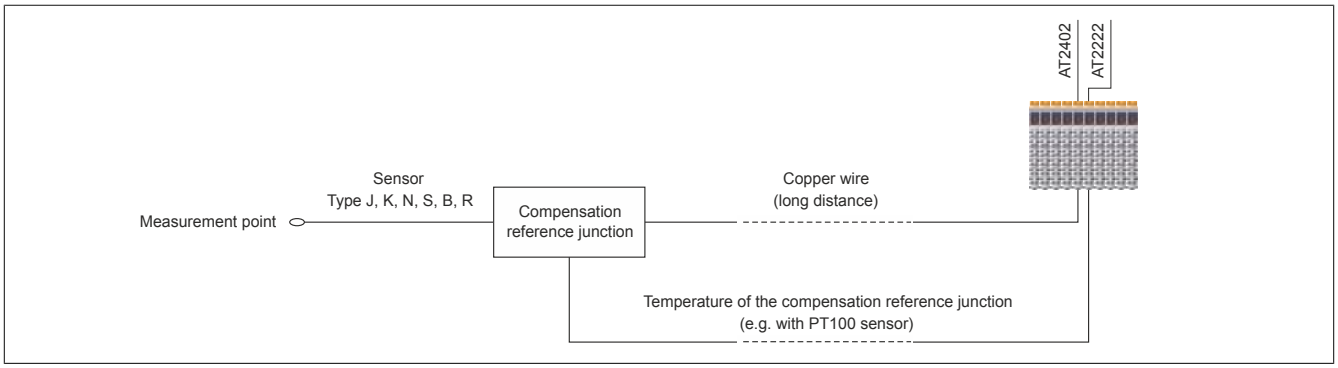


Figure 525: External cold junction for bridging large distances

Increased precision

Setting up an external cold junction is recommended to increase precision. The external cold junction is set up as described above. The installation of an external cold junction is especially helpful in the following cases:

- A module consuming more power than 1 W is connected in addition to the X20AT2402.
- No modules but the X20AT2402 are connected
- With strongly fluctuating ambient conditions (draft, temperature)

4.31.5.10 Register description

4.31.5.10.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.5.10.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
24	ConfigOutput01	USINT				●
26	ConfigOutput02	USINT				●
27	ConfigOutput03	USINT				●
Communication						
0	Temperature01	INT	●			
2	Temperature02	INT	●			
28	IOCycleCounter	USINT	●			
30	StatusInput01	USINT	●			
14	CompensationTemperature	INT		●		

4.31.5.10.3 Function model 1 - External cold junction temperature

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
24	ConfigOutput01	USINT				●
26	ConfigOutput02	USINT				●
27	ConfigOutput03	USINT				●
Communication						
12	ExternalCompensationTemperature	INT			●	
0	Temperature01	INT	●			
2	Temperature02	INT	●			
28	IOCycleCounter	USINT	●			
30	StatusInput01	USINT	●			

4.31.5.10.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
24	-	ConfigOutput01	USINT				●
26	-	ConfigOutput02	USINT				●
27	-	ConfigOutput03	USINT				●
Communication							
0	0	Temperature01	INT	●			
2	2	Temperature02	INT	●			
28	-	IOCycleCounter	USINT		●		
30	-	StatusInput01	USINT		●		
14	-	CompensationTemperature	INT		●		

1) The offset specifies the position of the register within the CAN object.

4.31.5.10.4.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.31.5.10.5 General information

4.31.5.10.5.1 Raw value measurement

If a sensor type other than J, K, N, S, B or R is used, the terminal temperature must be measured on at least one input. Based on this value, the user must then implement terminal temperature compensation.

4.31.5.10.5.2 Timing

The timing for acquiring measurement values is determined by the converter hardware. All enabled inputs are converted during each conversion cycle. In addition, the terminal temperature is measured (not in function model 1).

Any inputs that are not needed can be switched off, which reduces the I/O update time. Inputs can also be only switched off temporarily. Measuring the terminal temperature is switched off in function model 1.

4.31.5.10.5.3 Conversion time

The conversion time depends on the number of channels and the function model. For the formulas listed in the table, "n" corresponds to the number of channels that are switched on.

Function model	Conversion time
Model 0 - n channels	(n + 1) · (2 · Filter time + 200 µs)
Model 1 - n channels	n · (2 · Filter time + 200 µs)
Model 1 - 1 channel	Equal to the filter time

Examples

Inputs are filtered using a 50 Hz filter.

	Example 1		Example 2	
	Function model 0	Function model 1	Function model 0	Function model 1
Switched on inputs	1	1	1 - 2	1 - 2
Input conversion times	40.2 ms	20 ms	80.4 ms	80.4 ms
Conversion time for the terminal temperature	40.2 ms	-	40.2 ms	-
Total conversion time	80.4 ms	20 ms	120.6 ms	80.4 ms

4.31.5.10.6 Configuration

4.31.5.10.6.1 Input filter and ambient conditions

Name:
ConfigOutput01

This register configures input filters and ambient conditions.

Input filter

The filter time for all analog inputs is defined using the input filter parameter.

Value	Filter	Filter time	Digital converter resolution
0	15 Hz	66.7 ms	16-bit
1	25 Hz	40 ms	16-bit
2	30 Hz	33.3 ms	16-bit
3	50 Hz	20 ms	16-bit
4	60 Hz	16.7 ms	16-bit
5	100 Hz	10 ms	16-bit
6	500 Hz	2 ms	16-bit
7	1000 Hz	1 ms	16-bit

Environmental conditions

Ambient conditions are set in order to adjust the internal terminal temperature characteristic curve to the type and amount of generated heat dissipated to the module.

This selection is based on the power consumption of the modules connected immediately to the left and right on the X2X Link. Power consumption values can also be found in the technical data for the corresponding module. The higher value is used for the configuration.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Filter time	0000	15 Hz
		0001	25 Hz
		0010	30 Hz
		0011	50 Hz
		0100	60 Hz
		0101	100 Hz
		0110	500 Hz
		0111	1000 Hz
		1000 to 1111	Not permitted
4 - 7	Environmental conditions	0000	Default, no calculation for adjustment
		0001	Power dissipation less than 0.2 W
		0010	Power dissipation less than 1 W
		0011	Power dissipation more than 1 W
		0100 to 1111	Not permitted

4.31.5.10.6.2 Sensor type

Name:
ConfigOutput02

This module is designed for a wide range of sensor types. The sensor type must be configured because of the different alignment values.

Data type	Value	Information
USINT	0	Conversion switched off
	1	Sensor type J
	2	Sensor type K
	3	Sensor type S
	4	Sensor type N
	5	Conversion switched off
	6	Raw value without linearization and terminal temperature compensation: Resolution 1.0625 µV for a measurement range of ±35 mV
	7	Raw value without linearization and terminal temperature compensation: Resolution 2.125 µV for a measurement range of ±70 mV
	8 - 63	Conversion switched off
	64	Sensor type R
	65 - 71	Conversion switched off
	72	Sensor type B
	73 - 255	Conversion switched off

4.31.5.10.6.3 Channel disabling

Name:
ConfigOutput03

By default, all channels are switched on. To save time, individual channels can be switched off (see "Conversion time" on page 2964).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Off
		1	On
1	Channel 2	0	Off
		1	On
2 - 7	Reserved	0	

4.31.5.10.7 Communication

4.31.5.10.7.1 Analog inputs

Name:
Temperature01 to Temperature02

Analog input value depending on the configured sensor type:

Input signal	Digital value
Type J (FeCuNi)	-2100 to +12000 (for -210.0°C to +1200.0°C)
Type K (NiCrNi)	-2700 to +13720 (for -270.0°C to +1372.0°C)
Type N (NiCrSi)	-2700 to +13000 (for -270.0°C to +1300.0°C)
Type S (PtRhPt)	-500 to +17680 (for -50.0°C to +1768.0°C)
Type B (PtRhPt)	0 to +18200 (for 0°C to +1820.0°C)
Type R (PtRhPt)	-500 to +16640 (for -50.0°C to +1664.0°C)
Raw value without linearization and terminal temperature compensation: Resolution 1.0625 µV for a measurement range of ±35 mV	-32,768 to +32,767
Raw value without linearization and terminal temperature compensation: Resolution 2.125 µV for a measurement range of ±70 mV	-32,768 to +32,767

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is not switched on, 0x8000 is output.

4.31.5.10.7.2 I/O cycle counter

Name:
IOCycleCounter

The cyclic counter increases after all input data has been updated.

Data type	Value	Information
USINT	0 to 255	Repeating counter

4.31.5.10.7.3 Input status

The module's inputs are monitored. A change in the monitoring status generates an error message.

In addition to the status info, the error type also sets the analog value as follows:

Error status	Digital value for error
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

Name:
StatusInput01

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

4.31.5.10.7.4 Reads the internal cold junction temperature

Name:
CompensationTemperature

The internal cold junction temperature is stored in this register.

Data type	Value	Information
INT	-250 to 850	Internal cold junction temperature (PT1000): -25.0 to 85.0°C

4.31.5.10.7.5 Defines the external cold junction temperature

Name:
ExternalCompensationTemperature

The external cold junction temperature is defined in this register.

Data type	Value	Information
INT	-250 to 850	External cold junction temperature: -25.0 to 85.0°C

4.31.5.10.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.31.5.10.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

For the formulas listed in the table, 'n' corresponds to the number of channels that are switched on.

Function model 0	
n inputs	(n + 1) · (Filter time + 200 µs)

Function model 1	
1 input	Equal to the filter time
n inputs	n · (Filter time + 200 µs)

4.31.6 X20(c)AT4222

4.31.6.1 General information

The module is equipped with 4 inputs for PT100/PT1000 resistance temperature measurement.

- 4 inputs for resistance temperature measurement
- For PT100 and PT1000
- Configurable sensor type per channel
- Direct resistance measurement
- Configurable 2- or 3- wire connections per module
- Configurable filter time

4.31.6.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.31.6.3 Order data

Model number	Short description	Figure
	Temperature measurement	
X20AT4222	X20 temperature input module, 4 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections	
X20cAT4222	X20 temperature input module, coated, 4 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 V keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 695: X20AT4222, X20cAT4222 - Order data

4.31.6.4 Technical data

Product ID	X20AT4222	X20cAT4222
Short description		
I/O module	4 inputs for PT100 or PT1000 resistance temperature measurement	
General information		
B&R ID code	0x1BA7	0xE215
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Inputs	Yes, using status LED and software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.1 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	-
GOST-R	Yes	
Temperature inputs resistance measurement		
Input	Resistance measurement with constant current supply for 2- or 3-wire connections	
Digital converter resolution	16-bit	
Filter time	Configurable between 1 ms and 66.7 ms	
Conversion time		
1 channel	20 ms with 50 Hz filter	
2 - 4 channels	40 ms per channel with 50 Hz filter	
Conversion procedure	Sigma-delta	
Output format	INT or UINT for resistance measurement	
Sensor		
Sensor type	Configurable per channel	
PT100	-200 to 850°C	
PT1000	-200 to 850°C	
Resistance measurement range	0.1 to 4500 Ω / 0.05 to 2250 Ω	
Input filter	1st-order low pass / cutoff frequency 500 Hz	
Sensor standard	IEC/EN 60751	
Common-mode range	>0.7 V	
Isolation voltage between channel and bus	500 V_{eff}	
Linearization method	Internal	
Measuring current	250 µA ±1.25%	
Reference	4530 Ω ±0.1%	
Permitted input signal	Short-term max. ±30 V	
Max. error at 25°C		
Gain	0.037% [2]	
Offset	0.0015% [3]	
Max. gain drift	0.004% per °C [2]	
Max. offset drift	0.00015% per °C [3]	
Nonlinearity	<0.001% [3]	
Crosstalk between channels	<-93 dB	
Temperature sensor resolution		
PT100	1 LSB = 0.1°C	
PT1000	1 LSB = 0.1°C	
Resistance measurement resolution		
G = 1	0.1 Ω	
G = 2	0.05 Ω	
Common-mode rejection		
50 Hz	>80 dB	
DC	>95 dB	
Standardized value range for resistance measurement		
G = 1	0.1 to 4500 Ω	
G = 2	0.05 to 2250 Ω	
Temperature sensor normalization		
PT100	-200.0 to 850.0°C	
PT1000	-200.0 to 850.0°C	

Table 696: X20AT4222, X20cAT4222 - Technical data

Product ID	X20AT4222	X20cAT4222
Temperature measurement monitoring		
Range exceeded (neg.)	0x8001	
Above upper range limit	0x7FFF	
Open line	0x7FFF	
General error	0x8000	
Open inputs	0x7FFF	
Resistance measurement monitoring		
Above upper range limit	0xFFFF	
Open line	0xFFFF	
General error	0xFFFF	
Open inputs	0xFFFF	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	-25 to 60°C	
Vertical installation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 696: X20AT4222, X20cAT4222 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current resistance value.
3) Based on the entire resistance measurement range.

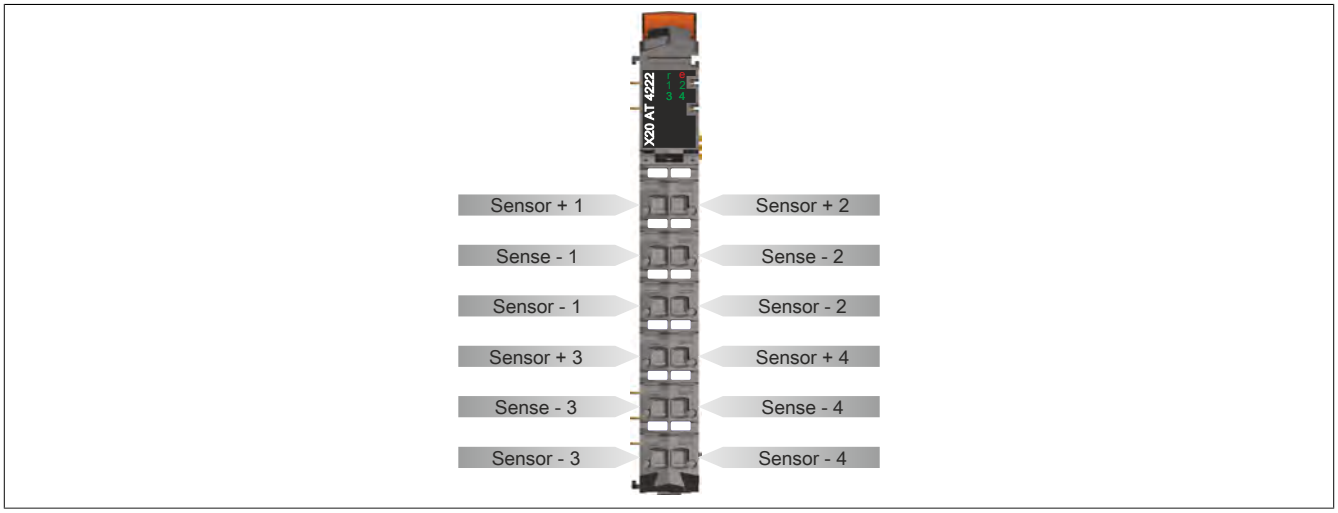
4.31.6.5 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

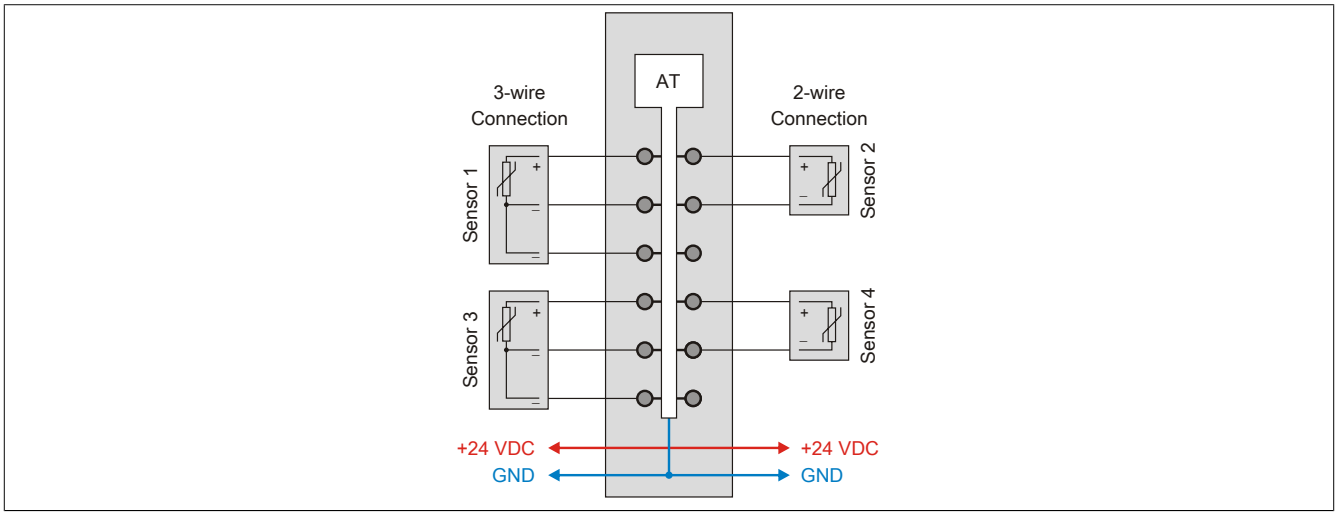
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel. Overflow or underflow of the analog inputs.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Off	The input is switched off
			Blinking	Overflow, underflow or open line
			On	Analog/digital converter running, value OK

4.31.6.6 Pinout

Channels that are not being used should be disabled.

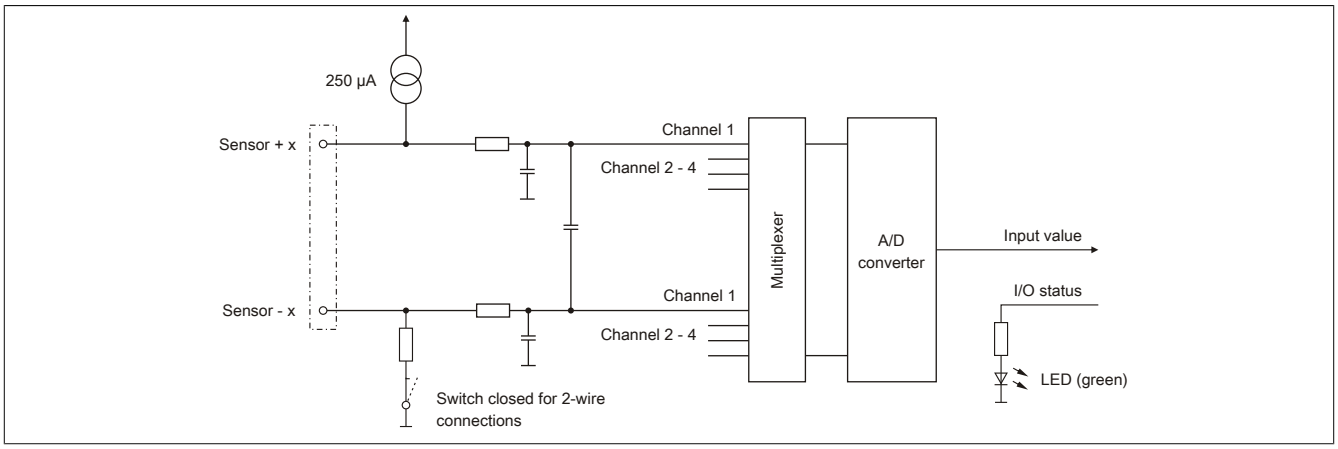


4.31.6.7 Connection example

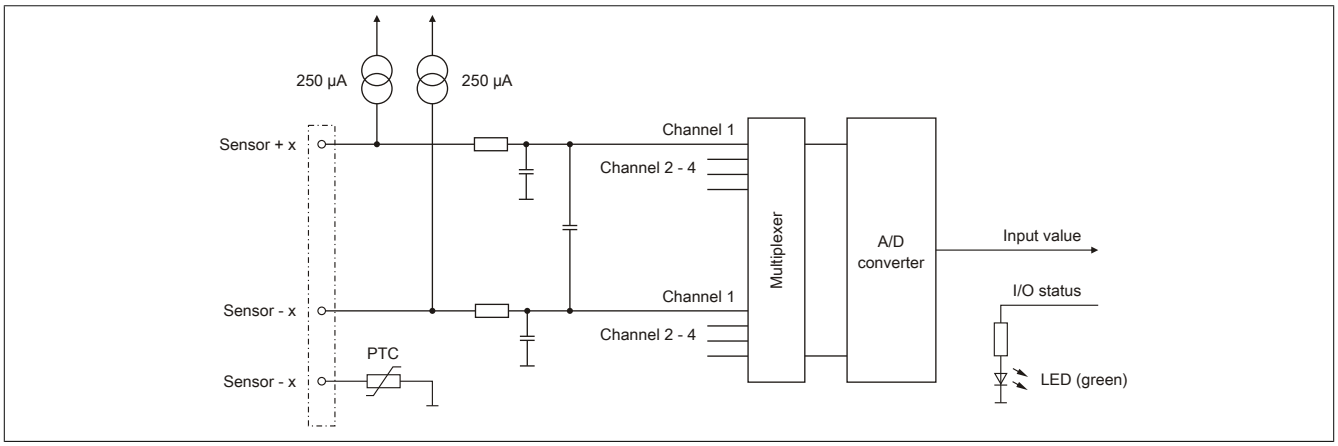


4.31.6.8 Input circuit diagram

2-wire connections



3-wire connections



4.31.6.9 Register description

4.31.6.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.6.9.2 Function model 0 - "3-wire connections" and function model 1 - "2-wire connections"

For this module, the connection type is selected using function models 0 and 1.

Function model	Connection type
0	3-wire connections (standard)
1	2-wire connections

The registers used are identical for both function models:

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigOutput01	USINT				●
18	ConfigOutput02	UINT				●
Communication						
0	Temperature01	INT	●			
	Resistor01	UINT				
2	Temperature02	INT	●			
	Resistor02	UINT				
4	Temperature03	INT	●			
	Resistor03	UINT				
6	Temperature04	INT	●			
	Resistor04	UINT				
28	IOCycleCounter	USINT	●			
30	StatusInput01	USINT	●			

4.31.6.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigOutput01	USINT				●
18	-	ConfigOutput02	UINT				●
Communication							
0	0	Temperature01	INT	●			
	0	Resistor01	UINT				
2	2	Temperature02	INT	●			
	2	Resistor02	UINT				
4	4	Temperature03	INT	●			
	4	Resistor03	UINT				
6	6	Temperature04	INT	●			
	6	Resistor04	UINT				
28	-	IOCycleCounter	USINT		●		
30	-	StatusInput01	USINT		●		

1) The offset specifies the position of the register within the CAN object.

4.31.6.9.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.31.6.9.4 General information

4.31.6.9.4.1 Analog inputs

This module stores converted analog values in the registers. Different resistance or temperature measurements will result in different value ranges and data types.

Information:

Operating channels outside the specification can have an effect on neighboring channels.

4.31.6.9.4.2 Timing

The timing for acquiring measurement values is determined by the converter hardware. All switched-on inputs are converted during each conversion cycle and transferred halfway through the X2X Link cycle.

4.31.6.9.4.3 Conversion time

The conversion time for the channels depends on their use. For the formulas listed in the table, "n" corresponds to the number of channels that are switched on.

Channel uses	Conversion time
1 channel	1 · Filter time
n channels with the same sensor type	n · (20 ms + Filter time)
n channels with different sensor types	n · (20 ms + 2 · Filter time)

4.31.6.9.4.4 Reduced update time

Any inputs that are not needed can be switched off, which reduces the I/O update time. Inputs can also be only switched off temporarily.

Calculating the time saved

The amount of time saved can be calculated with the following formula. And "n" corresponds to the number of inputs that are switched off.

$$\text{Time saved} = n \cdot (20\ \text{ms} + \text{filter time})$$

Examples

Inputs are filtered using a 60 Hz filter.

	Example 1	Example 2	Example 3
Switched on inputs	1	1 and 3	1 to 4
Conversion time	16.7 ms	73.4 ms	146.8 ms

4.31.6.9.5 Configuration

4.31.6.9.5.1 Input filter

Name:
ConfigOutput01

This register can be used to configure the filter time for all analog inputs.

Data type	Value	Filter	Filter time
USINT	0	15 Hz	66.7 ms
	1	25 Hz	40 ms
	2	30 Hz	33.3 ms
	3	50 Hz	20 ms
	4	60 Hz	16.7 ms
	5	100 Hz	10 ms
	6	500 Hz	2 ms
	7	1000 Hz	1 ms

4.31.6.9.5.2 Sensor configuration

Name:
ConfigOutput02

This register can be used to configure the sensor type for individual channels.

This module is designed for temperature and resistance measurement. The sensor type must be specified because of the different calibration values for temperature and resistance.

The default setting for all channels is ON. To save time, individual channels can be switched off (see "Reduced update time").

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 3	Channel 1	0000 - 0001	Reserved
		0010	PT100 sensor type
		0011	PT1000 sensor type
		0100	Reserved
		0101	Resistance measurement 0.1 to 4500 Ω
		0110	Resistance measurement 0.05 to 2250 Ω
		1111	Channel disabled
...		...	
12 - 15	Channel 4	0000 - 0001	Reserved
		0010	PT100 sensor type
		0011	PT1000 sensor type
		0100	Reserved
		0101	Resistance measurement 0.1 to 4500 Ω
		0110	Resistance measurement 0.05 to 2250 Ω
		1111	Channel disabled

4.31.6.9.6 Communication

4.31.6.9.6.1 Analog input values

Name:
Temperature01 to Temperature04
Resistor01 to Resistor04

This register is used to indicate the analog input values depending on the configured operating mode.

Data type	Digital value	Input signal
INT	-2000 to 8500 (for -200.0 to 850.0°C)	PT100 sensor type
	-2000 to 8500 (for -200.0 to 850.0°C)	PT1000 sensor type
UINT	1 to 45000 (resolution 0.1 Ω)	Resistance measurement 0.1 to 4500 Ω
	1 to 45000 (resolution 0.05 Ω)	Resistance measurement 0.05 to 2250 Ω

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is not switched on, 0x8000 is output.

4.31.6.9.6.2 I/O cycle counter

Name:
IOCycleCounter

The cyclic counter increases after all input data has been updated.

Data type	Value	Information
USINT	0 to 255	Repeating counter

4.31.6.9.6.3 Input status

Name:
StatusInput01

The module's inputs are monitored. A change in the monitoring status generates an error message.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs.

Error status	Temperature measurement Digital value for error	Resistance measurement Digital value for error
Open line	32767 (0x7FFF)	65535 (0xFFFF)
Upper limit value exceeded	32767 (0x7FFF)	65535 (0xFFFF)
Lower limit value exceeded	-32767 (0x8001)	0 (0x0000)
Invalid value	-32768 (0x8000)[1)] 32767 (0x7FFF)[2)] 65535 (0xFFFF)[3)]	65535 (0xFFFF)

1) Default value or channel was disabled in the I/O configuration.
2) After switching off the channel during operation.
3) Value in function model 254 - Bus controller.

4.31.6.9.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
100 µs

4.31.6.9.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
1 input	Equal to the filter time
n inputs	n · (20 ms + filter time)

4.31.7 X20(c)AT6402

4.31.7.1 General information

The module is equipped with 6 inputs for J, K, N, S, B and R thermocouple sensors. The module has an integrated terminal temperature compensation.

- 6 inputs for thermocouples
- For sensor types J, K, N, S, B, R
- Additional direct raw value measurement
- Integrated terminal temperature compensation
- Configurable filter time

4.31.7.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

4.31.7.3 Order data

Model number	Short description	Figure
	Temperature measurement	
X20AT6402	X20 temperature input module, 6 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C	
X20cAT6402	X20 temperature input module, coated, 6 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 697: X20AT6402, X20cAT6402 - Order data

4.31.7.4 Technical data

Product ID	X20AT6402	X20cAT6402
Short description		
I/O module	6 inputs for thermocouples	
General information		
B&R ID code	0x1BA9	0xDD57
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Inputs	Yes, using status LED and software	
Power consumption		
Bus	0.01 W	
Internal I/O	0.91 W	
Additional power dissipation caused by the actuators (resistive) [W]	-	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	No	
Certification		
CE	Yes	
cULus	Yes	
cCSAus HazLoc Class 1 Division 2	Yes	-
ATEX Zone 2 [1)]	Yes	
KC	Yes	-
GL	Yes	
LR	Yes	
GOST-R	Yes	
Thermocouple temperature inputs		
Input	Thermocouple	
Digital converter resolution	16-bit	
Filter time	Configurable between 1 ms and 66.7 ms	
Conversion time		
1 channel	80.4 ms with 50 Hz filter	
n channels	(n + 1) x 40.2 ms at 50 Hz filter	
Output format	INT	
Measurement range		
Sensor temperature		
Type J: Fe-CuNi	-210 to 1200°C	
Type K: NiCr-Ni	-270 to 1372°C	
Type N: NiCrSi-NiSi	-270 to 1300°C (Rev. ≥D0)	
Type S: PtRh10-Pt	-50 to 1768°C	
Type B: PtRh30-PtRh6	0 to 1820°C	
Type R: PtRh13-Pt	-50 to 1664°C	
Terminal temperature	-25 to 85°C	
Raw value	±65.534 mV	
Terminal temperature compensation	Internal	
Sensor standard	EN 60584	
Resolution		
Sensor temperature	1 LSB = 0.1°C	
Terminal temperature	1 LSB = 0.1°C	
Raw value output with respect to gain	1 LSB = 1 µV or 2 µV	
Normalization		
Type J	-210.0 to 1200.0°C	
Type K	-270.0 to 1372.0°C	
Type N (Rev. ≥ D0)	-270.0 to 1300.0°C	
Type S	-50.0 to 1768.0°C	
Type B	0 to 1820.0°C	
Type R	-50.0 to 1664.0°C	
Terminal temperature	-25.0 to 85.0°C	
Monitoring		
Range exceeded (neg.)	0x8001	
Above upper range limit	0x7FFF	
Open line	0x7FFF	
Open inputs	0x7FFF	
General error	0x8000	
Conversion procedure	Sigma-delta	
Linearization method	Internal	
Permitted input signal	Max. ±5 V	
Input filter	1st-order low pass / cutoff frequency 500 Hz	

Table 698: X20AT6402, X20cAT6402 - Technical data

Product ID	X20AT6402	X20cAT6402
Max. error at 25°C		
Gain	0.06% 2)	
Offset		
Type J	0.04% 3)	
Type K	0.05% 3)	
Type N (Rev. ≥ D0)	0.05% 3)	
Type S	0.11% 3)	
Type B	0.13% 3)	
Type R	0.09% 3)	
Max. gain drift	0.01 %/°C 2)	
Max. offset drift		
Type J	0.0019 %/°C 3)	
Type K	0.0024 %/°C 3)	
Type N (Rev. ≥ D0)	0.0029 %/°C 3)	
Type S	0.0079 %/°C 3)	
Type B	0.0114 %/°C 3)	
Type R	0.0074 %/°C 3)	
Nonlinearity	±0.001% 3)	
Common-mode rejection		
DC	>70 dB	
50 Hz	>70 dB	
Common-mode range	±15 V	
Crosstalk between channels	<-70 dB	
Isolation voltage		
Between channel and bus	500 V_{eff}	
Terminal temperature compensation precision		
With artificial convection	±4°C after 10 min	
With natural convection	±2°C after 10 min	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation at elevations above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
EN 60529 protection	IP20	
Environmental conditions		
Temperature		
Operation		
Horizontal installation	0 to 55°C	-25 to 60°C
Vertical installation	0 to 50°C	-25 to 50°C
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical characteristics		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Spacing	$12.5^{+0.2}$ mm	

Table 698: X20AT6402, X20cAT6402 - Technical data

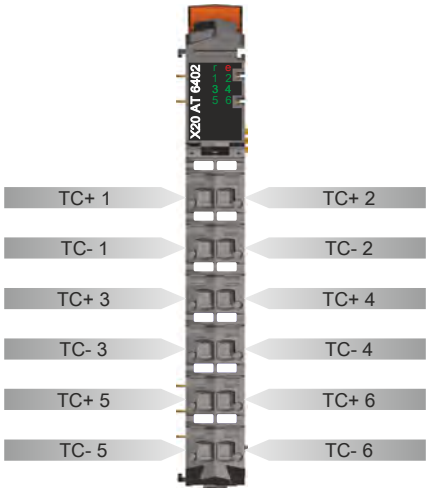
1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Based on the current measured value.
3) Based on the entire measurement range.

4.31.7.5 LED status indicators

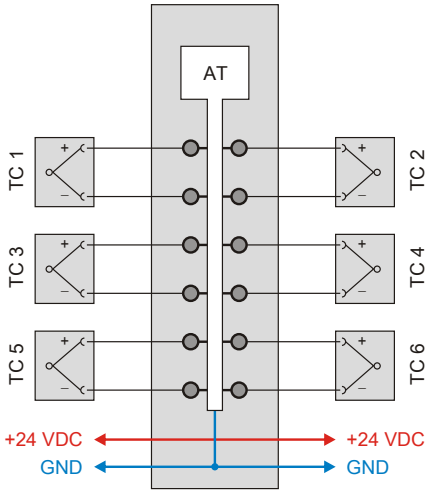
For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel. Overflow or underflow of the analog inputs.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 6	Green	Off	The input is switched off
			Blinking	Overflow, underflow or open line
			On	Analog/digital converter running, value OK

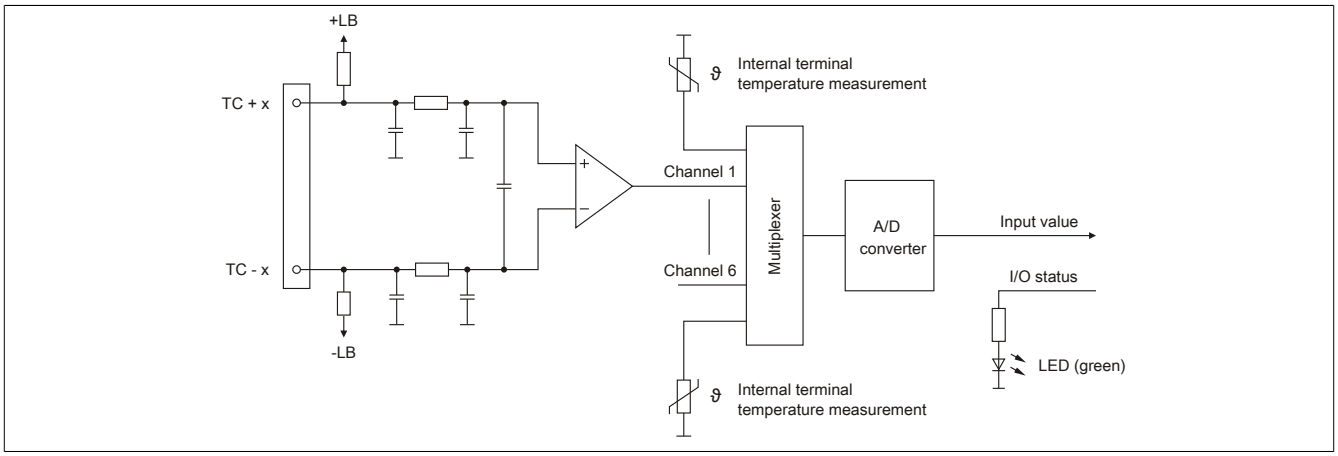
4.31.7.6 Pinout



4.31.7.7 Connection example

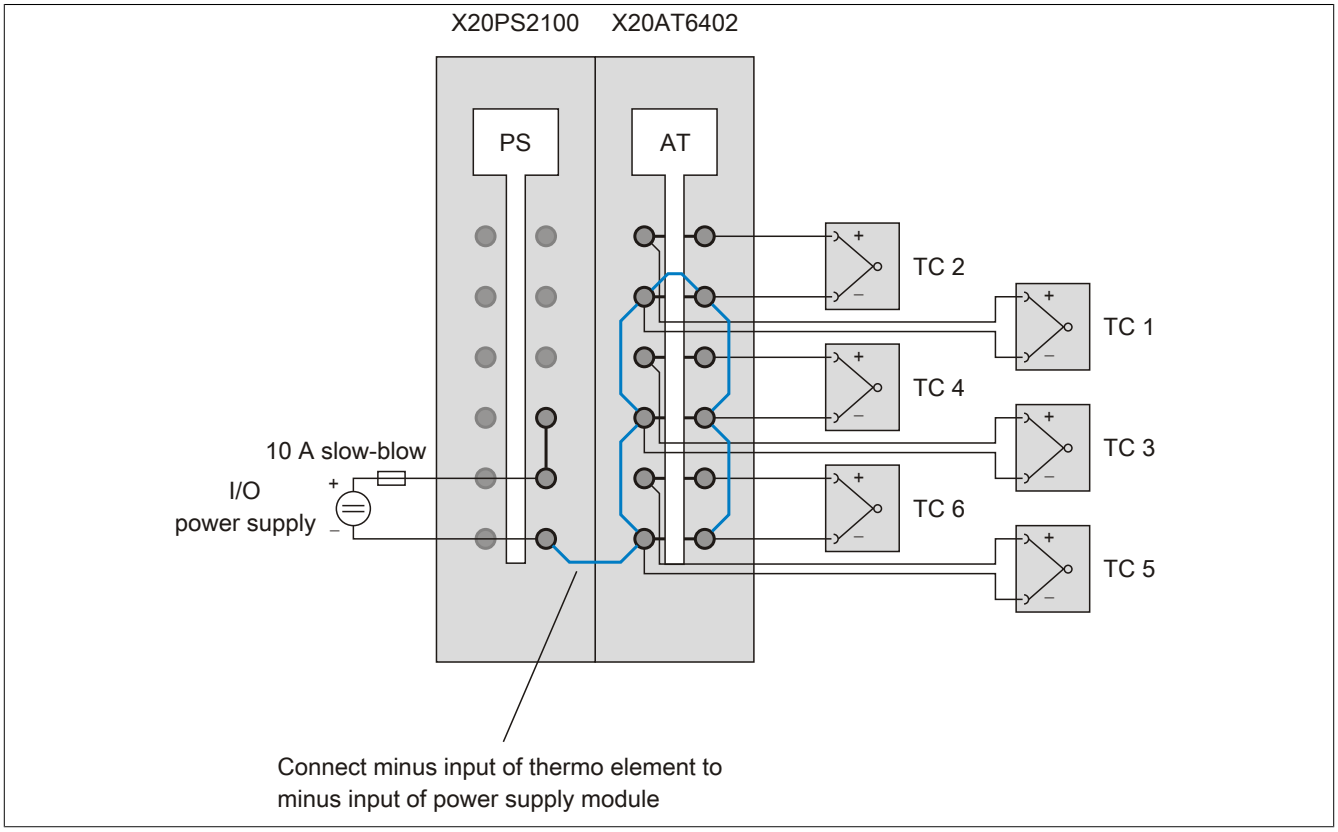


4.31.7.8 Input circuit diagram



4.31.7.9 Ceramic heating element with integrated thermo elements

We recommend connecting the minus input of the thermo element to the minus input of the supply feed module. This prevents potential measurement errors caused by ripple voltage effects in the measurement signal.



4.31.7.10 External cold junction

General information

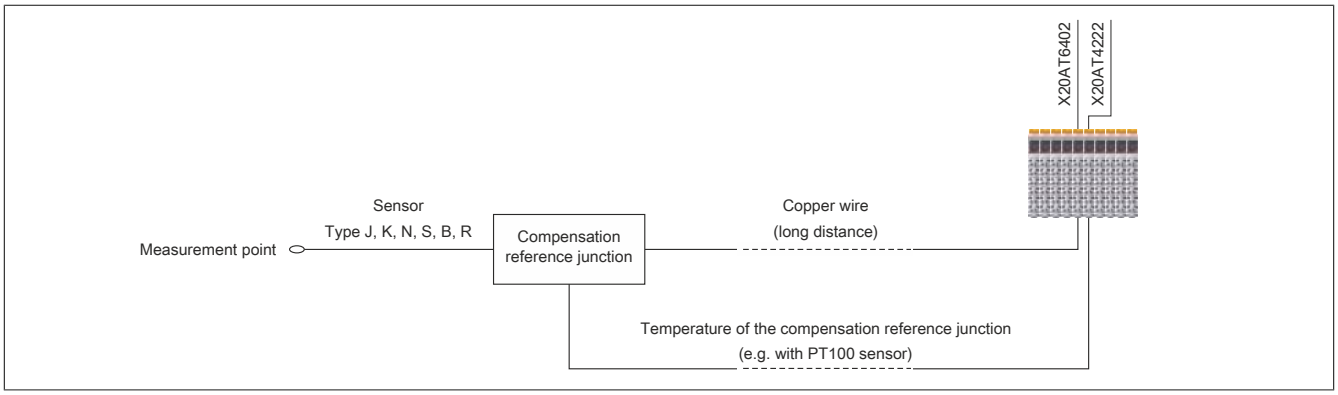
An external cold junction temperature value can be predefined for the module for measurement value correction. This makes it possible to set up an external cold junction. The same external cold junction temperature is used for measurement value correction on all channels.

An external cold junction makes sense in the following applications and situations:

- Large distances between the controller and measurement point
- To increase precision

To bridge large distances

Setting up an external cold junction is recommended when there are large distances between the controller and the measurement point. The thermocouple voltage is routed from the external cold junction to the terminal on the X20AT6402 via copper wires. The temperature measured at the external cold junction (e.g. with PT100 - X20AT4222) is stored in the I/O area of the X20AT6402 module. The X20AT6402 uses the measured voltage and the cold junction temperature to internally calculate the needed thermocouple temperature.



Increased precision

Setting up an external cold junction is recommended to increase precision. The external cold junction is set up as described above. The installation of an external cold junction is especially helpful in the following cases:

- A module consuming more power than 1 W is connected in addition to the X20AT6402.
- No modules but the X20AT6402 are connected
- With strongly fluctuating ambient conditions (draft, temperature)

4.31.7.11 Register description

4.31.7.11.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.7.11.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
24	ConfigOutput01	USINT				•
26	ConfigOutput02	USINT				•
27	ConfigOutput03	USINT				•
Communication						
0	Temperature01	INT	•			
2	Temperature02	INT	•			
4	Temperature03	INT	•			
6	Temperature04	INT	•			
8	Temperature05	INT	•			
10	Temperature06	INT	•			
28	IOCycleCounter	USINT	•			
30	StatusInput01	USINT	•			
31	StatusInput02	USINT	•			
22	CompensationTemperature	INT		•		

4.31.7.11.3 Function model 1 - External cold junction temperature

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
24	ConfigOutput01	USINT				•
26	ConfigOutput02	USINT				•
27	ConfigOutput03	USINT				•
Communication						
12	ExternalCompensationTemperature	INT			•	
0	Temperature01	INT	•			
2	Temperature02	INT	•			
4	Temperature03	INT	•			
6	Temperature04	INT	•			
8	Temperature05	INT	•			
10	Temperature06	INT	•			
28	IOCycleCounter	USINT	•			
30	StatusInput01	USINT	•			
31	StatusInput02	USINT	•			

4.31.7.11.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
24	-	ConfigOutput01	USINT				•
26	-	ConfigOutput02	USINT				•
27	-	ConfigOutput03	USINT				•
Communication							
0	0	Temperature01	INT	•			
2	2	Temperature02	INT	•			
4	4	Temperature03	INT	•			
6	8	Temperature04	INT	•			
8	10	Temperature05	INT	•			
10	12	Temperature06	INT	•			
28	-	IOCycleCounter	USINT		•		
30	-	StatusInput01	USINT		•		
31	-	StatusInput02	USINT		•		
22	-	CompensationTemperature	INT		•		

1) The offset specifies the position of the register within the CAN object.

4.31.7.11.4.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.31.7.11.5 General information

4.31.7.11.5.1 Raw value measurement

If a sensor type other than J, K, N, S, B or R is used, the terminal temperature must be measured on at least one input. Based on this value, the user must then implement terminal temperature compensation.

4.31.7.11.5.2 Timing

The timing for acquiring measurement values is determined by the converter hardware. All enabled inputs are converted during each conversion cycle. In addition, the terminal temperature is measured (not in function model 1).

Any inputs that are not needed can be switched off, which reduces the I/O update time. Inputs can also be only switched off temporarily. Measuring the terminal temperature is switched off in function model 1.

4.31.7.11.5.3 Conversion time

The conversion time depends on the number of channels and the function model. For the formulas listed in the table, "n" corresponds to the number of channels that are switched on.

Function model	Conversion time
Model 0 - n channels	(n + 1) · (2 · Filter time + 200 µs)
Model 1 - n channels	n · (2 · Filter time + 200 µs)
Model 1 - 1 channel	Equal to the filter time

Examples

Inputs are filtered using a 50 Hz filter.

	Example 1		Example 2	
	Function model 0	Function model 1	Function model 0	Function model 1
Switched on inputs	1	1	1 - 6	1 - 6
Input conversion times	40.2 ms	20 ms	241.2 ms	241.2 ms
Conversion time for the terminal temperature	40.2 ms	-	40.2 ms	-
Total conversion time	80.4 ms	20 ms	281.4 ms	241.2 ms

4.31.7.11.6 Configuration

4.31.7.11.6.1 Input filter and ambient conditions

Name:
ConfigOutput01

This register configures input filters and ambient conditions.

Input filter

The filter time for all analog inputs is defined using the input filter parameter.

Value	Filter	Filter time	Digital converter resolution
0	15 Hz	66.7 ms	16-bit
1	25 Hz	40 ms	16-bit
2	30 Hz	33.3 ms	16-bit
3	50 Hz	20 ms	16-bit
4	60 Hz	16.7 ms	16-bit
5	100 Hz	10 ms	16-bit
6	500 Hz	2 ms	16-bit
7	1000 Hz	1 ms	16-bit

Environmental conditions

Ambient conditions are set in order to adjust the internal terminal temperature characteristic curve to the type and amount of generated heat dissipated to the module.

This selection is based on the power consumption of the modules connected immediately to the left and right on the X2X Link. Power consumption values can also be found in the technical data for the corresponding module. The higher value is used for the configuration.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Filter time	0000	15 Hz
		0001	25 Hz
		0010	30 Hz
		0011	50 Hz
		0100	60 Hz
		0101	100 Hz
		0110	500 Hz
		0111	1000 Hz
		1000 to 1111	Not permitted
4 - 7	Environmental conditions	0000	Default, no calculation for adjustment
		0001	Power dissipation less than 0.2 W
		0010	Power dissipation less than 1 W
		0011	Power dissipation more than 1 W
		0100 to 1111	Not permitted

4.31.7.11.6.2 Sensor type

Name:
ConfigOutput02

This module is designed for a wide range of sensor types. The sensor type must be configured because of the different alignment values.

Data type	Value	Information
USINT	0	Conversion switched off
	1	Sensor type J
	2	Sensor type K
	3	Sensor type S
	4	Sensor type N
	5	Conversion switched off
	6	Raw value without linearization and terminal temperature compensation: Resolution 1.0625 µV for a measurement range of ±35 mV
	7	Raw value without linearization and terminal temperature compensation: Resolution 2.125 µV for a measurement range of ±70 mV
	8 - 63	Conversion switched off
	64	Sensor type R
	65 - 71	Conversion switched off
	72	Sensor type B
	73 - 255	Conversion switched off

4.31.7.11.6.3 Channel disabling

Name:
ConfigOutput03

By default, all channels are switched on. To save time, individual channels can be switched off (see "Conversion time" on page 2986).

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Off
		1	On
1	Channel 2	0	Off
		1	On
2	Channel 3	0	Off
		1	On
3	Channel 4	0	Off
		1	On
4	Channel 5	0	Off
		1	On
5	Channel 6	0	Off
		1	On
6 - 7	Reserved	0	

4.31.7.11.7 Communication

4.31.7.11.7.1 Analog inputs

Name:
Temperature01 to Temperature06

Analog input value depending on the configured sensor type:

Input signal	Digital value
Type J (FeCuNi)	-2100 to +12000 (for -210.0°C to +1200.0°C)
Type K (NiCrNi)	-2700 to +13720 (for -270.0°C to +1372.0°C)
Type N (NiCrSi)	-2700 to +13000 (for -270.0°C to +1300.0°C)
Type S (PtRhPt)	-500 to +17680 (for -50.0°C to +1768.0°C)
Type B (PtRhPt)	0 to +18200 (for 0°C to +1820.0°C)
Type R (PtRhPt)	-500 to +16640 (for -50.0°C to +1664.0°C)
Raw value without linearization and terminal temperature compensation: Resolution 1.0625 µV for a measurement range of ±35 mV	-32,768 to +32,767
Raw value without linearization and terminal temperature compensation: Resolution 2.125 µV for a measurement range of ±70 mV	-32,768 to +32,767

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is not switched on, 0x8000 is output.

4.31.7.11.7.2 I/O cycle counter

Name:
IOCycleCounter

The cyclic counter increases after all input data has been updated.

Data type	Value	Information
USINT	0 to 255	Repeating counter

4.31.7.11.7.3 Input status

The module's inputs are monitored. A change in the monitoring status generates an error message.

In addition to the status info, the error type also sets the analog value as follows:

Error status	Digital value for error
Open line	+32767 (0x7FFF)
Upper limit value exceeded	+32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value	-32768 (0x8000)

Status of inputs 1 to 4

Name:
StatusInput01

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 5	Channel 3	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Status of inputs 5 to 6

Name:
StatusInput02

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 5	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 6	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

4.31.7.11.7.4 Reads the internal cold junction temperature

Name:
CompensationTemperature

The internal cold junction temperature is stored in this register.

Data type	Value	Information
INT	-250 to 850	Internal cold junction temperature (PT1000): -25.0 to 85.0°C

4.31.7.11.7.5 Defines the external cold junction temperature

Name:
ExternalCompensationTemperature

The external cold junction temperature is defined in this register.

Data type	Value	Information
INT	-250 to 850	External cold junction temperature: -25.0 to 85.0°C

4.31.7.11.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

4.31.7.11.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

For the formulas listed in the table, 'n' corresponds to the number of channels that are switched on.

Function model 0	
n inputs	(n + 1) · (Filter time + 200 µs)

Function model 1	
1 input	Equal to the filter time
n inputs	n · (Filter time + 200 µs)

4.31.8 X20ATA312

4.31.8.1 General information

The module is equipped with 2 inputs for PT100 4-line resistance temperature measurement.

- 2 inputs for resistance temperature measurement
- PT100 sensor
- Direct resistance measurement as well
- 4-wire measurement
- Filter time can be configured

4.31.8.2 Order data

Model number	Short description	Figure
	Temperature measurement	
X20ATA312	X20 temperature input module, 2 inputs for resistance measurement, PT100, resolution 0.01°C, 4-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 699: X20ATA312 - Order data

4.31.8.3 Technical data

Product ID	X20ATA312
Short description	
I/O module	2 inputs for PT100 resistance temperature measurement
General information	
B&R ID code	0xE0E4
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.4 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
Temperature inputs resistance measurement	
Input	Resistance measurement with constant current supply for 4-wire connections
Digital converter resolution	24-bit
Filter time	1 to 200 ms
Conversion time	
1 channel	20 ms with 50 Hz filter
2 channels	40 ms per channel with 50 Hz filter
Conversion procedure	Sigma-delta
Output format	DINT or UDINT for resistance measurement
Resistance measurement range	0.5 to 390 Ω
Temperature sensor resolution	1 LSB = 0.01°C
Resistance measurement resolution	0.001 Ω
Input filter	1st-order low pass / cutoff frequency 1050 Hz
Sensor standard	IEC/EN 60751

Table 700: X20ATA312 - Technical data

Product ID	X20ATA312
Isolation voltage between channel and bus	500 V_{eff}
Linearization method	Internal
Measuring current	1 mA
Temperature sensor normalization	-200 to 850°C
Reference	1568 Ω ±0.1%
Temperature measurement range	-200 to 850°C
Permitted input signal	Short-term max. 28.8 V
Max. error at 25°C 2)	
Gain	0.0059% 3)
Offset	0.0015% 4)
Max. gain drift	<0.00065% per °C 3)
Max. offset drift	<0.000025% per °C 4)
Nonlinearity	<0.001% 4)
Standardized value range for resistance measurement	19 to 390 Ω
Temperature measurement monitoring	
Range exceeded (neg.)	0x80000001
Above upper range limit	0x7FFFFFFF
Open line	0x7FFFFFFF
General error	0x80000000
Open inputs	0x7FFFFFFF
Resistance measurement monitoring	
Range exceeded (neg.)	0x80000001
Above upper range limit	0xFFFFFFFF
Open line	0xFFFFFFFF
General error	0x80000000
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 or X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 700: X20ATA312 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) To ensure accuracy, modules with a power loss <1.2 W must be inserted to the left and right of this module.
3) Based on the current resistance value.
4) Based on the entire resistance measurement range.

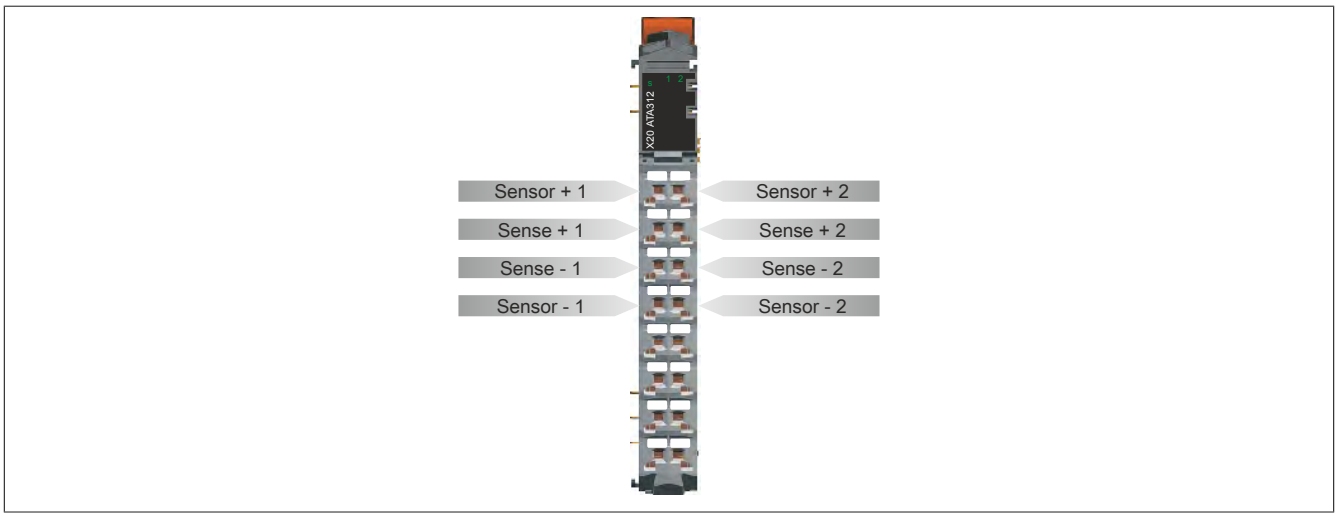
4.31.8.4 Status LEDs

For a description of the various operating modes, see section 2.11.1 "re LEDs".

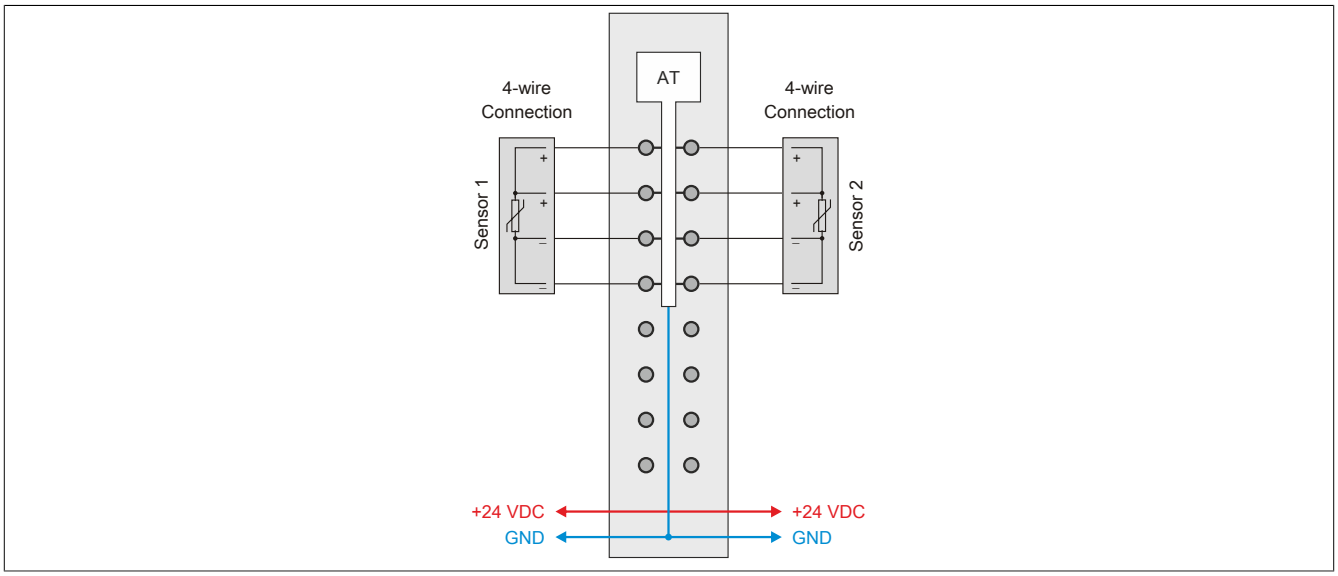
Image	LED	Color	Status	Description
	s	Green	Off	Module supply not connected
			Single flash	Reset mode
			Double flash	Boot mode (Updating firmware)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Parameter or conversion error[2]
		Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	Input turned off or not supplied
			Single flash	Parameter error[2]
			Double flash	Conversion error[2]
			Blinking	Overflow, underflow or open line
			On	A/D converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Parameter and conversion errors are indicated on both the red s-LED and the channel LED for the respective output at the same time.

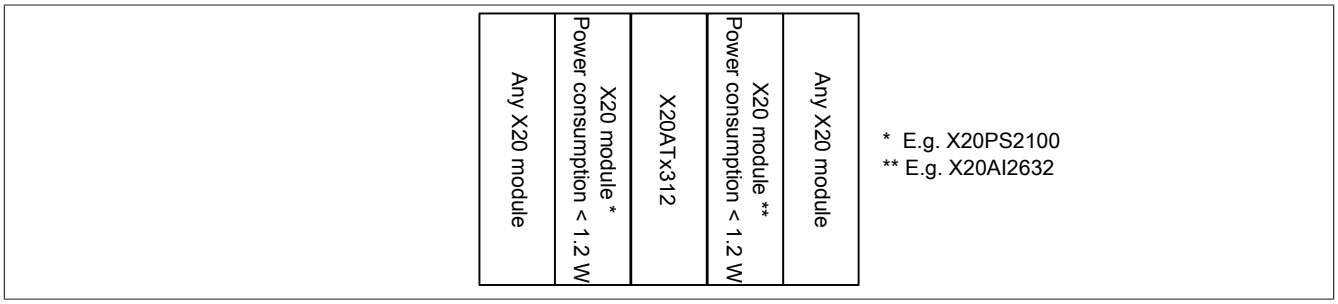
4.31.8.5 Pinout



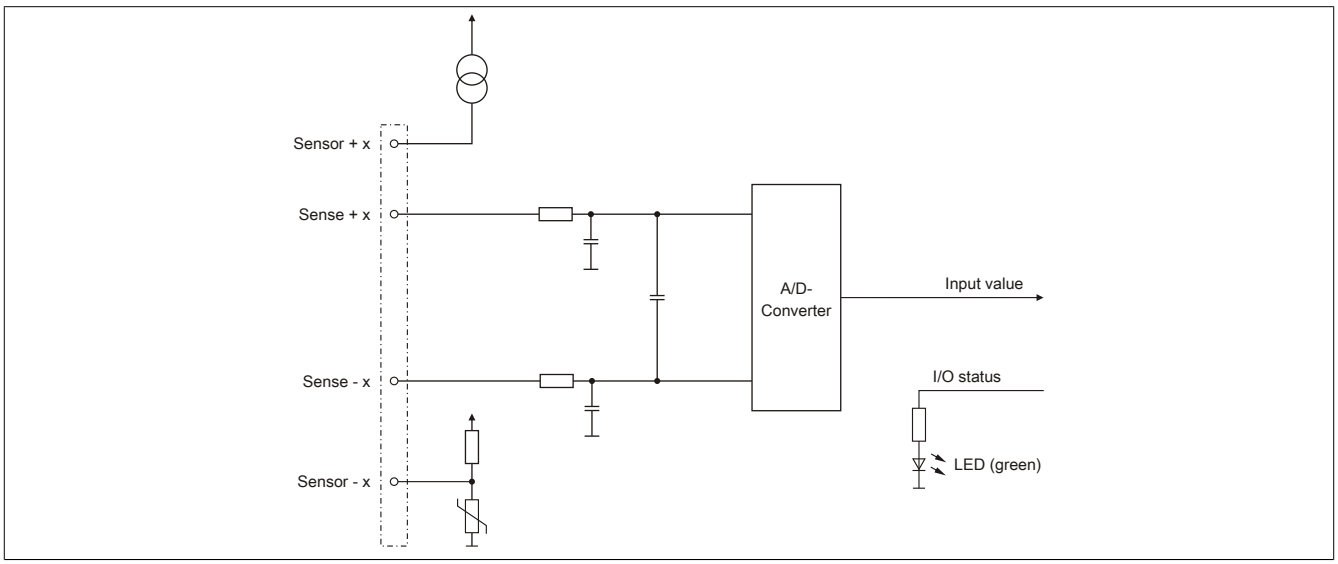
4.31.8.6 Connection example



To ensure accuracy, modules with a power consumption <1.2 W must be inserted to the left and right of this modules.



4.31.8.7 Input circuit diagram



4.31.8.8 Register description

4.31.8.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.8.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
130	InputFilter	UINT				•
134	ModeADC	UINT				•
514	SensorType01	UINT				•
578	SensorType02					
566	PreparationInterval01	UINT				•
630	PreparationInterval02					
548	ReplaceUpper01	DINT				•
612	ReplaceUpper02					
540	ReplaceLower01	DINT				•
604	ReplaceLower02					
532	UpperLimit01	DINT				•
596	UpperLimit02					
524	LowerLimit01	DINT				•
588	LowerLimit02					
554	Hysteresis01	UINT				•
618	Hysteresis02					
558	ErrorDelay01	UINT				•
622	ErrorDelay02					
562	SumErrorDelay01	UINT				•
626	SumErrorDelay02					
Communication						
0	Temperature01	DINT	•			
	Resistor01	UDINT				
4	Temperature02	DINT	•			
	Restistor02	UDINT				
260	Measurand01	DINT		•		
324	Measurand02					
281	IOCycleCounter01	USINT	•			
345	IOCycleCounter02					
282	IOCycleCounter01	UINT	•			
346	IOCycleCounter02					
274	Sampletime01	INT	•			
338	Sampletime02					
276	Sampletime01	DINT	•			
340	Sampletime02					
297	Status01	USINT	•			
	Underrun01	Bit 0				
	Overrun01	Bit 1				
	OpenLine01	Bit 2				
	ConverterFault01	Bit 4				
	SumFault01	Bit 5				
	ParameterFault01	Bit 6				
	IoSupplyFault01	Bit 7				
361	Status02	USINT	•			
	Underrun02	Bit 0				
	Overrun02	Bit 1				
	OpenLine02	Bit 2				
	ConverterFault02	Bit 4				
	SumFault02	Bit 5				
	ParameterFault02	Bit 6				
	IoSupplyFault02	Bit 7				

4.31.8.8.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
130	-	InputFilter	UINT				•
134	-	ModeADC	UINT				•
514	-	SensorType01	UINT				•
578	-	SensorType02					
566	-	PreparationInterval01	UINT				•
630	-	PreparationInterval02					
548	-	ReplaceUpper01	DINT				•
612	-	ReplaceUpper02					
540	-	ReplaceLower01	DINT				•
604	-	ReplaceLower02					
532	-	UpperLimit01	DINT				•
596	-	UpperLimit02					
524	-	LowerLimit01	DINT				•
588	-	LowerLimit02					
554	-	Hysteresis01	UINT				•
618	-	Hysteresis02					
558	-	ErrorDelay01	UINT				•
622	-	ErrorDelay02					
562	-	SumErrorDelay01	UINT				•
626	-	SumErrorDelay02					
Communication							
0	0	Temperature01	DINT	•			
		Resistor01	UDINT				
4	4	Temperature02	DINT	•			
		Restistor02	UDINT				
281	-	IOCycleCounter01	USINT		•		
345	-	IOCycleCounter02					
30	-	Status01To02	USINT		•		

1) The offset specifies where the register is within the CAN object.

4.31.8.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.31.8.8.4 Configuration of the A/D converter

4.31.8.8.4.1 Setting the conversion rate

Name:
InputFilter

This register can be used to set the conversion rate for the Analog/Digital converter.

Data type	Value
UINT	5 to 1023

Information:

The lower the conversion interval is set, the more precisely the value can be converted. However, this also increases the I/O update time.

4.31.8.8.4.2 A/D converter operating mode

Name:
ModeADC

This register can be used to set the operating mode for the Analog/Digital converter.

The individual options allow faster digitalization of the analog values, but this also reduces the precision of the measured values. The default value is 0.

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	Chopper mode	0	Alternating amplification of the analog value
		1	Chopper mode off
1	Order of the SINC filter	0	SINC4
		1	SINC3
2 - 15	Reserved	-	-

The following rules apply:

ConversionTime(SINC3) = ConversionTime(SINC4) - 1 x ConversionCycle
ConversionTime(without Chop) = 0.5 x ConversionTime(Chop)

4.31.8.8.5 Configuring the measurement channels

Each temperature measurement channel can be configured independently. All the registers required for this purpose by each channel are arranged separately.

4.31.8.8.5.1 General channel configuration

Name:
SensorType01 to SensorType02

This register defines the basic behavior of the channel.
The default value is 0x81.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	Sensor type with unit and resolution	001	PT100 [10 mK/bit] - Temperature measurement
		010	PT100 [1 mΩ/bit] - Resistance measurement
		011 to 111	Reserved
3 - 4	Reserved	-	
5	Replacement value strategy	0	Static replacement
		1	Retain last valid value
6	Monitoring the user-defined limit values	0	Switch off additional limits
		1	Switch on additional limits
7	Channel (on/off)	0	Switch off the entire channel
		1	Switch on the channel
8 - 15	Reserved	-	

4.31.8.8.6 Configuring the replacement value strategy

If a measured value is detected that is outside the permitted value range, the behavior of the input register must still remain clearly defined. The module provides the user two different options for this purpose.

Retain last valid value

With this strategy, the determined measured value is stored temporarily for a specific time and written to the input register after a delay. If an invalid measured value is detected, this value and all values that have been stored temporarily are discarded. The last valid input register value is retained. To update the value in the input register, there must be enough valid values stored in the temporary buffer. The number needed is determined by the time period specified in "PreparationInterval0x".

Replace with static value

With this strategy, the measured value is written to the input register without delay. If an invalid value occurs, it is replaced by a static value that has been predefined by the user.

4.31.8.8.6.1 Preparation interval

Name:
PreparationInterval01 to PreparationInterval02

This register defines the time interval in which the measured value is checked before being passed on.

Data type	Value
UINT	0 to 65535 (x 0.1 ms)

Information:

This register must be defined if the replacement value strategy "Retain last valid value" was selected in register "SensorType0x".

4.31.8.8.6.2 Static replacement value for upper limit

Name:
ReplaceUpper01 to ReplaceUpper02

This register is used to defined a replacement value that is output in place of the invalid measured value if the upper limit is violated.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Information:

This register must be defined if the replacement value strategy "Replace with static value" was selected in register "SensorType0x".

4.31.8.8.6.3 Static replacement value for lower limit

Name:
ReplaceLower01 to ReplaceLower02

This register is used to defined a replacement value that is output in place of the invalid measured value if the lower limit is violated.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Information:

This register must be defined if the replacement value strategy "Replace with static value" was selected in register "SensorType0x".

4.31.8.8.7 Configuring the user-defined limit values

This module provides the user the option to specify user-defined limits. If the valid measurement range is reduced in this way, the behavior of the replacement value strategy is more likely to be applied.

Valid measurement range

The valid range is derived from the properties of the sensor being used or the hardware and firmware of the respective B&R module. These values cannot be changed by the user.

Valid range of values

The range of values is always within the valid measurement range. The range of values can be adapted to the requirements of the application by specifying the upper and lower limit value.

4.31.8.8.7.1 Upper limit value

Name:
UpperLimit01 to UpperLimit02

This register specifies the upper limit value. The values entered should be within the valid measurement range.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.31.8.8.7.2 Lower limit value

Name:
LowerLimit01 to LowerLimit02

This register specifies the lower limit value. The values entered should be within the valid measurement range.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.31.8.8.7.3 Hysteresis

Name
Hysteresis01 to Hysteresis02

A hysteresis can be set in order to avoid frequent status changes in the measurement range close to the limit value. Here, a small section is defined at the edge of the valid range of values where the measured values retain the status (valid or invalid) of the previous measured value.

Data type	Value
UINT	0 to 65535

4.31.8.8.8 Configuring status messages

Errors are detected by the module and sent to the application. When using Function model 0 - Standard, the trigger behavior of these error messages can be influenced by the "Delay" register.

In Automation Studio, an error message can be read either packed as the entire register or individually as bits.

4.31.8.8.8.1 Delaying error messages

Name:
ErrorDelay01 to ErrorDelay02

In order to avoid false alarms due to short-term measurement variations, the status messages sent to the PLC can be delayed. This register determines the number of A/D conversions in which an error must exist before an error message is sent.

Data type	Value
UINT	0 to 65535 [A/D conversions]

4.31.8.8.8.2 Delaying the sum error message

Name:
SumErrorDelay01 to SumErrorDelay02

This register can be used to set the delay used when sending bit 5 of the "Status0x" register to the PLC independent of the other status messages.

Data type	Value
UINT	0 to 65535

4.31.8.8.9 Communication

The received temperature data is assigned a timestamp and, depending on the configuration, made available with different register names and data types.

4.31.8.8.9.1 Measured value – Temperature

Name:
Temperature01 to Temperature02

If the channel is configured for resistance measurement, the current temperature value is made available in this register.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.31.8.8.9.2 Measured value – Resistance

Name:
Resistor01 to Resistor02

If the channel is configured for resistance measurement, the current resistance value is made available in this register.

Data type	Value
UDINT	0 to 4,294,967,295

4.31.8.8.9.3 Measured value – Unweighted

Name:
Measurand01 to Measurand02

When using the AsIoAcc library, the unweighted measurement can be accessed via this register. This refers to a measured value that is within the valid measurement range and has not yet been compared with the user-defined limits.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Information:

If no user-defined limits are configured, the value of this register does not differ from the temperature or resistance value.

4.31.8.8.9.4 Cycle counter

Name:
IOCycleCounter01 to IOCycleCounter02

This register is used to provide a continuous counter for the application that is incremented each time a temperature value is read.

Data type	Value
USINT	0 to 32767 [A/D conversions]
UINT	0 to 65535 [A/D conversions]

4.31.8.8.9.5 Sampling time - Timestamp

Name:
Sampletime01 to Sampletime02

This register is used to provide the application the net time until the temperature will be evaluated.

Data type	Value
INT	-32,768 to 32,767 [µs]
DINT	-2,147,483,648 to 2,147,483,647 [µs]

Information:

The SDC library requires a 16-bit value for the sampling time. It is therefore also prepared as a 16-bit value.

4.31.8.8.9.6 Status messages

Name:
Status01 to Status02

The register bits are set if an error has been diagnosed and the error remains longer than the delay configured in the "ErrorDelay0x" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Underrun01 to Underrun02	0	No error
		1	Value below the permitted range
1	Overrun01 to Overrun02	0	No error
		1	Value above the permitted range
2	OpenLine01 to OpenLine02	0	No error
		1	Sensor is not connected correctly
3	Reserved	-	
4	ConverterFault01 to ConverterFault02	0	No error
		1	Invalid A/D converter output
5	SumFault01 to SumFault02	0	No error
		1	Composite error
6	ParameterFault01 to ParameterFault02	0	No error
		1	The 4.31.8.8.5.1 "SensorType0x" register is faulty
7	IoSupplyFault01 to IoSupplyFault02	0	No error
		1	The I/O supply voltage is faulty

4.31.8.8.9.7 Status messages for function model 254

Name:
Status01To02

The bits in this register are set if an error has been detected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Underrun on channel 01	0	No error
		1	Value below the permitted range
1	Overrun on channel 01	0	No error
		1	Value above the permitted range
2	Underrun on channel 02	0	No error
		1	Value below the permitted range
3	Overrun on channel 02	0	No error
		1	Value above the permitted range
4 - 7	Reserved	-	

Information:

If an open line is detected on a channel, then both error messages will be displayed at the same time.

4.31.8.8.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.31.8.8.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 ms

4.31.9 X20ATA492

4.31.9.1 General information

The module is equipped with 2 inputs for J, K, N, S, B, R, E, C and T thermocouple sensors. The 2 measurement channels are electrically isolated from each other.

This module can also be equipped with the X20TB1E thermocouple terminal block with integrated PT1000 temperature sensors. This makes it possible to achieve optimal terminal temperature compensation.

- Single-channel electrical isolation
- Integrated terminal temperature compensation
- 2x PT1000 sensor integrated in the terminal
- 2x external PT1000 sensor can be connected, 2-wire or 4-wire connections

4.31.9.2 Order data

Model number	Short description	Figure
	Temperature measurement	
X20ATA492	X20 temperature input module, 2 thermocouple inputs, type J, K, N, S, B, R, E, C, T, single channel electrically isolated, 2x PT1000 integrated for terminal temperature compensation, with 1x X20TB1E terminal block, order terminal block separately	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1E	X20 terminal block, 12-pin, 24 VDC keyed, 2x PT1000 integrated for terminal temperature compensation	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 701: X20ATA492 - Order data

4.31.9.3 Technical data

Product ID	X20ATA492
Short description	
I/O module	2 inputs for thermocouples
General information	
B&R ID code	0xBB98
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.35 W
Internal I/O	0.5 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	Yes
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Thermocouple temperature inputs	
Input	Thermocouple
Digital converter resolution	16-bit
Filter time	Configurable between 1 ms and 66.7 ms
Conversion time	
Internal terminal temperature comp.	2 * 4 * x ms [2)]
External terminal temperature comp.	x ms [2)]
Remote temperature comp.	2 * 4 * x ms [2)]
Output format	INT
Measurement range	
Sensor temperature	
Type J: Fe-CuNi	-210 to 1200°C
Type K: NiCr-Ni	-270 to 1372°C
Type N: NiCrSi-NiSi	-270 to 1298°C
Type S: PtRh10-Pt	-50 to 1768°C
Type B: PtRh30-PtRh6	0 to 1820°C
Type R: PtRh13-Pt	-50 to 1760°C
Type E: NiCr-CuNi	-270 to 997°C
Type C: WRe5-WRe26	0 to 2310°C
Type T: Cu-CuNi	-270 to 400°C
Terminal temperature	-40 to 130°C
Voltage	±65.534 mV
Sensor standard	EN 60584
Resolution	
Sensor temperature	1 LSB = 0.1°C
Terminal temperature	1 LSB = 0.1°C
Voltage	Depending on gain, 1 LSB = 1 µV or 2 µV
Normalization	
Type J	-210 to 1200°C
Type K	-270 to 1372°C
Type N	-270 to 1298°C
Type S	-50 to 1768°C
Type B	0 to 1820°C
Type R	-50 to 1760°C
Type E	-270 to 997°C
Type C	0 to 2310°C
Type T	-270 to 400°C
Terminal temperature (PT1000)	-40 to 130°C
Voltage	Depending on gain ±32.767 mV or ±65.534 mV
Monitoring	
Range exceeded (neg.)	0x8001
Above upper range limit	0x7FFF
Open line	0x7FFF
Open inputs	0x7FFF
General error	0x8000
Conversion procedure	Sigma-delta
Linearization method	Internal
Permitted input signal	Max. ±5 V
Input filter	1st-order low pass / cutoff frequency 500 Hz

Table 702: X20ATA492 - Technical data

Product ID	X20ATA492
Max. error at 25°C	
Gain	0.07% 3)
Offset	
Type J	0.03% 4)
Type K	0.04% 4)
Type N	0.04% 4)
Type S	0.1% 4)
Type B	0.12% 4)
Type R	0.08% 4)
Type E	0.03% 4)
Type C	0.05% 4)
Type T	0.08% 4)
Voltage	0.017% 4)
Max. gain drift	
Channel	0.01 %/°C 3)
Terminal temperature (PT1000)	0.003 %/°C 3)
Max. offset drift	
Type J	0.0019 %/°C 4)
Type K	0.0025 %/°C 4)
Type N	0.003 %/°C 4)
Type S	0.0081 %/°C 4)
Type B	0.0111 %/°C 4)
Type R	0.0072 %/°C 4)
Type E	0.0017 %/°C 4)
Type C	0.0039 %/°C 4)
Type T	0.0072 %/°C 4)
Terminal temperature (PT1000)	0.005 %/°C 4)
Voltage	0.001 %/°C 4)
Nonlinearity	
Channel	±0.004% 4)
Terminal temperature	±0.004% 3)
Terminal temperature compensation	
Operating modes	Internal/remote or external
Basic accuracy at 25°C without taking the PT1000 sensor into consideration	±0.06%
Accuracy of the internal terminal temperature	
With natural convection	±1.5°C after 20 min
With artificial convection	±3.0°C after 20 min
Common-mode rejection	
DC	>110 dB
50 Hz	>110 dB
60 Hz	>110 dB
Common-mode range	±50 V
Crosstalk between channels	>70 dB
Isolation voltage	
Between channel and bus	500 V_{eff}
Between channel and channel	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C

Table 702: X20ATA492 - Technical data

Product ID	X20ATA492
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1E terminal block for internal/remote terminal temperature compensation separately Order 1x X20TB1F terminal block for external terminal temperature compensation separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 702: X20ATA492 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) With a 50 Hz filter, x = 20 ms (1 / 50 Hz = 20 ms)
3) Based on the current measured value.
4) Based on the entire measurement range.

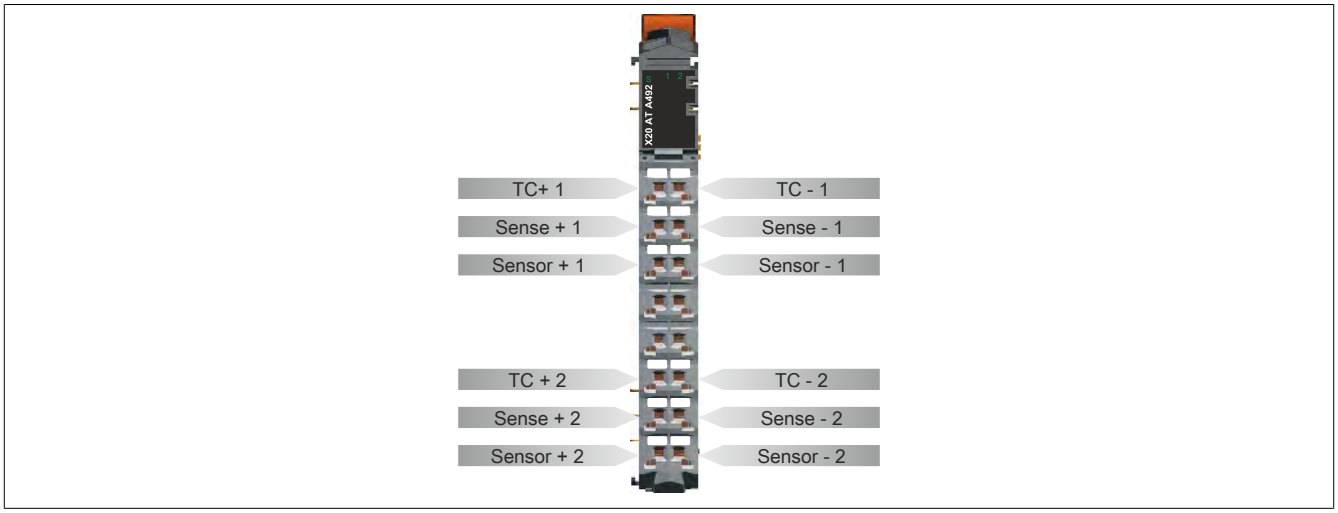
4.31.9.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	A parameter or conversion error has occurred. This status is output in addition to a single/double flash on the channel LED of the analog input where the error occurs.
		Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	Input turned off or not supplied
			Single flash	A parameter error has occurred. A single flash is output on the red "s" module status LED.
			Double flash	A conversion error has occurred. A single flash is output on the red "s" module status LED.
			Blinking	Overflow, underflow or open line
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

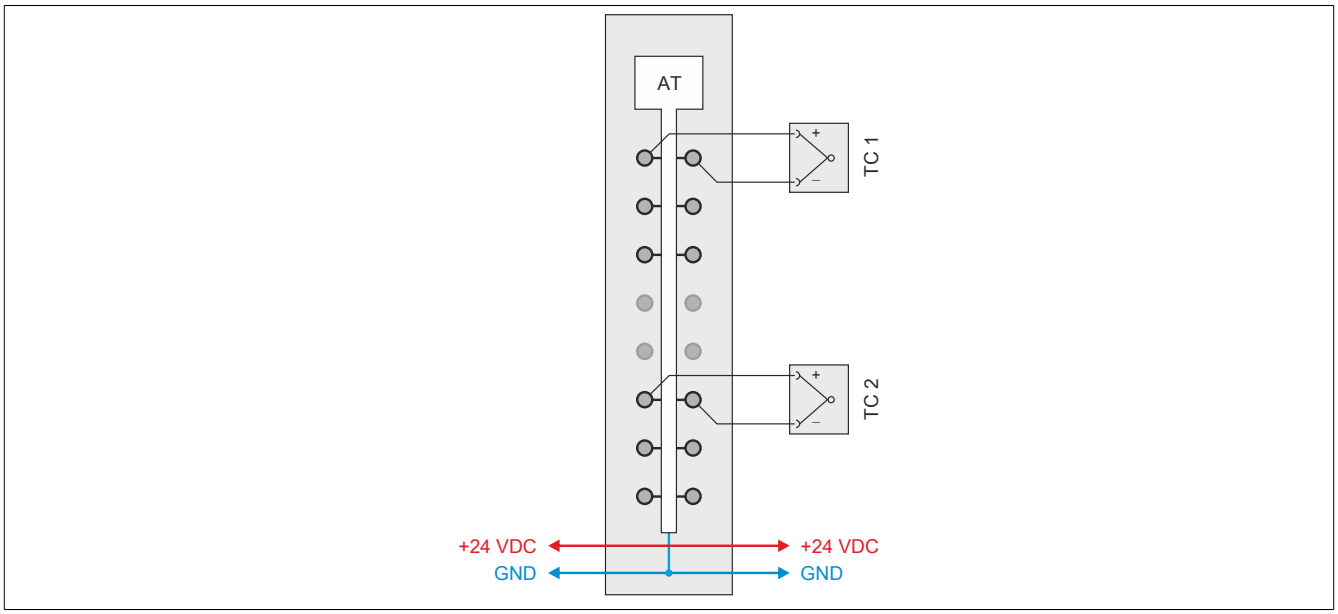
4.31.9.5 Pinout



4.31.9.6 Connection examples

Internal temperature compensation

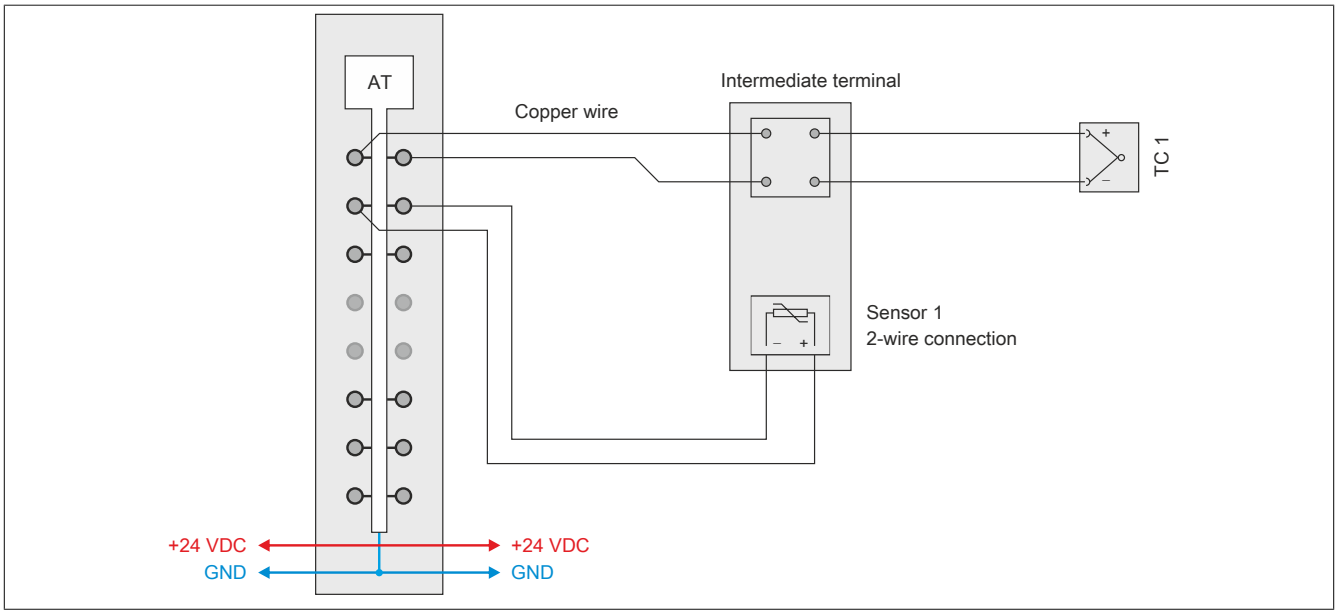
The thermocouple terminal block X20TB1E with integrated PT1000 sensors is used for internal temperature compensation.



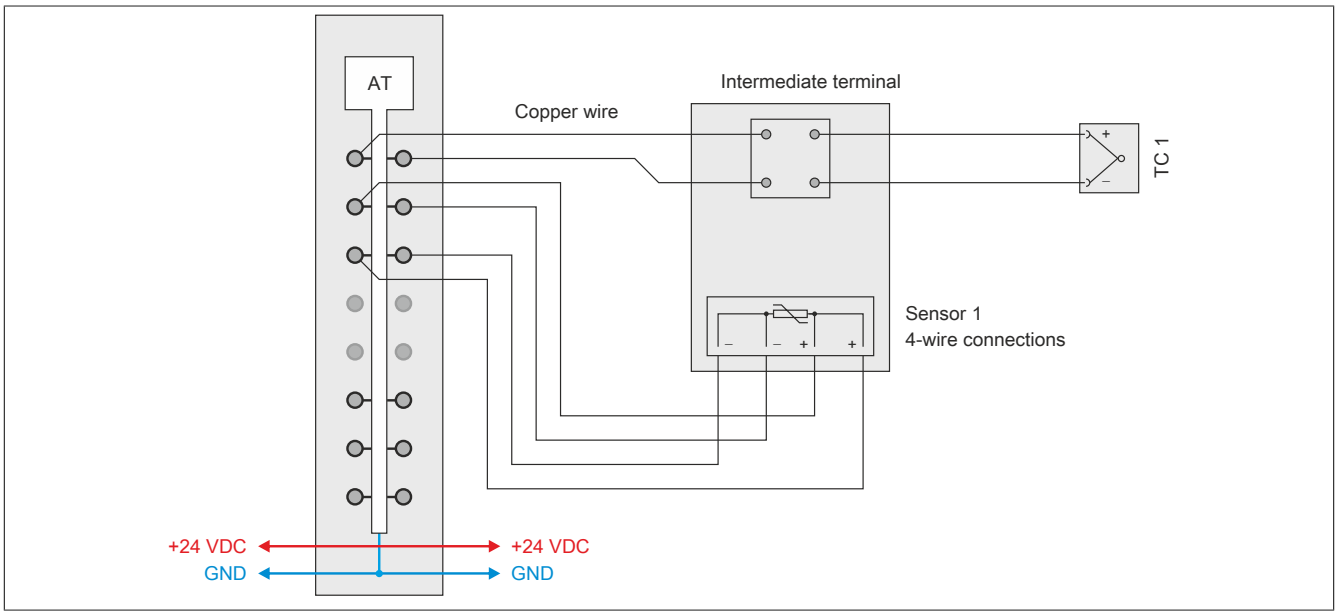
Remote temperature compensation

The 16x standard terminal X20TB1F is used for remote temperature compensation. The external PT1000 sensors are connected to the module using 2-wire or 4-wire connections.

2-wire connections



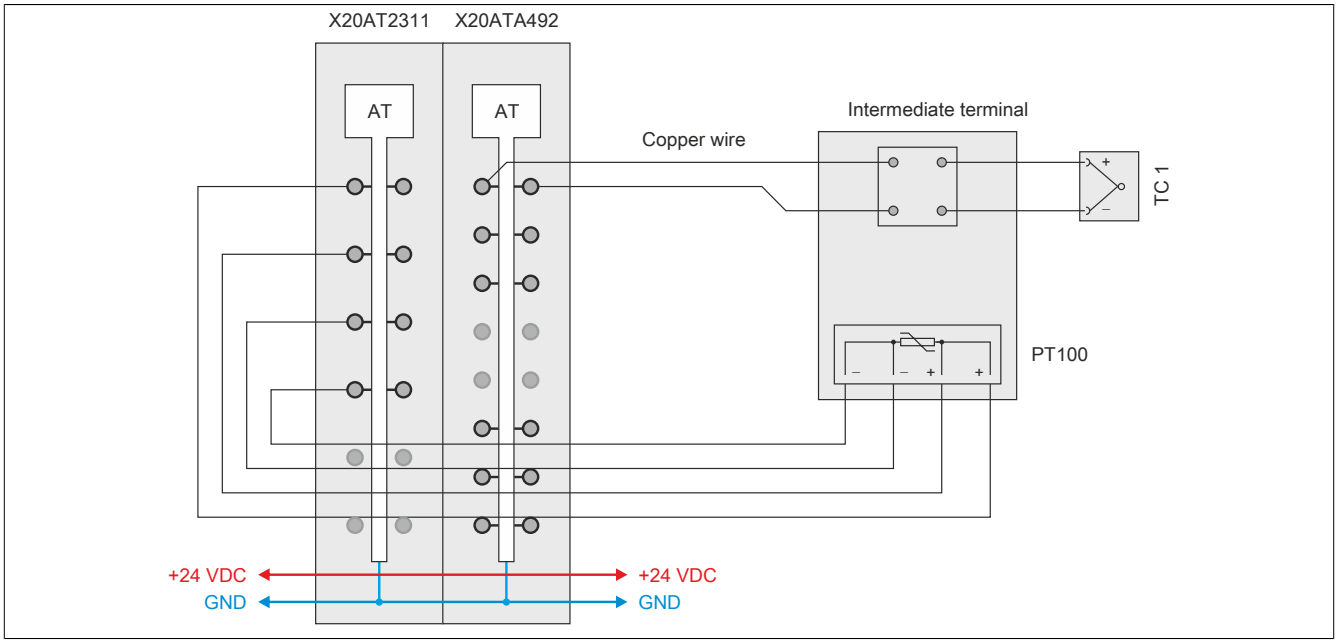
4-wire connections



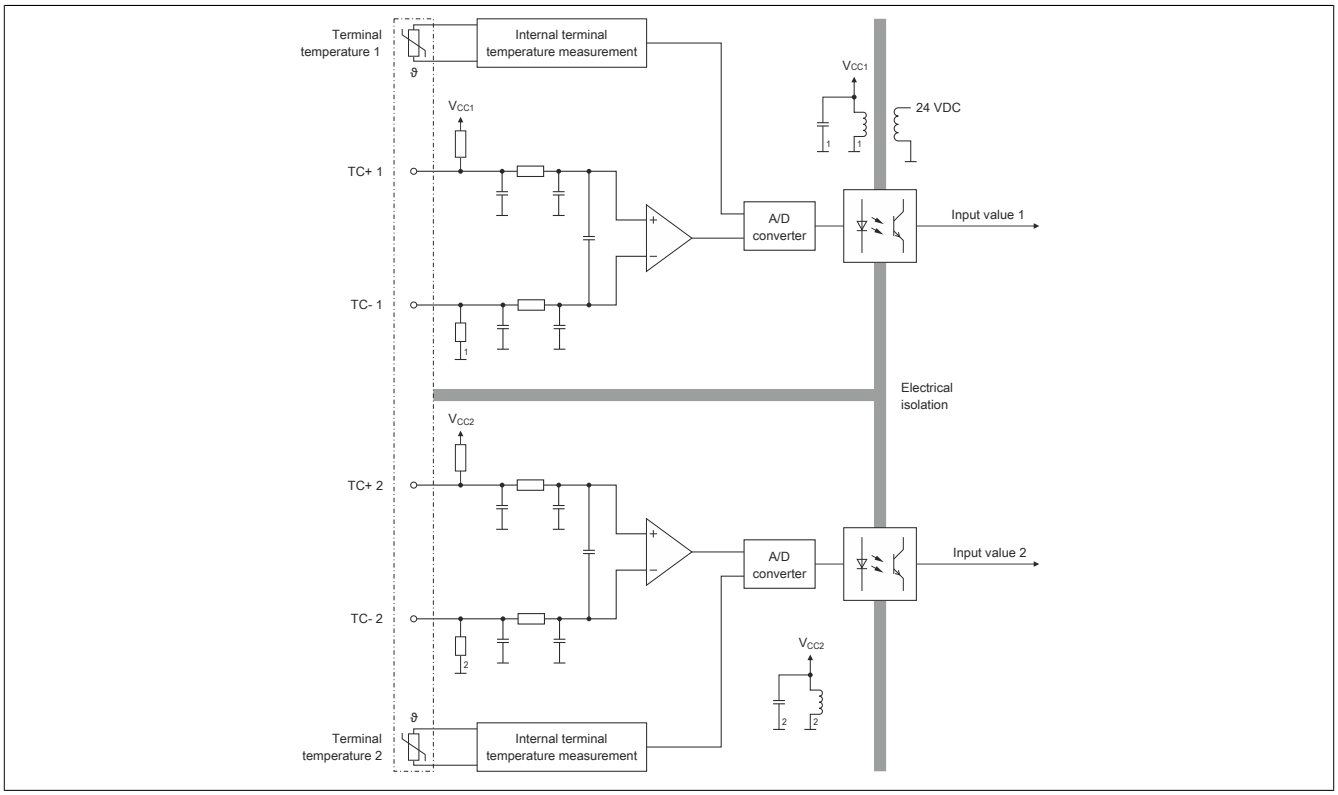
External temperature compensation

External compensation does not require the PT1000 values to be converted internally in the module. Instead, the reference temperatures have to be pre-processed in the program before being stored in the module. A separate register is available for each temperature channel to transfer an externally pre-processed compensation value.

In the following example, the compensation value is determined using the X20AT2311 temperature input module and a PT100 sensor on the intermediate terminal. The cold junction temperature determined externally is then made available to the X20ATA492 module via the respective I/O data points.



4.31.9.7 Input circuit diagram



4.31.9.8 Increased precision

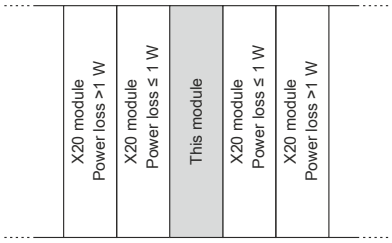
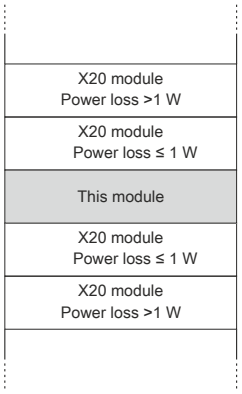
4.31.9.8.1 Internal temperature compensation

When using internal terminal temperature compensation, a temperature model must be defined in order to increase precision. A temperature model should be selected according to the following criteria:

- Thermal power loss of neighboring modules
- X20 system - Mounting orientation

4.31.9.8.1.1 Neighboring modules with low thermal power loss

The temperature model listed in the table must be configured according to the mounting orientation.

Horizontal installation	Vertical installation
	

The following temperature model must be set in the Cfo_SensorTypeCh0x register.

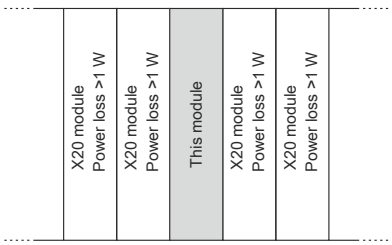
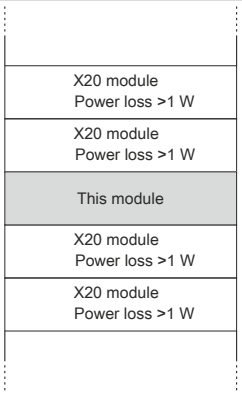
Bit 6 and 7	Temperature model	Bit 6 and 7	Temperature model
00	Horizontal installation, low thermal radiance <1W	10	Vertical installation, low thermal radiance <1W

Information:

The best results are achieved by placing a dummy module on both sides.

4.31.9.8.1.2 Neighboring modules with higher thermal power loss

The temperature model listed in the table must be configured according to the mounting orientation.

Horizontal installation	Vertical installation
	

The following temperature model must be set in the Cfo_SensorTypeCh0x register.

Bit 6 and 7	Temperature model	Bit 6 and 7	Temperature model
01	Horizontal installation, high thermal radiance >1 W	11	Vertical installation, high thermal radiance >1 W

4.31.9.8.2 Remote or external terminal temperature compensation

Setting up a remote or external cold junction can provide the most accurate temperature measurement in a machine or system.

The installation of a remote or external cold junction is especially helpful in the following cases.

- There is no module next to the temperature module
- With strongly fluctuating ambient conditions (draft, temperature)
- External fan is used in the control cabinet

4.31.9.9 Register description

4.31.9.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.9.9.2 Register overview - Function model 0 (standard)

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Data register – Channel 01						
0	TemperatureEvaluated01	INT	●	●		
4	CompensationValue01	INT	●	●		
258	Temperature01	INT	●	●		
281	StatusInput01	USINT	●	●		
285	CompensationStatus01	USINT	●	●		
290	SampleTime01_16bit	INT	●	●		
292	SampleTime01_32bit	DINT	●	●		
305	IOCycleCount01_8bit	SINT	●	●		
306	IOCycleCount01_16bit	INT	●	●		
514	ExternalCompensationTemperature01	INT			●	●
Data register – Channel 02						
2	TemperatureEvaluated02	INT	●	●		
6	CompensationValue02	INT	●	●		
262	Temperature02	INT	●	●		
283	StatusInput02	USINT	●	●		
287	CompensationStatus02	USINT	●	●		
298	SampleTime02_16bit	INT	●	●		
300	SampleTime02_32bit	DINT	●	●		
313	IOCycleCount02_8bit	SINT	●	●		
314	IOCycleCount02_16bit	INT	●	●		
518	ExternalCompensationTemperature02	INT			●	●
Configuration register – Channel 01						
386	Cfo_SensorTypeCh01	UINT			●	●
390	Cfo_InputFilterCh01	UINT			●	●
394	Cfo_LowerLimitCh01	INT			●	●
398	Cfo_UpperLimitCh01	INT			●	●
402	Cfo_HysteresisCh01	INT			●	●
406	Cfo_ReplaceLowerCh01	INT			●	●
410	Cfo_ReplaceUpperCh01	INT			●	●
414	Cfo_ErrorDelayCh01	UINT			●	●
418	Cfo_SumErrorDelayCh01	UINT			●	●
466	Cfo_PreparationInterval01	UINT			●	●
Configuration register – Channel 02						
426	Cfo_SensorTypeCh02	UINT			●	●
430	Cfo_InputFilterCh02	UINT			●	●
434	Cfo_LowerLimitCh02	INT			●	●
438	Cfo_UpperLimitCh02	INT			●	●
442	Cfo_HysteresisCh02	INT			●	●
446	Cfo_ReplaceLowerCh02	INT			●	●
450	Cfo_ReplaceUpperCh02	INT			●	●
454	Cfo_ErrorDelayCh02	UINT			●	●
458	Cfo_SumErrorDelayCh02	UINT			●	●
482	Cfo_PreparationInterval02	UINT			●	●

Table 703: Register overview - Function model 0 (standard)

4.31.9.9.3 Variable mapping in Automation Studio (X2X master)

Name	Data type	Read		Write	
		Cyclic	Acyclic	Cyclic	Acyclic
Variables – Channel 01					
Temperature01	INT	●			
SampleTime01	INT	●			
	DINT				
IOCycleCount01	SINT	●			
	INT				
CompensationValue01	INT	●			
ExternalCompensationTemperature01	INT			●	
StatusInput01	USINT	●			
Underflow01	BOOL	●			
Overflow01	BOOL	●			
OpenLine01	BOOL	●			
CompTemperaturError01	BOOL	●			
ConversionError01	BOOL	●			
SumError01	BOOL	●			
ParameterError01	BOOL	●			
IoSuppError01	BOOL	●			
CompensationStatus01	USINT	●			
CompUnderflow01	BOOL	●			
CompOverflow01	BOOL	●			
CompOpenLine01	BOOL	●			
CompConversionError01	BOOL	●			
CompSumError01	BOOL	●			
CompParameterError01	BOOL	●			
CompIoSuppError01	BOOL	●			
Variables – Channel 02					
Temperature02	INT	●			
SampleTime02	INT	●			
	DINT				
IOCycleCount02	SINT	●			
	INT				
CompensationValue02	INT	●			
ExternalCompensationTemperature02	INT			●	
StatusInput02	USINT	●			
Underflow02	BOOL	●			
Overflow02	BOOL	●			
OpenLine02	BOOL	●			
CompTemperaturError02	BOOL	●			
ConversionError02	BOOL	●			
SumError02	BOOL	●			
ParameterError02	BOOL	●			
IoSuppError02	BOOL	●			
CompensationStatus02	USINT	●			
CompUnderflow02	BOOL	●			
CompOverflow02	BOOL	●			
CompOpenLine02	BOOL	●			
CompConversionError02	BOOL	●			
CompSumError02	BOOL	●			
CompParameterError02	BOOL	●			
CompIoSuppError02	BOOL	●			

Table 704: Variable mapping in Automation Studio (X2X master)

4.31.9.9.4 Register overview - Function model 254 (bus controller)

Register	Name		Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Data register – Channel 01							
0	0[1)]	TemperatureEvaluated01	INT	●			
281	StatusInput01		USINT		●		
285	CompensationStatus01		USINT		●		
290	SampleTime01_16bit		INT		●		
292	SampleTime01_32bit		DINT		●		
305	IOCycleCount01_8bit		SINT		●		
306	IOCycleCount01_16bit		INT		●		
514	ExternalCompensationTemperature01		INT				●
Data register – Channel 02							
2	2[1)]	TemperatureEvaluated02	INT	●			
283	StatusInput02		USINT		●		
287	CompensationStatus02		USINT		●		
298	SampleTime02_16bit		INT		●		
300	SampleTime02_32bit		DINT		●		
313	IOCycleCount02_8bit		SINT		●		
314	IOCycleCount02_16bit		INT		●		
518	ExternalCompensationTemperature02		INT				●
Configuration register – Channel 01							
4	4[1)]	CompensationValue01	INT	●			
386	Cfo_SensorTypeCh01		UINT				●
390	Cfo_InputFilterCh01		UINT				●
394	Cfo_LowerLimitCh01		INT				●
398	Cfo_UpperLimitCh01		INT				●
402	Cfo_HysteresisCh01		INT				●
406	Cfo_ReplaceLowerCh01		INT				●
410	Cfo_ReplaceUpperCh01		INT				●
414	Cfo_ErrorDelayCh01		UINT				●
418	Cfo_SumErrorDelayCh01		UINT				●
466	Cfo_PreparationInterval01		UINT				●
Configuration register – Channel 02							
6	6[1)]	CompensationValue02	INT	●			
426	Cfo_SensorTypeCh02		UINT				●
430	Cfo_InputFilterCh02		UINT				●
434	Cfo_LowerLimitCh02		INT				●
438	Cfo_UpperLimitCh02		INT				●
442	Cfo_HysteresisCh02		INT				●
446	Cfo_ReplaceLowerCh02		INT				●
450	Cfo_ReplaceUpperCh02		INT				●
454	Cfo_ErrorDelayCh02		UINT				●
458	Cfo_SumErrorDelayCh02		UINT				●
482	Cfo_PreparationInterval02		UINT				●

Table 705: Register overview – Function model 254 (bus controller)

1) Offset in the cyclical CAN object (PDO, etc.).

4.31.9.9.5 Variable mapping in Automation Studio (CANIO)

Name	Data type	Read		Write	
		Cyclic	Acyclic	Cyclic	Acyclic
Variables – Channel 01					
Temperature01	INT	•			
SampleTime01	INT		•		
	DINT				
IOCycleCount01	SINT		•		
	INT				
CompensationValue01	INT	•			
ExternalCompensationTemperature01	INT				•
StatusInput01	USINT		•		
Underflow01	BOOL		•		
Overflow01	BOOL		•		
OpenLine01	BOOL		•		
CompTemperaturError01	BOOL		•		
ConversionError01	BOOL		•		
SumError01	BOOL		•		
ParameterError01	BOOL		•		
IoSuppError01	BOOL		•		
CompensationStatus01	USINT		•		
CompUnderflow01	BOOL		•		
CompOverflow01	BOOL		•		
CompOpenLine01	BOOL		•		
CompConversionError01	BOOL		•		
CompSumError01	BOOL		•		
CompParameterError01	BOOL		•		
CompIoSuppError01	BOOL		•		
Variables – Channel 02					
Temperature02	INT	•			
SampleTime02	INT		•		
	DINT				
IOCycleCount02	SINT		•		
	INT				
CompensationValue02	INT	•			
ExternalCompensationTemperature02	INT				•
StatusInput02	USINT		•		
Underflow02	BOOL		•		
Overflow02	BOOL		•		
OpenLine02	BOOL		•		
CompTemperaturError02	BOOL		•		
ConversionError02	BOOL		•		
SumError02	BOOL		•		
ParameterError02	BOOL		•		
IoSuppError02	BOOL		•		
CompensationStatus02	USINT		•		
CompUnderflow02	BOOL		•		
CompOverflow02	BOOL		•		
CompOpenLine02	BOOL		•		
CompConversionError02	BOOL		•		
CompSumError02	BOOL		•		
CompParameterError02	BOOL		•		
CompIoSuppError02	BOOL		•		

Table 706: Variable mapping in Automation Studio (CANIO)

4.31.9.9.6 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.31.9.9.7 Temperature measurement

4.31.9.9.7.1 Data registers

The module stores converted analog values in the registers. The configured sensor type will affect the value ranges.

The channels for Group 01 – temperature sensor and cold junction temperature, respectively – are electrically isolated from Group 02. The channels for both groups are operated at the same time by a separate analog converter. If the terminal is not used with integrated measuring resistance, it is important to make sure that the sensor and the corresponding cold junction are connected properly in the external wiring.

4.31.9.9.7.2 "Temperature0x" and "TemperatureEvaluated0x" registers

Analog input value depending on the configured sensor type:

Input signal	Digital value
Type J (Fe-CuNi)	-2100 to 12000 (for -210.0 to 1200.0°C)
Type K (NiCr-Ni)	-2700 to 13720 (for -270.0 to 1372.0°C)
Type N (NiCrSi-NiSi)	-2700 to 12980 (for -270.0 to 1298.0°C)
Type S (PtRh10-Pt)	-500 to 17680 (for -50.0 to 1768.0°C)
Type R (PtRh13-Pt)	-500 to 17600 (for -50.0 to 1760.0°C)
Type C (WRe5-WRe26)	0 to 23100 (for 0 to 2310.0°C)
Type T (Cu-CuNi)	-2700 to 4000 (for -270.0 to 400.0°C)
Type B (PtRh30-PtRh6)	0 to 18200 (for 0 to 1820.0°C)
Type E (NiCr-CuNi)	-2700 to 9970 (for -270.0 to 997.0°C)
Voltage without linearization and terminal temperature compensation Resolution 1.0625 µV for a measurement range of ±35 mV	-32,768 to 32,767
Voltage without linearization and terminal temperature compensation Resolution 2.125 µV for a measurement range of ±70 mV	-32,768 to 32,767

Table 707: "Temperature01", "Temperature02", "TemperatureEvaluated01" and "TemperatureEvaluated02" registers

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is switched off, 0x8000 is output.
- If an I/O voltage supply failure occurs, 0x8000 is output

4.31.9.9.7.3 Voltage measurement

If a sensor type different than the module's integrated sensor is used, then the terminal temperature must be measured on the corresponding cold junction input. Based on this value, the user must then implement terminal temperature compensation in the application.

4.31.9.9.7.4 Timing

The timing for acquiring measurement values is determined by the converter hardware and the configured filter time. All enabled inputs are converted by the two analog converters during each conversion cycle.

The temperature input and the cold junction temperature of the corresponding galvanic measurement group are counted as channels. The maximum number of channels to calculate is therefore n = 2.

Any inputs that are not needed can be switched off, which reduces the I/O update time. To generate a temperature value with the configured filter time as the I/O update time, the temperature compensation must be configured using an externally specified cold junction value.

The conversion time depends on the number of channels. For the formula listed in the table, "n" corresponds to the number of channels that are switched on.

Number of channels	Conversion time
n channels	n * defined filter time

Table 708: Conversion time calculation

4.31.9.9.7.5 "CompensationValue0x" registers

The two internal cold junction temperatures on the module can be read in standard operation. These are not available when using an internal temperature model for compensation.

Analog input value:

Input signal	Digital value
Compensation temperature (PT1000)	-250 to 850 (for -25.0 to 85.0°C)

Table 709: "CompensationValue01" and "CompensationValue02" registers

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is switched off, 0x8000 is output.
- If an I/O voltage supply failure occurs, 0x8000 is output

4.31.9.9.7.6 "ExternalCompensationTemperature0x" registers

For the module, it is possible to specify external cold junction temperatures to be used for measurement correction.

Output value:

Description	Digital value
External compensation temperature	-250 to 850 (for -25.0 to 85.0°C)

Table 710: "ExternalCompensationTemperature01" and "ExternalCompensationTemperature02" registers

4.31.9.9.7.7 "SampleTime0x", "SampleTime0x_16bit" and "SampleTime0x_32bit" registers and data points

These registers and data points return the timestamp of the values currently being read as signed 2- or 4-byte values in µs.

Data type	Description
INT	-32,768 to 32,767 ... Nettime timestamp of the current input value
DINT	-2,147,483,648 to 2,147,483,647 ... Nettime timestamp of the current input value

Table 711: "SampleTime01", "SampleTime02", "SampleTime01_16bit", "SampleTime02_16bit", "SampleTime01_32bit" and "SampleTime02_32bit" registers and data points

4.31.9.9.7.8 "IOCycleCount0x", "IOCycleCount0x_08bit" and "IOCycleCount0x_16bit" registers and data points

These registers and data points are cyclic counters. They are incremented as soon as the module has converted all enabled values. When there is a difference of ≥1 compared to the previous cycle, the defined filter time has elapsed and new values are provided.

Data type	Description
USINT	-128 to 127 ... Conversion cycle counter
INT	-32,768 to 32,767 ... Conversion cycle counter

Table 712: "IOCycleCount01", "IOCycleCount02", "IOCycleCount01_08bit", "IOCycleCount02_08bit", "IOCycleCount01_16bit" and "IOCycleCount02_16bit" registers and data points

4.31.9.9.8 Configuration

4.31.9.9.8.1 Configuration registers

The following registers are used to configure the necessary operating settings for the temperature inputs and the cold junction readings.

4.31.9.9.8.2 "Cfo_SensorTypeCh0x" registers

These registers are used to set the configuration accordingly for temperature channel and cold junction measurement 01 and 02.

Data type UINT Bit	Name		Information
0 - 5	Defines sensor	000000	Sensor type J (default)
		000001	Sensor type K
		000010	Sensor type N
		000011	Sensor type S
		000100	Sensor type R
		000101	Sensor type C
		000110	Sensor type T
		000111	Sensor type B
		001000	Sensor type E
		111101	Voltage without linearization and terminal temperature compensation Resolution 1.0625 µV for a measurement range of ±35 mV
		111110	Voltage without linearization and terminal temperature compensation Resolution 2.125 µV for a measurement range of ±70 mV
6 - 7	Selection of temperature model	00	Horizontal installation, low thermal radiance ≤1 W
		01	Horizontal installation, high thermal radiance >1 W
		10	Vertical installation, low thermal radiance ≤1 W
		11	Vertical installation, high thermal radiance >1 W
8 - 9	Cold junction type	00	Cold junction sensor PT1000
		01	Reserved
		10	Reserved
		11	Cold junction conversion disabled
10	Unit for cold junction value	0	Standardization / display 0.1°C
		1	Standardization / display 0.1°C Ω
11	Cold junction value input	0	Measurement of the internal cold junction
		1	External specific via analog output value
12	Internal terminal compensation according to temperature model	0	Mode disabled
		1	Internal compensation mode according to the configured temperature model (see bits 6 and 7)
13	Replacement value strategy	0	Use replacement values if error occurs
		1	Keep the last valid converted value (see Cfo_PreparationIntervalCh0x)
14	User limit value monitoring[1)]	0	User limit value monitoring disabled
		1	User limit value monitoring enabled
15	Channel activation	0	Channel disabled
		1	Channel enabled

Table 713: "Cfo_SensorTypeCh01" and "Cfo_SensorTypeCh02" registers

1) Signal monitoring and generation of error states for underflow, overflow and open line are already automatically enabled on the module; however, the user limit values are not applied until bit 14 is set. Likewise, the replacement value strategy is only enabled if this bit is set.

Operating mode - Internal terminal compensation according to temperature model

If this mode is selected, it is important to make sure that both PT1000 cold junction sensors are configured and connected!

Selection of temperature model when internal compensation is used

This setting is used to adjust the internal terminal temperature characteristic curve to the type and amount of generated heat dissipated to the module. This selection is based on the power consumption of the modules connected immediately to the left and right on the X2X Link. This data can be found in the modules' data sheet. The higher value is used for the configuration.

4.31.9.9.8.3 "Cfo_InputFilterCh0x" registers

These registers are used to configure the filter/sampling time for a galvanic group. The defined filter/sampling time applies to the temperature input as well as the input for the terminal temperature measurement within a group.

Data type UINT Value	Description
4	Filter time 1 ms [1 kHz]
9	Filter time 2 ms [500 Hz]
48	Filter time 10 ms [100 Hz]
80	Filter time 16.67 ms [60 Hz]
96	Filter time 20 ms [50 Hz]
160	Filter time 33.3 ms [30 Hz]
192	Filter time 40 ms [25 Hz]
480	Filter time 100 ms [10 Hz]
960	Filter time 200 ms [5 Hz]

Table 714: "Cfo_InputFilterCh01" and "Cfo_InputFilterCh02" registers

4.31.9.9.8.4 "Cfo_LowerLimitCh0x" registers

These registers are used to define the lower user limit value for the respective temperature channel. If limit value monitoring is active, the corresponding error status is output after a configured delay when falling below this temperature value. When this error state occurs, the "TemperatureEvaluated0x" channel is evaluated according to the replacement value strategy.

Data type	Description
INT	-32,767 to 32,767 ... Lower limit value: 32,767 (default)

Table 715: "Cfo_LowerLimitCh01" and "Cfo_LowerLimitCh02" registers

4.31.9.9.8.5 "Cfo_UpperLimitCh0x" registers

These registers are used to define the upper user limit value for the respective temperature channel. If limit value monitoring is active, the corresponding error status is output after a configured delay when exceeding this temperature value. When this error state occurs, the "TemperatureEvaluated0x" channel is evaluated according to the replacement value strategy.

Data type	Description
INT	-32,767 to 32,767 ... Upper limit value: 32,767 (default)

Table 716: "Cfo_UpperLimitCh01" and "Cfo_UpperLimitCh02" registers

4.31.9.9.8.6 "Cfo_HysteresisCh0x" registers

These registers are used to configure the error hysteresis for the respective temperature channel. The error status is cleared if the actual temperature value changes by at least this hysteresis value in the allowed direction from the limit value.

Data type	Description
INT	-32,767 to 32,767 ... Hysteresis: 16 (default)

Table 717: "Cfo_HysteresisCh01" and "Cfo_HysteresisCh02" registers

4.31.9.9.8.7 "Cfo_ReplaceLowerCh0x" registers

These registers are used to define the lower replacement value for the respective temperature channel. If limit value monitoring is active in the replacement value strategy mode (see section 4.31.9.9.8.2 ""Cfo_SensorTypeCh0x" registers" on page 3017) and an underflow error occurs, the respective error status is generated after the configured delay and the temperature value in the "TemperatureEvaluated0x" register is kept at this replacement value.

Data type	Description
INT	-32,767 to 32,767 ... Lower replacement value: 32,767 (default)

Table 718: "Cfo_ReplaceLowerCh01" and "Cfo_ReplaceLowerCh02" registers

4.31.9.9.8.8 "Cfo_ReplaceUpperCh0x" registers

These registers are used to define the upper replacement value for the respective temperature channel. If limit value monitoring is active in the replacement value strategy mode (see section 4.31.9.9.8.2 ""Cfo_SensorTypeCh0x" registers" on page 3017) and an overflow error occurs, the respective error status is generated after the configured delay and the temperature value in the "TemperatureEvaluated0x" register is kept at this replacement value.

Data type	Description
INT	-32,767 to 32,767 ... Upper replacement value: 32,767 (default)

Table 719: "Cfo_ReplaceUpperCh01" to "Cfo_ReplaceUpperCh02" registers

4.31.9.9.8.9 "Cfo_PreparationIntervalCh0x" registers

These registers are used to configure the preparation interval for the respective temperature channel. This parameter becomes active if "Keep the last valid converted value" (see section 4.31.9.9.8.2 ""Cfo_SensorTypeCh0x" registers" on page 3017) has been selected for the replacement value strategy.

The module continues to sample and convert the temperature based on the configured filter/sampling time. The measured value must first be checked to ensure that a permissible value is being shown. If the value is valid, then the measurement value that was sampled two preparation intervals prior is always output.

Data type	Description
UINT	0 to 65,535 ... Interval time: 0 ms (default)

Table 720: "Cfo_PreparationIntervalCh01" and "Cfo_PreparationIntervalCh02" registers

"Application" Value being measured (analog)	Procedure: • Measurement values are acquired according to the configured input filter. After the sampling time elapses, a new digitally converted value is stored in the measurement value memory. After the configured interval time elapses, the current contents of the measurement value memory are checked. • If a permissible value is present, then the contents of the buffer memory are transferred to the display memory and the contents of the measurement value memory are transferred to the buffer. • If the check turns up an impermissible value, then the contents of the measurement value memory are discarded. The copy direction between the display and buffer memory reverses and the last valid value continues to be output.
↓ Condition: - Sampling time elapsed	
"Measurement value memory" Measurement value (digital)	
↓ Condition: - PreparationInterval elapsed - Measurement value permissible	
"Cache" of last valid value	
↓ Condition: - PreparationInterval elapsed - Measurement value permissible	
"Display memory" Previous valid/displayed value	

Information:

If configured to keep the last valid value, the delay time from measuring to outputting the value will be at least twice the preparation interval. In the worst case scenario, this can take twice the interval time plus the configured I/O update time.

Table 721: How the preparation interval works

4.31.9.9.8.10 "Cfo_ErrorDelayCh0x" registers

These registers are used to configure the delay for generating an error. This delay applies to underflow, overflow and open line errors and can be used to hide temporary measurement value overshoots, for example.

Data type	Description
UINT	0 to 10 ... Error formation delay: 2 conversion cycles (default)

Table 722: "Cfo_ErrorDelayCh01" and "Cfo_ErrorDelayCh02" registers

4.31.9.9.8.11 "Cfo_SumErrorDelayCh0x" registers

These registers are used to configure the delay for the composite error status. The composite error status is made up of all other error statuses.

Data type	Description
UINT	0 to 65,535 ... Composite error bit delay time: 4000 ms (default)

Table 723: "Cfo_SumErrorDelayCh01" and "Cfo_SumErrorDelayCh02" registers

4.31.9.9.9 Error handling

4.31.9.9.9.1 "StatusInput0x" registers

The module's temperature inputs are monitored. A change in the monitoring status generates an error message. Some error information is only enabled after a configurable delay [ms] (as with the composite error) or after a configurable delay as a multiple of the conversion cycle when underflow, overflow or open lines occurs.

Data type USINT Bit	Name		Information
0	Underflow monitoring for channel 0x	0	No error
		1	Underflow
1	Overflow monitoring for channel 0x	0	No error
		1	Overrun
2	Open line monitoring for channel 0x	0	No error
		1	Open line
3	Composite message: Terminal temperature measurement error for channel 0x	0	No error
		1	Error during terminal temperature measurement
4	Conversion monitoring for channel 0x	0	No error
		1	Conversion error
5	Composite error monitoring for channel 0x	0	No error
		1	Composite error
6	Parameter monitoring for channel 0x	0	No error
		1	Parameter error
7	I/O supply monitoring for channel 0x	0	No error
		1	I/O supply error

Table 724: "StatusInput01" and "StatusInput02" registers

In addition to the status info, the error type also sets the analog value to the following values:

Error type	Digital value for error
Open circuit	32767 (0x7FFF)
Upper limit value exceeded	32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value or I/O supply error	-32768 (0x8000)

Table 725: Display values in error state

4.31.9.9.9.2 "Underflow0x" data points

These data points generate the error status when the signal falls below the minimum value on the respective temperature channel. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

BOOL	Name		Information
x	Underflow monitoring for channel 0x	0	No error
		1	Underflow

Table 726: "Underflow01" and "Underflow02" data points

4.31.9.9.9.3 "Overflow0x" data points

These data points generate the error status when the signal exceeds the maximum value on the respective temperature channel. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

BOOL	Name		Information
x	Overflow monitoring for channel 0x	0	No error
		1	Overrun

Table 727: "Overflow01" and "Overflow02" data points

4.31.9.9.9.4 "OpenLine0x" data points

These data points generate the error status when an open line is detected on the respective temperature channel. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

BOOL	Name		Information
x	Open line monitoring for channel 0x	0	No error
		1	Open line

Table 728: "OpenLine01" and "OpenLine02" data points

4.31.9.9.9.5 "CompTemperaturError0x" data points

These data points generate the error status (composite message) for the cold junction temperature measurement on the respective channel. For more detailed information, see section 4.31.9.9.9.10 ""CompensationStatus0x" registers" on page 3022.

BOOL	Name		Information
x	Composite message: Terminal temperature measurement error for channel 0x	0	No error
		1	Terminal temperature measurement error

Table 729: "CompTemperaturError01" and "CompTemperaturError02" data points

4.31.9.9.9.6 "ConversionError0x" data points

These data points generate the error status for the respective temperature channel. The error is triggered when the conversion time is exceeded on the hardware.

BOOL	Name		Information
x	Conversion monitoring for channel 0x	0	No error
		1	Conversion error

Table 730: "ConversionError01" and "ConversionError02" data points

4.31.9.9.9.7 "SumError0x" data points

These data points generate the composite error for the respective temperature channel. This error information is enabled after the configurable delay time [ms] has elapsed. Linking this error information to an application makes it possible to hide temporary temperature value overflows and underflows, for example.

BOOL	Name		Information
x	Composite error monitoring for channel 0x	0	No error
		1	Composite error

Table 731: "SumError01" and "SumError02" data points

4.31.9.9.9.8 "ParameterError0x" data points

These data points generate the parameter error for the respective temperature channel. This error state is triggered by configuring a sensor type that is not allowed.

BOOL	Name		Information
x	Parameter monitoring for channel 0x	0	No error
		1	Parameter error

Table 732: "ParameterError01" and "ParameterError02" data points

4.31.9.9.9.9 "IoSuppError0x" data points

If the supply falls below 20 VDC, then the I/O power supply error is generated in these data points for the respective temperature channel. The following actions also take place:

- Channel LEDs are turned off
- Temperature values are set to an invalid value = 0x8000
- IOCycleCount0x and SampleTime0x stop changing

BOOL	Name		Information
x	I/O supply monitoring for channel 0x	0	No error
		1	I/O supply error

Table 733: "IoSuppError01" and "IoSuppError02" data points

4.31.9.9.9.10 "CompensationStatus0x" registers

The module's cold junction temperature inputs are monitored. A change in the monitoring status generates an error message. Some error information is only enabled after a configurable delay [ms] (as with the composite error) or after a configurable delay as a multiple of the conversion cycle when underflow, overflow or open lines occurs.

Data type USINT Bit	Name		Information
0	Underflow monitoring for cold junction 0x	0	No error
		1	Underflow
1	Overflow monitoring for cold junction 0x	0	No error
		1	Overrun
2	Open line monitoring for cold junction 0x	0	No error
		1	Open line
3	Composite message: Terminal temperature measurement error for cold junction 0x	0	No error
		1	Error during terminal temperature measurement
4	Conversion monitoring for cold junction 0x	0	No error
		1	Conversion error
5	Composite error monitoring for cold junction 0x	0	No error
		1	Composite error
6	Parameter monitoring for cold junction 0x	0	No error
		1	Parameter error
7	I/O supply monitoring for cold junction 0x	0	No error
		1	I/O supply error

Table 734: "CompensationStatus01" and "CompensationStatus02" registers

In addition to the status info, the error type also sets the analog value to the following values:

Error type	Digital value for error
Open circuit	32767 (0x7FFF)
Upper limit value exceeded	32767 (0x7FFF)
Lower limit value exceeded	-32767 (0x8001)
Invalid value or I/O supply error	-32768 (0x8000)

Table 735: Display values in error state

4.31.9.9.9.11 "CompUnderflow0x" data points

These data points generate the error status when the signal falls below the minimum value on the respective cold junction channel. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

BOOL	Name		Information
x	Underflow monitoring for cold junction 0x	0	No error
		1	Underflow

Table 736: "CompUnderflow01" and "CompUnderflow02" data points

4.31.9.9.9.12 "CompOverflow0x" data points

These data points generate the error status when the signal exceeds the maximum value on the respective cold junction channel. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

BOOL	Name		Information
x	Overflow monitoring for cold junction 0x	0	No error
		1	Overrun

Table 737: "CompOverflow01" and "CompOverflow02" data points

4.31.9.9.9.13 "CompOpenLine0x" data points

These data points generate the error status when an open line is detected on the respective cold junction channel. This error information is enabled as a multiple of the converter cycle only after the configurable delay time.

BOOL	Name		Information
x	Open line monitoring for cold junction 0x	0	No error
		1	Open line

Table 738: "CompOpenLine01" and "CompOpenLine02" data points

4.31.9.9.9.14 "CompConversionError0x" data points

These data points generate the error status for the respective cold junction channel. The error is triggered when the conversion time is exceeded on the hardware.

BOOL	Name		Information
x	Conversion monitoring for cold junction 0x	0	No error
		1	Conversion error

Table 739: "CompConversionError01" and "CompConversionError02" data points

4.31.9.9.9.15 "CompSumError0x" data points

These data points generate the composite error for the respective cold junction channel. This error information is enabled after the configurable delay time [ms] has elapsed. Linking this error information to an application makes it possible to hide temporary temperature value overflows and underflows, for example.

BOOL	Name		Information
x	Composite error monitoring for cold junction 0x	0	No error
		1	Composite error

Table 740: "CompSumError01" and "CompSumError02" data points

4.31.9.9.9.16 "CompParameterError0x" data points

These data points generate the parameter error for the respective cold junction channel. This error state is triggered by configuring a sensor type that is not allowed.

BOOL	Name		Information
x	Parameter monitoring for cold junction 0x	0	No error
		1	Parameter error

Table 741: "CompParameterError01" and "CompParameterError02" data points

4.31.9.9.9.17 "CompIoSuppError0x" data points

If the supply falls below 20 VDC, then the I/O power supply error is generated in these data points for the respective cold junction channel. The following actions also take place:

- Channel LEDs are turned off
- Temperature values are set to an invalid value = 0x8000
- IOCycleCount0x and SampleTime0x stop changing

BOOL	Name		Information
x	I/O supply monitoring for cold junction 0x	0	No error
		1	I/O supply error

Table 742: "CompIoSuppError01" and "CompIoSuppError02" data points

4.31.9.9.10 Function models

A function model specifies the registers on the module (storage model) that are available for the application. Only these registers are processed on the module during each cycle and transferred cyclically via the bus. In this way, it is possible to minimize the cycle time by selecting the correct function model.

Function model	Number	Automation Studio	CANopen	DeviceNet	Modbus/TCP	CAN I/O
Default	0	•				
Bus controllers	254		•	•	•	•

Table 743: Overview of possible function models

4.31.9.9.11 B&R ID code

Code for module identification (0xBB98).

4.31.9.9.12 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.31.9.9.13 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

For the formulas listed in the table, "n" corresponds to the number of channels that are switched on.

Minimum I/O update time	
Normal operation "n" channels	n * defined filter time
Replacement value mode: "Keep the last valid converted value" n channels	Sampling interval + (n * defined filter time)

4.31.10 X20ATB312

4.31.10.1 General information

The module is equipped with 4 inputs for PT100 4-line resistance temperature measurement.

- 4 inputs for resistance temperature measurement
- PT100 sensor
- Direct resistance measurement as well
- 4-wire measurement
- Filter time can be configured

4.31.10.2 Order data

Model number	Short description	Figure
	Temperature measurement	
X20ATB312	X20 temperature input module, 4 inputs for resistance measurement, PT100, resolution 0.01 °C, 4-wire connections	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 744: X20ATB312 - Order data

4.31.10.3 Technical data

Product ID	X20ATB312
Short description	
I/O module	4 inputs for PT100 resistance temperature measurement
General information	
B&R ID code	0xE0EF
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.6 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
Temperature inputs resistance measurement	
Input	Resistance measurement with constant current supply for 4-wire connections
Digital converter resolution	24-bit
Filter time	1 to 200 ms
Conversion time [2)]	
1 channel	20 ms with 50 Hz filter
2 channels	40 ms per channel with 50 Hz filter
Conversion procedure	Sigma-delta
Output format	DINT or UDINT for resistance measurement
Resistance measurement range	0.5 to 390 Ω
Temperature sensor resolution	1 LSB = 0.01°C
Resistance measurement resolution	0.001 Ω
Input filter	1st-order low pass / cutoff frequency 1050 Hz
Sensor standard	IEC/EN 60751

Table 745: X20ATB312 - Technical data

Product ID	X20ATB312
Isolation voltage between channel and bus	500 V_{eff}
Linearization method	Internal
Measuring current	1 mA
Temperature sensor normalization	-200 to 850°C
Reference	1568 Ω ±0.1%
Temperature measurement range	-200 to 850°C
Permitted input signal	Short-term max. 28.8 V
Max. error at 25°C [3]	
Gain	0.0059% [4]
Offset	0.0015% [5]
Max. gain drift	<0.00065% per °C [4]
Max. offset drift	<0.000025% per °C [5]
Nonlinearity	<0.001% [5]
Standardized value range for resistance measurement	19 to 390 Ω
Temperature measurement monitoring	
Range exceeded (neg.)	0x80000001
Above upper range limit	0x7FFFFFFF
Open line	0x7FFFFFFF
General error	0x80000000
Open inputs	0x7FFFFFFF
Resistance measurement monitoring	
Range exceeded (neg.)	0x80000001
Above upper range limit	0xFFFFFFFF
Open line	0xFFFFFFFF
General error	0x80000000
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB12 or X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 745: X20ATB312 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) The module is equipped with two independent converters (sensor 1 and 2, sensor 3 and 4). The conversion time is valid for the number of channels connected to the corresponding converter.
3) To ensure accuracy, modules with a power loss <1.2 W must be inserted to the left and right of this module.
4) Based on the current resistance value.
5) Based on the entire resistance measurement range.

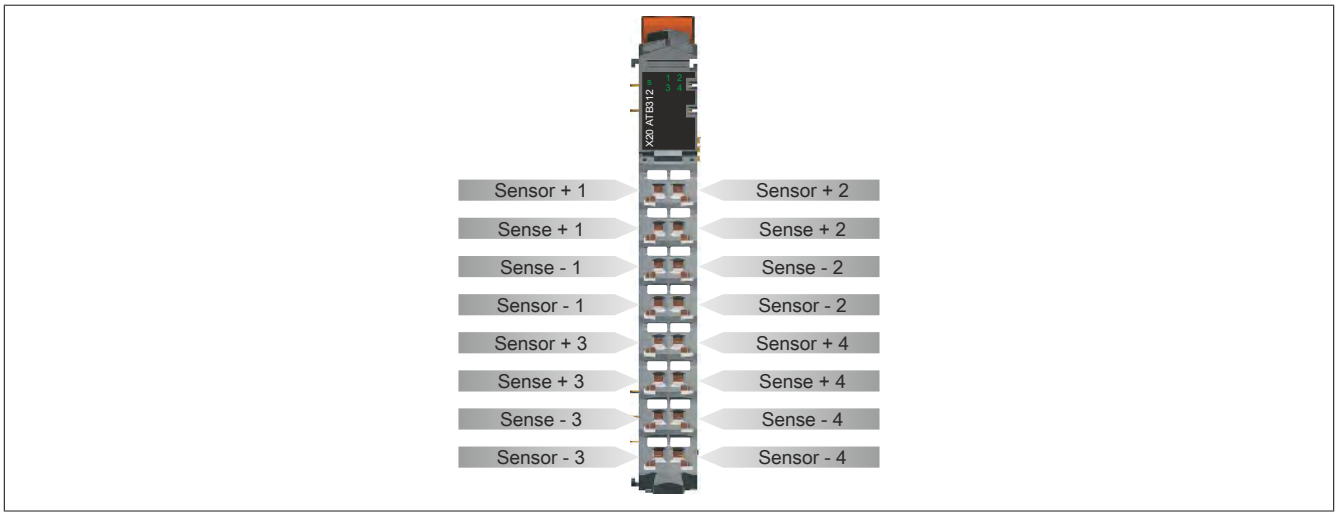
4.31.10.4 Status LEDs

For a description of the various operating modes, see section 2.11.1 "re LEDs".

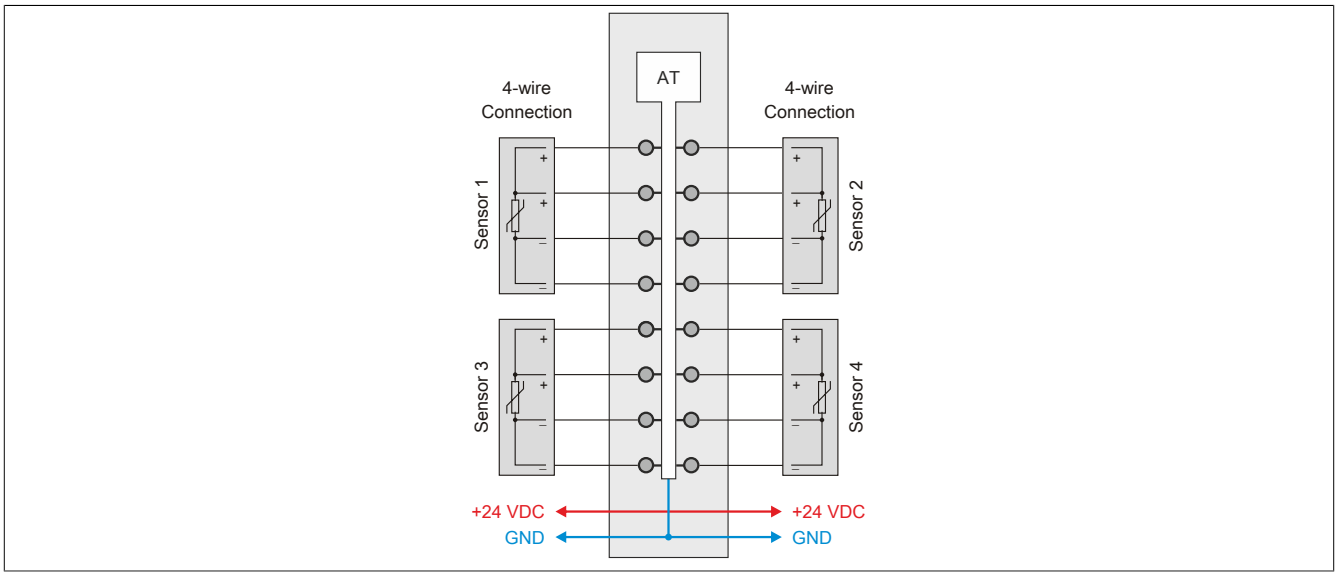
Image	LED	Color	Status	Description
	s	Green	Off	Module supply not connected
			Single flash	Reset mode
			Double flash	Boot mode (Updating firmware)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	Module supply not connected or everything OK
			On	Error or reset status
			Single flash	Parameter or conversion error[2]
		Red on / Green single flash		Invalid firmware
	1 - 4	Green	Off	Input turned off or not supplied
			Single flash	Parameter error[2]
			Double flash	Conversion error[2]
			Blinking	Overflow, underflow or open line
			On	A/D converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Parameter and conversion errors are indicated on both the red s-LED and the channel LED for the respective output at the same time.

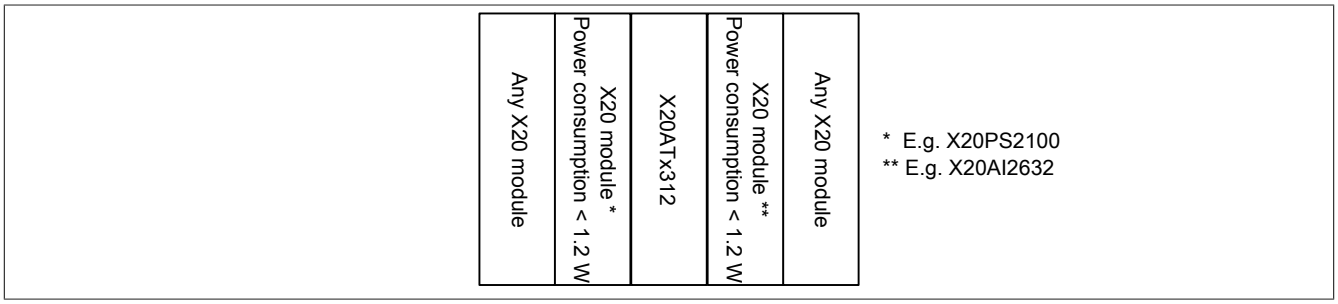
4.31.10.5 Pinout



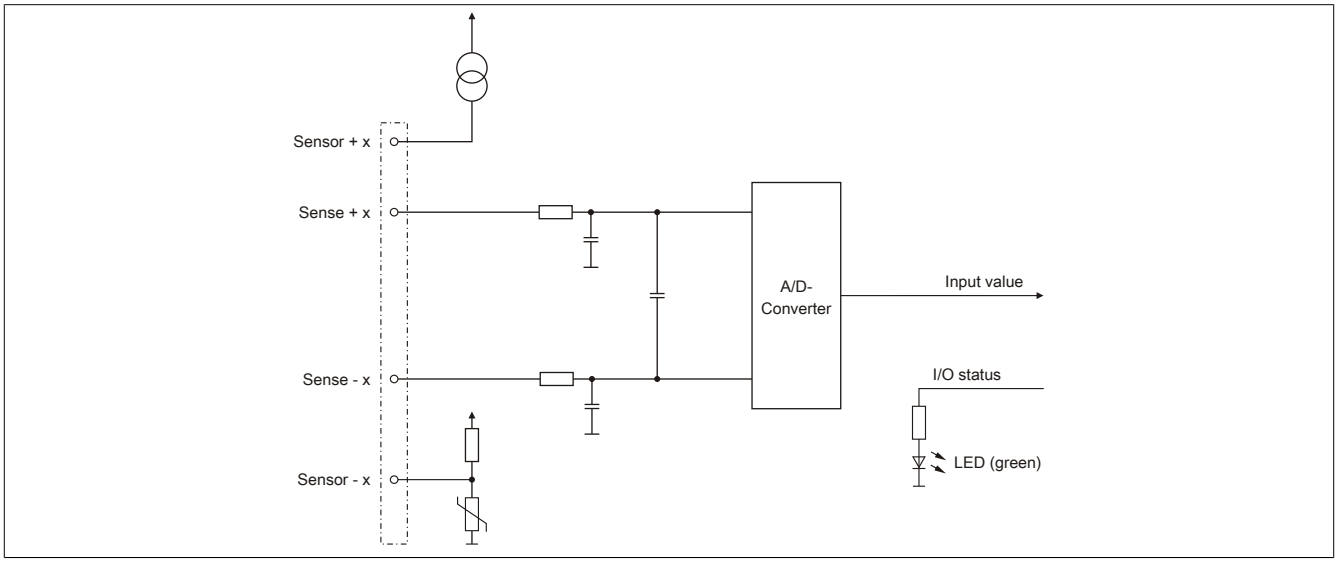
4.31.10.6 Connection example



To ensure accuracy, modules with a power consumption <1.2 W must be inserted to the left and right of this modules.



4.31.10.7 Input circuit diagram



4.31.10.8 Register description

4.31.10.8.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.10.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
130	InputFilter	UINT				•
134	ModeADC	UINT				•
Index * 64 + 450	SensorType0x (Index x = 1 to 4)	UINT				•
Index * 64 + 502	PreparationInterval0x (Index x = 1 to 4)	UINT				•
Index * 64 + 484	ReplaceUpper0x (Index x = 1 to 4)	DINT				•
Index * 64 + 476	ReplaceLower0x (Index x = 1 to 4)	DINT				•
Index * 64 + 468	UpperLimit0x (Index x = 1 to 4)	DINT				•
Index * 64 + 460	LowerLimit0x (Index x = 1 to 4)	DINT				•
Index * 64 + 490	Hysteresis0x (Index x = 1 to 4)	UINT				•
Index * 64 + 494	ErrorDelay0x (Index x = 1 to 4)	UINT				•
Index * 64 + 498	SumErrorDelay0x (Index x = 1 to 4)	UINT				•
Communication						
Index * 4 - 4	Temperature0x (Index x = 1 to 4)	DINT	•			
	Resistor0x (Index x = 1 to 4)	UDINT				
Index * 64 + 196	Measurand0x (Index x = 1 to 4)	DINT		•		
Index * 64 + 217	IOCycleCounter0x (Index x = 1 to 4)	USINT	•			
Index * 64 + 218	IOCycleCounter0x (Index x = 1 to 4)	UINT	•			
Index * 64 + 210	Sampletime0x (Index x = 1 to 4)	INT	•			
Index * 64 + 212	Sampletime0x (Index x = 1 to 4)	DINT	•			
Index * 64 + 233	Status0x (Index x = 1 to 4)	USINT	•			
	Underrun0x	Bit 0				
	Overrun0x	Bit 1				
	OpenLine0x	Bit 2				
	ConverterFault0x	Bit 4				
	SumFault0x	Bit 5				
	ParameterFault0x	Bit 6				
	IoSupplyFault0x	Bit 7				

4.31.10.8.3 Function model 254 - Bus Controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
130	-	InputFilter	UINT				●
134	-	ModeADC	UINT				●
Index * 64 + 450	-	SensorType0x (Index x = 1 to 4)	UINT				●
Index * 64 + 502	-	PreparationInterval0x (Index x = 1 to 4)	UINT				●
Index * 64 + 484	-	ReplaceUpper0x (Index x = 1 to 4)	DINT				●
Index * 64 + 476	-	ReplaceLower0x (Index x = 1 to 4)	DINT				●
Index * 64 + 468	-	UpperLimit0x (Index x = 1 to 4)	DINT				●
Index * 64 + 460	-	LowerLimit0x (Index x = 1 to 4)	DINT				●
Index * 64 + 490	-	Hysteresis0x (Index x = 1 to 4)	UINT				●
Index * 64 + 494	-	ErrorDelay0x (Index x = 1 to 4)	UINT				●
Index * 64 + 498	-	SumErrorDelay0x (Index x = 1 to 4)	UINT				●
Communication							
Index * 4 - 4	Index * 4 - 4	Temperature0x (Index x = 1 to 4)	DINT	●			
		Resistor0x (Index x = 1 to 4)	UDINT				
Index * 64 + 217	-	IOCycleCounter0x (Index x = 1 to 4)	USINT		●		
30	-	Status01To04	USINT		●		

1) The offset specifies where the register is within the CAN object.

4.31.10.8.3.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN-I/O 1.

4.31.10.8.4 Configuration of the A/D converter

4.31.10.8.4.1 Setting the conversion rate

Name:
InputFilter

This register can be used to set the conversion rate for the Analog/Digital converter.

Data type	Value
UINT	5 to 1023

Information:

The lower the conversion interval is set, the more precisely the value can be converted. However, this also increases the I/O update time.

4.31.10.8.4.2 A/D converter operating mode

Name:
ModeADC

This register can be used to set the operating mode for the Analog/Digital converter.

The individual options allow faster digitalization of the analog values, but this also reduces the precision of the measured values. The default value is 0.

Data type	Value
UINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	Chopper mode	0	Alternating amplification of the analog value
		1	Chopper mode off
1	Order of the SINC filter	0	SINC4
		1	SINC3
2 - 15	Reserved	-	-

The following rules apply:

ConversionTime(SINC3) = ConversionTime(SINC4) - 1 x ConversionCycle
ConversionTime(without Chop) = 0.5 x ConversionTime(Chop)

4.31.10.8.5 Configuring the measurement channels

Each temperature measurement channel can be configured independently. All the registers required for this purpose by each channel are arranged separately.

4.31.10.8.5.1 Channel parameters

Name:
SensorType01 to SensorType04

This register defines the basic behavior of the channel.
The default value is 0x81.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	Sensor type with unit and resolution	001	PT100 [10 mK/bit] - Temperature measurement
		010	PT100 [1 mΩ/bit] - Resistance measurement
		011 to 111	Reserved
3 - 4	Reserved	-	
5	Replacement value strategy	0	Static replacement
		1	Retain last valid value
6	Monitoring the user-defined limit values	0	Switch off additional limits
		1	Switch on additional limits
7	Channel (on/off)	0	Switch off the entire channel
		1	Switch on the channel
8 - 15	Reserved	-	

4.31.10.8.6 Configuring the replacement value strategy

If a measured value is detected that is outside the permitted value range, the behavior of the input register must still remain clearly defined. The module provides the user two different options for this purpose.

Retain last valid value

With this strategy, the determined measured value is stored temporarily for a specific time and written to the input register after a delay. If an invalid measured value is detected, this value and all values that have been stored temporarily are discarded. The last valid input register value is retained. To update the value in the input register, there must be enough valid values stored in the temporary buffer. The number needed is determined by the time period specified in "PreparationInterval0x".

Replace with static value

With this strategy, the measured value is written to the input register without delay. If an invalid value occurs, it is replaced by a static value that has been predefined by the user.

4.31.10.8.6.1 Preparation interval

Name:
PreparationInterval01 to PreparationInterval04

This register defines the time interval in which the measured value is checked before being passed on.

Data type	Value
UINT	0 to 65535 (x 0.1 ms)

Information:

This register must be defined if the replacement value strategy "Retain last valid value" was selected in register "SensorType0x".

4.31.10.8.6.2 Static replacement value when exceeding the upper limit

Name:
ReplaceUpper01 to ReplaceUpper04

This register is used to defined a replacement value that is output in place of the invalid measured value if the upper limit is violated.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Information:

This register must be defined if the replacement value strategy "Replace with static value" was selected in register "SensorType0x".

4.31.10.8.6.3 Static replacement value when falling below the lower limit

Name:
ReplaceLower01 to ReplaceLower04

This register is used to defined a replacement value that is output in place of the invalid measured value if the lower limit is violated.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Information:

This register must be defined if the replacement value strategy "Replace with static value" was selected in register "SensorType0x".

4.31.10.8.7 Configuring the user-defined limit values

This module provides the user the option to specify user-defined limits. If the valid measurement range is reduced in this way, the behavior of the replacement value strategy is more likely to be applied.

Valid measurement range

The valid range is derived from the properties of the sensor being used or the hardware and firmware of the respective B&R module. These values cannot be changed by the user.

Valid range of values

The range of values is always within the valid measurement range. The range of values can be adapted to the requirements of the application by specifying the upper and lower limit value.

4.31.10.8.7.1 Upper limit value

Name:
UpperLimit01 to UpperLimit04

This register specifies the upper limit value. The values entered should be within the valid measurement range.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.31.10.8.7.2 Lower limit value

Name:
LowerLimit01 to LowerLimit04

This register specifies the lower limit value. The values entered should be within the valid measurement range.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.31.10.8.7.3 Hysteresis

Name
Hysteresis01 to Hysteresis04

A hysteresis can be set in order to avoid frequent status changes in the measurement range close to the limit value. Here, a small section is defined at the edge of the valid range of values where the measured values retain the status (valid or invalid) of the previous measured value.

Data type	Value
UINT	0 to 65535

4.31.10.8.8 Configuring status messages

Errors are detected by the module and sent to the application. When using Function model 0 - Standard, the trigger behavior of these error messages can be influenced by the "Delay" register.

In Automation Studio, an error message can be read either packed as the entire register or individually as bits.

4.31.10.8.8.1 Delaying error messages

Name:
ErrorDelay01 to ErrorDelay04

In order to avoid false alarms due to short-term measurement variations, the status messages sent to the PLC can be delayed. This register determines the number of A/D conversions in which an error must exist before an error message is sent.

Data type	Value
UINT	0 to 65535 [A/D conversions]

4.31.10.8.8.2 Delaying the sum error message

Name:
SumErrorDelay01 to SumErrorDelay04

This register can be used to set the delay used when sending bit 5 of the "Status0x" register to the PLC independent of the other status messages.

The sum error can be delayed separately, independent of all other status messages.

Data type	Value
UINT	0 to 65535 [ms]

4.31.10.8.9 Communication

The received temperature data is assigned a timestamp and, depending on the configuration, made available with different register names and data types.

4.31.10.8.9.1 Measured value – Temperature

Name:
Temperature01 to Temperature04

If the channel is configured for resistance measurement, the current temperature value is made available in this register.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

4.31.10.8.9.2 Measured value – Resistance

Name:
Resistor01 to Resistor04

If the channel is configured for resistance measurement, the current resistance value is made available in this register.

Data type	Value
UDINT	0 to 4,294,967,295

4.31.10.8.9.3 Measured value – Unweighted

Name:
Measurand01 to Measurand04

When using the AsIoAcc library, the unweighted measurement can be accessed via this register. This refers to a measured value that is within the valid measurement range and has not yet been compared with the user-defined limits.

Data type	Value
DINT	-2,147,483,648 to 2,147,483,647

Information:

If no user-defined limits are configured, the value of this register does not differ from the temperature or resistance value.

4.31.10.8.9.4 Cycle counter

Name:
IOCycleCounter01 to IOCycleCounter04

This register is used to provide a continuous counter for the application that is incremented each time a temperature value is read.

Data type	Value
USINT	0 to 32767 [A/D conversions]
UINT	0 to 65535 [A/D conversions]

4.31.10.8.9.5 Sampling time

Name:
Sampletime01 to Sampletime04

This register is used to provide the application the net time until the temperature will be evaluated.

Data type	Value
INT	-32,768 to 32,767 [µs]
DINT	-2,147,483,648 to 2,147,483,647 [µs]

Information:

The SDC library requires a 16-bit value for the sampling time. It is therefore also prepared as a 16-bit value.

4.31.10.8.9.6 Status messages

Name:
Status01 to Status04

The register bits are set if an error has been diagnosed and the error remains longer than the delay configured in the "ErrorDelay0x" register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Underrun01 to Underrun04	0	No error
		1	Value below the permitted range
1	Overrun01 to Overrun04	0	No error
		1	Value above the permitted range
2	OpenLine01 to OpenLine04	0	No error
		1	Sensor is not connected correctly
3	Reserved	-	
4	ConverterFault01 to ConverterFault04	0	No error
		1	Invalid A/D converter output
5	SumFault01 to SumFault04	0	No error
		1	Composite error
6	ParameterFault01 to ParameterFault04	0	No error
		1	The 4.31.10.8.5.1 "SensorType0x" register is faulty
7	IoSupplyFault01 to IoSupplyFault04	0	No error
		1	The supply voltage (I/O) is faulty

4.31.10.8.9.7 Status messages for function model 254

Name:
Status01To04

The bits in this register are set if an error has been detected.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Underrun on channel 01	0	No error
		1	Value below the permitted range
1	Overrun on channel 01	0	No error
		1	Value above the permitted range
...		...	
6	Underrun on channel 04	0	No error
		1	Value below the permitted range
7	Overrun on channel 04	0	No error
		1	Value above the permitted range

Information:

If an open line is detected on a channel, then both error messages will be displayed at the same time.

4.31.10.8.10 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.31.10.8.11 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 ms

4.31.11 X20ATC402

4.31.11.1 General information

The module is equipped with 6 inputs for J, K, N, S, B, R, E, C and T thermocouple sensors.

This module can also be equipped with the X20TB1E thermocouple terminal block with integrated PT1000 temperature sensors. This makes it possible to achieve optimal terminal temperature compensation.

- 6 channels for thermocouples
- For sensor types J, K, N, S, B, R, E, C, T, raw value measurement
- Integrated terminal temperature compensation
- 2x PT1000 sensor integrated in the terminal (X20TB1E)
- 2x external PT1000 sensor can be connected (X20TB1F)
- Configurable filter time

4.31.11.2 Order data

Model number	Short description	Figure
	Temperature measurement	
X20ATC402	X20 temperature input module, 6 thermocouple inputs, type J, K, N, S, B, R, E, C, T, 2x PT1000 integrated for terminal temperature compensation, with 1x X20TB1E terminal block, order terminal block separately	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB1E	X20 terminal block, 12-pin, 24 VDC keyed, 2x PT1000 integrated for terminal temperature compensation	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 746: X20ATC402 - Order data

4.31.11.3 Technical data

Product ID	X20ATC402
Short description	
I/O module	6 inputs for thermocouples
General information	
B&R ID code	0xBB99
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.85 W
Additional power dissipation caused by the actuators (resistive) [W]	-
Electrical isolation	
Channel - Bus	Yes
Channel - Channel	No
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1)]	Yes
KC	Yes
GOST-R	Yes
Thermocouple temperature inputs	
Input	Thermocouple
Digital converter resolution	16-bit
Filter time	Configurable between 1 and 200 ms

Table 747: X20ATC402 - Technical data

Product ID	X20ATC402
Conversion time	
Internal terminal temperature comp.	
n channels	(n + 2) * 4 * x ms [2]
External terminal temperature comp.	
1 channel	x ms [2]
n channels	n * 4 * x ms [2]
Remote temperature comp.	
n channels	(n + 2) * 4 * x ms [2]
Output format	INT
Measurement range	
Sensor temperature	
Type J: Fe-CuNi	-210 to 1200°C
Type K: NiCr-Ni	-270 to 1372°C
Type N: NiCrSi-NiSi	-270 to 1298°C
Type S: PtRh10-Pt	-50 to 1768°C
Type B: PtRh30-PtRh6	0 to 1820°C
Type R: PtRh13-Pt	-50 to 1760°C
Type E: NiCr-CuNi	-270 to 997°C
Type C: WRe5-WRe26	0 to 2310°C
Type T: Cu-CuNi	-270 to 400°C
Terminal temperature	-40 to 130°C
Voltage	±65.534 mV
Sensor standard	EN 60584
Resolution	
Sensor temperature	1 LSB = 0.1°C
Terminal temperature	1 LSB = 0.1°C
Voltage	Depending on gain, 1 LSB = 1 µV or 2 µV
Normalization	
Type J	-210 to 1200°C
Type K	-270 to 1372°C
Type N	-270 to 1298°C
Type S	-50 to 1768°C
Type B	0 to 1820°C
Type R	-50 to 1760°C
Type E	-270 to 997°C
Type C	0 to 2310°C
Type T	-270 to 400°C
Terminal temperature	-145 to 840°C
Voltage	Depending on gain ±32.767 mV or ±65.534 mV
Monitoring	
Range exceeded (neg.)	0x8001
Above upper range limit	0x7FFF
Open line	0x7FFF
Open inputs	0x7FFF
General error	0x8000
Conversion procedure	Sigma-delta
Linearization method	Internal
Permitted input signal	Max. ±15 V
Input filter	1st-order low pass / cutoff frequency 500 Hz
Max. error at 25°C	
Gain	0.04% [3]
Offset	
Type J	0.06% [4]
Type K	0.07% [4]
Type N	0.07% [4]
Type S	0.13% [4]
Type B	0.15% [4]
Type R	0.11% [4]
Type E	0.06% [4]
Type C	0.08% [4]
Type T	0.11% [4]
Voltage	0.015% [4]
Max. gain drift	
Channel	0.01 %/°C [3]
Terminal temperature	0.03 %/°C [3]

Table 747: X20ATC402 - Technical data

Product ID	X20ATC402
Max. offset drift	
Type J	0.0033 %/°C 4)
Type K	0.0042 %/°C 4)
Type N	0.0048 %/°C 4)
Type S	0.0123 %/°C 4)
Type B	0.0166 %/°C 4)
Type R	0.0109 %/°C 4)
Type E	0.003 %/°C 4)
Type C	0.0062 %/°C 4)
Type T	0.011 %/°C 4)
Terminal temperature	0.005 %/°C 4)
Voltage	0.003 %/°C 4)
Nonlinearity	
Channel	±0.004% 4)
Terminal temperature	±0.004% 3)
Terminal temperature compensation	
Operating modes	Internal/remote or external
Basic accuracy at 25°C without taking the PT1000 sensor into consideration	±0.06%
Accuracy of the internal terminal temperature	
With natural convection	±1.5°C after 20 min
With artificial convection	±3°C after 20 min
Common-mode rejection	
DC	>100 dB
50 Hz	>100 dB
60 Hz	>100 dB
Common-mode range	±14 V
Crosstalk between channels	>70 dB
Isolation voltage	
Between channel and bus	500 V_{eff}
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP20
Environmental conditions	
Temperature	
Operation	
Horizontal installation	-25 to 60°C
Vertical installation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical characteristics	
Note	Order 1x X20TB1E terminal block for internal/remote terminal temperature compensation separately Order 1x X20TB1F terminal block for external terminal temperature compensation separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 747: X20ATC402 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) With a 50 Hz filter, x = 20 ms (1 / 50 Hz = 20 ms)
3) Based on the current measured value.
4) Based on the entire measurement range.

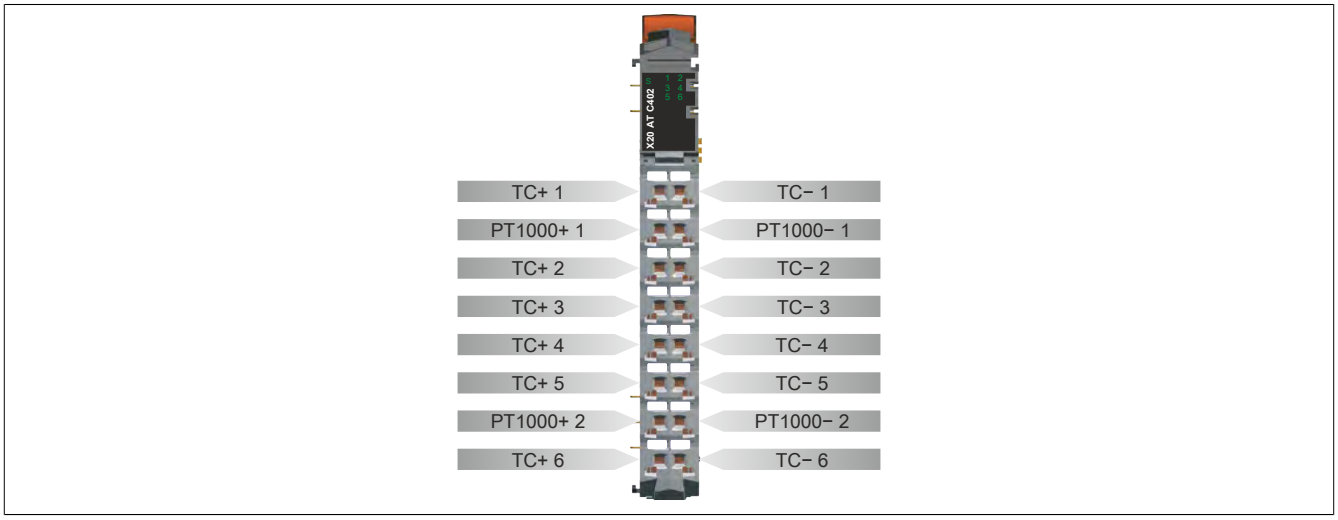
4.31.11.4 LED status indicators

For a description of the various operating modes, see section 2.11.1 "re LEDs".

Figure	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	A parameter or conversion error has occurred. This status is output in addition to a single/double flash on the channel LED of the analog input where the error occurs.
		Red on / Green single flash		Invalid firmware
	1 - 6	Green	Off	Input turned off or not supplied
			Single flash	A parameter error has occurred. A single flash is output on the red "s" module status LED.
			Double flash	A conversion error has occurred. A single flash is output on the red "s" module status LED.
			Blinking	Overflow, underflow or open line
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

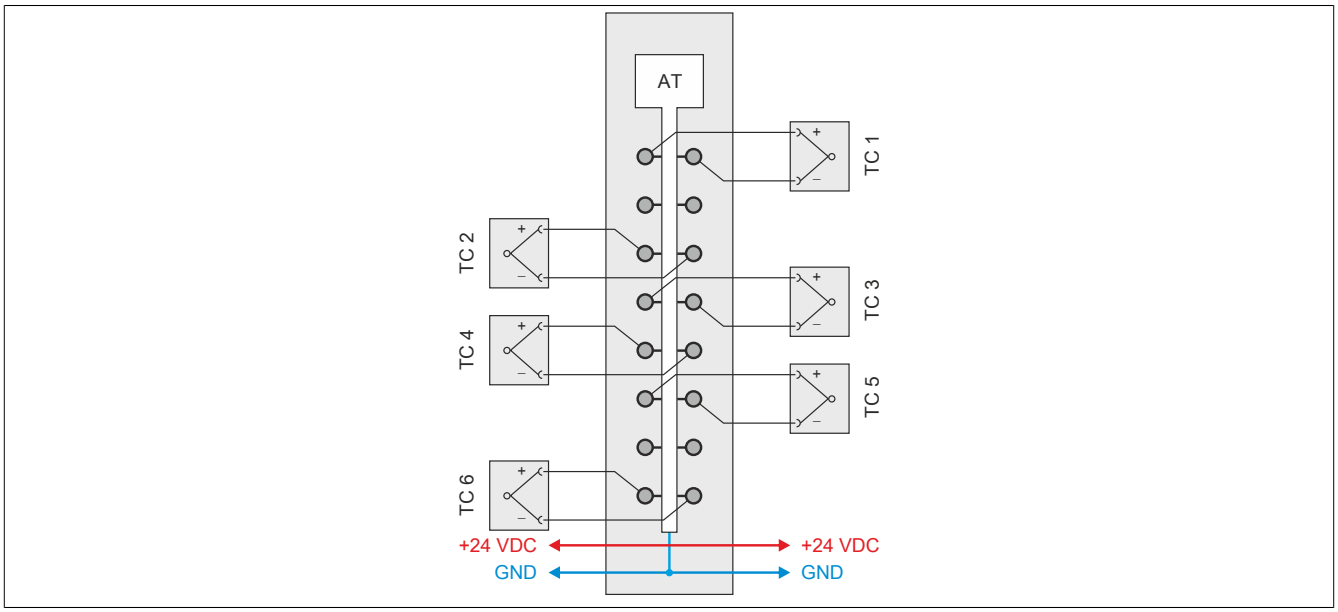
4.31.11.5 Pinout



4.31.11.6 Connection examples

Internal temperature compensation

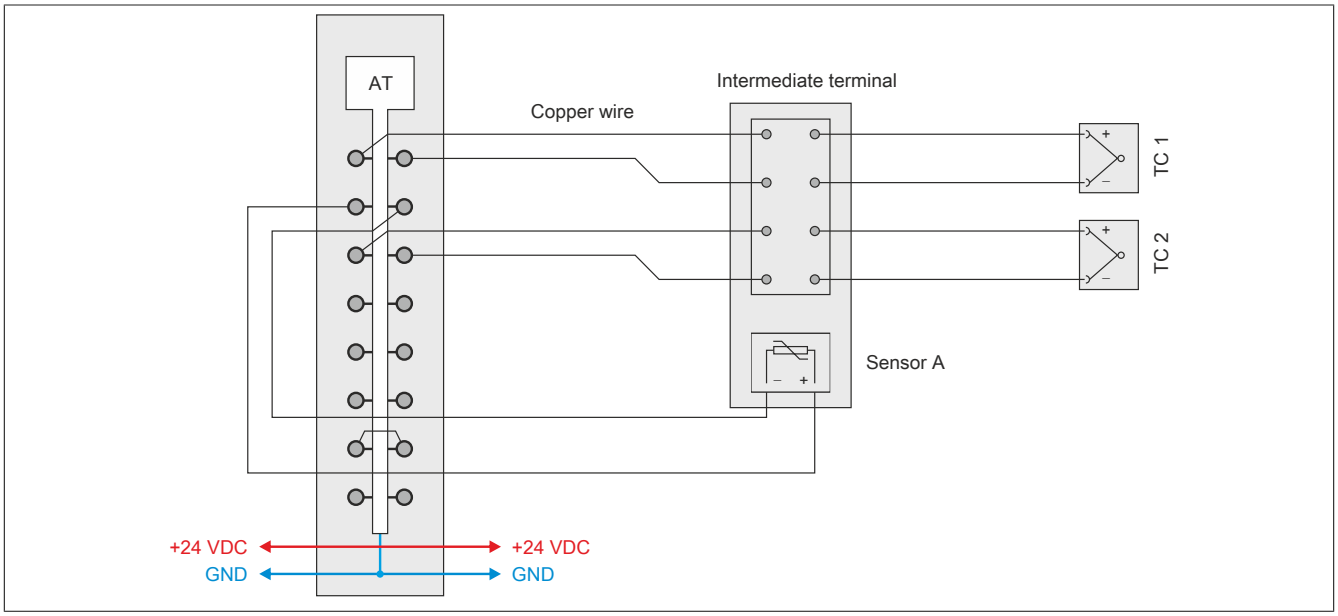
The thermocouple terminal block X20TB1E with integrated PT1000 sensors is used for internal temperature compensation.



Remote temperature compensation

The 16x standard terminal X20TB1F is used for remote temperature compensation. The external PT1000 sensors are connected to the module using 2-wire connections.

If Sensor B is not needed for temperature compensation, then the terminal points need to be bypassed.

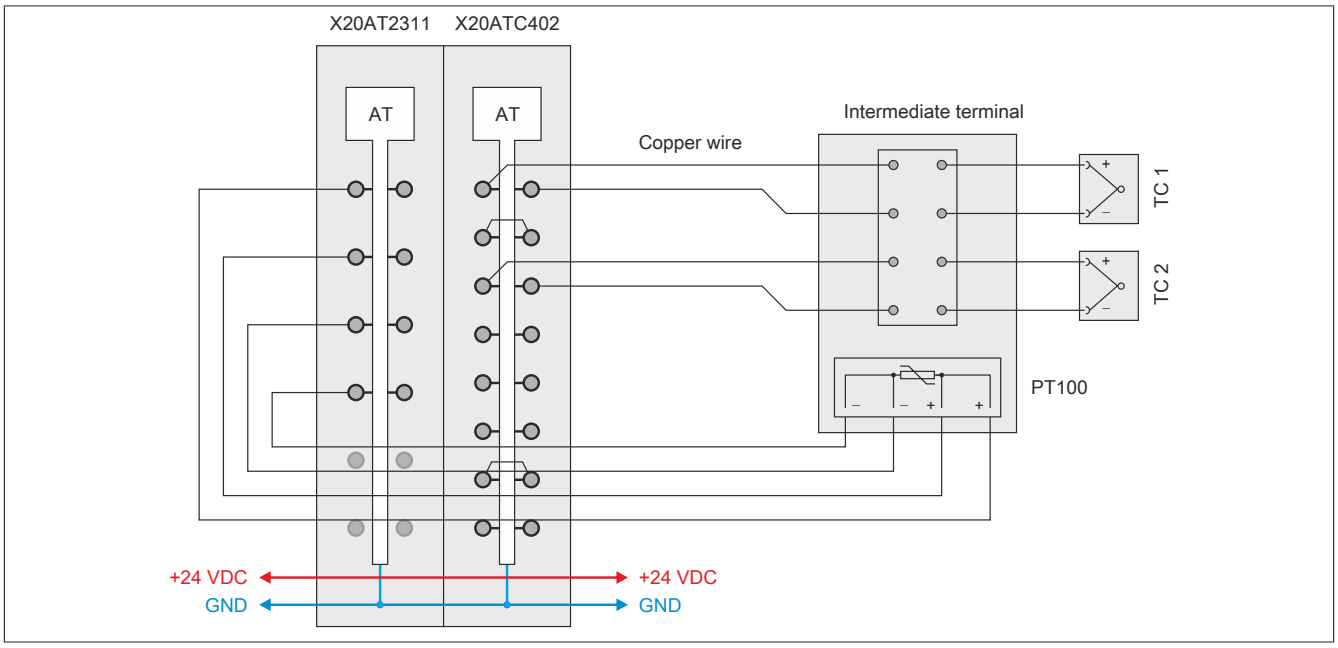


External temperature compensation

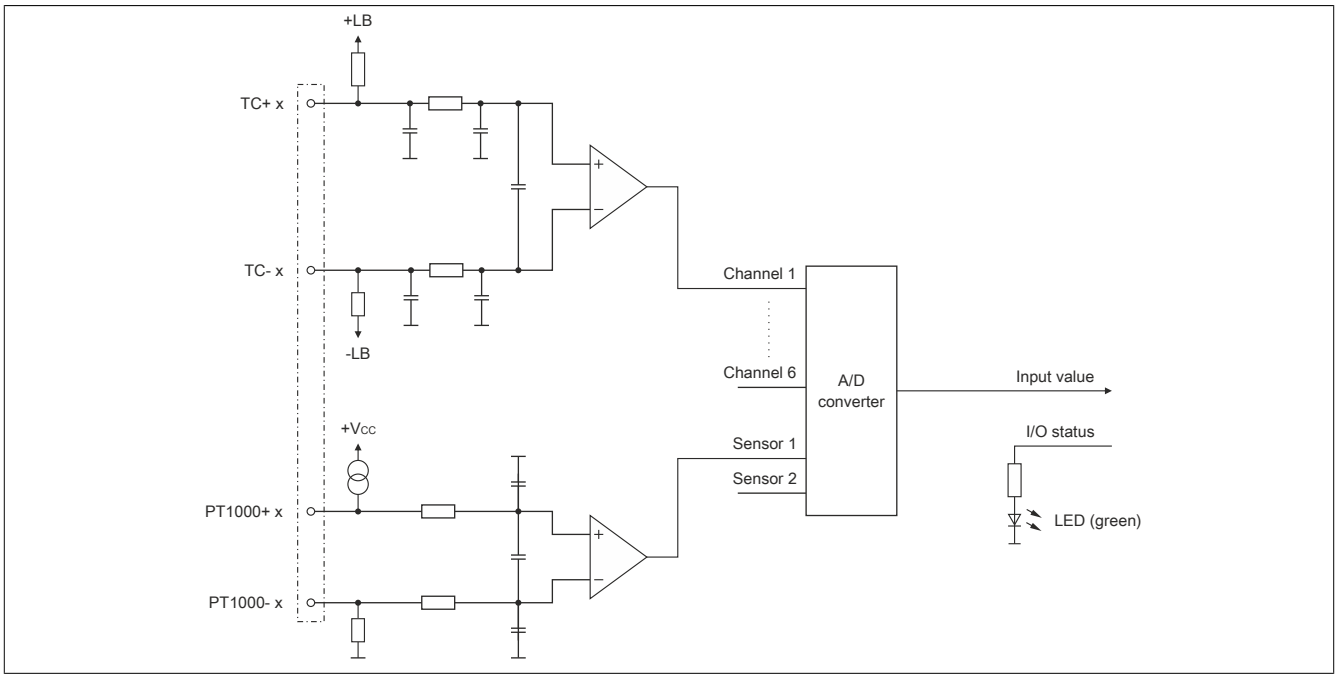
External compensation does not require the PT1000 values to be converted internally in the module. Instead, the reference temperatures have to be pre-processed in the program before being stored in the module. A separate register is available for each temperature channel to transfer an externally pre-processed compensation value.

In the following example, the compensation value is determined using the X20AT2311 temperature input module and a PT100 sensor on the intermediate terminal. The cold junction temperature determined externally is then made available to the X20ATC402 module via the respective I/O data points.

Since sensors A and B aren't needed for temperature compensation, the respective terminal points need to be bypassed.



4.31.11.7 Input circuit diagram



4.31.11.8 Increased precision

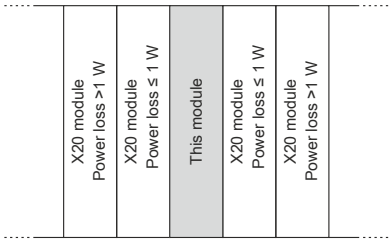
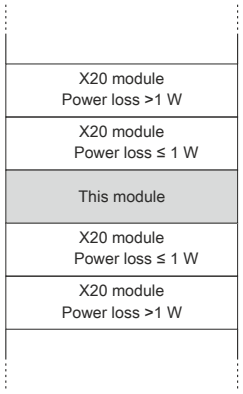
4.31.11.8.1 Internal temperature compensation

When using internal terminal temperature compensation, a temperature model must be defined in order to increase precision. A temperature model should be selected according to the following criteria:

- Thermal power loss of neighboring modules
- X20 system - Mounting orientation

4.31.11.8.1.1 Neighboring modules with low thermal power loss

The temperature model listed in the table must be configured according to the mounting orientation.

Horizontal installation	Vertical installation
	

The following temperature model must be set in the Cfo_SensorTypeCh0x register.

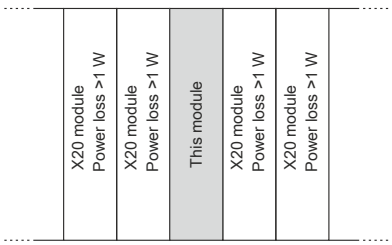
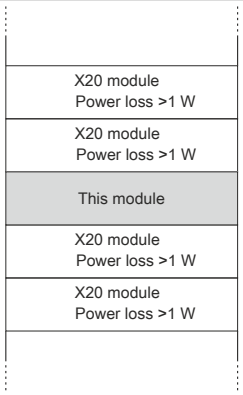
Bit 6 and 7	Temperature model	Bit 6 and 7	Temperature model
00	Horizontal installation, low thermal radiance <1W	10	Vertical installation, low thermal radiance <1W

Information:

The best results are achieved by placing a dummy module on both sides.

4.31.11.8.1.2 Neighboring modules with higher thermal power loss

The temperature model listed in the table must be configured according to the mounting orientation.

Horizontal installation	Vertical installation
	

The following temperature model must be set in the Cfo_SensorTypeCh0x register.

Bit 6 and 7	Temperature model	Bit 6 and 7	Temperature model
01	Horizontal installation, high thermal radiance >1 W	11	Vertical installation, high thermal radiance >1 W

4.31.11.8.2 Remote or external terminal temperature compensation

Setting up a remote or external cold junction can provide the most accurate temperature measurement in a machine or system.

The installation of a remote or external cold junction is especially helpful in the following cases.

- There is no module next to the temperature module
- With strongly fluctuating ambient conditions (draft, temperature)
- External fan is used in the control cabinet

4.31.11.9 Register description

4.31.11.9.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

The general data points are described in section 4.33 "General data points".

4.31.11.9.2 Function model 0 - Standard

Register	Product ID	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module configuration						
1026	Cfo_InputFilter	UINT				•
Compensation						
1030 1034	Cfo_ClampTypeA Cfo_ClampTypeB	UINT				•
266 270	CompensationValueA CompensationValueB	INT	•	•		
1038 1042	Cfo_ClampOffsetA Cfo_ClampOffsetB	INT				•
261 263	CompensationStatusA CompensationStatusB	USINT	•	•		
	UnderrunA UnderrunB	Bit 0				
	OverrunA OverrunB	Bit 1				
	OpenLineA OpenLineB	Bit 2				
	ConverterFaultA ConverterFaultB	Bit 4				
	SumFaultA SumFaultB	Bit 5				
	ParameterFaultA ParameterFaultB	Bit 6				
Index*4 + 766	ExternalCompensation01 ExternalCompensation[02]	INT			•	•
Temperature measurement - Configuration						
Index*64 + 1026	Cfo_SensorType01 Cfo_SensorType[02...06]	UINT				•
Index*64 + 1058	Cfo_PreparationInterval01 Cfo_PreparationInterval[02...06]	UINT				•
Index*64 + 1046	Cfo_ReplaceUpper01 Cfo_ReplaceUpper[02...06]	INT				•
Index*64 + 1042	Cfo_ReplaceLower01]Cfo_ReplaceLower[02...06	INT				•
Index*64 + 1034	Cfo_UpperLimit01 Cfo_UpperLimit[02...06]	INT				•
Index*64 + 1030	Cfo_LowerLimit01 Cfo_LowerLimit[02...06]	INT				•
Index*64 + 1038	Cfo_Hysteresis01 Cfo_Hysteresis[02...06]	INT				•
Index*64 + 1050	Cfo_ErrorDelay01 Cfo_ErrorDelay[02...06]	UINT				•
Index*64 + 1054	Cfo_SumErrorDelay01 Cfo_SumErrorDelay[02...06]	UINT				•
Temperature measurement						
Index*64 + 262	TemperatureEvaluated01 TemperatureEvaluated[02...06]	INT	•	•		
Index*64 + 258	Measurand01 Measurand[02...06]	INT	•	•		
Index*64 + 274	SampleTime01_16bit SampleTime[02...06]_16bit	INT	•	•		
Index*64 + 276	SampleTime01_32bit SampleTime[02...06]_32bit	DINT	•	•		
Index*64 + 281	IOCycleCounter01_8bit IOCycleCounter[02...06]_8bit	USINT	•	•		
Index*64 + 282	IOCycleCounter01_16bit IOCycleCounter[02...06]_16bit	UINT	•	•		
Index*64 + 269	Status01 Status[02...06]	USINT				
	Underrun01 Underrun[02…06]	Bit 0				
	Overrun01 Overrun[02…06]	Bit 1				
	OpenLine01 OpenLine[02…06]	Bit 2	•	•		
	CompensationFault01 CompensationFault[02…06]	Bit 3				
	ConverterFault01 ConverterFault[02…06]	Bit 4				
	SumFault01 SumFault[02…06]	Bit 5				
	ParameterFault01 ParameterFault[02…06]	Bit 6				

4.31.11.9.3 Function model 254 - Bus controller

Register	Product ID	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module configuration						
1026	Cfo_InputFilter	UINT		•		•
Compensation						
1030 1034	Cfo_ClampTypeA Cfo_ClampTypeB	UINT		•		•
266 270	CompensationValueA CompensationValueB	INT	•	•		
1038 1042	Cfo_ClampOffsetA Cfo_ClampOffsetB	INT		•		•
261 263	CompensationStatusA CompensationStatusB	USINT	•	•		
	UnderrunA UnderrunB	Bit 0				
	OverrunA OverrunB	Bit 1				
	OpenLineA OpenLineB	Bit 2				
	ConverterFaultA ConverterFaultB	Bit 4				
	SumFaultA SumFaultB	Bit 5				
	ParameterFaultA ParameterFaultB	Bit 6				
Index*4 + 766	ExternalCompensation01 ExternalCompensation[02...06]	INT		•	•	•
Temperature measurement - Configuration						
Index*64 + 1026	Cfo_SensorType01 Cfo_SensorType[02...06]	UINT		•		•
Index*64 + 1058	Cfo_PreparationInterval01 Cfo_PreparationInterval[02...06]	UINT		•		•
Index*64 + 1046	Cfo_ReplaceUpper01 Cfo_ReplaceUpper[02...06]	INT		•		•
Index*64 + 1042	Cfo_ReplaceLower01 Cfo_ReplaceLower[02...06]	INT		•		•
Index*64 + 1034	Cfo_UpperLimit01 Cfo_UpperLimit[02...06]	INT		•		•
Index*64 + 1030	Cfo_LowerLimit01 Cfo_LowerLimit[02...06]	INT		•		•
Index*64 + 1038	Cfo_Hysteresis01 Cfo_Hysteresis[02...06]	INT		•		•
Temperature measurement						
0	TemperatureEvaluated01_CANIO	INT	•	•		
2	TemperatureEvaluated02_CANIO	INT	•	•		
4	TemperatureEvaluated03_CANIO	INT	•	•		
8	TemperatureEvaluated04_CANIO	INT	•	•		
10	TemperatureEvaluated05_CANIO	INT	•	•		
12	TemperatureEvaluated06_CANIO	INT	•	•		
Index*64 + 281	IOCycleCounter01_8bit IOCycleCounter[02...06]_8bit	USINT	•	•		
30	ModuleStatus01To04	USINT	•	•		
31	ModuleStatus05To06	USINT	•	•		

4.31.11.9.3.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN-I/O.

4.31.11.9.4 Module configuration

The X20ATC402 is an I/O module for temperature measurement. It has six non electrically isolated channels. The module requires a 16-pin standard terminal or the 16-pin terminal with 2 integrated PT1000 inputs for temperature compensation. The remaining six channels can be equipped with thermocouples and record the difference in temperature between the reference point (e.g. the terminal) and the actual measurement point.

4.31.11.9.4.1 I/O update time

The analog/digital converter must convert up to eight values. After switching between two inputs there are four measurements in order to obtain a meaningful value. Since not all inputs need to be used, the actual I/O update time may vary greatly.

The following formula can be used to calculate the I/O update time:

Conversion rate * 4 * (number of converted compensation values + number of converted temperature differences)

4.31.11.9.4.2 InputFilter

Designations (pChannelName):
Cfo_InputFilter

The "Filter" register allows the user to set the conversion interval for the analog/digital converter.

Data type	Values [msec]
UINT	0…65535

Information:

The lower the conversion interval is set, the more precisely the value can be converted. However, this also increases the I/O update time.

The following formula applies:

Conversion rate = (4920000/1024) * InputFilter

4.31.11.9.5 Compensation

The measurement process is based on the interaction between the temperature sensors and the thermocouples. Each thermocouple measures the difference in temperature between the measurement point and the terminal. To calculate the absolute temperature, the measurement value must be placed in relation to a compensation value. The compensation value can be provided to the module via cyclic data points or read in via PT1000 temperature sensors.

4.31.11.9.5.1 Internal compensation

The input channels of the PT1000 temperature sensor are used for internal compensation.
When using the 16-pin standard terminal (X20TB1F), the reference point for compensation measurements can be moved from the terminal to a thermally isolated location. Using such a "remote terminal" makes it possible to achieve very precise measurement results. There are two of each configuration register required for this, which allows the two measurements to be configured independently of one another. The reference temperatures can be displayed and calibrated using an offset value.

Information:

To avoid unnecessary traffic on the X2X bus, the compensation registers should only be transferred cyclically during the fine-tuning process and for service and maintenance purposes. The information is generally not required during normal operation.

Alternatively, the module can be operated with a special 16-pin terminal (X20TB1E). This is equipped with two PT1000 temperature sensors and is used to determine the default values. To allow for this compensation method, extra temperature distribution models have been built into the module.

ClampType

Designations (pChannelName):
Cfo_ClampTypeA
Cfo_ClampTypeB

The ClampType register specifies the type of sensor and registers the conversion of the compensation value on the ADC.

Data type	Values
UINT	See bit structure Bus controller default: 0

Bit structure:

Bit	Product ID		Note
0	Sensor type	0	PT1000
1	Compensation channel (on/off)	0	Channel not converted by the ADC
		1	Channel registered on the ADC
2	Compensation value (see CompensationValue)	0	Prepare as temperature value
		1	Prepare as resistance value
3	Reserved	-	
4	Installation parameter	0	Horizontal installation
		1	Vertical installation
5	Thermal radiance	0	Low
		1	High
6…15	Reserved	-	

Four different temperature distribution models have been built into the module, optimized for the various ways the module can be installed. The respective model is selected using the following bits:

Installation parameter:
If the X2X bus modules are installed next to each other, the installation parameter should be set to 0.
If the X2X bus modules are installed above and below each other, the installation parameter should be set to 1.

Thermal radiance:
If an active module that generates additional heat is installed in the immediate vicinity of the temperature module, then this parameter should be set to 1.

CompensationValue

Designations (pChannelName):
CompensationValueA
CompensationValueB

The "CompensationValue" registers can be used to read the compensation value. Depending on how the "ClampType" register is set, it is output as either a temperature or resistance value.

Data type	Values [0.1°C or 0.1 Ohm]
INT	-32767…32767

ClampOffset

Designations (pChannelName):
Cfo_ClampOffsetA
Cfo_ClampOffsetB

The "ClampOffset" registers define the offsets that are deducted from the respective compensation values.

Data type	Values [0.1 Ohm]
INT	-32767…32767 Bus controller default: 0

CompensationStatus

Designations (pChannelName):
CompensationStatusA
CompensationStatusB

The "CompensationStatus" registers provide information about the current status of the respective compensation value. The structure is based on the status registers of the six measurement channels.

Data type	Values
USINT	See bit structure

Bit structure:

Bit	Product ID		Note
0	UnderrunA UnderrunB	0	No error
		1	Value below the permitted range
1	OverrunA OverrunB	0	No error
		1	Value above the permitted range
2	OpenLineA OpenLineB	0	No error
		1	Open line
3	(Compensation error)	-	no meaning
4	ConverterFaultA ConverterFaultB	0	No error
		1	Converter error
5	SumFaultA SumFaultB	0	No error
		1	Immediate composite error
6	ParameterFaultA ParameterFaultB	0	No error
		1	Setting for "ClampType" register not permitted
7	Reserved	-	

4.31.11.9.5.2 External compensation

With external compensation, there is no need for internal conversion of the PT1000 values in the module. Instead, the reference temperatures have to be pre-processed in the program before being stored in the module. Additional output registers are provided in the I/O mapping to allow for the exchange.

ExternalCompensation

Designations (pChannelName):
ExternalCompensation01
ExternalCompensation[02…06]

The "ExternalCompensation" registers can be used to send an externally generated compensation value from the PLC program to the module. There is a separate register for each temperature channel.

Data type	Values [0.1°C]
INT	-32767…32767

4.31.11.9.6 Temperature measurement - Configuration

The temperature measurement channels can be configured independently of each other. All the registers required for each channel are arranged separately.
The "SensorType" register needs to be adjusted in order to enable a temperature channel. The rest of the registers complement this configuration and only need to be defined as required.

4.31.11.9.6.1 SensorType

Designations (pChannelName):
Cfo_SensorType01
Cfo_SensorType[02...06]

The "SensorType" registers control the basic functionality of a temperature channel.

Data type	Values
UINT	See bit structure

Bit structure:

Bit	Product ID		Note
0…5	Standardization		Sensor type used
6…7	Reserved	-	
8…11	Method of compensation		Reference point
12	Reserved	-	
13	Replacement value	0	Replace with static preset value
		1	Retain last valid value
14	Additional user limits	0	Valid value range for sensor type
		1	Additional restrictions to value range
15	Temperature channel (on/off)	0	Channel not converted by the ADC
		1	Channel registered on the ADC

Sensor type:
00…000000 - Sensor J (Fe-CuNi)
01…000001 - Sensor K (NiCr-Ni)
02…000010 - Sensor N (NiCrSi-NiSi)
03…000011 - Sensor S (PtRh10-Pt)
04…000100 - Sensor R (PtRh13-Pt)
05…000101 - Sensor C (WRe5-WRe26)
06…000110 - Sensor T (Cu-CuNi)
07…000111 - Sensor B (PtRh30-PtRh6)
08…001000 - Sensor E (NiCr-CuNi)
Raw values without linearization and temperature compensation
61…111101 - RawValue1; Resolution 1.0625 µV; Measurement range ±35 mV
62…111110 - RawValue2; Resolution 2.125 µV; Measurement range ±70 mV

Reference point:
0…0000 - Compensation A
1…0001 - Compensation B
4…0100 - Temperature model implemented for special terminal
8…1000 - External compensation

4.31.11.9.6.2 PreparationInterval

Name (pChannelName):
Cfo_PreparationInterval01
Cfo_PreparationInterval[02…06]

If the last valid measurement value should be kept when violating the limit value, then PreparationInterval must be defined. The measurement values continue to be acquired and converted according to the configured I/O update time. They are then checked and discarded if they do not meet the specifications. When an error does not occur, therefore, the measurement value acquired two preparation intervals ago is constantly output.

Data type	Values [0.1 ms]
UINT	0…65535

How it works:
Measured values are converted at the configured conversion rate and saved to measurement value memory. The current contents of the measurement value memory are checked within the configured interval. If a permissible value is present, then the contents of the buffer memory are passed to output memory and the contents of the measurement value memory are passed to the buffer.
If the check turns up an impermissible value, then the contents of the measurement value memory are discarded. The copy direction between the output and buffer memory reverses and the last valid value continues to be output.

"Application" for the value being measured (analog)	
↓	Condition: - Conversion interval (ADC) elapsed
"Measurement value memory" Measurement value (digital)	
↓	Condition: - PreparationInterval elapsed - Measurement value permissible
"Buffer" Last valid value	
↓	Condition: - PreparationInterval elapsed - Measurement value permissible
"Output memory" Next-to-last valid/ displayed value	

Information:

If configured to keep the last valid value, the delay time from measuring to outputting the value will be at least twice the preparation interval. In the worst case scenario, this can also take twice the interval time plus the configured ADC conversion rate.

Information:

The registers are only set for the channel when "SensorType" bit 13 is set.

4.31.11.9.6.3 ReplaceUpper, ReplaceLower

Names (pChannelName):
Cfo_ReplaceUpper01
Cfo_ReplaceUpper[02…06]

Cfo_ReplaceLower01
Cfo_ReplaceLower[02…06]

The "Replace" register is used to define the static values to be displayed instead of the current measurement value when the limit is violated.

Data type	Values
INT	-32767…32767

Information:

The registers are only set for the channel when "SensorType" bit 13 is not set.

4.31.11.9.6.4 UpperLimit, LowerLimit

Condition: The registers are only set for the channel when "ClampType" bit 14 is set.

Names (pChannelName):
Cfo_UpperLimit01
Cfo_UpperLimit[02…06]

Cfo_LowerLimit01
Cfo_LowerLimit[02…06]

If the value range needs to be restricted further, the "UpperLimit" and "LowerLimit registers can be used to enter new user-specific limit values.

Data type	Values
INT	-32767…32767
UINT	0...65535

4.31.11.9.6.5 Hysteresis

Designations (pChannelName):
Cfo_Hysteresis01
Cfo_Hysteresis[02…06]

If the user-specific limit values are being used, then a hysteresis range should also be defined. The "Hysteresis" registers configure how far a limit value can be exceeded before a response is triggered.

Data type	Values
INT	-32767…32767
UINT	0...65535

Information:

The registers are only set for the channel when "ClampType" bit 14 is set.

4.31.11.9.6.6 ErrorDelay

Names (pChannelName):
Cfo_ErrorDelay01
Cfo_ErrorDelay[02…06]

This register specifies the number of consecutive conversion procedures where an error is pending until the corresponding individual error status bit is set. The delay applies to underflow, overflow and open circuit errors. This delay can be used to hide temporary measurement value deviations, for example.

Data type	Values
UINT	0…65535

4.31.11.9.6.7 SumErrorDelay

Names (pChannelName):
Cfo_SumErrorDelay01
Cfo_SumErrorDelay[02…06]

A "SumErrorDelay" register can be used to set the time that an error must remain pending before the composite error bit is set.

Data type	Values
UINT	0…65535

4.31.11.9.7 Temperature measurement

The received temperature data is prepared in two different formats and given a time stamp. For each channel there are two separate registers for transmitting the measurement values to the PLC. The user is free to select the format that best fits the application at hand.

4.31.11.9.7.1 TemperatureEvaluated, Measurand

Designations (pChannelName):
TemperatureEvaluated01
TemperatureEvaluated[02…06]

TemperatureEvaluated01_CANIO
TemperatureEvaluated[02…06]_CANIO

Measurand01
Measurand[02...06]

Analog input value with respect to sensor type:

Input signal	Digital value
Type J (Fe-CuNi)	-2100 to 12000 (for -210.0 to 1200.0°C)
Type K (NiCr-Ni)	-2700 to 13720 (for -270.0 to 1372.0°C)
Type N (NiCrSi-NiSi)	-2700 to 12980 (for -270.0 to 1298.0°C)
Type S (PtRh10-Pt)	-500 to 17680 (for -50.0 to 1768.0°C)
Type R (PtRh13-Pt)	-500 to 17600 (for -50.0 to 1760.0°C)
Type C (WRe5-WRe26)	0 to 23100 (for 0 to 2310.0°C)
Type T (Cu-CuNi)	-2700 to 4000 (for -270.0 to 400.0°C)
Type B (PtRh30-PtRh6)	0 to 18200 (for 0 to 1820.0°C)
Type E (NiCr-CuNi)	-2700 to 9970 (for -270.0 to 997.0°C)
Voltage without linearization and terminal temperature compensation Resolution 1.0625 µV for a measurement range of ±35 mV	-32768 to 32767
Voltage without linearization and terminal temperature compensation Resolution 2.125 µV for a measurement range of ±70 mV	-32768 to 32767

In order for the user to always be supplied with a defined output value, the following must be taken into consideration:

- Up to the first conversion, 0x8000 is output.
- After switching the sensor type, 0x8000 is output until the first conversion.
- If the input is switched off, 0x8000 is output.
- If an I/O voltage supply failure occurs, 0x8000 is output

4.31.11.9.7.2 SampleTime

Names (pChannelName):
SampleTime01_16bit
SampleTime[02…06]_16bit

SampleTime01_32bit
SampleTime[02…06]_32bit

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

Data type	Values [µs]	Information
INT	-32,768 to 32767	Nettime timestamp of the current input value
DINT	-2,147,483,648 to 2,147,483,647	Nettime timestamp of the current input value

4.31.11.9.7.3 IOCycleCounter

Designations (pChannelName):
IOCycleCounter01_8bit
IOCycleCounter[02…06]_8bit

IOCycleCounter01_16bit
IOCycleCounter[02…06]_16bit

The "IOCycleCounter" is a cyclic counter that is incremented each time a value is converted. It can be used as either a 1-byte or 2-byte counter.

Data type	Values
USINT	0...255
UINT	0…65535

4.31.11.9.7.4 Error management

The module can diagnose various error states. Detected errors can be read out via the status registers and the individual error bits. If an error only occurs briefly, the error status is reset automatically. The error management method must be tailored to the particular function model being used.

Status messages in function model 0

When using function model 0 (e.g. operation with X20 CPU) six different error sources can be analyzed. The "Delay" registers allow the user to control how errors are triggered on each channel. Error messages can be called either in packages or bit-wise.

Status

Names (pChannelName):
Status01
Status[02…06]

The current error status of the module channels is displayed in this register, regardless of the configured replacement value strategy. Some error information may be delayed according to the previously configured condition.

Data type	Values
USINT	See bit structure

Bit structure:

Bit	Name		Information
0	Underrun01 Underrun[02...06]	0	No error
		1	Value below the permitted range
1	Overrun01 Overrun[02...06]	0	No error
		1	Value above the permitted range
2	OpenLine01 OpenLine[02...06]	0	No error
		1	Open line
3	CompensationFault01 CompensationFault[02...06]	0	No error
		1	Compensation error
4	ConverterFault01 ConverterFault[02...06]	0	No error
		1	Conversion error
5	SumFault01 SumFault[02...06]	0	No error
		1	Immediate composite error
6	ParameterFault01 ParameterFault[02...06]	0	No error
		1	Setting for "ClampType" register not permitted
7	Reserved	-	

Status messages in function model 254 (CANIO)

In function model 254 there is no configuration required in advance to activate error detection. It is always activated during startup. To streamline the transfer, however, only the four basic diagnostics were implemented.

ModuleStatus (CANIO)

Designations (pChannelName):
ModuleStatus01To04
ModuleStatus05To06

The bits of the "ModuleStatus" registers are set when one of the implemented error diagnostics is triggered.

Data type	Values
USINT	See bit structures I and II

Bit structure I:

Bit	Product ID		Note
0…1	Channel 1	0 - 3	See error description
2…3	Channel 2	0 - 3	See error description
4…5	Channel 3	0 - 3	See error description
6…7	Channel 4	0 - 3	See error description

Bit strucrture II:

Bit	Product ID		Note
0…1	Channel 5	0 - 3	See error description
2…3	Channel 6	0 - 3	See error description
4…7	Reserved	-	

Error description:
0…00 - No error
1…01 - Underflow (lower value limit violated)
2…10 - Overflow (upper value limit violated)
3…11 - Open line

4.31.11.9.8 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

4.31.11.9.9 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time
1 ms

4.32 Terminal blocks

Various terminal blocks are available for wiring X20 modules.

4.32.1 Brief information

Product ID	Short description	on page
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	3057
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	3057
X20TB1E	X20 terminal block, 12-pin, 24 VDC keyed, 2x PT1000 integrated for terminal temperature compensation	3059
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	3061
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	3063

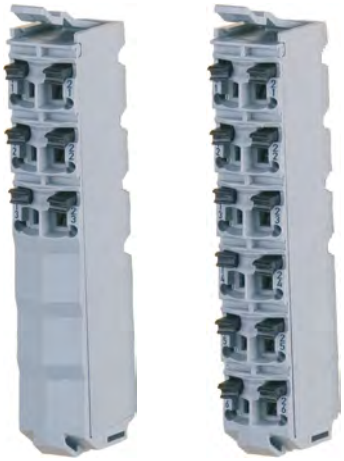
4.32.2 X20TB06/X20TB12

4.32.2.1 General information

The X20 24 VDC modules are wired using the X20TB06 and X20TB12 terminal blocks.

- Tool-free wiring with push-in technology
- Simple wire release using lever
- Ability to label each terminal
- Plain text labeling also possible
- Test access for standard probes
- Can be customer-coded

4.32.2.2 Order data



X20TB06 X20TB12

Model number	Short description
	Terminal blocks
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed

Table 748: X20TB06, X20TB12 - Order data

4.32.2.3 Technical data

Product ID	X20TB06	X20TB12
General information		
Certification		
CE	Yes	
cULus	Yes	
ATEX Zone 2 [1]	Yes	
GL	Yes	
LR	Yes	
GOST-R	Yes	
Terminal block		
Number of pins	6	12
Type of terminal clamp	Push-in terminal	
Push-in force per contact	Typ. 10 N	
Cable type	Only copper wires (no aluminum wires!)	
Wire stripping length	7 to 9 mm	
Connection cross section		
Solid wires	0.08 to 2.50 mm² / 28 to 14 AWG	
Fine strand wires	0.25 to 2.50 mm² / 24 to 14 AWG	
With wire end sleeves	0.25 to 1.50 mm² / 24 to 16 AWG	
With double wire end sleeves	Up to 2x 0.75 mm²	
Distance between contacts		
Left - Right	4.2 mm	
Above - Below	10.96 mm	
Electrical characteristics		
Nominal voltage	240 VAC	
Max. voltage	300 VAC	
Nominal current [2]	10 A / contact	
Contact resistance	≤5 mΩ	
Environmental conditions [3]		
Temperature		
Operation	Corresponds to the X20 module used	
Relative humidity		
Operation	Corresponds to the X20 module used	

Table 749: X20TB06, X20TB12 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Take the respective limit data for the I/O modules into consideration!
3) Identical for operation, storage and transport.

Warning!

It is possible to come into contact with parts that carry voltage when the clamping block is disconnected. For this reason, working on a disconnected clamping block is not permitted at voltages of 50 V or higher.

4.32.2.4 Contact holding force

To ensure that cables maintain a secure contact with the terminal block, they must not be under too much stress. If the holding force is exceeded, the cable will come loose from the terminal block and cause a malfunction.

	Fine strand wires			Solid wires				With wire end sleeves	
Cables in mm²	0.25	1.5	2.5	0.08	0.25	1.5	2.5	0.25	1.5
Standard spec. (min. value in Newton)	12.5	40	50	4	12.5	40	50	12.5	40

Information:

Fine strand wires must be twisted to provide sufficient holding force.

4.32.3 X20TB1E

4.32.3.1 General information

The X20TB1E terminal block is equipped with two integrated PT1000 sensors. It is therefore optimally suited for internal terminal temperature compensation. The terminal block can be used on all thermocouple modules with 12 connections.

- Integrated terminal temperature compensation
- Tool-free wiring with push-in technology
- Simple wire release using a screwdriver
- Ability to label each terminal
- Plain text labeling also possible
- Test access for standard probes
- Can be customer-coded

4.32.3.2 Order data

Model number	Short description	Figure
	Terminal blocks	
X20TB1E	X20 terminal block, 12-pin, 24 VDC keyed, 2x PT1000 integrated for terminal temperature compensation	

Table 750: X20TB1E - Order data

4.32.3.3 Technical data

Product ID	X20TB1E
General information	
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Terminal block	
Number of pins	12
Type of terminal clamp	Push-in terminal
Push-in force per contact	Typ. 10 N
Cable type	Only copper wires (no aluminum wires!)
Wire stripping length	7 to 9 mm
Connection cross section	
Solid wires	0.08 to 1.50 mm² / 28 to 16 AWG
Fine strand wires	0.25 to 1.50 mm² / 24 to 16 AWG
With wire end sleeves	0.25 to 0.75 mm² / 24 to 20 AWG
Distance between contacts	
Left - Right	4.2 mm
Above - Below	8.25 mm
Terminal temperature compensation	2x PT1000 integrated in the terminal
Electrical characteristics	
Nominal voltage	24 VDC
Max. voltage	50 VDC
Nominal current [2]	2 A / contact
Contact resistance	≤5 mΩ
Environmental conditions [3]	
Temperature	
Operation	Corresponds to the X20 module used
Relative humidity	
Operation	Corresponds to the X20 module used

Table 751: X20TB1E - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Take the respective limit data for the I/O modules into consideration!
3) Identical for operation, storage and transport.

Warning!

It is possible to come into contact with parts that carry voltage when the clamping block is disconnected. For this reason, working on a disconnected clamping block is not permitted at voltages of 50 V or higher.

4.32.3.4 Contact holding force

To ensure that cables maintain a secure contact with the terminal block, they must not be under too much stress. If the holding force is exceeded, the cable will come loose from the terminal block and cause a malfunction.

	Fine strand wires			Solid wires				With wire end sleeves	
Cables in mm²	0.25	1.5	2.5	0.08	0.25	1.5	2.5	0.25	1.5
Standard spec. (min. value in Newton)	12.5	40	50	4	12.5	40	50	12.5	40

Information:

Fine strand wires must be twisted to provide sufficient holding force.

4.32.4 X20TB1F

4.32.4.1 General information

X20 24 VDC modules with 16 connections are wired using the X20TB1F terminal block.

- Tool-free wiring with push-in technology
- Simple wire release using a screwdriver
- Ability to label each terminal
- Plain text labeling also possible
- Test access for standard probes
- Can be customer-coded

4.32.4.2 Order data

Model number	Short description	Figure
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 752: X20TB1F - Order data

Information:

To avoid damaging the terminals, the B&R X20AC0SD1 screw driver should be used.

4.32.4.3 Technical data

Product ID	X20TB1F
General information	
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Terminal block	
Number of pins	16
Type of terminal clamp	Push-in terminal
Push-in force per contact	Typ. 10 N
Cable type	Only copper wires (no aluminum wires!)
Wire stripping length	7 to 9 mm
Connection cross section	
Solid wires	0.08 to 1.50 mm² / 28 to 16 AWG
Fine strand wires	0.25 to 1.50 mm² / 24 to 16 AWG
With wire end sleeves	0.25 to 0.75 mm² / 24 to 20 AWG
Distance between contacts	
Left - Right	4.2 mm
Above - Below	8.25 mm
Electrical characteristics	
Nominal voltage	24 VDC
Max. voltage	50 VDC
Nominal current [2]	2 A / contact
Contact resistance	≤5 mΩ
Environmental conditions [3]	
Temperature	
Operation	Corresponds to the X20 module used
Relative humidity	
Operation	Corresponds to the X20 module used

Table 753: X20TB1F - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Take the respective limit data for the I/O modules into consideration!
3) Identical for operation, storage and transport.

Warning!

It is possible to come into contact with parts that carry voltage when the clamping block is disconnected. For this reason, working on a disconnected clamping block is not permitted at voltages of 50 V or higher.

4.32.4.4 Contact holding force

To ensure that cables maintain a secure contact with the terminal block, they must not be under too much stress. If the holding force is exceeded, the cable will come loose from the terminal block and cause a malfunction.

	Fine strand wires			Solid wires				With wire end sleeves	
Cables in mm²	0.25	1.5	2.5	0.08	0.25	1.5	2.5	0.25	1.5
Standard spec. (min. value in Newton)	12.5	40	50	4	12.5	40	50	12.5	40

Information:

Fine strand wires must be twisted to provide sufficient holding force.

4.32.5 X20TB32

4.32.5.1 General information

The X20 240 VAC modules are wired using X20TB32 terminal blocks.

- Tool-free wiring with push-in technology
- Simple wire release using lever
- Ability to label each terminal
- Plain text labeling also possible
- Test access for standard probes
- Can be customer-coded
- Special color
- 240 V coding

4.32.5.2 Order data

Model number	Short description	Figure
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 754: X20TB32 - Order data

4.32.5.3 Technical data

Product ID	X20TB32
General information	
Certification	
CE	Yes
cULus	Yes
ATEX Zone 2 [1]	Yes
GL	Yes
LR	Yes
GOST-R	Yes
Terminal block	
Number of pins	12
Type of terminal clamp	Push-in terminal
Push-in force per contact	Typ. 10 N
Cable type	Only copper wires (no aluminum wires!)
Wire stripping length	7 to 9 mm
Connection cross section	
Solid wires	0.08 to 2.50 mm² / 28 to 14 AWG
Fine strand wires	0.25 to 2.50 mm² / 24 to 14 AWG
With wire end sleeves	0.25 to 1.50 mm² / 24 to 16 AWG
With double wire end sleeves	Up to 2x 0.75 mm²
Distance between contacts	
Left - Right	4.2 mm
Above - Below	10.96 mm
Electrical characteristics	
Nominal voltage	240 VAC
Max. voltage	300 VAC
Nominal current [2]	10 A / contact
Contact resistance	≤5 mΩ
Environmental conditions [3]	
Temperature	
Operation	Corresponds to the X20 module used
Relative humidity	
Operation	Corresponds to the X20 module used

Table 755: X20TB32 - Technical data

1) Ta min.: 0°C
   Ta max.: See environmental conditions
2) Take the respective limit data for the I/O modules into consideration!
3) Identical for operation, storage and transport.

Warning!

It is possible to come into contact with parts that carry voltage when the clamping block is disconnected. For this reason, working on a disconnected clamping block is not permitted at voltages of 50 V or higher.

4.32.5.4 Contact holding force

To ensure that cables maintain a secure contact with the terminal block, they must not be under too much stress. If the holding force is exceeded, the cable will come loose from the terminal block and cause a malfunction.

	Fine strand wires			Solid wires				With wire end sleeves	
Cables in mm²	0.25	1.5	2.5	0.08	0.25	1.5	2.5	0.25	1.5
Standard spec. (min. value in Newton)	12.5	40	50	4	12.5	40	50	12.5	40

Information:

Fine strand wires must be twisted to provide sufficient holding force.

4.33 General data points

In addition to the registers listed in the register description, X20 modules also have other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

4.33.1 FirmwareVersion

Name:
FirmwareVersion

The firmware version of the module can be read using this data point.

The last two positions correspond to the number after the decimal point.

Example: 345 corresponds to 3.45.

Data type	Value	Information
UINT	1 to 99	Release version of older modules or developmental versions of new modules
	100 to 29999	Release version
	30000 to 59999	Test version

4.33.2 HardwareVariant

Name:
HardwareVariant

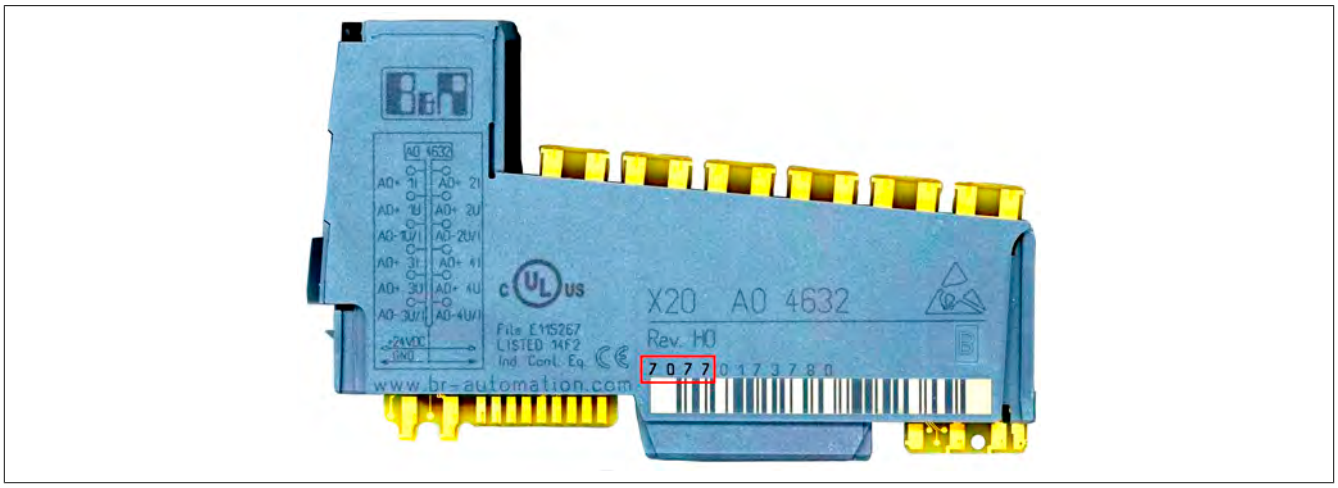
The hardware variant of the module can be read using this data point.

Data type	Value
UINT	0 to 65535

4.33.3 ModuleID

Name:
ModuleID

The module ID of the module can be read using this data point. The module hardware ID can be found in the respective module documentation. In addition, a serial number is printed on each electronics module; the module hardware ID corresponds to the first four positions of the serial number. (See figure: Hardware ID is additionally colored black.)



Data type	Value
UINT	0 to 65535

Information:

IDs beginning from 9999 are printed as hexadecimal numbers and must be converted to their decimal values for comparison!

4.33.4 SerialNumber

Name:
SerialNumber

The module's unique serial number can be read using this data point.

The complete serial number is made up of ModuleID and SerialNumber as follows: Serial number = (Hardware ID * 1E+7) + SerialNumber

The serial number is printed in decimal form on the module's housing.

Example

Hardware ID = (decimal) 1213

Serial number = (decimal) 67671339

Serial number = 1213 * 10000000 + 671339 = 12130671339

Data type	Value
UDINT	0 to 4,294,967,295

4.33.5 ModuleOK

Name:
ModuleOK

Whether the module is physically present in the slot or not can be read from this register.

Data type	Value	Information
BOOL	0	Module not ready for operation
	1	Module connected and configured

4.33.6 StaleData

Name:
StaleData

Whether the transferred data originates from the current cycle or a previous cycle can be read using this data point.

This error can result from cycle times that are too short or disturbances in module communication, for example.

Information:

This data point is only valid if ModuleOK = 1.

Data type	Value	Information
BOOL	0	Data originates from the current cycle
	1	Data does not originate from the current cycle

5 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, Exposure 21 days

Differences between coated and uncoated modules

- Suitable for operation in adverse atmospheric environments
- Suitable for operation in 100% humidity, condensing
- Coated modules have a different Module ID than the corresponding uncoated variants

5.1 Module overview: Alphabetically

Order data	Short description
X20cAI2438	X20 analog input module, coated, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply, supports the HART protocol
X20cAI4622	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter
X20cAI4632	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20cAI4632-1	X20 analog input module, coated, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20cAO2437	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated
X20cAO2438	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated, supports HART protocol
X20cAO4622	X20 analog output module, coated, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution
X20cAO4632	X20 analog output module, coated, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution
X20cAO4632-1	X20 analog output module, coated, 4 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution
X20cAP3121	X20 energy metering module, coated, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed
X20cAT4222	X20 temperature input module, coated, 4 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections
X20cAT6402	X20 temperature input module, coated, 6 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20cBC0083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, 2x RJ45, order bus base, power supply module and terminal block separately
X20cBC0087	X20 bus controller, coated, Modbus/TCP or Modbus/UDP interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately
X20cBC0088	X20 bus controller, coated, 1 EtherNet/IP interface, integrated switch, web interface, 2x RJ45, order bus base, power supply module and terminal block separately
X20cBC00E3	X20 bus controller, coated, 1 PROFINET RT interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately
X20cBC1083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, supports X20 interface module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20cBC8083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, supports X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20cBC8084	X20 bus controller, coated, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous
X20cBM12	X20 bus module, coated, 240 VAC keyed, internal I/O supply continuous
X20cBM31	X20 bus module, coated, for double-width modules, 24 VDC keyed, internal I/O supply continuous
X20cBM32	X20 bus module, coated, for double-width modules, 240 VAC keyed, internal I/O supply continuous
X20cBR9300	X20 bus receiver, coated, X2X Link, supply for X2X Link and internal I/O supply, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included
X20cBT9100	X20 bus transmitter, coated, X2X Link, supply for internal I/O supply

Coated modules

Order data	Short description
X20cCP1584	X20 CPU, coated, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCP1586	X20 CPU, coated, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCP3584	X20 CPU, coated, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCP3586	X20 CPU, coated, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCS1020	X20 interface module, coated, 1 RS232 interface, max. 115.2 kbit/s
X20cCS1030	X20 interface module, coated, 1 RS422/485 interface, max. 115.2 Mbit/s
X20cDC1198	X20 digital counter module, coated, 1 SSI absolute encoders, 5 V, 1 Mbit/s, 32-bit
X20cDC1396	X20 digital counter module, coated, 1 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation
X20cDC2395	X20 digital counter module, coated, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function
X20cDI4371	X20 digital input module, coated, 4 inputs, 24 VDC, sink, configurable input filter, 3-wire connections
X20cDI4375	X20 digital input module, coated, 4 inputs, 24 VDC, sink, configurable input filter, open line and short circuit detection, 3-wire connections
X20cDI4760	X20 digital input module, coated, 4 NAMUR inputs, 8.05 V
X20cDI6371	X20 digital input module, coated, 6 inputs, 24 VDC, sink, configurable input filter, 2-wire connections
X20cDI6372	X20 digital input module, coated, 6 inputs, 24 VDC, source, configurable input filter, 2-wire connections
X20cDI9371	X20 digital input module, coated, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections
X20cDI9372	X20 digital input module, coated, 12 inputs, 24 VDC, source, configurable input filter, 1-wire connections
X20cDM9324	X20 digital mixed module, coated, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20cDO2633	X20 digital output module, coated, 2 triac outputs, 12 to 240 VAC, 2 A, L switching, phase angle control, 240 V keyed
X20cDO4322	X20 digital output module, coated, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections
X20cDO4332	X20 digital output module, coated, 4 outputs, 24 VDC, 2 A, source, 3-wire connections
X20cDO4633	X20 digital output module, coated, 4 triac outputs, 12 to 240 VAC, 1 A, L switching, phase angle control, 240 V keyed
X20cDO4649	X20 digital output module, coated, 4 relays, N.O. contacts, 240 VAC / 5 A
X20cDO6321	X20 digital output module, coated, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections
X20cDO6322	X20 digital output module, coated, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections
X20cDO6639	X20 digital output module, coated, 6 relays, normally open contacts, 240 VAC / 2 A, 30 VDC / 2 A
X20cDO8331	X20 digital output module, coated, 8 outputs, 24 VDC, 2 A, sink, supply directly on module, 1-wire connections
X20cDO8332	X20 digital output module, coated, 8 outputs, 24 VDC, 2 A, source, supply directly on module, 1-wire connections
X20cDO9321	X20 digital output module, coated, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections
X20cDO9322	X20 digital output module, coated, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20cDS1119	X20 multifunctional digital signal processor, coated, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module
X20cHB1881	X20 hub expansion module, coated, integrated 1-port hub, for fiber optic cable
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45
X20cHB2881	X20 hub expansion module, coated, integrated 2-port hub, for fiber optic cable
X20cHB2885	X20 hub expansion module, coated, integrated active 2-port hub, 2x RJ45
X20cHB2886	X20 hub expansion module, coated, integrated active 2-port hub, 2 fiber optic interfaces
X20cHB8815	X20 POWERLINK - TCP/IP gateway, coated, can be expanded with active hub modules, 2x RJ45
X20cHB8880	X20 base hub module, coated, integrated 2-port hub, 2x RJ45
X20cHB8884	X20 compact link selector, coated, 2x RJ45, order bus base, power supply module and terminal block separately.
X20cIF1030	X20 interface module, coated, 1 RS422/485 interface, max. 115.2 kbit/s, electrically isolated
X20cIF1041-1	X20 interface module, coated, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately
X20cIF1061-1	X20 interface module coated, for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated
X20cIF1063-1	X20 interface module, coated, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated
X20cIF1072	X20 interface module, coated, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately
X20cIF1082-2	X20 interface module, coated, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function PRC function
X20cIF10D3-1	X20 interface module, coated, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated
X20cIF10E3-1	X20 interface module, coated, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated
X20cIF10X0	X20 interface module, coated, 1 redundancy link interface 1000 Base-FX, CPU-CPU data synchronization for controller redundancy
X20cIF2181-2	X20 interface module, coated, 1x link selector for POWERLINK cable redundancy, POWERLINK functions: - Managing node - Controlled node for iCN operation - Redundant managing node for controller redundancy - Ring redundancy - 2x hub - Multi ASend - PRC function 2x RJ45
X20cPD2113	X20 potential distributor, coated, 6x GND, 6x 24 VDC, with supply option, integrated microfuse
X20cPS2100	X20 power supply module, coated, for internal I/O supply
X20cPS2110	X20 power supply module, coated, for internal I/O supply, integrated microfuse
X20cPS3300	X20 power supply module, coated, for X2X Link and internal I/O supply
X20cPS3310	X20 power supply module, coated, for X2X Link and internal I/O supply integrated microfuse
X20cPS8002	X20 power supply module, coated, for standalone hub and compact link selector
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply

5.2 Module overview: Grouped

5.2.1 CPUs

Order data	Short description
X20cCP1584	X20 CPU, coated, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCP1586	X20 CPU, coated, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 1 insert slot for X20 interface modules, 2 USB ports, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot cover and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCP3584	X20 CPU, coated, ATOM 0.6 GHz, 256 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.
X20cCP3586	X20 CPU, coated, ATOM 1.6 GHz, 512 MB DDR2 RAM, 1 MB SRAM, removable application memory: CompactFlash, 3 insert slots for X20 interface modules, 2 USB interfaces, 1 RS232 interface, 1 Ethernet interface 10/100/1000 Base-T, 1 POWERLINK interface, incl. supply module, 1 X20TB12 terminal block, slot covers and X20 locking plate (right) X20AC0SR1 included, order application memory separately.

5.2.2 Other modules

Analog inputs

Order data	Short description
X20cAI2438	X20 analog input module, coated, 2 inputs, 4-20 mA, 16-bit converter resolution, single channel electrically isolated and with separate sensor supply, supports the HART protocol
X20cAI4622	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter
X20cAI4632	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20cAI4632-1	X20 analog input module, coated, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions
X20cAP3121	X20 energy metering module, coated, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates root mean square values, 240 V keyed

Analog outputs

Order data	Short description
X20cAO2437	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated
X20cAO2438	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated, supports HART protocol
X20cAO4622	X20 analog output module, coated, 4 outputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution
X20cAO4632	X20 analog output module, coated, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution
X20cAO4632-1	X20 analog output module, coated, 4 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution

Bus Controllers

Order data	Short description
X20cBC0083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, 2x RJ45, order bus base, power supply module and terminal block separately
X20cBC0087	X20 bus controller, coated, Modbus/TCP or Modbus/UDP interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately
X20cBC0088	X20 bus controller, coated, 1 EtherNet/IP interface, integrated switch, web interface, 2x RJ45, order bus base, power supply module and terminal block separately
X20cBC00E3	X20 bus controller, coated, 1 PROFINET RT interface, integrated 2-port switch, 2x RJ45, order bus base, power supply module and terminal block separately

Bus modules

Order data	Short description
X20cBM01	X20 power supply bus module, coated, 24 VDC keyed, internal I/O supply interrupted to the left
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O supply continuous
X20cBM12	X20 bus module, coated, 240 VAC keyed, internal I/O supply continuous
X20cBM31	X20 bus module, coated, for double-width modules, 24 VDC keyed, internal I/O supply continuous
X20cBM32	X20 bus module, coated, for double-width modules, 240 VAC keyed, internal I/O supply continuous

Bus receivers and transmitters

Order data	Short description
X20cBR9300	X20 bus receiver, coated, X2X Link, supply for X2X Link and internal I/O supply, X20 locking plates (left and right) X20AC0SL1/ X20AC0SR1 included
X20cBT9100	X20 bus transmitter, coated, X2X Link, supply for internal I/O supply

Counter functions

Order data	Short description
X20cDC1198	X20 digital counter module, coated, 1 SSI absolute encoders, 5 V, 1 Mbit/s, 32-bit
X20cDC1396	X20 digital counter module, coated, 1 ABR incremental encoders, 24 V, 100 kHz input frequency, 4x evaluation
X20cDC2395	X20 digital counter module, coated, 1 SSI absolute encoder, 24 V, 1 ABR incremental encoder, 24 V, 2 AB incremental encoders, 24 V, 4 event counters or 2 PWM, local time measurement function

Digital inputs

Order data	Short description
X20cDI4371	X20 digital input module, coated, 4 inputs, 24 VDC, sink, configurable input filter, 3-wire connections
X20cDI4375	X20 digital input module, coated, 4 inputs, 24 VDC, sink, configurable input filter, open line and short circuit detection, 3-wire connections
X20cDI4760	X20 digital input module, coated, 4 NAMUR inputs, 8.05 V
X20cDI6371	X20 digital input module, coated, 6 inputs, 24 VDC, sink, configurable input filter, 2-wire connections
X20cDI6372	X20 digital input module, coated, 6 inputs, 24 VDC, source, configurable input filter, 2-wire connections
X20cDI9371	X20 digital input module, coated, 12 inputs, 24 VDC, sink, configurable input filter, 1-wire connections
X20cDI9372	X20 digital input module, coated, 12 inputs, 24 VDC, source, configurable input filter, 1-wire connections
X20cDM9324	X20 digital mixed module, coated, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20cDS1119	X20 multifunctional digital signal processor, coated, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module

Digital inputs/outputs

Order data	Short description
X20cDM9324	X20 digital mixed module, coated, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source, 1-wire connections

Digital outputs

Order data	Short description
X20cDO4322	X20 digital output module, coated, 4 outputs, 24 VDC, 0.5 A, source, 3-wire connections
X20cDO4332	X20 digital output module, coated, 4 outputs, 24 VDC, 2 A, source, 3-wire connections
X20cDO4633	X20 digital output module, coated, 4 triac outputs, 12 to 240 VAC, 1 A, L switching, phase angle control, 240 V keyed
X20cDO4649	X20 digital output module, coated, 4 relays, N.O. contacts, 240 VAC / 5 A
X20cDO6321	X20 digital output module, coated, 6 outputs, 24 VDC, 0.5 A, sink, 2-wire connections
X20cDO6322	X20 digital output module, coated, 6 outputs, 24 VDC, 0.5 A, source, 2-wire connections
X20cDO6529	X20 digital output module, coated, 6 relays, normally open contacts, 115 VAC / 0.5 A, 30 VDC / 1 A
X20cDO6639	X20 digital output module, coated, 6 relays, normally open contacts, 240 VAC / 2 A, 30 VDC / 2 A
X20cDO8331	X20 digital output module, coated, 8 outputs, 24 VDC, 2 A, sink, supply directly on module, 1-wire connections
X20cDO8332	X20 digital output module, coated, 8 outputs, 24 VDC, 2 A, source, supply directly on module, 1-wire connections
X20cDO9321	X20 digital output module, coated, 12 outputs, 24 VDC, 0.5 A, sink, 1-wire connections
X20cDO9322	X20 digital output module, coated, 12 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20cDM9324	X20 digital mixed module, coated, 8 inputs, 24 VDC, sink, configurable input filter, 4 outputs, 24 VDC, 0.5 A, source, 1-wire connections
X20cDS1119	X20 multifunctional digital signal processor, coated, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module

Digital signal processing and preparation

Order data	Short description
X20cDS1119	X20 multifunctional digital signal processor, coated, 3 digital channels 5 V (symmetric) configurable as inputs or outputs, 2 digital input channels 24 V (asymmetric), max. 2 event counters, 1 universal counter pair configurable as A/B or up/down counter, linear movement generator (A/B, direction/frequency) with 1 reference pulse, 1 SSI absolute encoder, NetTime module

Electronics module communication

Order data	Short description
X20cCS1020	X20 interface module, coated, 1 RS232 interface, max. 115.2 kbit/s
X20cCS1030	X20 interface module, coated, 1 RS422/485 interface, max. 115.2 Mbit/s

Expandable bus controllers

Order data	Short description
X20cBC1083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, supports X20 interface module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20cBC8083	X20 bus controller, coated, 1 POWERLINK interface, integrated 2-port hub, supports X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately
X20cBC8084	X20 bus controller, coated, 1 POWERLINK interface, 1x link selector, for POWERLINK cable redundancy, supports active X20 hub module expansions, 2 RJ45, order bus base, power supply module and terminal block separately

Expandable bus controllers System modules

Order data	Short description
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20cHB1881	X20 hub expansion module, coated, integrated 1-port hub, for fiber optic cable
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45
X20cHB2881	X20 hub expansion module, coated, integrated 2-port hub, for fiber optic cable
X20cHB2886	X20 hub expansion module, coated, integrated active 2-port hub, 2 fiber optic interfaces
X20cIF1061-1	X20 interface module coated, for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated
X20cIF1063-1	X20 interface module, coated, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated
X20cIF10D3-1	X20 interface module, coated, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated
X20cIF10E3-1	X20 interface module, coated, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply

Interface module communication

Order data	Short description
X20cIF1030	X20 interface module, coated, 1 RS422/485 interface, max. 115.2 kbit/s, electrically isolated
X20cIF1041-1	X20 interface module, coated, for DTM configuration, 1 CANopen master interface, electrically isolated, order 1x TB2105 terminal block separately
X20cIF1061-1	X20 interface module coated, for DTM configuration, 1 PROFIBUS DP V0/V1 master interface, electrically isolated
X20cIF1063-1	X20 interface module, coated, for DTM configuration, 1 PROFIBUS DP V1 slave interface, electrically isolated
X20cIF1072	X20 interface module, coated, 1 CAN bus interface, max. 1 Mbit/s, electrically isolated, order 1x TB2105 terminal block separately
X20cIF1082-2	X20 interface module, coated, 1 POWERLINK interface, managing or controlled node, integrated 2-port hub, ring redundancy function PRC function
X20cIF10D3-1	X20 interface module, coated, for DTM configuration, 1 EtherNet/IP adapter (slave) interface, electrically isolated
X20cIF10E3-1	X20 interface module, coated, for DTM configuration, 1 PROFINET RT device (slave) interface, electrically isolated
X20cIF10X0	X20 interface module, coated, 1 redundancy link interface 1000 Base-FX, CPU-CPU data synchronization for controller redundancy
X20cIF2181-2	X20 interface module, coated, 1x link selector for POWERLINK cable redundancy, POWERLINK functions: - Managing node - Controlled node for iCN operation - Redundant managing node for controller redundancy - Ring redundancy - 2x hub - Multi ASend - PRC function 2x RJ45

Hub system

Order data	Short description
X20cHB8815	X20 POWERLINK - TCP/IP gateway, coated, can be expanded with active hub modules, 2x RJ45
X20cHB8880	X20 base hub module, coated, integrated 2-port hub, 2x RJ45

Other functions

Order data	Short description
X20cPD2113	X20 potential distributor, coated, 6x GND, 6x 24 VDC, with supply option, integrated microfuse

Power supply modules

Order data	Short description
X20cPS2100	X20 power supply module, coated, for internal I/O supply
X20cPS2110	X20 power supply module, coated, for internal I/O supply, integrated microfuse
X20cPS3300	X20 power supply module, coated, for X2X Link and internal I/O supply
X20cPS3310	X20 power supply module, coated, for X2X Link and internal I/O supply integrated microfuse

Redundancy system

Order data	Short description
X20cHB8884	X20 compact link selector, coated, 2x RJ45, order bus base, power supply module and terminal block separately.

System modules for the X20 hub system

Order data	Short description
X20cBB80	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, X20 end plates (left and right) X20AC0SL1/ X20AC0SR1 included
X20cBB81	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with one expansion slot for an X20 add-on module (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20cBB82	X20 bus base, coated, for X20 base module (BC, HB, etc.) and X20 power supply module, with two expansion slots for two X20 add-on modules (IF, HB, etc.), X20 locking plates (left and right) X20AC0SL1/X20AC0SR1 included
X20cHB1881	X20 hub expansion module, coated, integrated 1-port hub, for fiber optic cable
X20cHB2880	X20 hub expansion module, coated, integrated 2-port hub, 2x RJ45
X20cHB2881	X20 hub expansion module, coated, integrated 2-port hub, for fiber optic cable
X20cPS8002	X20 power supply module, coated, for standalone hub and compact link selector
X20cPS9400	X20 power supply module, coated, for bus controller and internal I/O supply, X2X Link supply

System modules for the X20 redundancy system

Order data	Short description
X20cHB2885	X20 hub expansion module, coated, integrated active 2-port hub, 2x RJ45
X20cHB2886	X20 hub expansion module, coated, integrated active 2-port hub, 2 fiber optic interfaces

Temperature measurement

Order data	Short description
X20cAT4222	X20 temperature input module, coated, 4 inputs for resistance measurement, PT100, PT1000, resolution 0.1°C, 3-wire connections
X20cAT6402	X20 temperature input module, coated, 6 thermocouple inputs, Type J, K, N, S, B, R, resolution 0.1°C

6 Accessories

6.1 Additional equipment for X20 modules

Accessories available for the X20 modules include a plain text tag, an accessory locking clip and a tag holder. Installation of these accessories is described in the section 7.7 "Installing accessories".

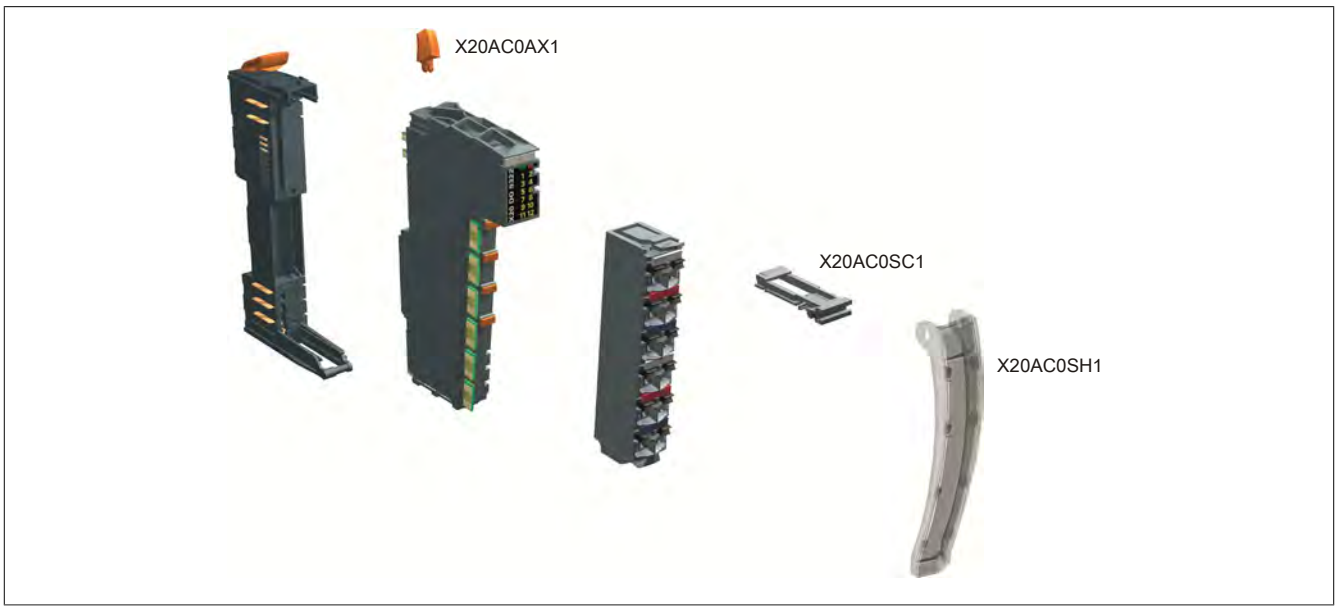


Figure 526: Additional equipment for X20 modules

6.1.1 Tag holders, terminal locking clips

Model number	Short description	Figure
	Tag holders, terminal locking clips	
X20AC0SC1	X20 terminal locking clip and tag holder for plain text tag	
X20AC0SC1.0100	X20 terminal locking clip and tag holder for plain text tag, 100 pcs. per package	

6.1.2 Plain text tags

Model number	Short description	Figure
	Plain text tags	
X20AC0SH1	X20 plain text tag	
X20AC0SH1.0100	X20 plain text tag, 100 pcs.	
	X20 slide-in labels	
X20AC0LB1.0100	X20 slide-in labels for X20 plain text tag, paper, white, perforated, 84 labels on A4 sheets, 100 sheets per package	

6.1.3 Accessory locking clips

Model number	Short description	Figure
	Accessory locking clips	
X20AC0AX1	X20 accessory locking clip	
X20AC0AX1.0100	X20 accessory locking clip, 100 pcs. per package	

6.2 Locking plates

The locking plate protects the modules on the outside against dirt and damage.

Model number	Short description	Figure
	Locking plates	
X20AC0SL1	X20 locking plate, left	
X20AC0SR1	X20 locking plate, right	
X20AC0SL1.0010	X20 locking plate, left, 10 pcs. per package	
X20AC0SR1.0010	X20 locking plate, right, 10 pcs. per package	

6.3 Cable shield clamp

For information on use, see section 3.6.2 "X20 cable shield clamp".

Model number	Short description	Figure
	Cable shield clamp	
X20AC0SG1.0010	X20 cable shield grounding clamp, 10 pcs. per package	
X20AC0SG1.0100	X20 cable shield grounding clamp, 100 pcs. per package	

6.4 Shielding bracket

The X20 shielding bracket provides an easy and space-saving way to ground the cable shielding (see section 3.6.3 "X20 shielding bracket").

Model number	Short description	Figure
	Undefined	
X20AC0SF7.0010	X20 shielding bracket 66mm	
X20AC0SF9.0010	X20 shielding bracket 88mm	

Table 756: X20AC0SF7.0010, X20AC0SF9.0010 - Order data

6.5 Terminal labeling

Each terminal connection is identified clearly directly on the terminal. It is also possible to attach tags to label the terminals individually.

The labeling tool is needed for attachment (see 7.8 "Label tags").

X20AC0M0x / X20AC0M1x

X20AC0M21

	Blank X20 tag labels (10.4 x 2.4 mm)
X20AC0M01	Blank X20 tag labels, white, set for 16 modules
X20AC0M02	Blank X20 tag labels, red, set for 16 modules
X20AC0M03	Blank X20 tag labels, blue, set for 16 modules
X20AC0M04	Blank X20 tag labels, orange, set for 16 modules
	Printed X20 tag labels (10.4 x 2.4 mm)
X20AC0M11	Printed X20 tag labels, white, set for 16 modules, label text: Module (modules 1 to 16), terminal (1 to 192)
X20AC0M12	Printed X20 tag labels, red, set for 16 modules, label text: +24 V
X20AC0M13	Printed X20 tag labels, blue, set for 16 modules, label text: GND
X20AC0M14	Printed X20 tag labels, orange, set for 16 modules, label text: Module (modules 1 to 16), terminal (1 to 192)
	Blank X20 tag labels, 10 pcs. per package (10.4 x 2.4 mm)
X20AC0M01.0010	Blank X20 tag labels, white, set for 16 modules, 10 pcs. per package
X20AC0M02.0010	Blank X20 tag labels, red, set for 16 modules, 10 pcs. per package
X20AC0M03.0010	Blank X20 tag labels, blue, set for 16 modules, 10 pcs. per package
X20AC0M04.0010	Blank X20 tag labels, orange, set for 16 modules, 10 pcs. per package
	Printed X20 tag labels, 10 pcs. per package (10.4 x 2.4 mm)
X20AC0M11.0010	Printed X20 tag labels, white, set for 16 modules, 10 pcs. per package, label text: Module (modules 1 to 16), terminal (1 to 192)
X20AC0M12.0010	Printed X20 tag labels, red, set for 16 modules, 10 pcs. per package, label text: +24 V
X20AC0M13.0010	Printed X20 tag labels, blue, set for 16 modules, 10 pcs. per package, label text: GND
X20AC0M14.0010	Printed X20 tag labels, orange, set for 16 modules, 10 pcs. per package, label text: Module (modules 1 to 16), terminal (1 to 192)
	Blank X20 tag labels, large (10.4 x 7.0 mm)
X20AC0M21	Blank X20 tag labels, large white, set for 48 modules
X20AC0M21.0010	Blank X20 tag labels, large white, set for 48 modules, 10 pcs. per package

6.6 Labeling tool

The labeling tool is needed to attach the tag labels.

Model number	Short description	Figure
	Labeling tool	
X20AC0MT1	X20 labeling tool for X20 tag labels	

6.7 Screwdriver

The screwdriver was developed specially for use with terminal blocks X20TB1E and X20TB1F to prevent damage to the terminals.

Model number	Short description	Figure
	Screwdriver	
X20AC0SD1	B&R screwdriver	

Table 757: X20AC0SD1 - Order data

6.8 POWERLINK cables

Pre-assembled POWERLINK cables with various lengths and connector combinations (RJ45 to RJ45, RJ45 to M12) ensure quick connectivity, thus saving time setting up the system.

6.8.1 RJ45 to RJ45

Not for use in cable drag chains

Model number	Short description	Figure
	POWERLINK cables	
X20CA0E61.00020	POWERLINK connection cable, RJ45 to RJ45, 0.2 m	
X20CA0E61.00025	POWERLINK connection cable, RJ45 to RJ45, 0.25 m	
X20CA0E61.00030	POWERLINK connection cable, RJ45 to RJ45, 0.3 m	
X20CA0E61.00035	POWERLINK connection cable, RJ45 to RJ45, 0.35 m	
X20CA0E61.00040	POWERLINK connection cable, RJ45 to RJ45, 0.4 m	
X20CA0E61.00050	POWERLINK connection cable, RJ45 to RJ45, 0.5 m	
X20CA0E61.00100	POWERLINK connection cable, RJ45 to RJ45, 1 m	
X20CA0E61.00150	POWERLINK connection cable, RJ45 to RJ45, 1.5 m	
X20CA0E61.00200	POWERLINK connection cable, RJ45 to RJ45, 2 m	
X20CA0E61.00500	POWERLINK connection cable, RJ45 to RJ45, 5 m	
X20CA0E61.01000	POWERLINK connection cable, RJ45 to RJ45, 10 m	
X20CA0E61.01500	POWERLINK connection cable, RJ45 to RJ45, 15 m	
X20CA0E61.02000	POWERLINK connection cable, RJ45 to RJ45, 20 m	

Table 758: X20CA0E61.00020, X20CA0E61.00025, X20CA0E61.00030, X20CA0E61.00035, X20CA0E61.00040, X20CA0E61.00050, X20CA0E61.00100, X20CA0E61.00150, X20CA0E61.00200, X20CA0E61.00500, X20CA0E61.01000, X20CA0E61.01500, X20CA0E61.02000 - Order data

Model number	Short description	Figure
	POWERLINK cable	
X20CA0E61.0300	POWERLINK connection cable, RJ45 to RJ45, 30.0 m	
X20CA0E61.0500	POWERLINK connection cable, RJ45 to RJ45, 50 m	
X20CA0E61.0600	POWERLINK connection cable, RJ45 to RJ45, 60.0 m	

Table 759: X20CA0E61.0300, X20CA0E61.0500, X20CA0E61.0600 - Order data

Can be used in cable drag chains

Model number	Short description	Figure
	POWERLINK cable	
X20CA3E61.0100	POWERLINK connection cable, RJ45 to RJ45, can be used in drag chains, 10 m	
X20CA3E61.0150	POWERLINK connection cable, RJ45 to RJ45, can be used in drag chains, 15 m	
X20CA3E61.0200	POWERLINK connection cable, RJ45 to RJ45, can be used in drag chains, 20.0 m	

Table 760: X20CA3E61.0100, X20CA3E61.0150, X20CA3E61.0200 - Order data

6.8.2 RJ45 to M12

Model number	Short description	Figure
	POWERLINK cable	
X67CA0E41.0010	POWERLINK attachment cable, RJ45 to M12, 1 m	
X67CA0E41.0050	POWERLINK attachment cable, RJ45 to M12, 5 m	
X67CA0E41.0150	POWERLINK attachment cable, RJ45 to M12, 15 m	
X67CA0E41.0500	POWERLINK attachment cable, RJ45 to M12, 50 m	

Table 761: X67CA0E41.0010, X67CA0E41.0050, X67CA0E41.0150, X67CA0E41.0500 - Order data

6.9 X2X Link cables

6.9.1 X2X Link connection cable

Pre-assembled

Model number	Short description	Figure
	X2X Link cables	
X20CA0X68.0003	X2X Link connection cable, 0.3 m	
X20CA0X68.0010	X2X Link connection cable, 1 m	
X20CA0X68.0020	X2X Link connection cable, 2 m	
X20CA0X68.0050	X2X Link connection cable, 5 m	
X20CA0X68.0100	X2X Link connection cable, 10 m	

Table 762: X20CA0X68.0003, X20CA0X68.0010, X20CA0X68.0020, X20CA0X68.0050, X20CA0X68.0100 - Order data

Open on one side

Model number	Short description	Figure
	X2X Link cables	
X20CA0X48.0010	X2X Link connection cable, open on one side, 1 m	
X20CA0X48.0020	X2X Link connection cable, open on one side, 2 m	
X20CA0X48.0050	X2X Link connection cable, open on one side, 5 m	
X20CA0X48.0100	X2X Link connection cable, open on one side, 10 m	
X20CA0X48.0200	X2X Link connection cable, open on one side, 20 m	

Table 763: X20CA0X48.0010, X20CA0X48.0020, X20CA0X48.0050, X20CA0X48.0100, X20CA0X48.0200 - Order data

6.9.2 Field-assembled

Model number	Short description	Figure
	X2X Link cable	
X67CA0X99.1000	Cable for custom assembly, 100 m	
X67CA0X99.5000	Cable for custom assembly, 500 m	

Table 764: X67CA0X99.1000, X67CA0X99.5000 - Order data

6.9.3 General specifications for X2X Link cables

When using a non-B&R cable for field wiring, it is important that the cable satisfies the following general specifications. For X2X Link segments up to 30 m, any cable that meets these specifications can be used. Cable lengths over this value must be inspected and approved by B&R.

	Data line	Supply line
Wires	2 x 0.25 mm² (AWG 24), stranded wire	2 x 0.34 mm² (AWG 22), stranded wire
Cable construction	Pair stranding, paired shield, aluminum foil	
Conductor resistance	Approx. 90 Ω/km	Approx. 55 Ω/km
Wave impedance	120 - 150 Ω	
Operating capacitance	<40 pF/m	
Cable shield	Tinned copper wire braiding, optical coverage ≥85%	

Table 765: General specifications for X2X Link cables

7 Mechanical handling

7.1 Solid mechanics

With all the advantages that the three-part modularity of the X20 system offers, one emphasis has always been solid mechanical design.

Its robust design, long guides and strengthened housing guarantee the stability it needs in industrial environments. These features allow the X20 system to be mounted on a top-hat rail with the same ease as a rack system. They also make it just as simple to remove it from the rail.

The following sections describe the mechanical design of the X20 system. The following topics are covered:

- Number of connection cycles
- Assembling an X20 system
- Top-hat rail installation
- Removal from the top-hat rail
- Expanding an X20 system
- Installing accessories
- Adding the terminal labels
- Application coding of terminal blocks

7.2 Number of connection cycles

The modules of the X20 system are divided into three parts. A module is made up of three basic elements:

- Bus module
- Electronic module
- Terminal block

The number of connection cycles between the respective basic elements is specified at 50.

Basic element	Number of connection cycles
Bus module ↔ Bus module	50
Bus module ↔ Electronic module	
Electronic module ↔ Terminal block	

Table 766: Number of connection cycles between the respective basic elements

7.3 Assembling an X20 system

There are several ways to assemble an X20 system. Two methods are described below:

Assembling an X20 system	Description
Variant 1	The X20 system is completely assembled and then installed on the top-hat rail.
Variant 2	The X20 system is installed and assembled directly on the top-hat rail.

Table 767: Two of the several methods for assembling an X20 system

Information:

- **Store X20 modules in the protective packaging until immediately before assembly.**
- **Only touch X20 modules on the housing.**
- **Take the necessary protective measures against electrostatic discharges (see also section 1.2.3 "Protection against electrostatic discharge").**

7.3.1 Variant 1

The X20 system is completely assembled and then installed on the top-hat rail.

1. Remove X20 modules from protective packaging. Check modules for obvious mechanical damages.
2. Insert electronic module in the guides on the bus module.

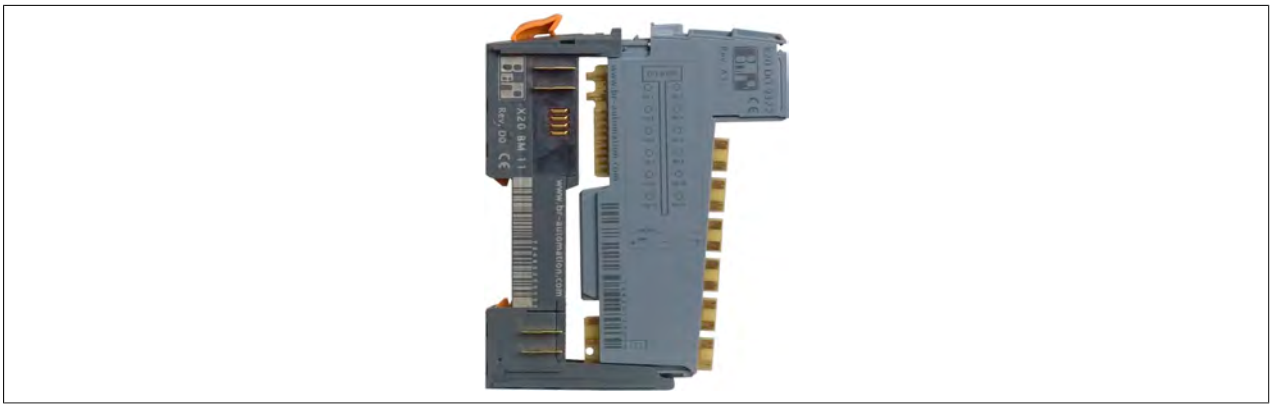


Figure 527: Insert electronic module in the guides on the bus module

3. Push the electronic module and the bus module flush together.

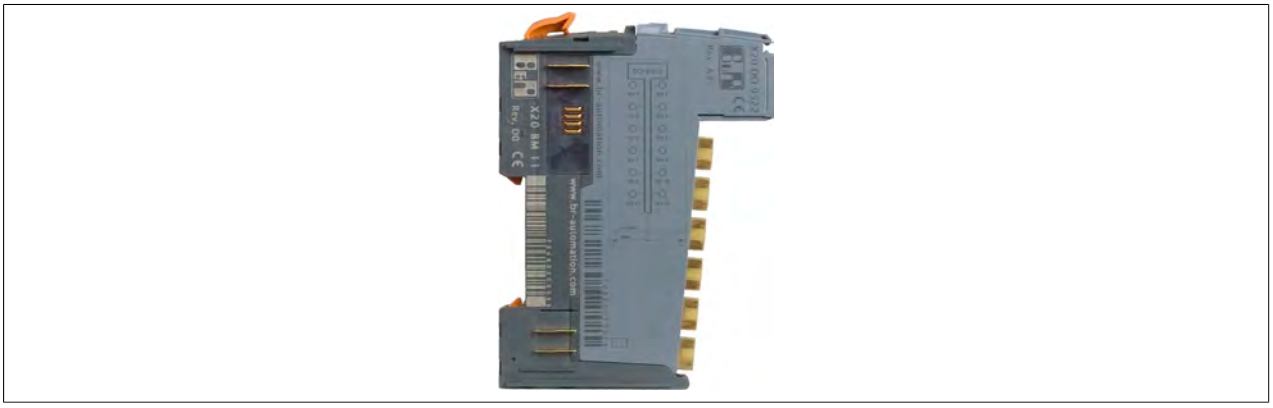


Figure 528: Push the electronic module and the bus module flush together

4. Hang the bottom edge of the terminal block in its place on the bus module.

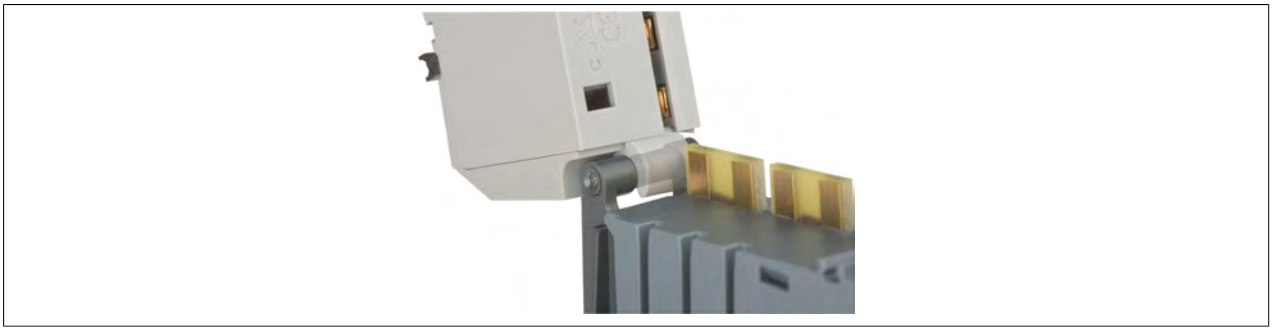


Figure 529: Hang the bottom edge of the terminal block in its place on the bus module

5. Rotate the terminal block up into place.

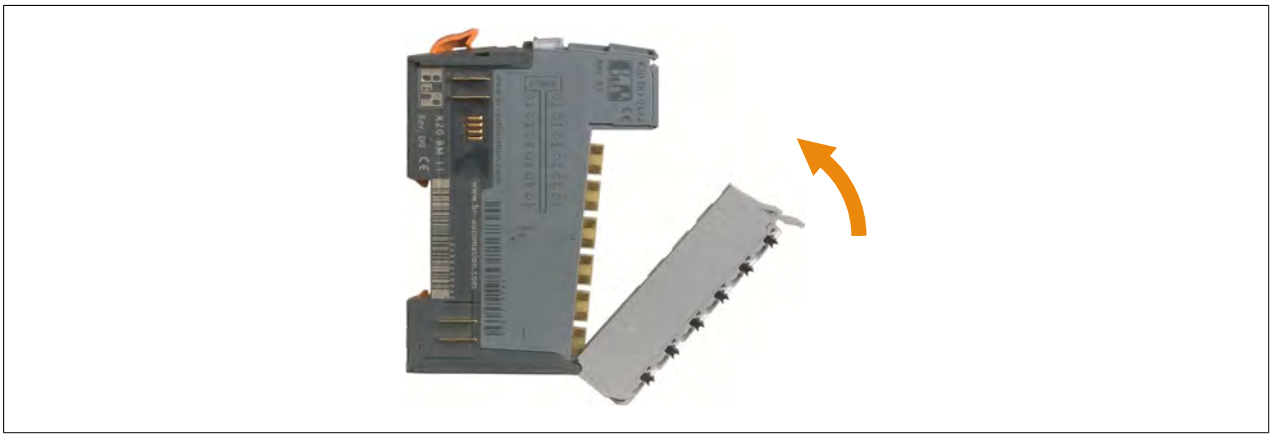


Figure 530: Rotate the terminal block up into place

6. The terminal block latch must close with an audible click. If the latch does not catch, the lever must be pushed up.

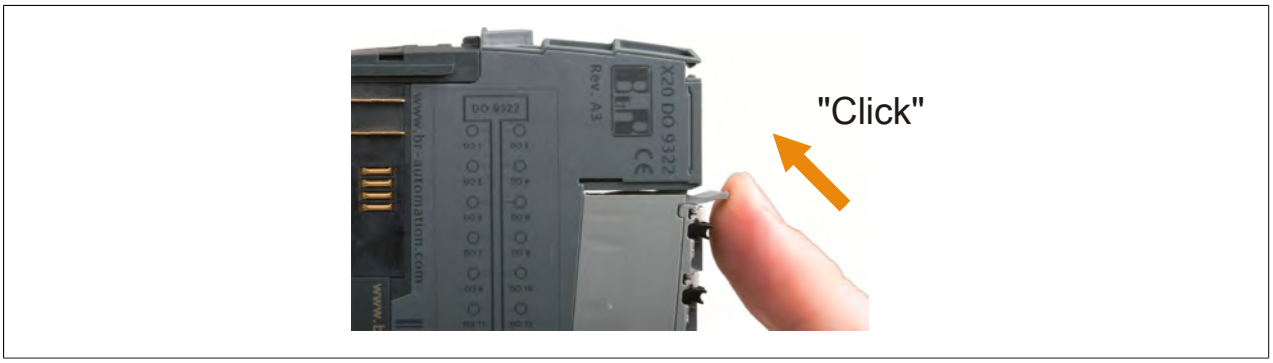


Figure 531: If the latch does not catch, the lever must be pushed up

7. Individual X20 modules should be assembled from left to right (viewed from front) to form the complete X20 system. To do this, connect the right module from behind to the guides for the left bus module.

Figure 532: Connect the right module from behind to the guides for the left bus module

8. Slide the right module forward until the two modules fit flush together.
9. Proceed like this until the second to last module.
10. For the last module, only insert the bus module in the guides of the left bus module.
11. Slide the right bus module forward until the two bus modules fit flush together.

12. Insert the right locking plate into the guides on the bus module from the front and push it all the way in.

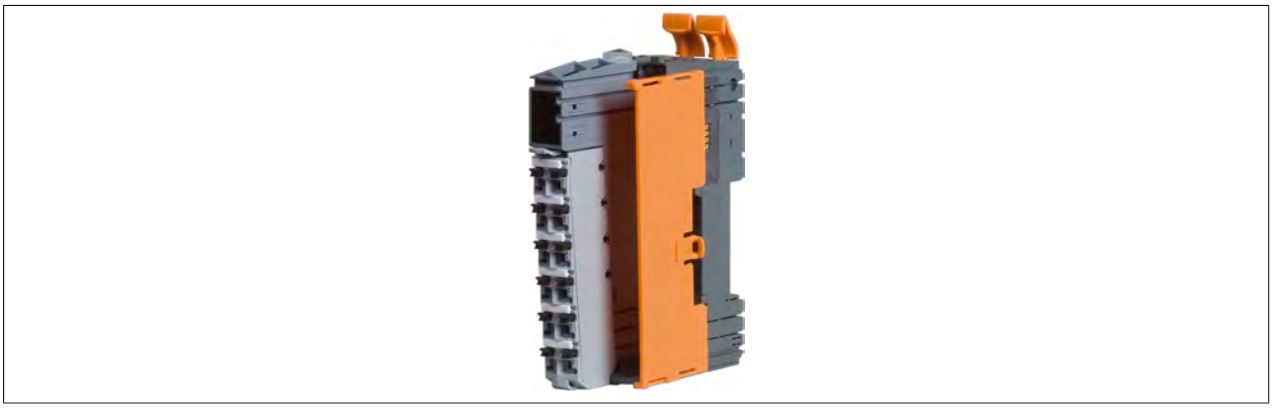


Figure 533: Insert the right locking plate into the guides on the bus module from the front

13. Insert the electronic module into the bus module and push firmly so that the two modules fit flush together.
14. Hang the bottom of the terminal block in its place on the bus module and push it up into place. The terminal block latch must close with an audible click.
15. Lay the left locking plate on the left module and insert it in the guides. Finally, slide the locking plate forward.

Figure 534: Lay the left locking plate on the left module and insert it in the guides

16. The procedure for hanging the X20 system on the top-hat rail is described in section 7.4 "Installing the X20 system on the top-hat rail".

7.3.2 Variant 2

The X20 system is installed and assembled directly on the top-hat rail.

1. Remove X20 modules from protective packaging. Check modules for obvious mechanical damages.
2. Push the locking lever all the way up on all of the bus modules. This opens the locking mechanism for top-hat rail installation.

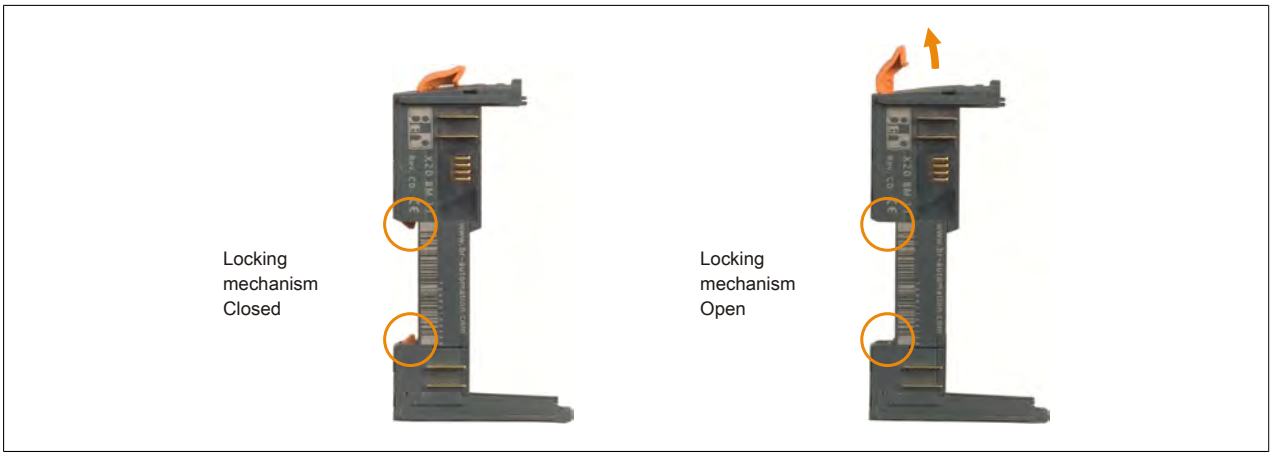


Figure 535: Push the locking lever all the way up to open the locking mechanism

3. Hang the first bus module in the desired position on the top-hat rail and close the locking mechanism by pushing the lever down.
4. Insert the next bus module in the guides of the previously mounted bus module.

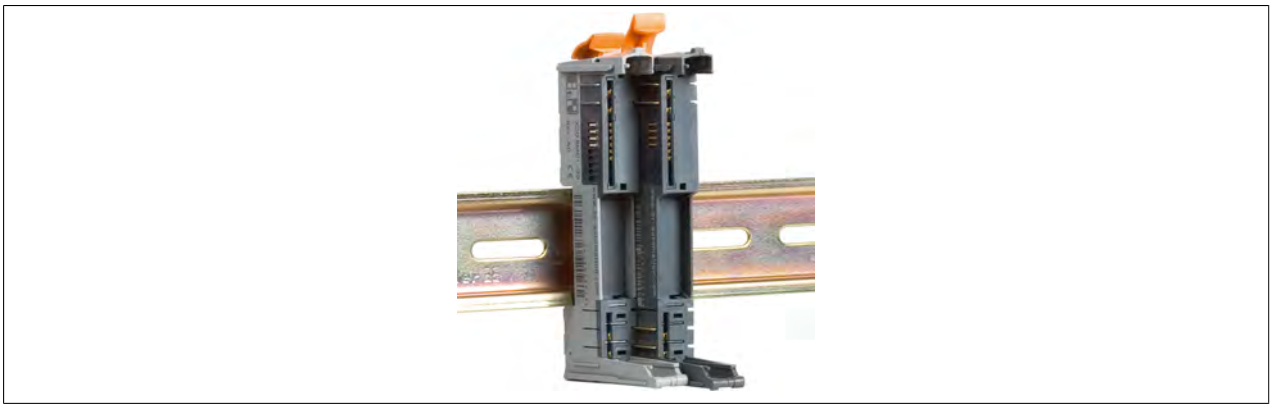


Figure 536: Insert the next bus module in the guides of the previously mounted bus module

5. Slide the bus module in against the top-hat rail and secure it by pushing down the locking lever.
6. Proceed like this with the rest of the bus modules.
7. Insert the corresponding electronic module in the guides on the leftmost bus module.

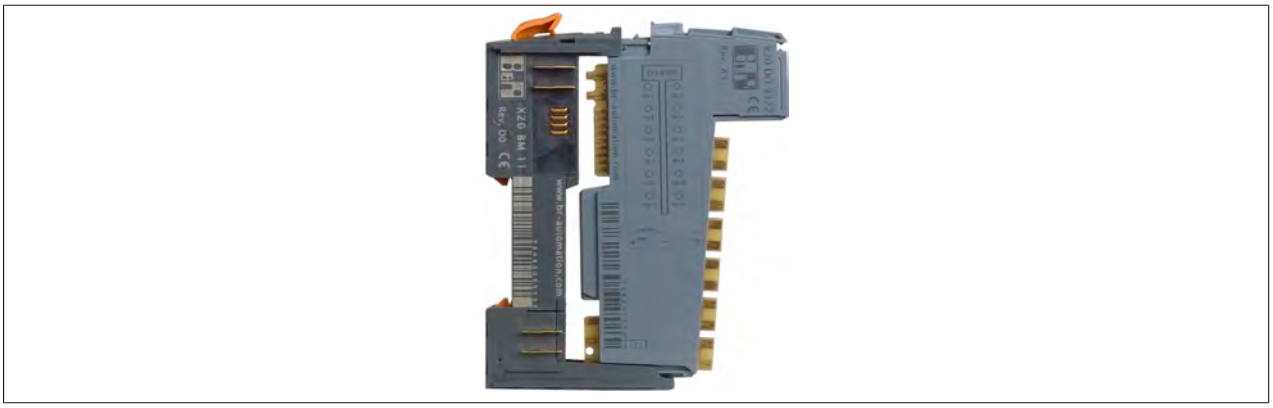


Figure 537: Insert electronic module in the guides on the bus module

8. Push the electronic module and the bus module flush together.

Figure 538: Push the electronic module and the bus module flush together

9. Proceed like this until the second to last electronic module.
10. Insert the right locking plate into the guides from the front and push it in all the way.

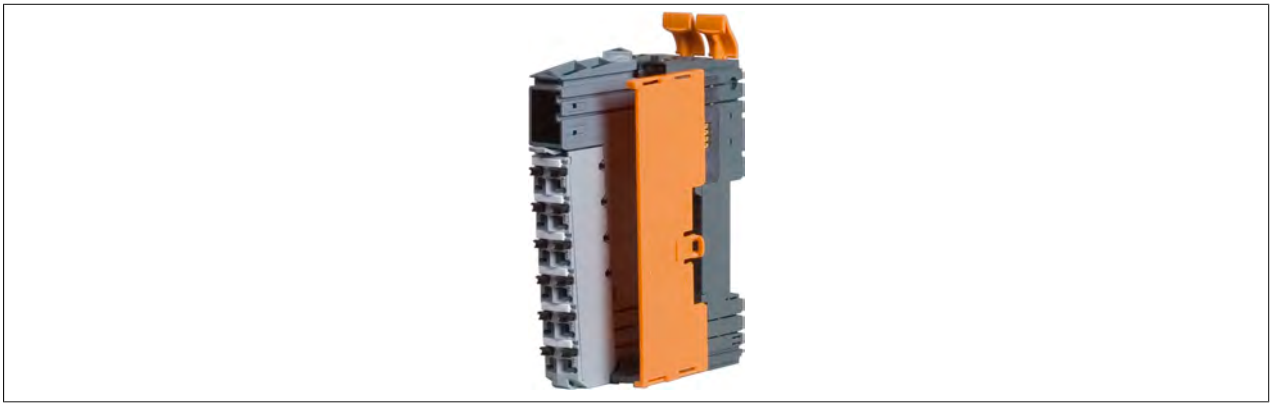


Figure 539: Insert the right locking plate into the guides on the bus module from the front

11. Insert the electronic module into the bus module and push firmly so that the two modules fit flush together.
12. Hang the terminal block in its place on the leftmost bus module.

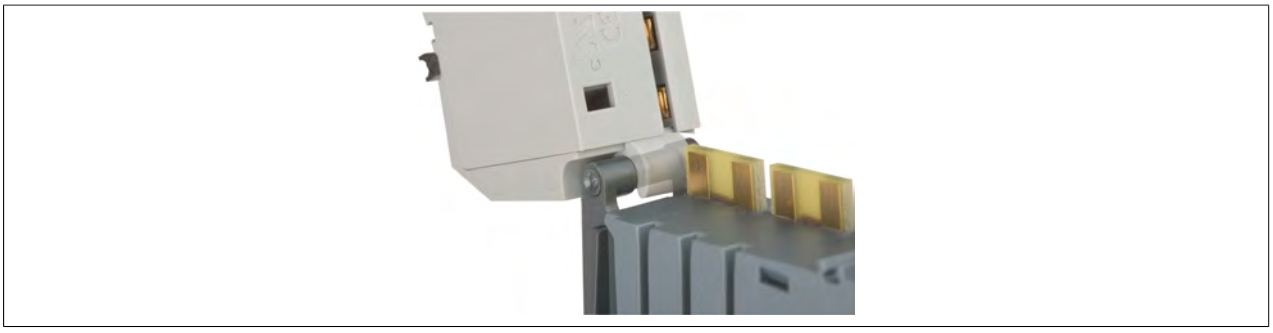


Figure 540: Hang the bottom edge of the terminal block in its place on the bus module

13. Rotate the terminal block up into place.

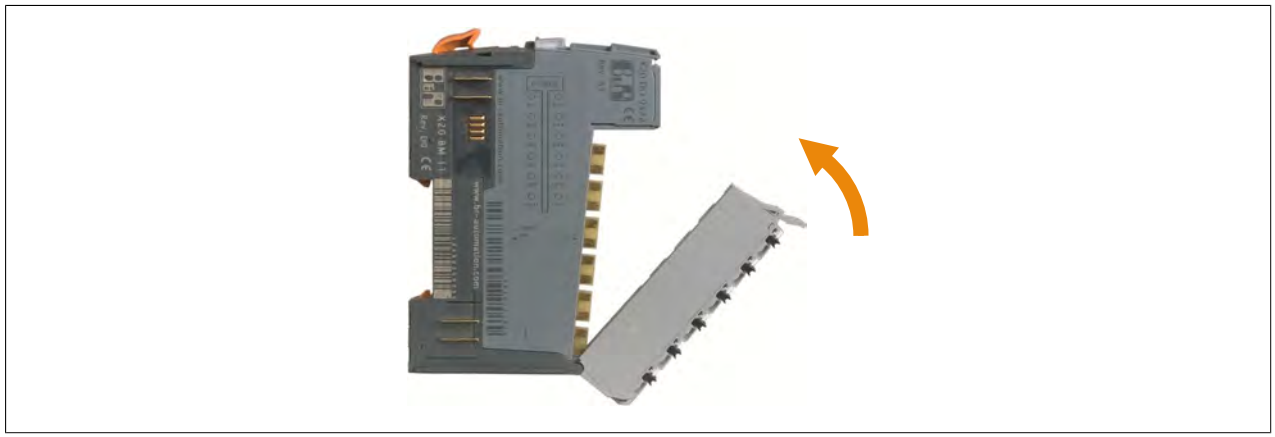


Figure 541: Rotate the terminal block up into place

14. The terminal block latch must close with an audible click. If the latch does not catch, the lever must be pushed up.

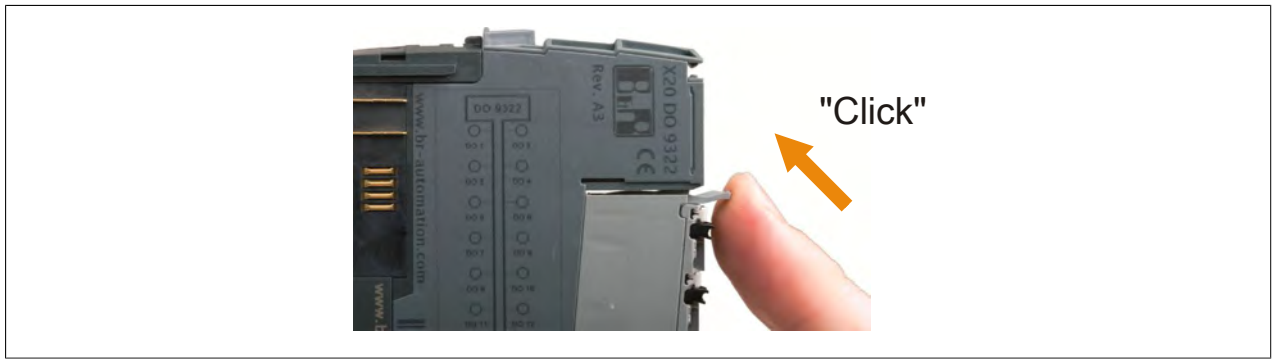


Figure 542: If the latch does not catch, the lever must be pushed up

15. Proceed like this with the rest of the terminal blocks.
16. Lay the left locking plate on the left module and insert it in the guides. Finally, slide the locking plate forward.

Figure 543: Lay the left locking plate on the left module and insert it in the guides

7.4 Installing the X20 system on the top-hat rail

Complete the following steps to install an assembled X20 system on the top-hat rail.

1. Push the locking lever all the way up on all of the bus modules. This opens the locking mechanism for top-hat rail installation.

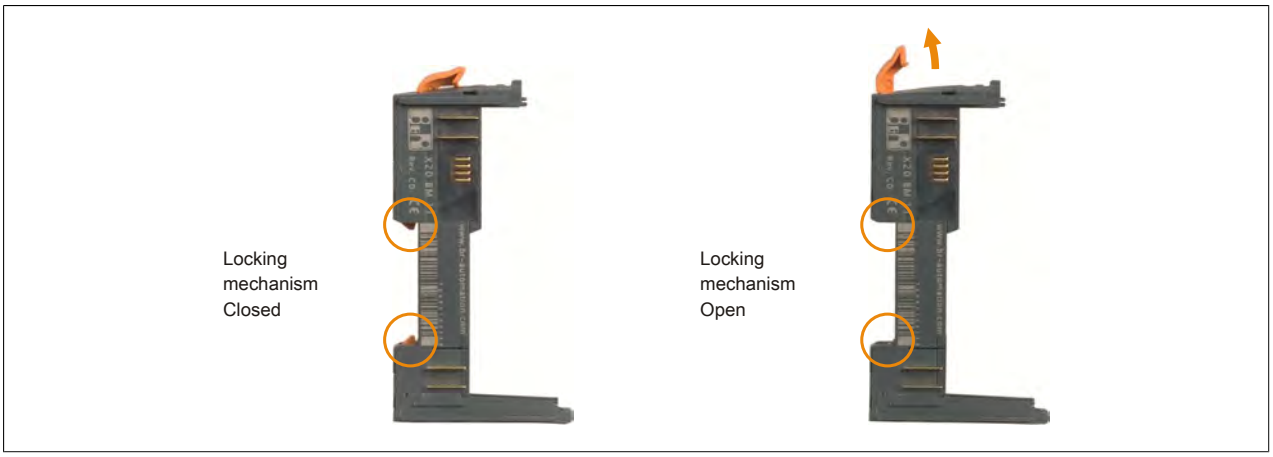


Figure 544: Push the locking lever all the way up to open the locking mechanism

2. Hang the X20 system in the desired position on the top-hat rail and close the locking mechanism by pushing the lever down.

7.5 Removing the X20 system from the top-hat rail

7.5.1 Remove the entire system from the top-hat rail

1. Push the locking lever all the way up on all of the bus modules. This opens the locking mechanism for top-hat rail installation.

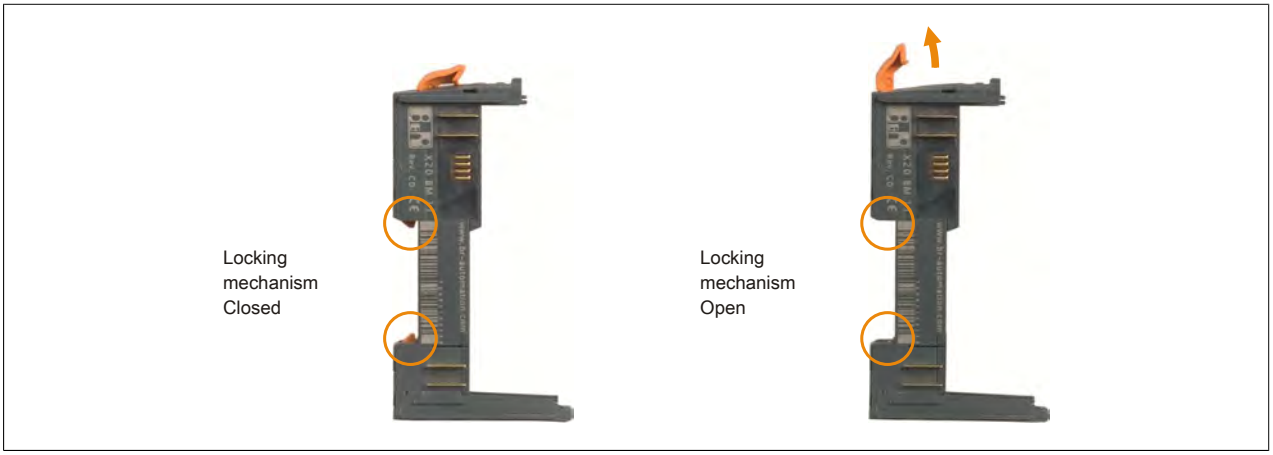


Figure 545: Push the locking lever all the way up to open the locking mechanism

2. Remove the X20 system from the top-hat rail.

7.5.2 Removing a block of modules from the top-hat rail

1. Push the locking lever all the way up on all of the modules that you wish to remove from the top-hat rail. This opens the locking mechanism for top-hat rail installation.

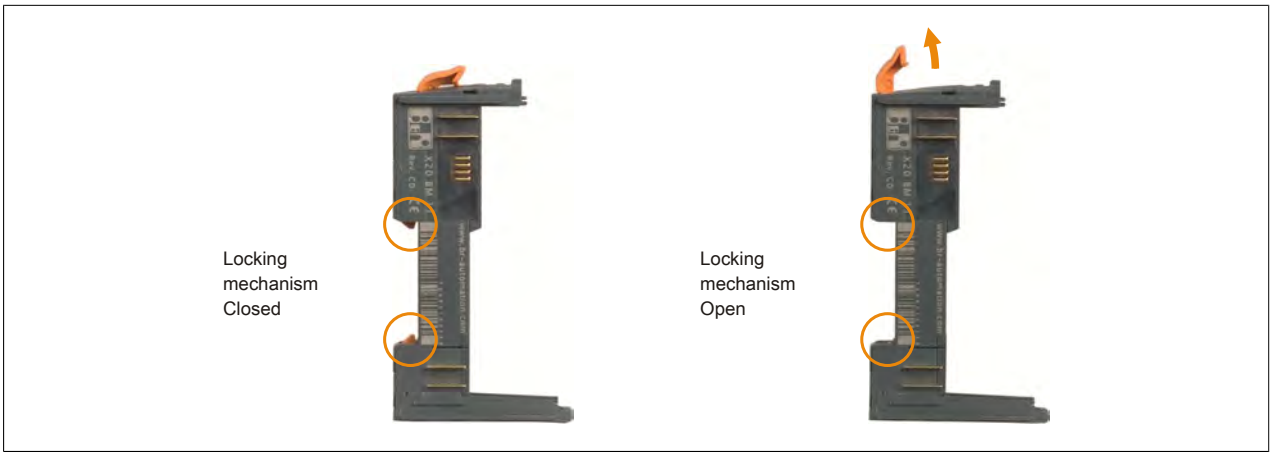


Figure 546: Push the locking lever all the way up to open the locking mechanism

2. The terminal block must be removed from the module to the left of the module block that is to be removed. To do this, push down on the locking lever on the terminal block ① and rotate the terminal block out and down ②.

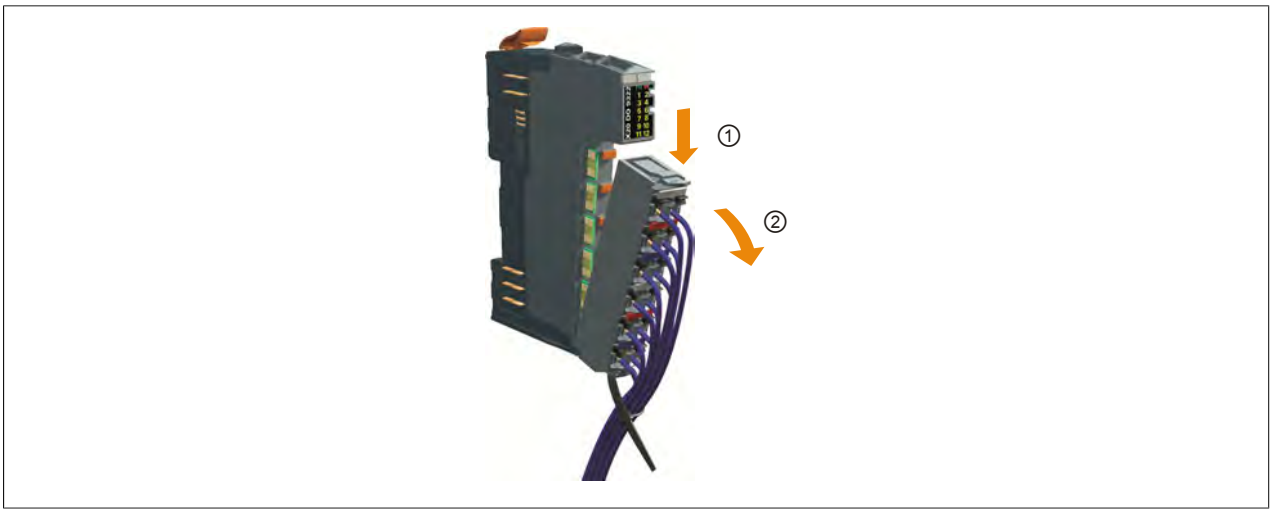


Figure 547: Remove the terminal block from the module to the left

3. Remove the module block from the top-hat rail.

Figure 548: Module block removed from the top-hat rail

4. Put the removed terminal block back on the module. To do this, hang the bottom in place in the bus module.

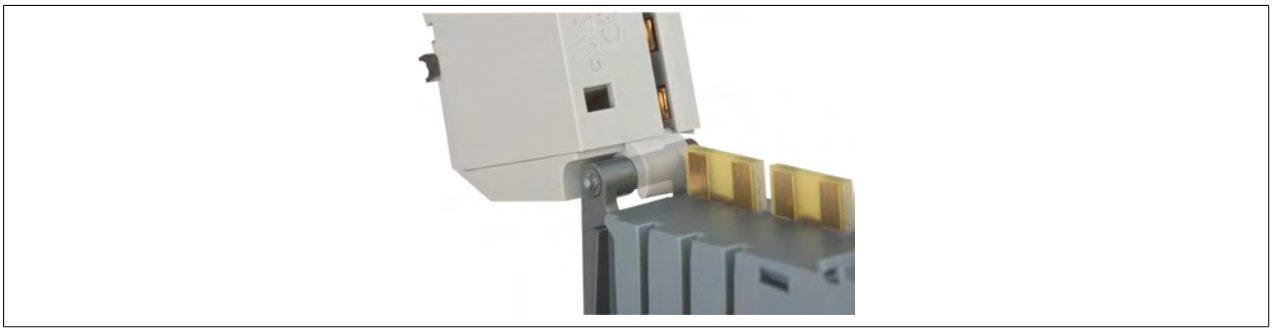


Figure 549: Hang the bottom edge of the terminal block in its place on the bus module

5. Rotate the terminal block up into place.

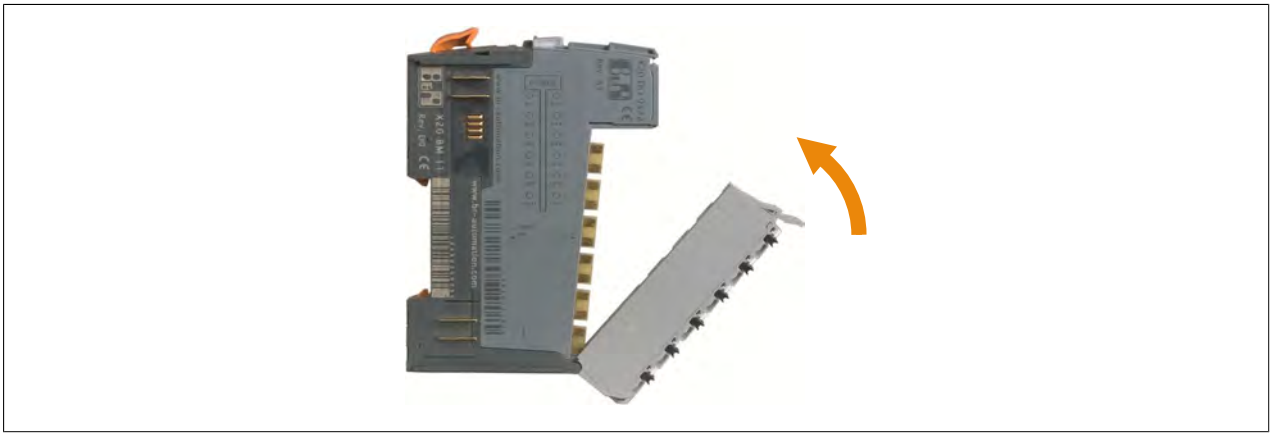


Figure 550: Rotate the terminal block up into place

6. The terminal block latch must close with an audible click. If the latch does not catch, the lever must be pushed up.

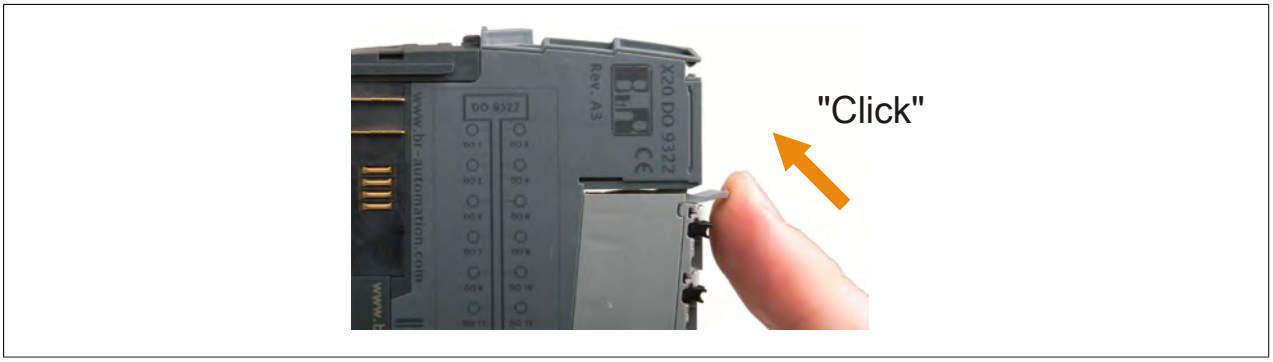


Figure 551: If the latch does not catch, the lever must be pushed up

7.6 Expanding an X20 system

If you want to expand an existing X20 system to the right, the right locking plate must be removed.

1. Remove the terminal block from the rightmost module. To do this, push down on the locking lever on the terminal block ① and rotate the terminal block out and down ②.

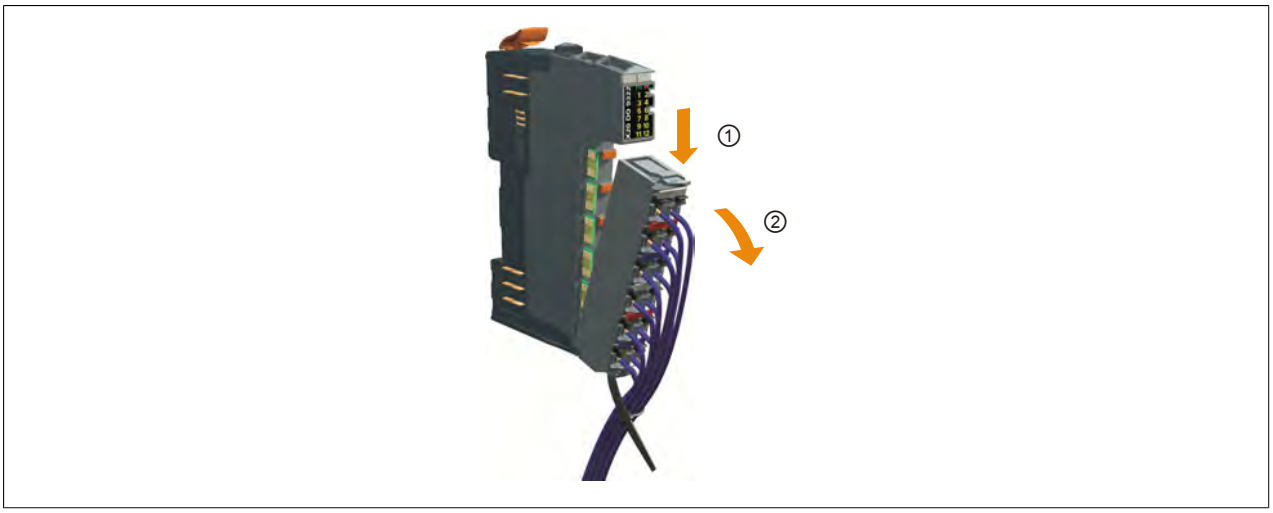


Figure 552: Remove the terminal block from the module to the left

2. Push down on the electronic module's locking lever ① and remove the electronic module ②.

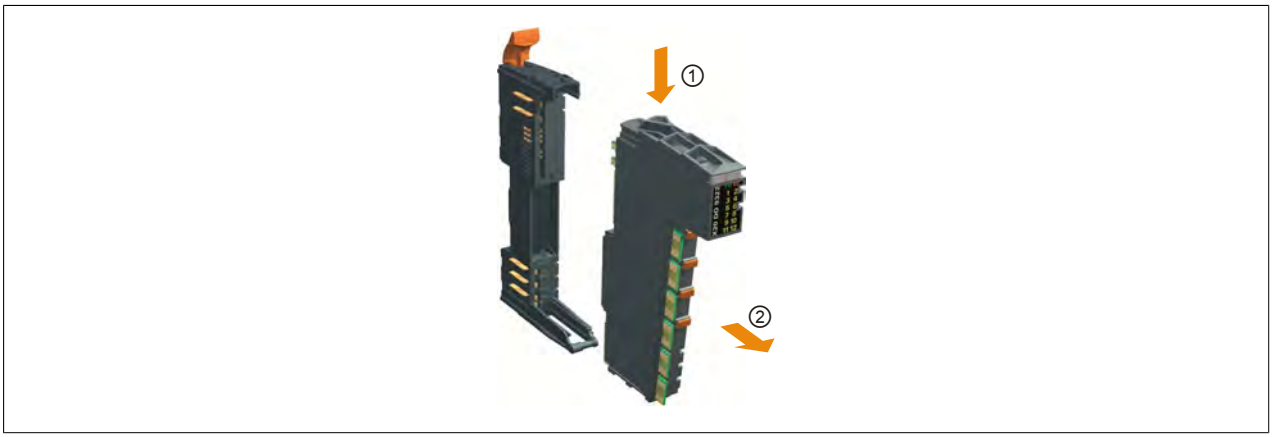


Figure 553: Remove the electronic module

3. Use a screwdriver to lift the locking lever of the right locking plate and pull the locking plate off of the bus module.

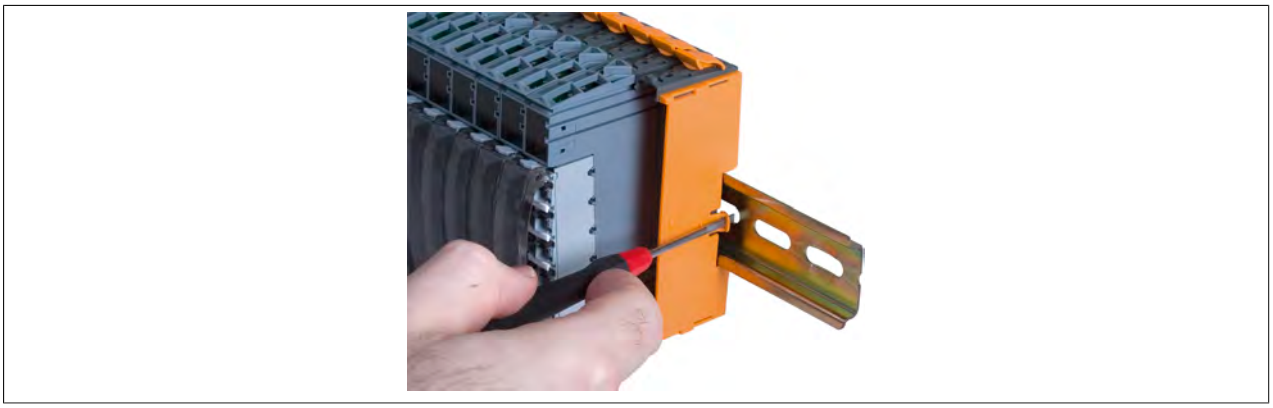


Figure 554: Unlock the right locking plate with a screwdriver

4. Now you can add more modules as described for assembly method 2 (see section 7.3.2 "Variant 2").

7.7 Installing accessories

7.7.1 Additional locking mechanisms

Some specific areas require additional locking mechanisms to prevent accidental release of the mechanical components.

7.7.1.1 Accessory locking clips

The accessory locking clip attaches the electronic module to the bus module. The locking clip is inserted in the appropriate opening on the module and pushed down.

Figure 555: Installing the accessory locking clip

7.7.1.2 Terminal locking clip

The terminal locking clip attaches the terminal block securely to the electronic module.

1. Set the terminal locking clip on the terminal block locking lever as shown.

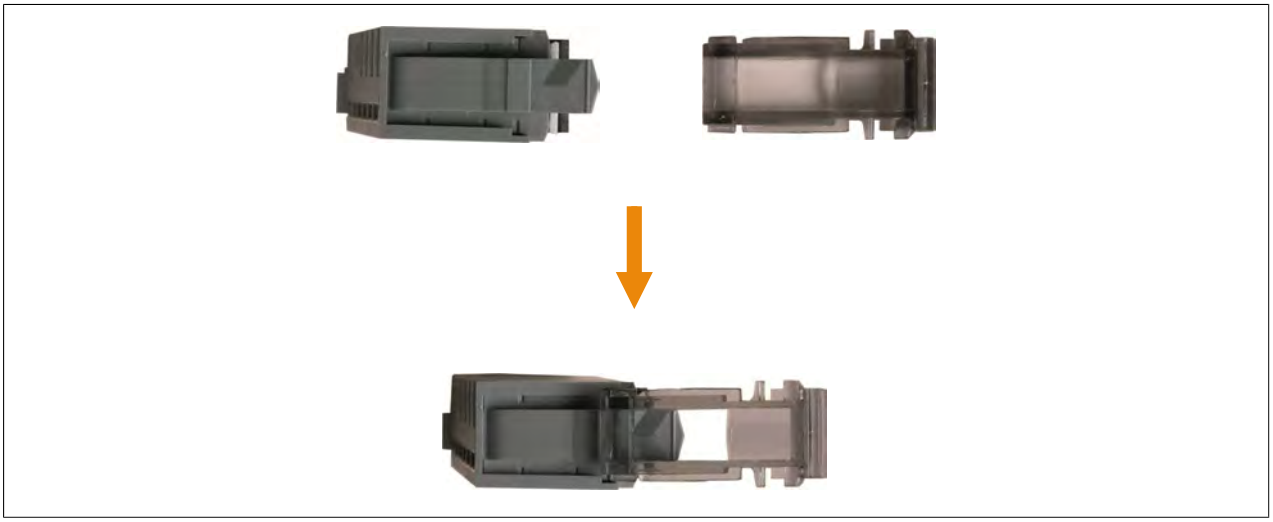


Figure 556: Set the terminal locking clip on the terminal block locking lever

2. Push down and hold the terminal locking clip and the locking lever with your index finger ①. Finally, slide the terminal locking clip forward with your thumb ②.

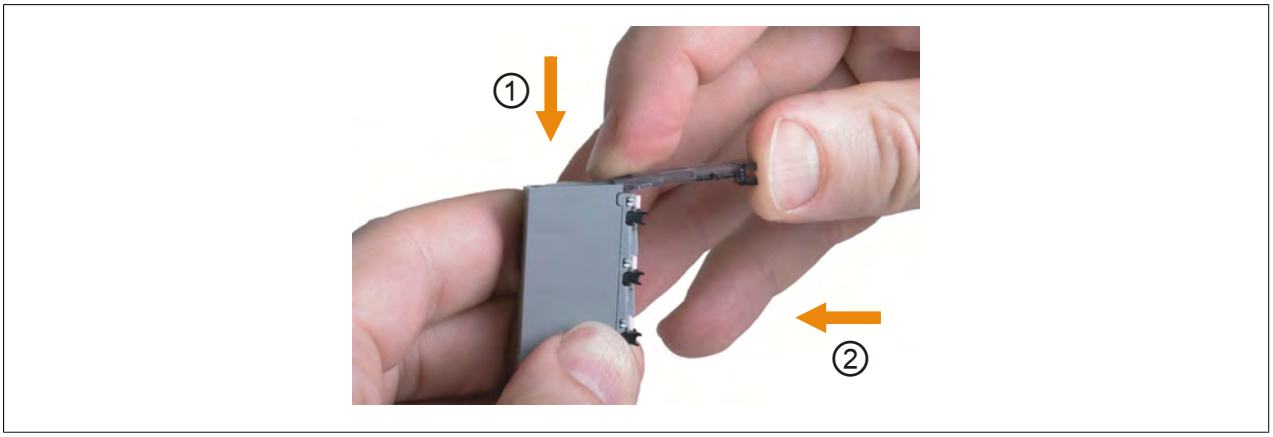


Figure 557: Install terminal locking clip on terminal block

3. Hang the bottom edge of the terminal block in its place on the bus module.

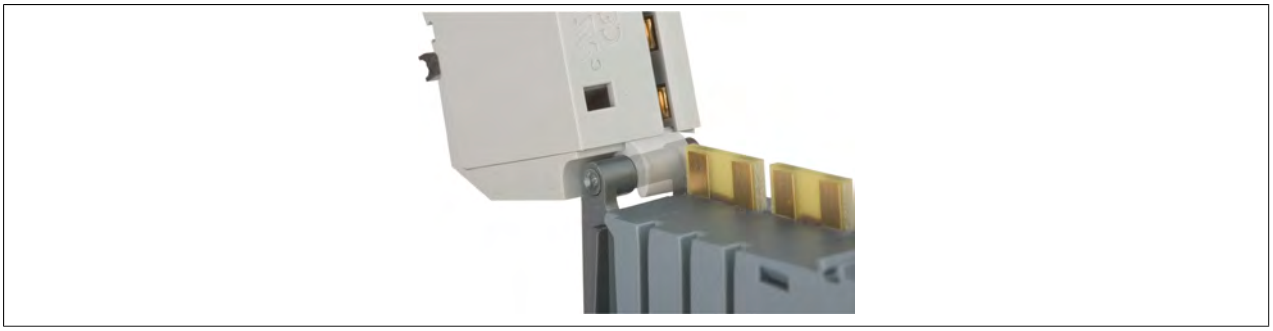


Figure 558: Hang the bottom edge of the terminal block in its place on the bus module

4. Rotate the terminal block up into place.

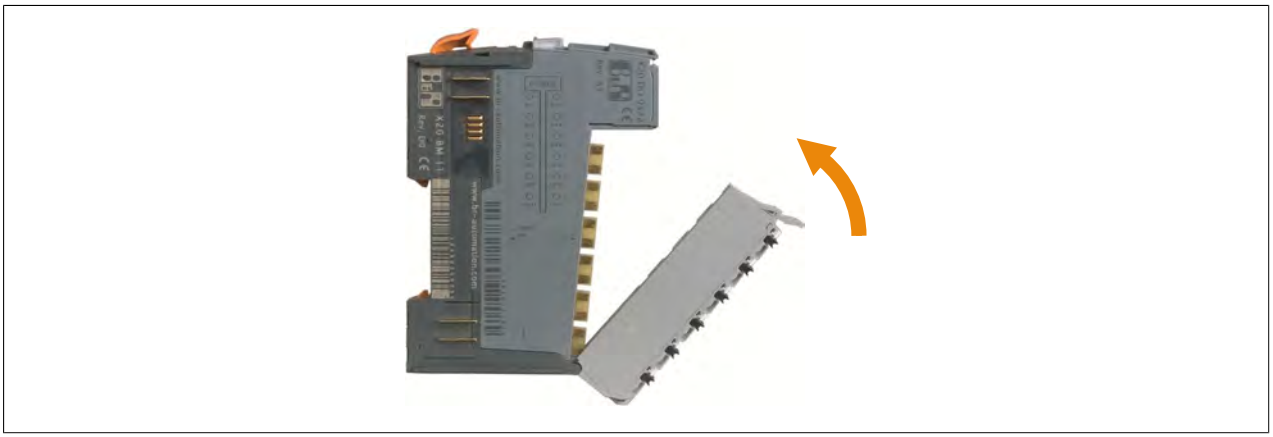


Figure 559: Rotate the terminal block up into place

5. Secure the terminal block in the electronic module by pushing in the terminal locking clip.

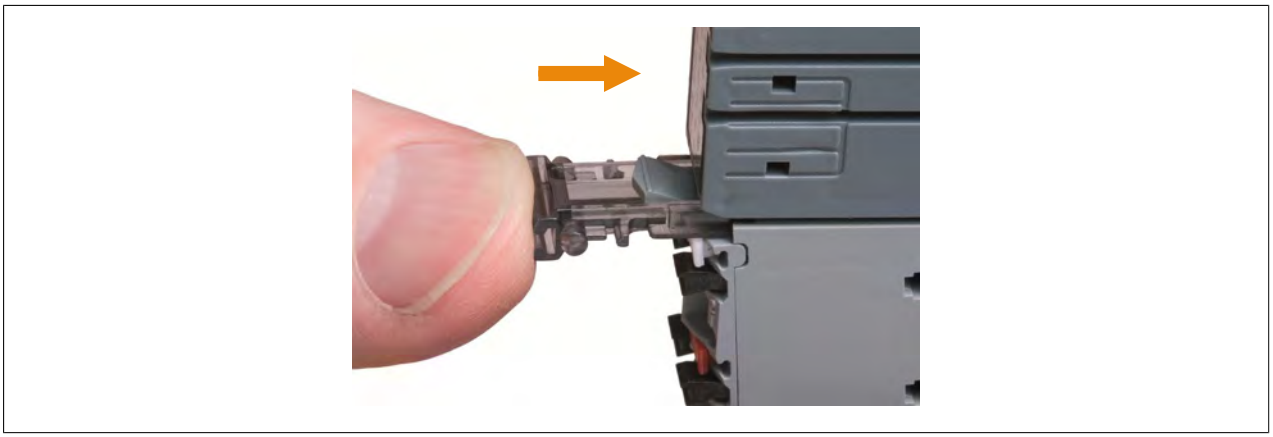


Figure 560: Secure the terminal block in the electronic module

6. Installed terminal locking clip.

Figure 561: Installed terminal locking clip

7. To remove the terminal block, pull the terminal locking clip out again.

7.7.2 Plain text tags

Tags are available for X20 modules into which plain text slide-in labels can be inserted. The tags are attached to the terminal locking clips.

1. Hold the plain text tag at a 90° angle to the terminal locking clip.
2. Push the plain text tag into the terminal locking clip's slot until it clicks into place.

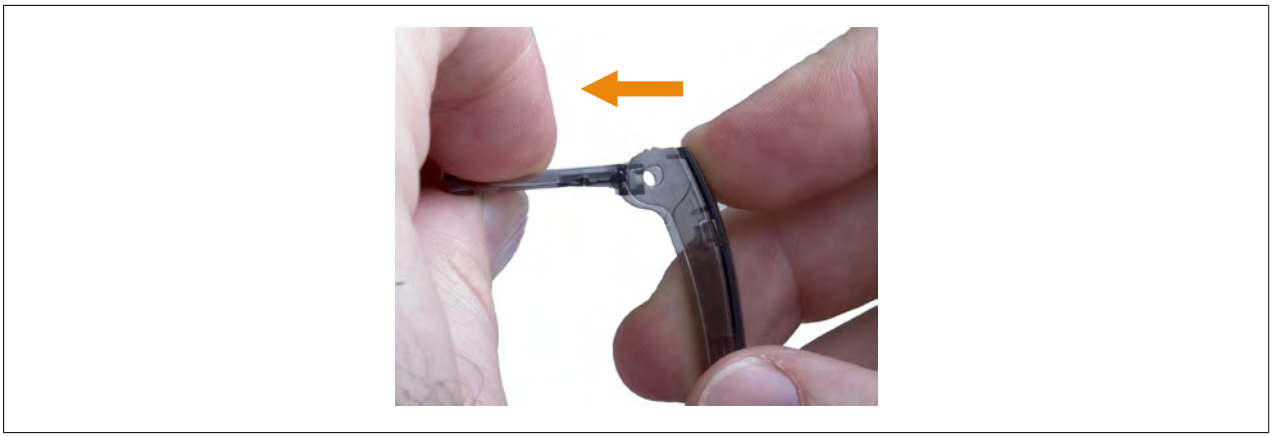
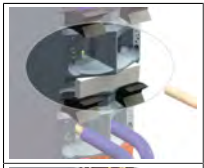
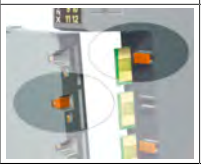


Figure 562: Attach plain text tag to terminal locking clip

7.8 Label tags

Label tags can serve the following purposes:

	Labeling the terminal connection		Labeling the module
	Labeling the terminal blocks		Labeling the terminals

The labeling tool is needed to attach the label tags.

Figure 563: Labeling tool

7.8.1 Labeling the terminal connection

This section explains how to label the terminal connection. The terminal connection, terminal blocks and modules are labeled in a similar manner.

Figure 564: Terminal block with label tags

1. Grip the desired label tags with the double-width cutters of the labeling tool.

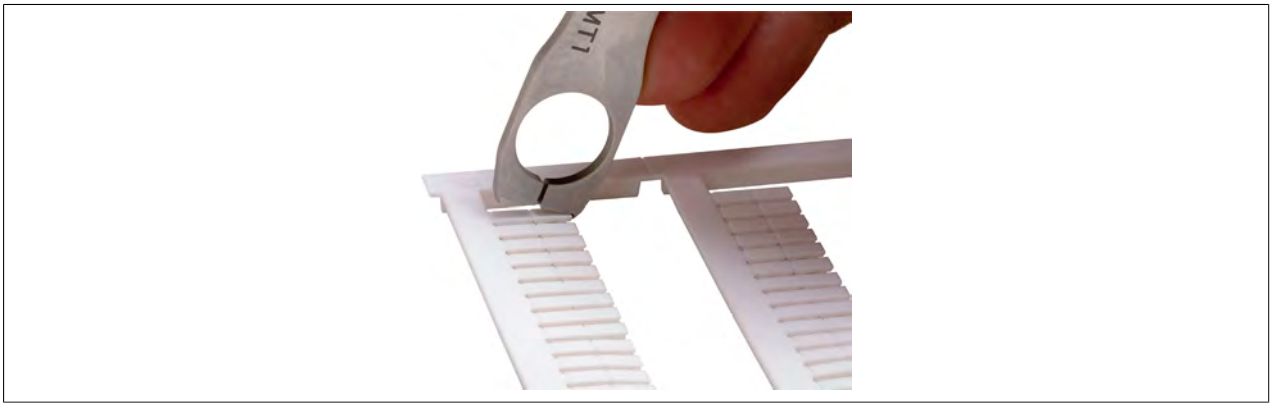


Figure 565: Grip desired label tags with labeling tool

2. Press with the labeling tool to separate the label tags.

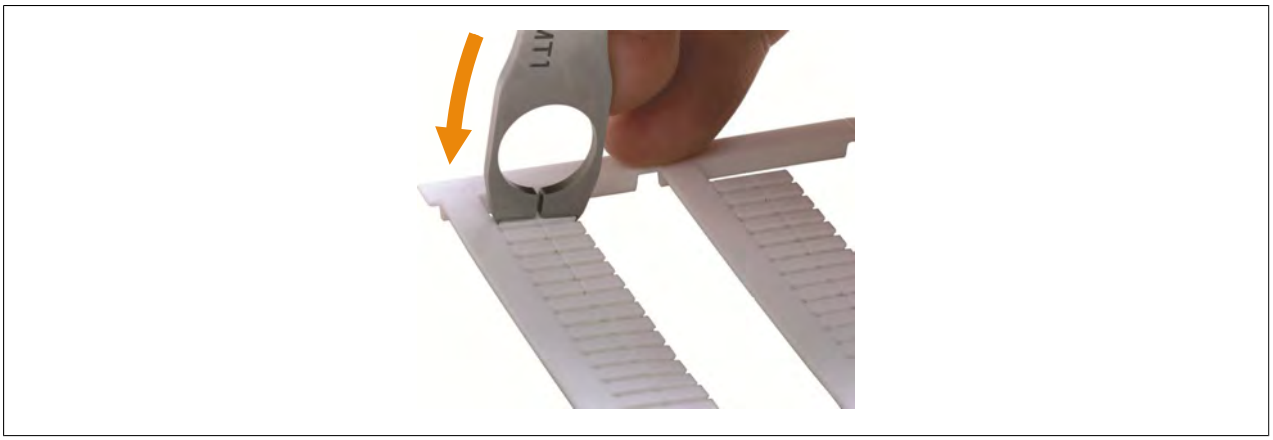


Figure 566: Separate the label tags with the labeling tool

3. Center the label tags over the slot on the terminal block.

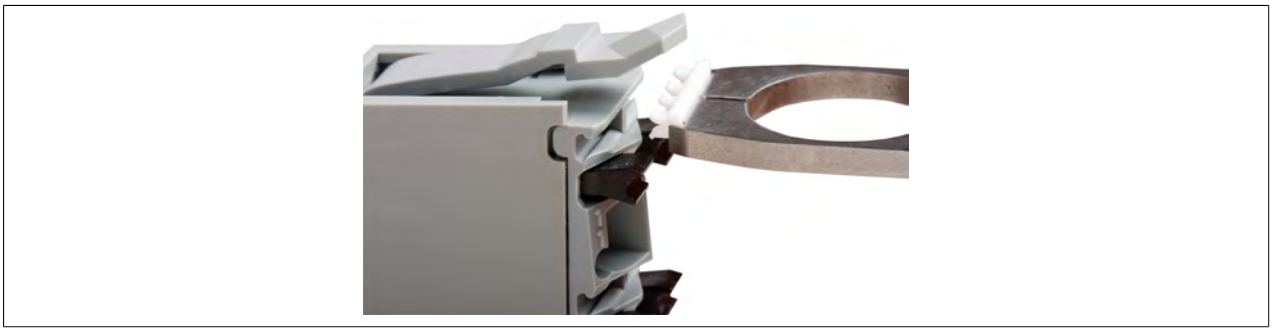


Figure 567: Center the label tags over the slot

4. Hold the labeling tool at approximately an 80° angle to the terminal block.

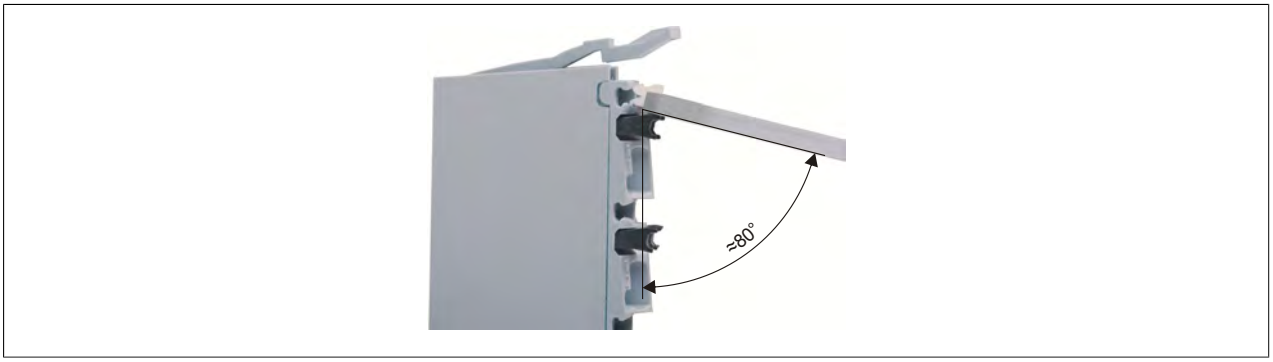


Figure 568: Hold the labeling tool at an approximately 80° angle to the terminal block

5. Press with the labeling tool to insert the feet of the label tags into the slot.
6. Inserted label tag.

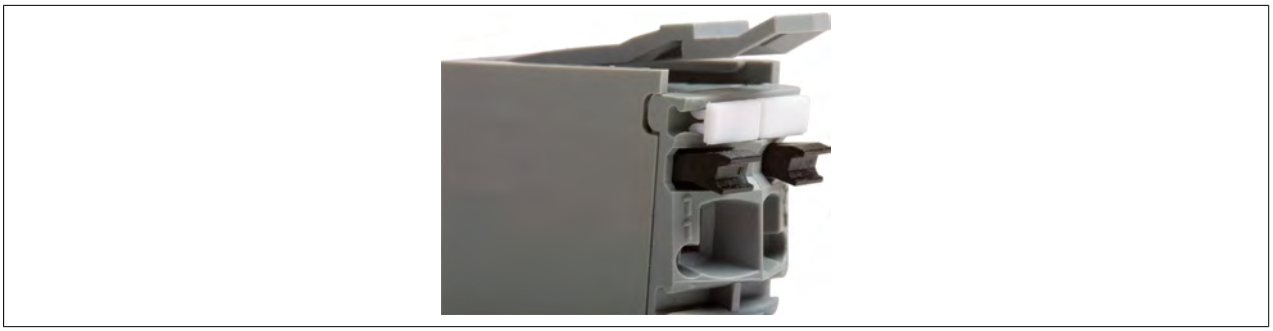


Figure 569: Inserted label tag

7.8.2 Labeling the terminals

To prevent errors, the X20 terminal blocks can be coded. This helps prevent terminal blocks from being inserted in the wrong electronic module.

Figure 570: Terminal coding helps prevent errors from the start.

1. Grip the desired label tag with the single-width cutters of the labeling tool (compare with section 7.8.1 "Labeling the terminal connection").
2. Center the label tag over the slot on the electronic module.

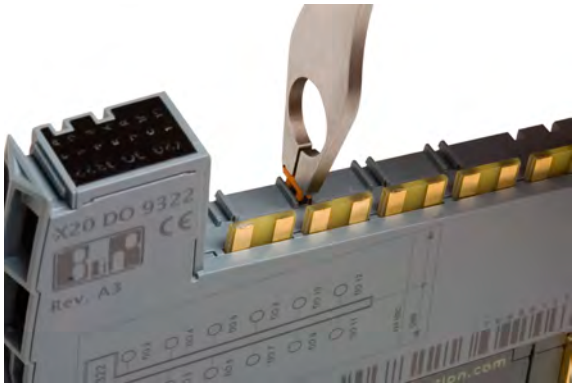


Figure 571: Center the label tag over the slot on the electronic module

3. Hold the labeling tool at a 90° angle to the electronic module and press to insert the label's feet into the slot.
4. Remove a label tag with the single-width cutter of the labeling tool.
5. Set the label tag in the slot on the back of the terminal block as shown.

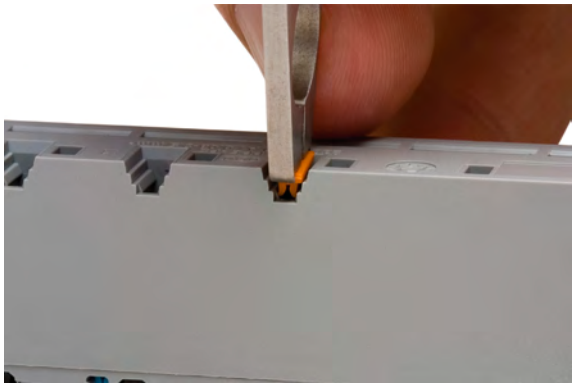


Figure 572: Set the label tag in the slot on the back of the terminal block

6. Use the labeling tool to push the left feet of the label into the slot.

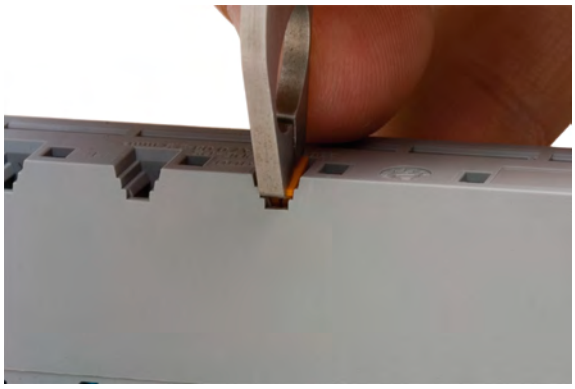


Figure 573: Press left feet of the label into the holes

7. With the labeling tool, press the right feet of the label into the slot.

Figure 574: Press right feet of the label into the slot

8. Inserted label for terminal coding.

Figure 575: Inserted label for terminal coding

8 Standards and certifications

8.1 Directives and explanations

CE mark

Product complies with all applicable directives and their harmonized EN standards.

EMC directive

These devices meet the requirements of EC directive "Electromagnetic compatibility 2004/108/EC" and are designed for industrial use:

EN 61131-2	Programmable logic controllers - Part 2: Equipment requirements and tests
EN 61000-6-2	Electromagnetic compatibility (EMC) - Part 6-2: Generic standards - Immunity for industrial environments
EN 61000-6-4	Electromagnetic compatibility (EMC) - Part 6-4: Generic standards - Emission standard for industrial environments

Low voltage directive

These devices satisfy the requirements of EC directive "Low voltage directive 2006/95/EC" and are designed for industrial use:

EN 61131-2	Programmable logic controllers - Part 2: Equipment requirements and tests

Machinery directive

The functional safety devices satisfy the requirements of the EC "Machinery directive 2006/42/EC". The products are certified by the recognized authorities (TÜV Rheinland, TÜV Süd, Underwriters Laboratories).

Information:

All standards refer to the currently valid year.

8.2 Certifications

Products and services from B&R comply with applicable standards. This includes international standards from organizations such as ISO, IEC and CENELEC, as well as national standards from organizations such as UL, CSA, GL, etc. We are committed to ensuring the reliability of our products in an industrial environment.

Information:

The certifications that apply to a particular module can be found in the following locations:

- **On the data sheet, in the "Technical data" table under "General information / Certification".**
- **At www.br-automation.com under "Products" in the "Certifications" area of the technical data**
- **On the side of the module housing**

UL certification

Products with this mark have been tested by Underwriters Laboratories and are listed as "Industrial Control Equipment". This mark is valid for the USA and Canada and simplifies the certification of your machines and systems in these areas.

Underwriters Laboratories (UL) in accordance with the UL508 standard - 17th Edition
Canadian (CSA) standard in accordance with C22.2 No. 142-M1987

CSA

Hazardous Locations

Products with this mark have been certified by the Canadian Standard Association and are suitable for use in potentially explosive environments. The X20 system is certified for Hazardous Locations Class I Division 2.
Each module is accompanied by an information sheet providing detailed installation and safety guidelines. This mark is valid for the USA and Canada and simplifies the certification of your machines and systems in these areas.

Functional safety

Products with this mark were designed, developed and manufactured for special applications for machine and personnel protection. The products are certified by the recognized authorities (TÜV Rheinland, TÜV Süd, Underwriters Laboratories), and satisfy the requirements of international safety standards ISO 13849, IEC 62061, IEC 61511 and IEC 61508.

DNV GL Maritime (Germanischer Lloyd)

Many B&R products are certified by Germanischer Lloyd and suitable for use in maritime environments. DNV GL Maritime certificates (type approval) are generally accepted by other classification societies during ship acceptance procedures.

Germanischer Lloyd (GL) in accordance with standard GL VI-7-2 (2012) (Categories B and D, each EMC1)

LR (Lloyd's Register Marine)

Products are suitable for use in maritime environments in accordance with the guidelines set forth by the Lloyd's Register classification society. Approval has been granted for marine, offshore and industrial applications for environmental categories ENV1, ENV2, and ENV3. These environmental categories are defined in the Lloyd's Register's Type Approval System, Test Specification Number 1-2013.

ATEX

Products with this mark have been tested by an accredited testing laboratory and are suitable for use in potentially explosive environments.
The X20 system is certified for use in environments with explosive gases with a normal level of safety in Zone 2.
Each module is accompanied by an information sheet providing detailed installation and safety guidelines.

GOST-R

Products with this mark have been tested by an accredited testing laboratory and approved for import to the Russian Federation (based on EU compliance).

EAC

Products with this mark have been tested by an accredited testing laboratory and approved for import (based on EU compliance) to the newly founded Eurasian Economic Union (Russia, Belarus, Kazakhstan).

KC

Products with this mark have been tested by an accredited testing laboratory and have been approved for import to the Korean market (based on EU compliance).

RCM

Products with this mark have been tested by an accredited testing laboratory and certified by the ACMA. This mark is valid in Australia/Oceania and simplifies the certification of your machines and systems in these areas (based on EU compliance).

Appendix A Abbreviations

A.1 General information

Abbreviations appear throughout this user's manual in technical data tables or descriptions of pinouts, for example.

A.2 Overview

Abbreviation	Stands for	Description
NC	Normally closed	A normally closed relay contact
	Not connected	Used in pinout descriptions if a terminal or pin is not connected to a module
ND	Not defined	In data tables, this stands for a value that has not been defined. This may be because a cable manufacturer does not provide certain technical data, for example.
NO	Normally open	A normally open relay contact
TBD	To be defined	Used in technical data tables when certain information is not yet available. The value will be provided later.

Table 768: Abbreviations used in this user's manual

Appendix B B&R ID codes

B.1 General information

This appendix contains two overviews of B&R ID codes:

- B&R ID codes sorted by ID code
- B&R ID codes sorted by model number

The B&R ID code is displayed in Automation Studio for error messages, for example. The tables in this appendix can be used to determine the corresponding module type and respective description.

B.2 B&R ID codes sorted by ID code

Product ID	B&R ID code (hex.)	B&R ID code (dec.)	on page
X20DI2371	0x1B8D	7053	1215
X20DI2377	0x1B8E	7054	1227
X20DI4371	0x1B92	7058	1241
X20DI6371	0x1B93	7059	1280
X20DI6372	0x1B94	7060	1286
X20DI9371	0x1B95	7061	1310
X20DO2322	0x1B96	7062	1357
X20DO4322	0x1B97	7063	1404
X20DO6322	0x1B98	7064	1490
X20DO6321	0x1B99	7065	1483
X20DO9322	0x1B9A	7066	1580
X20DO9321	0x1B9B	7067	1572
X20DO4332	0x1B9C	7068	1423
X20DO8332	0x1B9D	7069	1560
X20AI2622	0x1B9E	7070	252
X20AI2632	0x1BA0	7072	263
X20AI4632	0x1BA1	7073	373
X20AO2622	0x1BA2	7074	661
X20AO4622	0x1BA3	7075	682
X20AO2632	0x1BA4	7076	668
X20AT2222	0x1BA6	7078	2939
X20AT4222	0x1BA7	7079	2969
X20AT2402	0x1BA8	7080	2957
X20AT6402	0x1BA9	7081	2979
X20AI4622	0x1BAA	7082	362
X20DC2396	0x1BAB	7083	1048
X20DC1396	0x1BAC	7084	961
X20DC2398	0x1BAD	7085	1059
X20DC1398	0x1BAE	7086	971
X20DC1196	0x1BAF	7087	898
X20DC1198	0x1BB0	7088	908
X20PS2100	0x1BBF	7103	2884
X20PS3300	0x1BC0	7104	2900
X20BR9300	0x1BC1	7105	815
X20BT9100	0x1BC2	7106	821
X20DC4395	0x1CC5	7365	1066
X20DC2395	0x1CD4	7380	1008
X20AI1744	0x1CDE	7390	132
X20DI9372	0x1D28	7464	1317
X20CM8323	0x1D43	7491	2759
X20CM1941	0x1E85	7813	860
X20BC0043	0x1F1A	7962	717
X20BC0053	0x1F1B	7963	731
X20BC0063	0x1F1C	7964	737
X20BC0073	0x1F1D	7965	741
X20BC0083	0x1F1E	7966	747
X20IF1082	0x1F1F	7967	2224
X20IF1072	0x1F20	7968	2220
X20IF1061	0x1F22	7970	2203
X20IF1063	0x1F23	7971	2210
X20IF1091	0x1F24	7972	2242
X20IF2772	0x1F25	7973	2279
X20IF2792	0x1F26	7974	2283
X20IF1020	0x1F27	7975	2181
X20IF1030	0x1F28	7976	2184
X20PS4951	0x1F43	8003	2877
X20PS9400	0x1F8C	8076	784
X20CS1020	0x1FCF	8143	1949
X20CS1030	0x1FD0	8144	1992
X20CS1070	0x1FD1	8145	2035
X20PS2110	0x2016	8214	2889
X20PS9500	0x2018	8216	848
X20DO6529	0x2019	8217	1509
X20DM9324	0x20B9	8377	1338
X20DO4529	0x20D9	8409	1433
X20DO2649	0x20DA	8410	1390
X20DI4760	0x2105	8453	1271
X20DC2190	0x2188	8584	994
X20CM1201	0x21EF	8687	1603
X20BC1083	0x2268	8808	2125
X20BC0087	0x227C	8828	753
X20CP0201	0x22A2	8866	837

Product ID	B&R ID code (hex.)	B&R ID code (dec.)	on page
X20CP0291	0x22A4	8868	837
X20CP0292	0x22A6	8870	837
X20DI2372	0x22A7	8871	1221
X20DI4372	0x22A8	8872	1248
X20DO2321	0x22B3	8883	1349
X20DO4321	0x22B4	8884	1396
X20DO4331	0x22B5	8885	1413
X20DO8331	0x22EB	8939	1548
X20CM0985	0x2433	9267	2552
X20CM8281	0x24C3	9411	2740
X20IF1091-1	0x2525	9509	2154
X20DI2653	0x2544	9540	1235
X20DI4653	0x2545	9541	1265
X20DS1319	0x2547	9543	1678
X20XC0201	0x2563	9571	2160
X20XC0202	0x2564	9572	2160
X20DI6553	0x256F	9583	1298
X20BC8083	0x2673	9843	2132
X20BC8084	0x2674	9844	2138
X20DO2623	0x267B	9851	1365
X20DO4623	0x267C	9852	1452
X20PD0011	0x267D	9853	2858
X20PD0012	0x267E	9854	2862
X20PD2113	0x267F	9855	2871
X20PD0016	0x2680	9856	2866
X20SM1426	0x2681	9857	2387
X20SM1436	0x2682	9858	2432
X20MM2436	0x26B5	9909	2318
X20BC0088	0x26D8	9944	759
X20CS2770	0xA009	40969	2079
X20DS1119	0xA067	41063	1637
X20MM4456	0xA177	41335	2366
X20BT9400	0xA238	41528	828
X20CP1483	0xA239	41529	1168
X20XC0292	0xA252	41554	2160
X20AI4632-1	0xA29D	41629	399
X20AI2632-1	0xA29E	41630	288
X20PS9402	0xA389	41865	791
X20PS9502	0xA38A	41866	854
X20CS1011	0xA38D	41869	1875
X20DS4387	0xA38E	41870	2777
X20IF1074	0xA399	41881	2176
X20AT2311	0xA4AA	42154	2949
X20DI8371	0xA4AB	42155	1304
X20DO8322	0xA4AC	42156	1532
X20DO8232	0xA4AD	42157	1521
X20IF1065	0xA4C6	42182	2217
X20AI1744-3	0xA4EF	42223	132
X20DO4649	0xA704	42756	1477
X20DC1376	0xA705	42757	931
X20DC1176	0xA706	42758	867
X20DC1976	0xA707	42759	978
X20DC1178	0xA708	42760	883
X20IF1041-1	0xA709	42761	2187
X20IF1043-1	0xA70B	42763	2191
X20IF1051-1	0xA70C	42764	2195
X20IF1053-1	0xA715	42773	2199
X20IF1061-1	0xA716	42774	2206
X20IF1063-1	0xA717	42775	2213
X20IF10A1-1	0xA718	42776	2245
X20IF10D1-1	0xA71B	42779	2249
X20IF10D3-1	0xA71C	42780	2253
X20IF10E1-1	0xA71D	42781	2257
X20IF10E3-1	0xA71E	42782	2261
X20IF10G3-1	0xA72C	42796	2265
X20CM6209	0xA7A1	42913	2737
X20DI6373	0xA7A2	42914	1292
X20IF1082-2	0xA7A3	42915	2230
X20AO4635	0xA7FE	43006	708
X20BC0043-10	0xA8B8	43192	724
X20DI4375	0xA911	43281	1254
X20DS1928	0xA912	43282	1780
X20DS4389	0xA93B	43323	1833
X20MM4331	0xA976	43382	2353

Product ID	B&R ID code (hex.)	B&R ID code (dec.)	on page
X20MM3332	0xA982	43394	2338
X20BC00G3	0xAC23	44067	770
X20DO2633	0xAC39	44089	1374
X20DO4633	0xAC3A	44090	1461
X20DO4613	0xAD05	44293	1439
X20BC0143-10	0xAD3E	44350	774
X20BC80G3	0xAEC2	44738	2145
X20CP1483-1	0xAEC5	44741	1168
X20DC1073	0xAEC6	44742	1623
X20DS1828	0xAEC7	44743	1720
X20AI2636	0xB3A7	45991	313
X20AI4636	0xB3A8	45992	425
X20AI2438	0xB3A9	45993	199
X20AO2438	0xB3AA	45994	608
X20IF1086-2	0xB455	46165	2236
X20CM0985-1	0xB768	46952	2481
X20DC11A6	0xB76B	46955	915
X20AI2437	0xB784	46980	183
X20AO2437	0xB785	46981	597
X20BC00E3	0xBB7D	47997	764
X20ATA492	0xBB98	48024	3002
X20ATC402	0xBB99	48025	3036
X20CP3586	0xBF2B	48939	1189
X20DID371	0xC0E7	49383	1324
X20DIF371	0xC0E8	49384	1330
X20DOD322	0xC0E9	49385	1588
X20DOF322	0xC0EA	49386	1594
X20AO2632-1	0xC36E	50030	675
X20CP1584	0xC370	50032	1185
X20CP3584	0xC3AD	50093	1189
X20CP1585	0xC3AE	50094	1185
X20CP3585	0xC3AF	50095	1189
X20CP1586	0xC3B0	50096	1185
X20IF2181-2	0xC3B3	50099	2273
X20IF10X0	0xC3B4	50100	2269
X20CM4810	0xC8F9	51449	2594
X20AI2237	0xC9C4	51652	157
X20AP3111	0xC9DA	51674	510
X20AP3121	0xC9DB	51675	510
X20AP3131	0xC9DC	51676	510
X20AI2222	0xCAB0	51888	148
X20AI4222	0xCAB1	51889	344
X20AI2322	0xCAB2	51890	174
X20AI4322	0xCAB3	51891	353
X20CS1012	0xCABF	51903	1890
X20DS438A	0xCAC0	51904	2794
X20CP1583	0xD45B	54363	1185
X20CP3583	0xD45C	54364	1189
X20cDI9371	0xD574	54644	1310
X20cBC0087	0xD577	54647	753
X20cDO9322	0xD578	54648	1580
X20cPS9400	0xD579	54649	784
X20cAI4632-1	0xD57A	54650	399
X20AI8221	0xD82F	55343	456
X20AI8321	0xD831	55345	465
X20CP1382	0xDABB	55995	1112
X20DC137A	0xDD28	56616	946
X20cBR9300	0xDD48	56648	815
X20cAT6402	0xDD57	56663	2979
X20CS1013	0xDE85	56965	1938
X20cBC8084	0xDF10	57104	2138
X20cPS3300	0xDF13	57107	2900
X20DO8323	0xDF4E	57166	1539
X20DO6639	0xDF50	57168	1515
X20ATA312	0xE0E4	57572	2991
X20ATB312	0xE0EF	57583	3025
X20AP3161	0xE17B	57723	510
X20cAI2438	0xE1EE	57838	199
X20cAI4622	0xE1EF	57839	362
X20cAI4632	0xE1F0	57840	373
X20cAO2437	0xE1F2	57842	597
X20cDS1119	0xE20D	57869	1637
X20cAO2438	0xE211	57873	608
X20cAO4622	0xE212	57874	682

Product ID	B&R ID code (hex.)	B&R ID code (dec.)	on page
X20cAP3121	0xE214	57876	510
X20cAT4222	0xE215	57877	2969
X20cBC0083	0xE216	57878	747
X20cBC1083	0xE217	57879	2125
X20cBC8083	0xE218	57880	2132
X20cBT9100	0xE219	57881	821
X20cCP1584	0xE21B	57883	1185
X20cCP1586	0xE21C	57884	1185
X20cCP3584	0xE21D	57885	1189
X20cCP3586	0xE21E	57886	1189
X20cDI4371	0xE21F	57887	1241
X20cDI4375	0xE220	57888	1254
X20cDI4760	0xE221	57889	1271
X20cDI6371	0xE222	57890	1280
X20cDI6372	0xE223	57891	1286
X20cDI9372	0xE224	57892	1317
X20cDM9324	0xE225	57893	1338
X20cDO4322	0xE226	57894	1404
X20cDO4332	0xE227	57895	1423
X20cDO6321	0xE228	57896	1483
X20cDO6322	0xE229	57897	1490
X20cDO6639	0xE22A	57898	1515
X20cDO8331	0xE22B	57899	1548
X20cDO8332	0xE22C	57900	1560
X20cDO9321	0xE22D	57901	1572
X20cIF1030	0xE233	57907	2184
X20cIF1061-1	0xE234	57908	2206
X20cIF1063-1	0xE235	57909	2213
X20cIF1082-2	0xE236	57910	2230
X20cIF10D3-1	0xE237	57911	2253
X20cIF10E3-1	0xE238	57912	2261
X20cIF10X0	0xE239	57913	2269
X20cIF2181-2	0xE23A	57914	2273
X20cPD2113	0xE23B	57915	2871
X20cPS2100	0xE23C	57916	2884
X20cPS2110	0xE23D	57917	2889
X20DO6325	0xE284	57988	1498
X20AIB744	0xE286	57990	492
X20CP1301	0xE35B	58203	1112
X20CP1381	0xE35C	58204	1112
X20cBC00E3	0xE4E0	58592	764
X20cCS1030	0xE500	58624	1992
X20cDC1198	0xE501	58625	908
X20cDC1396	0xE502	58626	961
X20cDC2395	0xE503	58627	1008
X20cIF1041-1	0xE505	58629	2187
X20cIF1072	0xE506	58630	2220
X20AIA744	0xE50C	58636	474
X20cDO4633	0xE67D	59005	1461
X20cDO4649	0xE67E	59006	1477
X20cBC0088	0xE67F	59007	759
X20cDO2633	0xE680	59008	1374
X20DI0471	0xE7CE	59342	1208
X20cCS1020	0xE7F2	59378	1949

B.3 B&R ID codes sorted by model number

Product ID	B&R ID code (hex.)	B&R ID code (dec.)	on page
X20AI1744	0x1CDE	7390	132
X20AI1744-3	0xA4EF	42223	132
X20AI2222	0xCAB0	51888	148
X20AI2237	0xC9C4	51652	157
X20AI2322	0xCAB2	51890	174
X20AI2437	0xB784	46980	183
X20AI2438	0xB3A9	45993	199
X20AI2622	0x1B9E	7070	252
X20AI2632	0x1BA0	7072	263
X20AI2632-1	0xA29E	41630	288
X20AI2636	0xB3A7	45991	313
X20AI4222	0xCAB1	51889	344
X20AI4322	0xCAB3	51891	353
X20AI4622	0x1BAA	7082	362
X20AI4632	0x1BA1	7073	373
X20AI4632-1	0xA29D	41629	399
X20AI4636	0xB3A8	45992	425
X20AI8221	0xD82F	55343	456
X20AI8321	0xD831	55345	465
X20AIA744	0xE50C	58636	474
X20AIB744	0xE286	57990	492
X20AO2437	0xB785	46981	597
X20AO2438	0xB3AA	45994	608
X20AO2622	0x1BA2	7074	661
X20AO2632	0x1BA4	7076	668
X20AO2632-1	0xC36E	50030	675
X20AO4622	0x1BA3	7075	682
X20AO4635	0xA7FE	43006	708
X20AP3111	0xC9DA	51674	510
X20AP3121	0xC9DB	51675	510
X20AP3131	0xC9DC	51676	510
X20AP3161	0xE17B	57723	510
X20AT2222	0x1BA6	7078	2939
X20AT2311	0xA4AA	42154	2949
X20AT2402	0x1BA8	7080	2957
X20AT4222	0x1BA7	7079	2969
X20AT6402	0x1BA9	7081	2979
X20ATA312	0xE0E4	57572	2991
X20ATA492	0xBB98	48024	3002
X20ATB312	0xE0EF	57583	3025
X20ATC402	0xBB99	48025	3036
X20BC0043	0x1F1A	7962	717
X20BC0043-10	0xA8B8	43192	724
X20BC0053	0x1F1B	7963	731
X20BC0063	0x1F1C	7964	737
X20BC0073	0x1F1D	7965	741
X20BC0083	0x1F1E	7966	747
X20BC0087	0x227C	8828	753
X20BC0088	0x26D8	9944	759
X20BC00E3	0xBB7D	47997	764
X20BC00G3	0xAC23	44067	770
X20BC0143-10	0xAD3E	44350	774
X20BC1083	0x2268	8808	2125
X20BC8083	0x2673	9843	2132
X20BC8084	0x2674	9844	2138
X20BC80G3	0xAEC2	44738	2145
X20BR9300	0x1BC1	7105	815
X20BT9100	0x1BC2	7106	821
X20BT9400	0xA238	41528	828
X20CM0985	0x2433	9267	2552
X20CM0985-1	0xB768	46952	2481
X20CM1201	0x21EF	8687	1603
X20CM1941	0x1E85	7813	860
X20CM4810	0xC8F9	51449	2594
X20CM6209	0xA7A1	42913	2737
X20CM8281	0x24C3	9411	2740
X20CM8323	0x1D43	7491	2759
X20CP0201	0x22A2	8866	837
X20CP0291	0x22A4	8868	837
X20CP0292	0x22A6	8870	837
X20CP1301	0xE35B	58203	1112
X20CP1381	0xE35C	58204	1112

Product ID	B&R ID code (hex.)	B&R ID code (dec.)	on page
X20CP1382	0xDABB	55995	1112
X20CP1483	0xA239	41529	1168
X20CP1483-1	0xAEC5	44741	1168
X20CP1583	0xD45B	54363	1185
X20CP1584	0xC370	50032	1185
X20CP1585	0xC3AE	50094	1185
X20CP1586	0xC3B0	50096	1185
X20CP3583	0xD45C	54364	1189
X20CP3584	0xC3AD	50093	1189
X20CP3585	0xC3AF	50095	1189
X20CP3586	0xBF2B	48939	1189
X20CS1011	0xA38D	41869	1875
X20CS1012	0xCABF	51903	1890
X20CS1013	0xDE85	56965	1938
X20CS1020	0x1FCF	8143	1949
X20CS1030	0x1FD0	8144	1992
X20CS1070	0x1FD1	8145	2035
X20CS2770	0xA009	40969	2079
X20DC1073	0xAEC6	44742	1623
X20DC1176	0xA706	42758	867
X20DC1178	0xA708	42760	883
X20DC1196	0x1BAF	7087	898
X20DC1198	0x1BB0	7088	908
X20DC11A6	0xB76B	46955	915
X20DC1376	0xA705	42757	931
X20DC137A	0xDD28	56616	946
X20DC1396	0x1BAC	7084	961
X20DC1398	0x1BAE	7086	971
X20DC1976	0xA707	42759	978
X20DC2190	0x2188	8584	994
X20DC2395	0x1CD4	7380	1008
X20DC2396	0x1BAB	7083	1048
X20DC2398	0x1BAD	7085	1059
X20DC4395	0x1CC5	7365	1066
X20DI0471	0xE7CE	59342	1208
X20DI2371	0x1B8D	7053	1215
X20DI2372	0x22A7	8871	1221
X20DI2377	0x1B8E	7054	1227
X20DI2653	0x2544	9540	1235
X20DI4371	0x1B92	7058	1241
X20DI4372	0x22A8	8872	1248
X20DI4375	0xA911	43281	1254
X20DI4653	0x2545	9541	1265
X20DI4760	0x2105	8453	1271
X20DI6371	0x1B93	7059	1280
X20DI6372	0x1B94	7060	1286
X20DI6373	0xA7A2	42914	1292
X20DI6553	0x256F	9583	1298
X20DI8371	0xA4AB	42155	1304
X20DI9371	0x1B95	7061	1310
X20DI9372	0x1D28	7464	1317
X20DID371	0xC0E7	49383	1324
X20DIF371	0xC0E8	49384	1330
X20DM9324	0x20B9	8377	1338
X20DO2321	0x22B3	8883	1349
X20DO2322	0x1B96	7062	1357
X20DO2623	0x267B	9851	1365
X20DO2633	0xAC39	44089	1374
X20DO2649	0x20DA	8410	1390
X20DO4321	0x22B4	8884	1396
X20DO4322	0x1B97	7063	1404
X20DO4331	0x22B5	8885	1413
X20DO4332	0x1B9C	7068	1423
X20DO4529	0x20D9	8409	1433
X20DO4613	0xAD05	44293	1439
X20DO4623	0x267C	9852	1452
X20DO4633	0xAC3A	44090	1461
X20DO4649	0xA704	42756	1477
X20DO6321	0x1B99	7065	1483
X20DO6322	0x1B98	7064	1490
X20DO6325	0xE284	57988	1498
X20DO6529	0x2019	8217	1509
X20DO6639	0xDF50	57168	1515
X20DO8232	0xA4AD	42157	1521

Product ID	B&R ID code (hex.)	B&R ID code (dec.)	on page
X20DO8322	0xA4AC	42156	1532
X20DO8323	0xDF4E	57166	1539
X20DO8331	0x22EB	8939	1548
X20DO8332	0x1B9D	7069	1560
X20DO9321	0x1B9B	7067	1572
X20DO9322	0x1B9A	7066	1580
X20DOD322	0xC0E9	49385	1588
X20DOF322	0xC0EA	49386	1594
X20DS1119	0xA067	41063	1637
X20DS1319	0x2547	9543	1678
X20DS1828	0xAEC7	44743	1720
X20DS1928	0xA912	43282	1780
X20DS4387	0xA38E	41870	2777
X20DS4389	0xA93B	43323	1833
X20DS438A	0xCAC0	51904	2794
X20IF1020	0x1F27	7975	2181
X20IF1030	0x1F28	7976	2184
X20IF1041-1	0xA709	42761	2187
X20IF1043-1	0xA70B	42763	2191
X20IF1051-1	0xA70C	42764	2195
X20IF1053-1	0xA715	42773	2199
X20IF1061	0x1F22	7970	2203
X20IF1061-1	0xA716	42774	2206
X20IF1063	0x1F23	7971	2210
X20IF1063-1	0xA717	42775	2213
X20IF1065	0xA4C6	42182	2217
X20IF1072	0x1F20	7968	2220
X20IF1074	0xA399	41881	2176
X20IF1082	0x1F1F	7967	2224
X20IF1082-2	0xA7A3	42915	2230
X20IF1086-2	0xB455	46165	2236
X20IF1091	0x1F24	7972	2242
X20IF1091-1	0x2525	9509	2154
X20IF10A1-1	0xA718	42776	2245
X20IF10D1-1	0xA71B	42779	2249
X20IF10D3-1	0xA71C	42780	2253
X20IF10E1-1	0xA71D	42781	2257
X20IF10E3-1	0xA71E	42782	2261
X20IF10G3-1	0xA72C	42796	2265
X20IF10X0	0xC3B4	50100	2269
X20IF2181-2	0xC3B3	50099	2273
X20IF2772	0x1F25	7973	2279
X20IF2792	0x1F26	7974	2283
X20MM2436	0x26B5	9909	2318
X20MM3332	0xA982	43394	2338
X20MM4331	0xA976	43382	2353
X20MM4456	0xA177	41335	2366
X20PD0011	0x267D	9853	2858
X20PD0012	0x267E	9854	2862
X20PD0016	0x2680	9856	2866
X20PD2113	0x267F	9855	2871
X20PS2100	0x1BBF	7103	2884
X20PS2110	0x2016	8214	2889
X20PS3300	0x1BC0	7104	2900
X20PS4951	0x1F43	8003	2877
X20PS9400	0x1F8C	8076	784
X20PS9402	0xA389	41865	791
X20PS9500	0x2018	8216	848
X20PS9502	0xA38A	41866	854
X20SM1426	0x2681	9857	2387
X20SM1436	0x2682	9858	2432
X20XC0201	0x2563	9571	2160
X20XC0202	0x2564	9572	2160
X20XC0292	0xA252	41554	2160
X20cAI2438	0xE1EE	57838	199
X20cAI4622	0xE1EF	57839	362
X20cAI4632	0xE1F0	57840	373
X20cAI4632-1	0xD57A	54650	399
X20cAO2437	0xE1F2	57842	597
X20cAO2438	0xE211	57873	608
X20cAO4622	0xE212	57874	682
X20cAP3121	0xE214	57876	510
X20cAT4222	0xE215	57877	2969
X20cAT6402	0xDD57	56663	2979

Product ID	B&R ID code (hex.)	B&R ID code (dec.)	on page
X20cBC0083	0xE216	57878	747
X20cBC0087	0xD577	54647	753
X20cBC0088	0xE67F	59007	759
X20cBC00E3	0xE4E0	58592	764
X20cBC1083	0xE217	57879	2125
X20cBC8083	0xE218	57880	2132
X20cBC8084	0xDF10	57104	2138
X20cBR9300	0xDD48	56648	815
X20cBT9100	0xE219	57881	821
X20cCP1584	0xE21B	57883	1185
X20cCP1586	0xE21C	57884	1185
X20cCP3584	0xE21D	57885	1189
X20cCP3586	0xE21E	57886	1189
X20cCS1020	0xE7F2	59378	1949
X20cCS1030	0xE500	58624	1992
X20cDC1198	0xE501	58625	908
X20cDC1396	0xE502	58626	961
X20cDC2395	0xE503	58627	1008
X20cDI4371	0xE21F	57887	1241
X20cDI4375	0xE220	57888	1254
X20cDI4760	0xE221	57889	1271
X20cDI6371	0xE222	57890	1280
X20cDI6372	0xE223	57891	1286
X20cDI9371	0xD574	54644	1310
X20cDI9372	0xE224	57892	1317
X20cDM9324	0xE225	57893	1338
X20cDO2633	0xE680	59008	1374
X20cDO4322	0xE226	57894	1404
X20cDO4332	0xE227	57895	1423
X20cDO4633	0xE67D	59005	1461
X20cDO4649	0xE67E	59006	1477
X20cDO6321	0xE228	57896	1483
X20cDO6322	0xE229	57897	1490
X20cDO6639	0xE22A	57898	1515
X20cDO8331	0xE22B	57899	1548
X20cDO8332	0xE22C	57900	1560
X20cDO9321	0xE22D	57901	1572
X20cDO9322	0xD578	54648	1580
X20cDS1119	0xE20D	57869	1637
X20cIF1030	0xE233	57907	2184
X20cIF1041-1	0xE505	58629	2187
X20cIF1061-1	0xE234	57908	2206
X20cIF1063-1	0xE235	57909	2213
X20cIF1072	0xE506	58630	2220
X20cIF1082-2	0xE236	57910	2230
X20cIF10D3-1	0xE237	57911	2253
X20cIF10E3-1	0xE238	57912	2261
X20cIF10X0	0xE239	57913	2269
X20cIF2181-2	0xE23A	57914	2273
X20cPD2113	0xE23B	57915	2871
X20cPS2100	0xE23C	57916	2884
X20cPS2110	0xE23D	57917	2889
X20cPS3300	0xDF13	57107	2900
X20cPS9400	0xD579	54649	784

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